July 1992

M68HC705L2PGMR PROGRAMMER BOARD

(REVision A PWBs only)

APPLICATION NOTE

1. INTRODUCTION

This application note describes the technique used to program and verify the MC68HC705L2 microcontroller (MCU) internal OTPROM/EPROM, and how to construct the programmer board (PGMR) used in conjunction with this application note. All that is required to program the 705L2 is the PGMR and a +5 volt and V_{PP} dc power supply.

2. PROGRAMMING TECHNIQUE

The PGMR programming technique (see section 4) allows the user program, contained in an external EPROM, to be copied into the internal PROM (OTPROM/EPROM) of the MCU device.

The 705L2 MCU device is inserted into the PGMR. The applicable program/verify routine is selected via jumper JP1, and power is applied to the PGMR via switch S1. The MCU is taken out of reset and placed in the run mode via switch S2, and MCU control is transferred to the bootstrap ROM. The selected programming routine is then executed.

2.1 PROGRAM AND VERIFY

The Program and verify mode setting requires jumper JP1 to be set to the 'PROGRAM' position.
In the program and verify MCU PROM routine, the contents of an external 16K or 32K EPROM are copied into the MCU PROM (EEPROM - C4) areas of the applicable device. There is a direct correlation of addresses between the two devices (MCU and external EPROM). Non-MCU PROM addresses are ignored so data contained in those areas are not accessed. Unprogrammed external EPROM address locations should contain $00 to speed up the programming operation. During the programming routine, the PROGRAM LED D2 is illuminated. At the end of the programming routine, D2 is turned off, and the verification routine is entered. If the contents of the MCU PROM and external EPROM exactly match, then the VERIFY LED D3 is illuminated.

During the verification routine, all locations are compared to the data residing in external EPROM. The verification routine will stop if a discrepancy has been detected and the error address location will be placed on the external memory address bus.

2.2 VERIFY MCU

The verify mode settings requires jumper JP1 to be set to the 'VERIFY' position.
The verify MCU PROM contents routine is normally entered automatically after the MCU PROM is programmed. Direct entry of this mode will cause the MCU PROM contents to be compared to external EPROM contents residing at the same address locations. Both D2 and D3 LEDs are turned off at this time until verification is completed. Upon completion of the verification routine (every location verified) the VERIFIED LED D3 is illuminated. If D3 does not illuminate, a discrepancy has been detected and the error address location will be placed on the external memory address bus.

NOTE

MCU PROM blank checking can be accomplished by placing $00 into the locations of the external EPROM that map those of the MCU PROM. The above verify MCU routine will then verify that the device is blank.

3 PROGRAMMING MODULE PREPARATION

The PGMR must be prepared/configured prior to any program/verify operations. Board preparation consists of the external power source (+5V and V_{PP}), EPROM installation and Jumper selection configuration.

3.1 EXTERNAL POWER SOURCE

Power connector P1 is used to connect an external power supply to the PGMR. A +5 Vdc @ 100 mA power source is connected to connector P1 pins labeled +5V and GND. The programming voltage power source is connected to pins labeled V_{PP} and GND. Refer to the specific device data sheet for programming voltage (V_{PP}) specifications.

NOTE

The programming voltage (V_{PP}) must be measured at SKT U2 pin 3 during programming cycle (D2 PROGRAM LED illuminated).

3.2 EPROM INSTALLATION

The basic EPROM device used on the PGMR (at location U4) is a 27128 or 27256, 16K or 32K EPROM, 28-pin device. This EPROM device contains the user code to be programmed into the applicable PROM MCU device.

3.3 DIP PGMR CONFIGURATION

For the shrink dual-in-line package (SDIP) device programming, the PGMR printed wiring board (PWB) must be fabricated with a SDIP zero-insertion-force (ZIF) socket located at SKT U1, or a low-insertion-force (LIF) socket located at SKT U2.

4 PROGRAMMING OPERATION

To program the 705L2 MCU, perform the following steps:

1. Place switch S1 to POWER-OFF (left) position.
2. Install MCU and EPROM devices into PGMR.
3. Place switch S2 to RESET-IN (left) position.
4. Select appropriate setting for JP1 (As outlined in the initial part of this document).
5. Place switch S1 to POWER-ON (left) position.
6. Place switch S2 to RESET-OUT (right) position.

   PROGRAM LED illuminates signifying programming sequence being performed. VERIFY LED illuminates signifying verification is completed.
7. Place switch S2 to RESET-IN (left) position.
8. Remove power (via S1), or select and run new routine.

5 PROGRAMMER BOARD CONSTRUCTION

The PGMR is a two-sided Printed Wiring Board (PWB). Table 1 provides the parts list for the PGMR. Component tolerances are generally not critical. Use of Integrated Circuit (IC) or Zero Insertion Force (ZIF) sockets are recommended for both EPROM and MCU devices located at SKT U1, U2 and U4. This will simplify the removal and installation of both devices. Figure 1 is the schematic diagram for the PGMR board.

TABLE 1 - PGMR Parts List

REFERENCE DESIGNATION	COMPONENT DESCRIPTION
C2,C3	Capacitor, 47uF @ 35 Vdc
C1,C6,C7,C8,C9, C10,C11	Capacitor, 0.1uF @ 50 Vdc
C4,C5	Capacitor, 22pF @ 50 Vdc
D1	Diode, 1N4735
D2,D3	LED, HP # HLMP-4700 or equivalent (RED)
JP1	Header, 3-pin, single row, 3M #929450-01-30
P1	Power connector, Augat # RDI 2SV-03
R1	Resistor, 10M, 1/4W, 5%
R4,R6	Resistor, 10K, 1/4W, 5%
R7,R8	Resistor, 470 1/4W, 5%
R5	Resistor, 100K, 1/4W, 5%
R2, R3	Resistor, 51, 1/4W, 5%
U3	I.C., MC74HC393
S1, S2	Switch, DPDT, Augat ALCO # MHS223
SKT U4	Socket, DIP, 28-pin LIF, Welcon # 613-7280316
SKT U2	Socket, SDIP, 42-pin LIF, Yamaichi IC85-4206-G4
SKT U1	Socket, SDIP, 42 pin ZIF, Textool
Y1	1 MHz crystal or ceramic resonator
Jumper	For JP1 - shorting link

Figure 1 - PGMR Schematic Diagram

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com