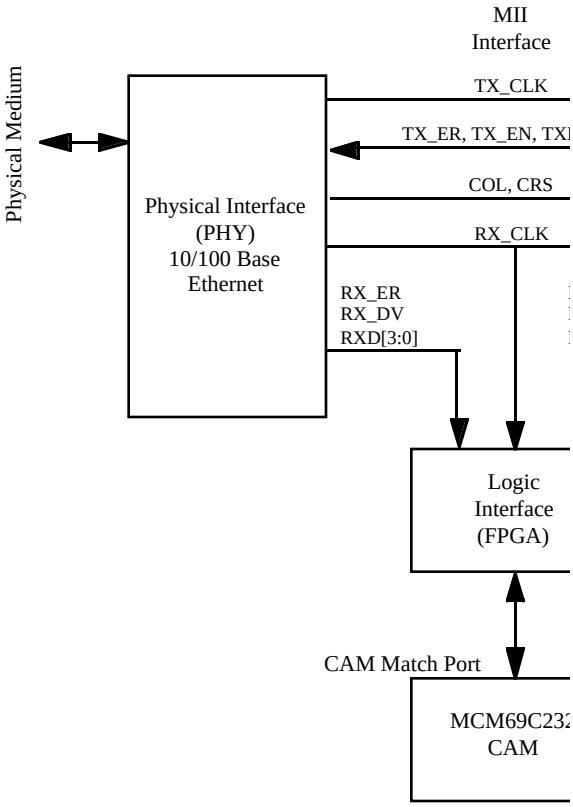
6. System Block Diagram



The FPGA uses several signals of both the CA
between the MPC860T and the CAMs' contro
application note: MPC860SAR Microprocesso
on the internet at: http://www.mot.com/netco

However, there is one major difference from t
Interface Example application and this paper,
control port operations. It may be desirable to
control port access. The 860s' chip select opti
externally generated cycle termination. The C
through the FPGA to provide the 860 with a o
meets the 860s' setup and hold times.

Using Motorola's Fast Sta
MPC860T's Media In

Roy Bieda, FAE, Mot
Jim Soroka, FAE,

1. Introduction

Not too long ago we were happy to have a 10
computer. However, given the growing popu
find ourselves needing even more bandwidth.
bandwidth we need without the need to rewire

Motorola's new MPC860T Fast Ethernet Com
version of the MPC860 PowerQUICC™ famil
capabilities, the MPC860T includes an additio
handling 10/100Mbps operation. This makes
routers/bridges.

The transition from 10Base to 100Base Ethern
differences. Given the relatively low data rate
bridge applications was often performed by th
rate of 100Base Ethernet doesn't allow the hos
reject frames. There is a need to implement a
This need can be filled by the addition of a Co
860T's Ethernet Media Access Controller (MA

The operation of a router or bridge would be t
address obtained from an incoming frame. Th
indicate to the MAC if the incoming address w
acceptance or rejection of the frame.

Although CAMs have been available for years
their use. The MCM69C232 CAM addresses
CAM technology. By combining logic with fa
is able to produce cost-effective, fast, and dee
and the MCM69C432 is a 16k x 64 CAM.

2. Purpose

The purpose of this note is to illustrate the con
CAM would exist between the Physical Interfa
860T's MAC has an industry standard interfac
Interface. What is needed is a single logic dev
PHY connection and signal the 860T to accep
easily implemented in a FPGA. We will discu

3. Media Independent Interface Descr

The Media Independent Interface is a standard
860T and the physical layer interface. The MI
path interface that runs at 25 MHz for a 100 M
networks.

The MII receive clock is generated by the PH
pin. The data from the PHY on RXD[3:0] is
RX_CLK. The receive process is started whe
for the entire receive frame length.

In order to support external CAM address filte
to gate the RX_DV signal generated by the PI
generated by the FPGA for the 860T. The FP
the CAM, will negate RX_DV_860T. The 86
frame and subsequently discard the frame. Th
time it takes to receive 64 bytes.

Relevant Signals:

Pin Name	Pin Function	Type	
RX_CLK	Receive Clock	Input	
RXD[3:0]	Receive Data	Input	
RX_DV	Receive Data Valid	Input	
RX_ER	Receive Error	Input	

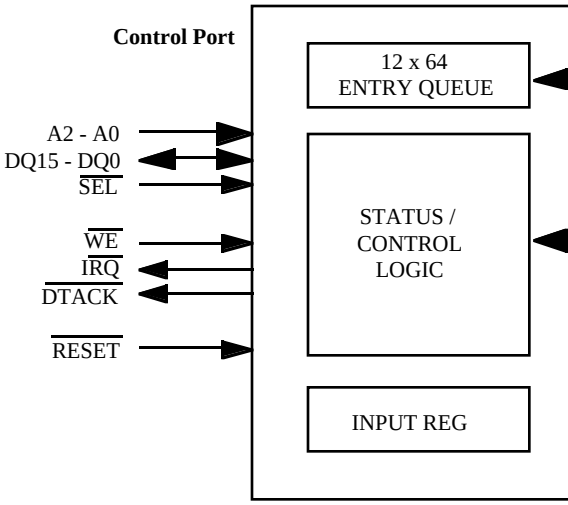
4. CAM Description

In its basic operating mode, the MCM69C232
all the entries in its CAM table. Whether a ma
after the comparisons have been made. If a ma
data associated with the matching entry is out
MQ bus remains in a high impedance state to
multiple CAMs.

The CAM is prepared for match operations by
the control port. Since we are only interested
the global mask to ignore 16 bits of the 64 bit

Relevant Signals:

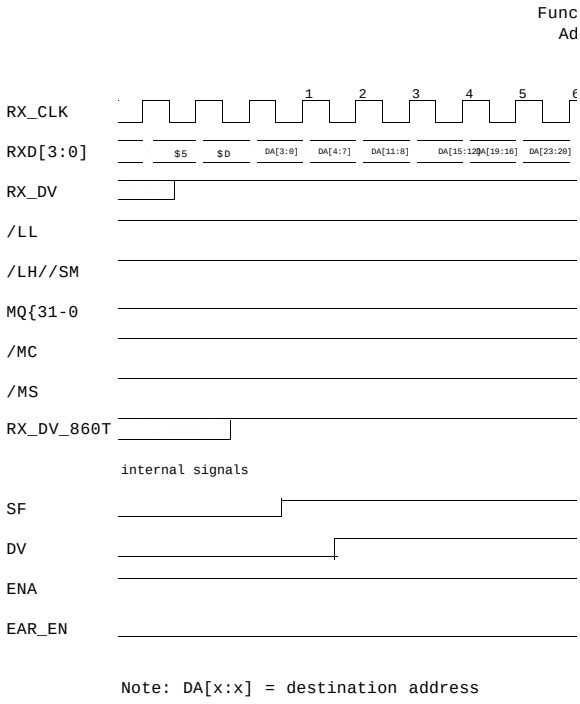
Pin Name	Pin Function	Type	
/LH//SM	Latch High / Start Match	Input	
/LL	Latch Low	Input	
/MC	Match Complete	Output	
/MS	Match Successful	Output	
MQ31 - MQ0	32-bit common I/O CAM data	Input / Output	



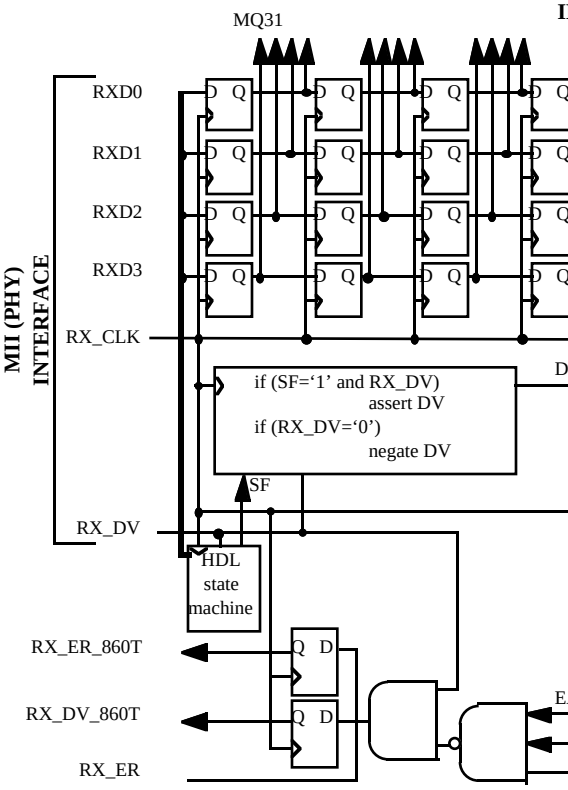
MCM69C232 CAM

An initial rising edge of the SF signal indicate
RXD[3:0] pins. The destination address, 48 b
bits per clock, and then presented to the CAM
signals. The /LH//SM signal then starts the m
then respond with MC and if the destination a
assert. The FPGA then signals rejection of the
signal.

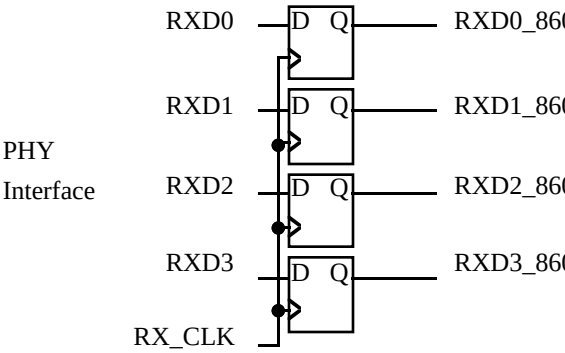
9. Simulation Diagram for Match Su



7. Logic Interface Diagram



The process of gating the RX_DV signal to th
clock delay. The following circuit is used to e
phase with the one RX_CLK delayed RX_DV



RX_DV	EAR_EN	/MC	/I
0	X	X	
1	0	X	
1	1	1	
1	1	0	
1	1	0	

8. Operation of the Logic Interface

Receive data from the PHY is continuously cl
RX_CLK signals. RX_DV is used to indicate
the RXD[3:0] signals. RX_DV remains asser
driven on RXD[3:0]. RX_DV, when negated

It will be necessary to detect a start of frame (S
destination address within the FPGA and pres
preamble bit pattern of one or more 0101 ($5)
signifies the start of frame (destination addres
language (HDL) can be used to detect the star
only a three flipflop state machine:

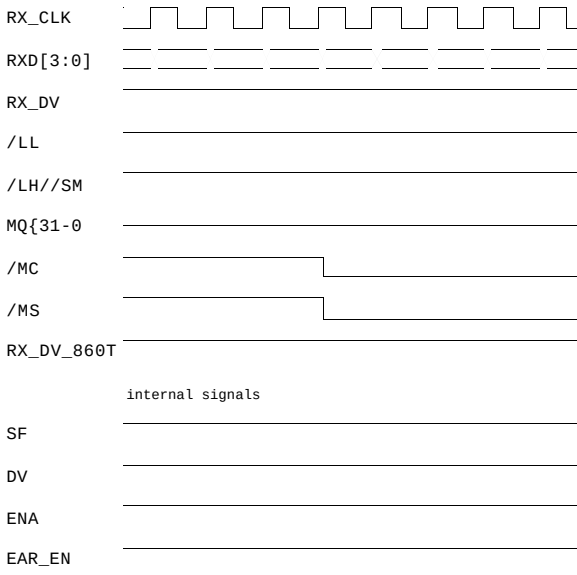
```
entity SAMPLE is
      port(
RX_CLK:     in std_logic;
RX_DV:      in std_logic;
RXD_bus:    in std_logic_vector(3 do
SF          out std_logic;
);
end SAMPLE

architecture archSAMPLE of SAMPLE is
      type OPERATINGSTATE is (Idle,
      signal OPState:   OPERATINGSTA
begin
      process (SCLK)
      begin
            if SCLK'Event and SCLK =
             case OPState is
                  when Idle =>
                   if RX_DV = '1' an
                    OPState <= Got5;
                   endif;

                  when Got5 =>
                   if RX_DV = '0' th
                        OPState <= I
                        SF <= '0';
                   elsif Data = "110
                    OPState <= GotD;
                    SF <= '1';
                   elsif Data /= "01
                    OPState <= Idle;
                   end if;

                  when GotD =>
                   if RX_DV = '0' th
                        OPState <= I
                        SF <= '0';
                   end if;
             end case;
            end if;
      end process;
end archSAMPLE;
```

Motorola's MPA1016, the smallest and lowes
FPGA family.

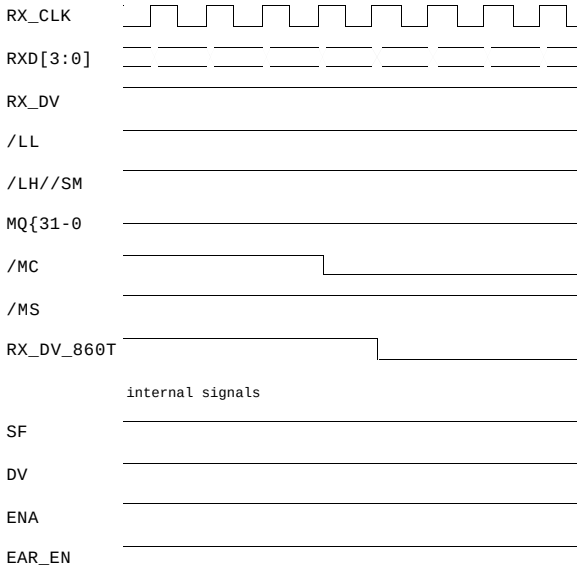
11. References

1. MCM69C232 4Kx64 CAM, Motorola Inc
2. MPC860T Fast Ethernet Controller, Moto

F



F



10. Summary

With the addition of the MPC860T to Motorol
controllers, coupled with Motorola's advent o
opportunities to build faster and more cost eff
small amount of logic makes it is easy to inter
860T/PHY Ethernet interface. The logic can b