

MPC860

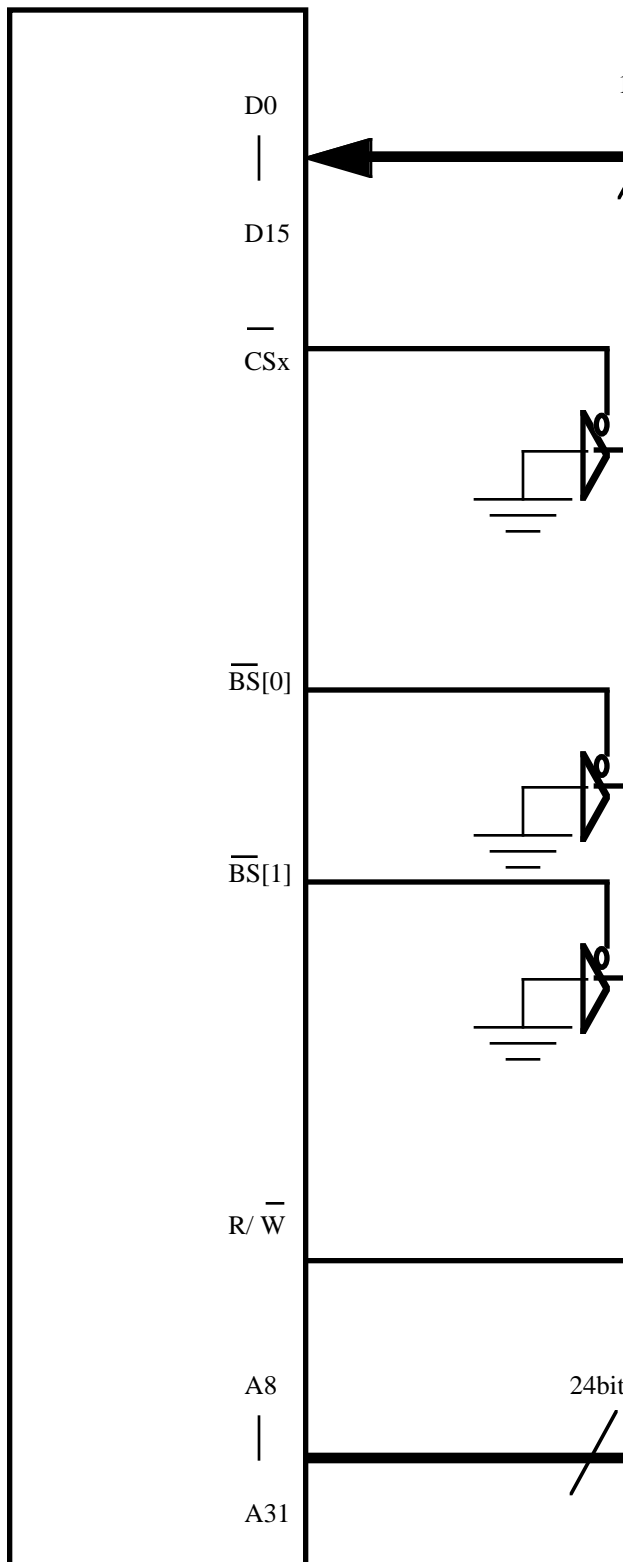


Figure 1. MPC860

MPC860 and MC68302 A

The main point of this document is to show the interface between an MPC860 and an MC68302. Within the MPC860 can be adjusted to allow for different bus speeds. For the purpose of this document, the following is assumed:

- Interface is between a 40MHz MPC860 and an MC68302.
- The MC68302 external master internal slave mode is used. (Please see Figures 6-17 and 6-18 of the MC68302 manual.)
- Transaction between the two chips is unidirectional. The 302 is the slave.
- MC68302 is a 16 bit port size that is defined by the PS(0:1) bits.
- MC68302 stores its serial data in its dual ported memory.
- The MPC860 user programmable machine select register is used for proper timing of the signals.
- General purpose lines available from the MPC860 can be programmed to behave like bus signals.

Programming the Option, Mode and Base Registers

The option and base registers of the MPC860 are used to configure the type of interface. Within the option register, the PS(0:1) bits according to the timing of the MC68302. Within the base register, bit 23 and bit 24 must be programmed for a 16 bit port size. For more information, see been appended from section 15 of the MPC860 manual.

Table 15-14

Bits	Mnemonic	Description
20-21	PS(0:1)	Port Size. This field specifies the memory region selected for the memory operations handling.
24-25	MS(0:1)	Machine Select. This field specifies the machine selected for the memory operations handling.
31	V	Valid Bit. This bit indicates that the bits of the base register pair are valid. If this signal does not assert, this bit is set. Note: An access to the memory does not have the valid bit set because a bus monitor is active. Following a system reset, this bit is set in BR0.

Table 15-15.

Bits	Mnemonic	Description
23	BI	Burst Inhibit. This attribute decid not this memory ba burst accesses. In case, the memory (drives the BI signal accessing this men Following a system bit is set in OR0.

Table 15-16. Mac

Bits	Mnemonic	Description
8	PTAE	Periodic Timer A I This bit allows the p A to request servic Following a system PTAE bit is reset.

Programming the Signals for a Suc Interface

For this interface, the MPC860 signals a MC68302. With examination of the timing s needed by the MC68302, the MPC860 can c The active low MPC860 chip select signal strobe. The chip select's assertion can be ir emulate the MC68302 bus operation. Bec: other MPC860 signal, it makes programming The active low signals BS[0] and BS[1] ca data strobe signals of the MC68302. Thes because they can be programmed using the general purpose signal.

The read/write signal of the MPC860 can di the MC68302. The timing is not a proble directly after the transfer start signal. BS[0] the upper half of the data bus.

In Figure 1-1 the interface between the two | buffers. These buffers ensure that more without creating bus contention (for five volt MC68302 is used, the three-state buffers a that a pull up resistor is connected to each when there is no activity taking place. They negation times.

DTACK* and IAC signals are not used ir internally by the MC68302 after a known nu debugging output to tell if the MC68302 is

timing of the DTACK* signal is the cycle interface with a MC68302 three wait state push the number of MPC860 clocks neede wait states+ 4 clocks] = 14). This interface Although only eight entries are available for burst read and write entries can be used in loop function can also be used to reduce th this application note for clarity. Knowledge the MPC860 and MC68302 enables the us read or write cycle appropriately.

The MC68302 SCC's store all data in the in is appropriate for low speed serial chann possible for the MC68302 to obtain bus mas is outside of the scope of this document.

A copy of the UPM programming for this inte