TN00205

MPC5746R Delayed crystal start-up

Rev. 1.0 — 24 March 2026 **Technical note**

Document information

Information	Content
Keywords	MPC5746R
Abstract	This document supplements erratum ERR052283 by providing additional details around the root cause and corrective action.

1 Preface

This document supplements erratum ERR052283 by providing additional details around the root cause and corrective action.

2 Failure Mode and Impact

The failure mode identified affecting the MPC5746R microcontroller is a delay in the crystal start-up time that exceeds the datasheet maximum of 5ms. The unexpected additional delay can only be seen at power up of the microcontroller entered from a power down condition. Start-up times vary drastically from silicon to silicon and from module to module. Start-up times can measure up to 800ms in some cases. The occurrence of this issue is not repeatable in that any one piece of silicon will never fail 100% of the time. Factors that affect the failure rate are:

- Temperature – failure rate is highest around 10-20C with no failures identified above 40C
- Module – subtle differences between module parasitics, power supply ramp rates and quality of ramp affects the occurrence probability
- Silicon – The failure rate varies across the fab normal process window

Conclusion:

Not every device is expected to fail on every or any module. Just the right piece of silicon needs to be mounted to just the right module for the failure to occur.

The **failure rate** recorded from an impacted application was **2,850 PPM** and due to the temperature sensitivity of the failure mode, failures accumulated around the colder months of the year.

In the application, the MPC5746R can be configured to enable the crystal oscillator at start up via a DCF record (UTEST_MISC.XOSC_EN =1). As a result of the delayed crystal start-up, after reset negation, the Boot Assist Flash (BAF) code will execute and monitor the status of the crystal. If the crystal does not start before the Software Watchdog Timer (SWT) expires, a reset will be asserted. The overall impact of this unexpected reset at power up is application dependent.

3 Root Cause

The delayed crystal start-up is ultimately due to a connection of the external oscillator (XOSC) IP block to a signal of the incorrect polarity called Core_V_Detect. This signal, which is powered by the 5V PMC supply voltage, is used to tell the IP block when the 1.2V core supply voltage to the device is present. In its current implementation, if the signal is low, the XOSC IP interprets this as the 1.2V core supply is present and if high this means the core voltage is not present. This introduces the impact of the ramp sequence of the various power supply pins of the device. Ideally, the XOSC IP should remain in a static state i.e nonfunctional state until all supplies are within their specified tolerances. However, given the incorrect logic level of the Core_V_Detect signal used by the XOSC IP, the XOSC is allowed to function even before the 5V and 1.2 supplies are powered. This means that when the VDD_HV_IO_JTAG power pin, which is the high voltage supply into the XOSC, ramps before the VDD_HV_PMC supply, the XOSC is allowed to respond to input control signals that are not properly driven at this time. This results in current paths being unexpectedly open within the XOSC IP specifically into the Automatic Level Control (ALC) circuit. Inside the ALC, there is a capacitor that receives and stores this unexpected charge which results in the XOSC thinking that the EXTAL input to the microcontroller is too high and therefore shuts off any current going out to the crystal. The charge upon this capacitor has no direct path of discharge during this time frame and therefore will only deplete its charge through the effects of leakage hence the reason for the variable amounts of time observed to start the crystal. Figure 1 shows the problematic power ramp sequence.

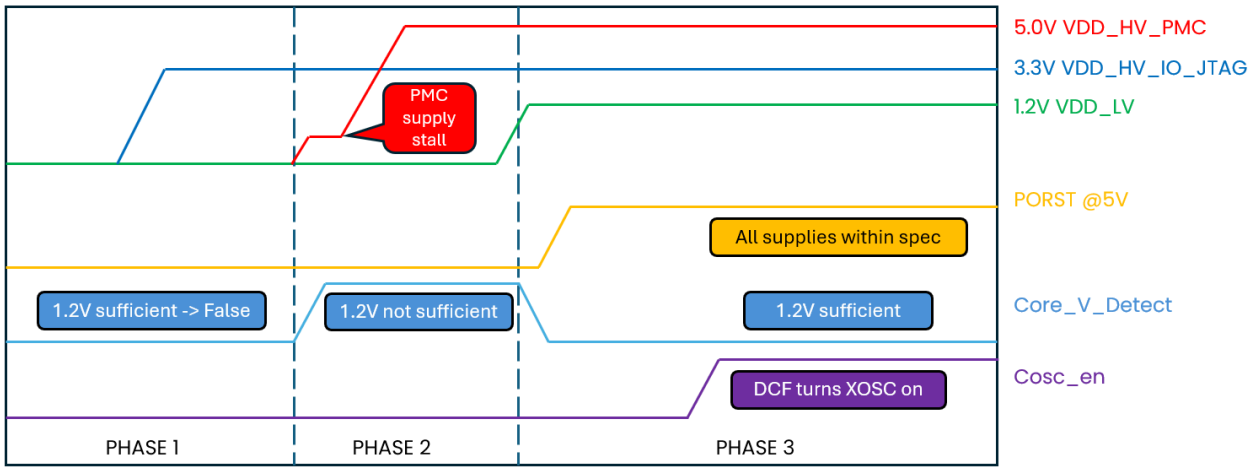

Figure 1. Power ramp sequence

During PHASE 1 in Figure 1, the XOSC IP is powered yet the Core_V_Detect signal is low indicating that the IP is allowed to function. However, due to the fact that the other supplies are not present, it is not defined as to what the XOSC IP is supposed to do. During PHASE 1, charge is injected into the ALC cap and is held such that when the device comes out of reset, reads the DCF record to turn on the crystal, it cannot do so until the charge has naturally depleted enough to allow the XOSC IP to start driving current to the crystal. At hotter temperatures, internal leakage allows the charge to dissipate more quickly thus no failures are observed.

Simulations and silicon validation performed by NXP confirms the failure mode of non-deterministic crystal behavior when exposed to particular power ramp profiles. The issue is sensitive to a power ramp stall of the VDD_HV_PMC supply. It was found that that if this supply stalled, particularly around the 1.2V range, the level shifters inside the XOSC IP would respond incorrectly to incoming signals and would therefore provide nondeterministic output signals to the rest of the logic. In simulations, this voltage level varied with silicon process and temperature. Hence the reason the erratum workaround provides for voltage conditions for the VDD_HV_IO_JTAG and the VDD_HV_PMC supplies. Once the VDD_HV_PMC supply reaches 3V, the PMC logic is given sufficient power and can then drive the Core_V_Detect signal high effectively tri-stating the level shifters inside the XOSC IP. This will guarantee that the level shifters operate in an expected fashion as the power into the XOSC IP is ramping (VDD_HV_IO_JTAG) and no unexpected current paths will be enabled.

4 Workaround

The issue can be completely avoided using hardware or software strategies. Below is a summary of the workarounds provided in the erratum which can be referred to for further detail.

1. Hardware – Ramp the VDD_HV_PMC supply before the VDD_HV_IO_JTAG. This will effectively safe state the XOSC IP during power up preventing any unexpected charge from entering the block.
2. Software – Disable the ALC. If the ALC is disabled via the UTEST_MISC DCF record, this will enable pull down devices and immediately discharge the capacitor allowing the XOSC IP to effectively provide current to the crystal to begin oscillating.
3. Software – If the ALC must be used in the application, then programming a series of DCFs that force the ALC and the XOSC into a disabled state first will discharge the capacitor. Then a subsequent DCF to enable the ALC and the XOSC can be made to start the crystal.

5 Summary

The delayed crystal start-up has been confirmed possible to exist in specific applications and this is backed up and fully understood from a design perspective. The occurrence rate can be very high if just the right conditions

as described earlier in this document are provided. Effective workaround solutions have been provided to avoid this issue.

6 Revision history

Table 1. Revision history

Document ID	Release date	Description
TN00205 v.1.0	24 March 2026	Initial release

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