Save power and space with I²S-input Class-D audio amplifier

This small, mono digital-input Class-D audio amplifier delivers up to 3.4 W of power. It has ultra-low quiescent power consumption (6.5 mW), minimizes RF susceptibility, and is optimized for low-power portable and mobile applications.

Key features
- Dynamic Power Stage Activation for high efficiency and ultra-low quiescent power consumption (6.5 mW; f_s = 32 kHz)
- Low RF susceptibility
- Input-clock jitter insensitive
- Maximum RMS output power:
  - 1.4 W into 4 Ω at 3.6 V power supply (THD = 1%)
  - 2.7 W into 4 Ω at 5.0 V power supply (THD = 1%)
  - 3.4 W into 4 Ω at 5.0 V power supply (THD = 10%)
- Power supply voltage from 2.5 to 5.5 V
- Left / right selection
- Industry-standard 3-wire I²S audio format interface
- Automatic power-down when I²S signal is not present
- Optional control tokens embedded in the audio stream can control:
  - Three gain settings: -3, 0, or +3 dB
  - Slope control for EMI reduction
  - Clip control for smooth clipping
- Short power-up time: 4 ms
- Short power-down time: 5 µs
- 1.8 / 3.3 V tolerant digital inputs
- ‘Pop noise’ free during all mode transitions
- Output noise voltage (A-weighted): 24 µV
- Only two external components required

Applications
- Mobile phones
- Portable navigation devices (PNDs)
- Portable gaming devices
- PDAs / tablets
- MP3 players / PMPs

Ordering information
- TFA9882UK
- Package: WLCSP9
- Dimensions: 1.27 x 1.49 x 0.6 mm
- 12NC tape & reel: 9352 913 83118

The NXP TFA9882 is built for mobile phone and portable applications. This small, mono device has an industry-standard I²S audio interface that simplifies design by eliminating the need for a D/A converter in the host processor.
The TFA9882 uses NXP’s unique Dynamic Power Stage Activation (DPSA) technology to achieve best-in-class low quiescent power consumption (6.5 mW). DPSA scales the output transistors to match the current demands of the output signal, ensuring that the power stage operates very efficiently under all circumstances. The device is capable of delivering a high output power of 3.4 W with 90% efficiency.

The TFA9882 automatically powers down when the I²S signal is not present. This eliminates the need for extra control pins.

Optional control tokens embedded in the audio stream can be used to control, gain, clip behavior, and output slope. Controlling the output slope reduces the radiated emission by a factor of 10 dB.

The second-order closed-loop architecture, combined with sophisticated built-in D/A-conversion, provides excellent audio performance with a Signal-to-Noise Ratio (S/R) of 103 dB and a high Power Supply Rejection Ratio (PSRR) of 85 dB. The digital interface assures low RF susceptibility in the device and the total system, and low sensitivity to input-clock jitter.

The TFA9882 is offered in a 9-bump Wafer Level Chip Scale Package (WLCSP) that measures only 1.27 x 1.49 x 0.6 mm and has a pitch of 0.4 mm.

### TFA9882 block diagram

![TFA9882 block diagram](image)

### Operating characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDP</td>
<td>Power supply voltage</td>
<td>Operating mode with load; $V_{DDP} = 3.6$ V, $f_s = 32$ kHz</td>
<td>2.5</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VDDD</td>
<td>Digital supply voltage</td>
<td>Power-down mode</td>
<td>1.65</td>
<td>1.8</td>
<td>1.95</td>
<td>V</td>
</tr>
<tr>
<td>IDDP</td>
<td>Power supply current</td>
<td>Power-down mode</td>
<td>1.38</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IDDD</td>
<td>Digital supply current</td>
<td>Power-down mode</td>
<td>0.1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$P_{(RMS)}$</td>
<td>RMS output power</td>
<td>Operating mode; $f_s = 32$ kHz</td>
<td>0.85</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power-down mode</td>
<td>2.5</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4 \Omega; 3.6$ V (THD = 1%)</td>
<td>1.4</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4 \Omega; 5$ V (THD = 1%)</td>
<td>2.7</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4 \Omega; 5$ V (THD = 10%)</td>
<td>3.4</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total harmonic distortion-plus-noise</td>
<td>$4 \Omega; P_{(RMS)} = 100$ mW, $3.6$ V</td>
<td>0.03</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>$V_{(RMS)} = 200$ mV, $f_s = 217$ Hz</td>
<td>85</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>S/R</td>
<td>Signal-to-noise ratio</td>
<td>$V_{DDP} = 5$ V, $V_{(RMS)} = 3.4$ $V_{DDP}$ A-weighted</td>
<td>103</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$\eta_{po}$</td>
<td>Output power efficiency</td>
<td>$P_{(RMS)} = 1.4$ W, $4 \Omega; 3.6$ V</td>
<td>90</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>V_{(out)}</td>
<td>Output noise voltage</td>
<td>A-weighted</td>
<td>24</td>
<td></td>
<td></td>
<td>μV</td>
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</table>