

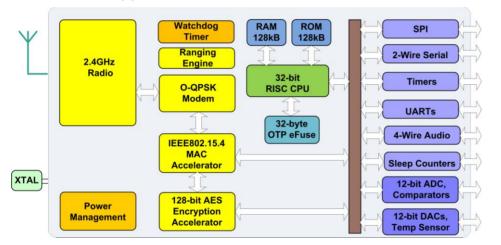
Product Brief – JN5148 Single Chip JenNet, ZigBee PRO and IEEE802.15.4 Solution

Overview

The JN5148 is an ultra low power, high performance wireless microcontroller targeted at low-power wireless networking applications. The device features an enhanced 32-bit RISC processor offering high coding efficiency through variable width instructions, a multi-stage instruction pipeline and low power operation with programmable clock speeds. It also includes a 2.4GHz IEEE802.15.4 compliant transceiver, 128kB of ROM, 128kB of RAM, and a rich mix of analogue and digital peripherals. The large memory footprint allows the device to run both the networking stack and an embedded application or in a co-processor mode. The operating current is below 18mA, allowing operation direct from a coin cell.

Enhanced peripherals include low power pulse counters running in sleep mode designed for pulse counting in AMR applications and a 4-wire I²S audio interface to interface directly to mainstream audio CODECs as well as conventional MCU peripherals.

Product and Support Overview



Benefits

- Single chip integrates transceiver and microcontroller for wireless sensor networks
- Small memory footprint
- Large memory footprint to run ZigBee PRO together with an application Co-existence with Wi-Fi and Bluetooth
- Very low current solution for long battery life
- Highly featured 32-bit RISC CPU for high performance and low power
- System BOM is low in component count and cost
- Extensive user peripherals

Applications

- Robust and secure low power wireless applications
- ZigBee PRO and JenNet networks
- Utilities metering (e.g. AMR)
- Home and commercial building automation
- Location Aware services eg Asset Tracking
- Industrial systems
- Telemetry
- Remote Control
- Toys and gaming peripherals

Features: Transceiver

- 2.4GHz IEEE802.15.4 compliant
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- 500 & 667kbps data rate modes
- Integrated sleep oscillator for low power
- On chip power regulation for 2.0V to 3.6V battery operation
- Deep sleep current 100nA
- Sleep current with active sleep timer 1.25µA
- <\$0.50 external component cost
- Rx current 17.5mA
- Tx current 15mA
- Receiver sensitivity -95dBm
- Transmit power 2.5dBm

Features: Microcontroller

- 32-bit RISC CPU, 4 to 32MHz clock speed
- Low power operation
- Variable instruction width for high coding efficiency
- Multi-stage instruction
 pipeline
- 128kB ROM and 128kB RAM for bootloaded program code
- JTAG debug interface
- 4-input 12-bit ADC, 2 12-bit DACs, 2 comparators
- 3 application timer/counters
- 2 UARTs
- SPI port with 5 selects
- 2-wire serial interface
- 4-wire digital audio interface
- Watchdog timer and Poweron-Reset circuit
- Up to 21 DIO

Industrial temp (-40°C to +85°C) 8x8mm 56-lead Sawn QFN Lead-free and RoHS compliant



Battery Life Optimisation

To maximise battery life, the JN5148 supports a number of power management and sleep modes. These include ultra low power sleep modes and reduced CPU clock speeds down to 4MHz. Used effectively, these will allow a battery's life expectancy for a typical remote sensing application, to be of the order of a few years.

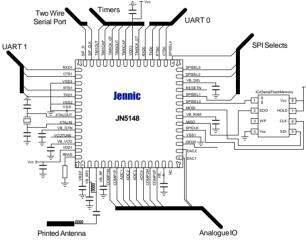
Power Saving Mode	Typical Current
Deep sleep	0.12µA
Sleep: wakeup on I/O or timer event	1.25µA
Sleep: wakeup on I/O or timer event and 128kB RAM retained	3.45µA

Wireless Networking Protocol Stacks

The IEEE802.15.4 MAC and elements of the wireless networking stacks are included in the device ROM. The JN5148's combined memory footprint of 256kB and its efficient code usage ensure that it supports a full JenNet and ZigBee PRO stack with sufficient code space to implement the application as well. Supported protocols include IEEE802.15.4, ZigBee PRO and NXP's proprietary stack, JenNet. Custom ROM masks will support the integration of user code into ROM giving cost reduction for higher volume applications.

Example Application Diagram

The JN5148 device requires a minimum of external components to support wireless applications; a crystal, serial flash memory, some decoupling components and printed antenna are all that is required for the lowest cost bill of materials and smallest size.



Evaluation Kits

To assist users with the development of wireless sensor networks, NXP provides a series of Evaluation Kits.

These contain everything that is needed to carry out product development and test, and include controller and sensor boards and a Software Developer Kit (SDK).

The SDK provides a comprehensive suite of tools to facilitate the development of application code. The kit includes a C compiler, graphical and text debuggers, assembler, linker and flash programmer. Libraries are supplied for the supported network stacks, the chip peripheral interface and also a simple Application Programming Interface (API) to drive the peripherals on the controller and sensor boards. These, combined with the many example applications provided on the website, ensure that designers can take products to market easily and quickly.

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