88W8977

2.4 GHz/5 GHz Dual-band 1x1 Wi-Fi 4® and Bluetooth® 5 Combo SoC

Rev. 1 — 13 July 2020 Product short data sheet

1 Product overview

The 88W8977 System-on-Chip (SoC) is a highly integrated single-chip solution that incorporates both Wi-Fi® (2.4/5 GHz) and Bluetooth® technology. The System-on-Chip (SoC) provides both simultaneous and independent operation of the following:

- IEEE 802.11n compliant, 1x1 spatial stream with data rates up to MCS7 (150 Mbps)
- Bluetooth 5 (includes Bluetooth Low Energy (LE))

The SoC also provides 3-way coexistence for Wi-Fi, Bluetooth, and ZigBee operation, and indoor location and navigation (802.11mc).

The internal coexistence arbitration and a Mobile Wireless Systems (MWS) serial transport interface provide the functionality for connecting an external Long Term Evolution (LTE) or ZigBee device. The device also supports a coexistence interface for co-located Bluetooth/Wi-Fi device arbitration.

For security, the device supports high performance 802.11i security standards through the implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP), AES/Cipher-Based Message Authentication Code (CMAC), WPA (AES), and Wi-Fi Authentication and Privacy Infrastructure (WAPI) security mechanisms.

For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. The device also features 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

Host interfaces include SDIO 3.0 and high-speed UART interfaces for connecting Wi-Fi and Bluetooth technologies to the host processor.

The device is available in QFN and eWLP package options.

Figure 1 shows the functional block diagram of the device.

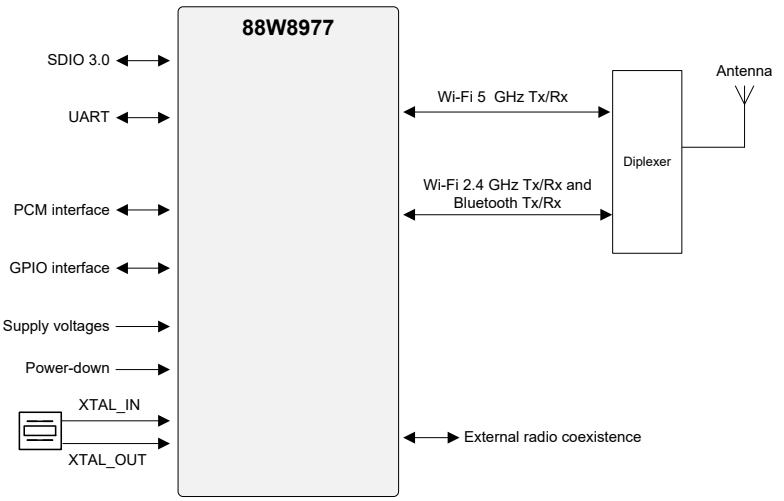


Figure 1. 88W8977 functional block diagram

1.1 Applications

Smart home applications:

- Wireless home audio and video entertainment systems
- Wearables
- Internet of Things (IoT) gateways
- Mobile routers

Mobile applications:

- Wi-Fi and Bluetooth enabled smart phones and tablets
- Personal computing systems including notebooks and ultrabooks

1.2 Wi-Fi key features

- Support 802.11 a/b/g/n
- Dual band: 2.4 GHz and 5 GHz
- Single stream 802.11n with 20 MHz and 40 MHz channels
- Up to MCS7 data rates (150 Mbps)
- Support 802.11mc for location
- Security: support WPA/WPA2 mixed mode, WPA2 and WPA3 security standards

1.3 Bluetooth key features

- Bluetooth 5 features
- Direction Finding—Connection-oriented Angle of Arrival (AoA)
- PCM audio interface
- Security: AES

1.4 Host interfaces

Wi-Fi and Bluetooth host interface options

Wi-Fi	Bluetooth
SDIO 3.0	UART
SDIO 3.0	SDIO 3.0

1.5 Operating characteristics

- Supply voltage: 2.2V, 1.8V, and 1.05V
- Operating temperature
  - Extended: -30 to 85°C
  - Industrial: -40 to 85°C

1.6 General features

- Package options
  - 68-pin QFN (8 mm x 8 mm)
  - 74-bump eWLP (4.674 mm x 3.46 mm)
- Simultaneous Wi-Fi and Bluetooth operation, including Bluetooth Low Energy (LE)
- Dynamic Rapid Channel Switching (DRCS) for simultaneous operation in 2.4 GHz and 5 GHz bands
- Power saving features
  - Efficient power management system
  - On-chip LDO for 1.05V generation from 1.8V supply
  - Sleep and standby modes
  - Deep-sleep mode
- Independent ARM-based Wi-Fi and Bluetooth CPUs
- Independent two-channel Direct Memory Access (DMA)
- Memory:
  - Internal SRAM
  - Boot ROM
  - OTP memory to store the MAC address and calibration data
- Peripheral Interface
  - General-Purpose I/O (GPIO) interface

1.7 Internal block diagram

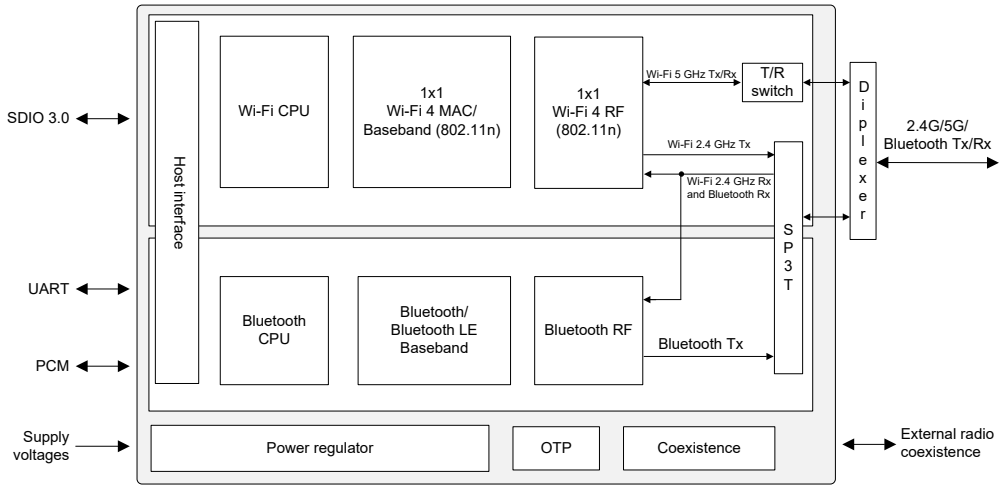


Figure 2. 88W8977 internal block diagram

2 Wi-Fi subsystem

2.1 IEEE 802.11 standards

- 802.11b data rates of 1 and 2 Mbps
- 802.11b data rates of 5.5 and 11 Mbps
- 802.11a/g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n with maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11mc precise indoor location and navigation
- 802.11n block acknowledgement extension
- 802.11r fast hand-off for AP roaming
- 802.11u Hotspot 2.0 (STA mode only)
- 802.11v TIM frame transmission/reception
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode

2.2 Wi-Fi MAC

- Simultaneous peer-to-peer and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- On-chip transmit and receive FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and transmit (aggregation)
- 20/40 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgement extension
- Dynamic frequency selection
- TIM frame transmission/reception
- Multiple-BSS/Station
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Mobile hotspot

2.3 Wi-Fi baseband

- 802.11n 1x1 SISO
- Backward compatibility with legacy 802.11a/g/b technology
- 2.4 GHz Wi-Fi and Bluetooth share LNA for receive operation
- PHY data rates up to 150 Mbps
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel, 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- Modulation and Coding Scheme (MCS)—MCS0~7
- Dynamic frequency selection (radar detection)
  - Enhanced radar detection for long and short pulse radar
  - Enhanced AGC scheme for DFS channel
  - Compliance with Japan DFS requirements for W53 and W56
- Radio resource measurement
- Optional 802.11n SISO features:
  - 20/40 MHz coexistence
  - One spatial stream STBC reception
  - Short guard interval
  - RIFS on receive path for 802.11n packets
  - 802.11n greenfield Tx/Rx
- Wi-Fi indoor locationing (802.11mc)
- Power save features

2.4 Wi-Fi radio

- Integrated direct-conversion radio
- 20 and 40 MHz channel bandwidths
- Shared Wi-Fi/Bluetooth receive input scheme for 2.4 GHz band

Wi-Fi receive path

- Direct conversion architecture eliminates need for external SAW filter
- On-chip gain selectable LNA with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

Wi-Fi transmit path

- Internal PA with power control
- Optimized transmit gain distribution for linearity and noise performance

Wi-Fi local oscillator

- Fine channel step

2.5 Wi-Fi encryption

- WEP 64- and 128-bit encryption with hardware TKIP processing (WPA)
- AES/CCMP hardware implementation as part of the 802.11i security standard (WPA2)
- Enhanced AES engine performance
- AES/Cipher-based Message Authentication Code (CMAC) as part of the 802.11w security standard
- Simultaneous Authentication of Equals (SAE) WPA3
- WLAN Authentication and Privacy Infrastructure (WAPI)

2.6 Wi-Fi host interfaces

- SDIO 3.0

3 Bluetooth subsystem

3.1 Bluetooth

- Bluetooth 5
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Wi-Fi/Bluetooth
- Shared LNA for Wi-Fi/Bluetooth
- PCM interface for voice applications
- Baseband and radio BDR and EDR packet types—1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), and 3 Mbps (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER)
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard SDIO and UART HCI transport layer
- HCI layer to integrate with profile stack
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power saving mechanisms (i.e., hold, sniff modes, and sniff-subrating)
- Enhanced Power Control (EPC)
- Channel Quality Driven Data Rate (CQDDR)
- Wideband Speech (WBS) support (1 WBS link)
- Encryption (AES) support
- LTE/MWS coexistence

3.2 Bluetooth Low Energy (LE)

- Broadcaster, observer, central, and peripheral roles
- Supports link layer topology to be master and slave (connects up to 16 links)
- Wi-Fi/Bluetooth Coexistence Arbiter (BCA) capability
- Shared RF with Bluetooth BDR/EDR
- Encryption (AES) support
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- Direction Finding—Connection-oriented Angle of Arrival (AoA)

3.3 Bluetooth host interfaces

- SDIO 3.0
- High-speed UART

3.4 PCM interface

- Master or slave mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- Short frame and long frame synchronization
- Tri-state PCM interface capability

4 Pin information

4.1 Signal diagram

Note: *Signals may be muxed. See Pin description (BRF_ANT signal is muxed with RF_TR_2 pin; Bluetooth external coexistence signals are muxed with both GPIO[11:8] and SD_DAT[3:0] pins).*

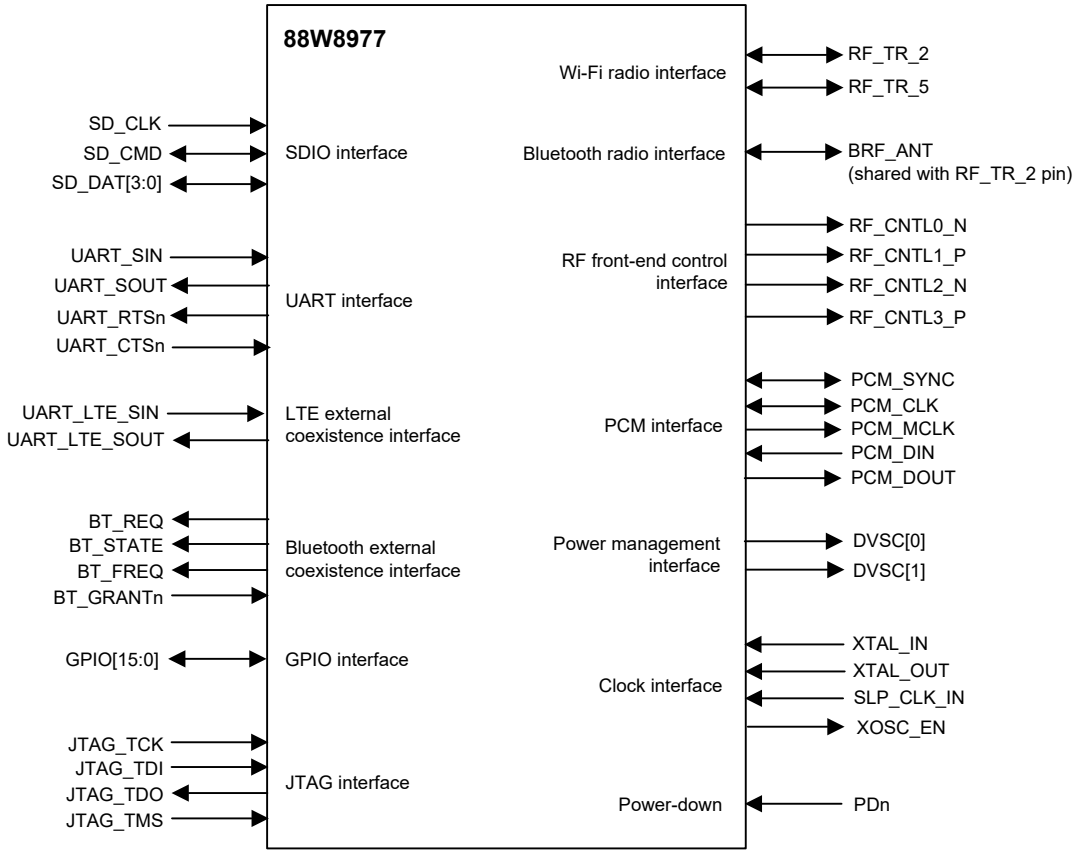


Figure 3. 88W8977 signal diagram

4.2 Pin assignment - 68-pin QFN package option

Note: *Pins may have muxed signals. See* Section 4.4 "Pin description".

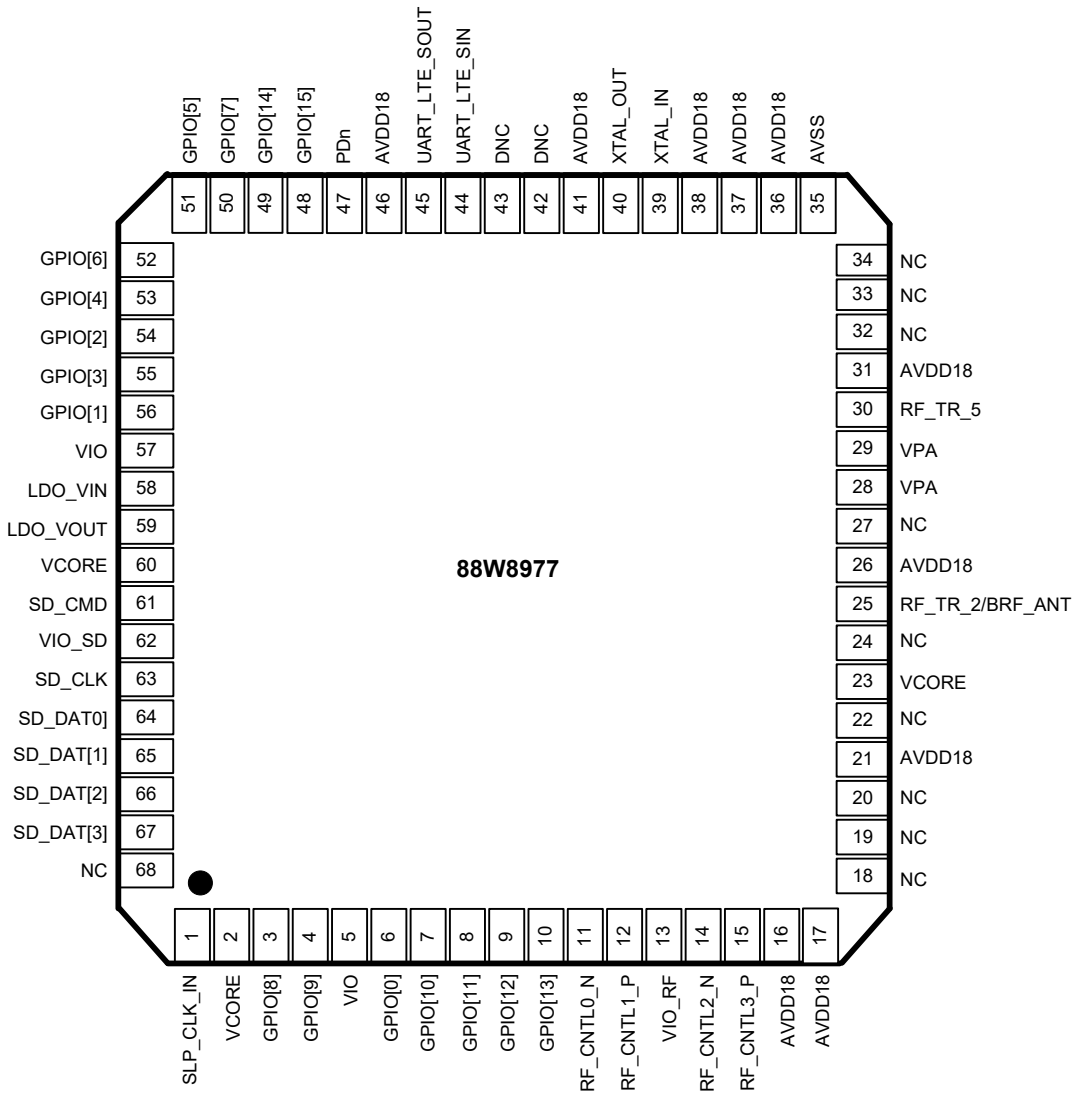


Figure 4. Pin assignement for 68-pin package option (top view)

4.3 Pad locations - 74-bump eWLP

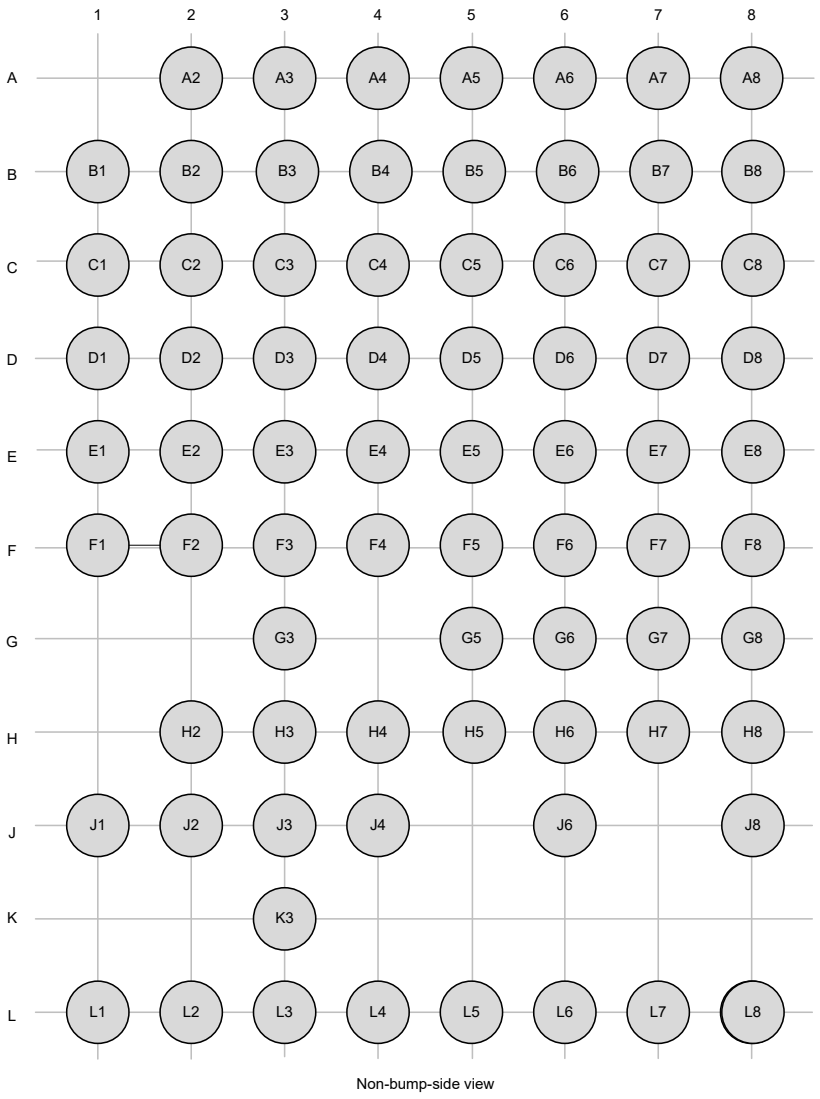


Figure 5. Pad locations—74-bump WLCSP (Non-bump-side view, bumps down) [1]

[1] Alphanumeric designations are approximations to the grid.

Table 1. Pad locations—74-bump eWLP[1]

Pin Name	Alpha-Numeric Designation	Flip Chip Pad Location Relative to Die Center (non-bump-side view)	
		X	Y
VIO	A2	-1000.0	2000.0
VSS	A3	-600.0	2000.0
LDO_VIN	A4	-200.0	2000.0

Pin Name	Alpha-Numeric Designation	Flip Chip Pad Location Relative to Die Center (non-bump-side view)	
		X	Y
VIO_SD	A5	200.0	2000.0
SD_DAT[0]	A6	600.0	2000.0
SD_DAT[1]	A7	1000.0	2000.0
VSS	A8	1400.00	2000.0
GPIO[5]	B1	-1400.0	1600.0
GPIO[6]	B2	-1000.0	1600.0
GPIO[3]	B3	-600.0	1600.0
LDO_VOUT	B4	-200.0	1600.0
VCORE	B5	200.0	1600.0
SD_CLK	B6	600.0	1600.0
SD_DAT[2]	B7	1000.0	1600.0
SD_DAT[3]	B8	1400.00	1600.0
AVDD18	C1	-1400.0	1200.0
GPIO[7]	C2	-1000.0	1200.0
GPIO[4]	C3	-600.0	1200.0
GPIO[2]	C4	-200.0	1200.0
GPIO[1]	C5	200.0	1200.0
SD_CMD	C6	600.0	1200.0
SLP_CLK_IN	C7	1000.0	1200.0
VSS	C8	1400.00	1200.0
AVDD18	D1	-1400.0	800.0
AVSS	D2	-1000.0	800.0
PDn	D3	-600.0	800.0
GPIO[14]	D4	-200.0	800.0
GPIO[15]	D5	200.0	800.0
GPIO[8]	D6	600.0	800.0
GPIO[0]	D7	1000.0	800.0
VIO	D8	1400.00	800.0
XTAL_IN	E1	-1400.0	400.0
XTAL_OUT	E2	-1000.0	400.0
DNC	E3	-600.0	400.0
DNC	E4	-200.0	400.0
UART_LTE_SOUT	E5	200.0	400.0
GPIO[9]	E6	600.0	400.0
GPIO[10]	E7	1000.0	400.0

Pin Name	Alpha-Numeric Designation	Flip Chip Pad Location Relative to Die Center (non-bump-side view)	
		X	Y
GPIO[13]	E8	1400.00	400.0
AVDD18	F1	-1400.0	0.0
AVSS	F2	-1000.0	0.0
AVDD18	F3	-600.0	0.0
AVSS	F4	-200.0	0.0
UART_LTE_SIN	F5	200.0	0.0
GPIO[11]	F6	600.0	0.0
GPIO[12]	F7	1000.0	0.0
VIO_RF	F8	1400.00	0.0
AVSS	G3	-600.0	-400.0
RF_CNTL0_N	G5	200.0	-400.0
RF_CNTL1_P	G6	600.0	-400.0
RF_CNTL2_N	G7	1000.0	-400.0
RF_CNTL3_P	G8	1400.00	-400.0
AVDD18	H2	-1000.0	-800.0
AVSS	H3	-600.0	-800.0
VCORE	H4	-200.0	-800.0
AVSS	H5	200.0	-800.0
AVSS	H6	600.0	-800.0
AVSS	H7	1000.0	-800.0
AVDD18	H8	1400.0	-800.0
AVSS	J1	-1400.0	-1200.0
AVSS	J2	-1000.0	-1200.0
AVSS	J3	-600.0	-1200.0
AVSS	J4	-200.0	-1200.0
AVSS	J6	600.0	-1200.0
AVDD18	J8	1400.0	-1200.0
VPA	K3	-600.00	-1600.0
NC	L1	-1400.0	-2000.0
RF_TR_5	L2	-1000.0	-2000.0
DNC	L3	-600.0	-2000.0
RF_TR_2	L4	-200.0	-2000.0
AVDD18	L5	200.0	-2000.0
AVDD18	L6	600.0	-2000.0

Pin Name	Alpha-Numeric Designation	Flip Chip Pad Location Relative to Die Center (non-bump-side view)	
		X	Y
AVSS	L7	1000.0	-2000.0
NC	L8	1400.0	-2000.0

[1] Alphanumeric designations are approximations to the grid shown in Figure 5.

4.4 Pin description

4.4.1 Pin types

Table 2. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A,O	Analog output
NC	No connect
DNC	Do not connect
Power	Power
Ground	Ground

4.4.2 Pin states

The pin state information provided in this section is defined as follows:

- After firmware is downloaded, pads like GPIO and RF control are programmed in functional mode per the functionality of the pins
- The Hardware State (HW State) at power-on may differ based on the pin muxing/strap setting. The HW State is the pin state at power-on after boot code finishes and before firmware download begins (firmware may change the pin state). For example, for UART_RTSn and UART_SOUT, the boot code will enable the UART interface, making the HW states output high and output low, respectively.
- PD State denotes the power-down state in default configuration. Many pads have programmable power-down values, which can be set by firmware.
- PD Prog denotes whether the power-down state is programmable or not
- PU denotes whether the pull-up is programmable or not
- PD denotes whether the pull-down is programmable or not
- Pull-up and pull-down are only effective when the pad is in input mode.
- For SDIO, once the command is received from the host, the pads are configured accordingly

4.4.3 General Purpose I/O (GPIO)/LED interface

Table 3. General purpose I/O/LED interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU/ PD	PU	PD
GPIO[15]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[15] (input/output) **JTAG Mode**: JTAG_TMS, JTAG controller select (input)									
GPIO[14]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[14] (input/output) **JTAG Mode**: JTAG_TCK, JTAG test clock (input)									
GPIO[13]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[13] (input/output)									
GPIO[12]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[12] (input/output)									
GPIO[11]	VIO	tristate	input	input	tristate	yes	weak PU	no	no
GPIO Mode: GPIO[11] (input/output) **UART Mode**: UART_RTSn (output) (active low) **Bluetooth External Coexistence Mode**: BT_REQ. See Section 4.4.6 "Bluetooth external coexistence interface".									
GPIO[10]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[10] (input/output) **UART Mode**: UART_CTSn (input) (active low) **Bluetooth External Coexistence Mode**: BT_GRANTn. See Section 4.4.6 "Bluetooth external coexistence interface".									
GPIO[9]	VIO	tristate	input	input	tristate	yes	nominal PU	no	no
GPIO Mode: GPIO[9] (input/output) **UART Mode**: UART_SIN (input) **Bluetooth External Coexistence Mode**: BT_STATE. See Section 4.4.6 "Bluetooth external coexistence interface".									
GPIO[8]	VIO	tristate	input	input	tristate	yes	weak PU	no	no
GPIO Mode: GPIO[8] (input/output) **UART Mode**: UART_SOUT (output) **Bluetooth External Coexistence Mode**: BT_FREQ. See Section 4.4.6 "Bluetooth external coexistence interface"									
GPIO[7]	VIO	tristate	input	input	tristate	yes	nominal PU	no	no
GPIO Mode: GPIO[7] (input/output) **PCM Mode**: PCM_SYNC (input/output) • Output if master • Input if slave									
GPIO[6]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[6] (input/output) **PCM Mode**: PCM_CLK (input/output) • Output if master • Input if slave									
GPIO[5]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU/ PD	PU	PD
GPIO Mode: GPIO[5] (input/output) **PCM Mode**: PCM_DOUT (output)									
GPIO[4]	VIO	tristate	input	input	tristate	yes	nominal PU	no	no
GPIO Mode: GPIO[4] (input/output) **PCM Mode**: PCM_DIN (input)									
GPIO[3]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[3] (input/output) **Power Management Mode**: DVSC[1] Digital voltage scaling control (output) **JTAG Mode:** JTAG_TDO, JTAG test data (output)									
GPIO[2]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[2] (input/output) **Power Management Mode**: DVSC[0] Digital voltage scaling control (output) **JTAG Mode:** JTAG_TDI, JTAG test data (input)									
GPIO[1]	VIO	tristate	input	input	tristate	yes	weak PU	no	no
GPIO Mode: GPIO[1] (input/output)									
GPIO[0]	VIO	tristate	output	output	drive low	yes	weak PU	yes	no
GPIO Mode: GPIO[0] (input/output) **Oscillator Mode**: XOSC_EN/CLK_REQ (output) (active high) 0 = disable external oscillator 1 = enable external oscillator									

4.4.4 RF front-end control interface

Table 4. RF front-end control interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU/PD	PU	PD
RF_CNTL0_N	VIO_RF	tristate	input	output	drive low	yes	weak PU	no	no
RF Control 0—RF Control Output Low (output) This pin is used as a configuration pin: CON[0] (input) See Section 4.5 "Configuration pins".									
RF_CNTL1_P	VIO_RF	tristate	input	output	drive high	yes	weak PU	no	no
RF Control 1—RF Control Output High (output)									
RF_CNTL2_N	VIO_RF	tristate	input	output	drive low	yes	weak PU	no	no
RF Control 2—RF Control Output Low (output) This pin is used as a configuration pin: CON[1] (input) See Section 4.5 "Configuration pins".									
RF_CNTL3_P	VIO_RF	tristate	input	output	drive high	yes	weak PU	no	no
RF Control 3—RF Control Output High (output)									

4.4.5 Wi-Fi/Bluetooth radio interface

Table 5. Wi-Fi/Bluetooth radio interface

Pin Name	Type	Supply	Description
RF_TR_2 / BRF_ANT	A, I/O	AVDD18	**Wi-Fi**: Wi-Fi Transmit/Receive (2.4 GHz) **Bluetooth**: Bluetooth Transmit/Receive
RF_TR_5	A, I/O	AVDD18	Wi-Fi Transmit/Receive (5 GHz)

4.4.6 Bluetooth external coexistence interface

Table 6. Bluetooth external coexistence interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU/ PD	PU	PD
BT_GRANTn	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
Coexistence Mode: BT_GRANTn input (active low) **SDIO Mode**: SD_DAT[0]. See Section 4.4.7 "SDIO host interface". **GPIO Mode**: GPIO[10]. See Section 4.4.3 "General Purpose I/O (GPIO)/LED interface".									
BT_STATE	VIO	tristate	output	output	tristate	yes	nominal PU	yes	yes
Coexistence Mode: BT_STATE output **SDIO Mode**: SD_DAT[2]. See Section 4.4.7 "SDIO host interface". **GPIO Mode**: GPIO[9]. See Section 4.4.3 "General Purpose I/O (GPIO)/LED interface".									
BT_REQ	VIO	tristate	output	output	tristate	yes	nominal PU	yes	yes
Coexistence Mode: BT_REQ output **SDIO Mode**: SD_DAT[3]. See Section 4.4.7 "SDIO host interface". **GPIO Mode**: GPIO[11]. See Section 4.4.3 "General Purpose I/O (GPIO)/LED interface".									
BT_FREQ	VIO	tristate	output	output	tristate	yes	nominal PU	yes	yes
Coexistence Mode: BT_FREQ output **SDIO Mode**: SD_DAT[1]. See Section 4.4.7 "SDIO host interface". **GPIO Mode**: GPIO[8]. See Section 4.4.3 "General Purpose I/O (GPIO)/LED interface".									
NOTE: Bluetooth external coexistence pin functions are unavailable when the SDIO interface signals are used.									

4.4.7 SDIO host interface

Table 7. SDIO host interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU/ PD	PU	PD
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Clock input **SDIO 1-bit Mode**: Clock input									
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Command/response (input/output) **SDIO 1-bit Mode**: Command line									
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[3] **SDIO 1-bit Mode**: Reserved **Bluetooth External Coexistence Mode**: BT_REQ. See Section 4.4.6 "Bluetooth external coexistence interface".									
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) **SDIO 1-bit Mode**: Read wait (optional) **Bluetooth External Coexistence Mode**: BT_STATE. See Section 4.4.6 "Bluetooth external coexistence interface".									
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[1] **SDIO 1-bit Mode**: Interrupt **Bluetooth External Coexistence Mode**: BT_FREQ. See Section 4.4.6 "Bluetooth external coexistence interface".									
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[0] **SDIO 1-bit Mode**: Data line **Bluetooth External Coexistence Mode**: BT_GRANT. See Section 4.4.6 "Bluetooth external coexistence interface".									
NOTE: SDIO pin functions are unavailable when the Bluetooth external coexistence interface signals are used.									

4.4.8 UART host interface

Table 8. UART host interface (MFP)

NOTE: Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
UART_SIN	I	VIO	UART serial input signal - GPIO[9] input/output
UART_SOUT	O	VIO	UART serial output signal - GPIO[8] input/output
UART_RTSn	O	VIO	UART request-to-send output signal . Active low - GPIO[11] input/ output
UART_CTSn	I	VIO	UART clear-to-send input signal - Active low - GPIO[10] input/output

4.4.9 LTE external coexistence interface

Table 9. LTE interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU	PU	PD
UART_LTE_SIN	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
UART_LTE_SIN (input)									
UART_LTE_SOUT	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
UART_LTE_SOUT (output)									

4.4.10 PCM interface

Table 10. PCM interface pins (MFP)

NOTE: Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
PCM_DIN	I	VIO	Receive PCM input. GPIO[4] input/output
PCM_DOUT	O	VIO	Transmit PCM output. GPIO[5] input/output
PCM_SYNC	I/O	VIO	PCM frame sync. GPIO[7] input/output • Output if master • Input if slave
PCM_CLK	I/O	VIO	PCM data clock. GPIO[6] input/output • Output if master • Input if slave

4.4.11 Power management interface

Table 11. Power management interface pins (MFP)

NOTE: Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
DVSC[1]	O	VIO	Digital voltage scaling control output signal. GPIO[3] input/output
DVSC[0]	O	VIO	Digital voltage scaling control output signal. GPIO[2] input/output

4.4.12 Power supply and ground pins

Table 12. Power supply and ground pins

Pin Name	Type	Description
VCORE	Power	1.05V Core Power Supply
VIO	Power	1.8V/2.5V/3.3V Digital I/O Power Supply
VIO_SD	Power	1.8V/3.3V Digital I/O SDIO Power Supply
VIO_RF	Power	1.8V/3.3V Analog I/O RF Power Supply
AVDD18	Power	1.8V Analog Power Supply
VPA	Power	2.2V Analog Power Supply
LDO_VIN	Power	LDO Voltage Input (1.8V)
LDO_VOUT	Power	LDO Voltage Output
AVSS	Ground	Ground
VSS	Ground	Ground
NC	NC	No Connected
DNC	DNC	Do Not Connect Do not connect these pins. Leave these pins floating.

4.4.13 Clock interface

Table 13. Clock interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD	PD Prog	Internal PU/ PD	PU	PD
XTAL_IN	AVDD18	--	--	--	--	--	--	--	--
Crystal / Crystal Oscillator / System Clock Input Accepts 26 MHz reference clock signal. See Section 8.10 "Clock specifications".									
XTAL_OUT	AVDD18	--	--	--	--	--	--	--	--
Crystal / Crystal Oscillator Output Connect this pin to ground when an external oscillator is used.									
SLP_CLK_IN	VIO	tristate	input	input	tristate	no	nominal PU	yes	yes
Sleep Clock Input (optional) Used for Wi-Fi and Bluetooth low-power modes. • An external sleep clock is recommended for minimal current consumption. • If no sleep clock input is provided, an internal sleep clock (derived from reference clock) will be used. This will cause an approximate ~50 uA current increase on the 3.3V rail, since the reference clock cannot be shut down during device sleep. If SLP_CLK_IN is not connected, the internal circuit will detect no signal, and firmware will initialize the sleep clock based on the reference clock. • To reduce further leakage, do not ground the SLP_CLK_IN pin / keep it floating (DNC) for cases where a sleep clock derived from the reference clock will be used.									
XOSC_EN	VIO	--	--	--	--	--	--	--	--
XOSC_EN/CLK_REQ (output) NOTE: Muxed with GPIO[0].									

4.4.14 Power-down pin

Table 14. Power-down pin

Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	PD Prog	Internal PU/ PD	PU	PD
PDn	AVDD18	--	--	--	--	--	--	--	--
Full Power-Down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.8V to 4.5V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin.									

4.4.15 JTAG interface

Table 15. JTAG interface pins (MFP)

NOTE: Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
JTAG_TDO	O	VIO	JTAG test data output signal. GPIO[3] input/output
JTAG_TDI	I	VIO	JTAG test data input signal. GPIO[2] input/output
JTAG_TMS	I	VIO	JTAG test mode select input signal. GPIO[15] input/output
JTAG_TCK	I	VIO	JTAG test clock input signal. GPIO[14] input/output

4.5 Configuration pins

Table 16 shows the pins used as configuration inputs to set the parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a 100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 16. Configuration pins

Configuration Bits	Pin Name	Configuration Function
CON[1]	RF_CNTL2_N	Firmware Boot Options No hardware impact. Software reads and boots accordingly. See Table 17 ***Note:*** *Boot code needs to use this host boot strap status to decide the correct boot sequence.*
CON[0]	RF_CNTL0_N	

Table 17. Firmware boot options

Strap value	Wi-Fi	Bluetooth/ Bluetooth LE	Firmware download	Firmware download mode	Number of SDIO functions
00	--	--	--	--	--
01	--	--	--	--	--
10	SDIO	UART	SDIO + UART	Parallel/Serial	1 (Wi-Fi)
11	SDIO	SDIO	SDIO + SDIO	Parallel/Serial	2 (Wi-Fi, Bluetooth)

5 Power information

The table in Section 4.4.12 "Power supply and ground pins " shows the required voltage levels for each rail and PDn input signal.

5.1 Leakage optimization

For applications not using Wi-Fi and Bluetooth, the device can be put into a low-leakage mode of operation. Methods include:

- Using the power-down (PDn) pin
  The power-down state provides the lowest leakage mode of operation. Assert PDn low to enter power-down. If the firmware is not downloaded, the device must be kept in power-down mode to reduce leakage.
- All rails powered off

Alternatively, all power rails can be powered off. In this case, the state of PDn pin is irrelevant.

5.2 Power-up

The 88W8977 VCORE is supplied through either an external PMIC or the internal LDO. In both cases, the PDn pin of the 88W8977 is tied to 1.8V.

The power configurations include:

- Section 5.2.1 "Configuration—PMIC supplies VCORE"
- Section 5.2.2 "Configuration—Internal LDO supplies VCORE"

In either configuration, the ramp-up is controlled by the Host using the PMIC_EN pin.

- PMIC_EN represents the input enable pin (EN) of the power regulator.
- PMIC_EN ramps up from Host 3.3V
- PMIC_EN ramps up from Host GPIO pin

Section 5.2.3 "Power-up sequence" shows the power-up sequence for both configurations.

5.2.1 Configuration—PMIC supplies VCORE

- PMIC suppplies VCORE
- PMIC_EN ramps up from the host 3.3V or the host GPIO pin
- AVDD18 supplies PDn (follow AVDD18; PDn is connected to 1.8V supply)
- PMIC supplies the external VPA and AVDD18 power supply pins
- The host (1.8V/3.3V) supplies the external VIO/VIO_REF power supply pins

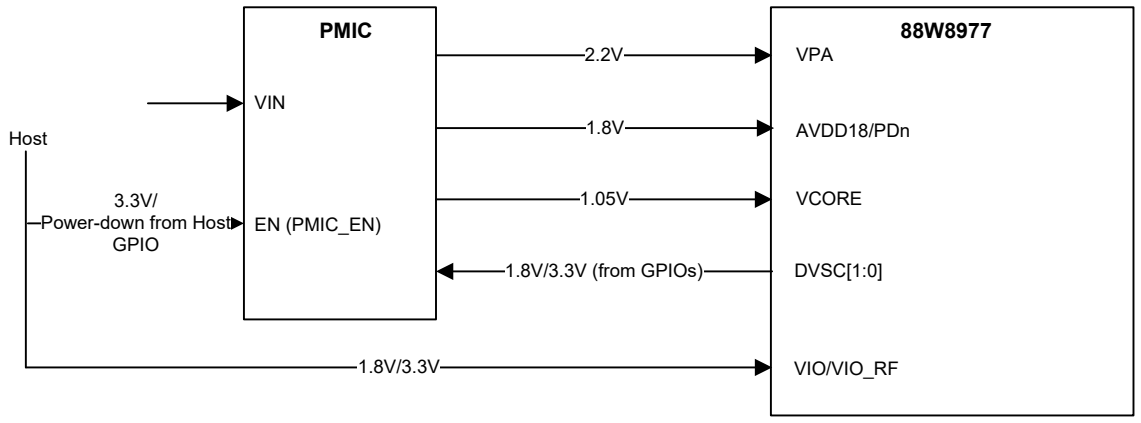


Figure 6. Configuration—VCORE from PMIC[1]

[1] A minimum time of 100 ms is required after PMIC_EN is deasserted (=0) and before it is asserted (=1).

5.2.2 Configuration—Internal LDO supplies VCORE

- LDO_VOUT supplies VCORE
- PMIC_EN ramps up from Host 3.3V or Host GPIO pin
- AVDD18 supplies PDn (follow AVDD18; PDn connected to 1.8V supply)
- PMIC supplies the external VPA and AVDD18/LDO_VIN power supply pins
- The host (1.8V/3.3V) supplies the external VIO/VIO_REF power supply pins

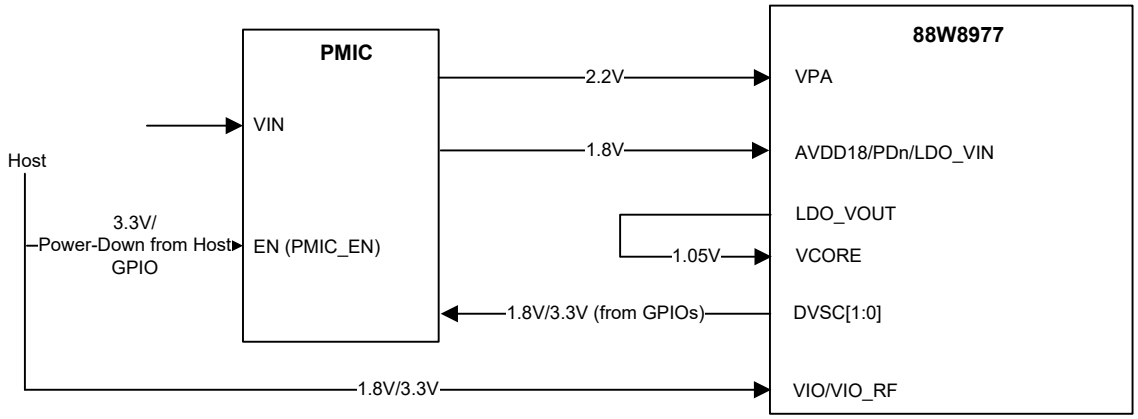


Figure 7. Configuration—VCORE from Internal LDO[1]

[1] A minimum time of 100 ms is required after PMIC_EN is deasserted (=0) and before it is asserted (=1).

5.2.3 Power-up sequence

- VPA must be good (90%) before AVDD18 starts ramping up.
- AVDD18 must be good (90%) before VCORE starts ramping up.

Figure 8 shows the power-up sequence.

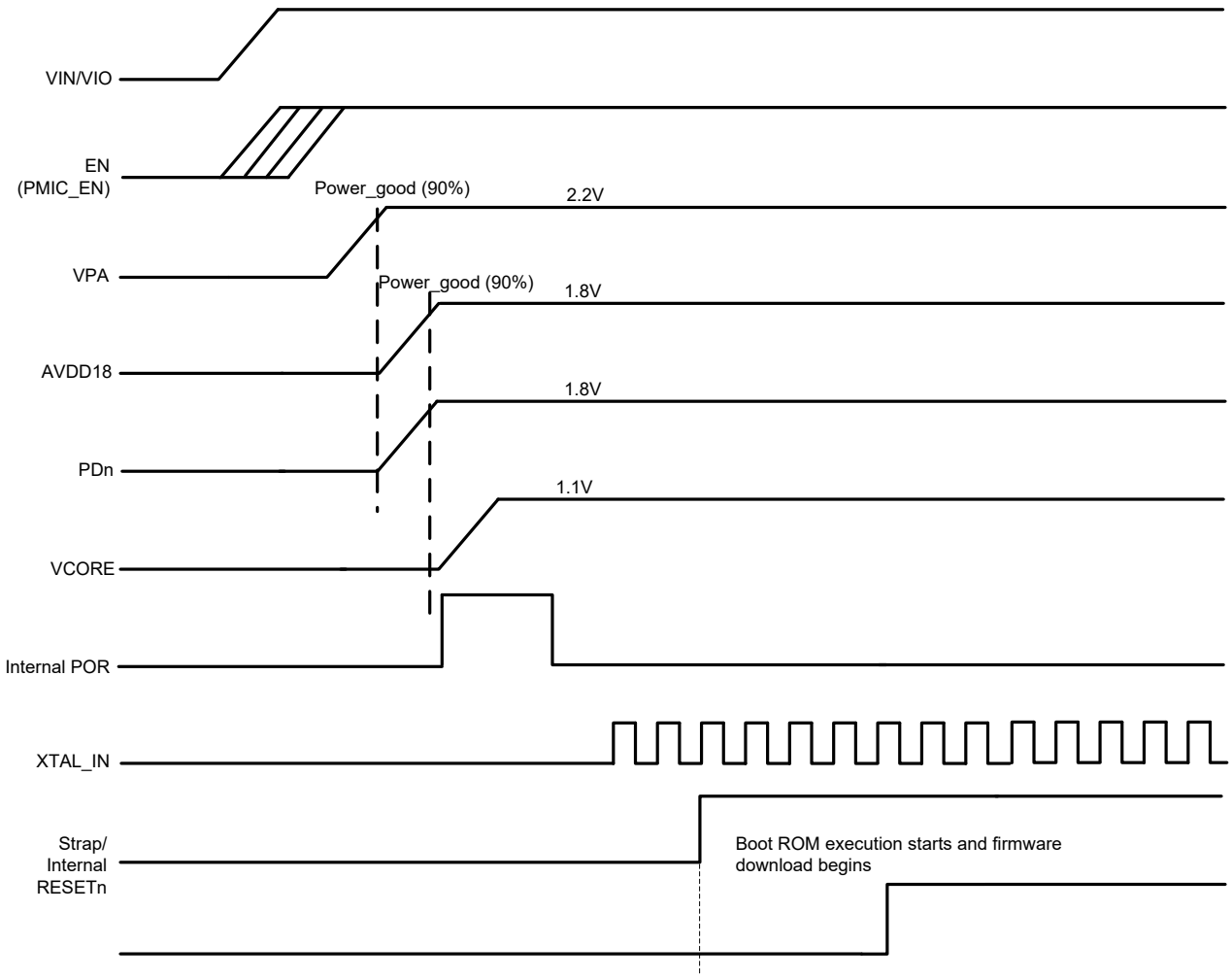


Figure 8. Power-up sequence

5.3 Power-down

5.3.1 Recommended power-down sequence

In the recommended power-down sequence, VPA ramps down before AVDD18 in order for the RF PA to turn the logic off (depends on the control logic generated from AVDD18). Also, when the PMIC VBAT is removed, the PMIC cannot guarantee a ramp-down requirement.

Figure 9 shows the recommended (but not required) power-down sequence.

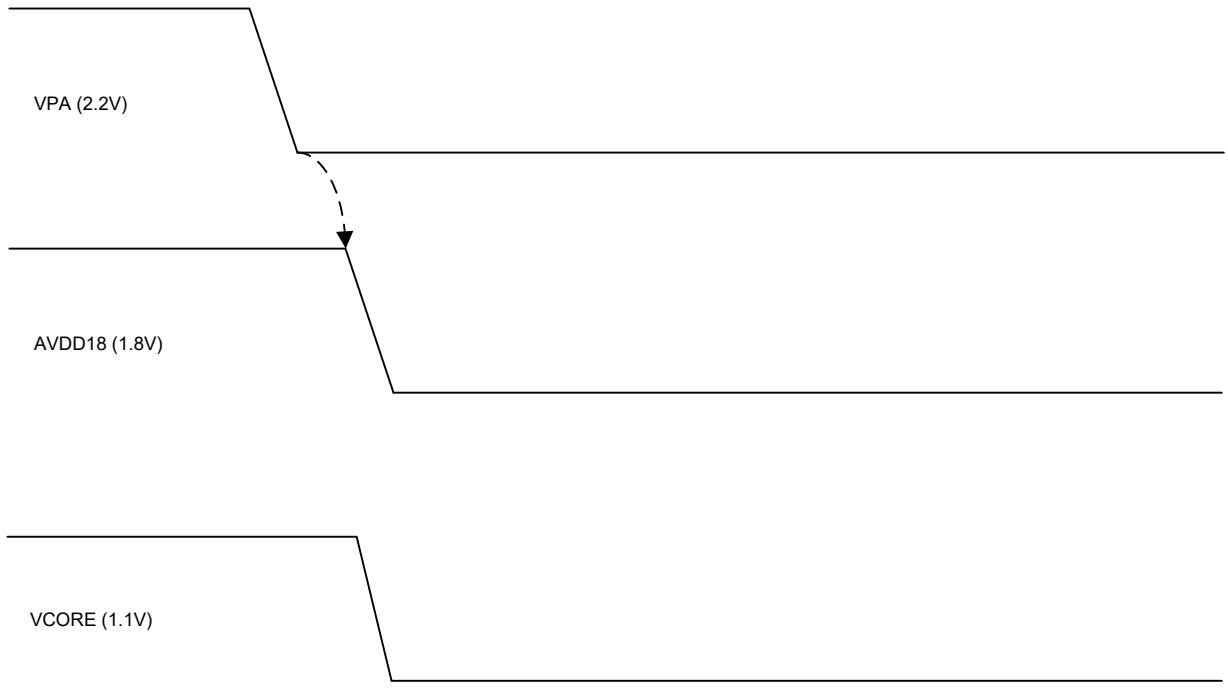


Figure 9. Recommended power-down sequence

5.3.2 Power-down using PMIC_EN host pin

The maximum ramp-down time for VCORE from PMIC_EN assertion is 10 ms. PMIC_EN must be asserted a minimum of 100 ms to guarantee that VCORE and AVDD18 are discharged to less than 0.2V for the POR to generate properly after PMIC_EN is deasserted.

Figure 10 shows the sequence.

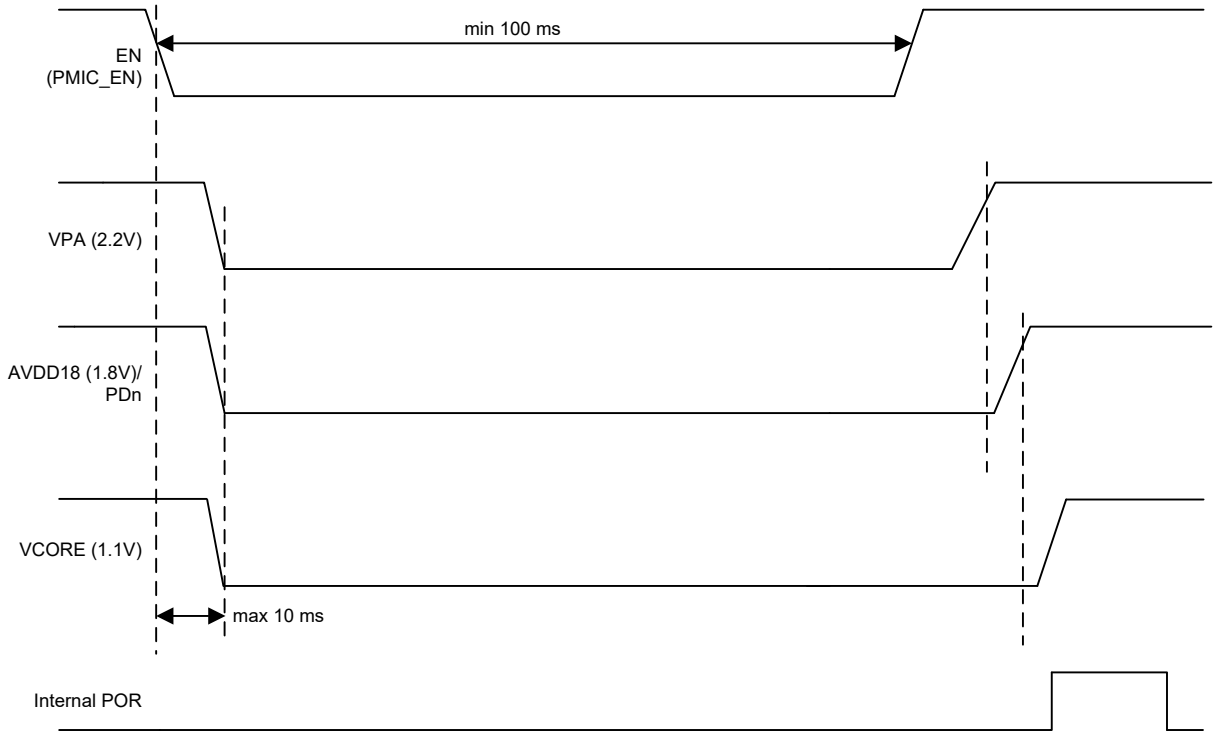


Figure 10. Power-down using PMIC_EN host pin - PMIC and 88W8977 both in power-down mode

5.4 Deep sleep

When a programmable power regulator is used to supply VCORE, 88W8977 may use the power management interface to reduce VCORE to approximately 0.8V to reduce the power consumption in deep sleep mode.

6 Absolute maximum ratings

Note: *The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.*

Table 18. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCORE	Power supply voltage with respect to VSS	--	--	1.05	1.21	V
VIO	Power supply voltage with respect to VSS	--	--	1.8	2.2	V
		--	--	2.5	3.0	V
		--	--	3.3	4.0	V
VIO_SD	Power supply voltage with respect to VSS	--	--	1.8	2.2	V
		--	--	3.3	4.0	V
VIO_RF	Power supply voltage with respect to VSS	--	--	1.8	2.2	V
		--	--	3.3	4.0	V
AVDD18	Power supply voltage with respect to VSS	--	--	1.8	1.98	V
VPA	Power supply voltage with respect to VSS	--	--	2.2	2.3	V
LDO_VIN	Power supply voltage with respect to VSS	--	--	1.8	2.0	V
$T_{STORAGE}$	Storage temperature	--	-55	--	+125	°C
V_{ESD}	Electrocstatic discharge voltage	human body model (HBM)[1]	-1	--	+1	kV
		charged device model (CDM)[2]	-500	--	+500	V

[1] According to JESD22-A114F
[2] According to JESD22-C101E

7 Recommended operating conditions

Note: *Operation beyond the recommended operating conditions is neither recommended nor guaranteed.*

Table 19. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCORE	1.05V core power supply	--	1.00	1.05	1.15	V
VIO	1.8V/2.5V/3.3V digital I/O power supply	--	1.62	1.8	1.98	V
		--	2.25	2.5	2.75	V
		--	2.97	3.3	3.47	V
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	--	1.62	1.8	1.98	V
		--	2.97	3.3	3.47	V
VIO_RF	1.8V/3.3V I/O power supply	--	1.62	1.8	1.98	V
		--	2.97	3.3	3.47	V
AVDD18	1.8V analog power supply	--	1.71	1.8	1.89	V
VPA	2.2V analog power supply	--	2.09	2.2	2.26	V
LDO_VIN	LDO input voltage supply	--	1.71	1.8	1.89	V
T_A	Ambient operating temperature	Extended	-30	--	85	°C
		Industrial	-40	--	85	°C
T_J	Maximum junction temperature	--	--	--	125	°C

8 Electrical specifications

8.1 GPIO/LED interface specifications

The GPIO pins are powered by the VIO voltage supply.

8.1.1 VIO DC characteristics

8.1.1.1 1.8V operation

Table 20. DC electricals—1.8V operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.1.1.2 2.5V operation

Table 21. DC electricals—2.5V operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.1.1.3 3.3V operation

Table 22. DC electricals—3.3V operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.1.2 LED Mode

Table 23. LED Mode Data

Over the full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Typ	Unit
I_{OH}	Switching current high	Tristate on pad (requires pull-up on board)	Tristate when driving high	mA
I_{OL}	Switching current low	at 0.4V	10	mA

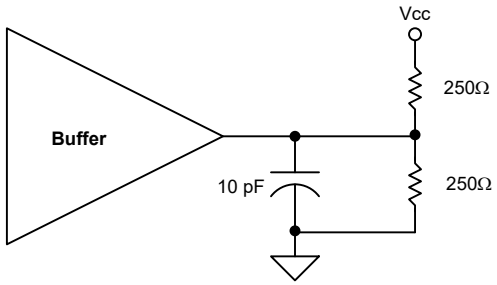


Figure 11. Slew rate measurement diagram

8.2 RF front-end control interface specifications

The RF front-end control pins are supplied by VIO_RF.

8.2.1 VIO_RF DC characteristics

8.2.1.1 1.8V operation

Table 24. DC electricals—1.8V operation (VIO_RF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_RF	--	VIO_RF+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_RF-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.2.1.2 3.3V operation

Table 25. DC electricals—3.3V operation (VIO_RF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_RF	--	VIO_RF+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_RF-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.3 Wi-Fi radio specifications

8.3.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip output port.

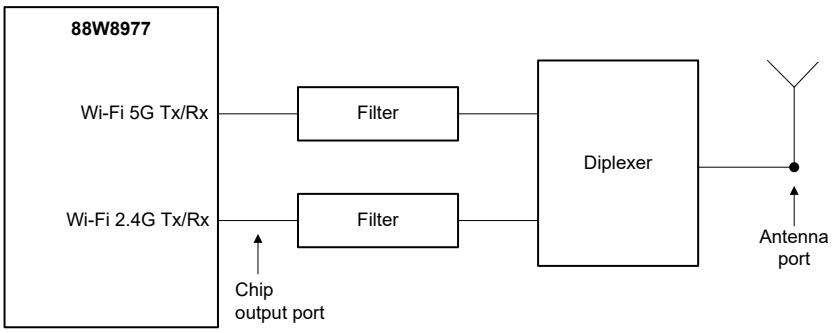


Figure 12. RF performance measurement points

8.3.2 2.4 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip output port.*

Table 26. 2.4 GHz Wi-Fi receiver performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	--	2500	MHz
Receiver input IP3 at RF high gain (in-band)	Receiver input IP3 when LNA in high gain mode (24 dB) at chip input	--	-20	--	dBm
Receiver sensitivity 802.11b	1 Mbit/s	--	-100	--	dBm
	2 Mbit/s	--	-96	--	dBm
	5.5 Mbit/s	--	-95	--	dBm
	11 Mbit/s	--	-91	--	dBm
Receiver sensitivity 802.11g	6 Mbit/s	--	-92	--	dBm
	9 Mbit/s	--	-92	--	dBm
	12 Mbit/s	--	-91	--	dBm
	18 Mbit/s	--	-89	--	dBm
	24 Mbit/s	--	-86	--	dBm
	36 Mbit/s	--	-83	--	dBm
	48 Mbit/s	--	-79	--	dBm
	54 Mbit/s	--	-77	--	dBm
Receiver sensitivity 802.11n, HT20 (with BCC)	MCS0	--	-92	--	dBm
	MCS1	--	-90	--	dBm
	MCS2	--	-88	--	dBm
	MCS3	--	-85	--	dBm
	MCS4	--	-82	--	dBm
	MCS5	--	-77	--	dBm
	MCS6	--	-76	--	dBm
	MCS7	--	-74	--	dBm
Receiver sensitivity 802.11n, HT40 (with BCC)	MCS0	--	-89	--	dBm
	MCS1	--	-88	--	dBm
	MCS2	--	-85	--	dBm
	MCS3	--	-83	--	dBm
	MCS4	--	-79	--	dBm
	MCS5	--	-75	--	dBm
	MCS6	--	-73	--	dBm
	MCS7	--	-72	--	dBm

Parameter	Conditions	Min	Typ	Max	Unit
Receiver maximum input level 802.11	802.11b	--	-1	--	dBm
	802.11g	--	-1	--	dBm
	MCS0-7	--	-1	--	dBm
Receiver adjacent channel interference rejection (ACI) 802.11b	1 Mbit/s	--	38	--	dB
	2 Mbit/s	--	39	--	dB
	5.5 Mbit/s	--	43	--	dB
	11 Mbit/s	--	47	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11g	6 Mbit/s	--	33	--	dB
	9 Mbit/s	--	33	--	dB
	12 Mbit/s	--	32	--	dB
	18 Mbit/s	--	30	--	dB
	24 Mbit/s	--	29	--	dB
	36 Mbit/s	--	27	--	dB
	48 Mbit/s	--	22	--	dB
	54 Mbit/s	--	19	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11n, HT20	MCS0	--	33	--	dB
	MCS1	--	32	--	dB
	MCS2	--	30	--	dB
	MCS3	--	27	--	dB
	MCS4	--	24	--	dB
	MCS5	--	19	--	dB
	MCS6	--	18	--	dB
	MCS7	--	17	--	dB

8.3.3 5 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, averaged over one channel per sub-band, averaged over the antenna path, and at the chip output port.*

Table 27. 5 GHz Wi-Fi receiver performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	5 GHz—IEEE 802.11n/a	4900	--	5925	MHz
Receiver input IP3 at RF high gain (in-band)[1]	Receiver Input IP3 when LNA in high gain mode (24 dB) at chip input	--	-20	--	dBm
Receiver sensitivity 802.11a	6 Mbit/s	--	-92	--	dBm
	9 Mbit/s	--	-92	--	dBm
	12 Mbit/s	--	-91	--	dBm
	18 Mbit/s	--	-89	--	dBm
	24 Mbit/s	--	-86	--	dBm
	36 Mbit/s	--	-83	--	dBm
	48 Mbit/s	--	-79	--	dBm
	54 Mbit/s	--	-77	--	dBm
Receiver sensitivity 802.11n HT20 (with BCC)	MCS0	--	-92	--	dBm
	MCS1	--	-90	--	dBm
	MCS2	--	-88	--	dBm
	MCS3	--	-85	--	dBm
	MCS4	--	-82	--	dBm
	MCS5	--	-77	--	dBm
	MCS6	--	-76	--	dBm
	MCS7	--	-74	--	dBm
Receiver sensitivity 802.11n HT40 (with BCC)	MCS0	--	-89	--	dBm
	MCS1	--	-87	--	dBm
	MCS2	--	-86	--	dBm
	MCS3	--	-83	--	dBm
	MCS4	--	-79	--	dBm
	MCS5	--	-75	--	dBm
	MCS6	--	-73	--	dBm
	MCS7	--	-72	--	dBm
Receiver maximum input level 802.11	802.11a	--	-3	--	dBm
	MCS0-7	--	-3	--	dBm
Receiver adjacent channel interference rejection (ACI) 802.11a	6 Mbit/s	--	30	--	dB
	9 Mbit/s	--	29	--	dB
	12 Mbit/s	--	29	--	dB

Parameter	Conditions	Min	Typ	Max	Unit
	18 Mbit/s	--	26	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11a (continued)	24 Mbit/s	--	26	--	dB
	36 Mbit/s	--	19	--	dB
	48 Mbit/s	--	16	--	dB
	54 Mbit/s	--	13	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11n HT20	MCS0	--	30	--	dB
	MCS1	--	28	--	dB
	MCS2	--	26	--	dB
	MCS3	--	24	--	dB
	MCS4	--	18	--	dB
	MCS5	--	14	--	dB
	MCS6	--	13	--	dB
	MCS7	--	9	--	dB

[1] Excludes an external LNA nominal gain of 16 dB. Gain can be extended if external LNA is not used.

8.3.4 2.4 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip output port.*

Table 28. 2.4 GHz Wi-Fi transmitter performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	--	2500	MHz
Transmit output saturation	Saturation power at chip output port	--	27	--	dBm
Transmit carrier suppression (CW)	Carrier suppression at chip output port	--	-36	--	dB
Transmit I/Q suppression with IQ calibration	I/Q suppression at chip output port	--	-45	--	dBc
Transmit power (EVM and mask compliant) 20 MHz per chain	802.11b	--	20	--	dBm
	OFDM BPSK	--	20	--	dBm
	OFDM QPSK	--	20	--	dBm
	OFDM 16-QAM	--	20	--	dBm
	OFDM 64-QAM (MCS7)	--	19	--	dBm
Transmit power (EVM and mask compliant) 40 MHz per chain	OFDM 64-QAM (MCS7)	--	18	--	dBm
Transmit output power level control range	--	--	20[1]	--	dB
Transmit output power control step	--	--	1[2]	--	dB
Transmit Carrier suppression	802.11b, 11 Mbit/s at 19 dBm, bandwidth = 20 MHz	--	37	--	dB

[1] 0-20 dB
[2] Hardware capability = 0.5 dB, software capability = 1 dB

8.3.5 5 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip output port.*

Table 29. 5 GHz Wi-Fi transmitter performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	5 GHz—IEEE 802.11n/a	4900	--	5925	MHz
Transmit output saturation	Saturation power at chip output	--	27	--	dBm
Transmit carrier suppression (CW)	Carrier suppression at chip output	--	-36	--	dB
Transmit I/Q suppression with IQ calibration	I/Q suppression at chip output	--	-45	--	dBc
Transmit power (EVM and mask compliant) 20 MHz per chain	OFDM BPSK	--	19	--	dBm
	OFDM QPSK	--	19	--	dBm
	OFDM 16-QAM	--	19	--	dBm
	OFDM 64-QAM (MCS7)	--	18	--	dBm
Transmit power (EVM and mask compliant) 40 MHz per chain	OFDM 64-QAM (MCS7)	--	17	--	dBm
Transmit output power level control range	--	--	20[1]	--	dB
Transmit output power control step	--	--	1[2]	--	dB
Transmit carrier suppression	802.11n MCS7 HT40, at 15 dBm	--	46	--	dBc

[1] 0-20 dBm
[2] Hardware capability = 0.5 dB, software capability = 1 dB

8.3.6 Local oscillator

Table 30. Local oscillator

Parameter	Condition	Min	Typ	Max	Unit
Phase noise	Measured at 2.438 GHz at 100 kHz offset	--	-103	--	dBc/Hz
	Measured at 5.501 GHz at 100 kHz offset	--	-100	--	dBc/Hz
Integrated RMS phase noise at RF output (from 10 kHz–10 MHz)	Reference clock frequency = 26 MHz (2.4 GHz)	--	0.35	--	degrees
	Reference clock frequency = 26 MHz (5 GHz)	--	0.65	--	degrees
Frequency resolution	--	0.02	--	--	kHz

8.4 Bluetooth radio specifications

The Bluetooth radio interface pin is powered by AVDD18 voltage supply.

8.4.1 Bluetooth/Bluetooth LE receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at chip output port.*

Table 31. Bluetooth/Bluetooth LE receiver performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	--	2.4	--	2.5	GHz
IF frequency	--	--	1.5	--	MHz
Input IP3 (at maximum gain of 72 dB)	--	--	-19	--	dBm
In-band blocking	**GFSK** C/I (Co-channel)	--	10	--	dB
	C/I (1 MHz)	--	-4	--	dB
	C/I (2 MHz)	--	-45	--	dB
	C/I (3 MHz)	--	-49	--	dB
	C/I (Image)	--	-21	--	dB
	C/I (Image ±1 MHz)	--	-32	--	dB
	Pi/4-DQPSK C/I (Co-channel)	--	10	--	dB
	C/I (1 MHz)	--	-9	--	dB
	C/I (2 MHz)	--	-47	--	dB
	C/I (3 MHz)	--	-51	--	dB
	C/I (Image)	--	-19	--	dB
	C/I (Image ±1 MHz)	--	-35	--	dB
	8-DPSK C/I (Co-channel)	--	16	--	dB
	C/I (1 MHz)	--	-6	--	dB
	C/I (2 MHz)	--	-42	--	dB
	C/I (3 MHz)	--	-48	--	dB
	C/I (Image)	--	-12	--	dB
	C/I (Image ±1 MHz)	--	-33	--	dB
Out-of-band blocking	30–2000 MHz	--	-12.5	--	dBm
	2–2.399 GHz	--	-12.4	--	dBm
	2.484–3 GHz	--	-18	--	dBm
	3–12.75 GHz	--	-2.6	--	dBm
RSSI Range	Resolution = 1 dB	--	-90	0	dBm
Sensitivity (RCV/CA/01/C, RCV/CA/02/C, and RCV/CA/07/C)	DH5	--	-96	--	dBm
	2DH5	--	-96	--	dBm
	3DH5	--	-89	--	dBm
Sensitivity (RCV-LE/CA/02/C)	LE 1 Mbit/s	--	-99	--	dBm

8.4.2 Bluetooth/Bluetooth LE transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and across frequency.*

Table 32. Bluetooth/Bluetooth LE transmitter performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	--	2.4	--	2.5	GHz
Output power @pin	Class 1 without external PA—BDR	--	+13	--	dBm
	Class 1 without external PA—EDR	--	+10	--	dBm
Gain range	Class 1 without external PA	--	30	--	dB
Gain resolution	--	--	0.5	--	dB
Spurious emission (BDR) (in-band)	±500 kHz	--	--	-20	dBc
	±2 MHz	--	-33	-20	dBm
	±3 MHz	--	-45	-40	dBm
Spurious emission (EDR) (in-band)	±1 MHz	--	--	-26	dBc
	±1.5 MHz	--	--	-20	dBm
	±2.5 MHz	--	--	-40	dBm
Spurious emission (out-of-band)	30–88 MHz	--	-65	-41.25	dBm
	88–960 MHz	--	-65	-41.25	
	0.96–20 GHz All frequencies in this range < -41.25 dBm, except at 2x Bluetooth channel frequency. Measured at pin without external filter.	--	-35	-25	
	Restricted—2.38–2.39 GHz	--	-55	-41.25	
	Restricted—2.4835–2.6 GHz	--	-50	-41.25	
Out-of-band/ Cellular band noise	GSM850 (869–894 MHz)	--	-140	--	dBm/Hz
	GSM900 (925–960 MHz)	--	-140	--	
	GSM DCS (1805–1880 MHz)	--	-135	--	
	GSM PCS (1930–1990 MHz)	--	-135	--	
	GPS (1575.42 ±1.023 MHz)	--	-140	--	
	WCDMA Band I (2110–2170 MHz)	--	-130	--	
	WCDMA Band V (869–894 MHz)	--	-140	--	
Transmit output power (TRM/CA/01/C)	DH5	--	13	--	dBm
Power control (TRM/CA/03/C)	--	--	4	--	dB
Frequency range (TRM/CA/04/C)	Freq Low	--	2400.9	--	MHz
	Freq High	--	2481.1	--	MHz
-20 dB bandwidth (TRM/CA/05/C)	DH5	--	955	--	MHz
Modulation characteristics (TRM/CA/07/C)	Delta F1 avg	--	165	--	kHz
	Delta F2 max Threshold	--	100	--	%

Parameter	Conditions	Min	Typ	Max	Unit
Modulation characteristics (TRM/CA/07/C) (continued)	Delta F2/Delta F1	--	0.9	--	--
	Delta F2 avg	--	145	--	kHz
ICFT (TRM/CA/08/C)	DH1	--	2	--	kHz
Carrier frequency drift (TRM/CA/09/C)	Max Drift - DH1	--	-3.5	--	kHz
	Drift Rate - DH1	--	1	--	kHz
	Max Drift - DH3	--	-4.5	--	kHz
	Drift Rate - DH3	--	1.5	--	kHz
	Max Drift - DH5	--	-5	--	kHz
	Drift Rate - DH5	--	1.5	--	kHz
EDR relative power (TRM/CA/10/C)	2DH5 (DPSK/GFSK)	--	-0.1	--	dB
	3DH5 (DPSK/GFSK)	--	-0.1	--	dB
EDR carrier frequency stability and modulation accuracy (TRM/CA/11/C)	2DH5 Peak DEVM	--	13	--	%
	2DH5 RMS DEVM	--	5	--	%
	3DH5 Peak DEVM	--	15	--	%
	3DH5 RMS DEVM	--	6	--	%
Diff. phase encoding (TRM/CA/12/C)	2DH5	--	100	--	%
	3DH5	--	100	--	%
Bluetooth LE output power (TRM/-LE/CA/01/C)	Bluetooth LE 1 Mbit/s	--	5	--	dBm
Bluetooth LE modulation characteristics (TRM-LE/CA/05/C)	Delta F1 avg - Bluetooth LE 1 Mbit/s	--	244	--	kHz
	Delta F2/Delta F1 Bluetooth LE 1 Mbit/s	--	0.9	--	kHz
	Delta F2 avg - Bluetooth LE 1 Mbit/s	--	222	--	kHz
Bluetooth LE carrier frequency drift (TRM-LE/CA/06/C)	Max Drift - Bluetooth LE 1 Mbit/s	--	1.5	--	kHz
	Drift Rate - Bluetooth LE 1 Mbit/s	--	1	--	kHz
Frequency accuracy (TRM-LE/CA/BV-06-C)	Bluetooth LE 1 Mbit/s	--	-3.5	--	kHz

8.5 Current consumption

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, across frequency, and at chip output port for transmit data is collected from SDIO-SDIO host interface configuration.*

Table 33. Current consumption

Mode	Conditions	2.2V	1.8V	1.1V	Unit
Sleep mode	Power down	0	0.002	0.001	mA
	Wi-Fi and Bluetooth in deep sleep mode	0.001	0.01	0.291	mA
	Bluetooth only in deep sleep mode	0.001	0.01	0.195	mA
	Bluetooth LE only in deep sleep mode	0.001	0.01	0.153	mA
Bluetooth LE (Wi-Fi in deep sleep mode)	Bluetooth LE link (master mode, interval=1.28s)	0.001	0.064	0.232	mA
	Bluetooth LE peak tranmsit (at 0 dBm), 1 Mbit/s	0.001	16	30	mA
	Bluetooth LE peak receive, 1 Mbit/s	0.001	18	15	mA
	Bluetooth LE advertise(interval=1.28s)	0.001	0.047	0.197	mA
	Bluetooth LE scan (interval = 1.28s, window = 11.25 ms)	0.001	0.154	0.28	mA
Bluetooth (Wi-Fi in deep sleep mode)	Bluetooth page scan	0.001	0.203	0.495	mA
	Bluetooth page and inquiry scan	0.001	0.353	0.622	mA
	Bluetooth ACL link, master sniff mode, (interval = 1.28s)	0.001	0.078	0.427	mA
	Bluetooth ACL link, master sniff mode, (interval=500ms)	0.001	0.193	0.604	mA
	Bluetooth ACL (data pump) DH1	0.001	10	17	mA
	Bluetooth ACL (data pump) 3-DH5	0.001	23	14	mA
	Bluetooth SCO HV3 peak transmit (at device maximum power)	0.001	88	14	mA
	Bluetooth SCO HV3 peak Rx	0.001	18	15	mA
	Bluetooth SCO HV3 Peak transmit (at 4 dBm)	0.001	17	37	mA
IEEE power save (Beacon interval: 100 msec)	IEEE-PS_2GHz-Legacy (DTIM-1)	0.001	0.916	0.886	mA
	IEEE-PS_2GHz-Legacy (DTIM-3)	0.001	0.42	0.502	mA
	IEEE-PS_2GHz-Legacy (DTIM-5)	0.001	0.274	0.439	mA
2.4 GHz Wi-Fi receive (Bluetooth in deep sleep mode)	802.11b, 11 Mbit/s, 1x1	0.005	36	24	mA
	802.11g, 54 Mbit/s, 1x1	0.005	37	32	mA
	802.11n, HT20 MCS7, 1x1	0.005	35	40	mA
5 GHz Wi-Fi receive (Bluetooth in deep sleep mode)	802.11a, 54 Mbit/s, 1x1	0.005	53	32	mA
	802.11n, HT20 MCS7, 1x1	0.005	52	40	mA
	802.11n, HT40 MCS7, 1x1	0.005	60	53	mA

Mode	Conditions	2.2V	1.8V	1.1V	Unit
2.4 GHz Wi-Fi transmit	802.11b, 11 Mbit/s at 16 dBm, 1x1	225	93	83	mA
	802.11g, 54 Mbit/s at 15 dBm, 1x1	185	91	95	mA
	802.11n, HT20 MCS7 at 14 dBm, 1x1	164	90	97	mA
5 GHz Wi-Fi transmit	802.11a, 54 Mbit/s at 15 dBm, 1x1	186	147	98	mA
	802.11n, HT20 MCS7 at 15 dBm, 1x1	185	148	105	mA
	802.11n, HT40 MCS7 at 14 dBm, 1x1	168	148	114	mA
Current consumption during device initialization	Max current consumption during device initialization	950	254	150	mA

8.6 Coexistence specifications

The 88W8977 MWS coexistence interface pins are powered by VIO voltage supply. Refer to the MWS standard for additional interface specifications.

See Section 8.1.1 "VIO DC characteristics" for specifications.

8.7 SDIO host interface specifications

The SDIO host interface pins are powered by VIO_SD voltage supply.

The SDIO electrical specifications are identical for 4-bit SDIO and 1-bit SDIO transfer modes.

8.7.1 VIO_SD DC characteristics

8.7.1.1 1.8V operation

Table 34. DC electricals—1.8V operation (VIO_SD)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_SD-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.7.1.2 3.3V operation

Table 35. DC electricals—3.3V operation (VIO_SD)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_SD-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.7.2 Default speed mode and high-speed mode

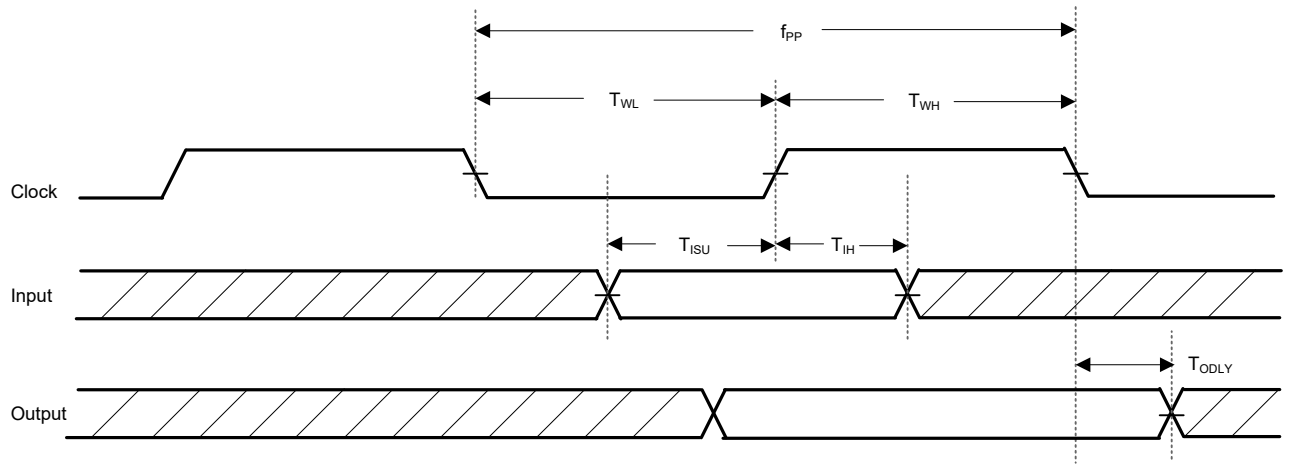


Figure 13. SDIO protocol timing diagram—Default speed mode (3.3V)

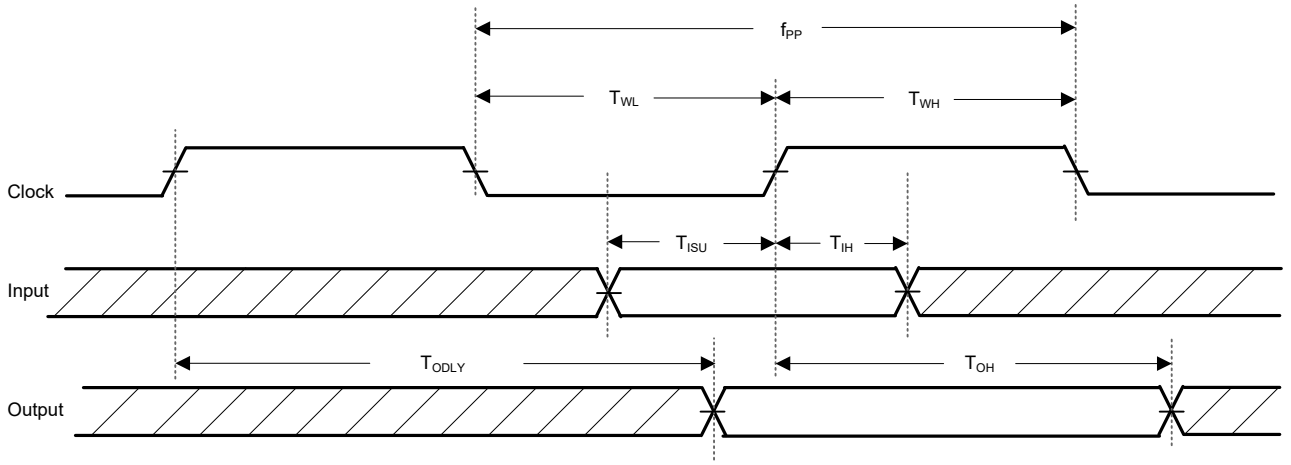


Figure 14. SDIO protocol timing diagram—High-speed mode (3.3V)

Table 36. SDIO timing data—Default speed mode and high-speed modes (3.3V)[1], [2]

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{WH}	Clock high time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{ISU}	Input setup time	Normal	5	--	--	ns
		High-speed	6	--	--	ns
T_{IH}	Input hold time	Normal	5	--	--	ns
		High-speed	2	--	--	ns
T_{ODLY}	Output delay time	Normal	--	--	14	ns
	CL ≤ 40 pF (1 card)	High-speed	--	--	14	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

[1] For SDIO 2.0 running at 50 MHz clock frequency, only 1.8V is supported.
[2] For SDIO 2.0 running at 25 MHz clock frequency, 1.8V or 3.3V is supported.

8.7.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

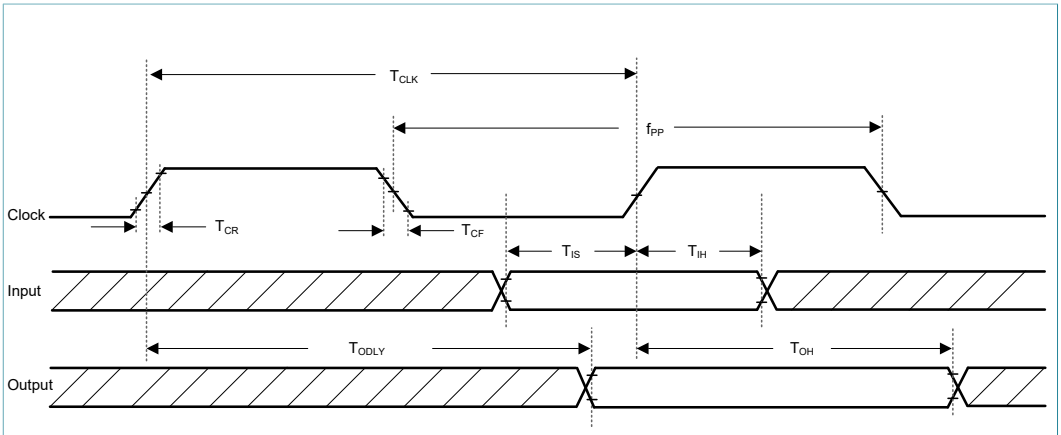


Figure 15. SDIO protocol timing diagram—SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Table 37. SDIO timing data——SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

8.7.4 DDR50 Mode (50 MHz) (1.8V)

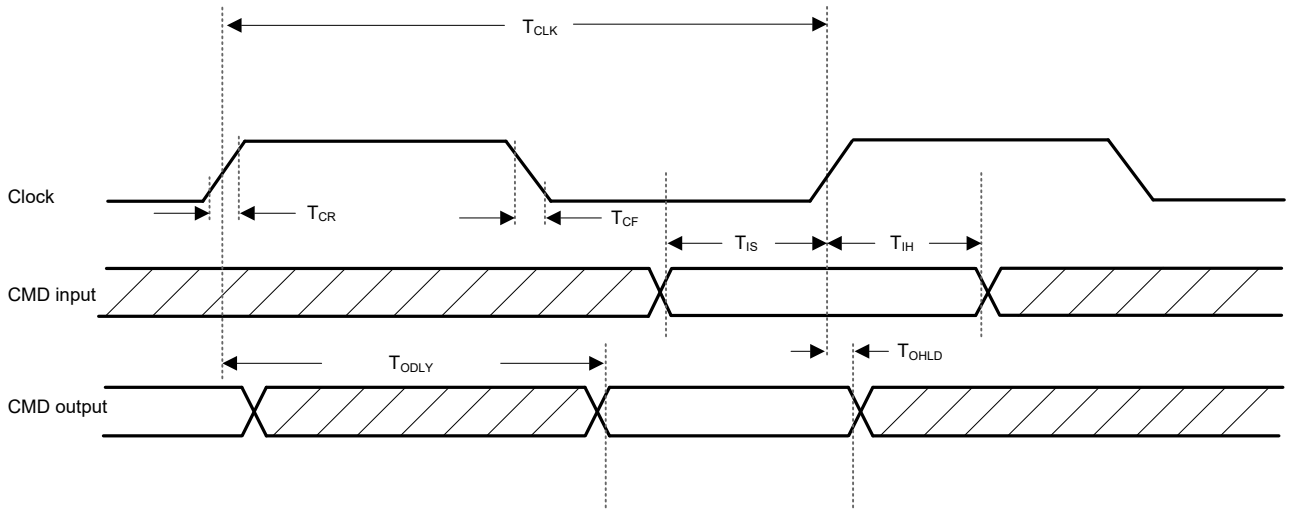


Figure 16. SDIO CMD timing diagram—DDR50 Mode (50 MHz)

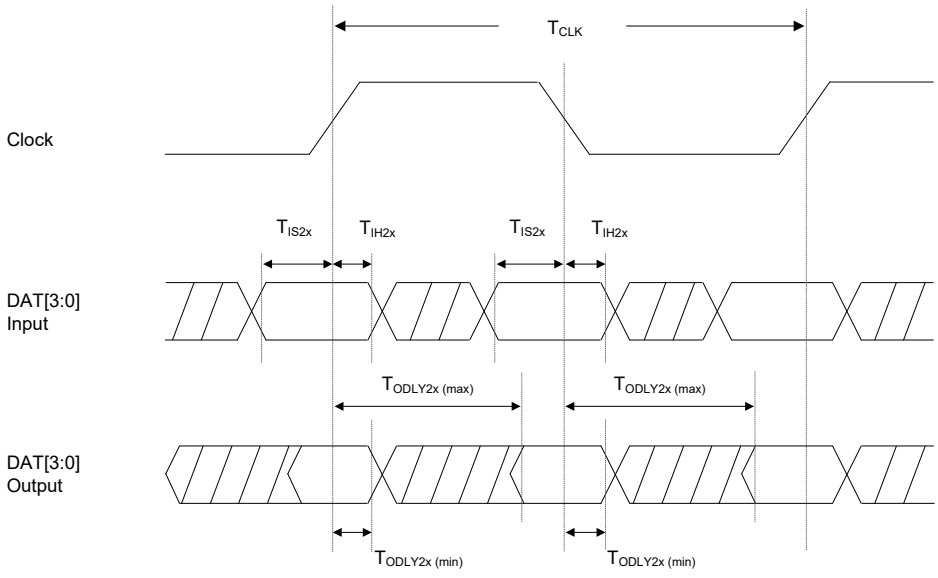


Figure 17. SDIO DAT[3:0] timing diagram—DDR50 mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Table 38. SDIO timing data—DDR50 mode (50 MHz)

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	--	--	0.2*T_{CLK}	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	--	--	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	--	--	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	--	--	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
T_{ODLY2x} (max)	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	--	--	7.0	ns
T_{ODLY2x} (min)	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns

8.8 UART interface specifications

The UART transmit and receive pins are powered by VIO voltage supply.

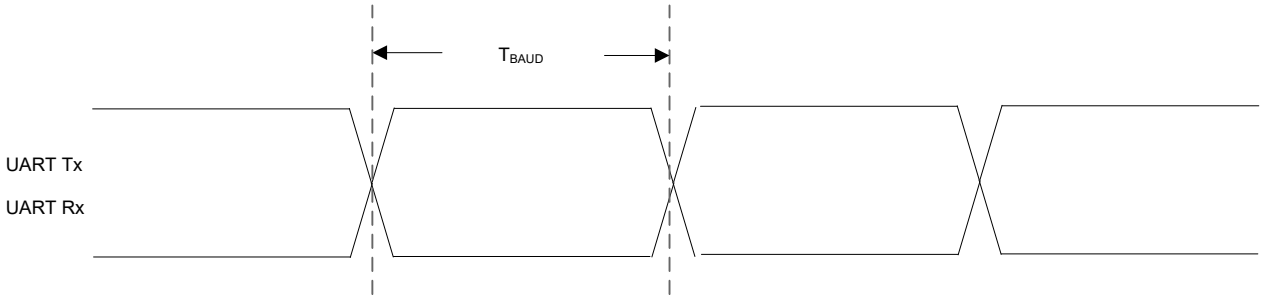


Figure 18. Figure Caption

Table 39. UART timing data[1]

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{BAUD}	Baud rate	26 MHz input clock	250	--	--	ns

[1] The acceptable deviation from the UART Rx target baud rate is ±3%.

8.9 PCM interface specifications

The PCM pins are powered by VIO voltage supply.

See Section 8.1.1 "VIO DC characteristics" for specifications.

Table 40. PCM timing specification diagram for data signals—Master mode

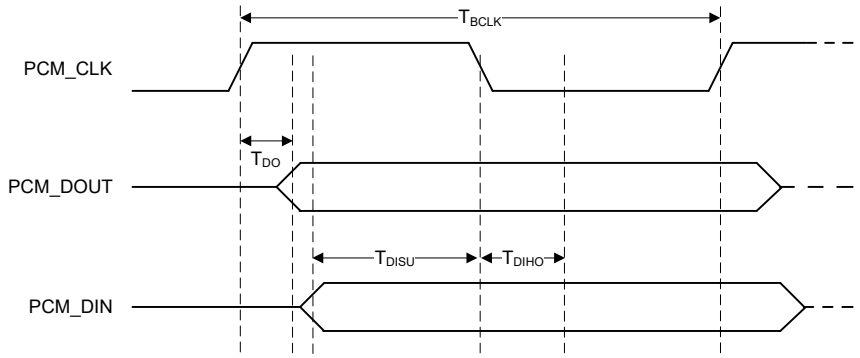


Table 41. PCM timing specification diagram for sync signal—Master mode

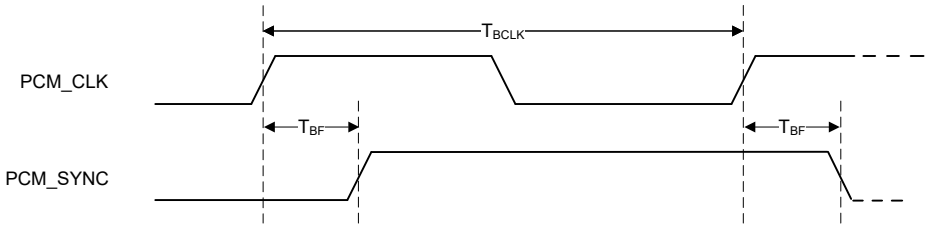


Table 42. PCM timing specification data—Master mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

Table 43. PCM timing specification diagram for data signals—Slave mode

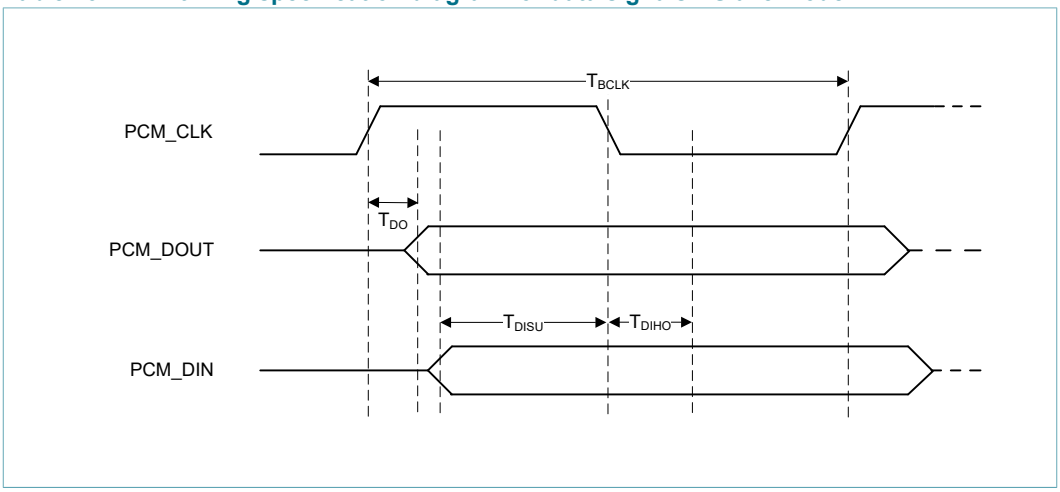


Table 44. PCM timing specification diagram for sync signal—Slave mode

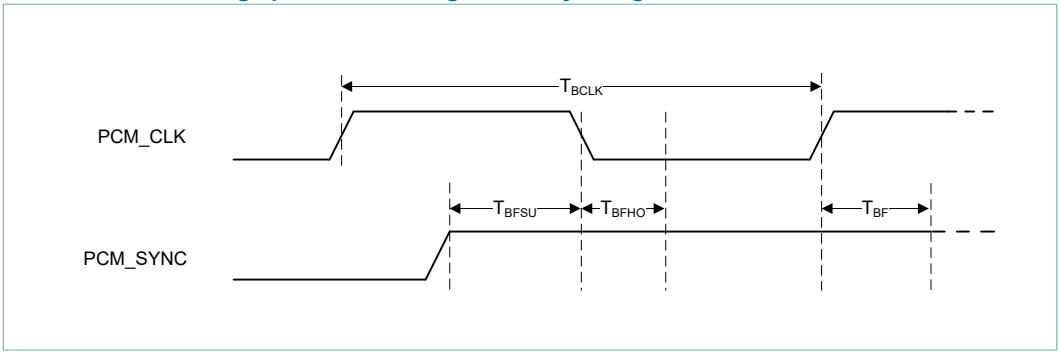


Table 45. PCM timing specification data—Slave mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

8.10 Clock specifications

8.10.1 Single-ended clock input modes

8.10.1.1 2.4 GHz mode

Table 46. CMOS mode[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	AVDD18 - 0.5	AVDD18	1.98	V
V_{IL}	Input low voltage	--	0	0	0.4	V

[1] Typical input capacitance is approximately 2 pF and input resistance is >20 kΩ.

Table 47. Low-Swing Mode[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VLS_IH	Single-ended high-level voltage	--	--	--	1.8	V
VLS_IL	Single-ended low-level voltage	--	0	--	--	V
VLS_Amp	Low-swing clock amplitude (pk-pk)	--	0.5	--	--	V
VLS_Slope	Low-swing mid-point slope	--	100	--	--	MV/s
Duty	Duty cycle	--	45	50	55	%

[1] AC-coupling capacitor is integrated into the SoC.

Table 48. Phase Noise—2.4 GHz operation

Parameter	Condition	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	--	--	-126	dBc /Hz
	Offset = 10 kHz	--	--	-137	dBc /Hz
	Offset = 100 kHz	--	--	-145	dBc /Hz
	Offset > 1 MHz	--	--	-145	dBc /Hz

8.10.1.2 2.4 GHz and 5 GHz dual-band mode

Table 49. Phase noise—Dual-band operation

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	--	--	-130	dBc/Hz
	Offset = 10 kHz	--	--	-150	dBc/Hz
	Offset = 100 kHz	--	--	-156	dBc/Hz
	Offset > 1 MHz	--	--	-156	dBc/Hz

8.10.2 Crystal

Table 50. Crystal specifications

Parameter	Condition	Typical	Unit
Fundamental frequencies	--	26	MHz
Frequency tolerance	Over operating temperature	< ±10	ppm
	Over process at 25ºC	< ±10	ppm
SMD and AT cut height	--	<1.2	mm
Load Capacitance	--	5	pF
Maximum series resistance	--	45	Ω
Resonance mode	--	A1, Fundamental	--

8.10.3 Sleep clock

Table 51. External sleep clock timing

Limited to within 10°C variance.

Symbol	Parameter	Min	Typ	Max	Unit
CLK	Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)	--	32.768	--	kHz
V_{IH}	Input levels, where VIO = 1.8, 2.5, 3.3V For VIH, VIL, see Section Section 8.1.1 "VIO DC characteristics".	0.7*VIO	--	VIO+0.4	V
V_{IL}		-0.4	--	0.3*VIO	V
PN	Phase noise requirement (at 100 kHz)	--	-125	--	dBc /Hz
Jc	Cycle jitter	--	1.5	--	ns (RMS)
SR	Slew rate limit (10-90%)	--	--	100	ns
DC	Duty cycle tolerance	20	--	80	%

8.11 JTAG interface specifications

The JTAG interface pins are powered by VIO voltage supply.

See Section 8.1.1 "VIO DC characteristics" for specifications.

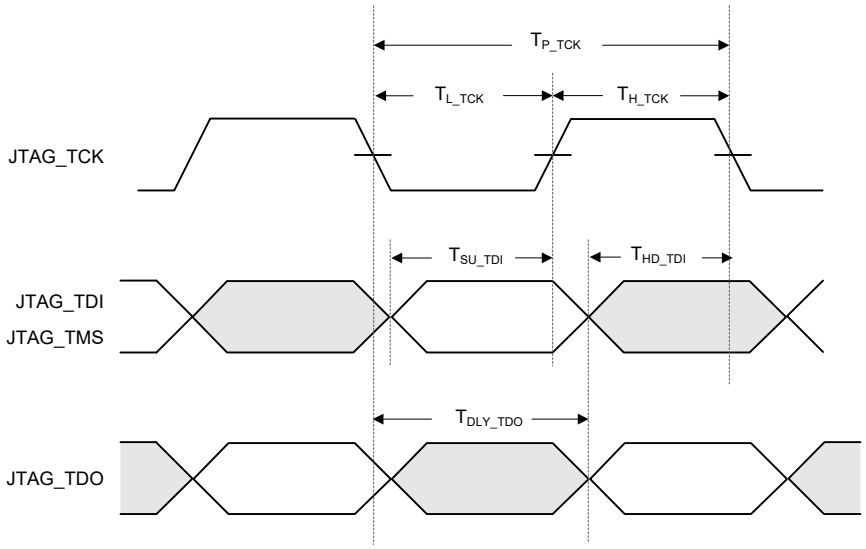


Figure 19. JTAG timing diagram

Table 52. JTAG timing data[1]

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_TCK}	TCK period	--	40	--	--	ns
T_{H_TCK}	TCK high	--	12	--	--	ns
T_{L_TCK}	TCK low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO delay	--	0	--	15	ns

[1] Does not apply to JTAG enabled by the JTAG_TMS pin.

9 Package information

9.1 Package thermal conditions

9.1.1 QFN package thermal conditions

Table 53. Thermal conditions of QFN package

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Thermal resistance Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	28.4	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 1 meter/sec air flow	27.6	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 2 meter/sec air flow	26.1	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 3 meter/sec air flow	25.3	°C/W
ψ_{JT}	Thermal characteristic parameter[1] Junction to top-center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top-center of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	0.44	°C/W
ψ_{JB}	Thermal characteristic parameter[1] Junction to bottom surface, center of PCB. $\psi_{JT} = (T_J - T_B)/P$ T_B = surface temperature of PCB	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	15.4	°C/W
θ_{JC}	Thermal resistance[1] Junction to case of the package. $\theta_{JC} = (T_J - T_C)/ P_{TOP}$ T_C = temperature on top-center of package P_{TOP} = power dissipation from top of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	13.0	°C/W
θ_{JB}	Thermal resistance[1] Junction to board of package. $\theta_{JB} = (T_J - T_B)/ P_{BOTTOM}$ P_{BOTTOM} = power dissipation from bottom of package to PCB surface	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	15.6	°C/W

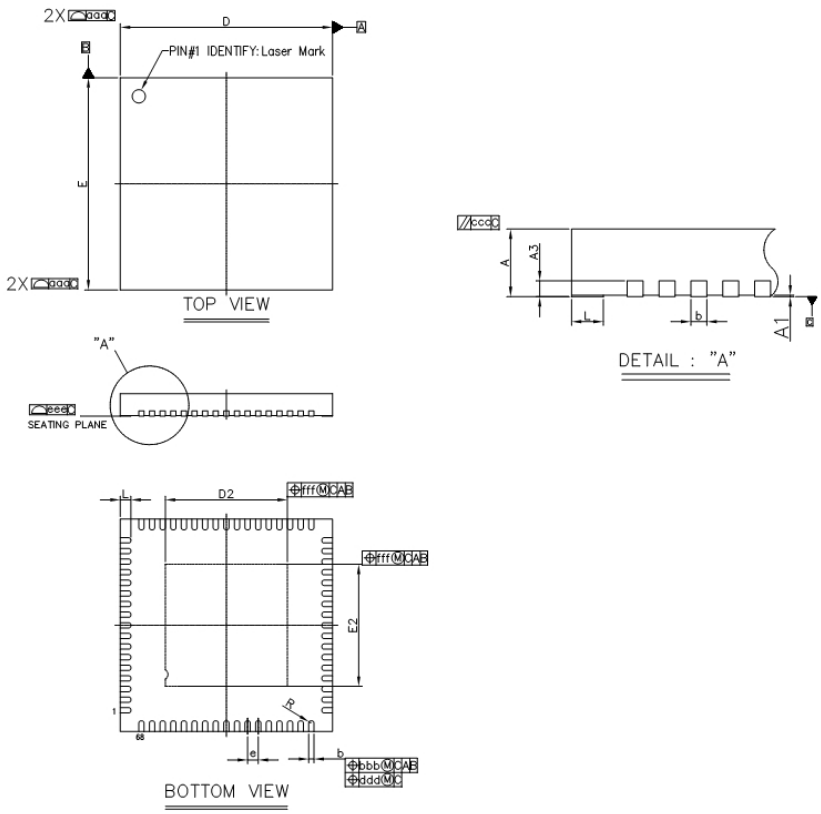
9.1.2 eWLP package thermal conditions

Table 54. Thermal conditions of eWLP package

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Thermal resistance Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB no air flow	44.22	°C/W
ψ_{JT}	Thermal characteristic parameter[1] Junction to top-center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top-center of package	JEDEC 4 in. x 4.5 in. 4-layer PCB no air flow	0.56	°C/W
ψ_{JB}	Thermal characteristic parameter[1] Junction to bottom-center of PCB. $\psi_{JT} = (T_J - T_{BOTTOM})/P$ T_B = temperature on bottom-center of package	JEDEC 4 in. x 4.5 in. 4-layer PCB no air flow	13.93	°C/W

9.2 Package mechanical data

9.2.1 68-pin QFN package mechanical drawing

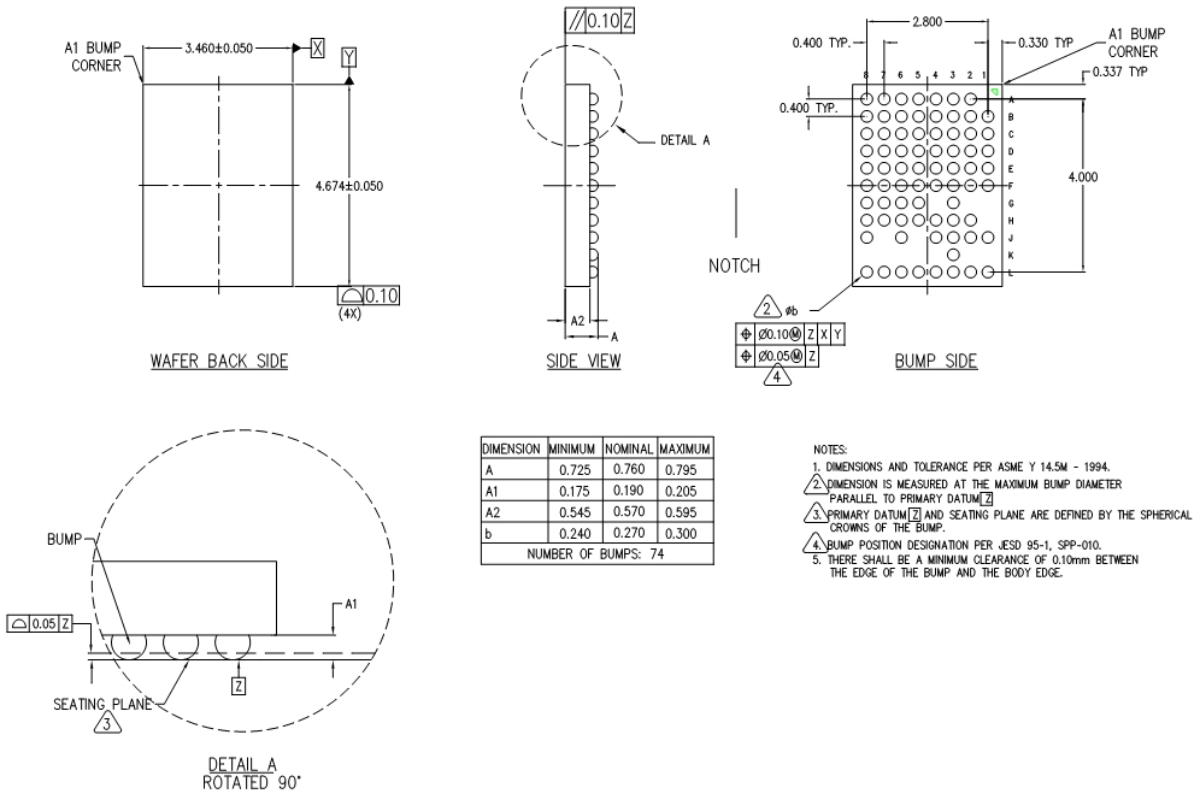


Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	7.90	8.00	8.10
e		0.40 BSC	
L	0.30	0.40	0.50
R	0.075	---	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

EPad Size	
Symbol	Dimension in mm
D2	3.60 ± 0.10
E2	4.60 ± 0.10

Figure 20. 68-pin QFN package mechanical drawing

9.2.2 74-bump eWLP package mechanical drawing



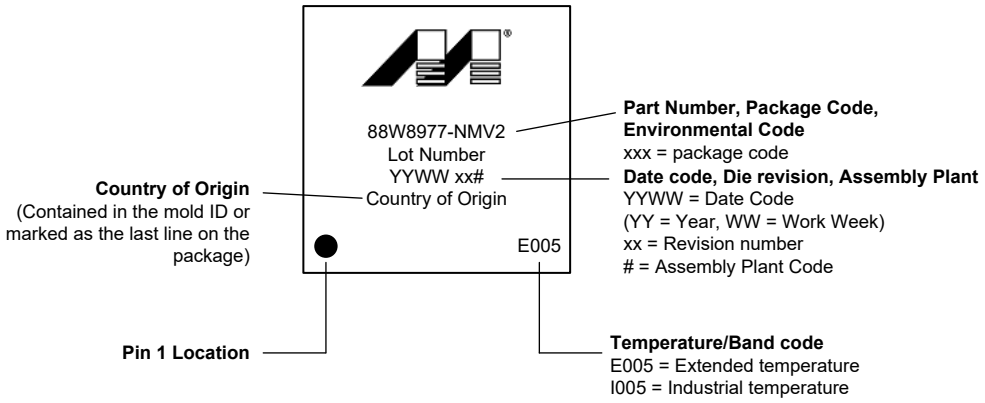
DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.725	0.760	0.795
A1	0.175	0.190	0.205
A2	0.545	0.570	0.595
b	0.240	0.270	0.300
NUMBER OF BUMPS: 74			

NOTES:
1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M - 1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM BUMP DIAMETER PARALLEL TO PRIMARY DATUM Z
3. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BUMP.
4. BUMP POSITION DESIGNATION PER JESD 95-1, SPP-010.
5. THERE SHALL BE A MINIMUM CLEARANCE OF 0.10mm BETWEEN THE EDGE OF THE BUMP AND THE BODY EDGE.

Figure 21. 74-bump package mechanical drawing

9.3 Package marking

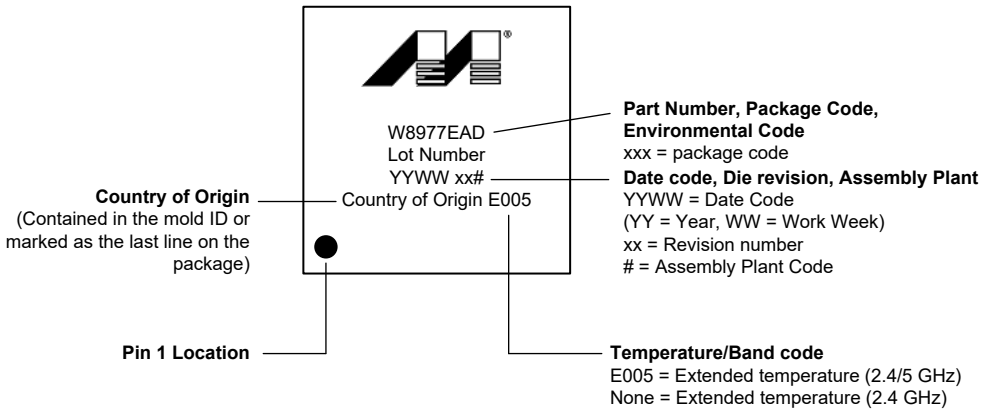
9.3.1 68-pin QFN package marking



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 22. 68-pin QFN package marking and pin 1 location

9.3.2 74-bump eWLP package marking



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 23. 74-bump eWLP package marking and pin 1 location

10 Ordering information

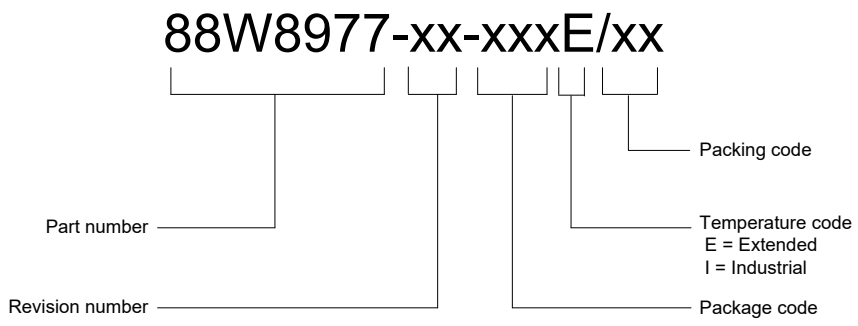


Figure 24. Part numbering scheme

Table 55. Part Order Codes

Part Order Code	Package Type	Packing
88W8977-A1-NMVE/AK	68-pin MQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tray
88W8977-A1-NMVE/AZ	68-pin MQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tape and Reel
88W8977-A1-NMVI/AK	68-pin MQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tray
88W8977-A1-NMVI/AZ	68-pin MQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tape and Reel
88W8977-A1-EADE/AZ	74-bump eWLP - 4.674 x 3.46 x 0.76 mm, with 0.4 mm pitch	Tape and Reel

11 Acronyms and abbreviations

Table 56. Acronyms and abbreviations

Acronym	Definition
A2DP	Advanced Audio Distribution Profiles
ABR	Automatic Baud Rate
ACK	Acknowledgment
ADAS	Advanced Driver Assistance Systems
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Correction
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIFS	Arbitration Interframe Space
AoA	Angle of Arrival
AoD	Angle of Departure
AP	Access Point
APB	Advanced Peripheral Bus
API	Application Program Interface
aQFN	Advanced Quad Flat Non-leaded Package
ARM	Advanced RISC Machine
ATIM	Announcement Traffic Indication Message
BAMR	Base Address Mask Register
BAR	Base Address Register
BBU	Baseband Processor Unit
BCB	Benzocyclobutene (flip chip bump process)
BDR	Basic Data Rate
BER	Bit Error Rate
BOM	Bill of Materials
BR	Baud Rate
BSS	Basic Service Set
BSSID	Basic Service Set Identifier
BTU	Bluetooth Baseband Unit
BRF	Bluetooth RF Unit
BWQ	Bandwidth Queue
CBC	Cipher Block Chaining
CBP	Contention-Based Period
CCA	Clear Channel Assessment

Acronym	Definition
CCK	Complementary Code Keying
CCMP	Counter Mode CBC-MAC Protocol
CDE	Close Descriptor Enable
CFP	Contention-Free Period
CFQ	Contention-Free Queue
CID	Connection Identifier
CIS	Card Information Structure
CIU	CPU Interface Unit
CMD	Command
CMQ	Control Management Queue
CRC	Cyclic Redundancy Check
CS	Card Select
CSMA/CA	Carrier Sense Multiple Access / Collision Avoidance
CSMA/CD	Carrier Sense Multiple Access / Collision Detection
CSU	Clocked Serial Unit
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DBPSK	Differential Binary Phase Shift Keying
DCD	Device Controller Driver
DCE	Data Communication Equipment
DCF	Distributed Coordination Function
DCLA	Direct Current Level Adjustment
DCLB	Digital Contactless Bridge
DCU	DMA Controller Unit
DFS	Dynamic Frequency Selection
DIFS	Distributed Interframe Space
DMA	Direct Memory Access
dQH	Device Queue Head
DQPSK	Differential Quadrature Phase Shift Keying
DSM	Distribution System Medium
DSP	Digital Signal Processor
DSRC	Dedicated Short Range Communications
dTD	Linked List Transfer Descriptors
DTIM	Delivery Traffic Indication Message
DVSC	Digital Voltage Scaling Control
EAP	Extensible Authentication Protocol
EBRAM	Extended Block Random Access Memory

Acronym	Definition
ED	Energy Detect
EDCA	Enhanced Distributed Channel Access
EEPROM	Electrically Erasable Programmable Read Only Memory
EIFS	Extended Interframe Space
EMC	Electromagnetic Compatibility
ERP-OFDM	Extended Rate PHY-Orthogonal Frequency Division Multiplexing
ETSI	European Telecommunications Standards Institute
eWLP	Embedded Wafer Level Package
FAE	Field Application Engineer
FCC	Federal Communications Commission
FIFO	First In First Out
FIPS	Federal Information Processing Standards
FIQ	Fast Interrupt Request
FW	Firmware
GATT	Generic Attribute Profile
GCMP	Galois/Counter Mode Protocol
GI	Guard Interval
GPIO	General Purpose Input/Output
GPL	General Public License
GPU	General Purpose Input/Output Unit
HID	Human Interface Device
HIU	Host Interface Unit
HOGP	HID Over GATT Profile
HSP	Hands-Free Profile
HT	High Throughput
HW	Hardware
I/Q	Inphase/Quadrature
IB	InBand
IBSS	Independent Basic Service Set
ICE	In-Circuit Emulator (or Emulation)
ICR	Interrupt Cause Register
ICU	Interrupt Controller Unit
ICV	Integrity Check Value
IE	Information Element
IEEE	Institute of Electrical and Electronics Engineers
IEMR	Interrupt Event Mask Register
I/F	Interface

Acronym	Definition
IFS	Interframe Space
IMR	Interrupt Mask Register
IPG	Inter-Packet Gap
IPsec	Internet Protocol Security
IR	Infrared
IRQ	Interrupt Request
ISA	Instruction Set Architecture
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific, and Medical
ISMR	Interrupt Status Mask Register
ISR	Interrupt Status Register
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Action Group
LDPC	Low Density Parity Check
LE	Low Energy
LED	Light Emitting Diode
LME	Layer Management Entity
LNA	Low Noise Amplifier
LPM	Low Power Management
LQFN	Low Quad Flat Non-leaded
LSb	Least Significant bit
LSB	Least Significant Byte
LSP	Low-Speed Peripheral
LTE	Long Term Evolution
MAC	Media/Medium Access Controller
MC	Memory Controller
MCS	Modulation and Coding Scheme
MCU	MAC Control Unit
MDI	Modem Data Interface
MIB	Management Information Base
MIC	Message Integrity Code
MII	Media Independent Interface
MIMO	Multiple Input Multiple Output
MIPS	Million Instructions Per Second
MLME	MAC Sublayer Management Entity
MMI	Modem Management Interface
MMPDU	MAC Management Protocol Data Unit

Acronym	Definition
MMU	Memory Management Unit
MPDU	MAC Protocol Data Unit
MSb	Most Significant bit
MSB	Most Significant Byte
MSDU	MAC Service Data Unit
MU-MIMO	Multi-User MIMO
MU-PPDU	Multi-User PPDU
MWS	Mobile Wireless System Multimedia Wireless System
NAV	Network Allocation Vector
NDP	Null Data Packet
NL	No Load
NPTR	Next Descriptor Pointer
OCB	Outside the Context of a BSS
OFDM	Orthogonal Frequency Division Multiplexing
OID	Object Identifier
OOB	Out of Band
OTP	One Time Programmable
P2P	Peer-to-Peer
PA	Power Amplifier
PAD	Packet Assembler/Disassembler
PBU	Peripheral Bus Unit
PC	Point Coordinator
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCM	Pulse Code Modulation
PDn	Power Down
PDU	Protocol Data Unit
PEAP	Protected EAP
PHY	Physical Layer
PIFS	Priority Interframe Space
PLL	Phase-Locked Loop
PLME	Physical Layer Management Entity
PMU	Power Management Unit
POST	Power-On Self Test

Acronym	Definition
PPDU	PHY Protocol Data Unit
PPK	Per-Packet Key
PPM	Pulse Position Modulation
PSK	Pre-Shared Keys
PTA	Packet Traffic Arbitration
PWK	Pairwise Key
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non-leaded Package
QoS	Quality of Service
RA	Receiver Address
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RFID	Radio Frequency Identification
RIFS	Reduced Interframe Space
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RSSI	Receiver Signal Strength Indication
RTS	Request to Send
RTU	General Purpose Timer Unit
RU	Resource Unit
SA	Source Address
SAP	Service Access Point
SCLK	Serial Interface Clock
SDA	Serial Interface Data
SE	Secure Element
SFD	Start of Frame Delimiter
SIFS	Short Interframe Space
SISO	Single Input Single Output
SIU	Serial Interface Unit (UART)
SJU	System/Software JTAG Controller Unit
SM	Switch Module
SMI	Serial Management Interface
SNR	Signal-to-Noise Ratio
SO	Serial Out
SoC	System-on-Chip
SPDT	Single Pole Double Throw

Acronym	Definition
SPI	Serial Peripheral Interface
SQU	Internal SRAM Unit
SRWB	Serial Interface Read Write
SS	Service Set
SSID	Service Set Identifier
STA	Station
STBC	Space-Time Block Code
SWD	Serial Wire Debug
SWP	Single Wire Protocol
TA	Transmitter Address
TBG	Time Base Generator
TBTT	Target Beacon Transmission Time
TCM	Tightly Coupled Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
TCQ	Traffic Category Queue
TIM	Traffic Indication Map
TKIP	Temporal Key Integrity Protocol
TPC	Transmit Power Control
TQFP	Thin Quad Flat Pack
TRPC	Transmit Rate-based Power Control
TSC	TKIP Sequence Counter
TSF	Timing Synchronization Function
TWT	Target Wait Time
UART	Universal Asynchronous Receiver/Transmitter
UBM	Under Bump Metal
UDP	User Datagram Protocol
UNII	Unlicensed National Information Infrastructure
VCO	Voltage Controlled Oscillator
VIF	Voice Interface
VHT	Very High Throughput
WAP	Wireless Application Protocol
WAVE	Wireless Access in Vehicular Environments
WCI-2	Wireless Coexistence Interface 2
WEP	Wired Equivalent Privacy
WI	Wired Interface
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless Local Area Network

Acronym	Definition
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPA2	Wi-Fi Protected Access 2
WPA2-PSK	Wi-Fi Protected Access 2-Pre-Shared Key
WPA-PSK	Wi-Fi Protect Access-Pre-Shared Key
XFQFN	Extra-Fine Quad Flat Non-leaded
XOSC	Crystal Oscillator

12 Revision history

Table 57. Revision history

Revision	Date	Description
Rev. 1	13-Jul-2020	Initial release

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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