ATD_10B16C
Block User Guide
V03.00

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V03.00	9 Oct. 2002	9 Oct. 2002		Copied from spec version 2. Added: configurable external trigger pin (ATDCTL1) configurable multi channel wrap (ATDCTL0) Improved register descriptions: ATDTEST0, ATDTEST1, ATDDR*x*

Table 0-1 Revision History

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Section 1 Introduction

1.1 Overview

The ATD_10B16C is an 16-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

The block is designed to be upwards compatible with the 68HC11 standard 10/8-bit A/D converter. In addition, there are new operating modes that are unique to the HC12 design.

1.2 Features

- 8/10 Bit Resolution.
- 7 µsec, 10-Bit Single Conversion Time.
- Sample Buffer Amplifier.
- Programmable Sample Time.
- Left/Right Justified, Signed/Unsigned Result Data.
- External Trigger Control.
- Conversion Completion Interrupt Generation.
- Analog Input Multiplexer for 16 Analog Input Channels.
- Analog/Digital Input Pin Multiplexing.
- 1 to 16 Conversion Sequence Lengths.
- Continuous Conversion Mode.
- Multiple Channel Scans.
- Configurable external trigger functionality on any ATD channel.
- Configurable location for channel wrap around (when converting multiple channels in a sequence).

1.3 Modes of Operation

1.3.1 Conversion modes

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

1.3.2 MCU Operating Modes

- **Stop Mode**
  Entering Stop Mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This halts any conversion sequence in progress. During recovery from Stop Mode, there must be a minimum delay for the Stop Recovery Time t_{SR} before initiating a new ATD conversion sequence.
- **Wait Mode**
  Entering Wait Mode the ATD conversion either continues or halts for low power depending on the logical value of the AWAIT bit.
- **Freeze Mode**
  In Freeze Mode the ATD_10B16C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

1.4 Block Diagram

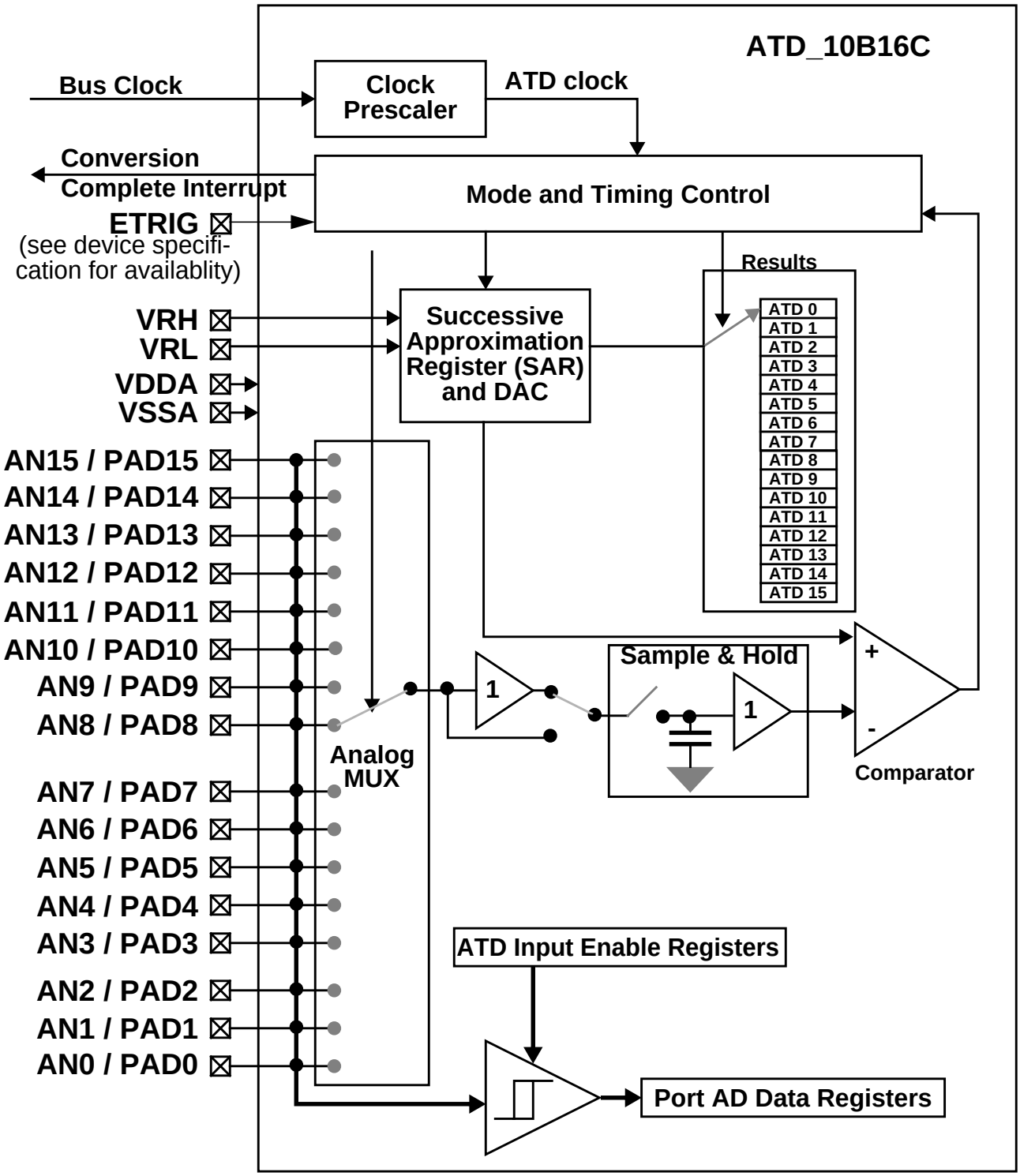

Figure 1-1 ATD_10B16C Block Diagram

Section 2 Signal Description

2.1 Overview

The ATD_10B16C has a total of 21 external pins.

2.2 Detailed Signal Descriptions

2.2.1 AN*x* / PAD*x* (*x* = 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as general purpose digital input and/or external trigger for the ATD conversion.

2.2.2 ETRIG

This pin can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of this pin!

2.2.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

2.2.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ATD_10B16C block.

Section 3 Memory Map and Register Definition

3.1 Overview

This section provides a detailed description of all registers accessible in the ATD_10B16C.

3.2 Module Memory Map

Table 3-1 gives an overview on all ATD_10B16C registers.

Table 3-1 Module Memory Map

Address Offset	Use	Access
$_00	ATD Control Register 0 (ATDCTL0)	R/W
$_01	ATD Control Register 1 (ATDCTL1)	R/W
$_02	ATD Control Register 2 (ATDCTL2)	R/W
$_03	ATD Control Register 3 (ATDCTL3)	R/W
$_04	ATD Control Register 4 (ATDCTL4)	R/W
$_05	ATD Control Register5 (ATDCTL5)	R/W
$_06	ATD Status Register 0 (ATDSTAT0)	R/W
$_07	Unimplemented	
$_08	ATD Test Register 0 (ATDTEST0)[1]	R
$_09	ATD Test Register 1 (ATDTEST1)	R/W
$_0A	ATD Status Register 2 (ATDSTAT2)	R
$_0B	ATD Status Register 1 (ATDSTAT1)	R
$_0C	ATD Input Enable Register 0 (ATDDIEN0)	R/W
$_0D	ATD Input Enable Register 1 (ATDDIEN1)	R/W
$_0E	Port Data Register 0 (PORTAD0)	R
$_0F	Port Data Register 1 (PORTAD1)	R
$_10, $_11	ATD Result Register 0 (ATDDR0H, ATDDR0L)	R/W
$_12, $_13	ATD Result Register 1 (ATDDR1H, ATDDR1L)	R/W
$_14, $_15	ATD Result Register 2 (ATDDR2H, ATDDR2L)	R/W
$_16, $_17	ATD Result Register 3 (ATDDR3H, ATDDR3L)	R/W
$_18, $_19	ATD Result Register 4 (ATDDR4H, ATDDR4L)	R/W
$_1A, $_1B	ATD Result Register 5 (ATDDR5H, ATDDR5L)	R/W
$_1C, $_1D	ATD Result Register 6 (ATDDR6H, ATDDR6L)	R/W
$_1E, $_1F	ATD Result Register 7 (ATDDR7H, ATDDR7L)	R/W
$_20, $_21	ATD Result Register 8 (ATDDR8H, ATDDR8L)	R/W
$_22, $_23	ATD Result Register 9 (ATDDR9H, ATDDR9L)	R/W
$_24, $_25	ATD Result Register 10 (ATDDR10H, ATDDR10L)	R/W
$_26, $_27	ATD Result Register 11 (ATDDR11H, ATDDR11L)	R/W
$_28, $_29	ATD Result Register 12 (ATDDR12H, ATDDR12L)	R/W
$_2A, $_2B	ATD Result Register 13 (ATDDR13H, ATDDR13L)	R/W
$_2C, $_2D	ATD Result Register 14 (ATDDR14H, ATDDR14L)	R/W

Table 3-1 Module Memory Map

$_2E, $_2F	ATD Result Register 15 (ATDDR15H, ATDDR15L)	R/W

NOTES:
1. ATDTEST0 is intended for factory test purposes only.

NOTE: *Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.*

3.3 Register Descriptions

This section describes in address order all the ATD_10B16C registers and their individual bits.

3.3.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence but will not start a new sequence.

$_00

BIT	7	6	5	4	3	2	1	0
R	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
RESET:	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 3-1 ATD Control Register 0 (ATDCTL0)

Read: anytime

Write: anytime

WRAP3, WRAP2, WRAP1, WRAP0 — Wrap Around Channel Select Bits

These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in **Table 3-2**.

Table 3-2 Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple channel conversions (MULT=1) wrap around to AN0/PAD0 after converting
0	0	0	0	reserved
0	0	0	1	AN1 / PAD1
0	0	1	0	AN2 / PAD2
0	0	1	1	AN3 / PAD3
0	1	0	0	AN4 / PAD4
0	1	0	1	AN5 / PAD5
0	1	1	0	AN6 / PAD6

Table 3-2 Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple channel conversions (MULT=1) wrap around to AN0/PAD0 after converting
0	1	1	1	AN7 / PAD7
1	0	0	0	AN8 / PAD8
1	0	0	1	AN9 / PAD9
1	0	1	0	AN10 / PAD10
1	0	1	1	AN11 / PAD11
1	1	0	0	AN12 / PAD12
1	1	0	1	AN13 / PAD13
1	1	1	0	AN14 / PAD14
1	1	1	1	AN15 / PAD15

3.3.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence but will not start a new sequence.

$_01

BIT	7	6	5	4	3	2	1	0
R	ETRIGSEL	0	0	0	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
W								
RESET:	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 3-2 ATD Control Register 1 (ATDCTL1)

Read: anytime

Write: anytime

ETRIGSEL—External Trigger Source Select

This bit selects the external trigger source to be either one of the AD channels or a specific port pin ETRIG. See device specification for availability and connectivity of ETRIG pin. If ETRIG pin option is not available, writing a 1 to ETRISEL only sets the bit but has not effect, that means still one of the AD channels (selected by ETRIGCH3-0) is the source for external trigger.

1 = External trigger source is ETRIG pin.

0 = External Trigger source is the AD channel selected by ETRIGCH3-0 (see **Table 3-3**).

ETRIGCH3, ETRIGCH2, ETRIGCH1, ETRIGCH0 — External Trigger Channel Select

If ETRIGSEL=0 then these bits select one of the AD channels as the source for external trigger. The coding is summarized **Table 3-3**.

Table 3-3 External Trigger Channel Select Coding

ETRIGSEL	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0	External trigger source is
0	0	0	0	0	AN0 / PAD0
0	0	0	0	1	AN1 / PAD1
0	0	0	1	0	AN2 / PAD2
0	0	0	1	1	AN3 / PAD3
0	0	1	0	0	AN4 / PAD4
0	0	1	0	1	AN5 / PAD5
0	0	1	1	0	AN6 / PAD6
0	0	1	1	1	AN7 / PAD7
0	1	0	0	0	AN8 / PAD8
0	1	0	0	1	AN9 / PAD9
0	1	0	1	0	AN10 / PAD10
0	1	0	1	1	AN11 / PAD11
0	1	1	0	0	AN12 / PAD12
0	1	1	0	1	AN13 / PAD13
0	1	1	1	0	AN14 / PAD14
0	1	1	1	1	AN15 / PAD15
1	X	X	X	X	ETRIG only if ETRIG pin option available (see device specification), else external trigger source is still on one of the AD channels selected by ETRIGCH3-0

3.3.3 ATD Control Register 2 (ATDCTL2)

This register controls power down, interrupt and external trigger. Writes to this register will abort current conversion sequence but will not start a new sequence.

$_02

BIT	7	6	5	4	3	2	1	0
R W	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 ATD Control Register 2 (ATDCTL2)

Read: anytime

Write: anytime

ADPU — ATD Power Down

This bit provides on/off control over the ATD_10B16C block allowing reduced MCU power consumption. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after ADPU bit is enabled.

1 = Normal ATD functionality
0 = Power down ATD

AFFC — ATD Fast Flag Clear All

1 = Changes all ATD conversion complete flags to a fast clear sequence. Any access to a result register will cause the associate CCF flag to clear automatically.
0 = ATD flag clearing operates normally (read the status register ATDSTAT1 before reading the result register to clear the associate CCF flag).

AWAI — ATD Power Down in Wait Mode

When entering Wait Mode this bit provides on/off control over the ATD_10B16C block allowing reduced MCU power. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after exit from Wait mode.

1 = Halt conversion and power down ATD during Wait mode
After exiting Wait mode with an interrupt conversion will resume. But due to the recovery time the result of this conversion should be ignored.
0 = ATD continues to run in Wait mode

ETRIGLE — External Trigger Level/Edge Control

This bit controls the sensitivity of the external trigger signal. See **Table 3-4** for details.

ETRIGP — External Trigger Polarity

This bit controls the polarity of the external trigger signal. See **Table 3-4** for details.

Table 3-4 External Trigger Configurations

ETRIGLE	ETRIGP	External Trigger Sensitivity
0	0	falling edge
0	1	rising edge
1	0	low level
1	1	high level

ETRIGE — External Trigger Mode Enable

This bit enables the external trigger on ETRIG pin or one of the ATD channels as described in **Table 3-3**. If external trigger source is one the ATD channels, the digital input buffer of this channel is enabled. The external trigger allows to synchronize sample and ATD conversions processes with external events.

1 = Enable external trigger
0 = Disable external trigger

NOTE: *If using one of the ATD channel as external trigger (ETRIGSEL=0) the conversion results for this channel have no meaning while external trigger mode is enabled.*

ASCIE — ATD Sequence Complete Interrupt Enable

1 = ATD Interrupt will be requested whenever ASCIF=1 is set.
0 = ATD Sequence Complete interrupt requests are disabled.

ASCIF — ATD Sequence Complete Interrupt Flag

If ASCIE=1 the ASCIF flag equals the SCF flag (see **3.3.7**), else ASCIF reads zero. Writes have no effect.

1 = ATD sequence complete interrupt pending
0 = No ATD interrupt occurred

3.3.4 ATD Control Register 3 (ATDCTL3)

This register controls the conversion sequence length, FIFO for results registers and behavior in Freeze Mode. Writes to this register will abort current conversion sequence but will not start a new sequence.

$_03

BIT	7	6	5	4	3	2	1	0
R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
W								
RESET:	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4 ATD Control Register 3 (ATDCTL3)

Read: anytime

Write: anytime

S8C, S4C, S2C, S1C — Conversion Sequence Length

These bits control the number of conversions per sequence. **Table 3-5** shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.

Table 3-5 Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5

Table 3-5 Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

FIFO — Result Register FIFO Mode

If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register, the second result in the second result register, and so on.

If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or ending of a conversion sequence; conversion results are placed in consecutive result registers between sequences. The result register counter wraps around when it reaches the end of the result register file. The conversion counter value in ATDSTAT0 can be used to determine where in the result register file, the current conversion result will be placed.

Finally, which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data.

1 = Conversion results are placed in consecutive result registers (wrap around at end).

0 = Conversion results are placed in the corresponding result register up to the selected sequence length.

FRZ1, FRZ0 — Background Debug Freeze Enable

When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in **Table 3-6**. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Table 3-6 ATD Behavior in Freeze Mode (breakpoint)

FRZ1	FRZ0	Behavior in Freeze mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

3.3.5 ATD Control Register 4 (ATDCTL4)

This register selects the conversion clock frequency, the length of the second phase of the sample time and the resolution of the A/D conversion (i.e.: 8-bits or 10-bits). Writes to this register will abort current conversion sequence but will not start a new sequence.

$_04

BIT	7	6	5	4	3	2	1	0
R W	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
RESET:	0	0	0	0	0	1	0	1

= Unimplemented or Reserved

Figure 3-5 ATD Control Register 4 (ATDCTL4)

Read: anytime

Write: anytime

SRES8 — A/D Resolution Select

This bit selects the resolution of A/D conversion results as either 8 or 10 bits. The A/D converter has an accuracy of 10 bits. However, if low resolution is required, the conversion can be speeded up by selecting 8-bit resolution.

1 = 8 bit resolution
0 = 10 bit resolution

SMP1, SMP0 — Sample Time Select

These two bits select the length of the second phase of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). The sample time consists of two phases. The first phase is two ATD conversion clock cycles long and transfers the sample quickly (via the buffer amplifier) onto the A/D machine's storage node. The second phase attaches the external analog signal directly to the storage node for final charging and high accuracy. **Table 3-7** lists the lengths available for the second sample phase.

Table 3-7 Sample Time Select

SMP1	SMP0	Length of 2nd phase of sample time
0	0	2 A/D conversion clock periods
0	1	4 A/D conversion clock periods
1	0	8 A/D conversion clock periods
1	1	16 A/D conversion clock periods

PRS4, PRS3, PRS2, PRS1, PRS0 — ATD Clock Prescaler

These 5 bits are the binary value prescaler value PRS. The ATD conversion clock frequency is calculated as follows:

$$\text{ATDclock} = \frac{[\text{BusClock}]}{[\text{PRS} + 1]} \times 0.5$$

Note that the maximum ATD conversion clock frequency is half the Bus Clock. The default (after reset) prescaler value is 5 which results in a default ATD conversion clock frequency that is Bus Clock divided by 12. **Table 3-8** illustrates the divide-by operation and the appropriate range of the Bus Clock.

Table 3-8 Clock Prescaler Values

Prescale Value	Total Divisor Value	Max. Bus Clock[1]	Min. Bus Clock[2]
00000	divide by 2	4 MHz	1 MHz
00001	divide by 4	8 MHz	2 MHz
00010	divide by 6	12 MHz	3 MHz
00011	divide by 8	16 MHz	4 MHz
00100	divide by 10	20 MHz	5 MHz
00101	divide by 12	24 MHz	6 MHz
00110	divide by 14	28 MHz	7 MHz
00111	divide by 16	32 MHz	8 MHz
01000	divide by 18	36 MHz	9 MHz
01001	divide by 20	40 MHz	10 MHz
01010	divide by 22	44 MHz	11 MHz
01011	divide by 24	48 MHz	12 MHz
01100	divide by 26	52 MHz	13 MHz
01101	divide by 28	56 MHz	14 MHz
01110	divide by 30	60 MHz	15 MHz
01111	divide by 32	64 MHz	16 MHz
10000	divide by 34	68 MHz	17 MHz
10001	divide by 36	72 MHz	18 MHz
10010	divide by 38	76 MHz	19 MHz
10011	divide by 40	80 MHz	20 MHz
10100	divide by 42	84 MHz	21 MHz
10101	divide by 44	88 MHz	22 MHz
10110	divide by 46	92 MHz	23 MHz
10111	divide by 48	96 MHz	24 MHz
11000	divide by 50	100 MHz	25 MHz
11001	divide by 52	104 MHz	26 MHz
11010	divide by 54	108 MHz	27 MHz
11011	divide by 56	112 MHz	28 MHz
11100	divide by 58	116 MHz	29 MHz
11101	divide by 60	120 MHz	30 MHz
11110	divide by 62	124 MHz	31 MHz
11111	divide by 64	128 MHz	32 MHz

NOTE:

1. Maximum ATD conversion clock frequency is 2MHz. The maximum allowed Bus Clock frequency is shown in this column.
2. Minimum ATD conversion clock frequency is 500KHz. The minimum allowed Bus Clock frequency is shown in this column.

3.3.6 ATD Control Register 5 (ATDCTL5)

This register selects the type of conversion sequence and the analog input channels sampled. Writes to this register will abort current conversion sequence and start a new conversion sequence.

$_05

BIT	7	6	5	4	3	2	1	0
R W	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 ATD Control Register 5 (ATDCTL5)

Read: anytime

Write: anytime

DJM — Result Register Data Justification

This bit controls justification of conversion data in the result registers. See **3.3.16 ATD Conversion Result Registers (ATDDRx)** for details.

1 = Right justified data in the result registers.
0 = Left justified data in the result registers.

DSGN — Result Register Data Signed or Unsigned Representation

This bit selects between signed and unsigned conversion data representation in the result registers. Signed data is represented as 2's complement. Signed data is not available in right justification. See **3.3.16 ATD Conversion Result Registers (ATDDRx)** for details.

1 = Signed data representation in the result registers.
0 = Unsigned data representation in the result registers.

Table 3-9 summarizes the result data formats available and how they are set up using the control bits.

Table 3-10 illustrates the difference between the signed and unsigned, left justified output codes for an input signal range between 0 and 5.12 Volts.

Table 3-9 Available Result Data Formats.

SRES8	DJM	DSGN	Result Data Formats Description and Bus Bit Mapping
1	0	0	8-bit / left justified / unsigned - bits 8-15
1	0	1	8-bit / left justified / signed - bits 8-15
1	1	X	8-bit / right justified / unsigned - bits 0-7
0	0	0	10-bit / left justified / unsigned - bits 6-15
0	0	1	10-bit / left justified / signed - bits 6-15
0	1	X	10-bit / right justified / unsigned - bits 0-9

Table 3-10 Left Justified, Signed and Unsigned ATD Output Codes.

Input Signal Vrl = 0 Volts Vrh = 5.12 Volts	Signed 8-Bit Codes	Unsigned 8-Bit Codes	Signed 10-Bit Codes	Unsigned 10-Bit Codes
5.120 Volts	7F	FF	7FC0	FFC0
5.100	7F	FF	7F00	FF00
5.080	7E	FE	7E00	FE00
2.580	01	81	0100	8100
2.560	00	80	0000	8000
2.540	FF	7F	FF00	7F00
0.020	81	01	8100	0100
0.000	80	00	8000	0000

SCAN — Continuous Conversion Sequence Mode

This bit selects whether conversion sequences are performed continuously or only once.

1 = Continuous conversion sequences (scan mode)
0 = Single conversion sequence

MULT — Multi-Channel Sample Mode

When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code or wrapping around to AN0 (channel 0.

1 = Sample across several channels
0 = Sample only one channel

CD, CC, CB, CA — Analog Input Channel Select Code

These bits select the analog input channel(s) whose signals are sampled and converted to digital codes. **Table 3-11** lists the coding used to select the various analog input channels.

In the case of single channel conversions (MULT=0), this selection code specified the channel to be examined.

In the case of multiple channel conversions (MULT=1), this selection code represents the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing the channel selection code or wrapping around to AN0 (after converting the channel defined by the Wrap Around Channel Select Bits WRAP3-0 in ATDCTL0). In case starting with a channel number higher than the one defined by WRAP3-0 the first wrap around will be AN15 to AN0.

Table 3-11 Analog Input Channel Select Coding

CD	CC	CB	CA	Analog Input Channel
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

3.3.7 ATD Status Register 0 (ATDSTAT0)

This read-only register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

$_06

BIT	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 ATD Status Register 0 (ATDSTAT0)

Read: anytime

Write:.anytime (No effect on (CC3, CC2, CC1, CC0))

SCF — Sequence Complete Flag

This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the following occurs:

A) Write “1” to SCF
B) Write to ATDCTL5 (a new conversion sequence is started)
C) If AFFC=1 and read of a result register
1 = Conversion sequence has completed
0 = Conversion sequence not completed

ETORF — External Trigger Overrun Flag

While in edge trigger mode (ETRIGLE=0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs:
A) Write “1” to ETORF
B) Write to ATDCTL0,1,2,3,4 (a conversion sequence is aborted)
C) Write to ATDCTL5 (a new conversion sequence is started)
1 = External trigger over run error has occurred
0 = No External trigger over run error has occurred

FIFOR - FIFO Over Run Flag.

This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been over written before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs:
A) Write “1” to FIFOR
B) Start a new conversion sequence (write to ATDCTL5 or external trigger)
1 = Overrun condition exists (result register has been written while associated CCFx flag was still set)
0 = No over run has occurred

CC3, CC2, CC1, CC0 — Conversion Counter

These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC3=0, CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the begin and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counters wraps around when its maximum value is reached.

3.3.8 Reserved Register (ATDTEST0)

$_08

BIT	7	6	5	4	3	2	1	0
R	U	U	U	U	U	U	U	U
W								
RESET:	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-8 Reserved Register (ATDTEST0)

Read: anytime, returns unpredictable values

Write: anytime in special modes, unimplemented in normal modes

NOTE: *Writing to this registers when in special modes can alter functionality.*

3.3.9 ATD Test Register 1 (ATDTEST1)

This register contains the SC bit used to enable special channel conversions.

$_09

	7	6	5	4	3	2	1	0
R	U	U	0	0	0	0	0	SC
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9 ATD Test Register 1 (ATDTEST1)

Read: anytime, returns unpredictable values for Bit7 and Bit6

Write: anytime

NOTE: *Writing to this registers when in special modes can alter functionality.*

SC - Special Channel Conversion Bit

If this bit is set, then special channel conversion can be selected using CC, CB and CA of ATDCTL5. **Table 3-12** lists the coding.

1 = Special channel conversions enabled
0 = Special channel conversions disabled

Table 3-12 Special Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
1	0	0	X	X	Reserved
1	0	1	0	0	V_{RH}
1	0	1	0	1	V_{RL}
1	0	1	1	0	$(V_{RH}+V_{RL}) / 2$
1	0	1	1	1	Reserved
1	1	X	X	X	Reserved

3.3.10 ATD Status Register 2 (ATDSTAT2)

This read-only register contains the Conversion Complete Flags CCF15 to CCF8.

$_0A

BIT	7	6	5	4	3	2	1	0
R	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 ATD Status Register 2 (ATDSTAT2)

Read: anytime

Write: anytime, no effect

CCFx — Conversion Complete Flag x (x= 15, 14, 13, 12, 11, 10, 9, 8)

A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore, CCF8 is set when the ninth conversion in a sequence is complete and the result is available in result register ATDDR8; CCF9 is set when the tenth conversion in a sequence is complete and the result is available in ATDDR9, and so forth. A flag CCFx (x= 15, 14, 13, 12, 11, 10, 9, 8) is cleared when one of the following occurs:

A) Write to ATDCTL5 (a new conversion sequence is started)
B) If AFFC=0 and read of ATDSTAT2 followed by read of result register ATDDRx
C) If AFFC=1 and read of result register ATDDRx
1 = Conversion number x has completed, result ready in ATDDRx
0 = Conversion number x not completed

3.3.11 ATD Status Register 1 (ATDSTAT1)

This read-only register contains the Conversion Complete Flags CCF7 to CCF0.

$_0B

BIT	7	6	5	4	3	2	1	0
R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 ATD Status Register 1 (ATDSTAT1)

Read: anytime

Write: anytime, no effect

CCFx — Conversion Complete Flag x (x= 7,6,5,4,3,2,1,0)

A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore, CCF0 is set when the first conversion in a sequence is complete and the result is available in result register ATDDR0; CCF1 is set when the second conversion in a sequence is complete and the result is available in ATDDR1, and so forth. A flag CCFx (x= 7,6,5,4,3,2,1,0) is cleared when one of the following occurs:

A) Write to ATDCTL5 (a new conversion sequence is started)
B) If AFFC=0 and read of ATDSTAT1 followed by read of result register ATDDRx
C) If AFFC=1 and read of result register ATDDRx
1 = Conversion number x has completed, result ready in ATDDRx
0 = Conversion number x not completed

3.3.12 ATD Input Enable Register 0 (ATDDIEN0)

$_0C

BIT	7	6	5	4	3	2	1	0
R W	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-12 Input Enable Register 0 (ATDDIEN0)

Read: anytime

Write: anytime

IENx — ATD Digital Input Enable on channel x (x= 15, 14, 13, 12, 11, 10, 9, 8)

This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register.
1 = Enable digital input buffer to PTADx.
0 = Disable digital input buffer to PTADx

NOTE: *Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.*

3.3.13 ATD Input Enable Register 1 (ATDDIEN1)

$_0D

BIT	7	6	5	4	3	2	1	0
R W	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-13 Input Enable Register 1 (ATDDIEN1)

Read: anytime

Write: anytime

IENx — ATD Digital Input Enable on channel x (x= 7, 6, 5, 4, 3, 2, 1, 0)

This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register.
1 = Enable digital input buffer to PTADx.
0 = Disable digital input buffer to PTADx

NOTE: *Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.*

3.3.14 Port Data Register 0 (PORTAD0)

The data port associated with the ATD is input-only. The port pins are shared with the analog A/D inputs AN15-8.

Read: anytime

Write: anytime, no effect

$_0E

BIT	7	6	5	4	3	2	1	0
R W	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
RESET:	1	1	1	1	1	1	1	1
Pin Func-tion	AN 15	AN14	AN13	AN12	AN11	AN10	AN9	AN8

= Unimplemented or Reserved

Figure 3-14 Port Data Register 0 (PORTAD0)

The A/D input channels may be used for general purpose digital input.

PTADx — A/D Channel x (ANx) Digital Input (x= 15, 14, 13, 12, 11, 10, 9, 8)

If the digital input buffer on the ANx pin is enabled (IENx=1) or channel x is enabled as external trigger (ETRIGE=1,ETRICH[3-0]=x,ETRIGSEL=0) read returns the logic level on ANx pin (signal potentials not meeting VIL or VIH specifications will have an indeterminate value)).

If the digital input buffers are disabled (IENx=0) and channel x is not enabled as external trigger, read returns a “1”.

Reset sets all PORTAD0 bits to “1”.

3.3.15 Port Data Register 1 (PORTAD1)

The data port associated with the ATD is input-only. The port pins are shared with the analog A/D inputs AN7-0.

Read: anytime

Write: anytime, no effect

$_0F

BIT	7	6	5	4	3	2	1	0
R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
W								
RESET:	1	1	1	1	1	1	1	1
Pin Func-tion	AN 7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

= Unimplemented or Reserved

Figure 3-15 Port Data Register 1 (PORTAD1)

The A/D input channels may be used for general purpose digital input.

PTADx — A/D Channel x (ANx) Digital Input (x= 7, 6, 5, 4, 3, 2, 1, 0)

If the digital input buffer on the ANx pin is enabled (IENx=1) or channel x is enabled as external trigger (ETRIGE=1,ETRICH[3-0]=x,ETRIGSEL=0) read returns the logic level on ANx pin (signal potentials not meeting VIL or VIH specifications will have an indeterminate value)).

If the digital input buffers are disabled (IENx=0) and channel x is not enabled as external trigger, read returns a “1”.

Reset sets all PORTAD1 bits to “1”.

3.3.16 ATD Conversion Result Registers (ATDDRx)

The A/D conversion results are stored in 16 read-only result registers. The result data is formatted in the result registers bases on two criteria. First there is left and right justification; this selection is made using the DJM control bit in ATDCTL5. Second there is signed and unsigned data; this selection is made using

the DSGN control bit in ATDCTL5. Signed data is stored in 2's complement format and only exists in left justified format. Signed data selected for right justified format is ignored.

Read: anytime

Write: anytime in special mode, unimplemented in normal modes

3.3.16.1 Left Justified Result Data

$_10 = ATDDR0H, $_12 = ATDDR1H, $_14 = ATDDR2H, $_16 = ATDDR3H
$_18 = ATDDR4H, $_1A = ATDDR5H, $_1C = ATDDR6H, $_1E = ATDDR7H
$_20 = ATDDR8H, $_22 = ATDDR9H, $_24 = ATDDR10H, $_26 = ATDDR11H
$_28 = ATDDR12H, $_2A = ATDDR13H, $_2C =ATDDR14H, $_2E =ATDDR15H

BIT	15	14	13	12	11	10	9	8	
R	BIT 9 MSB	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	10-bit data
W	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	8-bit data
RESET:	0	0	0	0	0	0	0	0	

= Unimplemented or Reserved

Figure 3-16 Left Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

$_11 = ATDDR0L, $_13 = ATDDR1L, $_15 = ATDDR2L, $_17 = ATDDR3L
$_19 = ATDDR4L, $_1B = ATDDR5L, $_1D = ATDDR6L, $_1F = ATDDR7L
$_21 = ATDDR8L, $_23 = ATDDR9L, $_25 = ATDDR10L, $_27 = ATDDR11L
$_29 = ATDDR12L, $_2B = ATDDR13L, $_2D =ATDDR14L, $_2F =ATDDR15L

BIT	15	14	13	12	11	10	9	8	
R	BIT 1	BIT 0	0	0	0	0	0	0	10-bit data
W	U	U	0	0	0	0	0	0	8-bit data
RESET:	0	0	0	0	0	0	0	0	

= Unimplemented or Reserved

Figure 3-17 Left Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

3.3.16.2 Right Justified Result Data

$_10 = ATDDR0H, $_12 = ATDDR1H, $_14 = ATDDR2H, $_16 = ATDDR3H
$_18 = ATDDR4H, $_1A = ATDDR5H, $_1C = ATDDR6H, $_1E = ATDDR7H
$_20 = ATDDR8H, $_22 = ATDDR9H, $_24 = ATDDR10H, $_26 = ATDDR11H
$_28 = ATDDR12H, $_2A = ATDDR13H, $_2C =ATDDR14H, $_2E =ATDDR15H

BIT	15	14	13	12	11	10	9	8	
R	0	0	0	0	0	0	BIT 9 MSB	BIT 8	10-bit data
W	0	0	0	0	0	0	0	0	8-bit data
RESET:	0	0	0	0	0	0	0	0	

= Unimplemented or Reserved

Figure 3-18 Right Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

$_11 = ATDDR0L, $_13 = ATDDR1L, $_15 = ATDDR2L, $_17 = ATDDR3L
$_19 = ATDDR4L, $_1B = ATDDR5L, $_1D = ATDDR6L, $_1F = ATDDR7L
$_21 = ATDDR8L, $_23 = ATDDR9L, $_25 = ATDDR10L, $_27 = ATDDR11L
$_29 = ATDDR12L, $_2B = ATDDR13L, $_2D =ATDDR14L, $_2F =ATDDR15L

BIT	15	14	13	12	11	10	9	8	
R	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	10-bit data
W	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	8-bit data
RESET:	0	0	0	0	0	0	0	0	

= Unimplemented or Reserved

Figure 3-19 Right Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

Section 4 Functional Description

4.1 General

The ATD_10B16C is structured in an analog and a digital sub-block.

4.2 Analog Sub-block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

4.2.1 Sample and Hold Machine

The Sample and Hold (S/H) Machine accepts analog signals from the external world and stores them as capacitor charge on a storage node.

The sample process uses a two stage approach. During the first stage, the sample amplifier is used to quickly charge the storage node.The second stage connects the input directly to the storage node to complete the sample for high accuracy.

When not sampling, the sample and hold machine disables its own clocks. The analog electronics still draw their quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

The input analog signals are unipolar and must fall within the potential range of VSSA to VDDA.

4.2.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

4.2.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

4.2.4 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine disables its own clocks. The analog electronics still draws quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output codes.

4.3 Digital Sub-block

This subsection explains some of the digital features in more detail. See register descriptions for all details.

4.3.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The external trigger signal (out of reset ATD channel 15, configurable in ATDCTL1) is programmable to be edge or level sensitive with polarity control. **Table 4-1** gives a brief description of the different combinations of control bits and their affect on the external trigger function.

Table 4-1 External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	X	Rising edge triggered. Performs one conversion sequence per trigger.
1	0	1	X	Trigger active low. Performs continuous conversions while trigger is active.
1	1	1	X	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received. In both cases, the maximum latency time is one Bus Clock cycle plus any skew or delay introduced by the trigger circuitry.

Once ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

4.3.2 General Purpose Digital Input Port Operation

The input channel pins can be multiplexed between analog and digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply external input data that can be accessed through the digital port registers (PORTAD0 & PORTAD1) (input-only).

The analog/digital multiplex operation is performed in the input pads. The input pad is always connected to the analog inputs of the ATD_10B16C. The input pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN0 & ATDDIEN1 register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

4.3.3 Low Power Modes

The ATD_10B16C can be configured for lower MCU power consumption in 3 different ways:

- Stop Mode: This halts A/D conversion. Exit from Stop mode will resume A/D conversion, But due to the recovery time the result of this conversion should be ignored.
- Wait Mode with AWAI=1: This halts A/D conversion. Exit from Wait mode will resume A/D conversion, but due to the recovery time the result of this conversion should be ignored.
- Writing ADPU=0 (Note that all ATD registers remain accessible.): This aborts any A/D conversion in progress.

Note that the reset value for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

Section 5 Resets

5.1 General

At reset the ATD_10B16C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see **Section 3 Memory Map and Register Definition**) which details the registers and their bit-field.

Section 6 Interrupts

6.1 General

The interrupt requested by the ATD_10B16C is listed in **Table 6-1**. Refer to MCU specification for related vector address and priority.

Table 6-1 ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2

See register descriptions for further details.

Section 7 Initialization/Application Information

7.1 Setting up and starting an A/D conversion

The following describes a typical setup procedure for starting A/D conversions. It is highly recommended to follow this procedure to avoid common mistakes.

Each step of the procedure will have a general remark and a typical example

7.1.1 Step 1

Power up the ATD and concurrently define other settings in ATDCTL2

Example: Write to ATDCTL2: ADPU=1 -> powers up the ATD, ASCIE=1 enable interrupt on finish of a conversion sequence.

7.1.2 Step 2

Wait for the ATD Recovery Time t_{REC} before you proceed with Step 3.

Example: Use the CPU in a branch loop to wait for a defined number of bus clocks.

7.1.3 Step 3

Configure how many conversions you want to perform in one sequence and define other settings in ATDCTL3.

Example: Write S4C=1 to do 4 conversions per sequence.

7.1.4 Step 4

Configure resolution, sampling time and ATD clock speed in ATDCTL4.

Example: Use default for resolution and sampling time by leaving SRES8, SMP1 and SMP0 clear. For a bus clock of 40MHz write 9 to PRS4-0, this gives an ATD clock of 0.5*40MHz/(9+1) = 2MHz which is within the allowed range for fATDCLK.

7.1.5 Step 5

Configure starting channel, single/multiple channel, continuous or single sequence and result data format in ATDCTL5. Writing ATDCTL5 will start the conversion, so make sure your write ATDCTL5 in the last step.

Example: Leave CD, CC,CB,CA clear to start on channel AN0. Write MULT=1 to convert channel AN0 to AN3 in a sequence (4 conversion per sequence selected in ATDCTL3).

7.2 Aborting an A/D conversion

7.2.1 Step 1

Write to ATDCTL4. This will abort any ongoing conversion sequence.

(Do not use write to other ATDCTL registers to abort, as this under certain circumstances might not work correctly.)

7.2.2 Step 2

Disable the ATD Interrupt by writing ASCIE=0 in ATDCTL2.

It is important to clear the interrupt enable at this point, prior to step 3, as depending on the device clock gating it may not always be possible to clear it or the SCF flag once the module is disabled (ADPU=0).

7.2.3 Step 3

Clear the SCF flag by writing a 1 in ATDSTAT0.

(Remaining flags will be cleared with the next start of a conversions, but SCF flag should be cleared to avoid SCF interrupt.)

7.2.4 Step 4

Power down ATD by writing ADPU=0 in ATDCTL2.

User Guide End Sheet

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