A30

Secure Authenticator

Rev. 3.1 — 1 July 2026 **Product data sheet**

1 General description

A30 is a secure authentication IC for IoT platforms, electronic accessories, and consumable devices such as home electronic devices, mobile accessories, and medical supplies.

A30 contains ECC key pairs, which can be generated by the IC itself to make sure that private keys are never exposed outside the IC. Also it performs cryptographic operations for security critical communication and control functions.

A30 offers Common Criteria EAL 6+ security certification with AVA_VAN.5 on product level ref.[1] and supports a generic Crypto API providing AES, ECDSA, ECDH, SHA, HMAC, and HKDF cryptographic functionality for users. Asymmetric cryptography features support 256-bit ECC over the NIST P-256 and brainpoolP256r1 curves. Symmetric cryptography features support both AES-128 and AES-256. It also supports PKI-based mutual authentication including certificate handling. The CC security certification ensures that the IC security measures and protection mechanisms have been evaluated against sophisticated noninvasive and invasive attack scenarios.

A30 supports an I^2C contact interface with two GPIOs.

A30 supports a low-power design, and consumes only 5 µA at Halt mode when an external VDD is supplied.

Note: *For the functional description and command set, refer to UM12553.*

2 Features and use cases

2.1 Use cases

A30 can be used for:

- Secure key(s) and certificate(s) storage
- PKI (Public Key Infrastructure) based authentication and communication
- Device only, device-to-device, and device-to-cloud authentication
- Secure connection for consumer devices, industrial machines, and medical devices
- Battery passport and/or Digital product passport
- Device to meet increasing cybersecurity requirements

2.2 Key features

A30 is designed to support many IoT applications and solves the problems in IoT applications' full life cycle.

- ECC key generation on the IC, and provisioning item level certificate(s) in NXP, or in the field.
- The following cryptographic primitives are supported: AES-128/256 (ECB, CBC, CMAC, CCM, GCM), ECDSA, and ECDH over NIST P-256 and brainpoolP256r1, SHA-256/384, HMAC, and HKDF.
  This allows to support advanced cryptographic protocols such as SIGMA-I, TLS1.3 and Matter.
- Nonreversible monotonic counter as the usage counter
- Delivery of the list of UID and certificates at shipping from NXP
- I^2C target operates at 100 kHz (standard mode), 400 kHz (fast mode), or 1 MHz (Fast-mode Plus)
- Two configurable GPIOs; 1 GPIO can be used for power downstream - up to 10 mW for batteryless applications
- 1 V operation with 1.5 V battery
- Small footprint on PCB with WLCSP16

2.3 Configuration

A30 can be used as an I^2C target with Host MCU.

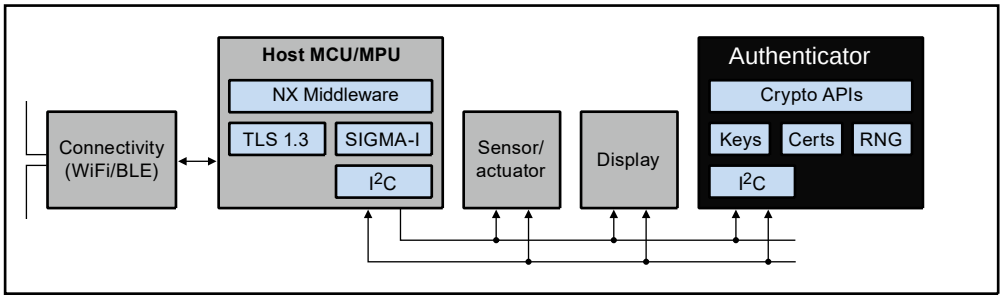

Figure 1. A30 solution block diagram

There are many configuration options for different types of applications.

2.4 Configuration as authenticator

A30 can be used for consumable authentication. An MCU can read the certificate from A30 and perform ECC-based authentication via ECDH, ECDSA, or full SIGMA-I protocol (see Section "SIGMA-I authentication with ISOGeneralAuthenticate" in UM12553).

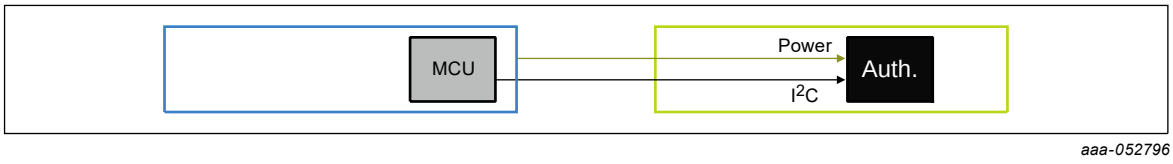

Figure 2. A30 for the consumable authentication

The user can check the originality of the consumable part and get its status, for example, how many times the device has been powered up or used with a nonreversible monotonic counter.

With this configuration, the target application is as an accessory for mobiles or electronic devices (for example, USB-C cable, Wireless charger, etc.)

2.5 Configuration to secure IoT applications

A30 can be used for many other IoT applications.

With many other wired/wireless standards - WiFi, Bluetooth, ZigBee, Thread, A30 can be used to store keys and certificates securely, provide one-way and/or mutual authentication, and transferred sign data.

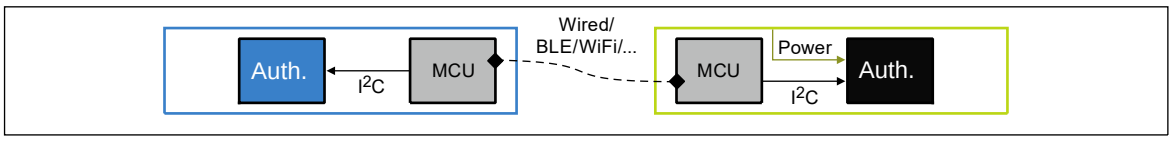

Figure 3. A30 solution block diagram

In this configuration, the target applications are IoT platforms supporting cloud onboarding and secure communications, for example, with Matter.

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
A30LDJUK	WLCSP	A30, 16 KB memory	SOT2127-2
A30LDJHN2	HVQFN	A30, 16 KB memory	SOT917-6(DD)

4 Block diagram

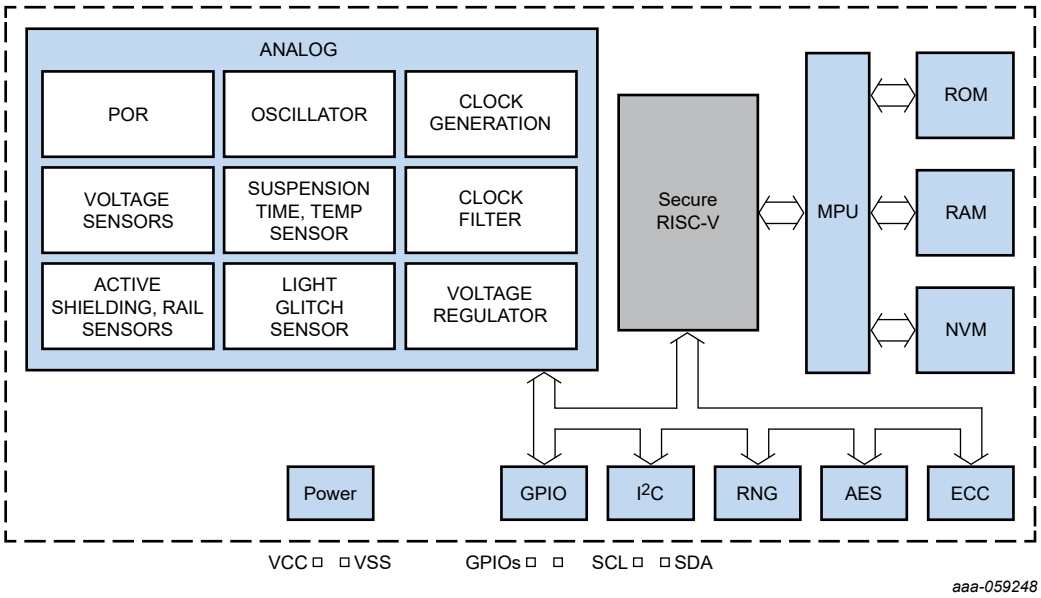

Figure 4. Block diagram

5 Pin description

A30 provides 6 pins:

Table 2. A30 pin configuration

Symbol	Description
V_{CC}	Logic and I^2C/GPIO power supply voltage input
V_{SS}	Ground
GPIO1	General Purpose IO
GPIO2	General Purpose IO
SDA	I^2C target data I/O
SCL	I^2C target clock input
RFU	To connected to Ground

Please refer the available pin outs in the section Section 9.

6 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		-0.3	-	+2	V
V_I	input voltage	Any supply pad	-0.3	-	+2	V
I_I	input current	pads SDA, SCL	-	-	10	mA
I_O	output current	pads SDA, SCL	-	-	10	mA
I_{LU}	latch-up current	$V_I < 0$ V or $V_I > V_{CC}$	-	-	100	mA
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1] pads V_{CC}, V_{SS}, SDA, SCL, GPIO1, GPIO2	-	-	+/- 2	kV
V_{ESD}	electrostatic discharge voltage	charged device model (CDM)[2] pads V_{CC}, V_{SS}, SDA, SCL, GPIO1, GPIO2	-	-	+/- 500	V
P_{tot}	total power dissipation	[3]	-	-	40	mW
T_{stg}	storage temperature		-65	-	150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002
[3] Depending on the appropriate thermal resistance of the package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

7 Recommended operating conditions

A30 is characterized by its specified operating supply voltage range of 1 V to 2 V.

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	norminal Supply voltage	1	-	2	V
V_I	DC input voltage on digital inputs and digital I/O pads	[1]	1 V + 10 %	-	V_{CC} + 0.3 V	V
H	field strength	contactless interface operation	1.5	-	7.5	A/m
T_{amb}	operating ambient temperature	[2]	-40	-	105	°C

[1] The supply voltage operating range of 1 V to 2 V requires internal supply elevation for the supply voltage range of 1 V to 1.62 V.
The supply voltage mode is automatically selected during boot-up based on internal supply voltage measurement.
To avoid continues activation and deactivation of the internal supply voltage elevation the external supply voltage of 1.55 V to 1.62 V should be avoided as performance degradation or resets might occur in this supply voltage range due to internal supply voltage switching. Performance degradation or chip resets might lead to timeouts during I^2C communication. Therefore it is recommended that the host would continue to retry the read for a preset number of times in case of timeouts and after that it will go to recovery mode trying with interface/chip reset and even if there is no response, returns with an error for the application to reopen the session.
The V_{CC} supply voltage rise time impacts the power consumption. V_{CC} supply voltage ramp times <600 µs to 1.8 V lead to higher power consumption as the device boots in voltage elevation mode. For V_{CC} supply voltages >1.62 V the supply voltage ramp shall therefore >600 µs.
The reference design recommendations of 100 nF cpacitor close to VCC/VSS pin must be followed. The minimum V_{CC} rise time (0 % - 100 %) is larger than 25 µs.

[2] All product properties and values specified within this data sheet are only valid within the operating ambient temperature range.

8 Characteristics

8.1 DC characteristics

Measurement conventions

Testing measurements are performed at the contact pads of the device under test. All voltages are defined with respect to the ground contact pad VSS. All currents flowing into the device are considered positive.

8.1.1 General-purpose I/O interface

Table 5. Electrical DC characteristics of GPIO1/2

V_{CC} = 1 V to 2 V (V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified
External pullup resistor 20 kΩ to V_{CC} assumed. The worst case test condition for parameter V_{OH} is present at minimum V_{CC}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage		0.7 x V_{CC}	-	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3	-	0.25 x V_{CC}	V
I_{IH}	HIGH level input current in "weak pullup" input mode	0.7 V_{CC} ≤ V_I ≤ V_{CC} Test conditions for the maximum absolute value: I_{IH}(max): V_I = 0.7 V_{CC}, V_{CC} = $V_{CC(max)}$	-	-1	-20	µA
I_{IL}	LOW level input current	0 V ≤ V_I ≤ 0.3 V_{CC}; Test conditions for the maximum absolute value: $I_{IL(max)}$: V_I = 0 V, V_{CC} = $V_{CC(max)}$	-	-1	-50	µA
I_I	Input current in "weak pullup" input mode	0 V ≤ V_I ≤ V_{CC}; Test conditions for the maximum absolute value: II(max):V_I = 0 V, V_{CC} = $V_{CC(max)}$	0	-	-50	µA
I_{ILIH}	Leakage input current at input voltage beyond V_{CC} in "weak pullup" input mode	V_{CC} < V_I ≤ V_{CC} + 0.3 V; -40 °C ≤ T_{amb} ≤ 105 °C; Test conditions: V_I = V_{CC} + 0.3 V; V_{CC} = $V_{CC(max)}$; T_{amb} = 105 °C	-	-	20	µA
I_{ILIL}	Leakage input current at input voltage below V_{SS} in "weak pullup" input mode	-0.3 V ≤ V_I < 0 V; -40 °C ≤ T_{amb} ≤ 30 °C Test conditions: V_I = -0.3 V; V_{CC}= $V_{CC(max)}$; T_{amb} = 30 °C	-	-	-50	µA
V_{OH}	HIGH level output voltage	I_{OH} = -20 µA	0.7 x V_{CC}	-	-	V
V_{OL}	LOW level output voltage	I_{OL} = 1 mA I_{OL} = 0.5 mA	-	-	0.3 0.7 x V_{CC}	V

Conditions:

V_{CC} = 1 V to 2 V (V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified

External pullup resistor 20 kΩ to V_{CC} assumed. The worst case test condition for parameter V_{OH} is present at minimum V_{CC}.

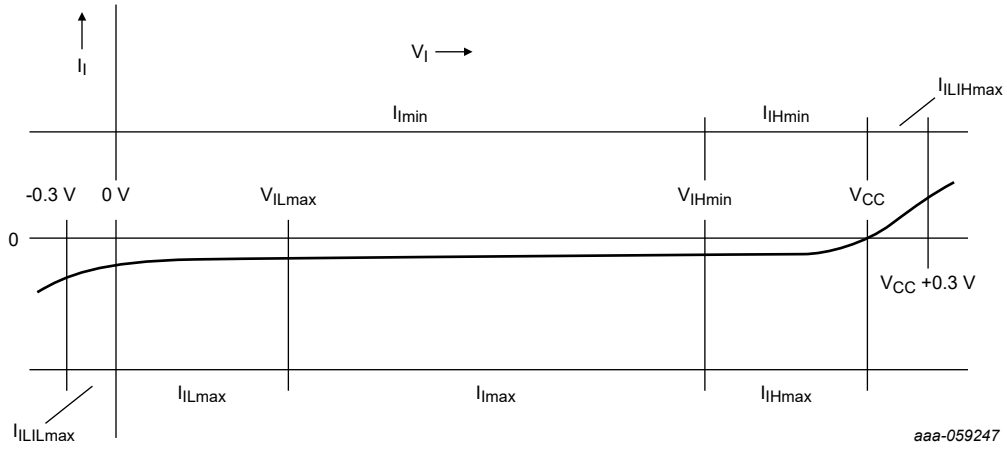

Figure 5. Input characteristics of GPIO1/2

8.1.2 I²C interface

Table 6. Electrical DC characteristics of I²C

V_{CC} = 1 V to 2 V (V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified
Pads SCL, SDA are in open-drain mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage		0.7 x V_{CC}	-	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3	-	0.25 x V_{CC}	V
V_{HYS}	input hysteresis voltage		0.081	-	-	V
$V_{OL(OD)}$	Low-level output voltage(open-drain mode)	I_{OL} = 3 mA	0	-	0.4	V
$I_{OL(OD)}$	Low-level output current(open-drain mode)	V_{CC} ≥1.1 V	0.6	-	-	mA
I_{WPU}	weak pullup current	V_{CC} ≥ 1.1 V	-	-180	-	µA
I_{ILIH}	leakage input current high level	V_{SDA} = 3.6 V, V_{SCL} = 3.6 V	-	0.27	15	µA

8.1.3 Power Consumption

Table 7. Electrical characteristics of IC supply voltage V_{CC}

V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage range		1	-	2	V
I_{DD}	supply current high-performance mode, CPU halted and AES or ECC cryptographic in operation		-	-	15	mA
	supply current Halt mode		-	-	5	µA
	supply current Off state		-	-	0.25	µA

8.2 AC characteristics

Table 8. Authentication application timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{DIT}	Initialization time from V_{CC} applied or wake from HALT mode		-	-	1	ms
t_{AUTH1}	Authentication time, with contact, SIGMA-I protocol		-	-	500	ms

Table 9. Nonvolatile memory timing characteristics

V_{CC} = 1 V to 2 V; V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{EEP}	FLASH erase + program time[1]		-	-	2.3	ms
t_{EEE}	FLASH program time		-	-	0.9	ms
t_{EEW}	FLASH erase time		-	-	1.4	ms

[1] The given value specifies physical access times of FLASH memory only.

Table 10. Nonvolatile memory data retention and endurance

V_{CC} = 1 V to 2 V; V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{EER}	FLASH data retention time <20 x 10^3 erase/program cycles to the whole memory block	T_{amb} = 55 °C	50	-	-	years
	FLASH data retention time <20 x 10^6 erase/program cycles to the whole memory block	T_{amb} = 55 °C	25	-	-	years
N_{EEC}	FLASH endurance (maximum number of programming cycles applied to the whole memory block performed by NXP static and dynamic wear leveling algorithm)		20 x 10^6	100 x 10^6	-	cycles

[1] Typical values are only referenced for information. They are subject to change without notice.

Table 11. Electrical AC characteristics of SDA, SCL

V_{CC} = 1 V to 2 V; V_{SS} = 0 V; T_{amb} = -40 °C to 105 °C, unless otherwise specified [1]
SCL, SDA pads in open-drain mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tr_{IO}[2][3]	I/O Input rise time	Input/reception mode	-	-	1	µs
tf_{IO}[2][4]	I/O Input fall time	Input/reception mode	-	-	1	µs
tf_{OIO}	I/O Output fall time	Output/transmission mode; C_L= 30 pF	-	-	0.3	µs
f_{CLK}	External clock frequency in I^2C applications	t_{CLKW}, T_{amb} and V_{CC} within specified limits	-	-	1	MHz
C_{PIN}	Pin capacitances SDA, SCL	Test f = 1 MHz; T_{amb} = 25 °C	-	-	10.5	pF
P_{OUT}	maximum output power in power harvesting mode at GPIO1		-	-	10	mW

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.
[2] maximum recommended load 5pF
[3] t_r is defined as rise time between 30 % and 70 % of the signal amplitude.
[4] t_f is defined as fall time between 70 % and 30 % of the signal amplitude.

8.3 I^2C Bus Timings

The A30 I^2C bus timing parameters are in accordance to the NXP I^2C bus specification, see Section 11.

8.4 EMC/EMI

EMC and EMI resistance according to IEC 61967-4, see Section 11.

9 Package information

A30 is either offered as Wafer Level Chip-Scale Package (WLCSP), or HVQFN.

9.1 WLCSP 16

A30 is provided in a four by four ball grid Wafer Level Chip-Scale Package (WLCSP):

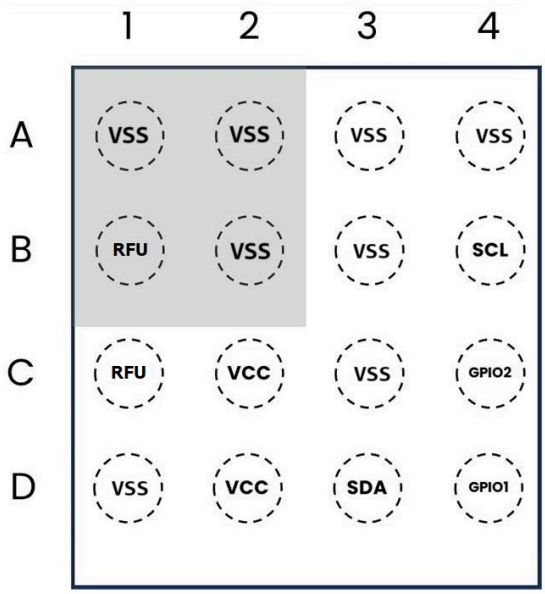

Figure 6. Package outline WLCSP (Top view)

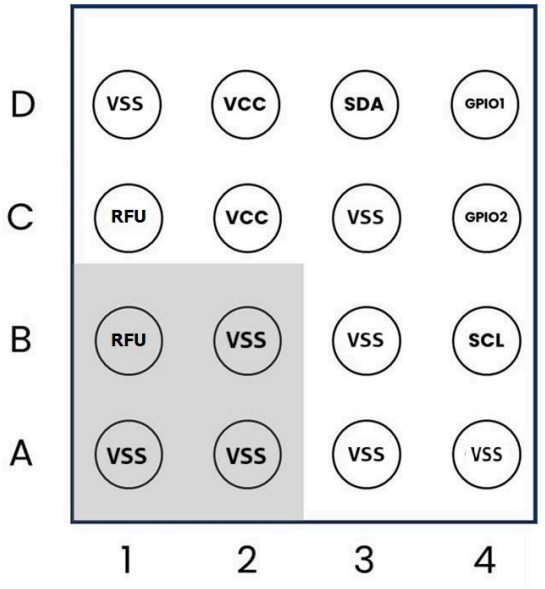

Figure 7. Package outline WLCSP (Bottom view)

WLCSP thickness is <= 0.5 mm with a ball pitch is 0.35 mm. A detailed description including pins can be found in "Delivery Specification ref.[2]"

9.2 HVQFN 20

A30 is provided in HVQFN:

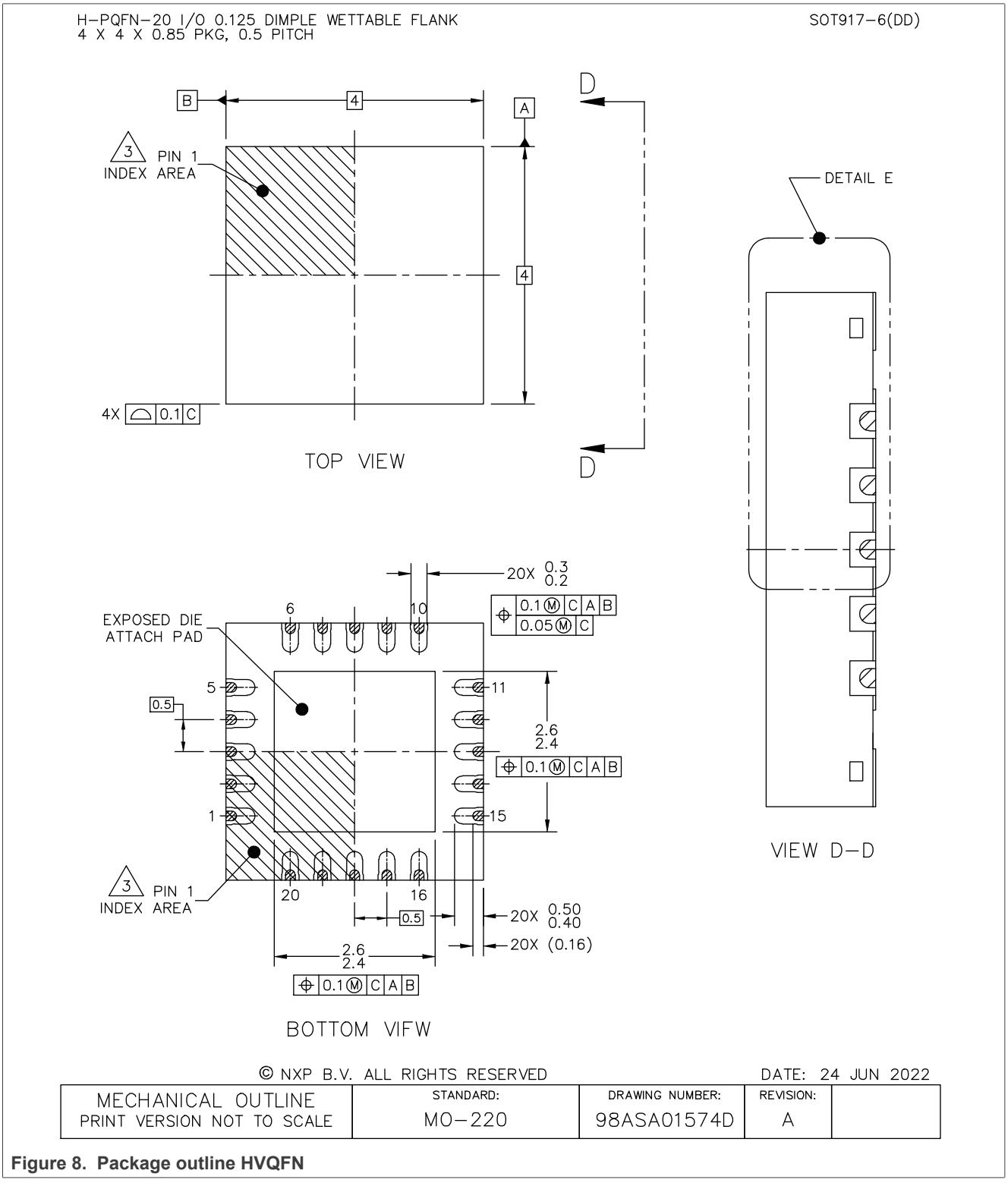

Figure 8. Package outline HVQFN

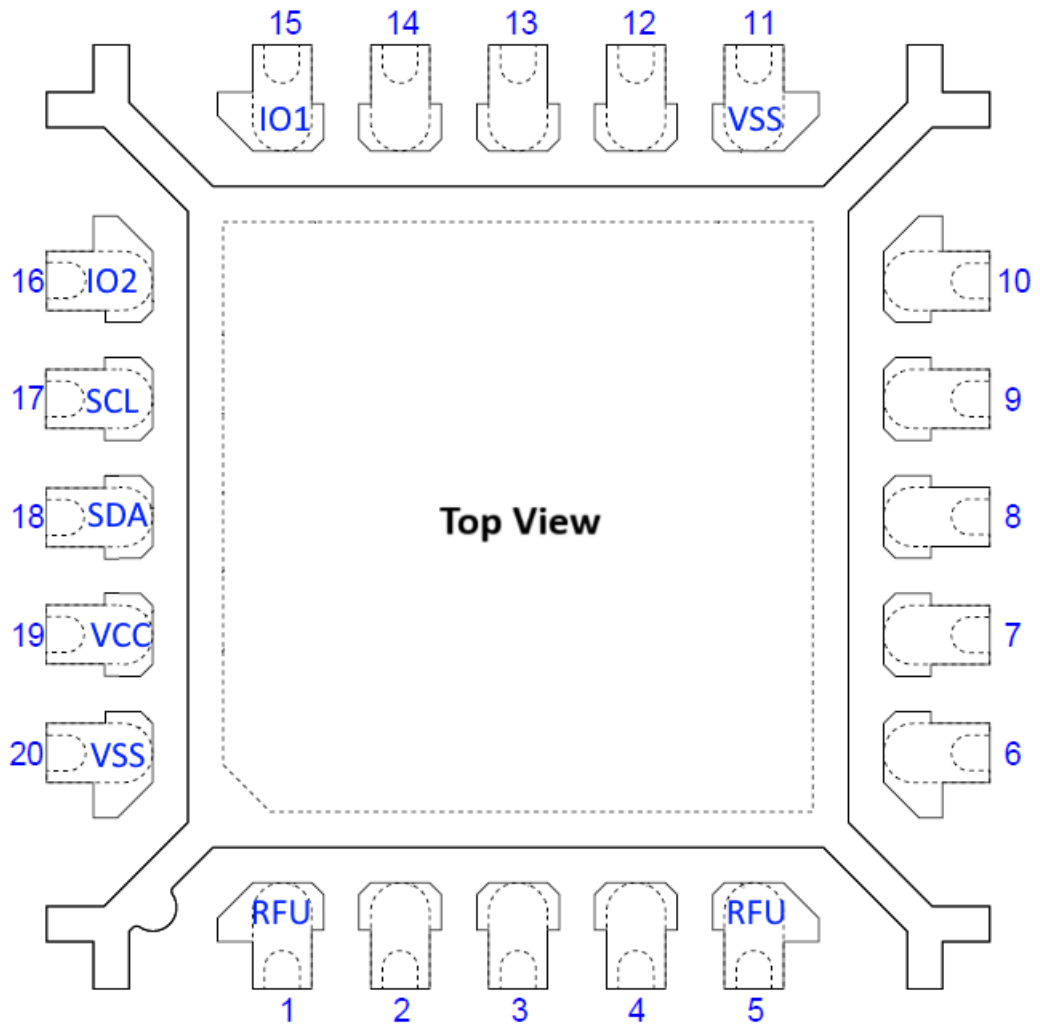

Figure 9. Pin description HVQFN

HVQFN thickness is 0.85 mm with a pitch is 0.5 mm. A detailed description can be found in "Delivery Specification ref.[2]"

10 Abbreviations

Table 12. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
APDU	Application Protocol Data unit
AppKey	Application Key
AppMasterKey	Application Master Key
API	Application Programming Interface
ASCII	American Standard Code for Information Interchange
ATQA	Answer to Request A
ATS	Answer to Select
CA	Certificate Authority
C-APDU	Command APDU
CBC	Cipher Block Chaining
CC	Capability Container
CCM	Counter with Cipher Block Chaining Message Authentication Code (CBC-MAC)
CID	Channel Identifier
CLA	Class
CMAC	Cipher-based Message Authentication Code
CmdCtr	Command Counter
CRC	Cyclic Redundancy Check
DF	Dedicated File (Application)
EAL	Evaluation Assurance Level
ECB	Electronic Code Book mode
ECC	Error Correcting Code
ECDH	Elliptic-curve Diffie Hellman
EF	Elementary File (File)
FCI	File Control Information
FSC	Frame Size for proximity Card (according to ISO/IEC 14443-4)
GPIO	General-Purpose Input/Output
HWDT	Halt WatchDog Timer
INS	INStruction byte (according to ISO/IEC 7816-4)
IV	Initialization Vector
KDF	Key Derivation Function
LSB	Least Significant Byte
MAC	Message Authentication Code
MCU	Microcontroller Unit

Table 12. Abbreviations...*continued*

Acronym	Description
MF	Master File
MSB	Most Significant Byte
NDEF	NFC Data Exchange Format
NFC	Near-Field Communication
NVM	Non-Volatile Memory
OID	Object IDentifier
PCB	Printed-Circuit Board
PCD	Proximity Coupling Device (Contactless Reader)
PCDCap	Proximity Coupling Device Capabilities
PD	Proximity Device, used as synonym for the PICC
PDCap	Proximity Device Capabilities
PICC	Proximity IC Card
PICCData	PICC data targeted for mirroring (e.g. UID, SDMReadCtr)
PKI	Public Key Infrastructure
POR	power-on-reset
PPS	Protocol Parameter Select
PRF	Pseudo-Random Function
PST	Power-Saving Time-out
RATS	Request for Answer To Select
RC	Return Code
RFU	Reserved for Future Use
RNG	Random Number Generator
SAK	Select Acknowledge
SDA	Serial Data
SDM	Secure Dynamic Messaging
SDMCtrRet	SDM Counter Retrieval, access right for GetFileCounters
SDMENCFileData	Refers to the encrypted part of data in the NDEF file
SDMFileRead	SDM File Reading, key/access setting for Secure Dynamic Messaging
SDMFileReadKey	Refers to the AppKey which is used for SDM MAC calculation
SDMMAC	Refers to the MAC calculated over response
SDMMetaRead	SDM Meta Reading, specifies PICCData encryption key or plain mirroring
SDMMetaReadKey	Refers to the AppKey which is used for SDM encryption of PICCData
SDMReadCtr	SDM Read Counter, counting number of interactions with a PICC
SesAuthENCKey	Session key for encryption
SesAuthMACKey	Session key for MACing
SP	Special Publication

Table 12. Abbreviations...*continued*

Acronym	Description
SPI	Serial Peripheral Interface
SUN	Secure Unique NFC
SV	Session Vector, input for session key calculation
SW	Status Word
TI	Transaction Identifier
TT	Tag Tamper
TTCurrStatus	Current status of the Tag Tamper loop
TTPermStatus	Permanently stores an Open status on the Tag Tamper loop
UID	Unique IDentifier
URI	Uniform Resource Identifier
WLCSP	Wafer Level Chip Sale Package

11 References

[1] User Manual - UM12053 - NRV11 Information on Guidance and Operation, Doc. No. UM9763**[1]
[2] Data sheet addendum - A30 - Delivery specification, Document number AD9772**
[3] User manual - UM12553 - A30 user manual (link)

1 ** … document version number

12 Note about the source code in the document

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13 Revision history

Table 13. Revision history

Document ID	Release date	Description
A30 v.3.1	1 July 2026	Editorial changes (typos, etc.) • Section 8.2 "AC characteristics": updated • Section 9.2 "HVQFN 20": Figure 9 "Pin description HVQFN " added • Section 11 "References": updated • Sections "Functional description" and "Command set" moved to UM12553
A30 v.3.0 [1]	27 January 2025	Initial version for the public release

[1] Previous versions are not published

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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