# A5G38H055N

## Airfast RF Power GaN Transistor

Rev. 1 — March 2023

Data Sheet: Technical Data

This 7.6 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 3700 to 3980 MHz.

This part is characterized and performance is guaranteed for applications operating in the 3700 to 3980 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

**3700–3980 MHz**

- Typical Doherty Single−Carrier W−CDMA Reference Circuit Performance: $V_{DD}$ = 48 Vdc, $I_{DQA}$ = 45 mA, $V_{GSB}$ = –3.9 Vdc, $P_{out}$ = 7.6 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

| Frequency | $G_{ps}$ (dB) | $\eta_D$ (%) | Output PAR (dB) | ACPR (dBc) |
|---|---|---|---|---|
| 3700 MHz | 14.7 | 55.5 | 8.5 | –29.5 |
| 3840 MHz | 14.9 | 53.2 | 8.5 | –35.0 |
| 3980 MHz | 14.7 | 53.0 | 8.2 | –33.4 |

1. All data measured in reference circuit with device soldered to printed circuit board.

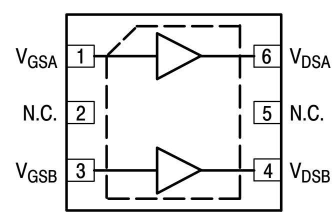
### Features

- High terminal impedances for optimal broadband performance
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for low complexity linearization systems
- Optimized for massive MIMO active antenna systems for 5G base stations

**A5G38H055N**

**3700–3980 MHz, 7.6 W Avg., 48 V AIRFAST RF POWER GaN TRANSISTOR**

**DFN 7 × 6.5 PLASTIC**




(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

**Figure 1. Pin Connections**

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 125 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | –16, 0 | Vdc |
| Operating Voltage | $V_{DD}$ | 55 | Vdc |
| Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ $T_C$ = 25°C | $I_{GMAX}$ | 9.0 | mA |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Case Operating Temperature Range | $T_C$ | –55 to +150 | °C |
| Maximum Channel Temperature | $T_{CH}$ | 225 | °C |

**Table 2. Recommended Operating Conditions**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Operating Voltage | $V_{DD}$ | 48 | Vdc |

**Table 3. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance by Infrared Measurement, Active Die Surface–to–Case<br>Case Temperature 117°C, $P_D$ = 9.3 W | $R_{\theta JC}$ (IR) | 2.6 (1) | °C/W |
| Thermal Resistance by Finite Element Analysis, Channel–to–Case<br>Case Temperature 117°C, $P_D$ = 9.3 W | $R_{\theta CHC}$ (FEA) | 7.6 (2) | °C/W |

**Table 4. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JS–001–2017) | 1A |
| Charge Device Model (per JS–002–2014) | C3 |

**Table 5. Moisture Sensitivity Level**

| Test Methodology | Rating | Package Peak Temperature | Unit |
|---|---|---|---|
| Per JESD22–A113, IPC/JEDEC J–STD–020 | 3 | 260 | °C |

**Table 6. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Off Characteristics (3)** | | | | | |
| Off–State Drain Leakage<br>($V_{DS}$ = 150 Vdc, $V_{GS}$ = –8 Vdc) Carrier<br>($V_{DS}$ = 150 Vdc, $V_{GS}$ = –8 Vdc) Peaking | $I_{D(BR)}$ | —<br>— | —<br>— | 1.6<br>3.1 | mAdc |
| Off–State Gate Leakage<br>($V_{DS}$ = 48 Vdc, $V_{GS}$ = –8 Vdc) Carrier<br>($V_{DS}$ = 48 Vdc, $V_{GS}$ = –8 Vdc) Peaking | $I_{GLK}$ | –0.4<br>–0.6 | —<br>— | —<br>— | mAdc |
| **On Characteristics — Side A, Carrier** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = 10 Vdc, $I_D$ = 2.9 mAdc) | $V_{GS(th)}$ | –4.6 | –2.0 | –1.5 | Vdc |
| Gate Quiescent Voltage<br>($V_{DD}$ = 48 Vdc, $I_{DA}$ = 35 mAdc, Measured in Functional Test) | $V_{GSA(Q)}$ | –2.9 | –2.4 | –1.9 | Vdc |
| Gate–Source Leakage Current<br>($V_{DS}$ = 150 Vdc, $V_{GS}$ = –8 Vdc) | $I_{GSS}$ | –0.6 | — | — | mAdc |
| **On Characteristics — Side B, Peaking** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = 10 Vdc, $I_D$ = 6.2 mAdc) | $V_{GS(th)}$ | –4.6 | –2.6 | –1.9 | Vdc |
| Gate–Source Leakage Current<br>($V_{DS}$ = 150 Vdc, $V_{GS}$ = –8 Vdc) | $I_{GSS}$ | –1.1 | — | — | mAdc |

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the channel temperature in degrees Celsius, *A* = –11.6 and *B* = 9129.
3. Each side of device measured separately.

(continued)

**Table 6. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted) **(continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Functional Tests** [(1)] (In NXP Doherty Production Test Fixture, 50 ohm system) $V_{DD}$ = 48 Vdc, $I_{DQA}$ = 35 mA, $V_{GSB}$ = ($V_t$ – 1.2) Vdc, $P_{out}$ = 8.1 W Avg., f = 3980 MHz, 1–tone CW. | | | | | |
| Power Gain | $G_{ps}$ | 13.0 | 15.0 | 18.0 | dB |
| Drain Efficiency | $\eta_D$ | 41.0 | 45.0 | — | % |
| $P_{out}$ @ 6 dB Compression Point | P6dB | 45.3 | 46.2 | — | dBm |
| **Wideband Ruggedness** [(2)] (In NXP Doherty Reference Circuit, 50 ohm system) $I_{DQA}$ = 45 mA, $V_{GSB}$ = –3.9 Vdc, f = 3840 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR | | | | | |
| ISBW of 400 MHz at 55 Vdc, 13.8 W Avg. Modulated Output Power (3 dB Input Overdrive from 7.6 W Avg. Modulated Output Power) | No Device Degradation | | | | |
| **Typical Performance** [(2)] (In NXP Doherty Reference Circuit, 50 ohm system) $V_{DD}$ = 48 Vdc, $I_{DQA}$ = 45 mA, $V_{GSB}$ = –3.9 Vdc, 3700–3980 MHz Bandwidth | | | | | |
| **Fast CW, 27 ms Sweep** | | | | | |
| $P_{out}$ @ 6 dB Compression Point | P6dB | — | 55 | — | W |
| AM/PM (Maximum value measured at the P6dB compression point across the 3700–3980 MHz bandwidth) | $\Phi$ | — | –9 | — | ° |
| Gain Variation over Temperature (–40°C to +85°C) | $\Delta G$ | — | 0.036 | — | dB/°C |
| Output Power Variation over Temperature (–40°C to +85°C) | ΔP6dB | — | 0.002 | — | dB/°C |
| **Single–Carrier W–CDMA, Unclipped** | | | | | |
| Gain Flatness in 280 MHz Bandwidth @ $P_{out}$ = 7.6 W Avg. | $G_F$ | — | 0.2 | — | dB |
| **2–Tone CW** | | | | | |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | $VBW_{res}$ | — | 300 | — | MHz |

**Table 7. Ordering Information**

| Device | Tape and Reel Information | Package |
|---|---|---|
| A5G38H055NT4 | T4 Suffix = 2,500 Units, 16 mm Tape Width, 13–inch Reel | DFN 7 × 6.5 |

1. Part internally input matched.
2. All data measured in reference circuit with device soldered to printed circuit board.

## Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

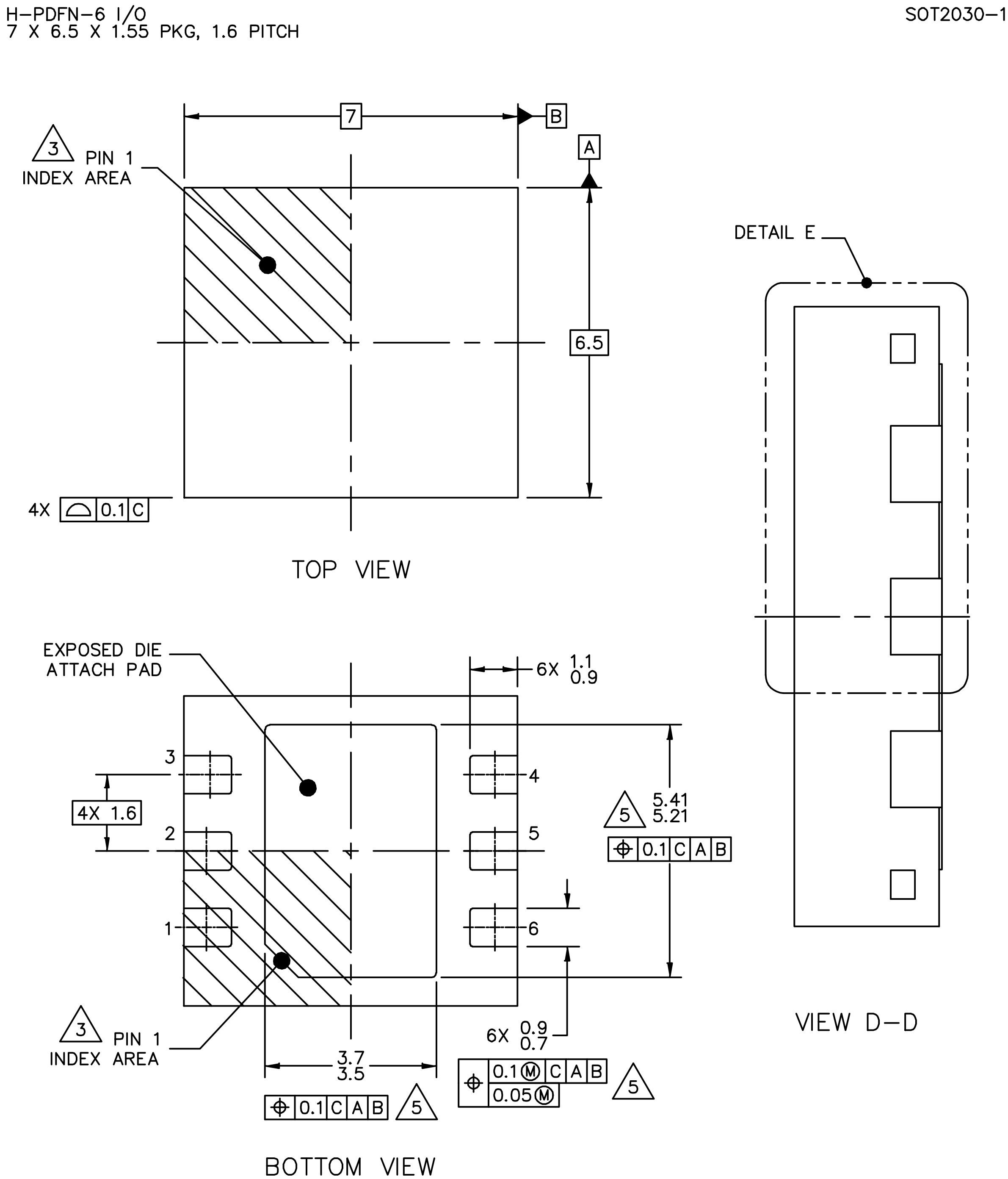
### Bias ON the device

1. Set gate voltage $V_{GSA}$ and $V_{GSB}$ to –5 V.
2. Set drain voltage $V_{DSA}$ and $V_{DSB}$ to nominal supply voltage (+48 V).
3. Increase $V_{GSA}$ (carrier side) until $I_{DQA}$ current is attained.
4. Increase $V_{GSB}$ (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

### Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage $V_{GSA}$ and $V_{GSB}$ to –5 V.
3. Adjust drain voltage $V_{DSA}$ and $V_{DSB}$ to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable $V_{GSA}$ and $V_{GSB}$.

# Package Information



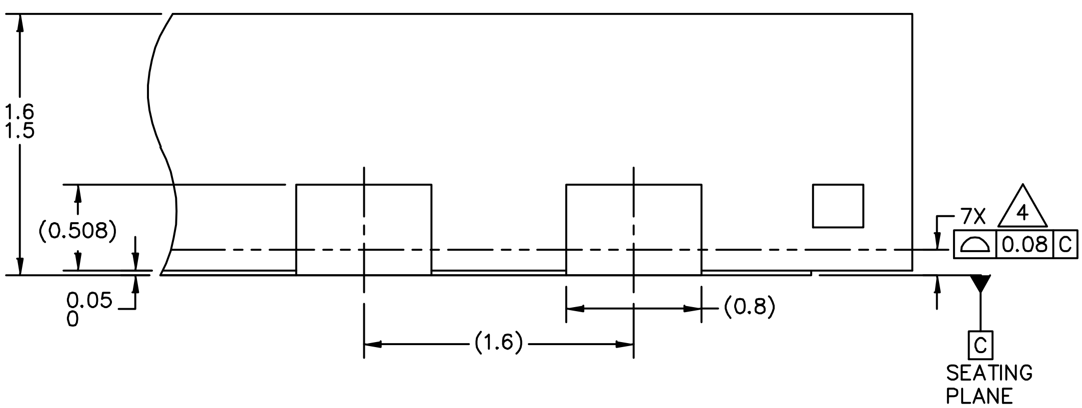



DATE: 02 APR 2020

| MECHANICAL OUTLINE | STANDARD: | DRAWING NUMBER: | REVISION: | PAGE: |
|---|---|---|---|---|
| PRINT VERSION NOT TO SCALE | NON JEDEC | 98ASA01485D | A | 1 OF 6 |

H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1




DETAIL E
VIEW ROTATED 90°CW

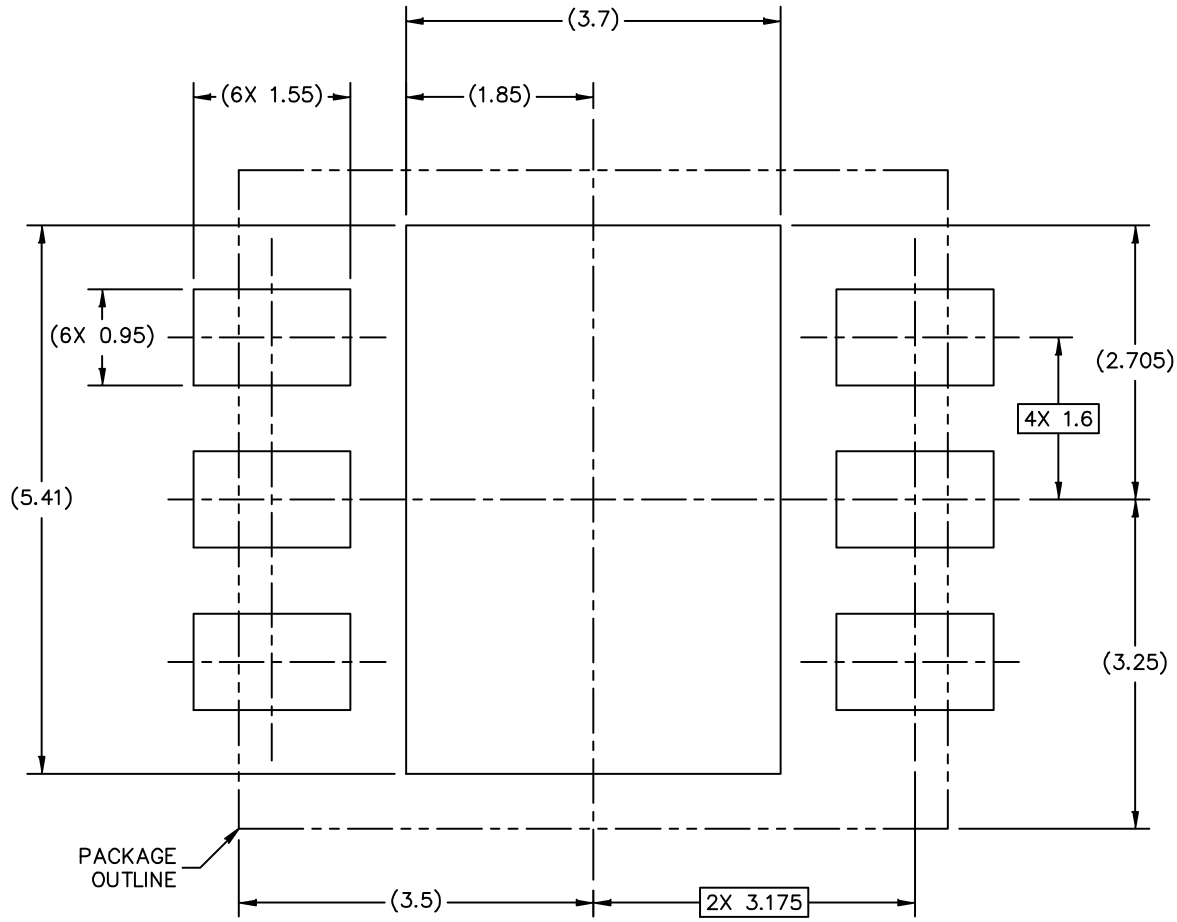


DATE: 02 APR 2020

| MECHANICAL OUTLINE | STANDARD: | DRAWING NUMBER: | REVISION: | PAGE: |
|---|---|---|---|---|
| PRINT VERSION NOT TO SCALE | NON JEDEC | 98ASA01485D | A | 2 |

H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1




PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

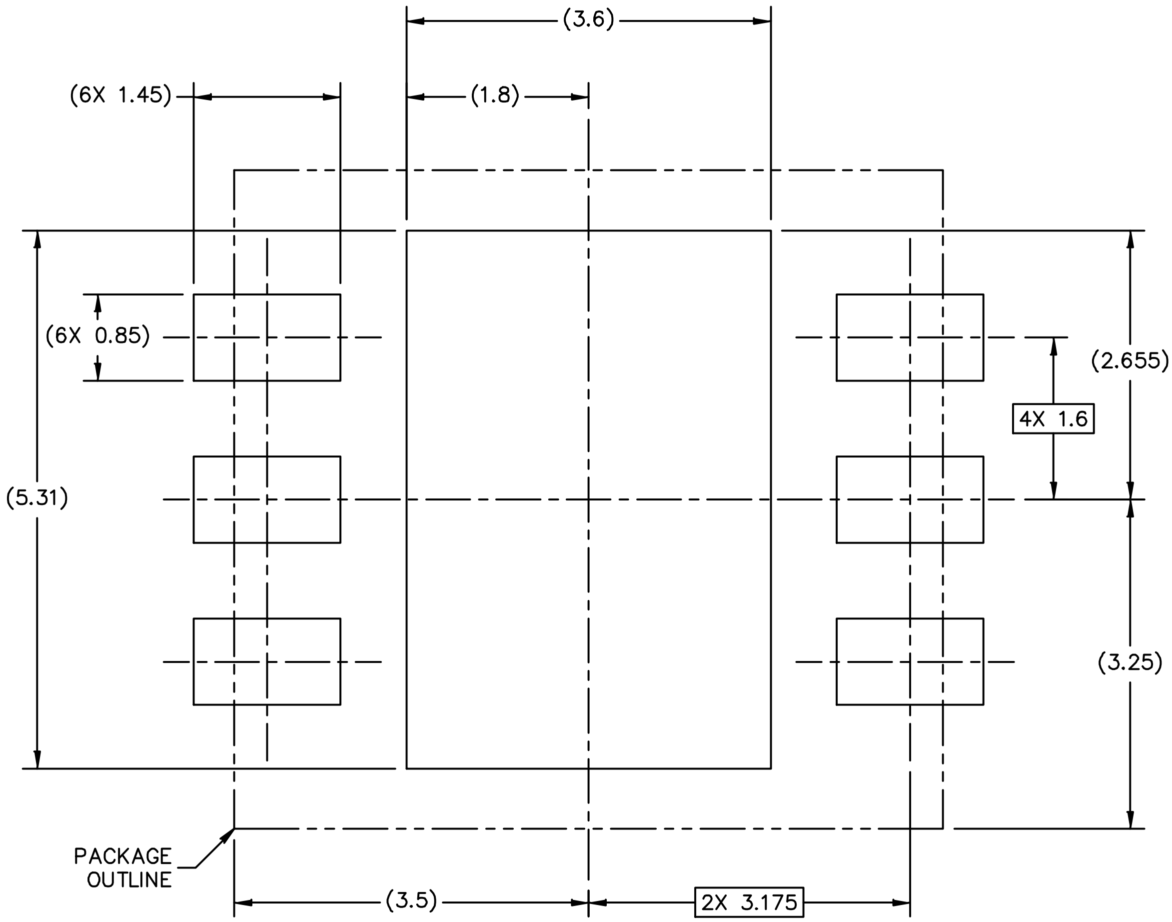


DATE: 02 APR 2020

| MECHANICAL OUTLINE | STANDARD: | DRAWING NUMBER: | REVISION: | PAGE: |
|---|---|---|---|---|
| PRINT VERSION NOT TO SCALE | NON JEDEC | 98ASA01485D | A | 3 |

H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1




PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

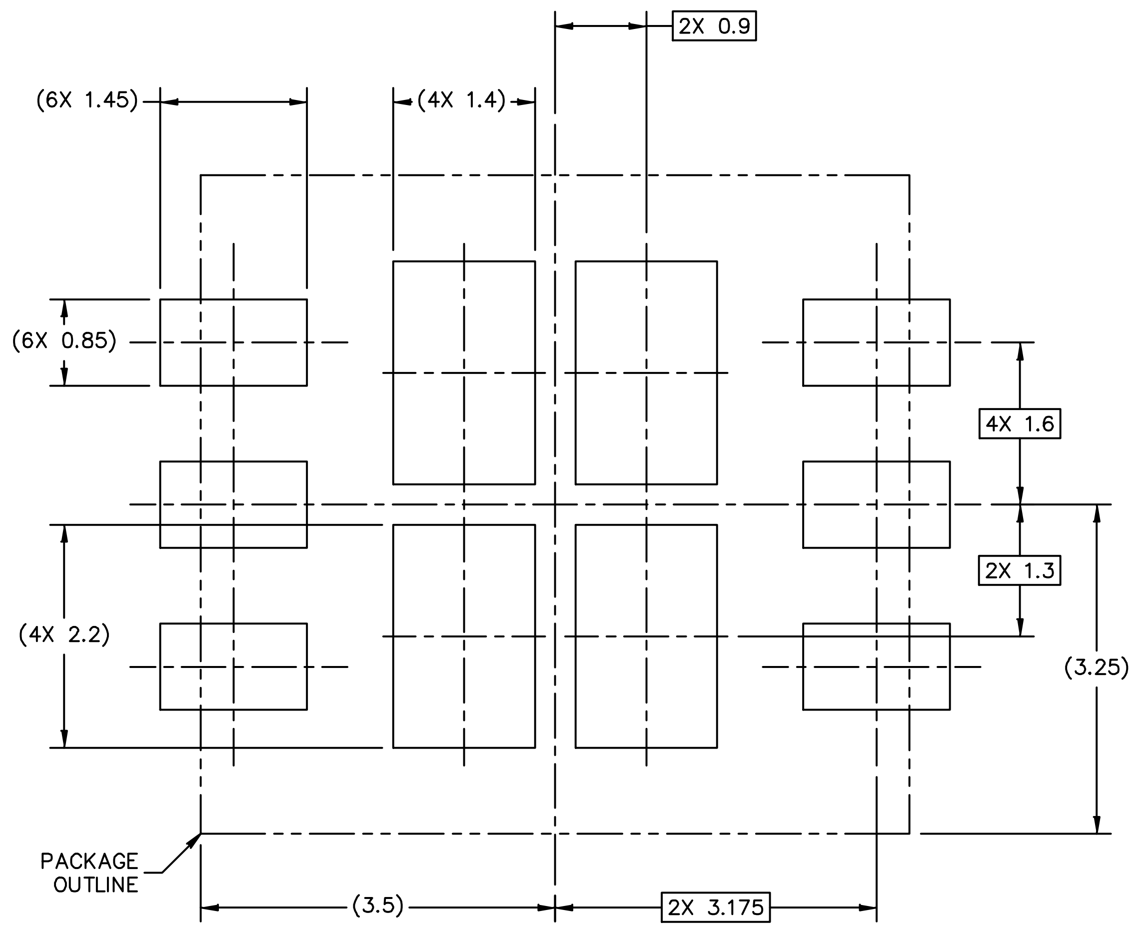


DATE: 02 APR 2020

| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: | DRAWING NUMBER: | REVISION: | PAGE: |
|---|---|---|---|---|
| | NON JEDEC | 98ASA01485D | A | 4 |

H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1




STENCIL THICKNESS 0.125 OR 0.15

## PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



DATE: 02 APR 2020

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01485D | REVISION:<br>A | PAGE:<br>5 |
| --- | --- | --- | --- | --- |

H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. RADIUS ON LEAD AND DIE ATTACH FLAG IS OPTIONAL.



DATE: 02 APR 2020

| MECHANICAL OUTLINE | STANDARD: | DRAWING NUMBER: | REVISION: | PAGE: |
|---|---|---|---|---|
| PRINT VERSION NOT TO SCALE | NON JEDEC | 98ASA01485D | A | 6 |

# Product Documentation and Software

Refer to the following resources to aid your design process.

**Application Notes**

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

**Software**

- .s2p File

# Revision History

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | Mar. 2023 | • Initial release of data sheet |
| 1 | Mar. 2023 | • Typical Performance table: updated, p. 3 |

## *How to Reach Us*

**Home Page:**
nxp.com

**Web Support:**
nxp.com/support



For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: March 2023
Document identifier: A5G38H055N