

# A5M34TG040-TC

## Airfast Power Amplifier Module

Rev. 1 — 13 March 2024

Product data sheet



## 1 General description

The A5M34TG040-TC is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN-on-SiC power amplifiers are designed for TDD LTE and 5G systems.

## 2 Features and benefits

- 2-stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Thermal path is separated from electrical/solder connection path for enhanced thermal dissipation
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude

## 3 Typical performance

Table 1. 3300–3670 MHz — Typical LTE performance

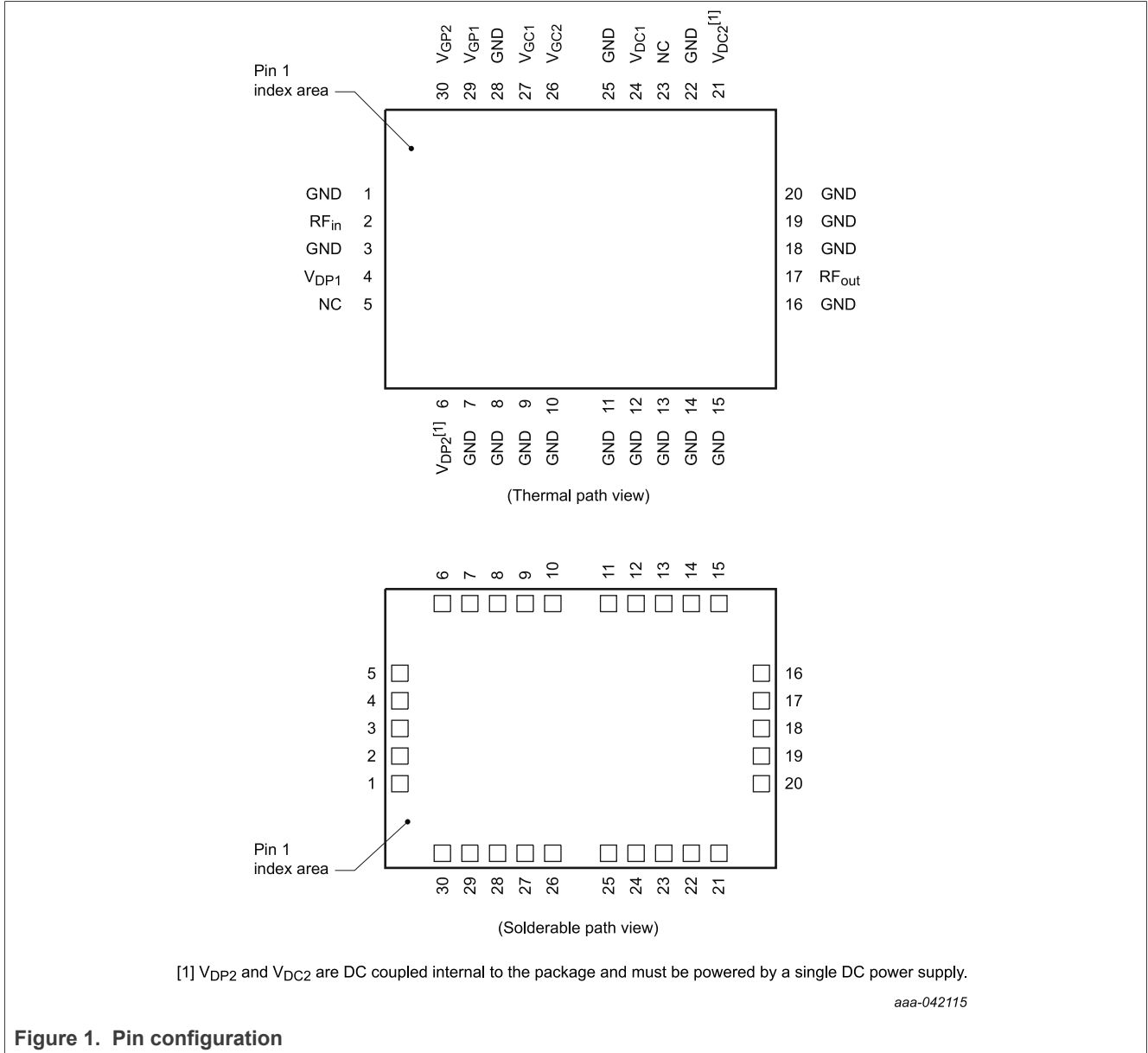
$P_{out} = 10.7 \text{ W Avg.}$ ,  $V_{DC1} = V_{DP1} = 5 \text{ Vdc}$ ,  $V_{DC2} = V_{DP2} = 48 \text{ Vdc}$ ,  $1 \times 20 \text{ MHz LTE}$ ,  $\text{Input Signal PAR} = 8 \text{ dB @ } 0.01\% \text{ Probability on CCDF.}^{[1]}$

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3310 MHz	31.2	-30.7	42.1
3500 MHz	31.0	-30.8	46.0
3660 MHz	30.7	-31.4	48.0

[1] All data measured with device soldered to NXP reference circuit.



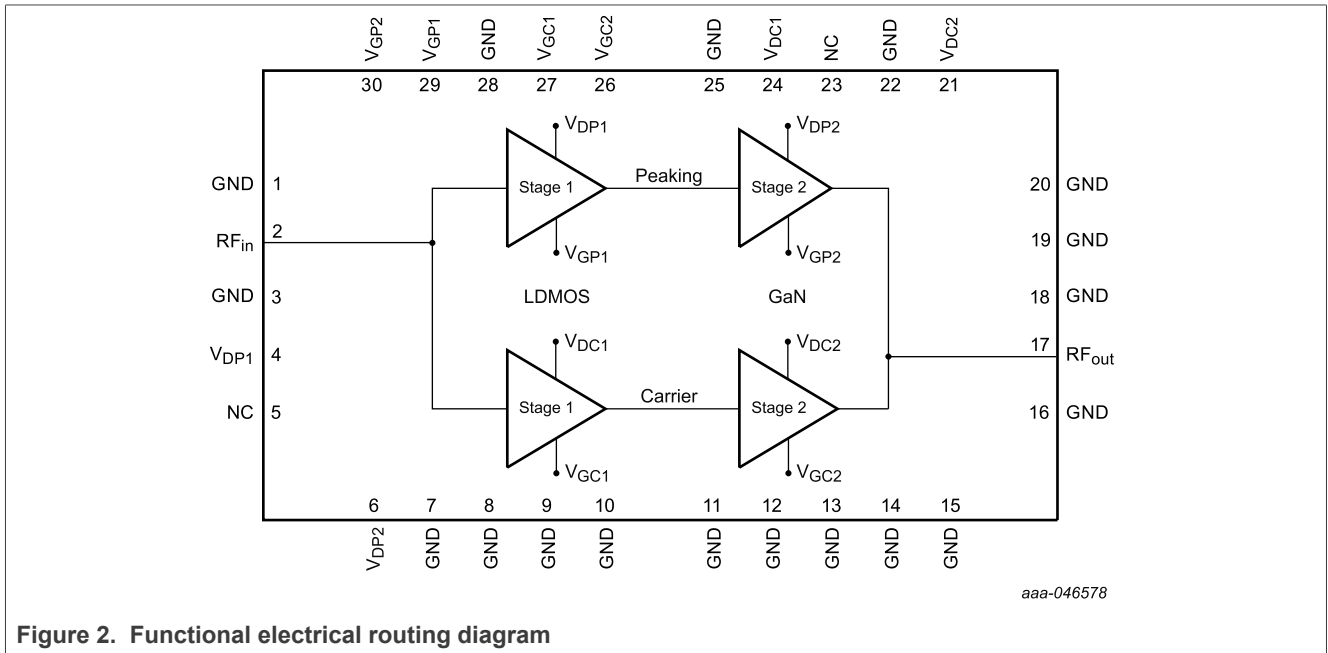
**4 Pinning information**



**Figure 1. Pin configuration**

**Table 2. Pin description**

Pin Number	Pin Function	Pin Description
1, 3, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 22, 25, 28	GND	Ground
2	RF <sub>in</sub>	RF Input
4	V <sub>DP1</sub>	Peaking Drain Supply, Stage 1
5, 23	NC	No Connection
6	V <sub>DP2</sub>	Peaking Drain Supply, Stage 2
17	RF <sub>out</sub>	RF Output
21	V <sub>DC2</sub>	Carrier Drain Supply, Stage 2
24	V <sub>DC1</sub>	Carrier Drain Supply, Stage 1
26	V <sub>GC2</sub>	Carrier Gate Supply, Stage 2
27	V <sub>GC1</sub>	Carrier Gate Supply, Stage 1
29	V <sub>GP1</sub>	Peaking Gate Supply, Stage 1
30	V <sub>GP2</sub>	Peaking Gate Supply, Stage 2



**Figure 2. Functional electrical routing diagram**

## 5 Ordering information

**Table 3. Ordering information**

Device	Tape and Reel Information	Package
A5M34TG040-TCT1	T1 Suffix = 1,000 Units, 24 mm Tape Width, 13-inch Reel	14 mm × 10 mm Module

## 6 Product marking

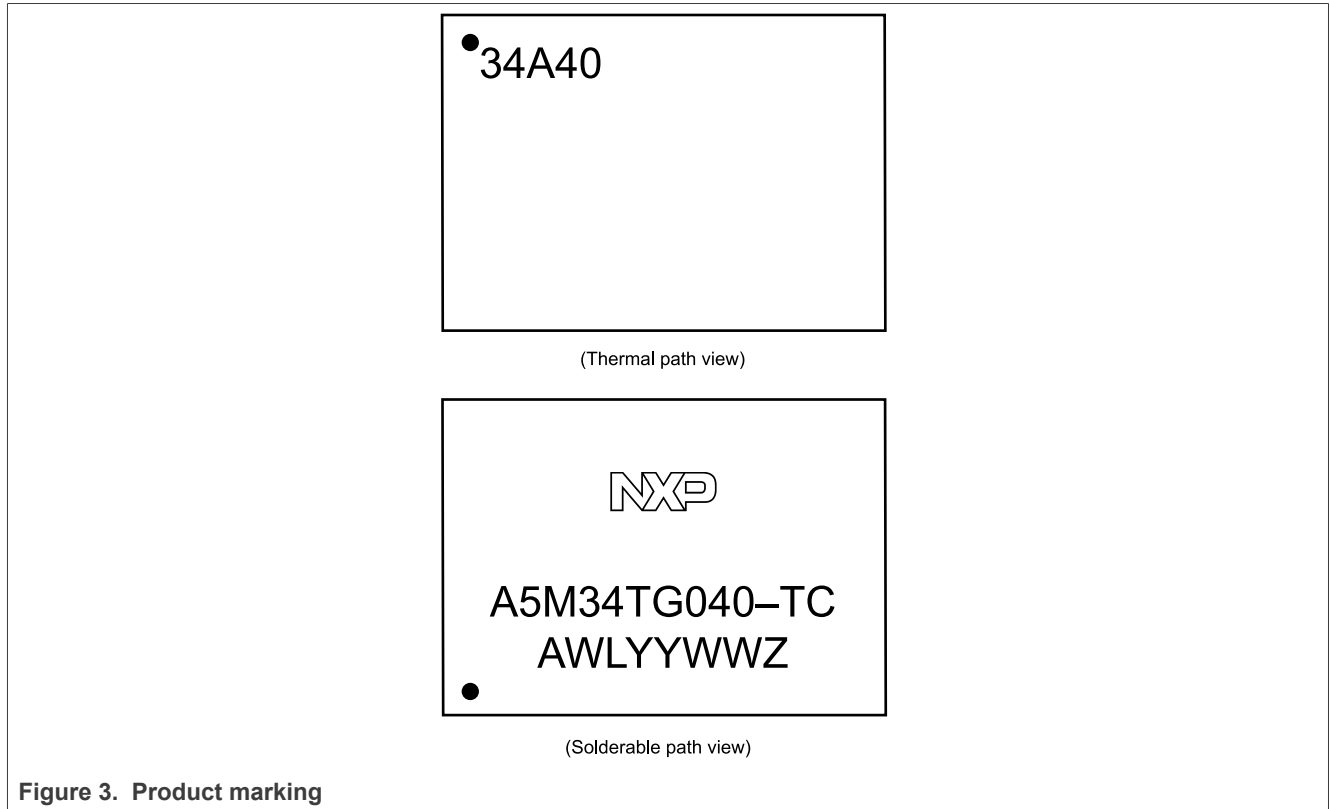


Figure 3. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

## 7 Limiting values

Table 5. Limiting values

Rating	Symbol	Value	Unit
Gate-Bias Voltage Range	$V_{G1}$ $V_{G2}$	-0.5 to +10 -6, 0	Vdc
Operating Voltage Range	$V_{DD1}$ $V_{DD2}$	4.75 to 5.25 +38 to +55	Vdc
Maximum Forward Gate Current, $I_{G(A+B)}$ , @ $T_C = 25^\circ\text{C}$	$I_{GMAX}$	11.3	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Case Operating Temperature	$T_C$	125	$^\circ\text{C}$
Maximum Channel Temperature	$T_{CH}$	225	$^\circ\text{C}$
Peak Input Power (3500 MHz, Pulsed CW, 10 $\mu\text{sec}(\text{on})$ , 10% Duty Cycle, $V_{DC1} = V_{DP1} = 5 \text{ Vdc}$ , $V_{DC2} = V_{DP2} = 48 \text{ Vdc}$ )	$P_{in}$	28	dBm

## 8 Lifetime

Table 6. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure (Case Temperature $125^\circ\text{C}$ , 75% Duty Cycle, 10.7 W Avg., $V_{DC1} = V_{DP1} = 5 \text{ Vdc}$ , $V_{DC2} = V_{DP2} = 48 \text{ Vdc}$ )	MTTF	> 10	Years

## 9 Thermal characteristics

Table 7. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case (Case Temperature $125^\circ\text{C}$ , $P_D = 14.0 \text{ W}$ )	$R_{\theta SC} \text{ (IR)}$	4.4 <sup>[1]</sup>	$^\circ\text{C/W}$
Thermal Resistance by Finite Element Analysis, Channel-to-Case (Case Temperature $125^\circ\text{C}$ , $P_D = 12.7 \text{ W}$ )	$R_{\theta CHC} \text{ (FEA)}$	7.9 <sup>[2]</sup>	$^\circ\text{C/W}$

- [1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955. High conductivity thermal interface used.
- [2]  $R_{\theta CHC} \text{ (FEA)}$  must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression  $\text{MTTF (hours)} = 10^{[A + B/(T + 273)]}$ , where T is the channel temperature in degrees Celsius, A = -11.6 and B = 9129.

## 10 ESD protection characteristics

Table 8. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

## 11 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, EIA/IPC/JEDEC J-STD-020/JEDEC J-STD-075A	3/R6	250	°C

## 12 Electrical characteristics

### 12.1 DC characteristics — off characteristics

Table 10. DC characteristics — off characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Carrier + Peaking Stage 2, GaN — off characteristics</b>					
Off-State Drain Leakage <sup>[1]</sup> ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ )	$I_{D(BR)}$	—	—	5.0	mAdc
Off-State Gate Leakage ( $V_{DS} = 48\text{ Vdc}$ , $V_{GS} = -7\text{ Vdc}$ )	$I_{GLK}$	-4.0	—	—	mAdc

[1] Carrier side and Peaking side are tied together for these measurements.

**12.2 DC characteristics — on characteristics**

**Table 11. DC characteristics — on characteristics**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
<b>Carrier Stage 1, LDMOS — on characteristics</b>				
Gate Threshold Voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DC1} = 120\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.4	$\pm 0.4$	Vdc
Gate Quiescent Voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DQC1} = 145\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	2.0	$\pm 0.4$	Vdc
<b>Carrier Stage 2, GaN — on characteristics</b>				
Gate Threshold Voltage <sup>[1]</sup> ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 11.3\text{ mAdc}$ )	$V_{GS(th)}$	-2.7	$\pm 1.0$	Vdc
Gate Quiescent Voltage ( $V_{DS} = 48\text{ Vdc}$ , $I_{DQC2} = 35\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	-2.7	$\pm 1.0$	Vdc
<b>Peaking Stage 1, LDMOS — on characteristics</b>				
Gate Threshold Voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DP1} = 120\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.4	$\pm 0.4$	Vdc
Gate Quiescent Voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DQP1} = 30\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	1.8	$\pm 0.4$	Vdc
<b>Peaking Stage 2, GaN — on characteristics</b>				
Gate Threshold Voltage <sup>[1]</sup> ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 11.3\text{ mAdc}$ )	$V_{GS(th)}$	-2.7	$\pm 1.0$	Vdc
Gate Quiescent Voltage ( $V_{DS} = 48\text{ Vdc}$ , $I_{DQP2} = 3\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	-2.9	$\pm 1.0$	Vdc

[1] Carrier side and Peaking side are tied together for these measurements.

**12.3 Functional tests**

**Table 12. Functional tests — 3300 MHz**

(In NXP Doherty Production ATE<sup>[1]</sup> Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[2]</sup>  $V_{DD1} = 5\text{ Vdc}$ ,  $V_{DD2} = 48\text{ Vdc}$ ,  $I_{DQC1} = 145\text{ mA}$ ,  $I_{DQC2} = 35\text{ mA}$ ,  $I_{DQP1} = 30\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 0.2)^{[3]}\text{ Vdc}$ ,  $P_{out} = 10.7\text{ W Avg.}$ , 1-tone CW,  $f = 3300\text{ MHz}$ .

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	29.3	31.9	—	dB
Drain Efficiency	$\eta_D$	39.0	42.1	—	%
$P_{out}$ @ 3 dB Compression Point (Pulsed CW, 5% Duty Cycle)	P3dB	48.0	49.1	—	dBm

[1] ATE is a socketed test environment.

[2] Part input and output matched to 50 ohms.

[3] Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 40\text{ mA}$  current is attained, and then subtract 0.2 V for final  $V_{GP2}$  bias voltage.

**Table 13. Functional tests — 3670 MHz**

(In NXP Doherty Production ATE<sup>[1]</sup> Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[2]</sup>  $V_{DD1} = 5\text{ Vdc}$ ,  $V_{DD2} = 48\text{ Vdc}$ ,  $I_{DQC1} = 145\text{ mA}$ ,  $I_{DQC2} = 35\text{ mA}$ ,  $I_{DQP1} = 30\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 0.2)^{[3]}\text{ Vdc}$ ,  $P_{out} = 10.7\text{ W Avg.}$ , 1-tone CW,  $f = 3670\text{ MHz}$ .

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	28.6	31.5	—	dB
Drain Efficiency	$\eta_D$	43.0	49.3	—	%
$P_{out}$ @ 3 dB Compression Point (Pulsed CW, 5% Duty Cycle)	P3dB	48.4	49.7	—	dBm

[1] ATE is a socketed test environment.

[2] Part input and output matched to 50 ohms.

[3] Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 40\text{ mA}$  current is attained, and then subtract 0.2 V for final  $V_{GP2}$  bias voltage.

## 12.4 Wideband ruggedness

**Table 14. Wideband ruggedness**

(In NXP Doherty Power Amplifier Module Reference Circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>  $I_{DQC1} = 145\text{ mA}$ ,  $I_{DQC2} = 35\text{ mA}$ ,  $I_{DQP1} = 30\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 0.2)^{[2]}\text{ Vdc}$ ,  $f = 3500\text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Symbol	Min	Typ	Max	Unit
ISBW of 400 MHz at 55 Vdc, 3 dB Input Overdrive from 10.7 W Avg. Modulated Output Power		No Device Degradation			

[1] All data measured in fixture with device soldered to NXP reference circuit.

[2] Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 40\text{ mA}$  current is attained, and then subtract 0.2 V for final  $V_{GP2}$  bias voltage.



**12.5 Typical performance**

**Table 15. Typical performance**

(In NXP Doherty Power Amplifier Module Reference Circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>

$V_{DD1} = 5\text{ Vdc}$ ,  $V_{DD2} = 48\text{ Vdc}$ ,  $I_{DQC1} = 145\text{ mA}$ ,  $I_{DQC2} = 35\text{ mA}$ ,  $I_{DQP1} = 30\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 0.2)^{[2]}\text{ Vdc}$ , 3500 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	230	—	MHz
<b>1-carrier 20 MHz LTE, 8 dB Input Signal PAR</b>					
Gain	G	—	31.0	—	dB
Power Added Efficiency	PAE	—	46.0	—	%
Adjacent Channel Power Ratio	ACPR	—	-30.8	—	dBc
Adjacent Channel Power Ratio	ALT1	—	-45.6	—	dBc
Adjacent Channel Power Ratio	ALT2	—	-52.0	—	dBc
Gain Flatness <sup>[3]</sup>	G <sub>F</sub>	—	0.5	—	dB
<b>Pulsed CW, 10% Duty Cycle</b>					
P <sub>out</sub> @ 3 dB Compression Point	P3dB	—	49.2	—	dBm
AM/PM @ P3dB	Φ	—	-16	—	°
Gain Variation @ Avg. Power over Temperature (-40°C to +125°C)	ΔG	—	0.034	—	dB/°C
P3dB Variation over Temperature (-40°C to +125°C)	ΔP3dB	—	0.005	—	dB/°C

[1] All data measured in fixture with device soldered to NXP reference circuit.

[2] Increase V<sub>GP2</sub> (peaking side) until I<sub>DQP2</sub> = 40 mA current is attained, and then subtract 0.2 V for final V<sub>GP2</sub> bias voltage.

[3] Gain flatness = Max(G(f<sub>Low</sub> to f<sub>High</sub>)) - Min(G(f<sub>Low</sub> to f<sub>High</sub>)).

**Correct Biasing Sequence****Turn ON:****Bias ON the GaN final stage first**

1. Set gate voltage  $V_{GC2}$  and  $V_{GP2}$  to  $-5$  V.
2. Set drain voltage  $V_{DC2}$  and  $V_{DP2}$  to nominal supply voltage ( $+48$  V).
3. Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 40$  mA current is attained, and then subtract  $0.2$  V for final  $V_{GP2}$  bias voltage.
4. Increase  $V_{GC2}$  (carrier side) until  $I_{DQC2}$  current is attained.

**Bias ON the LDMOS driver stage second**

5. Set drain voltage  $V_{DC1}$  and  $V_{DP1}$  to nominal supply voltage ( $+5$  V).
6. Increase  $V_{GC1}$  (carrier side) until  $I_{DQC1}$  current is attained.
7. Increase  $V_{GP1}$  (peaking side) until  $I_{DQP1}$  current is attained.
8. Apply RF input power to desired level.

**Turn OFF:****Bias OFF the GaN final stage first**

1. Disable RF input power.
2. Adjust gate voltage  $V_{GC2}$  and  $V_{GP2}$  to  $-5$  V.
3. Adjust drain voltage  $V_{DC2}$  and  $V_{DP2}$  to  $0$  V. Allow adequate time for drain voltage to reduce to  $0$  V from external drain capacitors.
4. Disable  $V_{GC2}$  and  $V_{GP2}$ .

**Bias OFF the LDMOS driver stage second**

5. Adjust gate voltage  $V_{GC1}$  and  $V_{GP1}$  to  $0$  V.
6. Adjust drain voltage  $V_{DC1}$  and  $V_{DP1}$  to  $0$  V.

### 13 Component layout and parts list

#### 13.1 Component layout

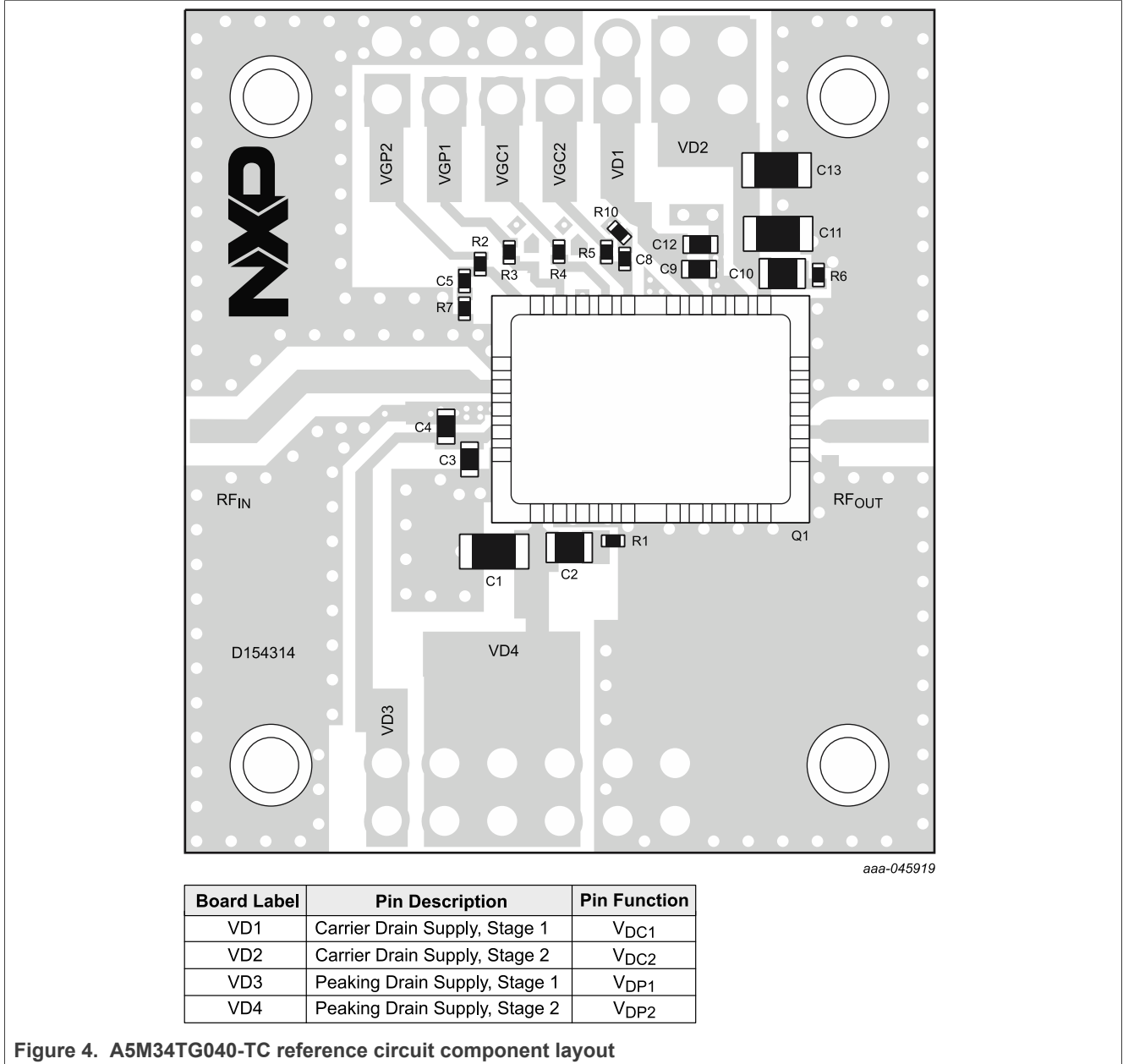


Figure 4. A5M34TG040-TC reference circuit component layout

**13.2 Component designations and values****Table 16. A5M34TG040-TC reference circuit component designations and values**

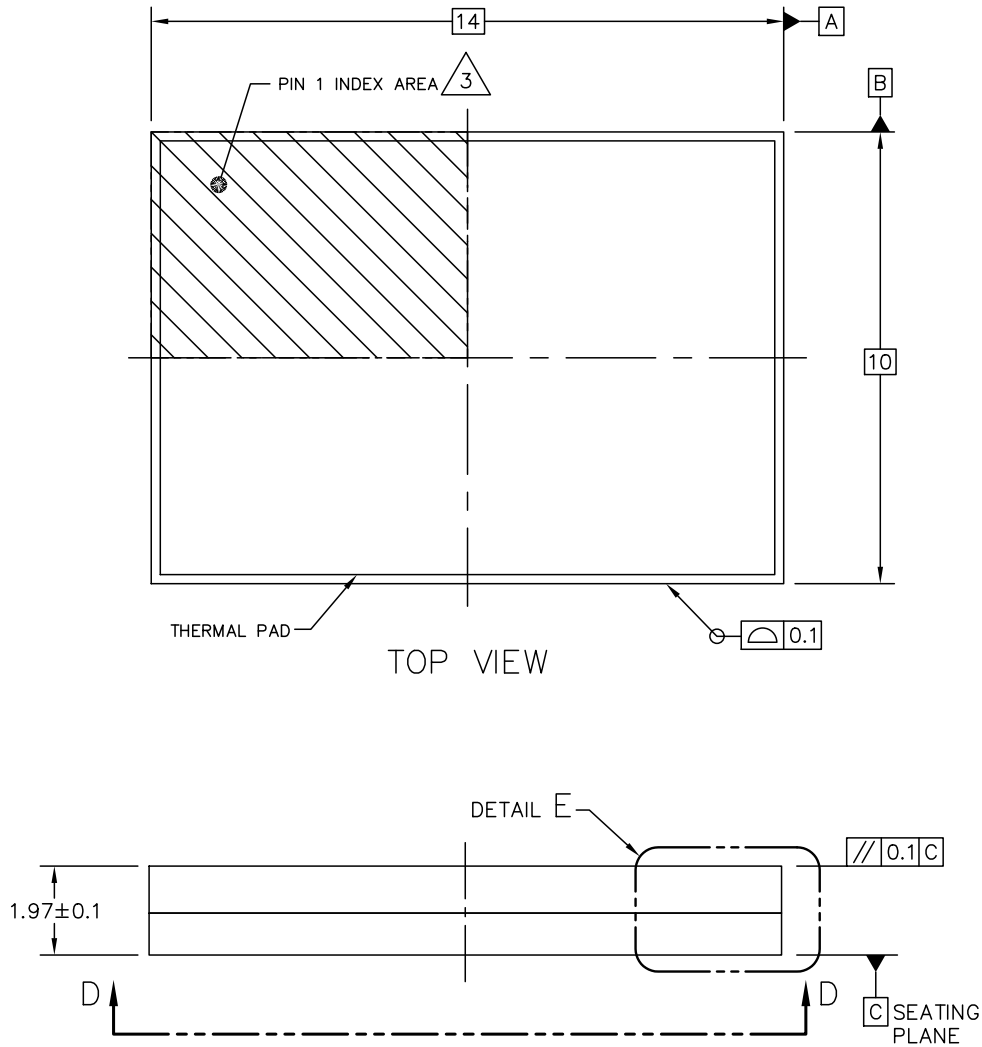
Part	Description	Part Number	Manufacturer
C1, C11, C13	4.7 $\mu$ F Chip Capacitor	GRM31CC72A475KE11L	Murata
C2, C10	1 $\mu$ F Chip Capacitor	GRM21BC72A105KE01L	Murata
C3, C9	1 $\mu$ F Chip Capacitor	GRT188R61H105KE13D	Murata
C4, C12	10 $\mu$ F Chip Capacitor	GRM188R61E106KA73D	Murata
C5	0.1 $\mu$ F Chip Capacitor	GRM155R61H104KE19D	Murata
C8	10 nF Chip Capacitor	GRM155R71E103KA01D	Murata
Q1	Power Amplifier Module	A5M34TG040-TC	NXP
R1, R6	2 $\Omega$ , 1/10 W Chip Resistor	ERJ-2GEJ2R0X	Panasonic
R2, R3, R5	1 $\Omega$ , 1/10 W Chip Resistor	ERJ-2GEJ1R0X	Panasonic
R4, R10	10 $\Omega$ , 1/10 W Chip Resistor	ERJ-2GEJ100X	Panasonic
R7	0 $\Omega$ , 1/20 W Chip Resistor	ERJ-1GN0R00C	Panasonic
PCB	Megtron R-5575, 0.020", $\epsilon_r = 3.67$	D154314	MTL

Note: Component numbers C6, C7, R8 and R9 are intentionally omitted.

**14 Package information**

H-PLGA-30 I/O  
14 X 10 X 1.97 PKG, 1 PITCH

SOT2131-2



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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01864D	REVISION: C	PAGE: 1 OF 6
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Figure 5. Package outline (14 mm × 10 mm Module) — top view, detail E

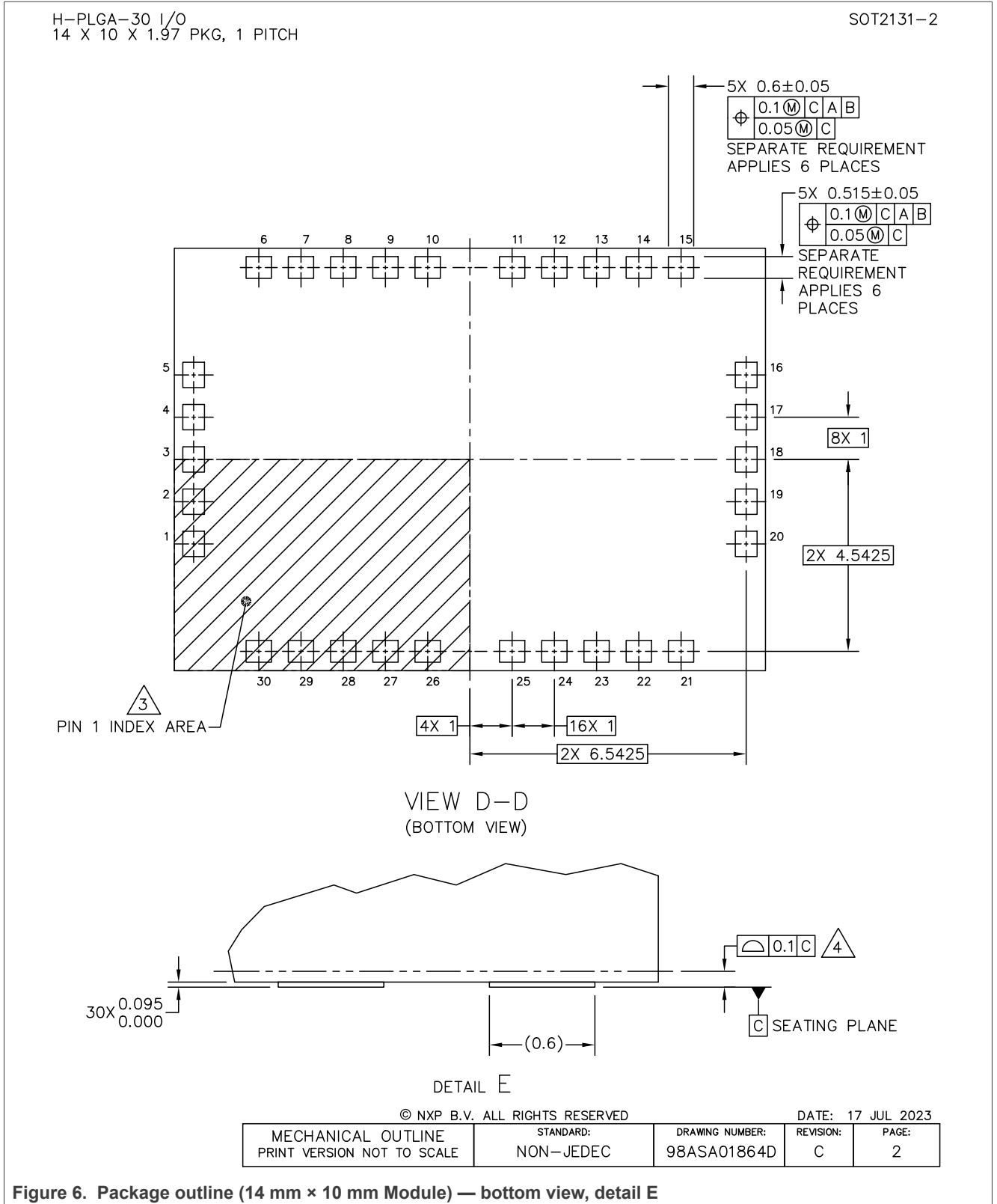
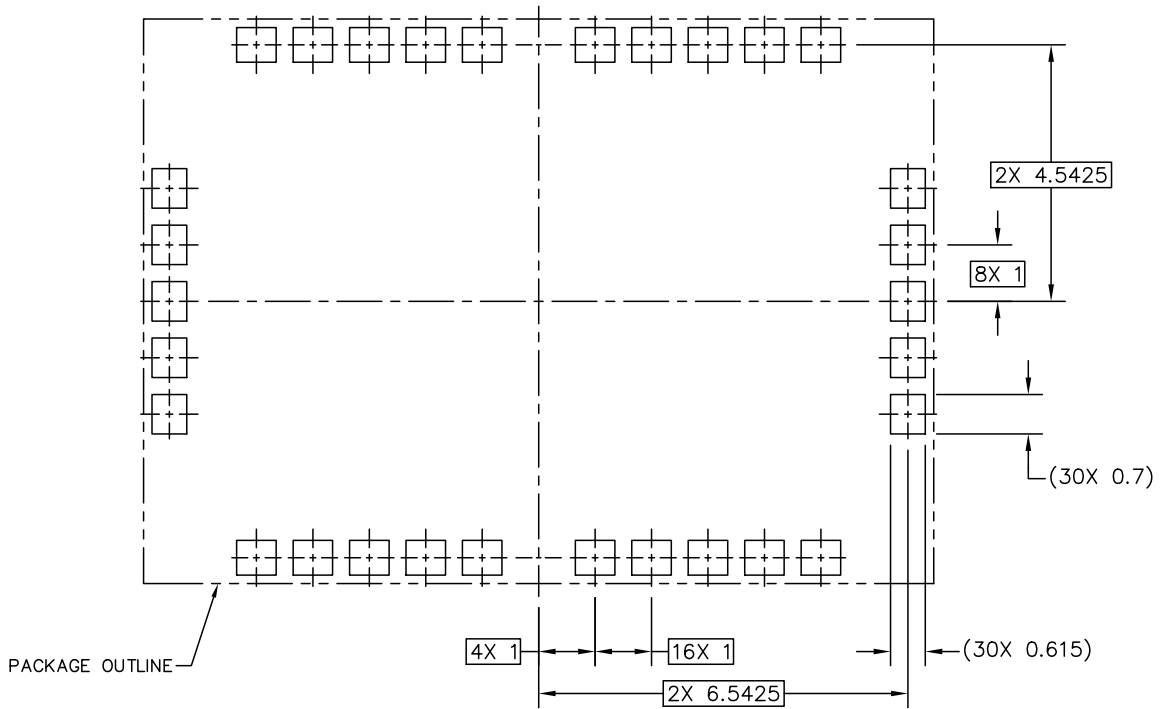


Figure 6. Package outline (14 mm x 10 mm Module) — bottom view, detail E

H-PLGA-30 I/O  
14 X 10 X 1.97 PKG, 1 PITCH

SOT2131-2



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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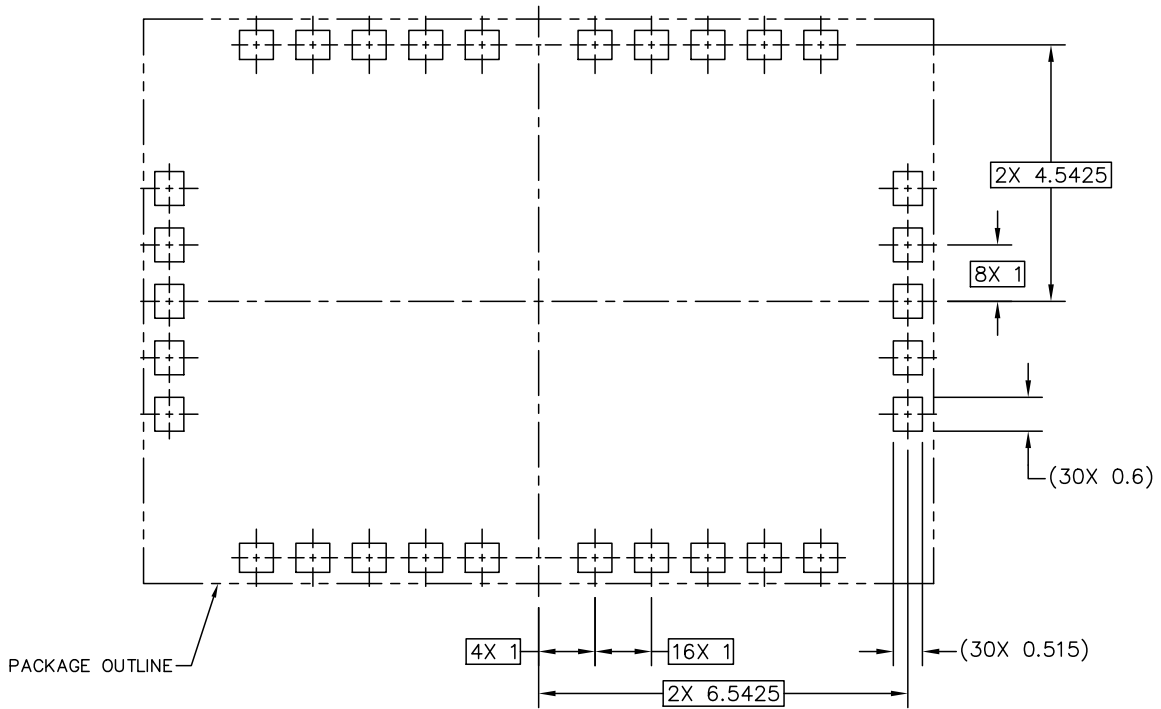
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Figure 7. Package outline (14 mm × 10 mm Module) — PCB design guidelines: solder mask opening pattern

H-PLGA-30 I/O  
14 X 10 X 1.97 PKG, 1 PITCH

SOT2131-2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

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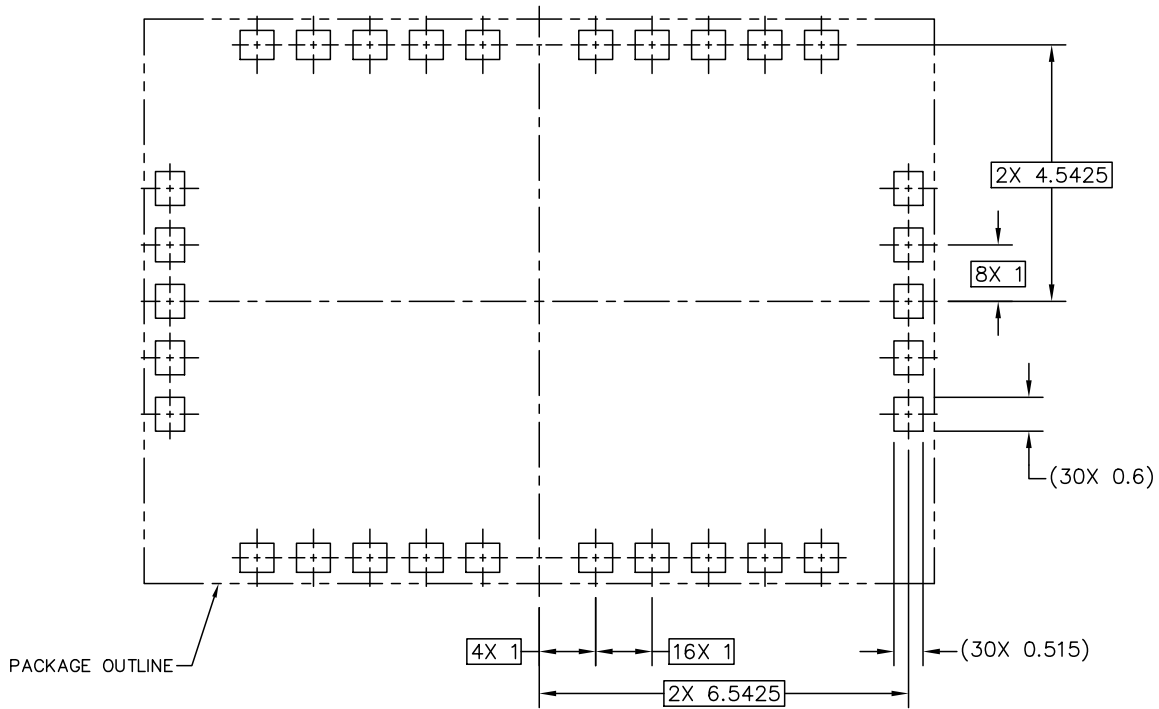
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01864D	REVISION: C	PAGE: 4
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Figure 8. Package outline (14 mm × 10 mm Module) — PCB design guidelines: I/O pads and solderable areas



H-PLGA-30 I/O  
14 X 10 X 1.97 PKG, 1 PITCH

SOT2131-2



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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**Figure 9. Package outline (14 mm × 10 mm Module) — PCB design guidelines: solder paste stencil**

H-PLGA-30 I/O  
14 X 10 X 1.97 PKG, 1 PITCH

SOT2131-2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO ALL LEADS.

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**Figure 10. Package outline (14 mm × 10 mm Module) — notes**

## 15 Product documentation and tools

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Refer to the following resources to aid your design process.

### Application notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Development tools

- Printed Circuit Boards

## 16 Revision history

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The following table summarizes revisions to this document.

Table 17. Revision history

Document ID	Release date	Description
A5M34TG040-TC Rev. 1	13 March 2024	• Initial release of product data sheet

## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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