BMA7124xB; BMA7126xB

24/26 cells analog front end IC

Rev. 1.0 — 31 August 2026 Product short data sheet

1 Product profile

1.1 General description

The BMA7124 and BMA7126 are lithium-ion battery cell controller (BCC) ICs designed for automotive applications, such as electric vehicle (EV) and hybrid electric vehicle (HEV). The BMA7124 provides 24 differential high precision lithium-ion cell voltage measurements and the BMA7126 provides 26 differential high precision lithium-ion cell voltage measurements. Both products are offering 13 temperature measurements. An integrated DC-to-DC buck converter with operation down to 15 V supply voltage allows a high power efficiency.

Both devices provide an extensive set of passive cell voltage balancing features to equalize the individual cell voltages across the battery stack. Both devices support an isolated daisy chain interface for communication with the host MCU and have been developed in accordance with ISO 26262 and automotive safety integrity level (ASIL) D.

1.2 Features and benefits

- AEC-Q100 grade 1 qualified: −40 °C to +125 °C ambient temperature range
- ISO 26262 ASIL D support for cell voltage and cell temperature measurements from the host microcontroller unit (MCU) to the cell
- Manufactured in the SMARTMOS 10 high-voltage bipolar CMOS DMOS on silicon-on-insulator (BCD-on-SOI) process technology ensuring high robustness and proven long-term accuracy stability
- Cell voltage measurement
  - BMA7124: 8 to 24 cells per device; 120 V maximum operating cell stack voltage
  - BMA7126: 8 to 26 cells per device; 130 V maximum operating cell stack voltage
  - Single analog-to-digital converter (ADC) per channel
  - 16-bit resolution and up to ±0.7 mV typical measurement accuracy with ultra low long-term drift
  - Integrated configurable digital filter
  - Redundant comparisons of primary and secondary cell voltages
- External temperature and auxiliary voltage measurements
  - 13 analog inputs configurable as absolute or ratiometric with 5 V input range
  - 16-bit resolution
  - Integrated configurable digital filter
- Internal measurement
  - Two redundant internal temperature sensors
  - Supply voltages
- Cell voltage balancing
  - 24 and 26 internal balancing field effect transistors (FET), up to 300 mA peak with 1.5 Ω R_{DSon} per channel (typ.)
  - Support for simultaneous passive balancing of all channels with automatic odd/even sequence

  - Support permanent full odd or even bank passive balancing with 300 mA current
  - Global balancing timeout timer
  - Timer-controlled balancing with individual timers with 10 s resolution and up to 45 h duration
  - Voltage-controlled balancing with global and individual undervoltage thresholds
  - Temperature-controlled balancing; if balancing resistors or the IC are in overtemperature, balancing is interrupted
  - Configurable pulse width modulation (PWM) duty cycle balancing
  - Automatic pause of balancing during measurement with configurable filter settling time
  - Configurable delay of the start of balancing after transition to sleep
  - Automatic discharge of the battery pack (emergency discharge)
- I^2C-bus host interface to control external devices, for example, EEPROMs and security ICs
- Serial peripheral interface (SPI) host interface to control external devices, for example, a pressure sensor
- MCU peripheral interface supporting SPI or isolated daisy chain communication [transformer physical layer 3 (TPL3)]
  - 2 Mbit/s data rate for transport protocol link (TPL) interface
  - 4 Mbit/s data rate for SPI
- TPL3 daisy chain communication supports
  - Two wire daisy chain with capacitive or inductive isolation
  - Synchronization of the monitoring ICs via the communication
  - Protocol supporting up to six daisy chains and 62 nodes per chain
  - Unique device ID with dynamic addressing
- Operation modes
  - Active mode (4 mA typical) resulting in maximum 290 mW worst case power consumption due to integrated DC-to-DC converter
  - Sleep mode (45 µA)
  - Deep sleep mode (4.5 µA)
  - Cyclic wake-up to monitor the pack and the balancing function during sleep
  - Capability to wake up the host MCU via daisy chain if there is a fault event
  - Alarm output to signal events to the MCU

1.3 Applications

Automotive:

- (Plugin) hybrid electric vehicle battery management system (BMS)
- EV BMS

2 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
BMA7126SB	HLQFP100	plastic, thermal enhanced low profile quad flat package; 100 terminals; 0.50 mm pitch; 14 × 14 × 1.5 mm body	SOT2229-1
BMA7126TB	HLQFP100	plastic, thermal enhanced low profile quad flat package; 100 terminals; 0.50 mm pitch; 14 × 14 × 1.5 mm body	SOT2229-1
BMA7124SB	HLQFP100	plastic, thermal enhanced low profile quad flat package; 100 terminals; 0.50 mm pitch; 14 × 14 × 1.5 mm body	SOT2229-1
BMA7124TB	HLQFP100	plastic, thermal enhanced low profile quad flat package; 100 terminals; 0.50 mm pitch; 14 × 14 × 1.5 mm body	SOT2229-1

2.1 Ordering options

Table 2. Orderable part number

Orderable part number	Description
MBMA7126SB1AE	BMA7126SB; 26 cells analog front end IC with SPI
MBMA7126TB1AE	BMA7126TB; 26 cells analog front end IC with TPL interface
MBMA7124SB1AE	BMA7124SB; 24 cells analog front end IC with SPI
MBMA7124TB1AE	BMA7124TB; 24 cells analog front end IC with TPL interface

3 Block diagram

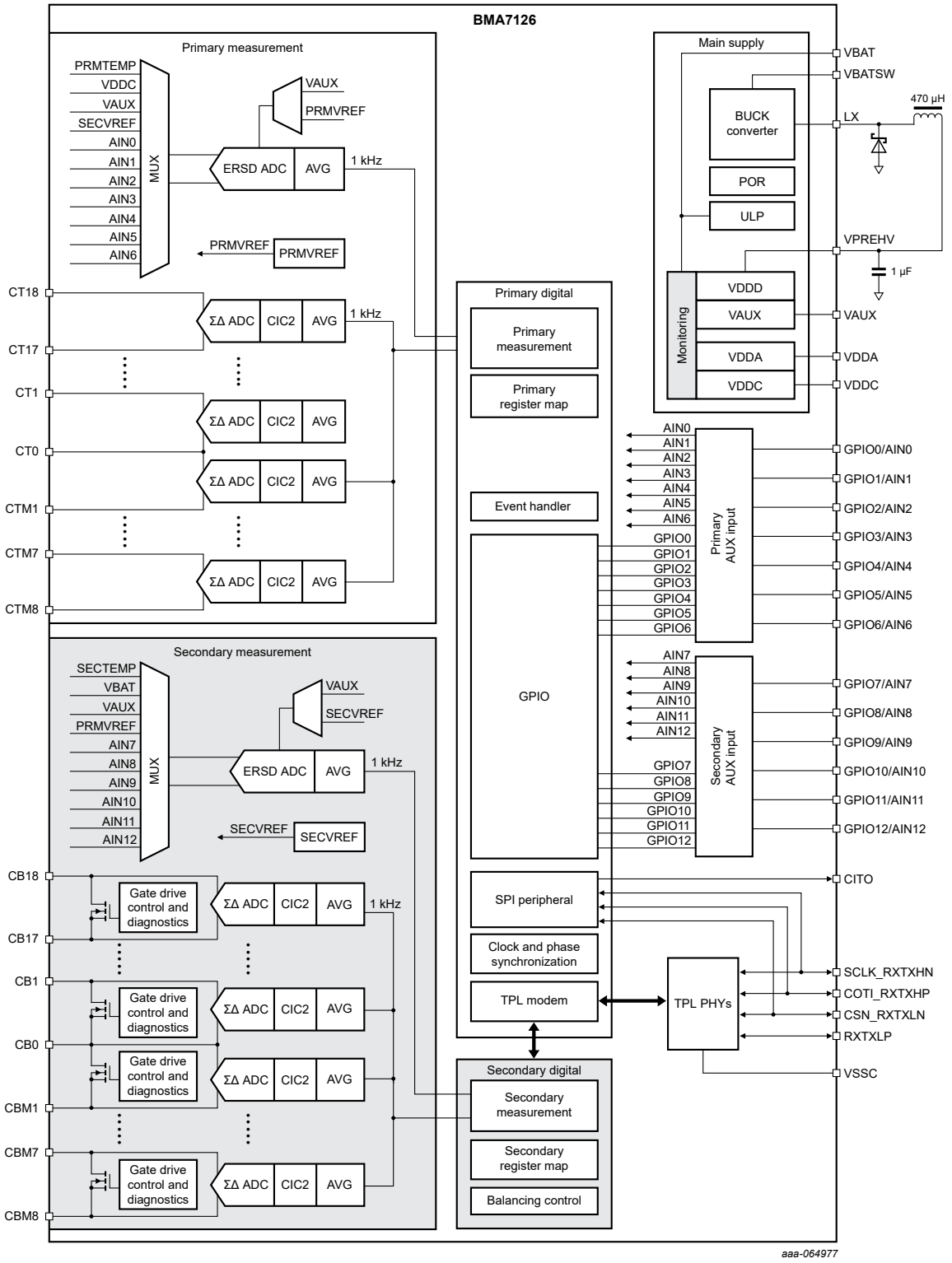


Figure 1. Block diagram of the BMA7126

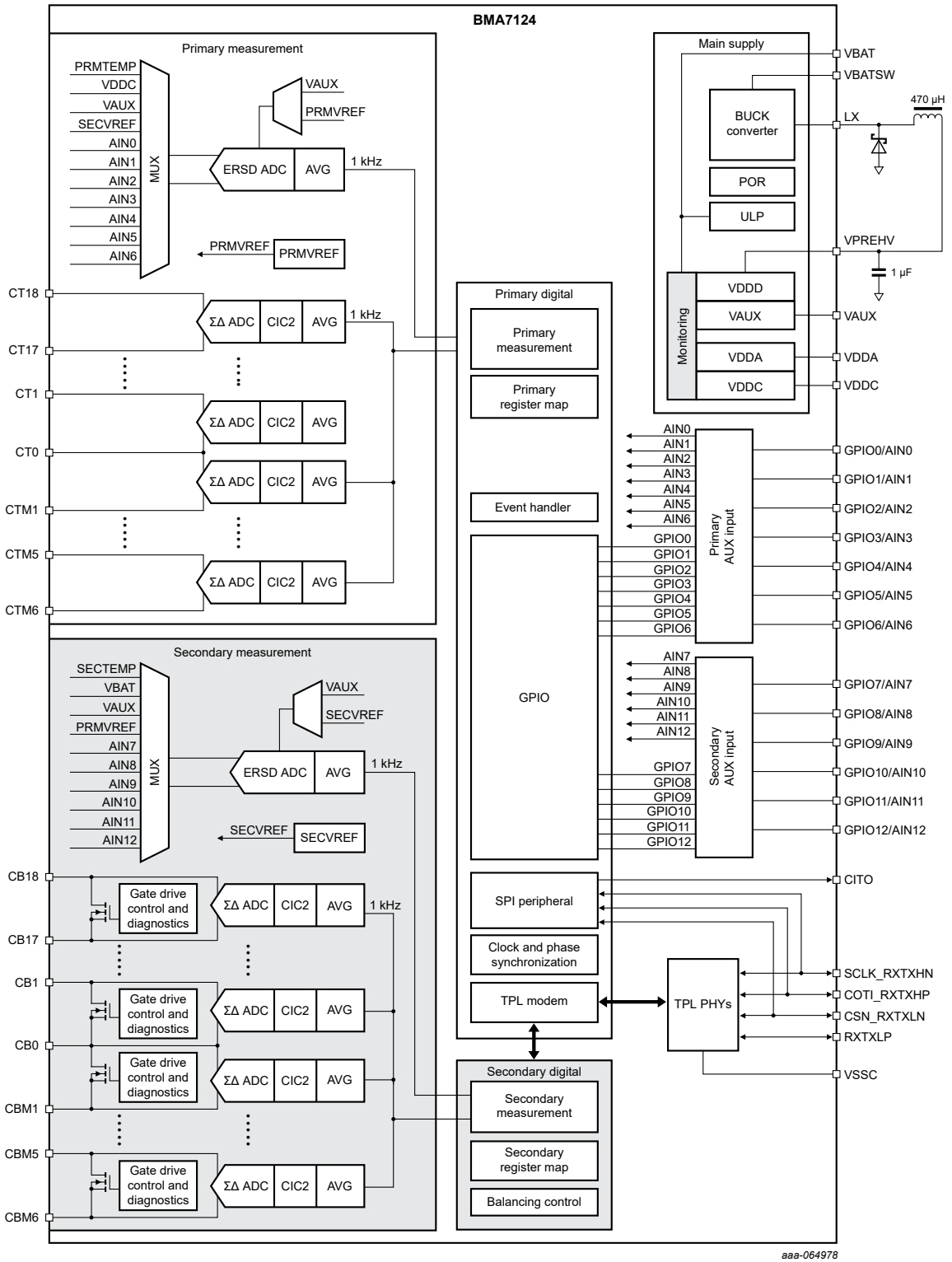


Figure 2. Block diagram of the BMA7124

4 Pinning information

4.1 Pinning

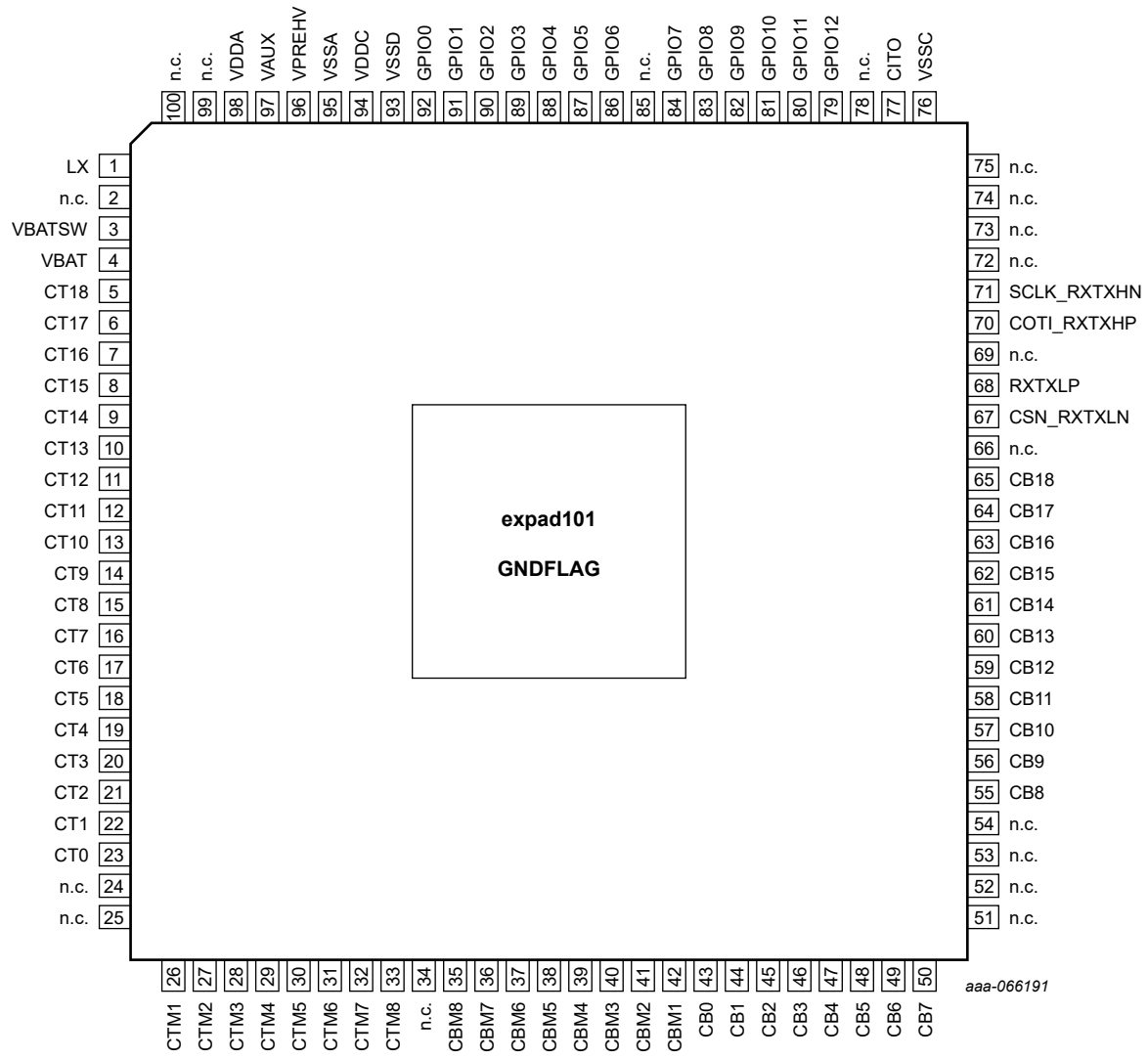


Figure 3. Pin configuration for BMA7126xB

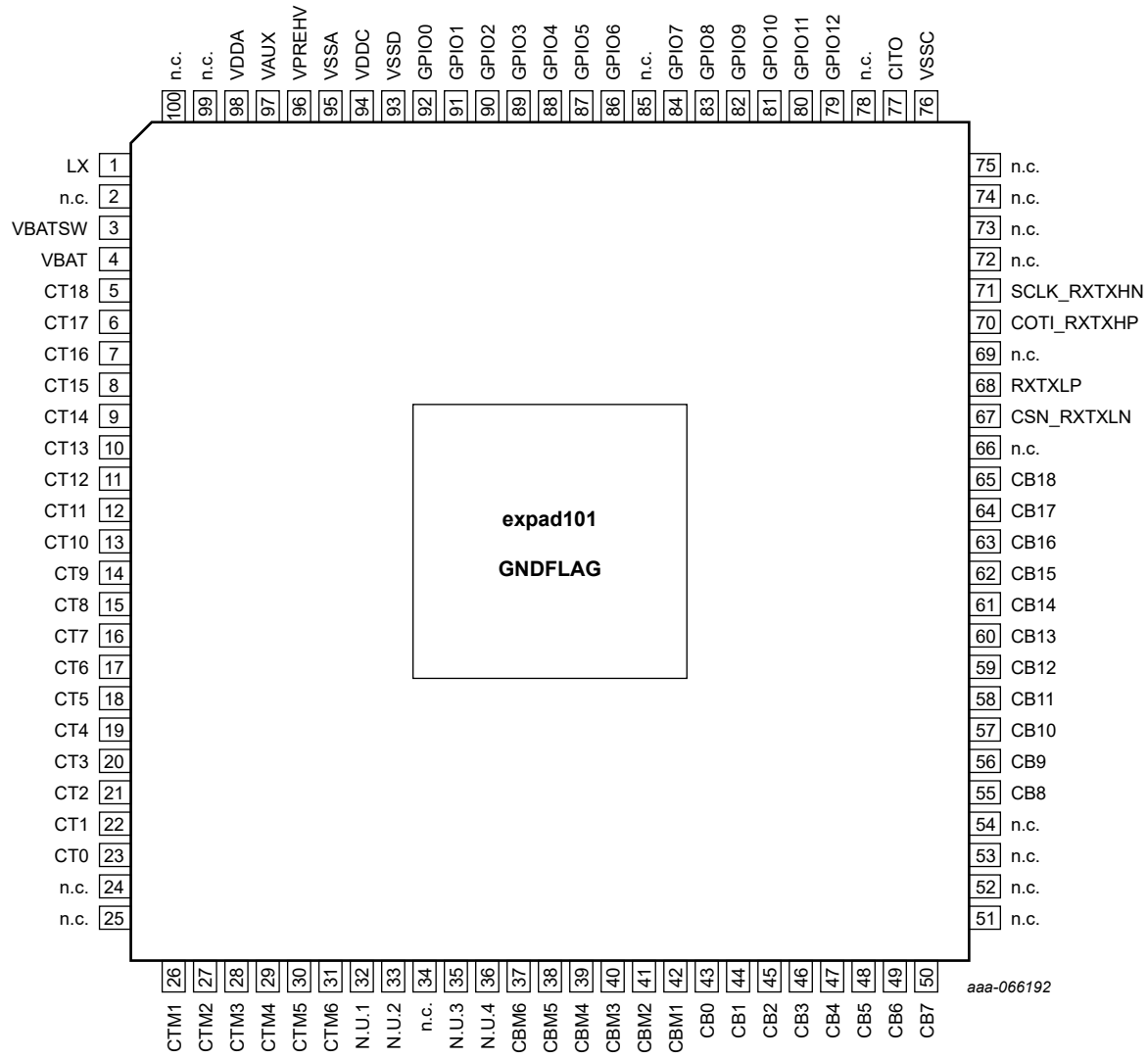


Figure 4. Pin configuration for BMA7124xB

4.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	BMA7126	BMA7124	
LX	1	1	buck converter switch output; connect to the inductance of the buck converter
n.c.	2	2	not connected
VBATSW	3	3	supply input to the internal buck converter of the device; connect to the highest cell of the module
VBAT	4	4	supply input of the product; connect to the highest cell of the module
CT18	5	5	cell terminal 18 input
CT17	6	6	cell terminal 17 input
CT16	7	7	cell terminal 16 input

Table 3. Pin description...*continued*

Symbol	Pin		Description
	BMA7126	BMA7124	
CT15	8	8	cell terminal 15 input
CT14	9	9	cell terminal 14 input
CT13	10	10	cell terminal 13 input
CT12	11	11	cell terminal 12 input
CT11	12	12	cell terminal 11 input
CT10	13	13	cell terminal 10 input
CT9	14	14	cell terminal 9 input
CT8	15	15	cell terminal 8 input
CT7	16	16	cell terminal 7 input
CT6	17	17	cell terminal 6 input
CT5	18	18	cell terminal 5 input
CT4	19	19	cell terminal 4 input
CT3	20	20	cell terminal 3 input
CT2	21	21	cell terminal 2 input
CT1	22	22	cell terminal 1 input
CT0	23	23	cell terminal 0 input
n.c.	24	24	not connected
n.c.	25	25	not connected
CTM1	26	26	cell terminal 19 input
CTM2	27	27	cell terminal 20 input
CTM3	28	28	cell terminal 21 input
CTM4	29	29	cell terminal 22 input
CTM5	30	30	cell terminal 23 input
CTM6	31	31	cell terminal 24 input
CTM7	32	-	cell terminal 25 input
N.U.1	-	32	not used; to be connected as detailed in the reference manual
CTM8	33	-	cell terminal 26 input
N.U.2	-	33	not used; connect to pin 32
n.c.	34	34	not connected
CBM8	35	-	1. Secondary cell terminal 26 input 2. Low input for cell 25 balancing
N.U.3	-	35	not used; connect to pin 36
CBM7	36	-	1. Secondary cell terminal 25 input 2. Low input for cell 24 balancing 3. High input for cell 25 balancing
N.U.4	-	36	not used; to be connected as detailed in the reference manual

Table 3. Pin description...*continued*

Symbol	Pin		Description
	BMA7126	BMA7124	
CBM6	37	-	1. Secondary cell terminal 24 input 2. Low input for cell 23 balancing 3. High input for cell 24 balancing
CBM6	-	37	1. Secondary cell terminal 24 input 2. Low input for cell 23 balancing
CBM5	38	38	1. Secondary cell terminal 23 input 2. Low input for cell 22 balancing 3. High input for cell 23 balancing
CBM4	39	39	1. Secondary cell terminal 22 input 2. Low input for cell 21 balancing 3. High input for cell 22 balancing
CBM3	40	40	1. Secondary cell terminal 21 input 2. Low input for cell 20 balancing 3. High input for cell 21 balancing
CBM2	41	41	1. Secondary cell terminal 20 input 2. Low input for cell 19 balancing 3. High input for cell 20 balancing
CBM1	42	42	1. Secondary cell terminal 19 input 2. Low input for cell 18 balancing 3. High input for cell 19 balancing
CB0	43	43	1. Secondary cell terminal 0 input 2. Low input for cell 0 balancing 3. High input for cell 18 balancing
CB1	44	44	1. Secondary cell terminal 1 input 2. Low input for cell 1 balancing 3. High input for cell 0 balancing
CB2	45	45	1. Secondary cell terminal 2 input 2. Low input for cell 2 balancing 3. High input for cell 1 balancing
CB3	46	46	1. Secondary cell terminal 3 input 2. Low input for cell 3 balancing 3. High input for cell 2 balancing
CB4	47	47	1. Secondary cell terminal 4 input 2. Low input for cell 4 balancing 3. High input for cell 3 balancing
CB5	48	48	1. Secondary cell terminal 5 input 2. Low input for cell 5 balancing 3. High input for cell 4 balancing
CB6	49	49	1. Secondary cell terminal 6 input 2. Low input for cell 6 balancing 3. High input for cell 5 balancing

Table 3. Pin description...*continued*

Symbol	Pin		Description
	BMA7126	BMA7124	
CB7	50	50	1. Secondary cell terminal 7 input 2. Low input for cell 7 balancing 3. High input for cell 6 balancing
n.c.	51	51	not connected
n.c.	52	52	not connected
n.c.	53	53	not connected
n.c.	54	54	not connected
CB8	55	55	1. Secondary cell terminal 8 input 2. Low input for cell 8 balancing 3. High input for cell 7 balancing
CB9	56	56	1. Secondary cell terminal 9 input 2. Low input for cell 9 balancing 3. High input for cell 8 balancing
CB10	57	57	1. Secondary cell terminal 10 input 2. Low input for cell 10 balancing 3. High input for cell 9 balancing
CB11	58	58	1. Secondary cell terminal 11 input 2. Low input for cell 11 balancing 3. High input for cell 10 balancing
CB12	59	59	1. Secondary cell terminal 12 input 2. Low input for cell 12 balancing 3. High input for cell 11 balancing
CB13	60	60	1. Secondary cell terminal 13 input 2. Low input for cell 13 balancing 3. High input for cell 12 balancing
CB14	61	61	1. Secondary cell terminal 14 input 2. Low input for cell 14 balancing 3. High input for cell 13 balancing
CB15	62	62	1. Secondary cell terminal 15 input 2. Low input for cell 15 balancing 3. High input for cell 14 balancing
CB16	63	63	1. Secondary cell terminal 16 input 2. Low input for cell 16 balancing 3. High input for cell 15 balancing
CB17	64	64	1. Secondary cell terminal 17 input 2. Low input for cell 17 balancing 3. High input for cell 16 balancing
CB18	65	65	1. Secondary cell terminal 18 input 2. High input for cell 17 balancing
n.c.	66	66	not connected

Table 3. Pin description...*continued*

Symbol	Pin		Description
	BMA7126	BMA7124	
CSN_RXTXLN	67	67	1. SPI chip select input from controller 2. TPL RX negative input from lower node 3. TPL TX negative output to lower node
RXTXLP	68	68	1. TPL RX positive input from lower node 2. TPL TX positive output to lower node if not used, keep floating
n.c.	69	69	not connected
COTI_RXTXHP	70	70	1. SPI target data input from controller 2. TPL RX positive input from upper node 3. TPL TX positive output to upper node if not used keep floating or connect a 60 Ω differential resistance to SCLK_RXTXHN to balance the current consumption
SCLK_RXTXHN	71	71	1. SPI clock input from controller 2. TPL RX negative input from upper node 3. TPL TX negative output to upper node if not used keep floating or connect a 60 Ω differential resistance to COTI_RXTXHP to balance the current consumption
n.c.	72	72	not connected
n.c.	73	73	not connected
n.c.	74	74	not connected
n.c.	75	75	not connected
VSSC	76	76	VDDC ground reference
CITO	77	77	SPI target data output to controller if not used, keep floating
n.c.	78	78	not connected
GPIO12	79	79	1. Analog input AIN12 for ratiometric measurement to VAUX 2. Analog input AIN12 for absolute measurement 3. General-purpose input 12 4. General-purpose output 12 if not used connect to VSSA
GPIO11	80	80	1. Analog input AIN11 for ratiometric measurement to VAUX 2. Analog input AIN11 for absolute measurement 3. General-purpose input 11 4. General-purpose output 11 if not used connect to VSSA
GPIO10	81	81	1. Analog input AIN10 for ratiometric measurement to VAUX 2. Analog input AIN10 for absolute measurement 3. General-purpose input 10 4. General-purpose output 10 if not used connect to VSSA

Table 3. Pin description...*continued*

Symbol	Pin		Description
	BMA7126	BMA7124	
GPIO9	82	82	1. Analog input AIN9 for ratiometric measurement to VAUX 2. Analog input AIN9 for absolute measurement 3. General-purpose input 9 4. General-purpose output 9 if not used connect to VSSA
GPIO8	83	83	1. Analog input AIN8 for ratiometric measurement to VAUX 2. Analog input AIN8 for absolute measurement 3. General-purpose input 8 4. General-purpose output 8 5. SPI controller CSN0 if not used connect to VSSA
GPIO7	84	84	1. Analog input AIN7 for ratiometric measurement to VAUX 2. Analog input AIN7 for absolute measurement 3. General-purpose input 7 4. General-purpose output 7 5. SPI CITO if not used connect to VSSA
n.c.	85	85	not connected
GPIO6	86	86	1. Analog input AIN6 for ratiometric measurement to VAUX 2. Analog input AIN6 for absolute measurement 3. General-purpose input 6 4. General-purpose output 6 5. I^2C-bus SDA 6. SPI COTI if not used connect to VSSA
GPIO5	87	87	1. Analog input AIN5 for ratiometric measurement to VAUX 2. Analog input AIN5 for absolute measurement 3. General-purpose input 5 4. General-purpose output 5 5. I^2C-bus SCL 6. SPI SCLK if not used connect to VSSA
GPIO4	88	88	1. Analog input AIN4 for ratiometric measurement to VAUX 2. Analog input AIN4 for absolute measurement 3. General-purpose input 4 4. General-purpose output 4 5. Alarm output if not used connect to VSSA
GPIO3	89	89	1. Analog input AIN3 for ratiometric measurement to VAUX 2. Analog input AIN3 for absolute measurement 3. General-purpose input 3 4. General-purpose output 3 if not used connect to VSSA

Table 3. Pin description...*continued*

Symbol	Pin		Description
	BMA7126	BMA7124	
GPIO2	90	90	1. Analog input AIN2 for ratiometric measurement to VAUX 2. Analog input AIN2 for absolute measurement 3. General-purpose input 2 4. General-purpose output 2 if not used connect to VSSA
GPIO1	91	91	1. Analog input AIN1 for ratiometric measurement to VAUX 2. Analog input AIN1 for absolute measurement 3. General-purpose input 1 4. General-purpose output 1 if not used connect to VSSA
GPIO0	92	92	1. Analog input AIN0 for ratiometric measurement to VAUX 2. Analog input AIN0 for absolute measurement 3. General-purpose input 0 4. General-purpose output 0 5. Strobe signal on each completion of a VC ADC sample if not used connect to VSSA
VSSD	93	93	digital ground
VDDC	94	94	external VDDC supply output
VSSA	95	95	analog ground
VPREHV	96	96	preregulated voltage from the internal buck converter
VAUX	97	97	supply output for external sensors
VDDA	98	98	internal analog supply
n.c.	99	99	not connected
n.c.	100	100	not connected
GNDFLAG	expad101	expad101	grounded exposed pad

5 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	pin VBAT and VBATSW	−0.3	-	+94	V
V_{LX}	voltage on pin LX		−2.0	-	V_{VBATSW} + 0.3	V

Table 4. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{I(CTn)}$	cell terminal input voltage	pin CTn; n = 16 to 18	−0.3	-	+94	V
		pin CTn; n = 6 to 15	−0.3	-	n × 6	V
		pin CTn; n = 1 to 5	−0.3	-	(n + 1) × 5	V
		pin CT0	−1	-	+5	V
		pin CTMn; n = 1 to 6	−1 − 6 × n	-	+0.3	V
		26 cell variants; pin CTMn; n = 7 and 8	−40	-	+0.3	V
$I_{I(CTn)}$	cell terminal input current	open load detection disabled	−1	-	+1	mA
$V_{I(CBn)}$	cell balancing input voltage	pin CBn; n = 16 to 18	−0.3	-	+94	V
		pin CBn; n = 6 to 15	−0.3	-	n × 6	V
		pin CBn; n = 1 to 5	−0.3	-	(n + 1) × 5	V
		pin CB0	−3	-	+5	V
		pin CBMn; n = 1 to 6	−3 − 6 × n	-	+0.3	V
		26 cell variants; pin CBMn; n = 7 and 8	−40	-	+0.3	V
$V_{dif(CTn)}$	cell terminal differential voltage	pin CTn to pin CT(n − 1); n = 1 to 18	−5	-	+10	V
		pin CTMn to pin CTM(n − 1); n = 1 to 6	−5	-	+10	V
		26 cell variants; pin CTMn to pin CTM(n − 1); n = 7 and 8	−5	-	+10	V
$V_{dif(CBn)}$	cell balancing differential voltage	pin CBn to pin CB(n − 1); n = 1 to 18	−0.3	-	+12.5	V
		pin CBMn to pin CBM(n − 1); n = 1 to 6	−0.3	-	+12.5	V
		26 cell variants; pin CBMn to pin CBM(n − 1); n = 7 and 8	−0.3	-	+12.5	V
$I_{I(bal)}$	input current on balancing pins	T_j = −40 °C to +135 °C	−33	-	+330	mA
V_{VPREHV}	voltage on pin VPREHV		−0.3	-	+9.9	V
V_{VDDA}	voltage on pin VDDA		−0.3	-	+1.65	V
V_{VDDC}	voltage on pin VDDC		−0.3	-	+5.5	V
V_{VAUX}	voltage on pin VAUX		−0.3	-	+5.5	V
V_{GPIOn}	voltage on GPIO pins		−0.3	-	V_{VDDC} + 0.5	V
V_{CITO}	voltage on pin CITO		−0.3	-	V_{VDDC} + 0.5	V

Table 4. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{bus(TPL)}$	voltage on TPL communication bus pins	pin CSN_RXTXLN, RXTXLP, COTI_RXTXHP, and SCLK_RXTXHN; relative to pin VSSC	−20	-	+20	V

6 Package outline

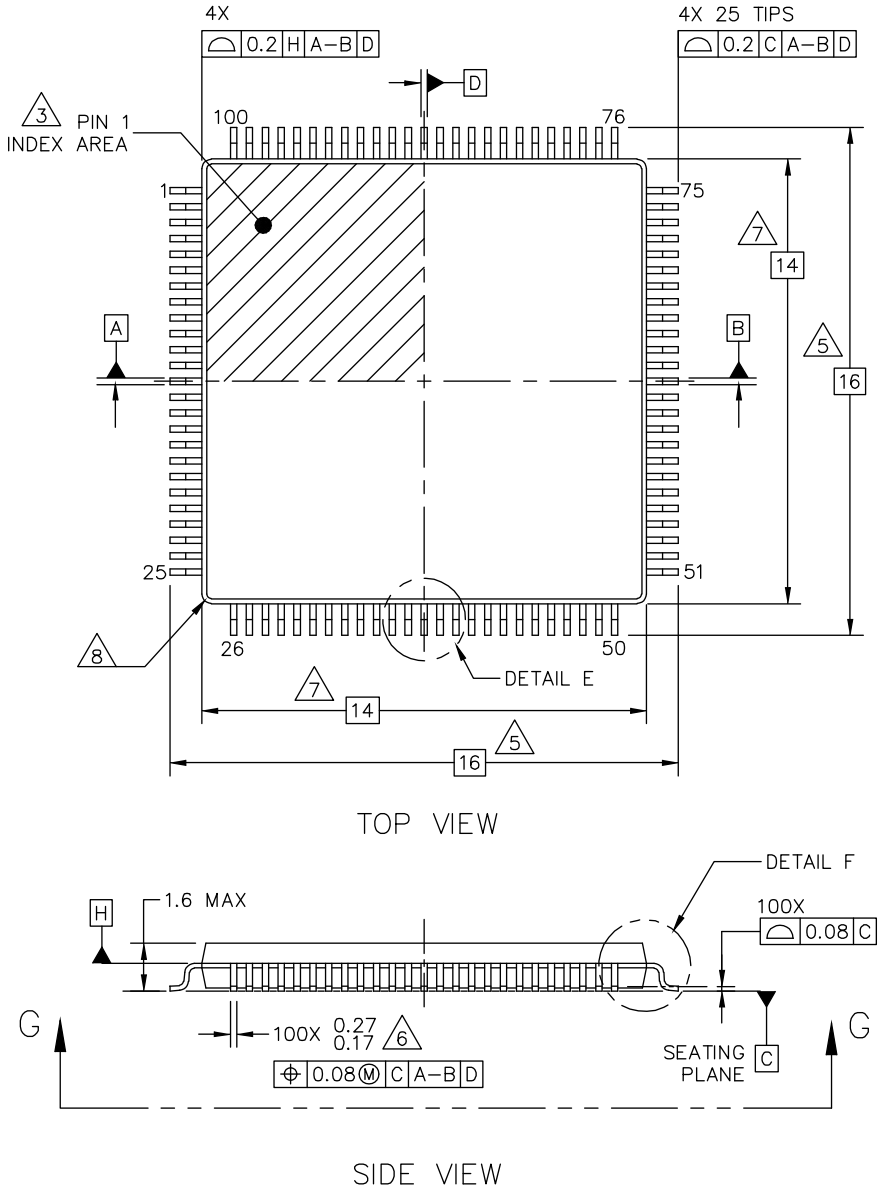


Figure 5. Package outline

6.1 Package mechanical dimensions

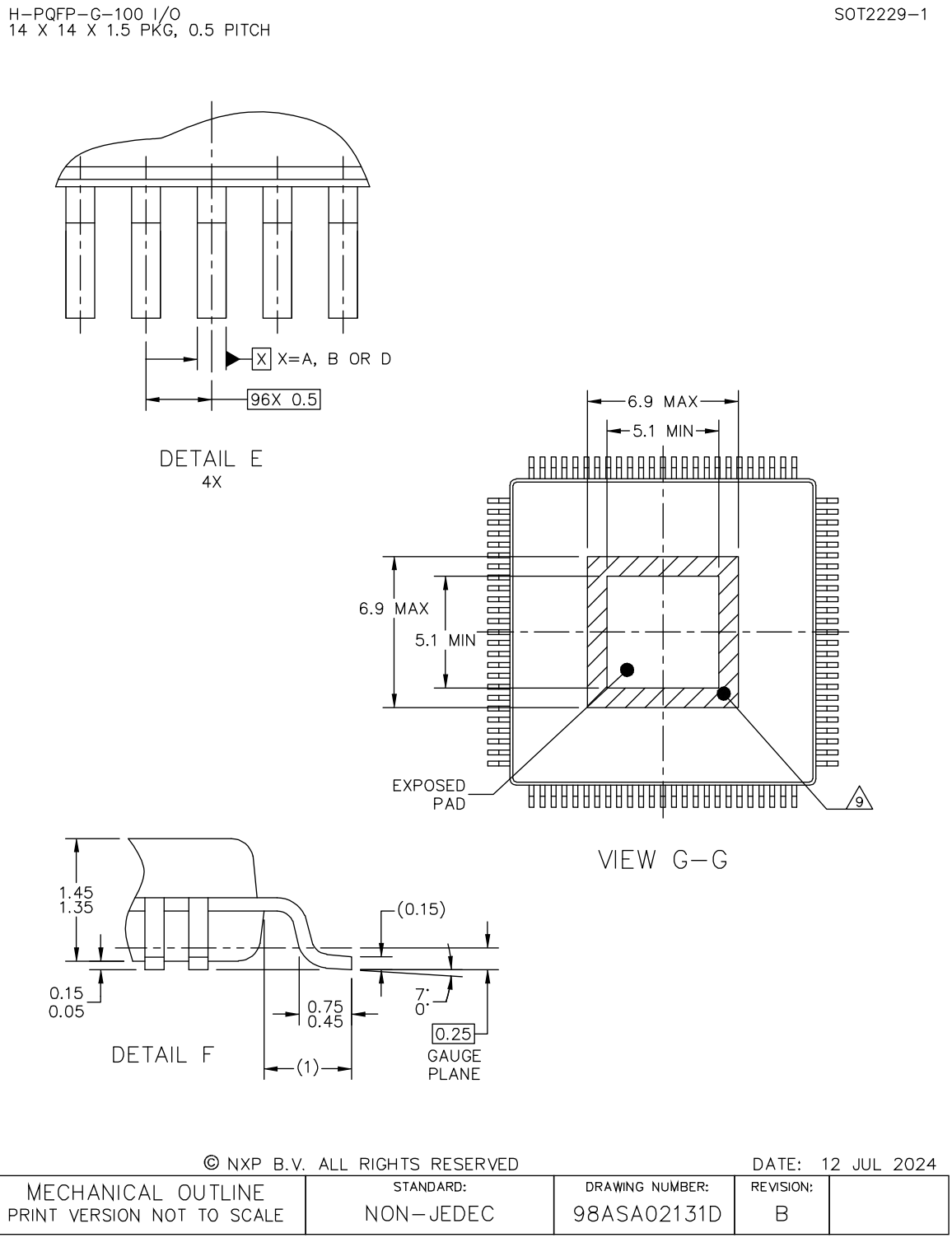
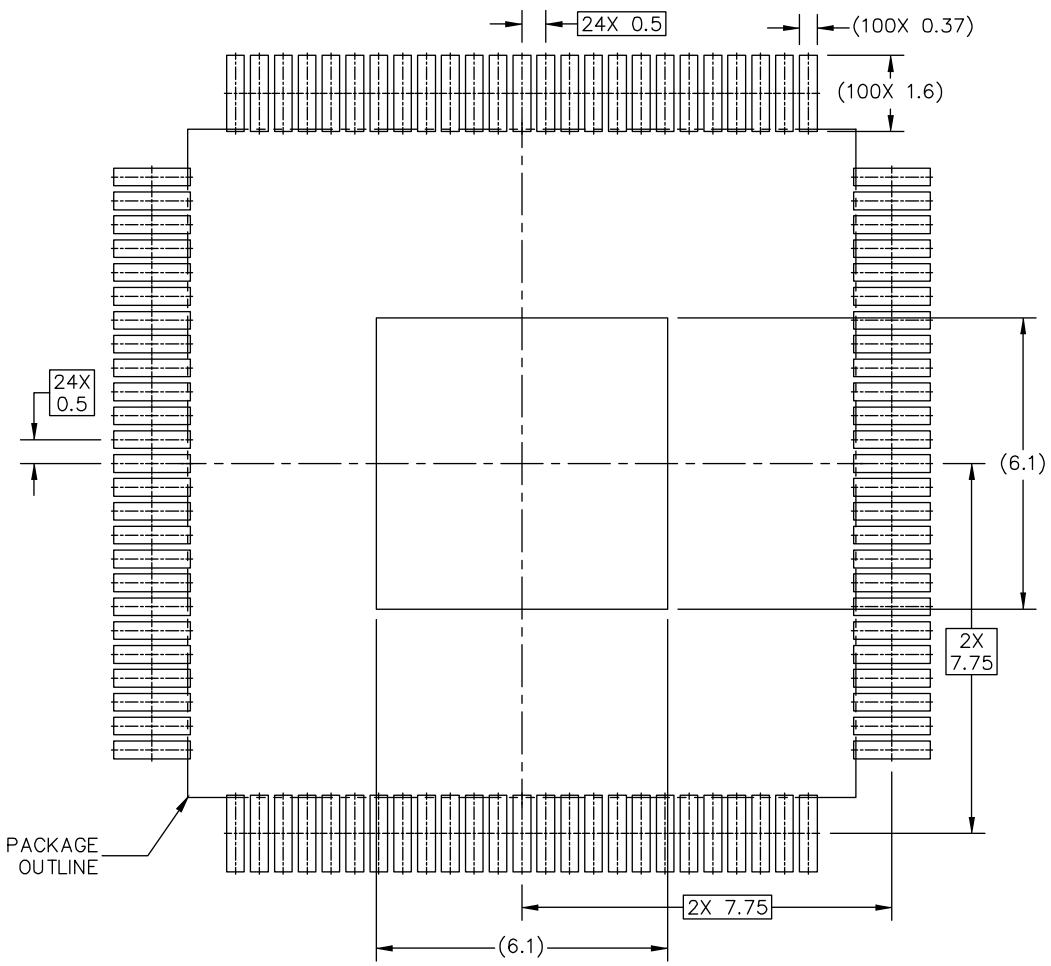


Figure 6. Package mechanical dimensions 1



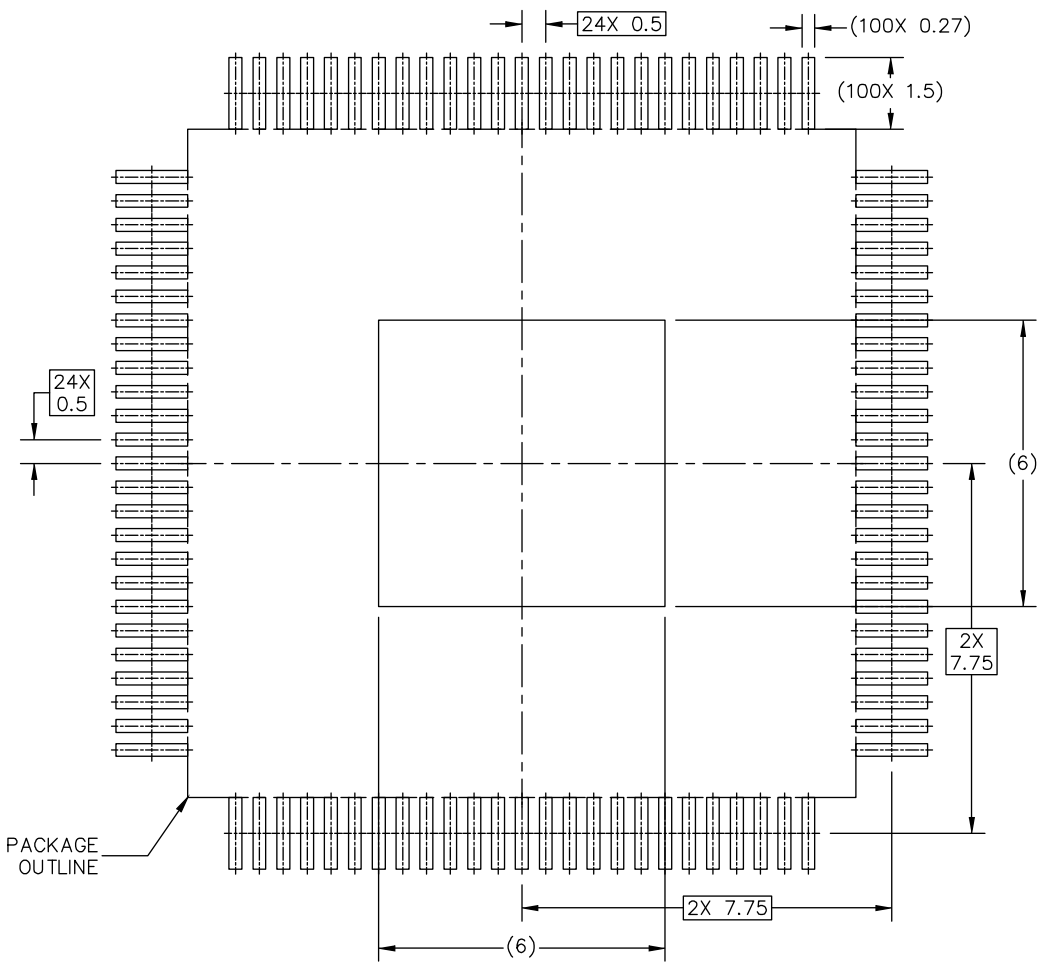
PCB DESIGN GUIDELINES − SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 12 JUL 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON−JEDEC	DRAWING NUMBER: 98ASA02131D	REVISION: B	

Figure 7. Package mechanical dimensions 2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 12 JUL 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA02131D	REVISION: B	

Figure 8. Package mechanical dimensions 3

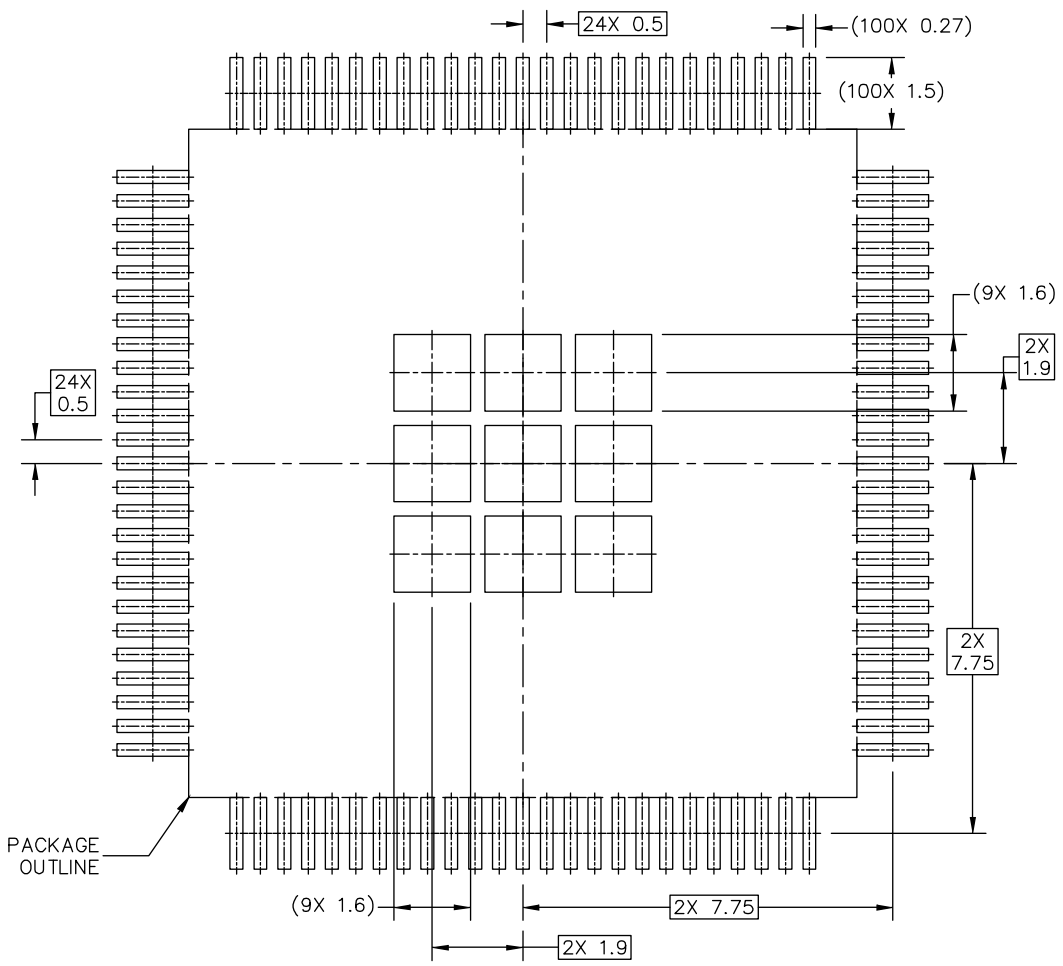


Figure 9. Package mechanical dimensions 4

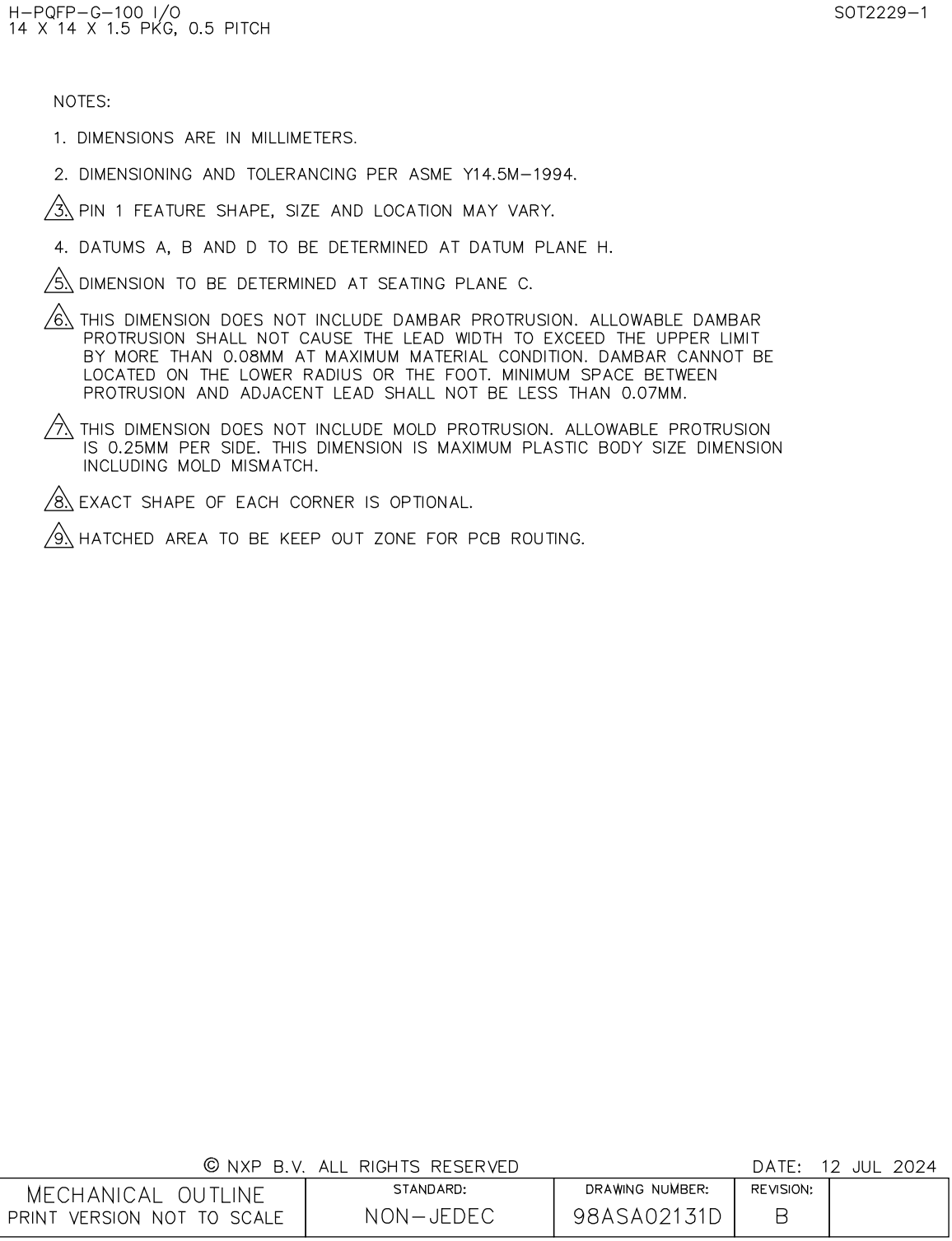


Figure 10. Package mechanical dimensions 5

7 Revision history

Table 5. Revision history

Document ID	Release date	Description
BMA7124XB_BMA7126XB_SDS v.1.0	31 August 2026	initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents