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NXP Semiconductors
MOSFET N-channel enhancement switching transistor  

**DESCRIPTION**
Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type. The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

**APPLICATIONS**
- analog and/or digital switch
- switch driver

**PINNING**

1 = substrate (b)  
2 = source  
3 = drain  
4 = gate

**Note**
1. Drain and source are interchangeable.

**QUICK REFERENCE DATA**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>Drain-source voltage</td>
<td>$V_{DS}$</td>
<td>max. 10 V</td>
</tr>
<tr>
<td>Source-drain voltage</td>
<td>$V_{SD}$</td>
<td>max. 10 V</td>
</tr>
<tr>
<td>Drain-substrate voltage</td>
<td>$V_{DB}$</td>
<td>max. 15 V</td>
</tr>
<tr>
<td>Source-substrate voltage</td>
<td>$V_{SB}$</td>
<td>max. 15 V</td>
</tr>
<tr>
<td>Drain current (DC)</td>
<td>$I_D$</td>
<td>max. 50 mA</td>
</tr>
<tr>
<td>Total power dissipation up to $T_{amb} = 25 , ^{\circ}C$</td>
<td>$P_{tot}$</td>
<td>max. 230 mW</td>
</tr>
<tr>
<td>Gate-source threshold voltage</td>
<td>$V_{DS} = V_{GS}; V_{SB} = 0; \quad I_D = 1 , \mu A$</td>
<td>$V_{GS(th)}$</td>
</tr>
<tr>
<td>Drain-source ON-resistance</td>
<td>$V_{GS} = 10 , V; V_{SB} = 0; \quad I_D = 0.1 , mA$</td>
<td>$R_{DSon}$</td>
</tr>
<tr>
<td>Feed-back capacitance</td>
<td>$V_{GS} = V_{BS} = -15 , V; \quad V_{DS} = 10 , V; f = 1 , MHz$</td>
<td>$C_{rss}$</td>
</tr>
</tbody>
</table>

Marking code: 
BSS83 = % M9

![Simplified outline and symbol](image)
### RATINGS
Limiting values in accordance with the Absolute Maximum System (IEC 134)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Maximum</th>
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<tr>
<td>Drain-source voltage</td>
<td>$V_{DS}$</td>
<td>10 V</td>
</tr>
<tr>
<td>Source-drain voltage</td>
<td>$V_{SD}$</td>
<td>10 V</td>
</tr>
<tr>
<td>Drain-substrate voltage</td>
<td>$V_{DB}$</td>
<td>15 V</td>
</tr>
<tr>
<td>Source-substrate voltage</td>
<td>$V_{SB}$</td>
<td>15 V</td>
</tr>
<tr>
<td>Drain current (DC)</td>
<td>$I_D$</td>
<td>50 mA</td>
</tr>
<tr>
<td>Total power dissipation up to $T_{amb} = 25 , ^\circ C$</td>
<td>$P_{tot}$</td>
<td>230 mW</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>$T_{stg}$</td>
<td>-65 to 150 °C</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>$T_J$</td>
<td>125 °C</td>
</tr>
</tbody>
</table>

### THERMAL RESISTANCE
From junction to ambient in free air

$$R_{th \, j-a} = 430 \, K/W$$
CHARACTERISTICS

$T_{\text{amb}} = 25 \, ^\circ \text{C}$ unless otherwise specified

Drain-source breakdown voltage

$V_{\text{GS}} = V_{\text{BS}} = -5 \, \text{V}; I_D = 10 \, \text{nA}$

Source-drain breakdown voltage

$V_{\text{GD}} = V_{\text{BD}} = -5 \, \text{V}; I_D = 10 \, \text{nA}$

Drain-substrate breakdown voltage

$V_{\text{GB}} = 0; I_D = 10 \, \text{nA}; \text{open source}$

Source-substrate breakdown voltage

$V_{\text{GB}} = 0; I_D = 10 \, \text{nA}; \text{open drain}$

Drain-source leakage current

$V_{\text{GS}} = V_{\text{BS}} = -2 \, \text{V}; V_{\text{DS}} = 6,6 \, \text{V}$

Source-drain leakage current

$V_{\text{GD}} = V_{\text{BD}} = -2 \, \text{V}; V_{\text{SD}} = 6,6 \, \text{V}$

Forward transconductance at $f = 1 \, \text{kHz}$

$V_{\text{DS}} = 10 \, \text{V}; V_{\text{SB}} = 0; I_D = 20 \, \text{mA}$

Gate-source threshold voltage

$V_{\text{DS}} = V_{\text{GS}}; V_{\text{SB}} = 0; I_D = 1 \, \mu\text{A}$

Drain-source ON-resistance

$I_D = 0,1 \, \text{mA};$

$V_{\text{GS}} = 5 \, \text{V}; V_{\text{SB}} = 0$

$V_{\text{GS}} = 10 \, \text{V}; V_{\text{SB}} = 0$

$V_{\text{GS}} = 3,2 \, \text{V}; V_{\text{SB}} = 6,8 \, \text{V}$ (see Fig.4)

Gate-substrate zener voltages

$V_{\text{DB}} = V_{\text{SB}} = 0; -I_G = 10 \, \mu\text{A}$

$V_{\text{DB}} = V_{\text{SB}} = 0; +I_G = 10 \, \mu\text{A}$

Capacitances at $f = 1 \, \text{MHz}$

$V_{\text{GS}} = V_{\text{BS}} = -15 \, \text{V}; V_{\text{DS}} = 10 \, \text{V}$

Feed-back capacitance

Input capacitance

Output capacitance

Switching times (see Fig.2)

$V_{\text{DD}} = 10 \, \text{V}; V_i = 5 \, \text{V}$

Note

1. Device mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.
**MOSFET N-channel enhancement switching transistor**

**BSS83**

**Pulse generator:**

\[ R_i = 50 \ \Omega \]

\[ t_r < 0.5 \ \text{ns} \]

\[ t_f < 1.0 \ \text{ns} \]

\[ t_p = 20 \ \text{ns} \]

\[ \delta < 0.01 \]

---

**Fig.2** Switching times test circuit and input and output waveforms.

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**Fig.3** \( V_{SB} = 0 \); typical values.

\( T_j = 25 \ ^\circ \text{C} \).

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**Fig.4** \( V_{SB} = 6.8 \ \text{V} \); typical values.

\( T_j = 25 \ ^\circ \text{C} \).
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**Fig. 5** $V_{DS} = 10 \text{ V}; V_{BS} = 0$; typical values.  

$T_j = 25 ^\circ \text{C}$.  

**Fig. 6** $V_{DS} = V_{GS} = V_{GS(th)}$.  

$T_j = 25 ^\circ \text{C}$.  

**Fig. 7** $V_{SB} = 0$; typical values.  

$T_j = 25 ^\circ \text{C}$.  

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MOSFET N-channel enhancement switching transistor

PACKAGE OUTLINE
Plastic surface mounted package; 4 leads

SOT143B

DIMENSIONS (mm are the original dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A</th>
<th>A1 max</th>
<th>b1</th>
<th>c</th>
<th>D</th>
<th>E</th>
<th>e</th>
<th>e1</th>
<th>H_E</th>
<th>L_P</th>
<th>Q</th>
<th>v</th>
<th>w</th>
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<tr>
<td>mm</td>
<td>1.1</td>
<td>0.9</td>
<td>0.48</td>
<td>0.88</td>
<td>0.15</td>
<td>3.0</td>
<td>2.8</td>
<td>1.4</td>
<td>1.9</td>
<td>2.5</td>
<td>0.45</td>
<td>0.55</td>
<td>0.2</td>
<td>0.1</td>
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OUTLINE VERSION

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Legal information

Data sheet status

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<td>This document contains data from the objective specification for product development.</td>
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<tr>
<td>Preliminary [short] data sheet</td>
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<tr>
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<td>Production</td>
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[2] The term ‘short data sheet’ is explained in section “Definitions”.
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