CLRC663

High performance multi-protocol NFC frontend CLRC663 and CLRC663 *plus*

Rev. 5.4 — 10 June 2026 Product short data sheet

1 General description

CLRC663, the high-performance multi-protocol NFC frontend.

The CLRC663 multi-protocol NFC frontend IC supports the following operating modes:

- Read/write mode supporting ISO/IEC 14443 type A and MIFARE Classic communication mode
- Read/write mode supporting ISO/IEC 14443B
- Read/write mode supporting JIS X 6319-4 (comparable with FeliCa)[1]
- Passive initiator mode according to ISO/IEC 18092
- Read/write mode supporting ISO/IEC 15693
- Read/write mode supporting ICODE EPC UID/ EPC OTP
- Read/write mode supporting ISO/IEC 18000-3 mode 3/ EPC Class-1 HF

The CLRC663's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A and MIFARE Classic IC-based cards and transponders without additional active circuitry. The digital module manages the complete ISO/IEC 14443A framing and error detection functionality (parity and CRC).

The CLRC663 supports MIFARE Classic with 1 kB memory, MIFARE Classic with 4 kB memory, MIFARE Ultralight, MIFARE Ultralight C, MIFARE Plus and MIFARE DESFire products. The CLRC663 supports higher transfer speeds of the MIFARE product family up to 848 kbit/s in both directions.

The CLRC663 supports layer 2 and 3 of the ISO/IEC 14443B reader/writer communication scheme except anticollision. The anticollision needs to be implemented in the firmware of the host controller as well as in the upper layers.

The CLRC663 is able to demodulate and decode FeliCa coded signals. The FeliCa receiver part provides the demodulation and decoding circuitry for FeliCa coded signals. The CLRC663 handles the FeliCa framing and error detection such as CRC. The CLRC663 supports FeliCa higher transfer speeds of up to 424 kbit/s in both directions.

The CLRC663 is supporting the P2P passive initiator mode in accordance with ISO/IEC 18092.

The CLRC663 supports the vicinity protocol according to ISO/IEC15693, EPC UID, and ISO/IEC 18000-3 mode 3/ EPC Class-1 HF.

The following host interfaces are supported:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS-232 with voltage levels dependent on pin voltage supply)
- I^2C-bus interface (two versions are implemented: I^2C and I^2CL)

1 In the following, the word FeliCa is used for JIS X 6319-4

The CLRC663 supports the connection of a secure access module (SAM). A dedicated separate I2C interface is implemented for a connection of the SAM. The SAM can be used for high secure key storage and acts as a very performant crypto-coprocessor. A dedicated SAM is available for connection to the CLRC663.

In this document, the term „MIFARE Classic card“ refers to a MIFARE Classic IC-based contactless card.

Note: *The replacement of "master/slave" with "controller/target" in this document follows the recommendation of the NXP, I^2C, and JEDEC SPI standards organizations.*

2 Features and benefits

- Includes NXP ISO/IEC14443-A and Innovatron ISO/IEC14443-B intellectual property licensing rights
- High-performance multi-protocol NFC frontend for transfer speed up to 848 kbit/s
- Supports ISO/IEC 14443 type A, MIFARE Classic, ISO/IEC 14443 B, and FeliCa reader modes
- P2P passive initiator mode in accordance with ISO/IEC 18092
- Supports ISO/IEC15693, ICODE EPC UID, and ISO/IEC 18000-3 mode 3/ EPC Class-1 HF
- Supports MIFARE Classic product encryption by hardware in read/write mode
  Allows reading cards based on MIFARE Ultralight, MIFARE Classic with 1 kB memory, MIFARE Classic with 4 kB memory, MIFARE DESFire EV1, MIFARE DESFire EV2, and MIFARE Plus ICs
- Low-Power Card Detection
- Compliance to the EMV contactless protocol specification on the RF level can be achieved
- Supported host interfaces:
  - SPI up to 10 Mbit/s
  - I^2C-bus interfaces up to 400 kBd in Fast mode, up to 1000 kBd in Fast-mode Plus
  - RS-232 Serial UART up to 1228.8 kBd, with voltage levels dependent on pin voltage supply
- Separate I^2C-bus interface for connection of a secure access module (SAM)
- FIFO buffer with size of 512 bytes for highest transaction performance
- Flexible and efficient power-saving modes including hard power down, standby, and low-power card detection
- Cost saving by integrated PLL to derive system clock from 27.12 MHz RF quartz crystal
- 3.0 V to 5.5 V power supply (CLRC66301, CLRC66302)
  2.5 V to 5.5 V power supply (CLRC66303)
- Up to 8 free programmable input/output pins
- Typical operating distance in read/write mode for communication to a ISO/IEC 14443 type A and MIFARE Classic card up to 12 cm, depending on the antenna size and tuning
- Two package options are available for the CLRC66303:
  1. HVQFN32: Package with wettable flanks easing the soldering process and quality control of soldered parts
  2. VFBGA36: Smallest package with optimized pin configuration for simple PCB layout
- The version CLRC66303 offers a more flexible configuration for Low-Power Card detection compared to the CLRC66301 and CLRC66302 with the new register LPCD_OPTIONS. In addition, the CLRC66303 offers new additional settings for the Load Protocol, which fit very well to smaller antennas. The CLRC66303 is therefore the recommended version for new designs.

3 Applications

- Industrial
- Access control
- Gaming

4 Quick reference data

Table 1. Quick reference data CLRC66301 and CLRC66302

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3.0	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		[1]	3.0	5.0	V_{DD}	V
$V_{DD(TVDD)}$	TVDD supply voltage			3.0	5.0	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH	[2]	-	8	40	nA
I_{DD}	supply current			-	17	20	mA
$I_{DD(TVDD)}$	TVDD supply current			-	100	250	mA
T_{amb}	operating ambient temperature			-25	+25	+85	°C
T_{stg}	storage temperature	no supply voltage applied		-55	+25	+125	°C

[1] VDD(PVDD) must always be the same or lower voltage than VDD.
[2] I_{pd} is the sum of all supply currents

Table 2. Quick reference data CLRC66303

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			2.5	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		[1]	2.5	5.0	V_{DD}	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	5.0	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH	[2]	-	8	40	nA
I_{DD}	supply current			-	17	20	mA
$I_{DD(TVDD)}$	TVDD supply current	recommended operation		-	180	350	mA
		absolute limiting value		-	-	500	mA
T_{amb}	operating ambient temperature	device mounted on PCB which allows sufficient heat dissipation for the actual power dissipation of the device		-40	+25	+105	°C
T_{stg}	storage temperature	no supply voltage applied		-55	+25	+125	°C

[1] VDD(PVDD) must always be the same or lower voltage than VDD.
[2] I_{pd} is the sum of all supply currents

5 Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
CLRC66301HN,551 [1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL2	SOT617-1
CLRC66301HN, 557[2]		plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL2	
CLRC66302HN,157[2]		plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL1	
CLRC66302HN,151[1]		Plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL1	
CLRC66302HN,118[3]		plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL1,	
CLRC66303HNE[1]		plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL2, wettable flanks	
CLRC66303HNY[3]		plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL2, wettable flanks	
CLRC66303HNK[2]		plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm, MSL2, wettable flanks	
CLRC66303A0EV[4]	VFBGA36	very thin fine-pitch ball grid array package; 36 terminals, 0.5 mm pitch, 3.5 mm x 3.5 mm x 0.8 mm body, MSL3	SOT1985-1

[1] Delivered in one tray, minimum order quantity (MOQ): 490 pcs
[2] Delivered in five trays; MOQ: 5 x 490 pcs
[3] Delivered on reel with 6000 pieces; MOQ: 6000 pcs
[4] Delivered on reel with 5000 pieces; MOQ: 5000 pcs

6 Block diagram

The analog interface handles the modulation and demodulation of the antenna signals for the contactless interface.

The contactless UART manages the protocol dependency of the contactless interface settings managed by the host.

The FIFO buffer ensures fast and convenient data transfer between host and the contactless UART.

The register bank contains the settings for the analog and digital functionality.

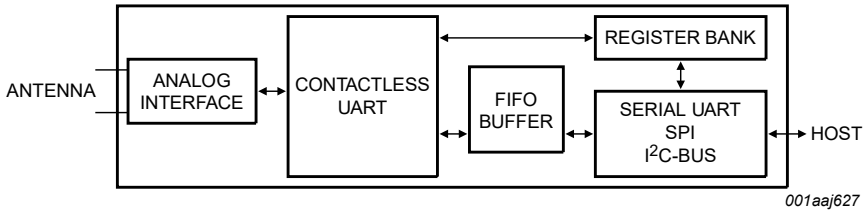

Figure 1. Simplified block diagram of the CLRC663

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.0	V
$V_{DD(PVDD)}$	PVDD supply voltage			-0.5	+6.0	V
$V_{DD(TVDD)}$	TVDD supply voltage			-0.5	+6.0	V
$I_{DD(TVDD)}$	TVDD supply current	CLRC66301, CLRC66302		-	250	mA
		CLRC66303		-	500	mA
$V_{i(RXP)}$	input voltage on pin RXP			-0.5	+2.0	V
$V_{i(RXN)}$	input voltage on pin RXN			-0.5	+2.0	V
P_{tot}	total power dissipation	per package		-	1125	mW
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1] ; 1500 Ω, 100 pF		-2000	2000	V
		charge device model (CDM)[2]		-500	500	V
$T_{j(max)}$	maximum junction temperature			-	+150	°C
T_{stg}	storage temperature	no supply voltage applied		-55	+150	°C

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002.

8 Revision history

Table 5. Revision history

Document ID	Release date	Description
CLRC663_SDS v.5.4	10 June 2026	Released alongside data sheet update.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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