



GD3162

Advanced IGBT/SiC gate driver with dynamic gate strength adjust

Rev. 1 — 29 November 2022

Objective short data sheet

1 General description

The GD3162 is an advanced, galvanically isolated, single-channel gate driver designed to drive the latest SiC and IGBT modules for xEV traction inverters. The device does this while enabling space savings and performance improvements through advanced gate-drive functionality.

The GD3162 offers integrated galvanic isolation, a programmable interface via SPI, and advanced programmable protection features, such as overtemperature, desaturation, and current sense protection. GD3162 with integrated boost capability, can drive most SiC MOSFET and IGBT/SiC module gates directly and is able to shape the gate drive capability in order to improve the power device's switching performance and reduce voltage stress.

The control of the gate strength can be done using either SPI commands or the GS Enable Pins. GS_ENH logic controls the drive strength of the turn on, and GS_ENL controls the drive strength of the turn off. To further improve performance, these functions are designed to operate independent of each other. Three separate pullup drive strengths and three pulldown drive strengths are made available via trilevel functions on the input pins or commands in SPI.

The GD3162 autonomously manages faults and reports power device and gate driver status via the INTB pin. VCE/VDS monitoring, as well as VGE monitoring, can be selected to be output on the INTA/RTRPT pin.

The GD3162 includes self-test and control protection functions for design of high functional safety integrity level systems (ASIL C/D) and meets the stringent requirements of automotive applications, being fully AEC-Q100 grade 1 qualified.

2 Features and benefits

This section summarizes the key features, safety features, and regulatory approvals for the GD3162.

2.1 Key features

- Integrated galvanic signal isolation (up to 8 kV)
- Integrated boost capability for increased drive strength: Up to 10 A/ 20 A/ 30 A source/sink current available by gate strength selection
- SPI or 3-state enabled GS_ENH and GS_ENL low-voltage domain pins to dynamically control gate drive strength. Adjustment of gate strength up to 20 KHz supported
- Dual gate pullup pins and dual gate pulldown pins for enhanced drive capability, synchronous adjustment of gate strength, reduced thermal loading during weak drive, and independent verification of each drive state operation
- SPI programmable ISEN/COMP setpoint, to allow the gate driver to automatically control gate drive strength based on high-voltage domain inputs.



- Temperature sense pins compatible with NTC and PTC thermistors allow for local control of temperature based gate-drive strength, as well as power device temperature monitoring via AOUP pin or SPI.
- Programmable ADC delay – Up to 8 μ s sampling delay from rising or falling edge of PWM.
- Active Bus Discharge Functionality (PGD3162AM551EK and PGD3162AM581EK only)
 - Provides either MCU controlled or Safety Logic Controlled Gate drive to actively discharge the DC Link Capacitor.
- SPI interface for safety monitoring, configuration, and diagnostic reporting
- VCE power device monitoring via the low-voltage domain INTA/RTRPT pin
- Supports high PWM switching frequencies: PWM up to 100 kHz, thermally limited
- Fail-safe state management from LV and HV domain for user-selectable safe state
- Configurable desaturation and current sense optimized for protecting SiC and IGBTs against short circuit in less than 1 μ s
- INTA/RTRPT and INTB Interrupt pins for current and voltage Fault Reporting and, if selected, VCE or VGE real-time reporting.
- Advanced two-level turn-off (2LTO) in combination with soft shut down gate current to reduce current and voltage stress associated with rapid turnoff.
- CMTI > 100 V/ns

2.2 Safety features

- Certified compliant with ISO 26262, supporting ASIL D level functional safety
- Error checking of SPI and configuration data with 8-bit CRC
- Autonomously manages severe faults and reports status via configurable INTB and/or INTA/RTRPT pins, and SPI interface
- VCE/VGE real-time cycle-by-cycle monitoring and reporting for feedback of power device status.
- Built-in self-test (BIST) of all analog and digital circuits
- Continuous watchdog of communications across isolation barrier
- Deadtime enforcement
- Overvoltage and undervoltage supervision of 5 V bias supply for LV circuitry
- Overvoltage and undervoltage supervision of VCC supply for HV circuitry
- Dedicated fail-safe state management pins on both low-voltage and high-voltage sides

2.3 Safety and regulatory approvals

- Reinforced isolation per DIN V VDE V 0884-10
- Withstand 5000 V rms (1 minute) isolation per UL 1577
- AEC-Q100 grade 1 automotive qualified

3 Ordering information

Table 1. Orderable part variations

Part number ^[1]	VDD (V)	External clearance and creepage distance (mm)	Material (isolation) group	Temperature (T _J) (°C)	Package
PGD3162AM550EK (without DC Link Discharge Mode)	5.0	>7.72 ^[2]	II ^[3]	-40 to 150	32-pin wide body SOIC, 0.65 mm pitch
PGD3162AM551EK (with DC Link Discharge Mode)	5.0	>7.72 ^[2]	II ^[3]	-40 to 150	32-pin wide body SOIC, 0.65 mm pitch
PGD3162AM580EK (without DC Link Discharge Mode)	5.0	>8.00 ^[2]	I ^[3]	-40 to 150	32-pin wide body SOIC, 0.65 mm pitch
PGD3162AM581EK (with DC Link Discharge Mode)	5.0	>8.00 ^[2]	I ^[3]	-40 to 150	32-pin wide body SOIC, 0.65 mm pitch

[1] To order parts in tape and reel, add the R2 suffix to the part number.

[2] per IEC 60950-1 Tables 2K and 2N

[3] per IEC 60664-1

4 Block diagram

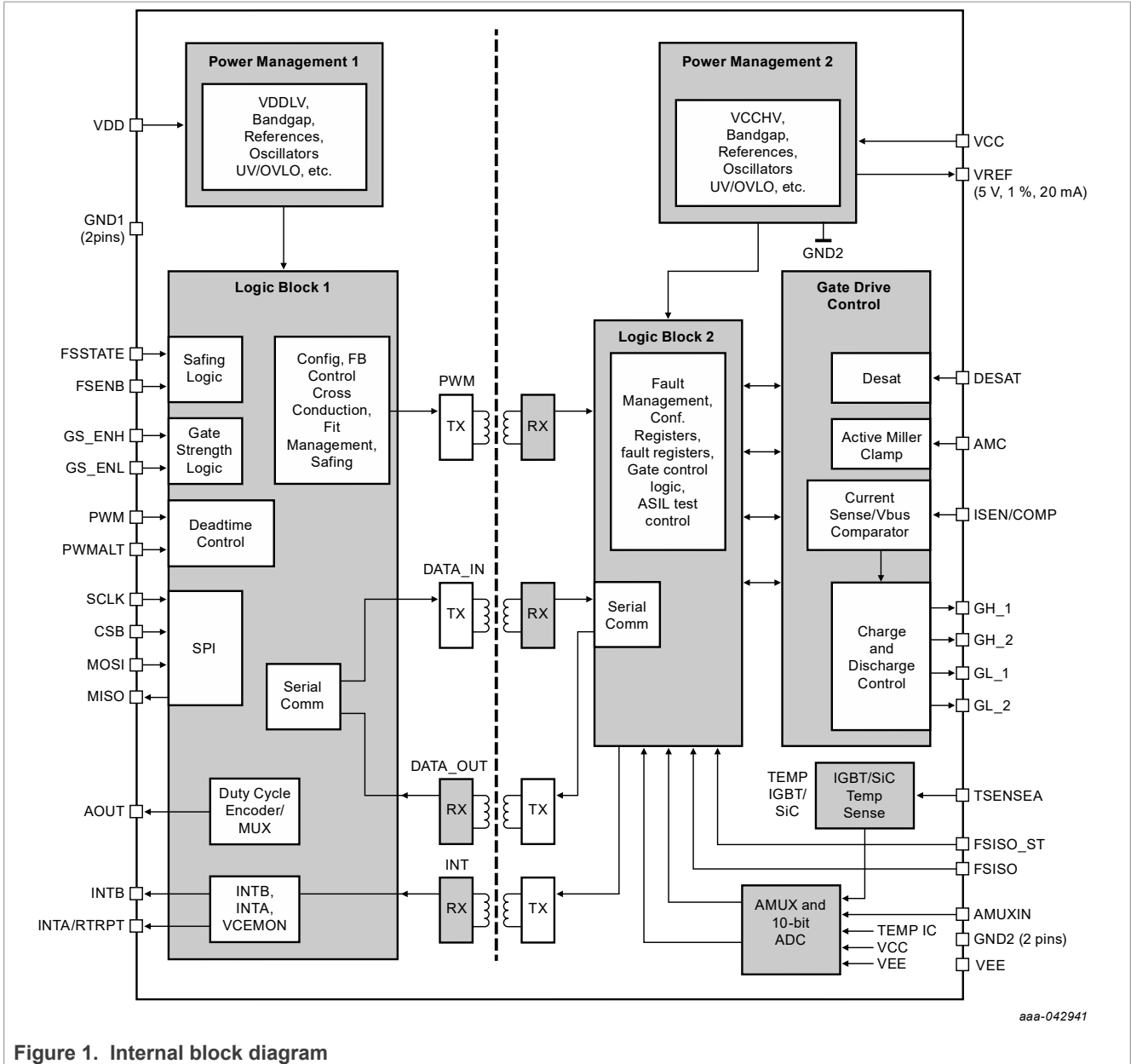


Figure 1. Internal block diagram

5 Limiting values

Table 2. Absolute maximum ratings

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). $T_J = -40$ to $+150$ °C, unless otherwise specified. Currents are positive into and negative out of the specified pins.

Symbol	Description (Rating)	Min	Max	Unit
Power supplies and current references				
V _{VDD}	Low-voltage domain logic supply voltage, 5.0 V	[1] -0.3	6.0	V
V _{VCC}	High-voltage domain positive supply voltage	[2] -0.3	25	V
V _{VEE}	High-voltage domain negative supply voltage	[2] -12	0.3	V
V _{VCC-VEE}	High-voltage domain positive/negative supply	-0.3	35	V
V _{VREF}	VREF voltage	[2] -0.3	6.0	V
I _{VREF}	VREF output current	—	-20	mA
Logic pins				
V _{IN}	Logic input pin voltage (FSSTATE, FSENB, PWM, PWMALT, GS_ENH, GS_ENL, SCLK, CSB, MOSI)	[1] -0.3	18	V
V _{OUT}	Logic output pin voltage (MISO, INTB, INTA/RTRPT, AOUT)	[1] -0.3	V _{VDD} + 0.3	V
V _{FSISO}	Logic input pin voltage (FSISO)	[2] -0.3	12	V
V _{FSISO_ST}	Logic input pin voltage (FSISO_ST)	[2] -0.3	12	V
Gate drive output stage				
V _{GH_1,2}	GH_1,2 voltage	[2] V _{VEE} - 0.3	V _{VCC} + 0.3	V
V _{GL_1,2}	GL_1,2 voltage	[2] V _{VEE} - 0.3	V _{VCC} + 0.3	V
V _{AMC}	AMC voltage	[2] V _{VEE} - 0.3	V _{VCC} + 0.3	V
I _{SOURCEMAX1}	GH_1 max. source current	[3] —	-14	A
I _{SOURCEMAX2}	GH_2 max. source current	[3] —	-5	A
I _{SINKMAX1}	GL_1, AMC max. sink current	[3] —	14	A
I _{SINKMAX2}	GL_2 max. sink current	[3] —	5	A
V _{DESAT}	DESAT voltage	[2] -0.3	V _{VCC} + 0.3	V
Temperature sense pin				
V _{TSENSEA}	TSENSEA voltage	[2] -0.3	6.0	V
Interrupt pins				
I _{INTA/RTRPT}	Open drain DC output current	[4] —	-20	mA
I _{INTB}	Open drain DC output current	[4] —	-20	mA
ISENSE sense pin				
V _{ISEN/COMP}	ISEN/COMP voltage	[2] -2.0	V _{VCC} + 0.3 V	V
AMUXIN pin				
V _{AMUXIN}	AMUXIN voltage	[2] -0.3	6.0	V
ESD ratings				
V _{ESDHBM}	ESD voltage (HBM) All pins	[5] -2.0	2.0	kV
V _{ESDCDM}	ESD voltage (CDM) Corner pins Other pins	[6] -750 -500	750 500	V

Table 2. Absolute maximum ratings...continued

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). $T_J = -40$ to $+150$ °C, unless otherwise specified. Currents are positive into and negative out of the specified pins.

Symbol	Description (Rating)	Min	Max	Unit
$V_{ESDModule}$	ESD voltage (module level) GND1, GND2 pins	-8.0	8.0	kV
IMMUNITY				
dV_{ISO}/dt	Common mode transient immunity	—	100	V/ns

[1] Ref = GND1

[2] Ref = GND2

[3] 50 %, 100 nF, 10 kHz

[4] $V_{INTB}, V_{INTA/RTTRPT} < 1.0$ V

[5] **Human Body Model (HBM) at device level**

ANSI/ESDA/JEDEC JS-001: 2010 Model HBM (human body model)

Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

Test points: pin to GND1 and pin to GND2

[6] **Charged Device Model (CDM)**

ANSI/ESD S5.3.1-2009

ESD Association Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level

[7] **Module Level ESD Tests**

ISO 10605:2008/Cor. 1:2010(E)

Road vehicles - Test methods for electrical disturbances from electrostatic discharge

[8] Pulse width = 10 ns

Revision history

Table 3. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
v.1.0	20221129	Objective	—	—
Modifications	—			

6 Legal information

6.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Tables

Tab. 1.	Orderable part variations	3	Tab. 3.	Revision history	7
Tab. 2.	Absolute maximum ratings	5			

Figures

Fig. 1.	Internal block diagram	4
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Contents

1	General description	1
2	Features and benefits	1
2.1	Key features	1
2.2	Safety features	2
2.3	Safety and regulatory approvals	2
3	Ordering information	3
4	Block diagram	4
5	Limiting values	5
6	Legal information	8

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