IMX952IEC

i.MX 952 Applications Processors Data Sheet for Industrial Products

Rev. 4.0 — 2 November 2026 Product data sheet

- For functional characteristics and the programming model, see i.*MX 952 Applications Processor Reference Manual* (IMX952RM).

1 Introduction

i.MX 952 applications processors offer advanced graphics and video cores, powerful vision and machine learning acceleration, efficient CPU performance plus real-time processing and advanced security with integrated EdgeLock® secure enclave to support energy-efficient edge computing.

i.MX 952 applications processors integrate up to four Arm Cortex®-A55 cores and are one of the i.MX devices to support functional safety with built-in Arm Cortex®-M33 and M7 which can be configured as a safety island. Optimizing performance and power efficiency for Industrial, IoT and automotive devices, i.MX 952 processors are built with NXP's innovative Energy Flex architecture.

i.MX 952 applications processors offer a rich set of peripherals targeting automotive, industrial and commercial IoT market segments. Part of the EdgeVerse™ portfolio of intelligent edge solutions, i.MX 952 family will be offered in commercial, industrial, extended industrial and automotive level qualification and backed by NXP's product longevity program.

Table 1. Feature summary

Subsystem	Features
Arm Cortex-A55 MPCore platform	• 4x Arm Cortex-A55, up to 1.7 GHz frequency • Arm v8.2 fully 64-bit capable • L1, L2, and L3 cache with ECC
Arm Cortex-M33 and Cortex-M7 platform	• 1x Arm Cortex-M33, up to 333 MHz frequency • 1x Cortex-M7, up to 800 MHz frequency • Arm v8-M supporting Trustzone-M • 16 KB + 16 KB / 32 KB + 32 KB cache (ECC) • 256 KB / 512 KB Tightly Coupled Memory (TCM) / on-chip SRAM (ECC)
Memory	• 19 x 19 mm package: one x32 LPDDR interface (with inline ECC), operating at up to 6000 MT/s in LPDDR5 mode or 4266 MT/s in LPDDR4X mode. • 15 x 15 mm package: one x32 LPDDR interface (with inline ECC), operating at up to 4266 MT/s in LPDDR5 mode or 4000 MT/s in LPDDR4X mode. • 3x uSDHC (SD3.0, SDIO3.0, eMMC5.1) • XSPI with IPED, including support for SPI NOR and SPI NAND memories • LPSPI and XSPI

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Table 1. Feature summary*...continued*

Subsystem	Features
Neural Processing Unit (NPU)	• 2 eTOP/s Neural Network performance, up to 1.0 GHz (overdrive mode) and 800 MHz (nominal mode) • 1 MByte of SRAM embedded within the NPU, but it is available for other SoC usage when not using for ML purposes.
Graphics	• Arm Mali-G310 Graphic Processing Unit (GPU) — 3D GPU supporting 64 GFLOPs FP32 — OpenGL® ES 3.2 — Vulkan® 1.3 — OpenCL 3.0
Video Processors	• 4Kp60 H.265 and H.264 decode, 4Kp30 H.264 encode • 1x JPEG Encoder • 1x JPEG Decoder
Display Controller (up to 3 simultaneous displays)	• 1x 350 MHz MIPI-DSI (1x 4 lanes) • 2x 1080p60 LVDS Tx (2x 4-lane or 1x 8-lane) • Local dimming (512 Zone) hardware accelerator • 2D accelerator • 16 kByte of SRAM, available for other SoC usage when not used for 2D blitter purposes
Camera and ISP	• MIPI-CSI DPHY driving up to 10 Gbps in total (1x 4-lane or 2x 2-lane, 2.5 Gbps/lane) • ISP up to 500 Mpixels/s (1x 4Kp60, 2x 4Kp30, 4x 1080p60, or 8x 1080p30) • Up to 8x cameras with MIPI virtual channels • Supports RGB-IR camera • 96 kByte of SRAM, but it is available for other SoC usage when not using for ISP purposes.
Audio	• 17-lane I2S TDM (32-bit at 768 kHz frequency) • 6x Synchronous Audio Interfaces (SAI) • 8-channel PDM Microphone Interface (MICFIL) • 2x Medium Quality Sound (MQS) output • 2x Asynchronous Sample Rate Converter (ASRC) • 1x Audmix
Connectivity	• 1x PCIe Gen 3.0 (1-lane) • 2x USB2.0 with PHY

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Table 1. Feature summary*...continued*

Subsystem	Features
	• 3x CAN-FD • 2x 32-pin FLEXIO interfaces (bus or serial I/O) • 8x LPI2C • 8x LPSPI • 2x I3C
Ethernet	• 2x 1 Gbps Ethernet controllers • 10M/100M/1G RGMII/RMII Ethernet port (MAC 0) • 10M/100M/1G SGMII/RGMII/RMII Ethernet port (MAC1), SGMII mux'd with PCIe • IEEE 1588 for sync; and EEE
Low Speed Communication Peripherals	• 8x UART
Timer and PWMs	• 2x Low Power Periodical Interrupt Timers (LPIT) — 4-channel — 4 external trigger sources — Generic 32-bit resolution timer — Periodical interrupt generation • 6x Timer/PWM modules (TPM) — Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128 — 16-bit counter, support free-running counter or modulo counter mode, counting up or down — Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode • 2x Low-Power Timers (LPTMR) • 6x WatchDog modules (WDOG) • 1x System Counter (SYS_CTR) • 2x Timestamp Timer (TSTMR) • 4x General Purpose Timer (GPT)
GPIO and Pin Multiplexing	• General-purpose input/output (GPIO) modules with interrupt capability • Input/Output Multiplexing Controller (IOMUXC) to provide centralized pad control
Analog	• FRO Clock Generator (FRO_TUNER) • 2x Temperature Sensor (TEMPSENSE) • 8-channel, 12-bit Analog-to-Digital Converter (SAR_ADC)

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Table 1. Feature summary...*continued*

Subsystem	Features
	• 1x Trigger Mux (TRGMUX) to configure the trigger inputs for various peripherals
Clocking	Centralized internal Clock Control Module (CCM), 24 MHz and 32 kHz oscillators internal clock gating for fine-grained power consumption saving (Low Power Clock Gating - LPCG)
Safety	• Integrated functional safety • ISO26262 ASIL-B and IEC61508 SIL2 compliance
Security	• Trusted Resource Domain Controller (TRDC) — Supports up to 16 resource domains • Arm TrustZone® (TZ) architecture • Secure and trusted access control • EdgeLock™ Secure Enclave • Additional high security enclave (EdgeLock PRIME) • Evolved on-die security with run-time attestation, silicon root of trust, trust provisioning, fine-grain key management augmented by extensive crypto services
System Debug	• Arm CoreSight® debug and trace architecture • Trace Port Interface Unit (TPIU) to support off-chip real-time trace • Support for 5-pin (JTAG) and SWD debug interfaces
Power management	• Supports PMIC integration to supply all power rails • Multiple power domains allow power gating of most digital and analog logic in low power mode • General Power Controller (GPC), several factors are involved in power management, not just a central controller
Package	• 15 x 15 mm, 0.5/0.54/0.56 mm pitch, FCBGA • 19 x 19 mm FCBGA, 0.7 mm pitch

1.1 Ordering Information

Table 2 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers.

Table 2. Orderable part numbers

Part Number	Feature Set	A-Cores Qty	Temp. Qual.	Package	A-Core GHz	Local Dimming
MIMX95294CVZMAB	9529 - Full featured / Vision	4	C Industrial	VZ 19x19 No Lid	M 1.7GHz	A - No
MIMX95294CVTMAB	9529 - Full featured / Vision	4	C Industrial	VT 15x15 No Lid	M 1.7GHz	A - No

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Table 2. Orderable part numbers...*continued*

MIMX95292CVZMAB	9529 - Full featured / Vision	2	C Industrial	VZ 19x19 No Lid	M 1.7GHz	A - No
MIMX95292CVTMAB	9529 - Full featured / Vision	2	C Industrial	VT 15x15 No Lid	M 1.7GHz	A - No
MIMX95254CVZMAB	9525 - HMI	4	C Industrial	VZ 19x19 No Lid	M 1.7GHz	A - No
MIMX95254CVTMAB	9525 - HMI	4	C Industrial	VT 15x15 No Lid	M 1.7GHz	A - No
MIMX95252CVTMAB	9525 - HMI	2	C Industrial	VT 15x15 No Lid	M 1.7GHz	A - No
MIMX95234CVZMAB	9523 - Compute	4	C Industrial	VZ 19x19 No Lid	M 1.7GHz	A - No
MIMX95234CVTMAB	9523 - Compute	4	C Industrial	VT 15x15 No Lid	M 1.7GHz	A - No

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page https://www.nxp.com/products/i.MX952 or contact an NXP representative for details.

Part Type	i.MX Family	Segment	A- Core Qty.	Temp. Qual.	Package	A- Core Freq	Special Config	Silicon Revision
P	IMX952	9	4	A	VZ	M	A	A

Segment	Short Description	A- Cores Qty	ISP	NPU	GPU	VPU	Display Interfaces	Safety Enab [2]	Temp. Qual.	Packages
9	Full Featured	4 / 2	✓	✓	✓	✓	✓		A/C/D/X	VT/VZ
8	Full Featured + Safety	4	✓	✓	✓	✓	✓	ASIL- B SIL2[1]	A/X	VT/VZ
5	HMI	4 / 2		✓	✓	✓	✓		A/C/D/X	VT/VZ
4	HMI + Safety	4		✓	✓	✓	✓	ASIL- B SIL2[1]	A/X	VT/VZ
3	Compute	4		✓					A/C/D/X	VT/VZ
2	Compute + Safety	4		✓				ASIL- B SIL2[1]	A/X	VT/VZ

FCBGA Package Type	
VT	15 x 15 mm, multi - pitch custom pattern with 0.56, 0.54, and 0.50 mm pitches, no lid
VZ	19 x 19 mm, 0.7mm pitch, no lid

Cortex - A55 CPU Frequency	
M	1.7 GHz

Silicon Revision	
A	Rev 1.0 (A0)
B	Rev 1.1 (A1)

Special Configuration	
A	Without local dimming,
B	With local dimming,

Part Type	
P	Sample
M	Mass Production
S	Special

Cortex - A Cores	
4	4 Cores
2	2 Cores

Temperature Qualification	
A	Automotive: - 40 °C T_a to 125 °C T_j
C	Industrial: - 40 °C T_a to 105 °C T_j
D	Commercial : 0°C T_a to 95 °C T_j
X	Extended Industrial: - 40 °C T_a to 125°C T_j

1. NXP compliant safety SW included: ASIL - B (additional fees may be required) for Auto qual; or SIL2 (for Ext Ind);
2. Non - compliant building blocks for SIL available on all non - Auto PNs

Figure 1. Part number nomenclature - i.MX 952

1.2 Part marking

Parts are marked as in the example shown in this figure.

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Figure 2. Part marking for FCBGA package

Legend:

- XIMX95XX is the first half of the part number
- XXXXXXXX is the second half of the part number (full part number is on one line for lidded packages)
- MMMMM is the mask number
- CCCCC is the country code
- AAWLYYWWZZ
  - AA is the assembly lot ID
  - WL is the wafer lot ID
  - YY is year
  - WW is work week
  - ZZ is an additional identifier

2 Block Diagram

Figure 3 shows the functional modules in the i.MX 952 processor system.

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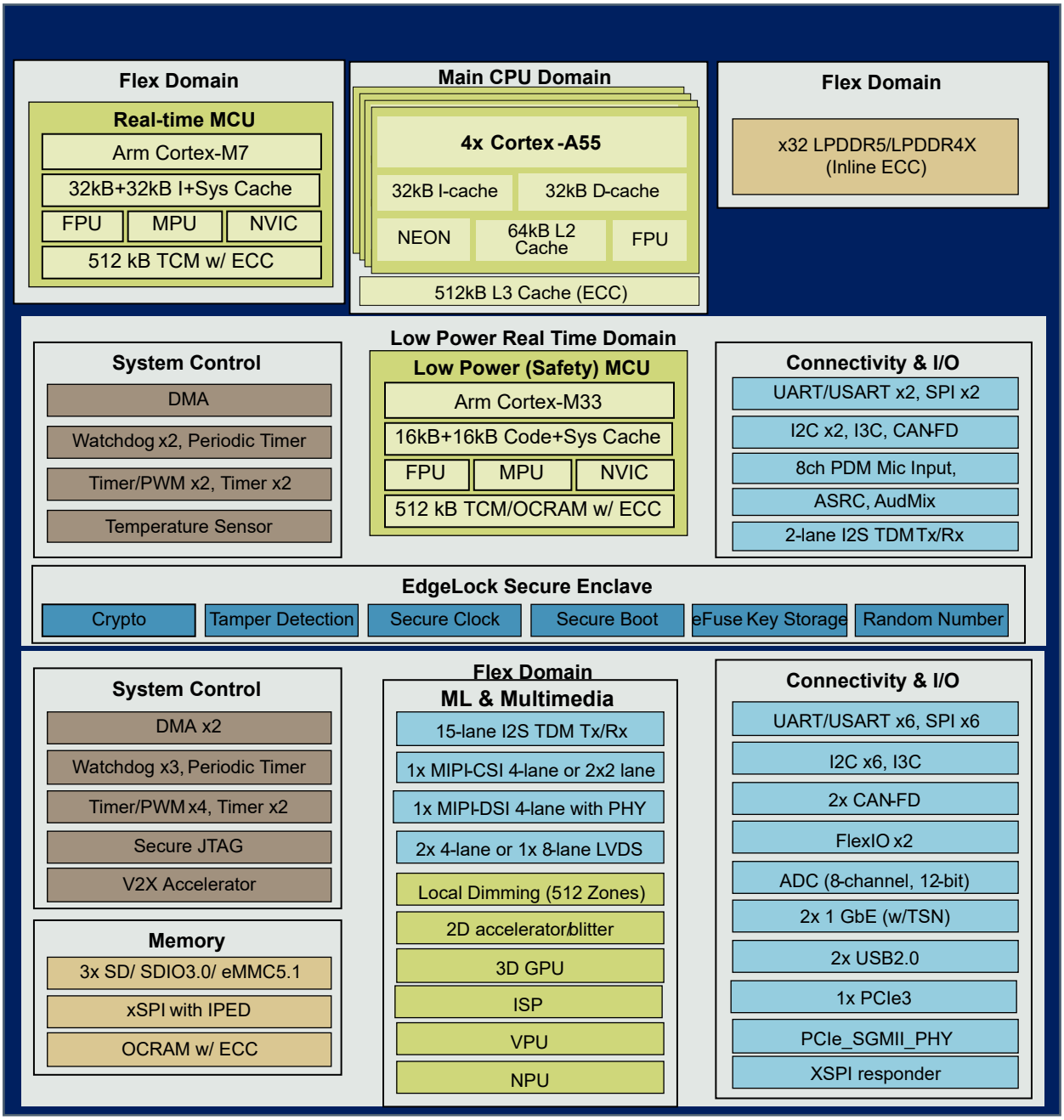


Figure 3. i.MX 952 system block diagram

Note: *Some modules shown in this block diagram are not offered on all derivatives.*

3 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 952 processors. The signal names are listed in alphabetical order.

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The package contact assignments can be found in Section, "Package information and contact assignments". Signal descriptions are provided in the i.MX 95 Reference Manual (IMX952RM).

Table 3. Special signal considerations

Signal Name	Remarks
CLKIN1/CLKIN2	CLKIN1 and CLKIN2 are input pins without internal pull-up and pull-down.
NC	These signals are No Connect (NC) and should be unconnected in the application.
ONOFF	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
POR_B	POR_B has no internal pull-up/down resistor, and requires external pull-up resistor to NVCC_BBSM. It is recommended that POR_B is properly handled during power up/down. Please refer to the Hardware Development Guide (HDG) for details.
RTC_XTALI/ RTC_XTALO	RTC_XTALI and RTC_XTALO can be coupled to an external crystal element to generate 32.768 k clock. Care must be taken to account parasitic capacitance of the pins in order to match the trimmed crystal assumptions for frequency accuracy. Care should also be taken to limit the parasitic leakage on or between RTC_XTALI and RTC_XTALO. This can debias the integrated amplifier resulting in reduced startup margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_ANA_1P8 level and the frequency shall be < 50 kHz under the typical condition.
XTALI_24M/ XTALO_24M	The system requires a 24 MHz clock to operate. A 24 MHz crystal can be created by coupling an appropriately tuned quartz element to XTALI and XTALO. Care must be taken that the resulting oscillation frequency complies with the utilized serial interface standards such as PCIe and USB.

3.1 Unused input and output guidance

If a function of the i.MX 952 is not used, terminated the I/Os and power rails of that function to reduce overall board power consumption.

Table 4. Unused function strapping recommendations for LVDS

Function	Pin name	Recommendations if unused
Single LVDS0	LVDS0_CLK_P, LVDS0_CLK_N, LVDS0_Dx_P, LVDS0_Dx_N	Not connected
Single LVDS1	LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N	Not connected
Both LVDS0 and LVDS1	LVDS0_CLK_P, LVDS0_CLK_N, LVDS0_Dx_P, LVDS0_Dx_N, LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N, VDD_LVDS_1P8	Not connected

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Table 5. Unused function strapping recommendations for MIPI

Function	Pin name	Recommendations if unused
MIPI_DSI	MIPI_DSI_CLK_N, MIPI_DSI_CLK_P, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N	Not connected
MIPI_CSI	MIPI_CSIx_Dx_P, MIPI_CSIx_Dx_N, MIPI_CSIx_CLK_P, MIPI_CSIx_CLK_N	Not connected
MIPI_CSI and MIPI_DSI	VDD_MIPI_1P8, VDD_MIPI_0P8, MIPI_REXT, MIPI_DSI_CLK_N, MIPI_DSI_CLK_P, MIPI_DSI_DX_P, MIPI_DSI_DX_N, MIPI_CSIx_Dx_P, MIPI_CSIx_Dx_N, MIPI_CSIx_CLK_P, MIPI_CSIx_CLK_N	Not connected

Table 6. Unused function strapping recommendations for USB

Function	Pin name	Recommendations if unused
USB1	USB1_VBUS, USB1_ID, USB1_D_P, USB1_D_N, USB1_TXRTUNE	Not connected
USB2	USB2_VBUS, USB2_ID, USB2_D_P, USB2_D_N, USB2_TXRTUNE	Not connected
Both USB1 and USB2	USB1_VBUS, USB1_ID, USB1_D_P, USB1_D_N, USB1_TXRTUNE, USB2_VBUS, USB2_ID, USB2_D_P, USB2_D_N, USB2_TXRTUNE, VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Not connected

Table 7. Unused function strapping recommendations for PCIe

Function	Pin name	Recommendations if unused
PCIE1	ETH_PCIE1_TX0_P, ETH_PCIE1_TX0_N, ETH_PCIE1_RX0_P, ETH_PCIE1_RX0_N, PCIE_REF_OUT_CLK_P, PCIE_REF_OUT_CLK_N	Not connected
	ETH_PCIE1_REF_PAD_CLK_P, ETH_PCIE1_REF_PAD_CLK_N, ETH_PCIE1_RESREF	Tie to ground using a 10K resistor
	VDD_PCI_1P8, VDD_PCI_0P8	Not connected

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 952 family of processors.

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4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 8 for a quick reference to the individual tables and sections.

Table 8. i.MX 952 chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	See Absolute maximum ratings
Thermal resistance	See Thermal resistance
Operating ranges	See Operating ranges
Clock sources	See Clock source
Maximum supply currents	See Maximum supply currents
Power modes	See Power modes
Power supplies requirements and restrictions	See Power supplies requirements and restrictions

4.1.1 Absolute maximum ratings

CAUTION: Stresses beyond those listed in the following table may reduce the operating lifetime or cause immediate permanent damage to the device. The table below does not imply functional operation beyond those indicated in the operating ranges and parameters table.

Table 9. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_SOC	Core supplies input voltages	-0.3	—	1.08	V	—	—
NVCC_SD2	IO supply for SD2	-0.3	—	3.96	V	—	—
VDD2H_DDR	DDR I/O supply voltage	-0.3	—	1.32	V	—	—
VDDQ_DDR	DDR I/O supply voltage	-0.3	—	0.72	V	—	—
NVCC_CCM_DAP	CCM supply voltage [1]	-0.3	—	3.96	V	—	—
NVCC_BBSM_1P8	IO supply and IO Pre-driver supply for BBSM bank	-0.3	—	2.16	V	—	—
USB1_VBUS, USB2_VBUS	USB VBUS input detected	-0.3	—	3.96	V	—	—
VDD_USB_0P8	Power for USB OTG PHY	-0.3	—	0.96	V	—	—

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Table 9. Absolute maximum ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_USB_1P8	Power for USB OTG PHY	-0.3	—	2.16	V	—	—
VDD_USB_3P3	Power for USB OTG PHY	-0.3	—	3.96	V	—	—
VDD_MIPI_0P8	MIPI PHY supply voltage	-0.3	—	0.96	V	—	—
VDD_MIPI_1P8	MIPI PHY supply voltage	-0.3	—	2.16	V	—	—
VDD_PCI_0P8	PCI PHY supply voltage	-0.3	—	0.96	V	—	—
VDD_PCI_1P8	PCI PHY supply voltage	-0.3	—	2.16	V	—	—
NVCC_GPIO, NVCC_WAKEUP, NVCC_AON, NVCC_ENET	GPIO supply voltage	-0.3	—	3.96	V	—	—
NVCC_GPIO_LD	GPIO LD supply voltage [2][3]	-0.3	—	3.95	V	—	—
VDD_LVDS_1P8	LVDS PHY supply voltage	-0.3	—	2.16	V	—	—
VDD_ANA_0P8	Analog core supply voltage [3]	-0.3	—	0.96	V	—	—
VDD_ANA_1P8	Analog core supply voltage [1]	-0.3	—	2.16	V	—	—
VREFH_1P8_ADC	1.8 V supply for ADC [1]	-0.3	—	2.16	V	—	—
VDD_ANAVDET_1P8	Analog core supply voltage	-0.3	—	2.16	V	—	—
Vin/Vout	Input/output voltage range [4]	-0.3	—	NVCC_XXX + 0.3	V	—	—
TSTORAGE	Storage temperature range	-55	—	150	℃	—	—

[1] This supply being incorrect can cause the IO pads to be misconfigured causing damage.
[2] It is combined with NVCC_GPIO on 19 x 19 mm package and separated on 15 x 15 mm package.
[3] VDD_ANA_0P8 refers to VDD_ANA0_0P8 and VDD_ANA1_0P8 on 15 x 15 mm package.
[4] Input Voltages to the GPIO must be no lower than -300mV and no higher than NVCC +300mV, where the NVCC is the GPIO supply operational voltage seen at the SoC. These offsets are inclusive of any DC offsets from the driving IC or AC transients (overshoots or undershoots) seen during signal switching

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4.1.2 Electrostatic discharge and latch-up ratings

Table 10. Electrostatic discharge and latch-up ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHBM	Electrostatic Discharge (ESD): Human Body Model (HBM) [1]	-1000	—	1000	V	—	—
VCDM	Electrostatic Discharge (ESD): Charged Device Model (CDM) [2]	-250	—	250	V	—	—
ILAT	Latch UP (LU) Immunity level: Class II at 105 °C ambient [3]	-100	—	100	mA	—	—

[1] Determined according to JEDEC Standard JS001, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
[2] Determined according to JEDEC Standard JS002, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
[3] Determined according to JEDEC Standard JESD78, IC Latch-up Test.

4.1.3 Thermal resistance

4.1.3.1 15 x 15 mm FCBGA package thermal characteristics

Table 11 displays the 15 x 15 mm FCBGA package thermal resistance data.

Table 11. 15 x 15 mm FCBGA thermal resistance data

Rating	Board Type[1]	Symbol	Value	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	17.3	°C/W
Junction-to-Top of Package Thermal Characterization parameter[2]	JESD51-9, 2s2p	ψ_{JT}	0.2	°C/W
Junction to Case Thermal Resistance[3]	N/A	$R_{\theta JC}$	0.4	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9). Test board has 40 vias under die shadow mapped according to BGA layout under die. Each vias is 0.2 mm in diameter and connects top layer with the first buried plane layer.
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment.
[3] Junction-to-Case (top) thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface temperature.

4.1.3.2 19 x 19 mm FCBGA package thermal characteristics

Table 12 displays the 19 x 19 mm FCBGA package thermal resistance data.

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Table 12. 19 x 19 mm FCBGA thermal resistance data

Rating	Board type[1]	Symbol	Value	Unit
			Bare die	
Junction to Ambient thermal resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	14.2	°C/W
Junction-to-Top of package thermal characterization parameter[2]	JESD51-9, 2s2p	ψ_{JT}	0.1	°C/W
Junction to Case thermal resistance[3]	N/A	$R_{\theta JC}$	0.2	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface.

4.1.4 Power architecture

The power architecture of i.MX 952 is defined based on the assumption that systems are constructed for the case where the PMIC is used to supply all the power rails to the processor. The SoC can be powered from discrete parts rather than a PMIC, but a discrete-based solution is not necessarily BOM cost-optimized.

NVCC_BBSM_1P8 must be powered first and stay until the last.

Majority of the digital logic is supplied with the supply from VDD_SOC.

The VDD_SOC has following modes:

- Overdrive mode
- Nominal mode
- Low drive mode
- Suspend mode

GPIO interfaces functionally only need to operate at 1.8 V. One exception is the SD card interface, which must support both 1.8 V and 3.3 V (for compatibility with legacy 3.3 V SD cards), as well as the “GPIO” pins that may be connected to a RPi-like expansion connector (which for compatibility with components in the ecosystem need to be able to support 3.3 V, while also needing to support 1.8 V for 1.8 V-optimized designs).

The DRAM controller and PHY have multiple external power supplies:

Table 13. Power supplies of the DRAM controller and PHY

Power supplies	Modules
VDD_SOC	SoC synthesized DRAM controller digital logic
VDD_ANA_0P8	DRAM PLL and PHY digital logic
VDD_ANA_1P8	DRAM PLL and PHY analog circuitry
VDD2H_DDR	DRAM I/O supply (1.1 V for LPDDR4X and 1.05 V for LPDDR5)
VDDQ_DDR	DRAM I/O supply (0.6 V for LPDDR4X and 0.5 V for LPDDR5)

For all the integrated analog modules, their 1.8 V analog power will be supplied externally through power pads. These supplies are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

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For the integrated LVDS PHY, PCIe PHY, and USB PHYs, their 3.3 V (where supported), 1.8 V and their digital power will be supplied externally through power pads. The powers to those PHYs are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For BBSM/RTC, the 1.8 V IO pre-driver supply and 1.8 V IO pad supply will also be supplied externally. The BBSM_LP core digital domain logic is supplied by an internal LDO.

Figure 4 is the power architecture diagram for the whole chip. Note that it only shows power supplies and does not show capacitors that may be required for internal LDO regulators.

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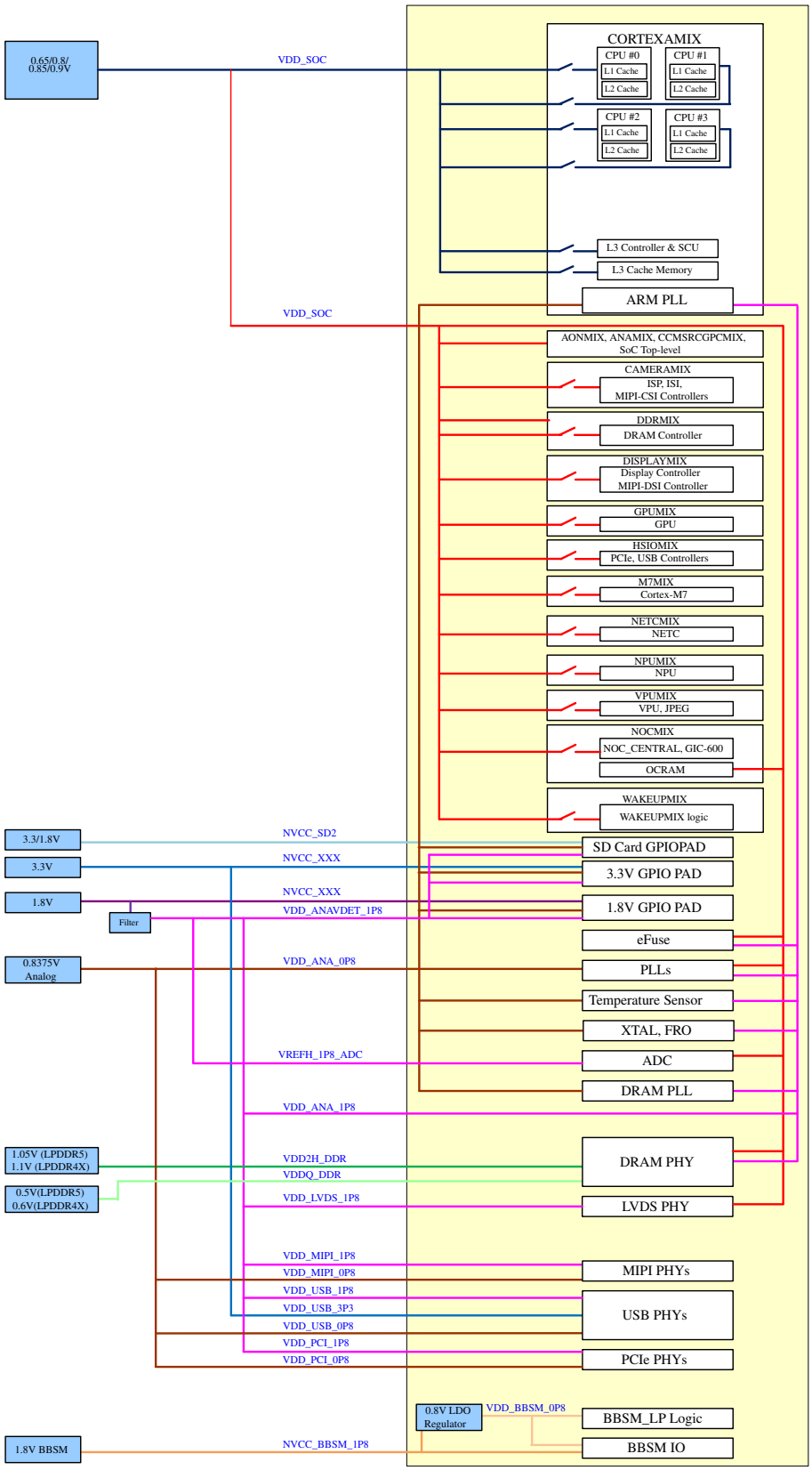


Figure 4. Power architecture of i.MX 952 family of processors

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4.1.4.1 Ramp rate specifications

Table 14. Ramp rate specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_SOC / VDD_ANA_0P8	Power supply for SoC logic, Cortext-A-55 core, PLLs, temperature sensor, and LVCMOS I/O	0.1	—	30	V/ms	Voltage level = 0.8 V	—
VDDQ_DDR / VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X PHY, LPDDR5/ LPDDR4X mode	0.1	—	5	V/ms	Voltage level = 0.5,0.6V / 1.05,1.1V	—
VDD_ANA_1P8/ VDD_ANAVDET_1P8/VREFH_1P8_ADC	1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, ADC, and 24 MHz XTAL	0.1	—	5	V/ms	Voltage level = 1.8 V	—
VDD_USB_3P3	3.3 V supply for USB PHY	0.1	—	30	V/ms	Voltage level = 3.3 V	—
NVCC_XXX	Power supply for GPIO	0.1	—	5	V/ms	Voltage level = 1.8 V	—
NVCC_XXX	Power supply for GPIO	0.1	—	30	V/ms	Voltage level = 3.3 V	—
NVCC_BBSM_1P8	I/O supply for GPIO in BBSM bank	0.1	—	30	V/ms	Voltage level = 1.8 V	—

4.1.5 Power modes

This section introduces the power modes used in the i.MX 952.

4.1.5.1 Power mode definition

The i.MX 952 supports the following power modes:

- RUN Mode: All external power rails are on, the Cortex®-A55 is active and running; other internal modules can be on/off based on application.
- Low Power RUN Mode: This mode is defined as a very low power run mode with all external power rails are on. In this mode, all the unnecessary power domain (MIX) can be off, except AONMIX and the internal modules required, such as OSC24M/PLL. Cortex-M33 CPU in AONMIX handles all the computing and data processing. Cortex-A55 is power down and DRAM can be in self-refresh/retention mode. All the modules in the AONMIX, such as SAI/CAN/UART, can be used directly. To use modules in other power domain, such as WAKEUPMIX, the user can turn on additional peripherals and related power by Cortex-M33 as needed. Additional low power modes are also supported, but do not have power characterized in the Data Sheet. Refer to the Reference Manual for a full set of power management capabilities.
- IDLE Mode: This mode is defined as a mode, which the Cortex®-A55 can automatically enter when there is no thread running and all high-speed devices are not active. The Cortex®-A55 can be put into power gated state but with L3 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated, but still remains powered. Compared with RUN mode,

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all the external power rails from the PMIC remain the same and most of the modules still remain in their state, so the interrupt response in this mode is very small.

- SUSPEND Mode: This mode is defined as the most power saving mode where all the clocks are off (including the Cortex®-M33 CPU), all the unnecessary power supplies are off and all power gateable portions of the SoC are power gated. The Cortex®-A55 CPUs and the Cortex®-M7 CPU are fully power gated, all internal digital logic and analog circuit that can be powered down will be off, all PHYs are power gated. DRAM is set at self-refresh/retention mode. VDD_SOC (and related digital supply) voltage is reduced to the “Suspend mode” voltage. The exit time from this mode will be much longer than IDLE, but the power consumption will also be much lower.
- BBSM Mode: This mode is also called RTC mode. Only the power for the Battery Backed non-Secure Module (BBNSM) and Battery Backed Secure Module (BBSM) remain on to keep RTC, BBNSM and BBSM logic are alive.
- OFF Mode: All power rails are off.

Note: *Beyond the modes defined here, additional options can be configured in software, such as to adjust clock frequencies or gate clocks through the CCM programming model, or to adjust on-die power-gating through the SRC or GPC programming model, or to adjust the voltage supplied to the VDD_SOC supply as per* Operating ranges *in the Data Sheet.*
Note: *These power modes are different than the voltage mode ranges.*

Table 15 summarizes the external power supply states in all the power modes.

Table 15. The power supply states

Power rail	OFF	BBSM	SUSPEND (Analog on)	IDLE	RUN/LP RUN
NVCC_BBSM_1P8	OFF	ON	ON	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
VDD2H_DDR VDDQ_DDR	OFF	OFF	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
VDD_ANA_0P8 VDD_MIPI_0P8 VDD_PCI_0P8 VDD_USB_0P8	OFF	OFF	ON	ON	ON
VDD_ANA_1P8/ VDD_ANAVDET_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_PCI_1P8 VDD_USB_1P8 VDD_USB_3P3	OFF	OFF	ON	ON	ON

4.1.5.2 Low power modes

The state of each module in the IDLE, SUSPEND, and BBSM modes are defined in the Table 16.

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Table 16. Low power mode definition

	IDLE	SUSPEND	BBSM
CCM LPM mode	WAIT	STOP	N/A
Arm A55 CPU	OFF	OFF	OFF
Shared L3 cache	ON	OFF	OFF
DRAM controller and PHY	ON	OFF	OFF
ARM_PLL	OFF	OFF	OFF
DRAM_PLL	OFF	OFF	OFF
SYSTEM_PLL1	ON	OFF	OFF
XTAL	ON	OFF	OFF
RTC	ON	ON	ON
External DRAM device	Self-Refresh[1]	Self-Refresh [2]	OFF
USB PHY	In Low Power State	OFF	OFF
DRAM clock	266 MHz	OFF	OFF
Module clocks	ON as needed	OFF	OFF
EdgeLock	ON	ON	OFF
GPIO Wakeup	Yes	Yes	No
RTC Wakeup	Yes	Yes	Yes
USB remote wakeup[3]	Yes	No[4]	No
Other wakeup source	Yes	No	No

[1] Automatic enter self-refresh when there is no DRAM access
[2] Put into self-refresh mode by SW before entering low power mode
[3] Remote wakeup can be supported if the USB PHY power is on in this mode.
[4] Turn off externally by PMIC when PMIC_STBY_REQ signal is asserted.

4.1.5.3 Chip power in different Low Power modes

The table below shows power consumption in different LP modes.

Table 17. BBSM Mode

Supply	Voltage (V)	Typical power (mw)[1]	Maximum power (mw)[1]
NVCC_BBSM_1P8	1.8	0.119	0.193

[1] The BBSM power numbers are based on bench measurement values with deviations derived from statistical limits.

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Table 18. SUSPEND Mode

Supply	Voltage	Typical power (mw)[1]
VDD SOC[2]	0.65	14.3
NVCC AON [3]	3.3	1.694
NVCC CCM DAP [3]	1.8	0.593
NVCC ENET	1.8	0.678
NVCC GPIO [3]	3.3	3.930
NVCC SD2 [3]	3.3	1.293
NVCC WAKEUP [3]	1.8	0.960
VDD USB 1P8	1.8	0.353
VDD ANA 1P8	1.8	1.359
VDD LVDS 1P8	1.8	0.038
VDD MIPI 0P8	0.8375	2.095
VDD MIPI 1P8	1.8	0.017
VDD PCI 1P8	1.8	0.010
VDD USB 0P8	0.8375	0.284
VDD ANA 0P8	0.8375	0.634
VDD PCI 0P8	0.8375	0.383
VDD2 DDR	1.05	0.056
VDDQ DDR	0.5	0.030
VDD ANA VDET 1P8	1.8	0.149
VDD USB 3P3	3.3	0.186
Total Power [mW]		**29.230**

[1] Except for VDD_SOC, all power measurement numbers are collected at 25 °C Tj based on characterization and values are use case dependent.
[2] VDD_SOC power measurements are tested in production.
[3] To achieve this low power consumption values for I/O power rails in SUSPEND mode, it is recommended to configure the IOMUX of those pins to GPIO input and change the PAD control settings to pull-up or pull-down depends on the board design before entering SUSPEND mode.

4.1.6 Operating ranges

The following table provides the operating ranges of the i.MX 952 processors. For details about the power structure of processors, see the “Clock and Power Overview” chapter of the i.MX 952 Reference Manual (IMX952RM).

Table 19. Operating ranges

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_SOC	Power supply for SoC logic, Cortex-A55 core and DDR PHY [1]	0.85	0.90	0.955	V	Overdrive mode	—

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Table 19. Operating ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_SOC	Power supply for SoC logic and Cortex-A55 [1]	0.80	0.85	0.905	V	Nominal mode	—
VDD_SOC	Power supply for SoC logic and Cortex-A55 [1]	0.76	0.80	0.85	V	Low drive mode	—
VDD_SOC	Power supply for SoC logic and Cortex-A55 [1]	0.61	0.65	0.7	V	Suspend mode	—
NVCC_BBSM_1P8	IO supply for GPIO in BBSM bank	1.65	1.8	1.95	V	—	—
VDD_ANA_0P8	Digital supply for PLLs, temperature sensor, and LVCMOS I/O	0.795	0.8375	0.88	V	—	—
VDD_ANA_1P8/ VDD_ANAVDET_ 1P8	1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, 24 MHz XTAL, and supply voltage for voltage detect	1.71	1.8	1.89	V	—	—
VREFH_1P8_ADC	1.8V reference voltage for ADC	1.71	1.8	1.89	V	—	—
VDD_MIPI_0P8	Digital supply for MIPI PHY	0.795	0.8375	0.88	V	—	—
VDD_USB_0P8	Digital supply for USB PHYs	0.795	0.8375	0.88	V	—	—
VDD_USB_1P8	1.8 V supply for USB PHYs	1.71	1.8	1.89	V	—	—
VDD_USB_3P3	3.3 V supply for USB PHY (Vmax consistent with Vmax supported by NVCC GPIO supplies)	3.069	3.3	3.45	V	—	—
VDD_PCI_0P8	Digital supply for PCIe PHY	0.795	0.8375	0.88	V	—	—
VDD_PCI_1P8	1.8 V supply for PCIe PHY	1.71	1.8	1.89	V	—	—

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Table 19. Operating ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_LVDS_1P8	1.8 V supply for LVDS	1.71	1.8	1.89	V	—	—
VDD_MIPI_1P8	1.8 V supply for MIPI PHYs	1.71	1.8	1.89	V	—	—
VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X PHY, LPDDR5 mode	1.01	1.05	1.12	V	—	—
VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X I/O, LPDDR4X mode	1.06	1.1	1.17	V	—	—
VDDQ_DDR	Voltage supply for LPDDR5/4X I/O, LPDDR5 Mode, ODT enabled or disabled	0.47	0.5	0.57	V	—	—
VDDQ_DDR	Voltage supply for LPDDR5/4X I/O, LPDDR4X Mode	0.57	0.6	0.65	V	—	—
NVCC_AON, NVCC_SD2, NVCC_GPIO, NVCC_GPIO_LD, NVCC_WAKEUP, NVCC_CCM_DAP, NVCC_ENET	Power supply for GPIO when it is in 1.8 V mode [2]	1.65	1.8	1.95	V	—	—
NVCC_AON, NVCC_SD2, NVCC_GPIO, NVCC_GPIO_LD, NVCC_WAKEUP, NVCC_CCM_DAP, NVCC_ENET	Power supply for GPIO when it is in 3.3 V mode	3	3.3	3.45	V	—	—

[1] Voltages > Vtyp x 1.05 but < Vmax are only supported if using a PMIC supporting Automatic Voltage Positioning (AVP).
[2] It is combined with NVCC_GPIO on 19 x 19 mm package and separated on 15 x 15 mm package.

4.1.7 Temperature ranges specifications

Table 20. Temperature ranges specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tj	Junction temperature—Industrial [1][2]	-40	—	105	°C	—	—
Ta	Ambient temperature—Industrial [2]	-40	—	—	°C	—	—

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[1] Tj minimum temperature supported at startup where Tj = Ta.
[2] See the application note, i.MX 952 Product Lifetime Usage Estimates for information on product lifetime (power-on hours) for this processor.

4.1.8 Maximum frequency of modules

The following table provides the maximum frequency of modules in the i.MX 952 family of processors.

Table 21. Maximum frequency of modules

Symbol	Description	Low Drive mode	Nominal Drive mode	Overdrive mode	Unit
Cortex-A55 cores	CORTEXMIX	900	1404	1700	MHz
DynamIQ Shared Unit (DSU)	CORTEXMIX	750	1170	1500	MHz
Cortex-M33 core	AONMIX	166.67	250	333.33	MHz
Cortex-M7 core	M7MIX	400	667	800	MHz
EdgeLock® Secure Enclave	AONMIX	133.33	200	250	MHz
NPU	NPUMIX	500	800	1000	MHz
ISP	CAMERAMIX	400	666.67	800	MHz
ISI	CAMERAMIX	333.33	500	667	MHz
3D GPU	GPUMIX	500	800	1000	MHz
Display controller	DISPLAYMIX	400	667	800	MHz
VPU	VPUMIX	333.33	500	666.67	MHz
DRAM (LPDDR5) 19 x 19 mm package	DDRMIX	3000	4500	6000	MT/s
DRAM (LPDDR4X) 19 x 19 mm package	DDRMIX	2667	3733	4266	MT/s
DRAM (LPDDR5) 15 x 15 mm package	DDRMIX	2667	3733	4266	MT/s
DRAM (LPDDR4X) 15 x 15 mm package	DDRMIX	2133	3200	4000	MT/s

4.1.9 Clock source

This section introduces on-chip oscillator and external clock sources.

4.1.9.1 External input clock sources

The i.MX 952 processor is designed to function with quartz crystals to generate the frequencies necessary for operation. 24 MHz for the main clock source and 32.768 kHz for the real time clock. External clock can be injected into RTC_XTALI if the frequency precision and jitter precision are sufficient.

The XTAL input is used to synthesize all of the clocks in the system with the RTC_XTAL input contributing to time keeping and low frequency operations.

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Table 22. External input clock sources

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fckil	RTC_XTALI Oscillator [1]	—	32.768	—	kHz	—	—

[1] External clock source or a crystal with the integrated oscillator amplifier. Recommended nominal frequency is 32.768 kHz.

4.1.9.1.1 Audio external clock frequency

Table 23 shows the maximum frequency of the audio external clock.

Table 23. Audio external clock frequency

Symbol	Description	Low drive mode	Nominal mode	Overdrive mode	Unit
fext_clk	EXT_CLK maximum frequency[1]	133	200	200	MHz

[1] Audio EXT_CLK signal muxed on either pin SD2_VSELECT or PDM_BIT_STREAM1.

4.1.9.2 RTC_OSC

The following table shows the external input clock case for the RTC_XTAL oscillator.

Table 24. RTC_OSC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
f	Frequency	—	32.768	—	kHz	—	—
VIH	RTC_XTALI	0.9 x NVCC_BBSM_1P8	—	NVCC_BBSM_1P8	V	—	—
VIL	RTC_XTALI	0	—	0.1 x NVCC_BBSM_1P8	V	—	—
—	Duty cycle	45	—	55	%	—	—

For the case where an external clock is desired to be the source of the 32.768 kHz clock, the RTC_XTALI pin may be driven with the RTC_XTALO pin disconnected.

4.1.9.3 24 MHz quartz specification

Table 25. 24 MHz quartz specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fXTAL	Frequency	—	24	—	MHz	—	—
DL	Drive level [1]	—	—	100	µW	—	—

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Table 25. 24 MHz quartz specification...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CLOAD	Cload	6	8/10	12	pF	—	—
ESR	ESR	—	—	120	Ω	CLOAD = 6/8/10pF	—
ESR	ESR	—	—	50	Ω	CLOAD = 12pF	—
Δf	Frequency Tolerance	—	—	30	ppm	Without considering aging and temperature-induced drift.	—

[1] The drive level value specifies the oscillator drive capability. The selected crystal must be rated for an allowable drive level of at least 100 µW to ensure stable operation and long-term reliability.

4.1.9.4 32.768 kHz quartz specification

Table 26. 32.768 kHz quartz specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fXTAL	Frequency (crystal mode)	—	32.768	—	kHz	—	—
CLOAD	Cload	—	12.5	—	pF	—	—
ESR	ESR	—	—	90	kΩ	—	—
DL	Drive level (crystal mode) [1]	—	—	0.5	µW	—	—

[1] Actual working drive level depends on real design. Please contact crystal vendor for selecting drive level of crystal.

4.1.9.5 Free-running oscillator (FRO) specifications

The FRO is a trimmable 200 to 400 MHz low power, high accuracy internal oscillator, that can be used as a clock source for some i.MX 952 modules.

Table 27. Free-running oscillator (FRO) specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FCLK	Clock Frequency	200	—	400	MHz	Depending upon trim / VDDCORE > 0.7 V	—
FACC	Frequency Accuracy	—	± 2.0	± 6.0	%	VDDCORE > 0.7 V / FCLK ≈ 256 MHz / Open Loop	—
TSU	Startup Time	—	50	—	µs	Fast startup disabled	—

4.1.10 Maximum supply currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.

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To help illustrate the effect of the application on power consumption, data was collected while running consumer standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Table 28. Maximum supply currents

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_SOC	Power supply for SoC logic	—	—	7300	mA	—	—
VDD_ANA_1P8	1.8 V supply for PLLs, temperature sensor, LVCMOS voltage detect reference, ADC, 24 MHz XTAL, LVDS, MIPI, and USB PHYS [1]	—	—	40	mA	—	—
NVCC_BBSM_1P8	I/O supply for GPIO in BBSM bank	—	—	2	mA	—	—
NVCC_<XXX>	Power supply for GPIO [1]	—	—	Imax = N x C x V x (0.5 x F)	mA	—	—
VDDQ_DDR	Voltage supply for LPDDR5/ LPDDR4X [1]	—	—	Imax = N x C x V x (0.5 x F)	mA	—	—
VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X PHY, LPDDR5 mode	—	—	22	mA	—	—
NVCC_CCM_DAP	CCM supply voltage	—	—	Imax = N x C x V x (0.5 x F)	mA	—	—
VDD_ANAVDET_ 1P8	Supply voltage for voltage detect	—	—	9	mA	—	—
VREFH_1P8_ADC	Supply voltage for voltage detect	—	—	2	mA	—	—
VDD_MIPI_1P8	1.8 V supply for MIPI PHYs	—	—	11.64	mA	—	—
VDD_MIPI_0P8	0.8 V Digital supply for MIPI PHYs	—	—	156.53	mA	—	—
VDD_PCI_0P8	0.8 V Digital supply for PCI	—	—	66.23	mA	—	—
VDD_PCI_1P8	1.8 V supply for PCI	—	—	28.13	mA	—	—
VDD_USB_0P8	0.8 V supply for USB PHY	—	—	8.74	mA	—	—

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Table 28. Maximum supply currents...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_USB_1P8	1.8 V supply for USB PHY	—	—	32.68	mA	—	—
VDD_USB_3P3	3.3 V supply for USB PHY (Vmax consistent with Vmax supported by NVCC GPIO supplies)	—	—	24.28	mA	—	—
VDD_LVDS_1P8	1.8 V supply for LVDS interface [2]	—	—	150	mA	—	—
VDD_ANAx_0P8	Digital supply for PLLs, temperature sensor, LVCMOS I/O, MIPI, PCIe and USB PHYS	—	—	200	mA	—	—

[1] Where, N—Number of I/O pins supplied by the power line, C—Equivalent external capacitive load, V—I/O voltage, (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.
[2] Maximum dynamic current

4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

Figure 5 illustrates the power-up and power-down sequence of i.MX 952 processors.

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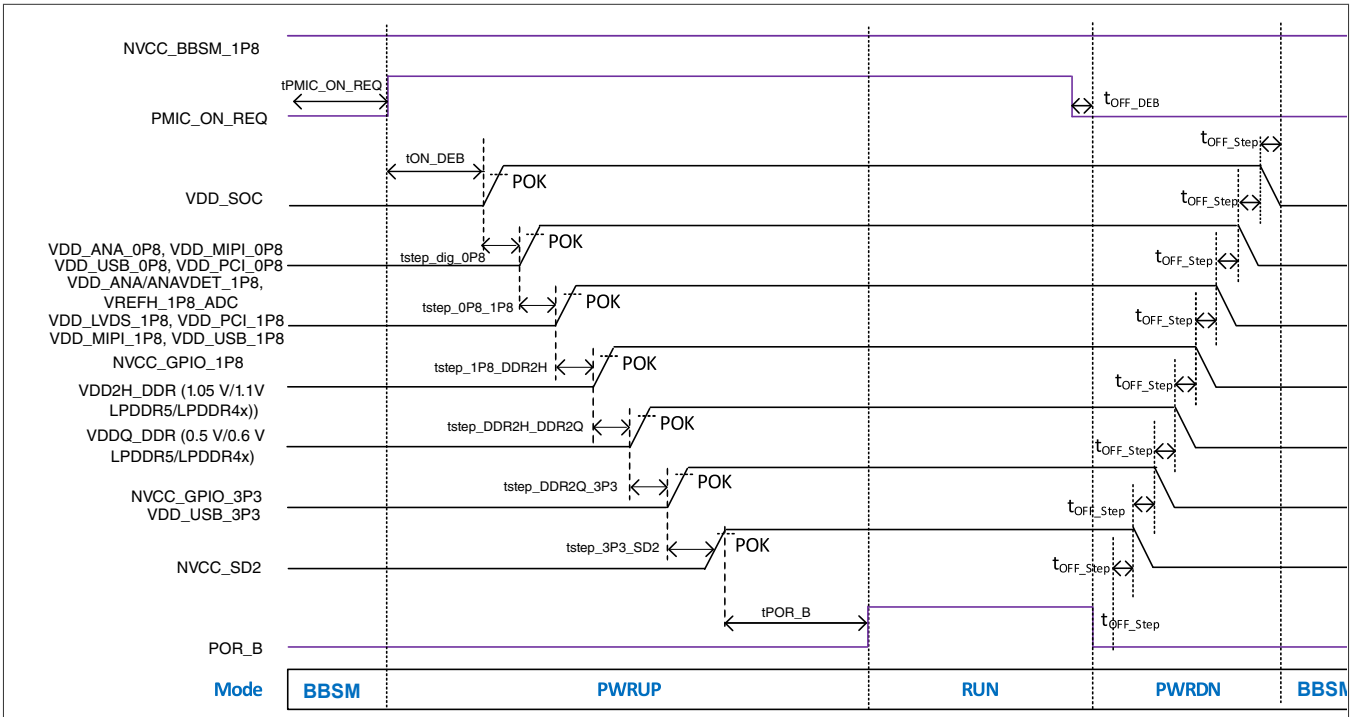


Figure 5. The power sequence of i.MX 952 processors

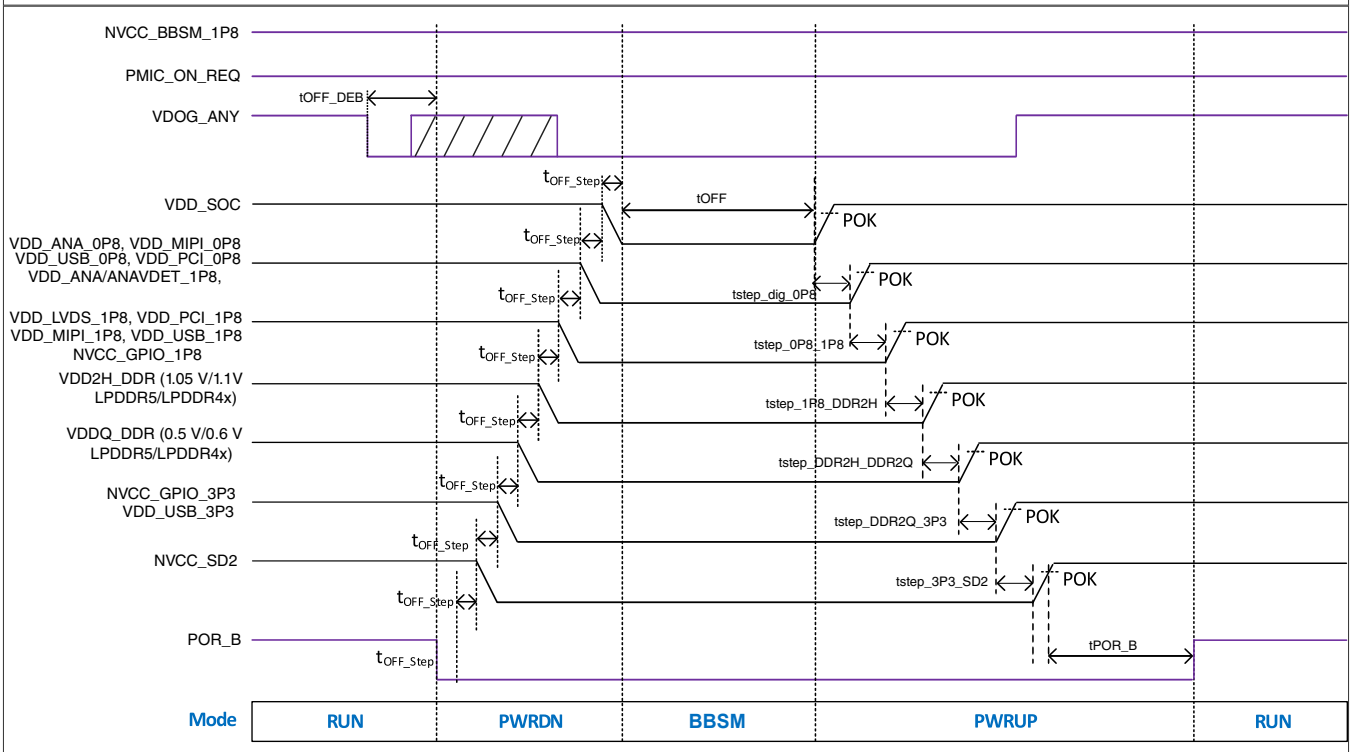


Figure 6. The power sequence of i.MX95 processor after cold reset (WDOG_ANY event)

Note: *WDOG_ANY signal is routed to the PMIC and can be configured to initiate a cold reset (i.e., a repower cycle). The signal polarity and active level are programmable, depending on the specific PMIC implementation.*

Note: *POR_B must be asserted whenever VDD_SOC is powered down, but NVCC_BBSM_1P8 is powered up (when the processor is in BBSM mode).*

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Note: *PMIC has a provision to recycle BBSM supply in case of abrupt supply drop beyond the operating range causing WDOG events.*
Note: *All non-NXP PMICs must have functional safety feature that ensures cycling of all supply rails when SoC does not respond or is in indeterminant state.*

Power sequencing

1. Turn on NVCC_BBSM_1P8
2. [The SoC asserts PMIC_ON_REQ at this point in time.]
3. Turn on VDD_SOC digital voltage supplies.
4. Turn on all VDD_*_0P8 analog, DDR, PHY, and PLL supplies.
   Note: *This step may be simultaneous with the VDD_SOC supplies if desired.*
5. Turn on all remaining 1.8 V supplies. This includes VDD_*_1P8 analog, PHY and PLL supplies, and any NVCC_XXX I/O supplies that are being operated at 1.8 V.
6. Turn on DDR VDD2H supply.
7. Turn on DDR VDDQ supply.
   Note: *The i.MX SoC has no VDD2H vs VDDQ sequencing requirements, but generally VDDQ must come up after VDD2H to meet DRAM memory component specification.*
8. Turn on any 3.3 V supplies. This includes NVCC_XX I/O supplies that being operated at 3.3 V and VDD_USB_3P3.
   Note: *This 3.3 V supply step may be simultaneous with the DDR VDD2H or DDR VDDQ supplies if desired.*
9. Turn on NVCC_SD2, if NVCC_SD2 is being used for a dynamically switchable 1.8/3.3 V SD card voltage (booting initially at 3.3 V).
   Note: *If NVCC_SD2 is operating at a fixed 1.8 V-only or 3.3 V-only voltlage in a give system, then it may power up at the same time as other supplies of the same voltage.*
10. POR_B release (it should be asserted during the entire power-up sequence).

4.2.1 Power-up sequence

The power-up sequence is defined as follows:

Table 29. Power-up sequence

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tPMIC_ON_Req	The time from when NVCC_BBSM_1P8 reaches its minimum operating range to when the SoC begins to assert PMIC_ON_REQ.	0	2	—	ms	—	—
tON_DEB	The time from when PMIC_ON_REQ reaches its high-level output voltage (VOH) to when VDD_SOC begins to power-up.	0	1	—	ms	—	—
tOFF_DEB	The time from PMIC_ON_REQ	—	1.6	—	ms	—	—

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Table 29. Power-up sequence...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	or WDOG_ANY reaches its low-level output voltage (VOL) to when PMIC begins to power-down.						
tstep_dig_0p8	The time from when VDD_SOC begins to power-up to when all VDD_*_0P8 analog, PHY and PLL supplies begin to power-up.	0	0.5	—	ms	—	—
tstep_0p8_1p8	The time from when the final VDD_*_0P8 analog, PHY and PLL supply begins to power-up to when 1.8 V supplies begin to power-up.	0.2	0.25	—	ms	—	—
tstep_1p8_ddr2h	The time from when the final 1.8V supply begins to power-up to when the DDR VDD2H supply begins to power-up.	0.4	0.5	—	ms	—	—
tstep_ddr2h_ddrq	The time from when the DDR VDD2H supply begins to power-up to when the DDR VDDQ supply begins to power-up.	0	0.3	—	ms	—	—
tstep_ddrq_3p3	The time from when the DDR VDDQ supply begins to power-up to when any 3.3 V supply begins to power-up.	0	0.1	—	ms	—	—
tstep_3p3_sd2	If NVCC_SD2 is being used for a dynamically switchable 1.8/3.3V SD card voltage	0	1	—	ms	—	—

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Table 29. Power-up sequence...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	(booting initially at 3.3 V), then this represents the time from when the final 3.3 V supply begins to power-up to when NVCC_SD2 begins to power-up.						
tPOR_B	The time from when all supplies reach their minimum operating range to when POR_B may be released.	0	—	—	ms	—	—
tOFF_Step	The time between voltage rails powering down.	0	—	—	ms	—	—
tOFF	tOFF represents the power-down delay requirement for all power rails to fully discharge to 0V. [1][2]	—	500	—	ms	—	—

[1] The minimum tOFF duration depends on system loading conditions, the total on-board capacitance, and the PMIC's discharge capability
[2] This parameter is typically programmable and may vary based on the specific PMIC implementation

4.2.2 Power-down sequence

The power-down sequence is defined as follows:

1. Turn off NVCC_BBSM_1P8 last

2. Turn off VDD_SOC after the other (non-BBSM) power rails or at the same time as other (non-BBSM) rails

3. No sequence for other power rails during power-down

Note: *When switching off supply group 0 (NVCC_BBSM_1P8), VDD_BBSM_0P8_CAP must be fully discharged to 0 V before starting the next power-up sequence to ensure correct operation.*

4.3 PLL electrical characteristics

Following sections introduce the Fractional-N (FracN) Phase-Locked Loops (PLL) and Low Noise PLL electrical characteristics.

4.3.1 Fracn PLL

Table 30. Fracn PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TLock	PLL lock time	—	—	100	µS	—	—

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Table 30. Fracn PLL*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fout	Output Clock Frequency	9.8M	—	2.5G	Hz	—	—
FPLL_MOD	SSCG modulation frequency	30	—	64	kHz	@40MHz and 50MHz ref clk	—
ΔFPLL_MOD	SSCG modulation depth	-4*Fref_pfd	—	—	Hz	Down Spread	—

4.3.2 Low Noise PLL

Table 31. Low Noise PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TLock	PLL lock time	—	—	100	µs	—	—
FPLL_MOD	SSCG modulation frequency	30	—	64	KHz	Fref_pfd =< 40 MHz	—
ΔFPLL_MOD	SSCG modulation depth	-4*Fref*pfd	—	—	Hz	Down Spread	—

4.4 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR5 and LPDDR4X modes
- LVDS I/O

4.4.1 General purpose I/O (GPIO) DC parameters

The following tables show the DC parameters for GPIO pads. The parameters are guaranteed per the operating ranges table, unless otherwise noted.

Table 32. General purpose I/O (GPIO) DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH (1.8V)	High-level output voltage	0.8 x NVCC_xxx	—	NVCC_xxx	V	DSE = X1, IOH = 1.1mA DSE = X6, IOH = 6.6 mA	—
VOL (1.8 V)	Low-level output voltage	0	—	0.2 x NVCC_xxx	V	DSE = X1, IOH = 1.1mA DSE = X6, IOH = 6.6 mA	—
VOH (3.3 V)	High-level output voltage	0.8 x NVCC_xxx	—	NVCC_xxx	V	DSE = X1, IOH = 2 mA DSE = X4, IOH = 8 mA	—

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Table 32. General purpose I/O (GPIO) DC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOL (3.3 V)	Low-level output voltage	0	—	0.2 x NVCC_xxx	V	DSE = X1, IOH = 2mA DSE = X4, IOH = 8 mA	—
VIL	Low-level input voltage	0	—	0.3 x NVCC_xxx	V	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125 °C	—
VIH	High-level input voltage	0.7 x NVCC_xxx	—	NVCC_xxx	V	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125 °C	—
Rpd3.3v	Pull-down resistor	24	43	87	kΩ	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125 °C	—
Rpu3.3v	Pull-up resistor	18	37	72	kΩ	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125 °C	—
Rpd1.8v	Pull-down resistor	13	23	48	kΩ	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125 °C	—
Rpu1.8v	Pull-up resistor	12	22	49	kΩ	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125 °C	—

Note: For GPIO pads, when the supplies are ramp-up or/and below operating level, the pad state values are undefined.

Note: For PHY pads, the PAD state values are undefined before POR_B is asserted.

4.4.1.1 Additional leakage parameters

Table 33. Additional leakage parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIH	Leakage high	-5	—	5	µA	Non-PHY IO, 1.65 V -3.465 V, Temp = -40° C to 125 °C | pad = VDDIO	—
IIL	Leakage low	-5	—	5	µA	Non-PHY IO, 1.65 V to 3.465 V, Temp = -40 °C to 125 °C | pad = VDDIO	—

4.4.2 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR4X/LPDDR5 operational modes. The DDR Memory Controller (DDRMC) is compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX952 application processors.

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4.4.3 DDR pin I/O leakage DC parameters

Table 34. DDR pin I/O leakage DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOz	I/O leakage current [1][2]	—	—	±180	µA	—	—

[1] Refer to IBIS model for complete IV curve characteristics
[2] Output leakage is measured with all outputs disabled, 0 V ≤ Vout ≤ VddQ

4.4.4 LVDS DC electrical characteristics

Table 35. LVDS DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vod	Differential Voltage Output Voltage	0.25	—	0.45	V	Rload = 100 Ω	—
Voh	Output Voltage High	1.25	—	1.6	V	Rload = 100 Ω	—
Vol	Output Voltage Low	0.9	—	1.25	V	Rload = 100 Ω	—
Vos	Offset Static Voltage (i.e. Common mode voltage)	1.125	—	1.375	V	Rload = 100 Ω	—
Vosdiff	VOS (Ripple peak to peak)	—	—	25	mV	Rload = 100 Ω	—
ISA ISB	Output short-circuited to GND	—	—	24	mA	—	—
ISAB	Output short current	—	—	12	mA	—	—

4.5 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR5 and LPDDR4X modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 7 and Figure 8.

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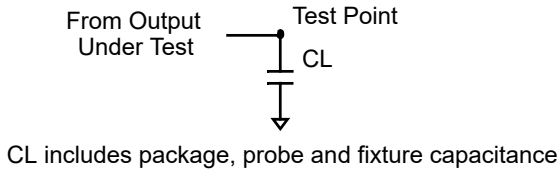


Figure 7. Load circuit for output

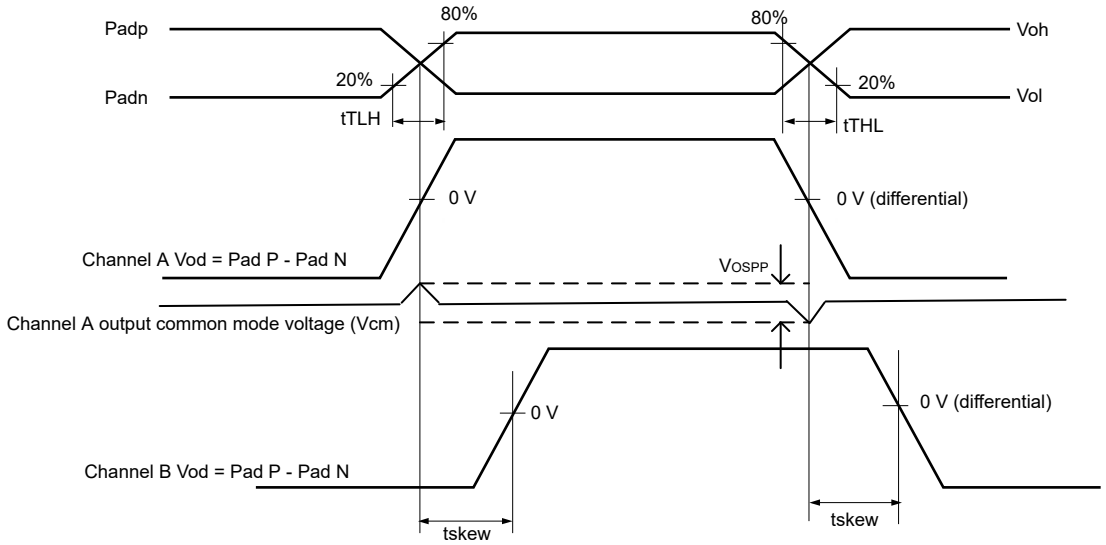


Figure 8. Output transition time waveform

4.5.1 General purpose I/O (GPIO) AC parameters

Table 36. General purpose I/O (GPIO) AC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fmax	Maximum frequency [1]	—	—	52	MHz	NVCC_xxx = 3.3 V, CL = 30 pF	—
fmax	Maximum frequency [1]	—	—	208	MHz	NVCC_xxx = 1.8 V, CL = 30 pF	—

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Table 36. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tR	TX rise time	3950	—	5950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X1	—
tF	TX fall time	4140	—	5600	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X1	—
tR	TX rise time	1890	—	2820	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X2	—
tF	TX fall time	1790	—	2560	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X2	—
tR	TX rise time	675	—	1950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X3	—
tF	TX fall time	584	—	1730	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X3	—
tR	TX rise time	521	—	1320	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X4	—
tF	TX fall time	442	—	748	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X4	—
tR	TX rise time	454	—	742	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X5	—
tF	TX fall time	380	—	554	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X5	—
tR	TX rise time	419	—	639	ps	Slew rate FSEL1 = 11b, Fast Slew Rate	—

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Table 36. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						(1.62 V, 1.8 V, 1.98 V), Drive strength X6	
tF	TX fall time	349	—	506	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X6	—
tR	TX rise time	4030	—	5790	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X1	—
tF	TX fall time	4410	—	6290	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X1	—
tR	TX rise time	1870	—	2950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X2	—
tF	TX fall time	1900	—	3310	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X2	—
tR	TX rise time	774	—	1930	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X3	—
tF	TX fall time	719	—	2070	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X3	—
tR	TX rise time	598	—	1360	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X4	—
tF	TX fall time	490	—	1590	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X4	—

[1] The frequency limit applies to all interfaces utilizing these pads, including but not limited to uSDHC, RGMII/RMII, XSPI, CAN, LPSPI, FlexIO and PWM.

4.5.2 DDR I/O AC electrical characteristics

The DDR I/O pads support LPDDR4X/LPDDR5 operational modes. The DDR Memory Controller (DDRMC) is compatible with JEDEC-compliant SDRAMs.

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DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX952 application processors.

4.5.3 LVDS AC timing specifications

Table 37. LVDS AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
f	Operating data rate	—	—	1155	Mbps	Rload = 100 Ω Vload = 2 pF Note: This is the maximum work condition of operating data rate.	—
Tfall	Vod fall time, 20 - 80%	—	—	0.3	UI (Unit Interval)	Rload = 100 Ω Vload = 2 pF Note: Measurement levels are 20% - 80% from output voltage.	—
Trise	Vod rise time, 20 - 80%	—	—	0.3	UI (Unit Interval)	Rload = 100 Ω Vload = 2 pF Note: Measurement levels are 20% - 80% from output voltage.	—
Tskew	Lane skew [1][2]	—	250	—	ps	Rload = 100 Ω, Cload = 2 pF	—

[1] Tskew is the differential time at Vod = 0 voltage between different channel.
[2] This value is absolute value and base on test.

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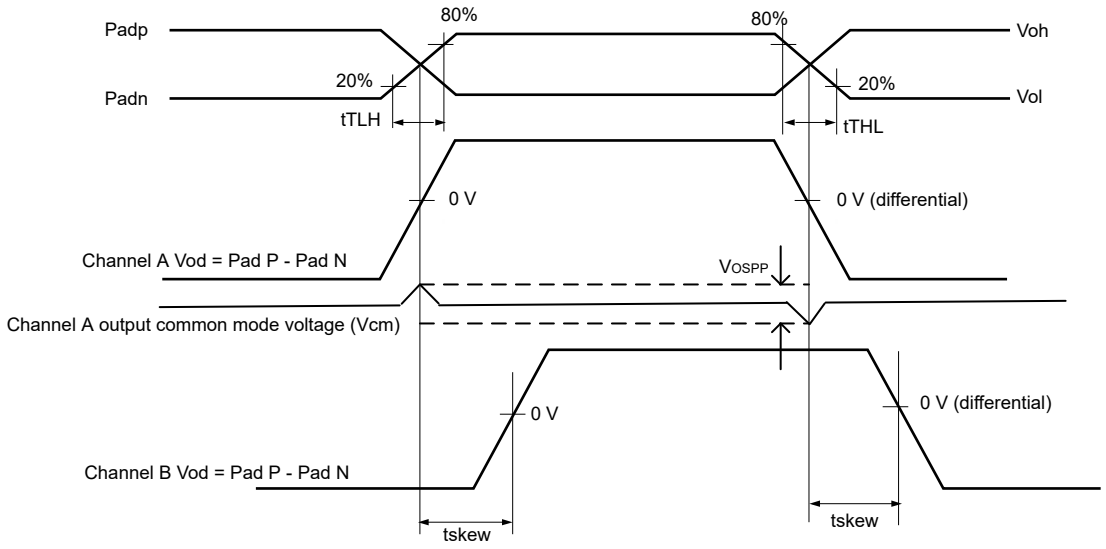


Figure 9. Output transition time waveform

4.6 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See *TIA/EIA STANDARD 644-A, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (2001)* for details.

4.6.1 DDR I/O output buffer impedance

The DDR output driver and ODT impedances are controlled across PVT using ZQ calibration procedure with a 120 Ω ±1% resistor connected to ground. Programmable drive strength and ODT impedance targets available in the NXP DDR tool are detailed in the device's IBIS model. Impedance deviation (calibration accuracy) is about approximately ±10% (maximum/minimum impedance) across PVT.

4.7 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 952 processor.

4.7.1 Reset timings parameters

The following figure shows the reset timing and table lists the timing parameters.

Table 38. Reset timings parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CC1	Duration of POR_B to be qualified as	1	—	—	RTC_XT ALI cycle	—	—

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Table 38. Reset timings parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	valid. Note: POR_B rise/fall times must be 400 uS or less.						

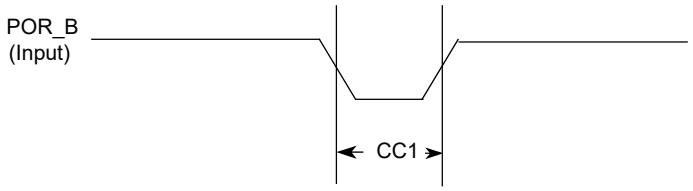


Figure 10. Reset timing diagram

4.7.2 WDOG Reset timing parameters

The table lists the WDOG reset timing parameters.

Table 39. WDOG Reset timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CC3	Duration of WDOG_ANY Assertion	1	—	—	RTC_XTALI cycle	—	—

Note: RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

The following figure shows the WDOG reset timing.

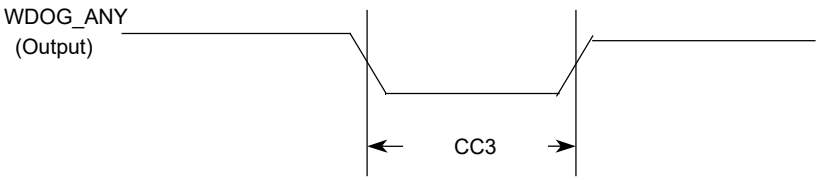


Figure 11. WDOGx_B timing diagram

4.7.3 JTAG timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Following table lists signal parameters.

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Table 40. JTAG timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SJ0	JTAG_TCK frequency of operation [1][2][3][4]	—	—	50	MHz	—	—
SJ1	JTAG_TCK cycle time in crystal mode [1][2]	20	—	—	ns	—	—
SJ2	JTAG_TCK clock pulse width measured at VM [1][2][5]	10	—	—	ns	—	—
SJ3	JTAG_TCK rise and fall times [1][2]	—	—	3	ns	—	—
SJ4	Boundary scan input data set-up time [1][2]	15	—	—	ns	—	—
SJ5	Boundary scan input data hold time [1][2]	15	—	—	ns	—	—
SJ6	JTAG_TCK low to output data valid [1][2]	—	—	600	ns	—	—
SJ7	JTAG_TCK low to output high impedance [1][2]	—	—	600	ns	—	—
SJ8	JTAG_TMS, JTAG_TDI data set-up time [1][2]	5	—	—	ns	—	—
SJ9	JTAG_TMS, JTAG_TDI data hold time [1][2]	5	—	—	ns	—	—
SJ10	JTAG_TCK low to JTAG_TDO data valid [1][2]	—	—	14	ns	—	—
SJ11	JTAG_TCK low to JTAG_TDO high impedance [1][2]	—	—	14	ns	—	—
SJ14	JTAG_TCK low to JTAG_TDO data invalid [1][2]	1	—	—	ns	—	—

[1] Input timing assumes an input signal slew rate of 3 ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 Ω , unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance of the transmission line can be equal to the selected RDSON of the I/O pad output driver.
[3] TDC = target frequency of JTAG
[4] 50 MHz frequency is for the JTAG debug interface. For boundary scan, the maximum TCK frequency is 10 MHz.
[5] VM = mid-point voltage

Following figure depicts the JTAG test clock input timing.

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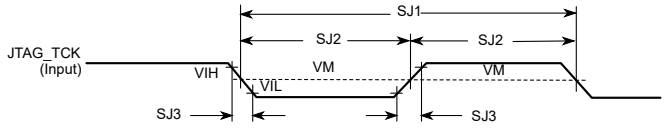


Figure 12. Test Clock Input Timing Diagram

Following figure depicts the JTAG boundary scan timing.

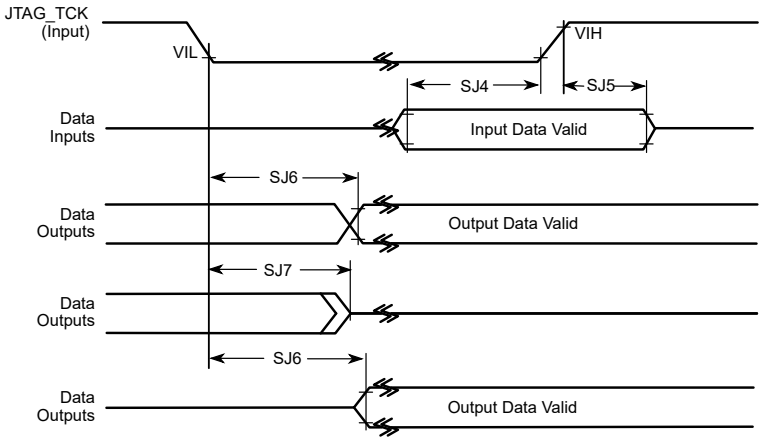


Figure 13. Boundary system (JTAG) timing diagram

Following figure depicts the JTAG test access port.

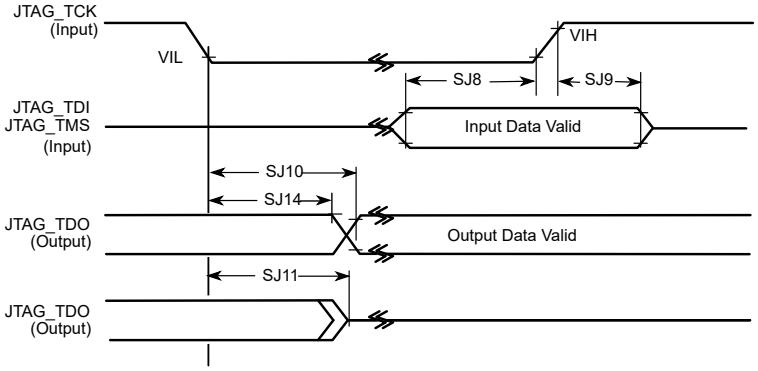


Figure 14. Test Access Port Timing Diagram

4.7.4 SWD timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Following table shows SWD timing.

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Table 41. SWD timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S0	SWD_CLK frequency	—	—	50	MHz	—	—
S1	SWD_CLK cycle time	20	—	—	ns	—	—
S2	SWD_CLK pulse width	10	—	—	ns	—	—
S3	Input data setup time	5	—	—	ns	—	—
S4	Input data hold time	5	—	—	ns	—	—
S5	Output data valid time	—	—	14	ns	—	—
S6	Output high impedance time	—	—	14	ns	—	—
S7	Output data invalid time	0	—	—	ns	—	—

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ω , unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line can be equal to the selected RDSON of the I/O pad output.

Following figure depicts the SWD timing.

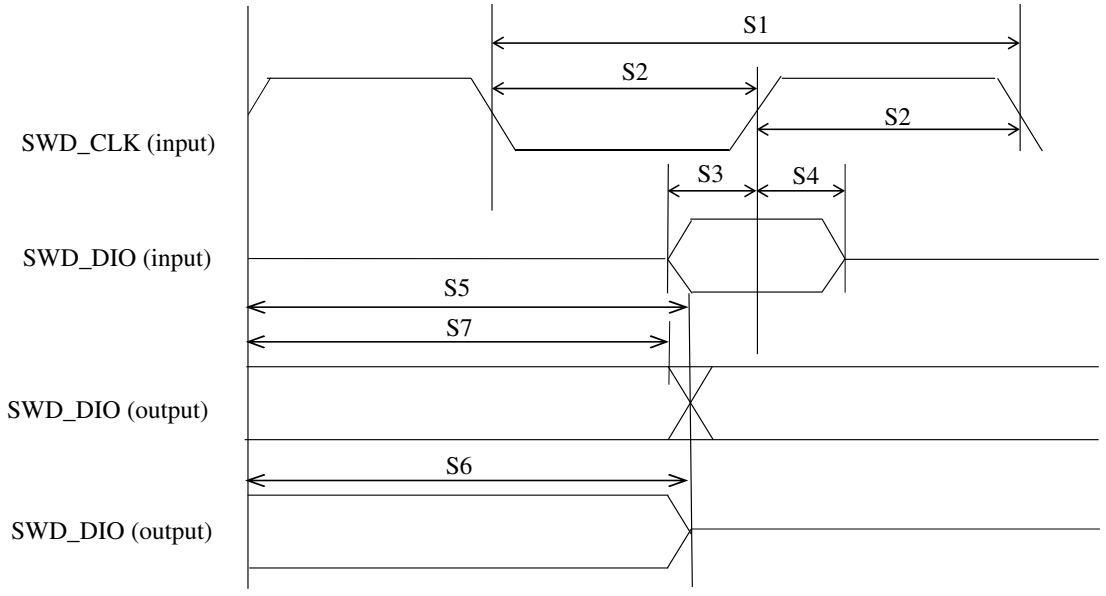


Figure 15. SWD timing

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4.7.5 DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)

The i.MX95 Family of processors have been designed and tested to work with JEDEC JESD209—compliant LPDDR5/LPDDR4X memory.

- JEDEC LPDDR4X Specification JESD209-4C, November 2019
- JEDEC LPDDR5 Specification JESD209-5A, January 2020

Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND, and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors:IMX9-PROCESSORS .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 42. DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Number of controllers (LPDDR4X)	—	—	1	—	—
—	Number of controllers (LPDDR5)	—	—	1	—	—
—	Number of channels (LPDDR4X)	—	—	2	—	—
—	Number of Chip Selects (LPDDR4X)	—	—	2	—	—
—	Bus Width	—	—	32	bit	—
—	Maximum Clock Frequency (LPDDR4X)	—	—	4266	MT/s	—
—	Maximum Clock Frequency (LPDDR5)	—	—	6000	MT/s	—

4.7.5.1 Clock/data/command/address pin allocations

These processors use generic names for clock, data, and command address bus.

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4.8 Analog interfaces

This section introduces the timing and electrical parameters about analog interfaces of i.MX 952 processors.

4.8.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended resolution specifications.

4.8.1.1 SAR ADC

Table 43. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VADIN	ADC Input Voltage	VGND	—	VDD_ANA_1P8	V	on or off channels	—
fADCK	ADC Conversion Clock Frequency	20	—	80	MHz	—	—
Csample	Sample cycles	5.5	—	—	number of cycles	—	—
Ccompare	Fixed compare cycles	—	58	131.5	number of cycles	—	—
Cconversion	Clock conversion cycles	Cconversion = Csample + Ccompare	Cconversion = Csample + Ccompare	Cconversion = Csample + Ccompare	number of cycles	—	—
CAD_INPUT	ADC Input Capacitance	—	—	7	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Series Resistance	—	—	1.25	kΩ	—	—
DNL	ADC Differential Non-linearity	-1	-	2	LSB	after calibration	—
INL	ADC Integral Non-linearity	-3	-	3	LSB	after calibration	—
ENOB	Effective Number of Bits [1]	—	10.5	—	bits	input signal frequency = 1KHz	—
RAS	Analog source resistance	—	—	5	kΩ	—	—
Bandgap	Output voltage ready time for bandgap [2] [3]	—	1	—	µs	—	—

[1] The ADC performance for inputs ADC0_CH0 to ADC0_CH3 can be impacted by JTAG operation (pins PB_4, PB_5, TMS, TCK). Performance specification is not guaranteed for these ADC inputs under this condition.
[2] Output voltage ready time = the ready time is the waiting time after enabling the Vbg output buffer from BBSM before ADC can convert data
[3] Based on simulation test (for the value -1)

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4.9 Audio

This section introduces the timing and electrical parameters about audio subsystem of I.MX 952 processor.

4.9.1 SAI switching specifications

This section provides the AC timings for the SAI in Controller (clocks driven) and Target (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR2[BCP] = 0, SAI_RCR2[BCP] = 0) and non inverted frame sync (SAI_TCR4[FSP] = 0, SAI_RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

The SAI4 pins muxed with ENET2 and the SAI4 pins muxed with XSPI1 are mutually exclusive. It does not support a use case where some SAI4 pins are connected to ENET2 and other SAI4 pins are simultaneously connected to XSPI1.

SAI5 is supported entirely on SD3 or entirely on XSPI1 (but not multiplexed across both XSPI1 and SD3 pins). SAI5 is also supported with some pins on SD3 and others on XSPI1, as long as the non-data signals (SYNCs and/or BCLKs) are on the one interface (SD3 or XSPI1), and all TX_DATA pins are on the one interface (SD3 or XSPI1), and all RX_DATA pins are on the one interface (SD3 or XSPI1).

SAI2 is supported entirely on ENET pins (at up to maximum supported speeds). However, the SAI2 on XSPI1 pins are limited to no more than 25 MHz – the faster 50 MHz Controller Tx and 66.67 MHz Target Rx modes are supported by the SAI2 only on ENET2 pins.

4.9.1.1 SAI/I2S Controller mode timing (50 MHz)

To achieve 50 MHz for BCLK operation, clock must be set in feedback mode and TCR2[BCI] = 1 must be configured to enable it for the transmitter.

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 44. SAI/I2S Controller mode timing (50 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SAI_MCLK cycle time	20	—	—	ns	—	—
S2	SAI_MCLK pulse width high/low	40%	—	60%	MCLK period	—	—
S3	SAI_BCLK cycle time	20	—	—	ns	—	—
S4	SAI_BCLK pulse width high/low	40%	—	60%	BCLK period	—	—
S5	SAI_BCLK to SAI_FS output valid	—	—	3	ns	—	—
S6	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—	—
S7	SAI_BCLK to SAI_TXD valid	—	—	3	ns	—	—

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Table 44. SAI/I2S Controller mode timing (50 MHz)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S8	SAI_BCLK to SAI_TXD invalid	-2	—	—	ns	—	—
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	3	—	—	ns	—	—
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—

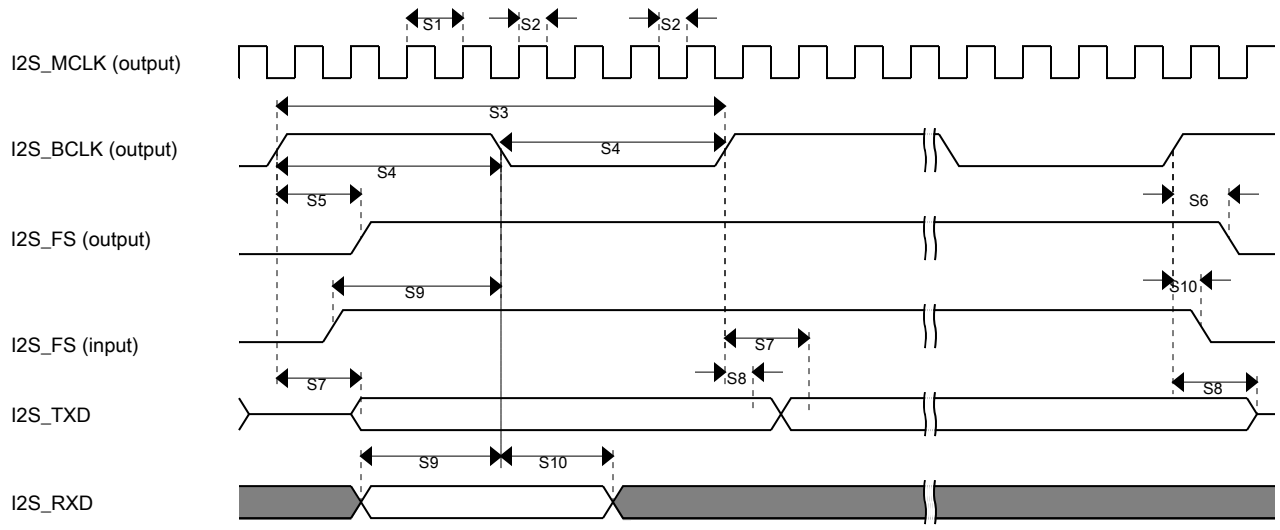


Figure 16. SAI timing-Controller modes

4.9.1.2 SAI/I2S Controller mode timing (25 MHz)

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 45. SAI/I2S Controller mode timing (25 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SAI_MCLK cycle time	40	—	—	ns	—	—
S2	SAI_MCLK pulse width high/low	40%	—	60%	MCLK period	—	—

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Table 45. SAI/I2S Controller mode timing (25 MHz)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S3	SAI_BCLK cycle time	40	—	—	ns	—	—
S4	SAI_BCLK pulse width high/low	40%	—	60%	BCLK period	—	—
S5	SAI_BCLK to SAI_FS output valid	—	—	3	ns	—	—
S6	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—	—
S7	SAI_BCLK to SAI_TXD valid	—	—	3	ns	—	—
S8	SAI_BCLK to SAI_TXD invalid	-2	—	—	ns	—	—
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK [1]	9.5	—	—	ns	—	—
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	—	ns	—	—

[1] SAI4 pins multiplexed over ENET2 when operating at 3.3 V I/O supply, this parameter value is 9.75 ns.

4.9.1.3 SAI/I2S Target mode timing (66 MHz)

To support 66 MHz for SAI Rx Target mode (input SAI Rx Clk, input SAI Rx Frame Sync, and input SAI Rx Data) for the following pins:

SAI2.RX_* pins multiplexed over ENET2

SAI5.RX_* pins multiplexed over SD3

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Table 46. SAI/I2S Target mode timing (66 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S11	SAI_BCLK cycle time (input)	15	—	—	ns	—	—
S12	SAI_BCLK pulse width high/low (input)	40%	—	60%	BCLK period	—	—
S13	SAI_FS input setup before SAI_BCLK	3	—	—	ns	—	—
S14	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—

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Table 46. SAI/I2S Target mode timing (66 MHz)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S17	SAI_RXD setup before SAI_BCLK	3	—	—	ns	—	—
S18	SAI_RXD hold after SAI_BCLK	2	—	—	ns	—	—

4.9.1.4 SAI/I2S Target mode timing (25 MHz)

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 47. SAI/I2S Target mode timing (25 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S11	SAI_BCLK cycle time (input)	40	—	—	ns	—	—
S12	SAI_BCLK pulse width high/low (input)	40%	—	60%	BCLK period	—	—
S13	SAI_FS input setup before SAI_BCLK	3	—	—	ns	—	—
S14	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid [1]	—	—	9.5	ns	—	—
S17	SAI_RXD setup before SAI_BCLK	3	—	—	ns	—	—
S18	SAI_RXD hold after SAI_BCLK	2	—	—	ns	—	—
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	—	ns	—	—
S19	SAI_FS input assertion to SAI_TXD output valid3 [2]	—	—	15	ns	—	—

[1] SAI4 pins multiplexed over ENET2 when operating at 3.3 V I/O supply, this parameter value is 9.75 ns.
[2] Applies to first bit in each frame and only if the TCR4[FSE] bit is clear.

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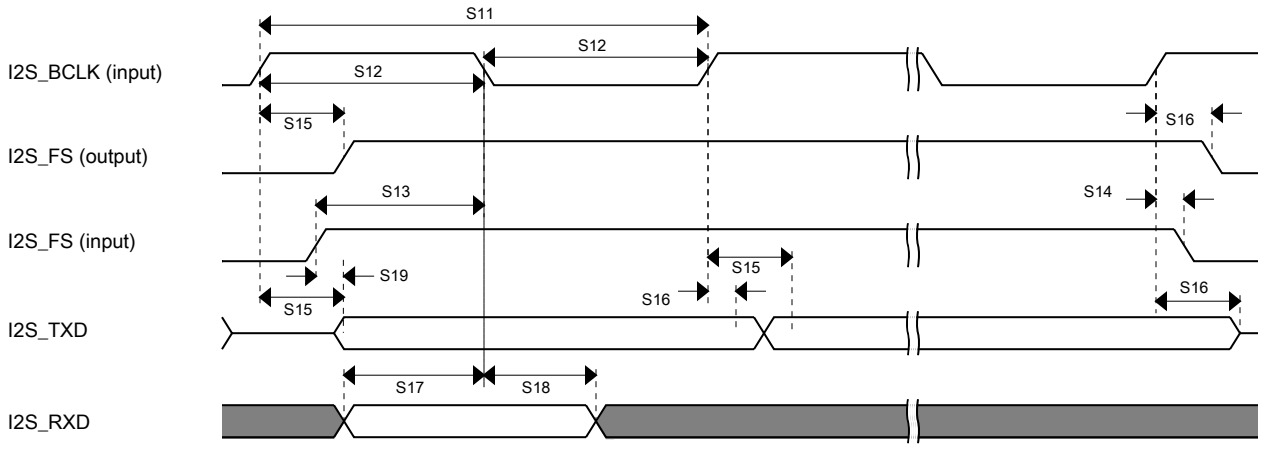


Figure 17. SAI timing-Target mode

4.9.1.5 SAI I/O specifications

Table 48. SAI I/O specifications

Mode	Pins	Clock	Frequency	Output	Input
Controller Tx	Any SAI interface multiplexes over ENET pins for a SAI instance is in NETCMIX. Any SAI interface does not multiplex over ENET pins for a SAI instance is not in NETCMIX.	TXC	50 MHz	TXD	—
		TXC	50 MHz	TXFS	—
	Any SAI interface multiplexes over ENET pins for a SAI instance is not in NETCMIX.	TXC	25 MHz	TXD	—
	Any SAI interface does not multiplex over ENET pins for a SAI instance is in NETCMIX.	TXC	25 MHz	TXFS	—
	Any	TXC	25 MHz	—	TXFS
Controller Rx	Any	RXC	25 MHz	—	RXD
		RXC	25 MHz	—	RXFS
		RXC	25 MHz	RXFS	—
	Any SAI interface multiplexes over ENET pins for a SAI instance is in NETCMIX. Any SAI interface does not multiplex over ENET pins	RXC Loopback Mode	50 MHz	—	RXD

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Table 48. SAI I/O specifications...*continued*

Mode	Pins	Clock	Frequency	Output	Input
	for a SAI instance is not in NETCMIX.	RXC Loopback Mode	50 MHz	—	RXFS
Target Tx	Any	TXC	25 MHz	TXD	—
		TXC	25 MHz	TXFS	—
		TXC	25 MHz	—	TXFS
Target Rx	SAI2 multiplexes over Ethernet pins, or (for SoCs supporting SAI5 and SD3), SAI5 multiplexes over SD3 pins.	RXC	66.7 MHz	—	RXD
		RXC	66.7 MHz	—	RXFS
		RXC	25 MHz	RXFS	—
	Any SAI instance or pinmux location is not mentioned above.	RXC	25 MHz	—	RXD
		RXC	25 MHz	—	RXFS
		RXC	25 MHz	RXFS	—

4.9.2 Pulse Width (PWM) timing parameters

This section describes the output timing parameters of the TPM.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

The following table lists the PWM timing parameters.

Table 49. Pulse Width (PWM) timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	PWM Module Clock Frequency	0	—	83.3	MHz	—	—
P1	PWM output pulse width high	12	—	—	ns	—	—
P2	PWM output pulse width low	12	—	—	ns	—	—

The following figure depicts the timing of the PWM.

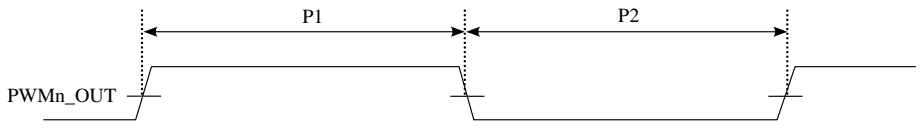


Figure 18. TPM timing

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4.9.3 Medium Quality Sound (MQS) electrical specifications

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. Two outputs are asynchronous PWM pulses and their maximum frequency is 1/32 x mclk_frequency.

Table 50. Medium Quality Sound (MQS) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fmclk	Bit clock is used to generate the mclk.	—	24.576	66.5	MHz	—	—

Frequency of mclk depends on software settings.

See Section, General purpose I/O AC parameters for other electrical specifications.

4.10 Display and graphics

This section introduces the timing and electrical parameters about display and graphic interfaces.

4.10.1 MIPI D-PHY electrical characteristics

The i.MX 952 processors conform to the MIPI CSI-2 and D-PHY standards for protocol and electrical specifications.

Compatible with standards:

- MIPI Alliance Specification for Display Serial Interface Version 1.2 (MIPI DSI controller)
- MIPI Standard 1.2 for D-PHY (MIPI DSI D-PHY)
- MIPI Alliance Standard for Camera Serial Interface 2 Version 2.1
- Conformance Test Suite for D-PHY v2.1 CTS Version 1.0

4.10.1.1 MIPI CSI-2

Table 51. MIPI CSI-2

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILEAK	Input pin leakage current	-100	—	100	uA	—	—
UIINST	HS UI Instantaneous	0.4	—	12.5	ns	—	—
VIL-LP	Input low voltage	—	—	550	mV	—	—
VIH-LP	Input high voltage	740	—	—	mV	Data rate > 1.5Gbps	—
VIH-LP	Input high voltage	880	—	—	mV	Data rate <= 1.5Gbps	—
VHYST	Input hysteresis	25	—	—	mV	—	—
VOL	Output low voltage level	-50	—	50	mV	—	—
VOH	Output high voltage level	1.1	—	1.3	V	Data rate <= 1.5Gbps	—
VOH	Output high voltage level	0.95	—	1.3	V	Data rate > 1.5Gbps	—

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Table 51. MIPI CSI-2*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIDTH	Differential input high voltage	—	—	70	mV	Data rate <= 1.5Gbps	—
VIDTH	Differential input high voltage	—	—	40	mV	Data rate > 1.5Gbps	—
VIDTL	Differential input low voltage	-40	—	—	mV	Data rate > 1.5Gbps	—
VIDTL	Differential input low voltage	-70	—	—	mV	Data rate <= 1.5Gbps	—
VIHHS	Single-ended input high voltage	—	—	460	mV	—	—
VILHS	Single-ended input low voltage	-40	—	—	mV	—	—
VCMRX_DC	Input common-mode voltage	70	—	330	mV	—	—
ZID	Differential input impedance	80	100	125	Ohm	—	—
VCMTX	HS transmitter static common-mode voltage	150	200	250	mV	(VP-VN)/2; Value when driven into a load impedance in the Zid range.	—
VOHHS	HS output high voltage	—	—	360	mV	Value when driven into a load impedance in the Zid range.	—
VOD	HS transmit absolute differential voltage	150	200	250	mV	—	—
eSPIKE	LP input pulse rejection	—	—	300	V.ps	Time-voltage integration of a voltage spike above VIL in LP-0 state, or below VIH in LP-1 state. Receiver does not change state if maximum pulse specification is met.	—
TMIN_RX	LP minimum input pulse	20	—	—	ns	Minimum pulse width recognized by the receiver.	—
VINT	LP peak interference voltage	—	—	200	mV	—	—
fINT	LP interference frequency	450	—	—	MHz	—	—

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Table 51. MIPI CSI-2*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tflp, Tflp	LP 15%-85% signal rise/fall time	—	—	25	ns	—	—
tslew	Output slew rate	—	—	150	mV/ns	@CLOAD = 70pF	—
tslew_fall	Output slew rate (falling edge)	25	—	—	mV/ns	@CLOAD = 0pF - 70pF	—
tslew_rise	Output slew rate (rising edge)	25	—	—	mV/ns	@CLOAD = 0pF - 70pF	—
CLOAD	Output load capacitance	—	—	70	pF	—	—
TSETUP	Data to clock setup time	0.15	—	—	UIINST	> 0.08Gbps, <= 1Gbps	—
TSETUP	Data to clock setup time	0.2	—	—	UIINST	> 1Gbps, <= 1.5Gbps	—
THOLD	Clock to data hold time	0.15	—	—	UIINST	> 0.08Gbps, <= 1Gbps	—
THOLD	Clock to data hold time	0.2	—	—	UIINST	> 1Gbps, <= 1.5Gbps	—
ΔVCMRX(HF)	HS common mode interference beyond 450 MHz	—	—	50	mV	Data rate > 1.5Gbps	—
ΔVCMRX(LF)	HS common mode interference between 50MHz and 450 MHz	-25	—	25	mV	Data rate > 1.5Gbps	—
RATE[RX]	Receive Serial Data Rate	80	—	2500	Mbps	80 Ω ≤ RL ≤ 125 Ω	—
RATE[TX]	Transmit Serial Data Rate	80	—	2500	Mbps	per lane, 80 Ω ≤ RL ≤ 125 Ω	—
TCLKP	HS Clock Period	0.8	—	25	ns	80 Ω ≤ RL ≤ 125 Ω	—
TSKEW[TX]	Data to clock skew	-0.15	—	0.15	UIinst	> 0.08Gbps, < 1Gbps	—
TSKEW[TX]	Data to clock skew	-0.2	—	0.2	UIinst	> 1Gbps, < 1.5Gbps	—
TSKEW[TLIS]	Data to clock skew	-0.2	—	0.2	UIinst	> 0.08Gbps, < 1Gbps	—
TSKEW[TLIS]	Data to clock skew	-0.1	—	0.1	UIinst	> 1Gbps, < 1.5Gbps	—
TSKEW[TX] static	Static data to clock skew (TX)	-0.2	—	0.2	UIinst	> 1.5Gbps	—
TSKEW[TLIS] static	Static data to clock skew (channel)	-0.1	—	0.1	UIinst	> 1.5Gbps	—

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Table 51. MIPI CSI-2*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TSKEW[RX] static	Static data to clock skew (RX) tolerance	-0.3	—	0.3	UIinst	> 1.5Gbps, < 2.5Gbps	—
TSKEW[TX] dynamic	Dynamic data to clock skew	-0.15	—	0.15	UIinst	> 1.5Gbps	—
TSKEWCAL initial	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	—	—	100	us	> 1.5Gbps	—
TSKEWCAL initial	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	2^15	—	—	UIinst	> 1.5Gbps	—
TSKEWCAL periodic	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	—	—	10	us	> 1.5Gbps	—
TSKEWCAL periodic	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	2^15	—	—	UIinst	> 1.5Gbps	—
ΔVCMTX(HF)	Common mode variations above 450 MHz	—	—	15	mV(RMS)	—	—
ΔVCMTX(LF)	Common mode variations between 50MHz - 450 MHz	—	—	25	mV(RMS)	—	—
Tssc_mod_rate	Modulation Rate	30	31.5	33	kHz	Measured per MIPI D-PHY CTS v2.1 Test 1.4.19	—
Tssc_freq_dev	SSC Deviation	-5000	—	0	ppm	Measured per MIPI D-PHY CTS v2.1 Test 1.4.19 (down spread only).	—

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Table 51. MIPI CSI-2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SSC df/dt	SSC df/dt	—	—	1250	ppm/us	Measured per MIPI D-PHY CTS v2.1 Test 1.4.19.	—
trise_fall	20% - 80% rise and fall time	100	—	—	ps	Data rate <= 1.5Gbps	—
trise_fall	20% - 80% rise and fall time	—	—	0.4	UI	Data rate > 1.5Gbps	—
trise_fall	20% - 80% rise and fall time	50	—	—	ps	Data rate > 1.5Gbps	—

4.11 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 uSDHC DC electrical characteristics (NVCC_xxx = 1.8V)

For recommended operating conditions, see Recommended Operating Conditions.

Table 52. uSDHC DC electrical characteristics (NVCC_xxx = 1.8V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage. [1]	0.7 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1]	—	—	0.3 x NVCC_xxx	V	—	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	uA	—	—
VOH	Output high voltage (IOH = -2mA at NVCC_xxx min)	NVCC_xxx - 0.45	—	—	V	—	—
VOL	Output low voltage (IOL = 2mA at NVCC_xxx min)	—	—	0.45	V	—	—

[1] The min VIL and max VI values are based on the respective min and max VDD values found in Recommended Operating Conditions

4.11.2 uSDHC DC electrical characteristics (NVCC_xxx = 3.3V)

For recommended operating conditions, see Recommended Operating Conditions.

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Table 53. uSDHC DC electrical characteristics (NVCC_xxx = 3.3V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage [1]	0.625 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1]	—	—	0.25 x NVCC_xxx	V	—	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	uA	—	—
VOH	Output high voltage (IOH = -2mA at NVCC_xxx min)	0.75 x NVCC_xxx	—	—	V	—	—
VOL	Output low voltage (IOL = 2mA at NVCC_xxx min)	—	—	0.125 x NVCC_xxx	V	—	—

[1] The min VIL and max VI values are based on the respective min and max VDD values found in Recommended Operating Conditions.

4.11.3 uSDHC SDR HS 200 AC timing - Nominal and Overdrive mode

Table 54. uSDHC SDR HS 200 AC timing - Nominal and Overdrive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	200	MHz	—	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	1	ns	—	—
—	Duty Cycle Distortion	—	—	0.3	ns	—	—
tNIKHOX	Controller output hold time (ns)	1.4	—	—	ns	—	—
tNIKHOV	Controller output delay (ns)	—	—	3.1	ns	—	—
tIDV	Input data window (UI)	0.475	—	—	UI	—	—

4.11.4 uSDHC SDR HS 200 AC timing - Low drive mode

Table 55. uSDHC SDR HS 200 AC timing - Low drive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	133	MHz	—	—

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Table 55. uSDHC SDR HS 200 AC timing - Low drive mode...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRISE/tFALL	Clk Rise/Fall Time (ns)	—	—	1.5	ns	—	—
—	Duty Cycle Distortion	—	—	0.45	ns	—	—
tNIKHOX	Controller output hold time (ns)	1.4	—	—	ns	—	—
tNIKHOV	Controller output delay (ns)	—	—	5	ns	—	—
tIDV	Input data window (UI)	0.475	—	—	UI	—	—

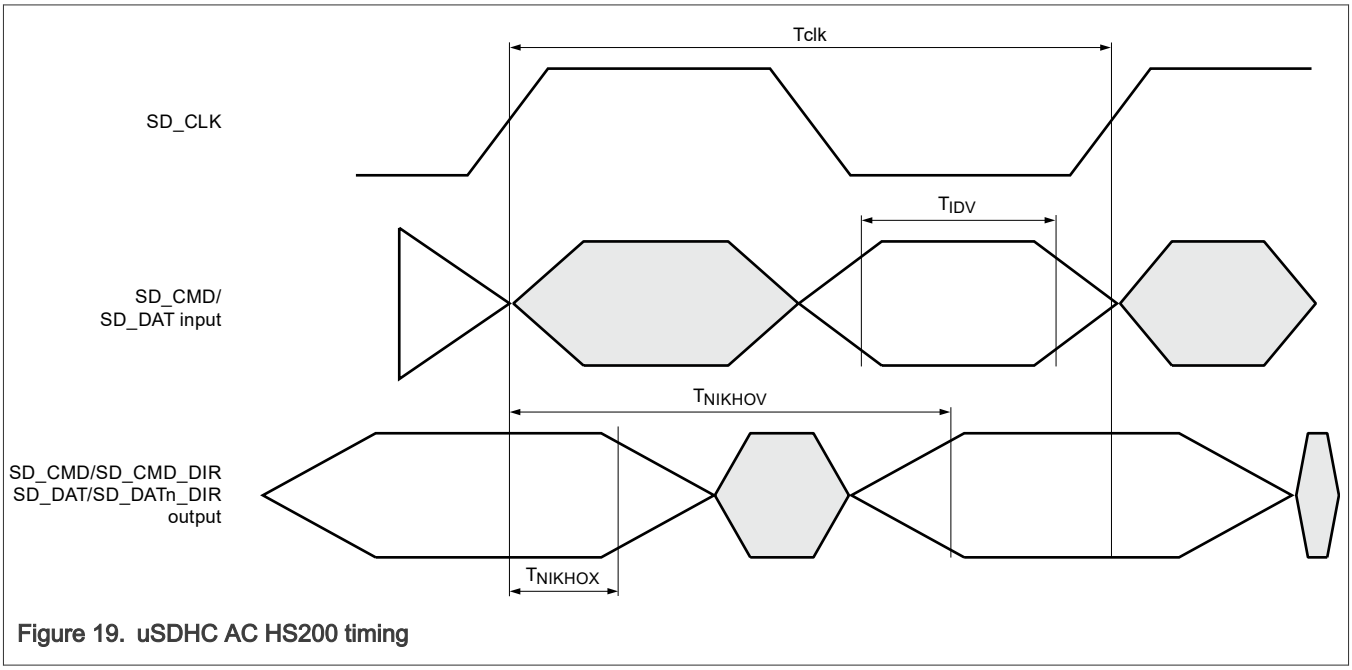


Figure 19. uSDHC AC HS200 timing

4.11.5 uSDHC DDR HS 400 AC timing - Nominal and Overdrive mode

Table 56. uSDHC DDR HS 400 AC timing - Nominal and Overdrive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	200	MHz	—	—
—	Duty Cycle distortion	0	—	0.3	ns	—	—
tCL	Clock low time	2.2	—	—	ns	—	—
tCH	Clock high time	2.2	—	—	ns	—	—

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Table 56. uSDHC DDR HS 400 AC timing - Nominal and Overdrive mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSHKHOX	Controller output hold time (ns)	0.6	—	—	ns	—	—
tSHKHOV	Controller output delay (ns)	—	—	1.85	ns	—	—
tSHRQV	Data valid skew to DQS [1]	—	—	0.75	ns	—	—
tSHRQHX	Data hold skew to DQS [1]	—	—	0.75	ns	—	—
tSHRQV_CMD	Commad valid skew to DQS [1]	—	—	0.75	ns	—	—
tSHRQHX_CMD	Command hold skew to DQS [1]	—	—	0.75	ns	—	—
tSHDSPWS	DQS pulse width (ns)	1.9	—	—	ns	—	—
—	DQS Duty Cycle distortion	—	—	0.3	ns	—	—

[1] Board skew margin between DQS and DATA/CMD is considered as +/-50 ps in calculations

4.11.6 uSDHC DDR HS 400 AC timing - Low drive mode

Table 57. uSDHC DDR HS 400 AC timing - Low drive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	133	MHz	—	—
—	Duty Cycle distortion	—	—	0.45	ns	—	—
tCL	Clock low time	3.3	—	—	ns	—	—
tCH	Clock high time	3.3	—	—	ns	—	—
tSHKHOX	Controller output hold time (ns)	0.8	—	—	ns	—	—
tSHKHOV	Controller output delay (ns)	—	—	2.95	ns	—	—
tSHRQV	Data valid skew to DQS	—	—	0.8	ns	—	—
tSHRQHX	Data hold skew to DQS	—	—	0.8	ns	—	—
tSHRQV_CMD	Command valid skew to DQS	—	—	0.8	ns	—	—

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Table 57. uSDHC DDR HS 400 AC timing - Low drive mode...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSHRQHX_CMD	Command hold skew to DQS	—	—	0.8	ns	—	—
tSHDSPWS	DQS pulse width (ns)	2.9	—	—	ns	—	—

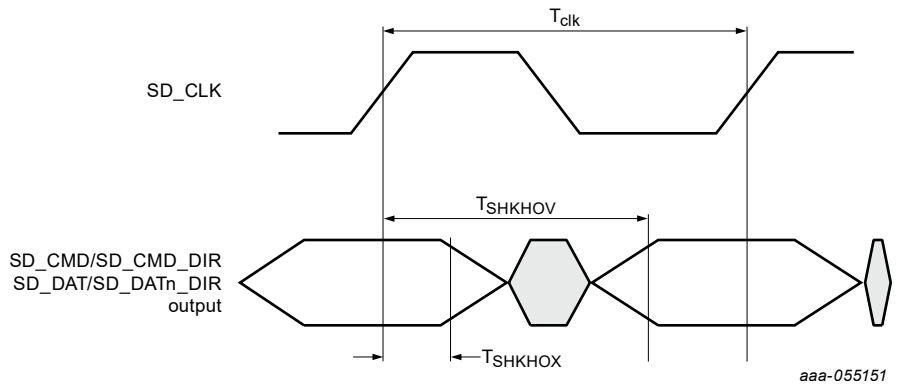


Figure 20. uSDHC AC HS400 timing

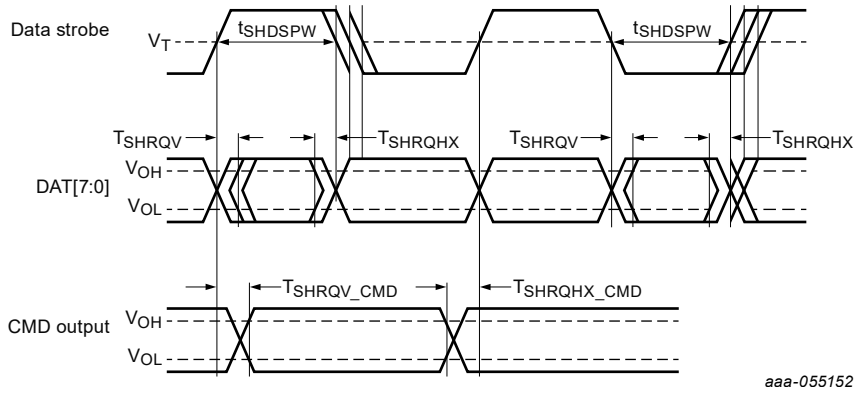


Figure 21. uSDHC AC HS400 timing 1

4.11.7 uSDHC AC SDR104 - Nominal and Overdrive mode

Table 58. uSDHC AC SDR104 - Nominal and Overdrive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	200	MHz	—	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	1	ns	—	—
—	Duty Cycle distortion	—	—	0.3	ns	—	—

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Table 58. uSDHC AC SDR104 - Nominal and Overdrive mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tNIKHOX	Controller output hold time (ns)	1.2	—	—	ns	—	—
tNIKHOV	Controller output delay (ns)	—	—	3.1	ns	—	—
tIDV	Input data window (UI)	0.5	—	—	UI	—	—

4.11.8 uSDHC AC SDR104 - Low drive mode

Table 59. uSDHC AC SDR104 - Low drive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	133	MHz	—	—
tRISE/tFALL	Clk Rise/Fall Time (ns)	—	—	1	ns	—	—
—	Duty cycle distortion	—	—	0.45	ns	—	—
tNIKHOX	Controller output hold time (ns)	1.35	—	—	ns	—	—
tNIKHOV	Controller output delay (ns)	—	—	5	ns	—	—
tIDV	Input data window (UI)	0.5	—	—	UI	—	—

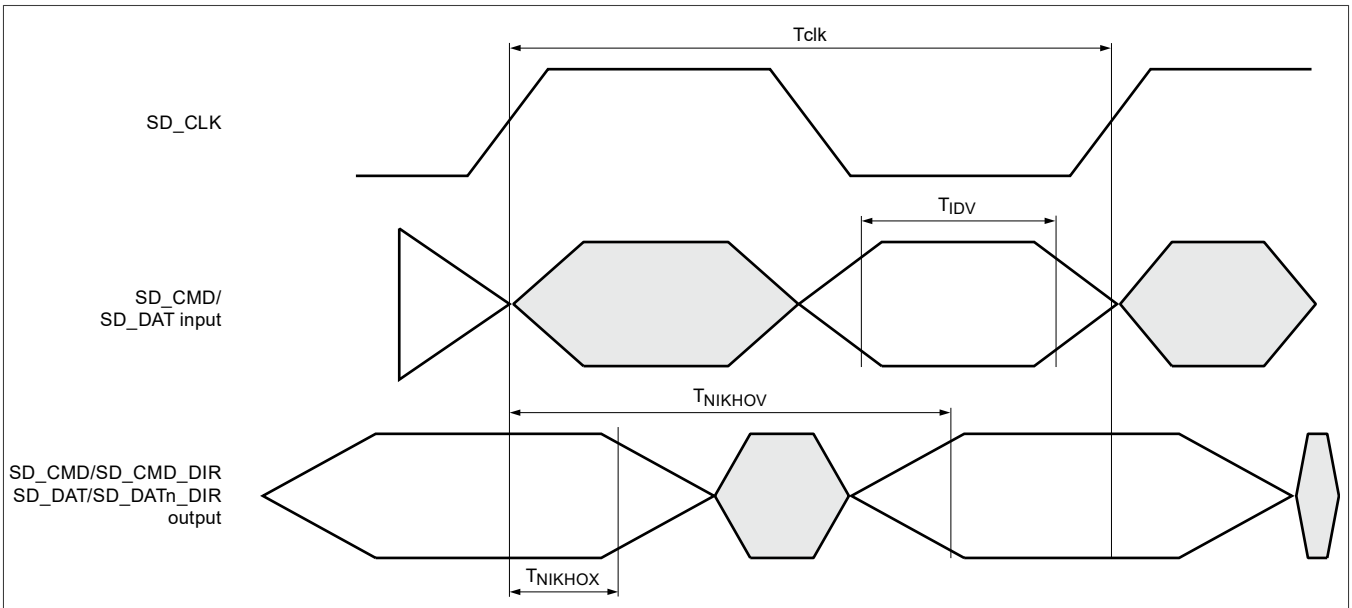


Figure 22. uSDHC AC SDR104 timing

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4.11.9 uSDHC AC SDR50 - Nominal and Overdrive mode

Table 60. uSDHC AC SDR50 - Nominal and Overdrive mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	100	MHz	—	—
tRISE/FALL	Clk Rise/Fall Time (ns)	—	—	2	ns	—	—
—	Duty Cycle distortion	—	—	0.3	ns	—	—
tNIKHOX	Controller output hold time (ns)	1.2	—	—	ns	—	—
tNIKHOV	Controller output delay (ns)	—	—	6.6	ns	—	—
tNDIVKH	Input setup Time for SD_DATn (ns)	2.1	—	—	ns	—	—
tNDIXKH	Input Hold Time for SD_DATn (ns)	1.5	—	—	ns	—	—

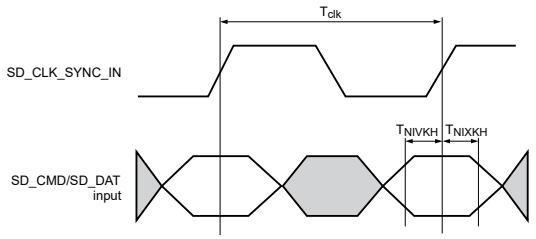


Figure 23. uSDHC AC SDR50 timing

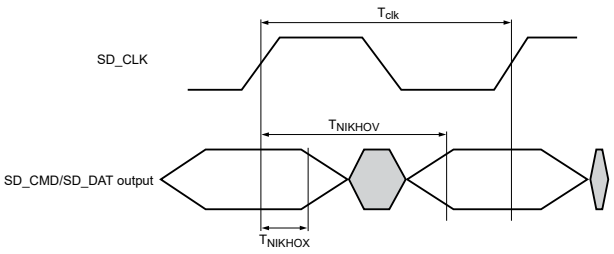


Figure 24. uSDHC AC SDR50 timing 2

4.11.10 uSDHC supported modes

For SD:

- All SD 3.0 protocols are supported at full speeds on all three SDHC interfaces. This includes DS, HS, SDR12, SDR25, SDR50, SDR104, and DDR50.
- The maximum supported SDR frequency is 200 MHz which is covered in SDR104 mode, and maximum DDR frequency is 50 MHz as a part of DDR50 mode.

For eMMC:

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- eMMC HS400 is only supported on SDHC1 as that is the only one with 8-bit interface.
- eMMC HS200 is supported on all three SDHC interfaces because this protocol supports both 4-bit mode and 8-bit mode, which can work on SDHC2 and SDHC3.
- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are also supported on all three SDHC interfaces.
- The maximum supported SDR frequency is 200 MHz which is covered in HS200 mode, and the maximum DDR frequency is 200 MHz as a part of HS400 mode.

uSDHC3 is multiplexing on GPIO_IO[27:22], below are the modes which are targeted:

- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are supported.
- SDR50 (100 MHz) and SDR104 (200 MHz) modes are NOT supported.
- eMMC HS400 and HS200 modes are NOT supported
- The maximum supported SDR and DDR frequency is 50 and 52 MHz

If I/O is supplied by 3.3 V, the maximum supported SDR/DDR frequency is 50/52 MHz

4.11.11 uSDHC AC DDR

Table 61. uSDHC AC DDR

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	eMMC High Speed DDR 1.8v	—	—	52	MHz	—	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	3	ns	—	—
—	Duty Cycle distortion	45	—	55	%	—	—
tNDKHOX	Controller output hold time for SD_DATn (ns)	3	—	—	ns	—	—
tNDKHOV	Controller output delay for SD_DATn (ns)	—	—	6.5	ns	—	—
tNDIVKH	Input setup Time for SD_DATn (ns)	2	—	—	ns	—	—
tNDIXKH	Input Hold Time for SD_DATn (ns)	1.5	—	—	ns	—	—
tNIKHOX	Controller output hold time for SD_CMD (ns)	3.7	—	—	ns	—	—
tNIKHOV	Controller output delay for SD_CMD (ns)	—	—	13	ns	—	—
tNIIVKH	Input setup Time for SD_CMD (ns)	5	—	—	ns	—	—
tNIIXKH	Input Hold Time for SD_CMD (ns)	1.5	—	—	ns	—	—

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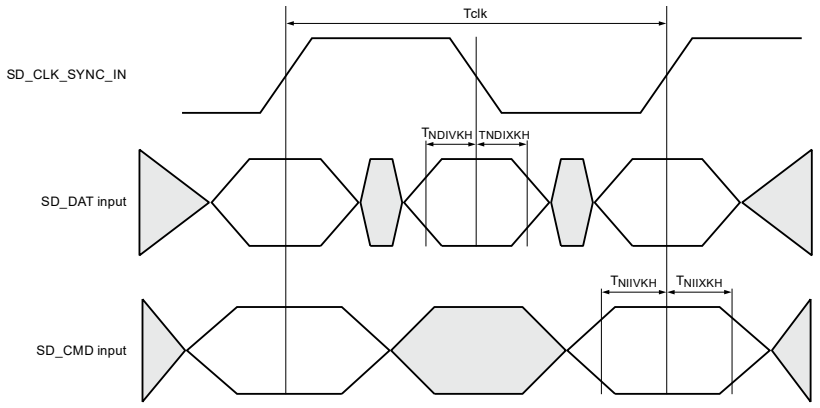


Figure 25. uSDHC AC DDR timing 1

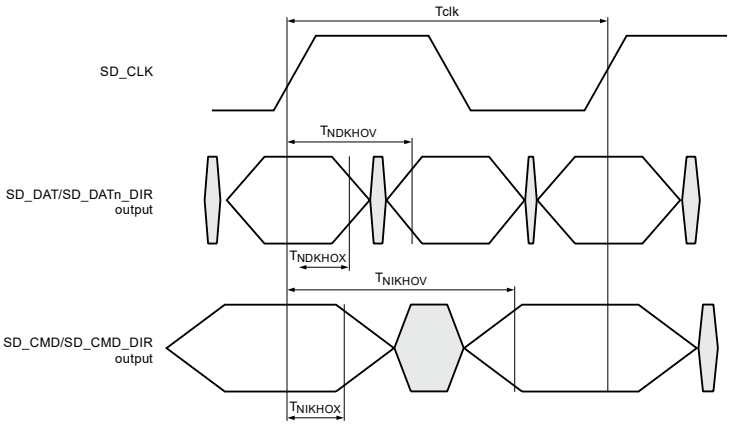


Figure 26. uSDHC AC DDR timing 2

4.11.12 uSDHC AC HS

Table 62. uSDHC AC HS

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	eMMC Low Speed 1.8V/3.3V	—	—	50	KHz	—	—
—	eMMC Full Speed/ High Speed 1.8v/ 3.3V	—	—	26/52	MHz	—	—
—	SD/SDIO SDR12/ SDR25 1.8V	—	—	25/50	MHz	—	—
—	SD/SDIO Identification Mode 3.3V	—	—	400	KHz	—	—

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Table 62. uSDHC AC HS*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	SD/SDIO Default Speed/High Speed 3.3V	—	—	25/50	MHz	—	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	2	ns	—	—
—	Duty Cycle distortion	45	—	55	%	—	—
tNIKHOX	Controller output hold time (ns)	3.7	—	—	ns	—	—
tNIKHOV	Controller output delay (ns)	—	—	12.8	ns	—	—
tNIIVKH	Input setup Time (ns)	2.8	—	—	ns	—	—
tNIIXKH	Input Hold Time (ns)	1.5	—	—	ns	—	—

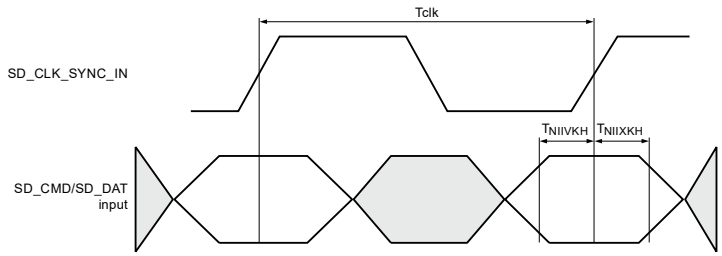


Figure 27. uSDHC AC HS timing

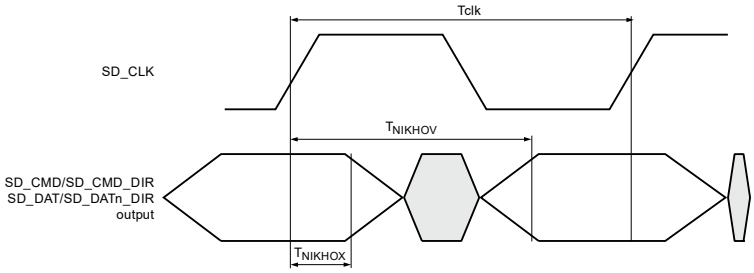


Figure 28. uSDHC AC HS timing 1

4.12 Ethernet controller (ENET)

Ethernet supports the following key features:

- Support ENET AVB
- Support IEEE 1588
- Support Energy Efficient Ethernet (EEE)
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation, 1G SGMII

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The following sections describe the DC and AC electrical characteristics for the EMI, RMII, RGMII, and IEEE standard 1588 interfaces.

4.12.1 Ethernet Management Interface (EMI)

This section describes the electical characteristics for the EMI interface.

4.12.1.1 Ethernet management interface AC Timing specifications

This table describes the EMI AC timing specifications

Table 63. Ethernet management interface AC Timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fMDC	Clock frequency [1]	2.5	5	10	MHz	—	—
tMGCH	MDC clock pulse width high	40	—	60	%	—	—
tMGCL	MDC clock pulse width low	40	—	60	%	—	—
tMDKHDX	MDC to MDIO output delay [2][3]	Y x tENET_CLK - 3	—	Y x tENET_CLK + 8	—	NEG=0	—
tMDKHDX	MDC to MDIO output delay [2][3][4]	Y x 0.5 * tENET_CLK - 3	—	Y x 0.5 * tENET_CLK + 8	—	NEG=1	—
tMDDVKH	MDIO to MDC input setup time [5]	8	—	—	ns	—	—
tMDDXKH	MDIO to MDC input hold time	0	—	—	ns	—	—

[1] This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the MDC clock frequency.
[2] tENET_CLK = 333 Mhz max.
[3] MDIO timing is configurable by programming the EMDIO_CFG register fields. The default value of Y = 5. Y is the value determined by EMDIO_CFG[NEG], EMDIO_CFG[MDIO_HOLD], and MDIO[EHOLD]. The easiest way is to program NEG=1, then MDIO is driven at negative edge of MDC, satisfying both setup and hold time requirement of Ethernet PHY.
[4] For NEG=0: Y = (1+(2+6*EHOLD)*MDIO_HOLD) For NEG=1: Y= (0.5 *MDIO_CLK_DIV)
[5] The setup time tMDDVKH is measured at a) 470pf load @ 1.8V in open-drain mode b) 300pf load @ 1.8V in push-pull mode

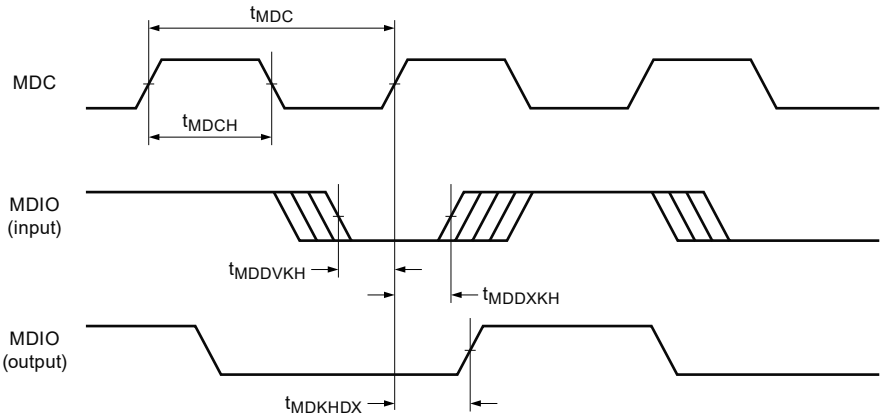


Figure 29. Ethernet management interface timing diagram

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4.12.1.2 Ethernet management interface DC electrical characteristics at voltage rail =1.8V

This table provides the EMI DC electrical characteristics

Table 64. Ethernet management interface DC electrical characteristics at voltage rail =1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	0.7 x SUPPLY	—	—	V	—	—
VIL	Input low voltage	—	—	0.3 x SUPPLY	V	—	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±50	µA	—	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—	—

4.12.2 RGMII interface

This section describe the electrical characteristics for the RGMII interface.

4.12.2.1 RGMII AC Timing Specifications

Timing is valid for RGMII unless stated otherwise.

Table 65. RGMII AC Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSKRGTTX	Data to clock output skew (at transmitter) [1]	-500	0	500	ps	—	—
tSKRGTRX	Data to clock input skew (at receiver) [2]	1	—	2.6	ns	—	—
tRGT	Clock period duration [3]	7.2	8	8.8	ns	—	—
tRGTHtRGT	Duty cycle for 10BASE-T and 100BASE-TX [3][4]	40	50	60	%	—	—
tRGTHtRGTgig	Duty cycle for Gigabit	45	60	55	%	—	—
tRGTR-HP	Rise time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	0.75	ns	—	—

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Table 65. RGMII AC Timing Specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRGTR-OpenAlliance	Rise time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	1	ns	—	—
tRGTF-HP	Fall time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	0.75	ns	—	—
tRGTF-OpenAlliance	Fall time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	1	ns	—	—

[1] The frequency of RGMII input clk should not exceed the frequency of RGMII output clk by more than 300 ppm.
[2] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
[3] For 10 and 100 Mbps, tRGT scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
[4] Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.
[5] Applies to inputs and outputs.
[6] The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

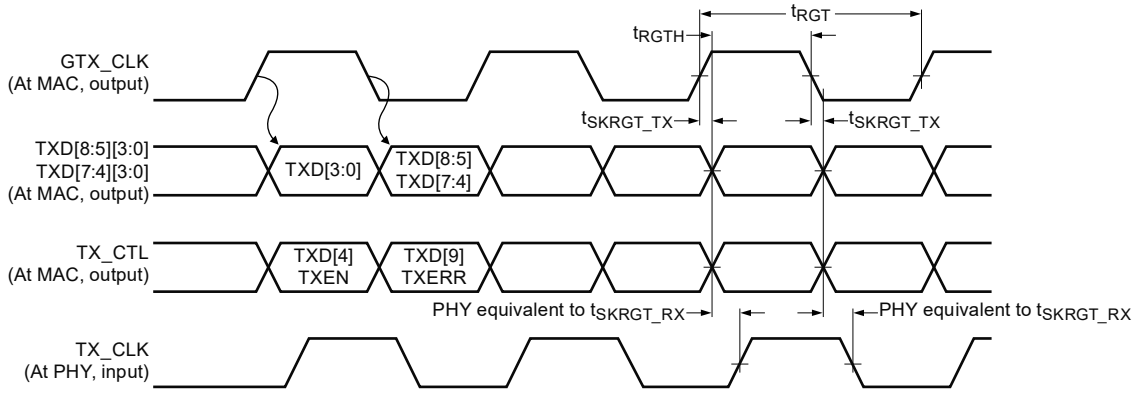


Figure 30. AC Transmit timing and multiplexing diagrams

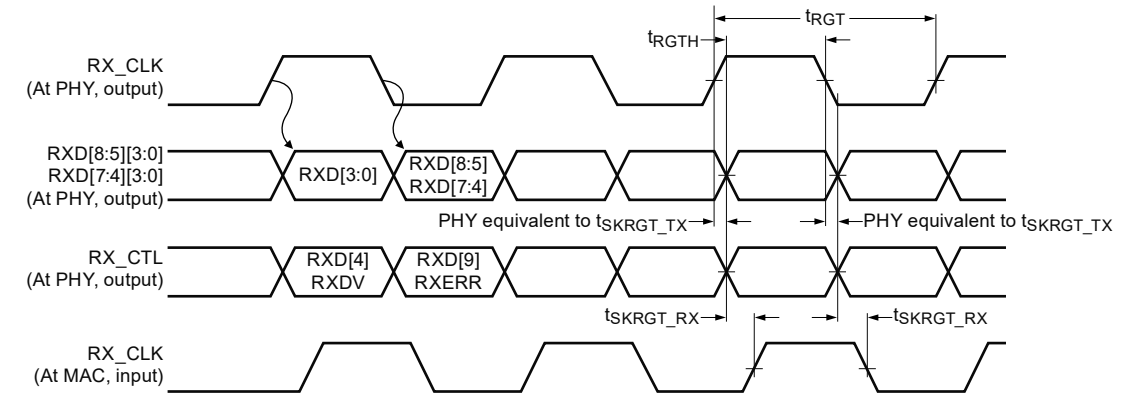


Figure 31. Receive timing and multiplexing diagram

4.12.2.2 RGMII Electrical Characteristics at (voltage rail) = 1.8V

The timings assume the following configuration: CTL[5:0] = 001111 and SL[1:0] = 11. Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a

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10 pF load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (15 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver. RGMII timing specifications are only valid for 1.8 V nominal I/O pad supply voltage. The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver device

Timing is valid for RGMII unless stated otherwise.

Table 66. RGMII Electrical Characteristics at (voltage rail) = 1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage [1]	0.7 x SUPPLY	—	—	V	—
VIL	Input low voltage [1]	—	—	0.3 x SUPPLY	V	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN) [2]	—	—	±50	µA	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA) [2]	SUPPLY - 0.2	—	—	V	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA) [2]	—	—	0.2	V	—

[1] The min VIL and max VIH values are based on the respective min and max (supply) values found in Recommended Operating Conditions.
[2] The symbol (supply) represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

4.12.3 RMII

This section describes the electrical characteristics for the RMII interface.

4.12.3.1 RMII AC Timing Specifications

Timing is valid for RMII unless stated otherwise.

Table 67. RMII AC Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRMT	TX Clock period duration	15	20	25	ns	—	—
tRMTH	TX Clock Duty cycle for 10BASE-T and 100BASE-TX	35	50	65	%	—	—
tRMTR	TX Rise time (20%-80%)	1	—	5	ns	—	—
tRGTF	TX Fall time (20%-80%)	1	—	5	ns	—	—
tRMTJ	TX Clock peak-to-peak jitter	—	—	250	ps	—	—
tRMTDX	TX Clock to Data/ TX_EN Delay	2	—	14	ns	—	—

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Table 67. RMII AC Timing Specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRMRDV	RXD/CRS_DV/ RXER to Clock rising edge, setup time	4	—	—	ns	—	—
tRMRDX	Clock rising edge to RXD/CRS_DV/ RXER, hold time	2	—	—	ns	—	—

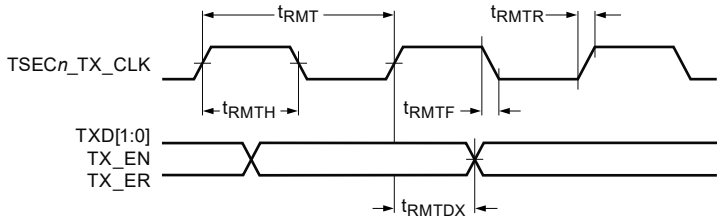


Figure 32. Transmit AC timing diagram

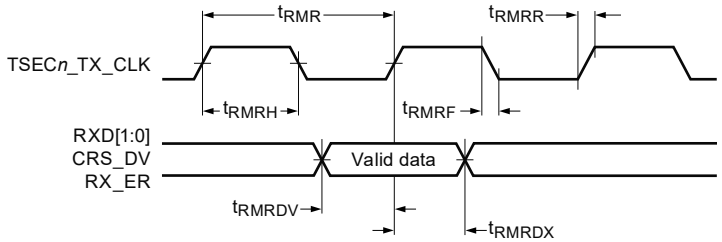


Figure 33. Receive AC timing diagram

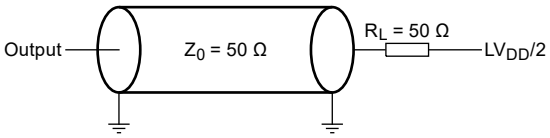


Figure 34. eTSEC AC Test Load

4.12.3.2 RMII DC Electrical Characteristics at voltage rail = 3.3V

Timing is valid for RMII unless stated otherwise.

Table 68. RMII DC Electrical Characteristics at voltage rail = 3.3V

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	2	—	—	V	—	—
VIL	Input low voltage	—	—	0.8	V	—	—

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Table 68. RMII DC Electrical Characteristics at voltage rail = 3.3V*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±5	µA	—	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—	—

4.12.3.3 RMII DC Electrical Characteristics at voltage rail =1.8V

Timing is valid for RMII unless stated otherwise.

Table 69. RMII DC Electrical Characteristics at voltage rail =1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	0.7 x SUPPLY	—	—	V	—	—
VIL	Input low voltage	—	—	0.3 x SUPPLY	V	—	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±50	µA	—	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—	—

4.12.4 IEEE1588 interface

The following table describes the IEEE Std 1588 electrical characteristics.

Table 70. IEEE1588 interface

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tT1588CLK	TMR_1588_CLK_IN clock period	5	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—

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Table 70. IEEE1588 interface*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tT1588CLKH/ tT1588CLK	TMR_1588_CLK_IN duty cycle	40	50	60	%	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKINJ	TMR_1588_CLK_IN peak-to-peak jitter	—	—	250	ps	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKINR	Rise time TMR_1588_CLK_IN (20% to 80%)	1.0	—	2.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKINF	Fall time TMR_1588_CLK_IN (80% to 20%)	1.0	—	2.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKOUT	TMR_1588_CLK_OUT clock period	—	2 x t1588CLK	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKOTH/ tT1588CLKOUT	TMR_1588_CLK_OUT duty cycle	30.0	50.0	70.0	%	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588OV	TMR_1588_CLK_OUT to TMR_1588_PULSE_OUT1/2,TMR_1588_ALARM_OUT1/2 valid	0.5	—	4.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588TRIGH	TMR_1588_TRIG_IN 1/2 pulse width	2 x t1588CLK	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

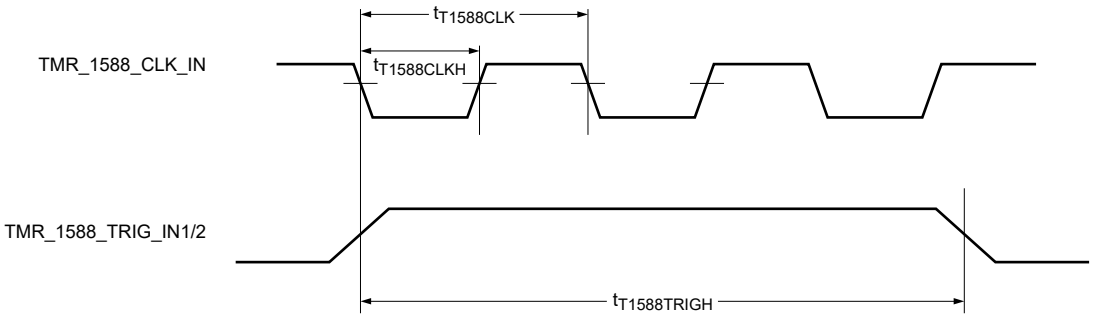
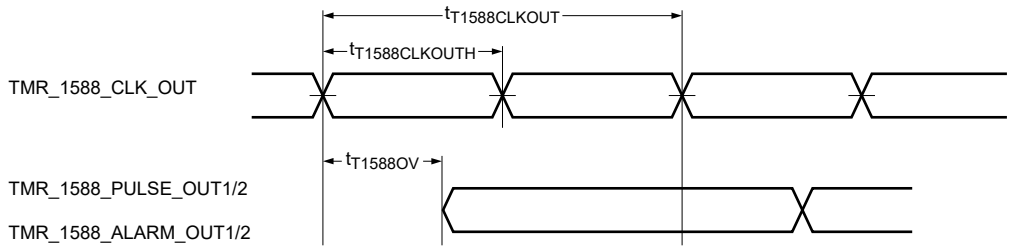


Figure 35. IEEE 1588 input AC timing

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Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 36. IEEE 1588 output AC timing

4.12.5 SGMII

SGMII electrical specifications will be compatible with the 1000Base-KX electrical specifications based on IEEE802.3 Clause 70.7.

4.12.6 1000Base-KX

1000Base-KX Electricals are compatible with Electrical Specifications as defined in IEEE 802.3, Clause 70 and is intended for Backplane Applications

Table 71. 1000Base-KX

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval (mean)	799.92	800	800.08	ps	—	—
CTX	AC Coupling Capacitor	—	100	—	nF	—	—
REXT	External Reference Resistor (RESREF) [1]	—	200	—	Ohms	—	—

[1] REXT requires 1% 100ppm/C precision resistor-to-ground on PC Board.

4.12.6.1 1000Base-KX Transmitter DC Specifications

Table 72. 1000Base-KX Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDIFF_PK-PK	Differential peak-to-peak output voltage	800	—	1600	mV	—	—

4.12.6.2 1000Base-KX Receiver DC Specifications

Table 73. 1000Base-KX Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VINdiffpk-pk	Differential Input Pk-Pk amplitude	—	—	1600	mV	—	—

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4.12.6.3 1000Base-KX Transmitter AC Specifications

Table 74. 1000Base-KX Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Trise_fall_typ	Transition Time (20% - 80%) [1]	—	25	—	ps	—	—
Dj	Deterministic Jitter (Max pk-pk)	—	—	0.1	UI	—	—
Rj	Random jitter	—	—	0.15	UI	—	—
Tj	Total jitter (Max pk-pk at BER 1E-12)	—	—	0.25	UI	—	—
TEYE-X1	TX Eye Mask X1 Time at 0mV Differential Amplitude	—	—	0.125	UI	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—
TEYE-X2	TX Eye Mask X2 Time at +/-A1 Differential Amplitude	—	—	0.325	UI	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—
TEYE-A2	TX Eye Mask A2 Differential Amplitude overall UI	-800	—	800	mV	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—
TEYE-A1	TX Eye Mask A1 Differential Amplitude at X2 UI	-400	—	400	mV	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—

[1] Trise_fall is faster than specified.

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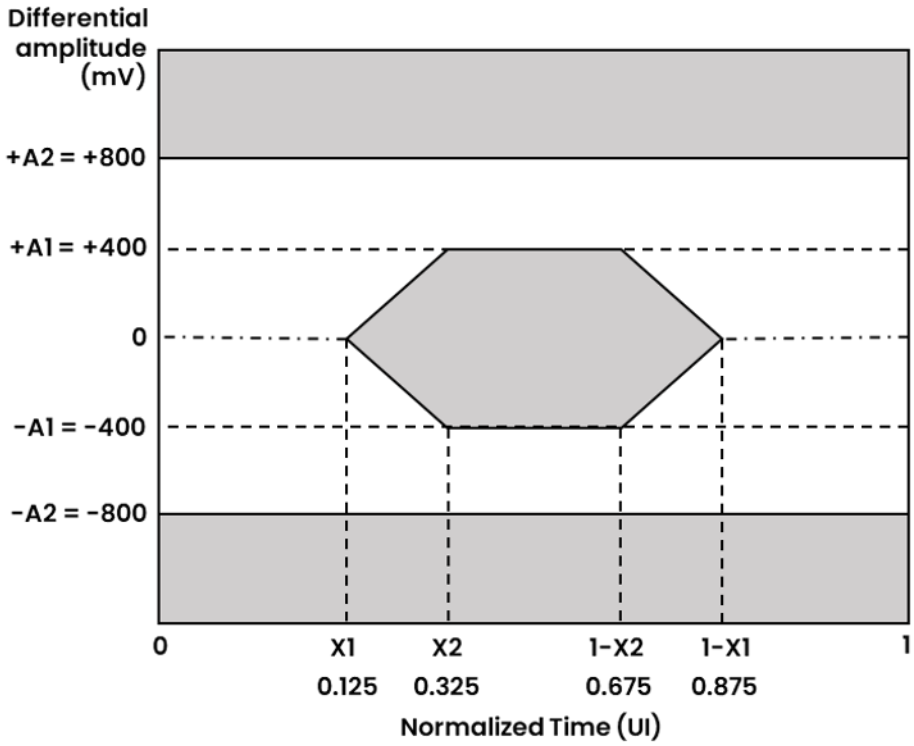


Figure 37. Eye Mask TP1

4.12.7 Ethernet reference clock

Tie any reference clock inputs that are not used to ground.

4.13 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and target operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% VDD and 80% VDD thresholds, unless noted, as well as input signal transitions of 3 ns and a 25 pF maximum load on all LPSPI pins.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.13.1 LPSPI DC electrical characteristics

Table 75. LPSPI DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage [1] [2]	0.7 x NVCC_xx	—	—	V	—	—
VIL	Input low voltage [1] [2]	—	—	0.3 x NVCC_xx	V	—	—

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Table 75. LPSPI DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIN/IOZ	Input/Output leakage current [1]	-5	—	5	µA	—	—
VOH	Output high voltage [1]	NVCC_xxx - 0.45	—	—	V	IOH = -2 mA at NVCC_xxx min	—
VOL	Output low voltage [1]	—	—	0.45	V	IOL = 2 mA at NVCC_xxx min	—

[1] For recommended operating conditions, see Recommended Operating Conditions.
[2] The minimum VIL and maximum VI values are based on the respective minimum and maximum VDD values found in Recommended Operating Conditions.

4.13.2 LPSPI Controller mode AC timing specifications

Table 76. LPSPI Controller mode AC timing specifications

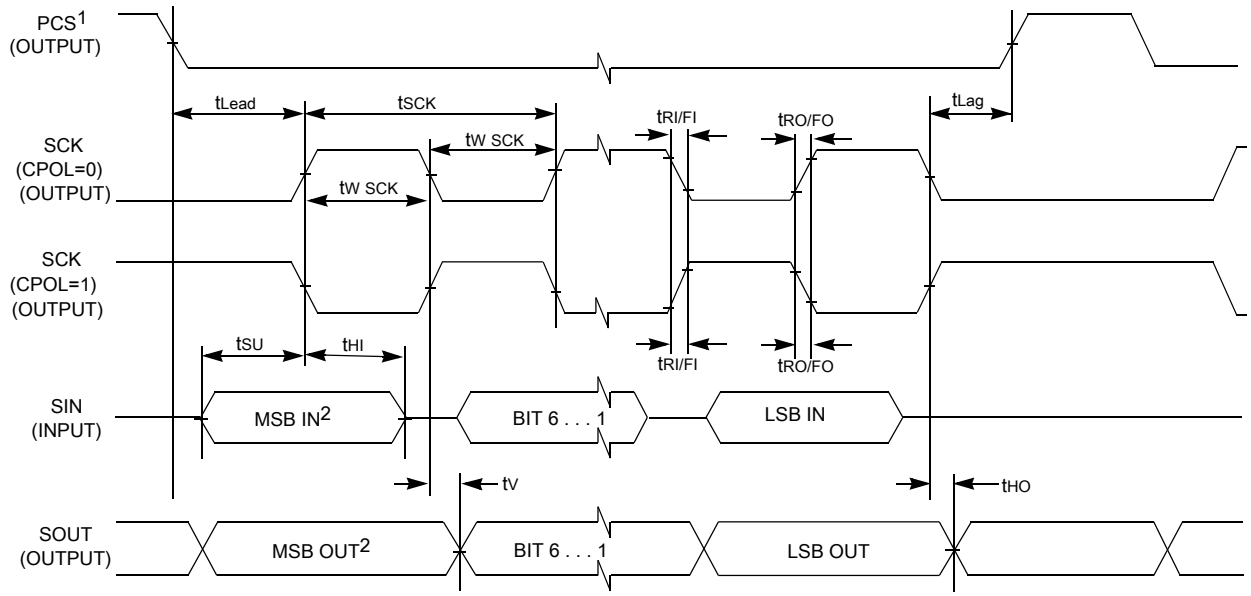
Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	Frequency of LPSPI clock root [1][2][3]	—	—	30	MHz	—	—
fSCK	Frequency of LPSPI clock root [4][5]	—	—	60	MHz	—	—
tSCK	SCK period [6]	2 x tperiph	—	—	ns	—	—
tLead	Enable lead time	1	—	—	tperiph	—	—
tLag	Enable lag time	1	—	—	tperiph	—	—
tWSCK	Clock (SCK) high or low time	tSCK / 2 - 3	—	tSCK / 2 + 3	ns	—	—
tSU	Data setup time (inputs) [5][7]	8	—	—	ns	When operating at 3.3 V I/O supply, this parameter value is 9 ns.	—
tHI	Data hold time (inputs) [5][7]	0	—	—	ns	—	—
tV	Data valid (after SCK edge)	—	—	2.5	ns	—	—
tHO	Data hold time (outputs)	-2.5	—	—	ns	—	—
tRI/FI	Rise/Fall time input	—	—	3	ns	—	—
tRO/FO	Rise/Fall time output	—	—	3	ns	—	—

[1] Input timing assumes an input signal slew rate of 3 ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
[3] The clock driver in the LPSPI module for fperiph must guaranteed this limit is not exceeded.
[4] In controller loopback mode when LPSPI_CFGR1[SAMPLE] bit is 1.
[5] The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.
[6] tperiph = 1000 / fperiph

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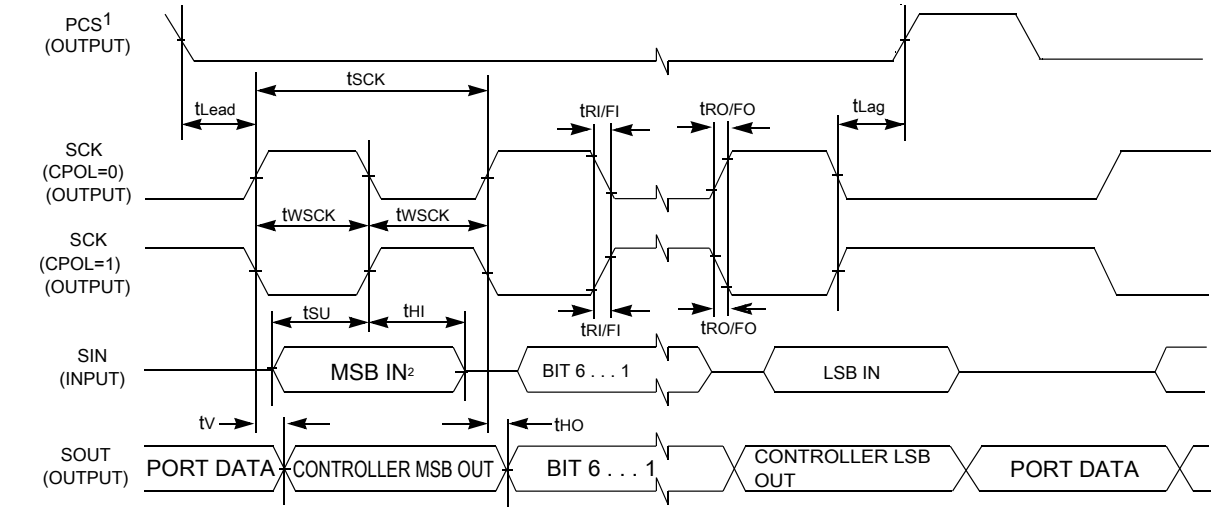
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[7] If LPSPI_CFGR1[SAMPLE] bit is 1, the data setup time (inputs) / data hold time (inputs) specifications are same with the one in Peripheral mode.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 38. LPSPI Controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 39. LPSPI Controller mode timing (CPHA = 1)

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4.13.3 LPSPI Peripheral mode AC timing specifications

Table 77. LPSPI Peripheral mode AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	Frequency of LPSPI clock root [1][2]	—	—	30	MHz	—	—
tSCK	SCK period [3]	2 x tperiph	—	—	ns	—	—
tLead	Enable lead time	1	—	—	tperiph	—	—
tLag	Enable lag time	1	—	—	tperiph	—	—
tWSCK	Clock (SCK) high or low time	tSCK / 2 - 5	—	tSCK / 2 + 5	ns	—	—
tSU	Data setup time (inputs)	3	—	—	ns	—	—
tHI	Data hold time (inputs)	3	—	—	ns	—	—
ta	Peripheral access time [4]	—	—	20	ns	—	—
tdis	Peripheral MISO disable time [5]	—	—	20	ns	—	—
tV	Data valid (after SCK edge)	—	—	8	ns	When operating at 3.3 V I/O supply, this parameter value is 9 ns.	—
tHO	Data hold time (outputs)	0	—	—	ns	—	—

[1] Input timing assumes an input signal slew rate of 3 ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
[3] tperiph = 1000 / fperiph
[4] Time to data active from high-impedance state
[5] Hold time to high-impedance state

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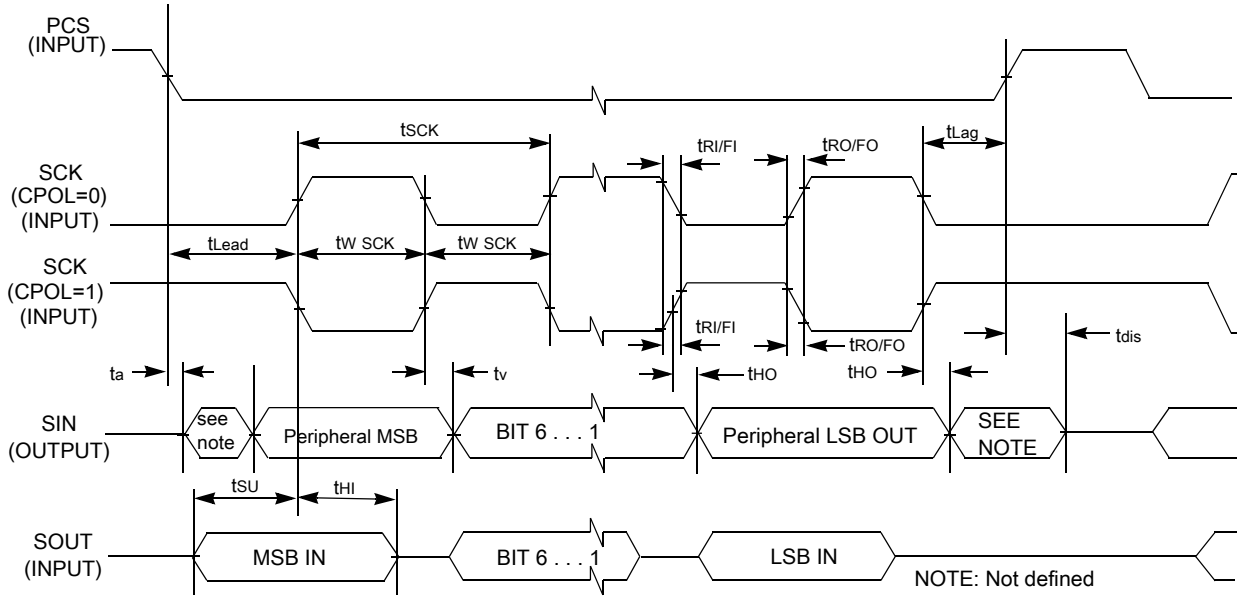


Figure 40. LPSPI Peripheral mode timing (CPHA = 0)

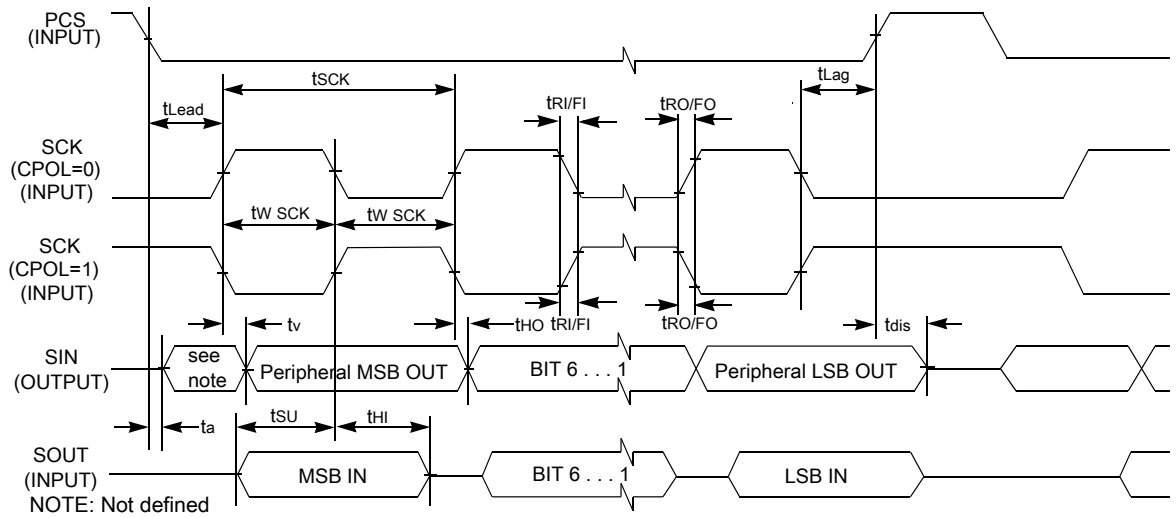


Figure 41. LPSPI Peripheral mode timing (CPHA = 1)

4.14 LPI2C timing parameters

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target.

Table 78. LPI2C timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIH_SC	Input Start condition hold time	2	—	—	MODULE_CLK cycle	—	—

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Table 78. LPI2C timing parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCL	Input Clock low time	8	—	—	MODULE_CLK cycle	—	—
tIH	Input Data hold time	0	—	—	ns	SDA transitions after SCL falling edge	—
tCH	Input Clock high time	4	—	—	MODULE_CLK cycle	—	—
tISU	Input Data setup time (standard mode)	250	—	—	ns	SDA transitions before SCL rising edge	—
tISU_F	Input Data setup time (fast mode)	100	—	—	ns	SDA transitions before SCL rising edge	—
tISU_RSC	Input Start condition setup time (repeated start condition)	2	—	—	MODULE_CLK cycle	—	—
tISU_SC	Input Start condition setup time	2	—	—	MODULE_CLK cycle	—	—
tOH_SC	Output Start condition hold time	6	—	—	MODULE_CLK cycle	—	—
tCL	Output Clock low time	10	—	—	MODULE_CLK cycle	—	—
tRISE	SDA/SCL rise time	—	—	100	ns	SRE[2:0] = 110	—
tOH	Output Data hold time	7	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
tFALL	SDA/SCL fall time	—	—	100	ns	SRE[2:0] = 110	—
tCH	Output Clock high time	10	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
tOSU	Output Data setup time	2	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
tOSU_RSC	Output repeated start condition setup time	20	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—

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Table 78. LPI2C timing parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOSU_SC	Output start condition setup time	11	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
fSCL	SCL clock frequency: Standard mode (Sm) [1][2]	0	—	100	kHz	—	—
fSCL	SCL clock frequency: Fast mode (Fm) [1][2]	0	—	400	kHz	—	—
fSCL	SCL clock frequency: Fast mode Plus (Fm++) [1][2]	0	—	1000	kHz	—	—
fSCL	SCL clock frequency: High speed mode (Hs-mode) [1][2]	0	—	3400	kHz	—	—
fSCL	SCL clock frequency: Ultra Fast mode (Ufm) [1][2]	0	—	5000	kHz	—	—

[1] For more details, see UM10204 I2C-bus specification and user manual.
[2] Standard, Fast, Fast+, and Ultra Fast modes are supported; High speed mode (HS) in target mode.

4.15 Improved Inter-Integrated Circuit Interface (I3C) specifications

Unless otherwise specified, I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

4.15.1 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 25 pf, input transition of 1 ns.

Table 79. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCL	SCL Clock Frequency	0.01	12.5	12.9	MHz	FSCL = 1 / (tDIG_L + tDIG_H)	—
tDIG_L	SCL Clock Low Period [1][2]	32	—	—	ns	—	—
tDIG_H	SCL Clock High Period [1]	32	—	—	ns	—	—
tSCO	Clock in to Data Out for Target [3][4]	—	—	12	ns	—	—

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Table 79. I3C Push-Pull Timing Parameters for SDR Mode...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCR	SCL Clock Rise Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—	—
tCF	SCL Clock Fall Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—	—
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Target [6][7]	0	—	—	ns	Applicable for target and controller loopback modes	—
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	N/A	ns	Applicable for target and controller loopback modes	—

[1] tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
[2] As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.
[3] Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Controller to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.
[4] Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Controller may be a Target in a multi-Controller system, and thus shall also adhere to this requirement
[5] The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
[6] tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Controller mode vs. Target mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.
[7] SDA Input Hold time in Target mode is 1 ns.

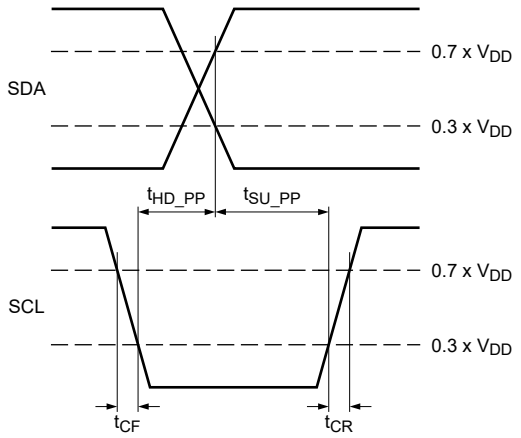


Figure 42. Controller out timing

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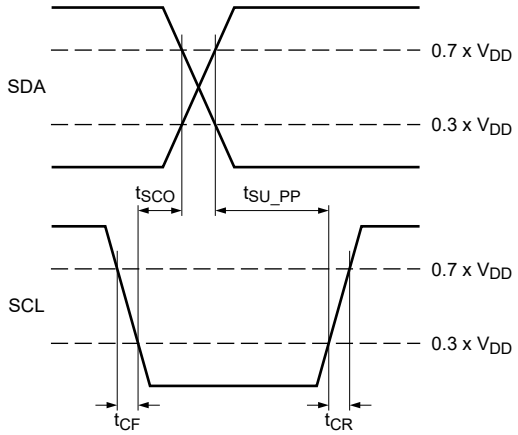


Figure 43. Target out timing

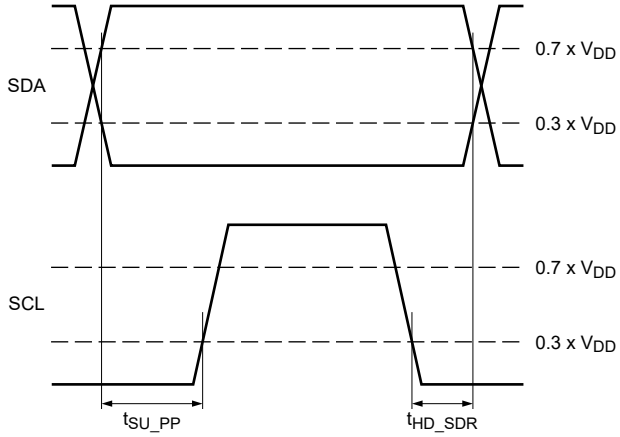


Figure 44. Controller SDR timing

4.16 CAN network AC timing characteristics

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has two CAN modules available. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Please see General purpose I/O (GPIO) AC parameters for timing parameters.

Table 80. CAN-FD timing characteristics

Parameters	FlexCAN (Classical and FD)	Unit
Minimum operating frequency	20/40	MHz
Maximum Baud Rate	8/8	Mbps
TXD Rise time wcs	4/4	ns

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Table 80. CAN-FD timing characteristics...*continued*

Parameters	FlexCAN (Classical and FD)	Unit
TXD Fall time wcs	4/4	ns
RXD Rise time wcs	4/4	ns
RXD Fall time wcs	4/4	ns
TXD	3.3/3.3	V
RXD	3.3/3.3	V
Internal delay wcs	100/50	ns
TX PAD delay wcs	25/25	ns
RX PAD delay wcs	10/10	ns
TX routing delay wcs	5/5	ns
RX routing delay wcs	5/5	ns
Transceiver loop delay wcs	250/250	ns
Total loop delay	395/345	ns

4.17 XSPI

An external resistor is needed to pull up a XSPI chip select signal.

4.17.1 XSPI electrical specifications

Table 81. TX/WRITE timing specs

Mode	Spec	Min	Typ	Max	Unit	Condition
DDR	SCK Output Frequency	-	-	200	MHz	Nominal and Overdrive mode
DDR	Data output valid time	0.615	-	1.815	ns	Nominal and Overdrive mode
DDR	SCK Output Frequency	-	-	133	MHz	Low drive mode
DDR	Data output valid time	0.9	-	2.75	ns	Low drive mode
SDR	SCK Output Frequency	-	-	200	MHz	Nominal and Overdrive mode
SDR	Data output valid time	-0.6	-	0.6	ns	Nominal and Overdrive mode
SDR	SCK Output Frequency	-	-	133	MHz	Low drive mode
SDR	Data output valid time	-2	-	2	ns	Low drive mode

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Table 82. RX/READ timing specs

MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)						
Mode	Spec	Min	Typ	Max	Unit	Condition
DDR	SCK Frequency	-	-	200	MHz	Nominal and Overdrive mode
DDR	Data setup time	0.6*	-	-	ns	Nominal and Overdrive mode
DDR	Data hold time	0.6*	-	-	ns	Nominal and Overdrive mode
DDR	SCK Frequency	-	-	125	MHz	Low drive mode
DDR	Data setup time	0.9*	-	-	ns	Low drive mode
DDR	Data hold time	0.9*	-	-	ns	Low drive mode
SDR	SCK Frequency	-	-	200	MHz	Nominal and Overdrive mode
SDR	Data setup time	0.6	-	-	ns	Nominal and Overdrive mode
SDR	Data hold time	0.6	-	-	ns	Nominal and Overdrive mode
SDR	SCK Frequency	-	-	125	MHz	Low drive mode
SDR	Data setup time	0.9	-	-	ns	Low drive mode
SDR	Data hold time	0.9	-	-	ns	Low drive mode

MCR[DQS_FA_SEL] = 2 (internal dummy read strobe and loopbacked from DQS pad)						
Mode	Spec	Min	Typ	Max	Unit	Condition
DDR	SCK Frequency	-	-	83	MHz	Overdrive mode
DDR	Data setup time	1.2	-	-	ns	Overdrive mode
DDR	Data hold time	1	-	-	ns	Overdrive mode
DDR	SCK Frequency	-	-	66	MHz	Nominal and Low drive mode
DDR	Data setup time	1.7	-	-	Ns	Nominal and Low drive mode
DDR	Data hold time	1	-	-	Ns	Nominal and Low drive mode
SDR	SCK Frequency	-	-	133	MHz	Nominal and Overdrive mode
SDR	Data setup time	1.2	-	-	Ns	Nominal and Overdrive mode
SDR	Data hold time	1	-	-	ns	Nominal and Overdrive mode
SDR	SCK Frequency	-	-	125	MHz	Low drive mode

Table continues on the next page...

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Table continued from the previous page...

MCR[DQS_FA_SEL] = 2 (internal dummy read strobe and loopbacked from DQS pad)						
Mode	Spec	Min	Typ	Max	Unit	Condition
SDR	Data setup time	1.7	-	-	ns	Low drive mode
SDR	Data hold time	1	-	-	ns	Low drive mode

4.17.2 XSPI Octal 1.8 V DDR 100 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 83. XSPI Octal 1.8 V DDR 100 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1][2]	—	—	100	MHz	fSCK duty cycle distortion is in the range of 45%-55%.	—
tCL_SCK	SCK low time [1][2]	4.500	—	—	ns	—	—
tCH_SCK	SCK high time [1][2]	4.500	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	1.1	—	3.45	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	3.016 - n/fSCK	—	-0.016 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	3.284	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.9	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.6	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

4.17.3 XSPI Octal 1.8 V DDR 133 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 84. XSPI Octal 1.8 V DDR 133 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1][2]	—	—	133	MHz	DLL mode enabled, fSCK duty cycle distortion is in the range of 45%-55%.	—

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Table 84. XSPI Octal 1.8 V DDR 133 MHz*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCL_SCK	SCK low time [1][2]	3.383	—	—	ns	—	—
tCH_SCK	SCK high time [1][2]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.9	—	2.5	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	3.015 - n/fSCK	—	-1.33 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	2.314	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.7	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

4.17.4 XSPI Octal 1.8 V DDR 166 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 85. XSPI Octal 1.8 V DDR 166 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK-DQS	SCK/DQS frequency [1][2]	—	—	166	MHz	fSCK duty cycle distortion is in the range of 45%-55%.	—
tCL_SCK	SCK low time [1][2]	2.711	—	—	ns	—	—
tCH_SCK	SCK high time [1][2]	2.711	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.6	—	2.095	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	3.016 - n/fSCK	—	-1.805 + m/fSCK	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	2.15	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.55	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

4.17.5 XSPI Octal 1.8 V DDR 200 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

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Table 86. XSPI Octal 1.8 V DDR 200 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK-DQS	SCK/DQS frequency [1][2]	—	—	200	MHz	fSCK duty cycle distortion is in the range of 45%-55%.	—
tCL_SCK	SCK low time [1][2]	2.25	—	—	ns	—	—
tCH_SCK	SCK high time [1][2]	2.25	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.6	—	1.725	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	3.016 - n/fSCK	—	-2.266 + m/fSCK	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	1.75	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.45	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

4.17.6 XSPI Octal 1.8 V SDR 100 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 87. XSPI Octal 1.8 V SDR 100 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1][2]	—	—	100	MHz	—	—
tCL_SCK	SCK clock low time [1][2]	4.5	—	—	ns	—	—
tCH_SCK	SCK clock high time [1][2]	4.5	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	-2.75	—	2.75	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	3.016 - n/fSCK	—	5.160 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	6.884	—	—	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	2.5	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	1	—	—	ns	—	—

[1] Input timing assumes an input signal transition of 1ns (20%/80%).
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

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[3] Where m=TCSS and n=TCSH-1.

4.17.7 XSPI Octal 1.8 V SDR 133 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 88. XSPI Octal 1.8 V SDR 133 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1][2]	—	—	133	MHz	DLL mode enabled	—
tCL_SCK	SCK clock low time [1][2]	3.383	—	—	ns	—	—
tCH_SCK	SCK clock high time [1][2]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	-1.5	—	1.5	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	3.016 - n/fSCK	—	2.704 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	4.609	—	—	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	0.6	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	1	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

4.17.8 XSPI Quad 1.8 V DDR 66 MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 89. XSPI Quad 1.8 V DDR 66 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1][2]	—	—	66	MHz	DLL mode enabled	—
tCL_SCK	SCK clock low time [1][2]	6.818	—	—	ns	—	—
tCH_SCK	SCK clock high time [1][2]	6.818	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	2.4	—	4.8	ns	—	—

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Table 89. XSPI Quad 1.8 V DDR 66 MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOD_CS	CS output delay (w.r.t. SCK) [2][3]	5.016 - n/fSCK	—	1.802 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	5.14	—	—	ns	—	—
tLSKEW	Skew target for Auto-learning mode	1.89	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

4.17.9 XSPI configurations

Frequency (MHz)	200	133/100
DDR/SDR	DDR	SDR
External DQS alignment	Edge-aligned	Dummy pad loopback
Flash	Octal Flash (1.8 V)	Quad/Octal Flash (1.8 V)
FLSHCR[TDH]	1	0
FLSHCR[TCHS]	2	2
FLSHCR[TCSS]	2	2
MCR[DLPEN]	0	1
DLLCR[DLLEN]	1	1
DLLCR[FREQEN]	1	0
DLLCR[DLL_REFCNTR]	2	2
DLLCR[DLLRES]	4	4
DLLCR[SLV_FINE_OFFSET]	0	0
DLLCR[SLV_DLY_OFFSET]	0	3
DLLCR[SLV_DLY_COARSE]	0	0
DLLCR[SLV_DLY_FINE]	0	0
DLLCR[SLAVE_AUTO_UPDT]	1	1
DLLCR[SLV_EN]	1	1
DLLCR[SLV_DLL_BYPASS]	0	0
DLLCR[SLV_UPD]	1	1
SMPR[DLLFSMPF*]	3	0
SMPR[FSDLY]	0	1
SMPR[FSPHS]	NA	1

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4.17.10 XSPI interfaces

The XSPI module supports 2 interfaces; XSPI A & XSPI B. These interfaces are not independent & the QSPI chapter of the reference manual should be consulted for their usage. The table below summarizes which specifications are supported on each interface.

Table 90. XSPI interfaces

Specification / Interface	1.8V Quad	1.8V Octal	1.8V Hyperflash
XSPI A	SDR 100/133MHz DDR 66MHz	SDR 100/133MHz DDR 100/133/166/200 MHz	DDR 100/133/166/200 MHz
XSPI B	SDR 100/133MHz DDR 66MHz	SDR 100/133MHz DDR 100/133MHz	DDR 100/133/166/200 MHz

4.17.11 XSPI timing diagrams

The sections shows the XSPI timing diagrams for all modes supported by the device. All data is based on a negative edge data launch from the device.

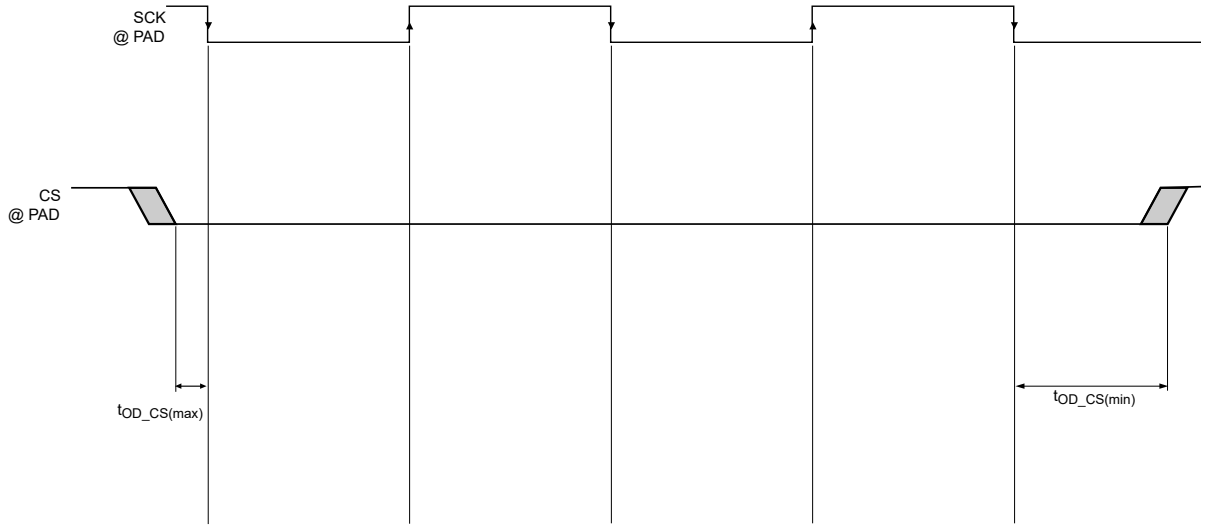


Figure 45. CS output timing

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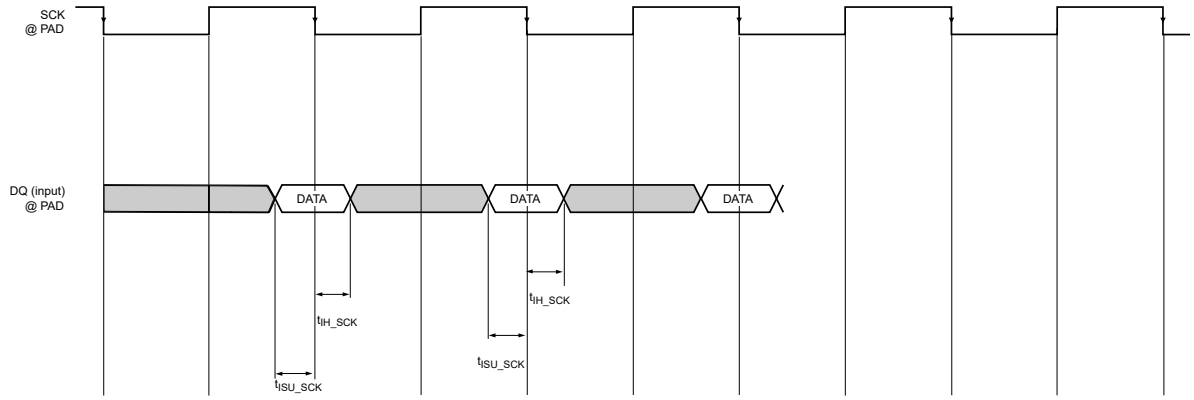


Figure 46. SDR input timing

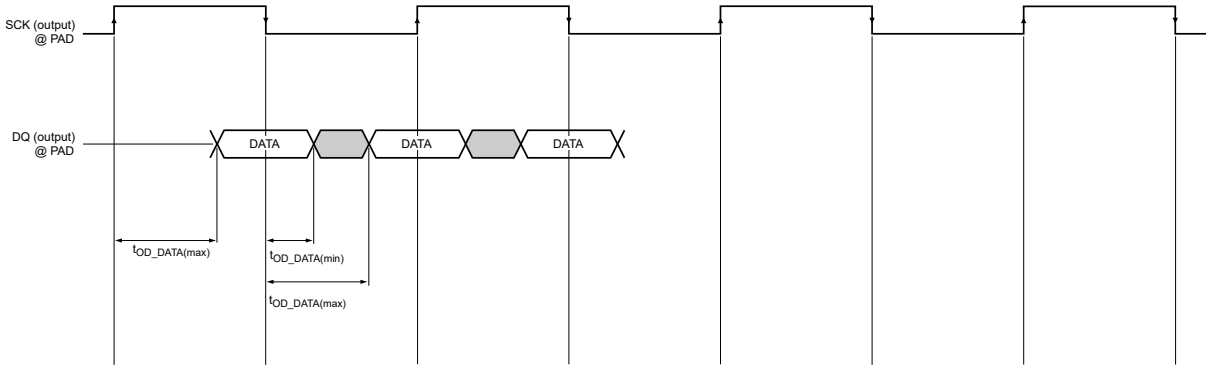


Figure 47. DDR output timing

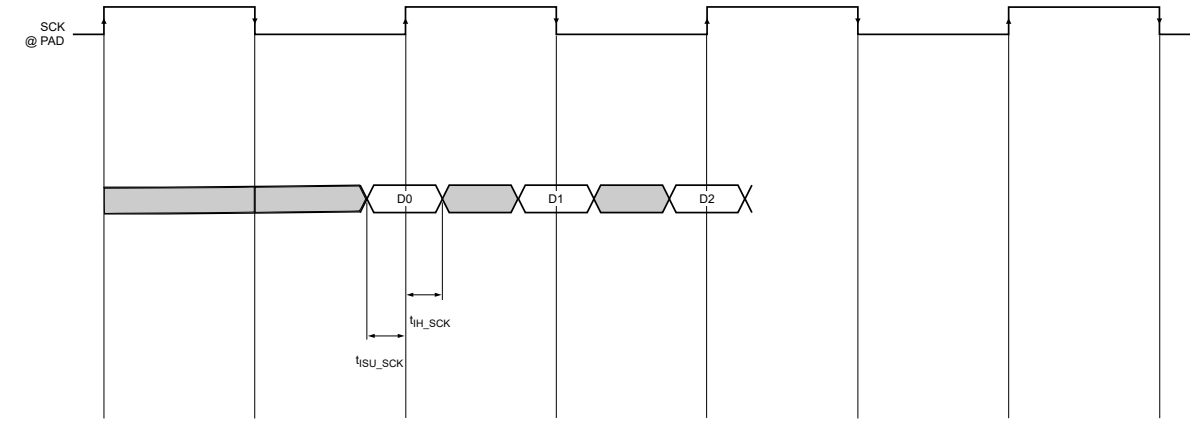


Figure 48. DDR with internal pad loopback input timing

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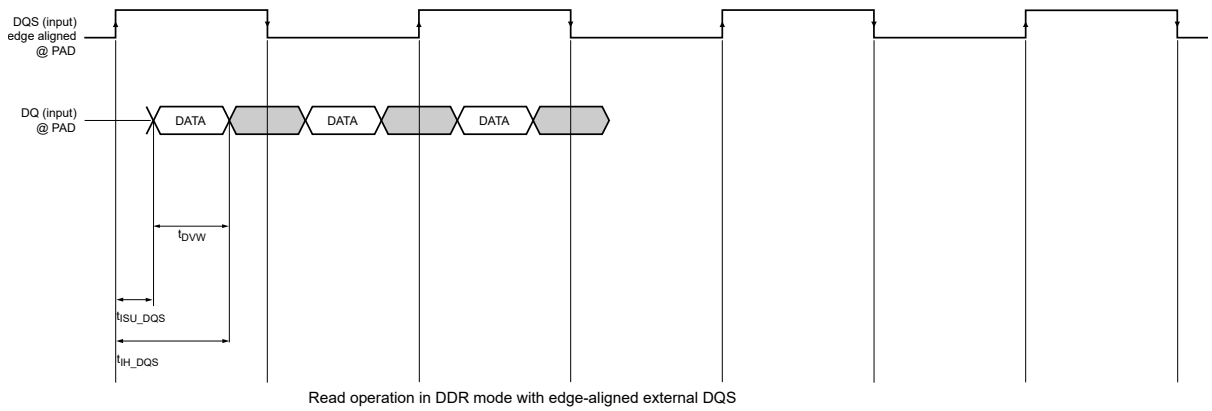


Figure 49. DDR edge-aligned DQS input timing

4.18 XSPI_FLR Specifications

Tested on samples basis and specified through design and characterization data. TA = 25 ℃, VCC = 3.0 V.

4-byte address alignment for Quad Read: read address start from A1, A 0 = 0,0

For details about XSPI Follower specifications, please refer to https://www.winbond.com.

4.19 LPUART I/O configuration and timing parameters

Please refer to General purpose I/O (GPIO) AC parameters.

4.20 Flexible I/O controller (FLEXIO) electrical specifications

4.20.1 Flexible I/O controller (FlexIO) AC timing characteristics

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 Ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

The following table shows FlexIO timing specifications.

Table 91. Flexible I/O controller (FlexIO) AC timing characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tODS	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle [1]	0	—	12	ns	—	—
tIDS	Input delay skew between any two	0	—	12	ns	—	—

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Table 91. Flexible I/O controller (FlexIO) AC timing characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle [1]						

[1] Assume pinx muxed on same VDD_IO domain with the load

4.20.2 Flexible I/O controller (FlexIO) DC electrical characteristics

Table 92. Flexible I/O controller (FlexIO) DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage [1] [2]	0.7 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1] [2]	—	—	0.3 x NVCC_xxx	V	—	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	µA	—	—
VOH	Output high voltage (IOH = -2mA at NVCC_xxx min)	NVCC_xxx - 0.45	—	—	V	—	—
VOL	Output high voltage (IOL = 2mA at NVCC_xxx min)	—	—	0.45	V	—	—

[1] For recommended operating conditions, see Recommended Operating Conditions.
[2] The min VIL and max VIH values are based on the respective min and max VDD values found in Recommended Operating Conditions.

4.21 USB PHY parameters

4.21.1 USB 2.0 AC timing specifications

Table 93. USB 2.0 AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FREF_OFFSET	Reference clock frequency offset	-300	—	300	ppm	—	—
JRMSREF_CLK	Reference clock random jitter (RMS) [1][2]	—	—	3	ps	—	—

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Table 93. USB 2.0 AC timing specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
DJREF_CLK	Reference clock cycle-to-cycle jitter [3]	—	—	150	ps	—	—
tKHK/tSYSCLK	Reference clock duty cycle	40	—	60	%	—	—
fSYSCLK	Reference clock frequency	—	24	—	MHz	—	—

[1] 1.5 MHz to Nyquist frequency. For example, 100 MHz reference clock, the Nyquist frequency is 50 MHz.
[2] The peak-to-peak Rj specification is calculated at 14.069 times the RJRMS for 10 - 12 BER.
[3] DJ across all frequencies.

4.21.2 USB 2.0 DC electrical characteristics

Table 94. USB 2.0 DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH	Output High voltage	2.8	—	—	V	VDD ≥3.0 V	—
VOL	Output Low voltage	—	—	0.8	V	VDD ≥3.0 V	—
VCRS	Output Crossover Point	1.3	—	2	V	—	—
ZDRV	Output impedance	28	36	44	Ω	Driving High	—
ZDRV	Output impedance	28	36	44	Ω	Driving Low	—
RPU	Pull-up resistance	1.425	1.5	1.575	kΩ	Full speed (D + Pull-up)	—
tR	Output Rise time	4	—	20	ns	Full speed	—
tF	Output Fall time	4	—	20	ns	Full speed	—
VDI	Differential Input Sensitivity	0.2	—	—	V	| (D+) - (D-) |	—
VCM	Differential Input Common mode range	0.8	—	2.5	V	—	—
IL	Input leakage current	—	< 1.0	—	µA	Pullups Disabled	—

4.22 PCIe 3.0 PHY parameters

The PCIe interface is designed to be compatible with PCIe specification Gen3 x1 lane and supports the *PCI Express Base Specification, Revision 3.1, November 2013, PCI-SIG*.

4.22.1 PCIe

PCIe Electricals are compatible with the PCIe Base Specification Rev 3.1, Section 4.3

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Table 95. PCIe

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval [1]	399.88	—	400.12	ps	2.5GT/s	—
UI	Unit Interval [1]	199.94	—	200.06	ps	5GT/s	—
UI	Unit Interval [1]	124.9625	—	125.0375	ps	8GT/s	—
CTX	AC Coupling Capacitor [2]	75	—	265	nF	2.5GT/s, 5GT/s	—
CTX	AC Coupling Capacitor [2]	176	—	265	nF	8GT/s	—
REXT	External Reference Resistor (RESREF)	—	200	—	Ohms	—	—

[1] The specified UI is equivalent to a tolerance of +/- 300ppm for each Reference Clock Source. Period does not account for SSC induced variations.
[2] All platforms that have transmitters supporting 8.0 GT/s must implement the 176 nf to 265 nF CTX value. Platforms operating at 2.5 or 5.0 GT/s only may increase that range to 75 nf to 265 nF.

REXT requires 1% 100ppm/C precision resistor-to-ground on PC Board

The specified UI is equivalent to a tolerance of +/- 300ppm for each Reference Clock Source. Period does not account for SSC induced variations. This parameter is measured by Validation as part of Transmitter AC Specifications. It is listed here in overview section as min/max also define reference clock allowed ppm offset.

All platforms that have transmitters supporting 8.0 GT/s must implement the 176 nf to 265 nF CTX value. Platforms operating at 2.5 or 5.0 GT/s only may increase that range to 75 nf to 265 nF.

4.22.2 PCIE Transmitter AC Specifications

Table 96. PCIE Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
BWTX-PKG-PLL-TYP	Typical TX PLL Bandwidth	—	8.762	—	MHz	2.5GT/s	—
PKGTX-PLL-TYP	Typical TX PLL Peaking	—	0.55	—	dB	2.5GT/s	—
BWTX-PKG-PLL-TYP	Typical TX PLL Bandwidth	—	9.041	—	MHz	5GT/s	—
PKGTX-PLL-TYP	Typical TX PLL Peaking	—	0.53	—	dB	5GT/s	—
BWTX-PKG-PLL-TYP	Typical TX PLL Bandwidth	—	3.443	—	MHz	8GT/s	—
PKGTX-PLL-TYP	Typical TX PLL Peaking	—	0.56	—	dB	8GT/s	—
TTX-EYE	Transmitter Eye including all jitter sources	0.75	—	—	UI	2.5GT/s, 5GT/s	—

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4.22.3 PCIE Receiver DC Specifications

Table 97. PCIE Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VRX-DIFF-PP-CC	Differential peak-peak voltage for common Refclk RX architecture	0.175	—	1.2	V	2.5GT/s	—
VRX-DIFF-PP-CC	Differential peak-peak voltage for common Refclk RX architecture	0.12	—	1.2	V	5GT/s	—

4.22.4 PCIE Reference Clock Output Specifications

PCIe Reference Clock Output Electricals are compatible with the PCIe Base Specification Rev 3.0 Version 1.0, Section 4.3.7

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

i.MX 952 supports three different boot modes:

- Normal Boot Mode
- Boot from Internal Fuse Mode
- Serial Download Boot Mode

Three different boot modes can be selected via different boot mode pins or overridden by fuses.

i.MX 952 has one kind of boot type:

- Low Power Boot (LPB): only M33 core is running after POR.

For detailed boot mode configuration, see the "Fusemap" and the "System Boot" chapter in i.MX 952 Reference Manual (IMX952RM).

5.1 Boot mode configuration pins

There are four boot mode pins used to select boot mode.

Table 98. Fuses and associated pins used for boot

BOOT_MODE [3:0]	Functions
X000	Boot from Internal Fueses
X001	Serial Download (USB1)
X010	uSDHC1 8-bit eMMC5.1
X011	uSDHC2 4-bit SD3.0

Table continues on the next page...

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Table 98. Fuses and associated pins used for boot*...continued*

BOOT_MODE [3:0]	Functions
X100	XSPI Serial NOR
X101	XSPI Serial NAND
X110	Reserved
X111	Reserved

- HW samples the boot CFG pins before ROM starts, these pins should be mapped to Boot CFG pins by default.
- Once HW samples the boot CFG pins and stores the boot CFG in CMC register, the register should be latched and reflecting the pins status.

Additional boot options are also supported for both Normal Boot Mode and Internal Fuse mode:

- All boot modes support for a range of speeds, timings, and protocol formats;
- eMMC and SD boot can be supported from any USDHC instance 1 or 2;
- Serial NOR boot supports 1-bit, 4-bit, and 8-bit mode;
- Serial NAND boot supports 1-bit, 4-bit, and 8-bit mode (8-bit Serial NAND)

BOOT_MODE pins are multiplexed over other functional pins. The functional I/O that multiplexed with these pins must be selected subject to two criteria:

- Functional I/O must not be used if they are inputs to the SoC, which could potentially be constantly driven by external components. Such functional mode driving may interfere with the need for the board to pull these pins a certain way while POR is asserted.
- Functional I/O must not be used if they are outputs of the SoC, which will be connected to components on the board that may misinterpret the signals as valid signals if they are toggled (such as, the board drives them while POR is asserted).

5.2 Boot devices interfaces allocation

i.MX 952 supports three kinds of boot devices:

- Primary Boot Device

  The primary boot device is selected by Boot Config pins if boot mode is the Normal Boot or Internal Fuses Boot. The valid primary boot device options are SD/eMMC/XSPI NOR/XSPI NAND. The valid options also depend on the Boot Type and other fuses configuration.

- Recovery Boot Device

  After failure of booting from Primary Boot Device, i.MX 952 tries to boot from another boot source. The recovery boot device is only from SPI1 or SPI2.

- Serial Download Boot Device

  Cortex-M33 supports serial download mode via USB1 and USB2.

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

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Table 99. Boot through XSPI

Signal name	Pad name	Alt
XSPIA_DATA0	XSPI1_DATA0	ALT0
XSPI_DATA1	XSPI1_DATA1	ALT0
XSPI_DATA2	XSPI1_DATA2	ALT0
XSPI_DATA3	XSPI1_DATA3	ALT0
XSPI_DQS	XSPI1_DQS	ALT0
XSPI_SS0_B	XSPI0_SS0_B	ALT0
XSPI_SS1_B	XSPI0_SS1_B	ALT0
XSPI_SCLK	XSPI0_DATA0	ALT0
XSPI_DATA4	XSPI0_DATA4	ALT0
XSPI_DATA5	XSPI0_DATA5	ALT0
XSPI_DATA6	XSPI0_DATA6	ALT0
XSPI_DATA7	XSPI0_DATA7	ALT0

Table 100. Boot through uSDHC1

Signal name	PAD name	ALT
USDHC1_CMD	SD1_CMD	ALT0
USDHC1_CLK	SD1_CLK	ALT0
USDHC1_DATA0	SD1_DATA0	ALT0
USDHC1_DATA1	SD1_DATA1	ALT0
USDHC1_DATA2	SD1_DATA2	ALT0
USDHC1_DATA3	SD1_DATA3	ALT0
USDHC1_DATA4	SD1_DATA4	ALT0
USDHC1_DATA5	SD1_DATA5	ALT0
USDHC1_DATA6	SD1_DATA6	ALT0
USDHC1_DATA7	SD1_DATA7	ALT0
USDHC1_RESET	SD1_DATA5	ALT2

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Table 101. Boot through uSDHC2

Signal name	PAD name	ALT
USDHC2_CMD	SD2_CMD	ALT0
USDHC2_CLK	SD2_CLK	ALT0
USDHC2_DATA0	SD2_DATA0	ALT0
USDHC2_DATA1	SD2_DATA1	ALT0
USDHC2_DATA2	SD2_DATA2	ALT0
USDHC2_DATA3	SD2_DATA3	ALT0
USDHC2_RESET	SD2_RESET_B	ALT0
USDHC2_VSELECT	SD2_VSELECT	ALT0

Table 102. Boot through SPI1

Signal name	PAD name	ALT
SPI1_PCS1	PDM_BIT_STREAM0	ALT2
SP11_SIN	SAI1_TXC	ALT2
SPI1_SOUT	SAI1_RXD0	ALT2
SPI1_SCK	SAI1_TXD0	ALT2
SPI1_PCS0	SAI1_TXFS	ALT2

Table 103. Boot through SPI2

Signal name	PAD name	ALT
SPI2_PCS1	PDM_BIT_STREAM1	ALT2
SP12_SIN	UART1_RXD	ALT2
SPI2_SOUT	UART2_RXD	ALT2
SPI2_SCK	UART2_TXD	ALT2
SPI2_PCS0	UART1_TXD	ALT2

USB1 interfaces are dedicated pins, thus no IOMUX options.

6 Package information and functional contact assignments

This section includes the contact assignment information and mechanical package drawing.

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6.1 15 x 15 mm package information

This section includes the 15 x 15 mm package contact assignment information and mechanical package drawing.

6.1.1 15 x 15 mm, 0.5/0.54/0.56 mm pitch, ball matrix

Figure 50 shows the top, bottom, and side views of the 15 x 15 mm FCBGA package.[1]

[1] FCBGA 15 × 15 mm has 10 lb of maximum force

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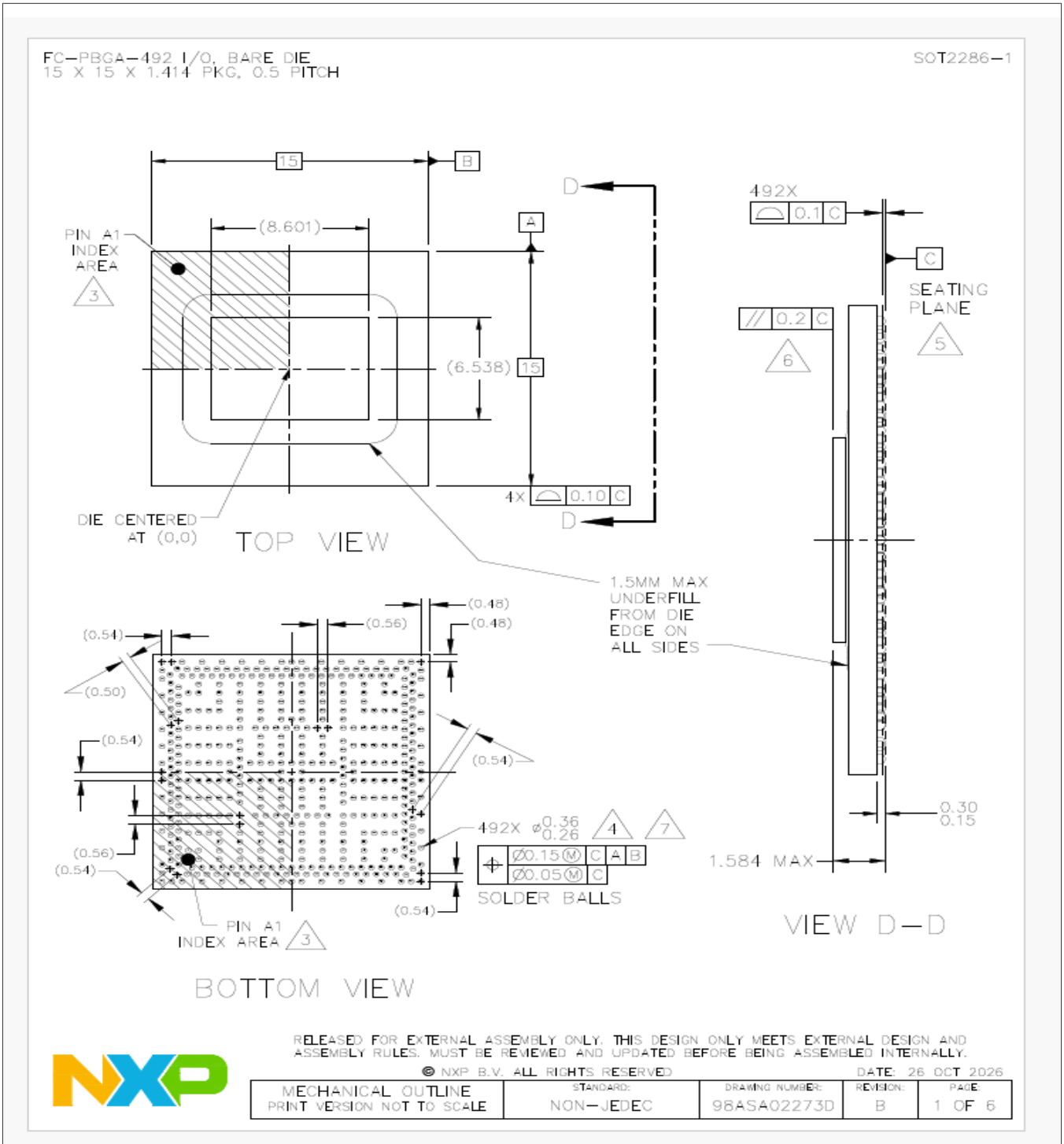


Figure 50. 15 x 15 mm FCBGA, case x package Top, Bottom, and Side Views

6.1.2 15 x 15 mm supplies contact assignments and functional contact assignments

See http://www.nxp.com/docs/en/data-sheet/iMX-952-Pin-list-and-Ball-map.zip

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6.1.3 15 x 15 mm, 0.5/0.54/0.56 mm pitch, ball map

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6.2 19 x 19 mm package information

This section includes the 19 x 19 mm package contact assignment information and mechanical package drawing.

6.2.1 19 x 19 mm, 0.7 mm pitch, ball matrix

Figure 51 shows the top, bottom, and side views of the 19 x 19 mm FCBGA package.[2]

[2] FCBGA 19 × 19 mm has 18 lb of maximum force

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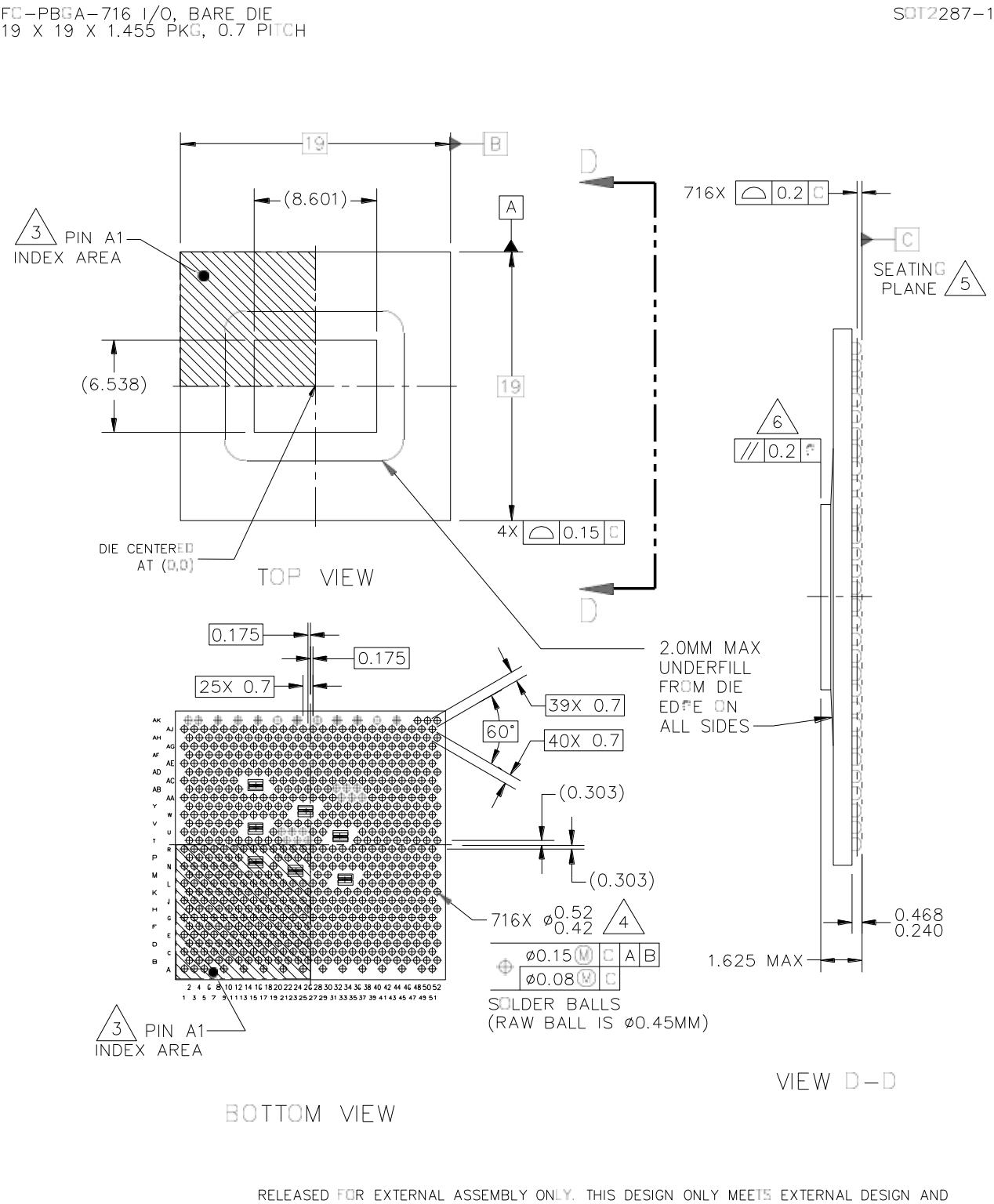


Figure 51. 19 x 19 mm FCBGA, case x package Top, Bottom, and Side view

6.2.2 19 x 19 mm supplies contact assignments and functional contact assignments

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6.2.3 19 x 19 mm, 0.7 mm pitch, ball map

See http://www.nxp.com/docs/en/data-sheet/iMX-952-Pin-list-and-Ball-map.zip

7 Revision history

Table 104 provides a revision history for this data sheet.

Table 104. Data Sheet document revision history

Document ID	Release date	Description
IMX952IEC v.4.0	02 November 2026	Product Data Sheet Initial Public Release

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Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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