IMX95IEC

i.MX 95 Applications Processors Data Sheet for Industrial Products

Rev. 8 — 7 April 2026 | Product data sheet

- For functional characteristics and the programming model, see i.*MX 95 Applications Processor Reference Manual* (IMX95RM).

1 Introduction

i.MX 95 applications processors offer advanced graphics and video cores, powerful vision and machine learning acceleration, efficient CPU performance plus real-time processing and advanced security with integrated EdgeLock® secure enclave to support energy-efficient Edge Computing.

i.MX 95 applications processors integrate up to six Arm Cortex®-A55 cores and are the first i.MX devices to support functional safety with built-in Arm Cortex®-M33 which can be configured as a safety island. Optimizing performance and power efficiency for Industrial, IoT and Automotive devices, i.MX 95 processors are built with NXP's innovative Energy Flex architecture.

i.MX 95 applications processors offer a rich set of peripherals targeting automotive, industrial and commercial IoT market segments. Part of the EdgeVerse™ portfolio of intelligent edge solutions, i.MX 95 family will be offered in Commercial, Industrial, Extended Industrial and Automotive level qualification and backed by NXP's product longevity program.

Table 1. Feature summary

Subsystem	Features
Arm Cortex-A55 MPCore platform	• 6x Arm Cortex-A55, up to 1.8 GHz frequency • Arm v8.2 fully 64-bit capable • 32 kB L1 instruction cache, 32 kB L1 data cache (per core, parity protected) • 64 kB L2 cache (per core, ECC protected) • 512 kB L3 cache (shared across all cores, ECC protected)
Arm Cortex-M7 platform	• 1x Cortex-M7, up to 800 MHz frequency • Arm v8-M supporting Trustzone-M • 512 kB TCM (Tightly Coupled Memory), sum of instruction and data
Arm Cortex-M33 platform	• 1x Cortex-M33, up to 333 MHz frequency • Arm v8-M supporting Trustzone-M • 16 kB instruction cache + 16 kB data cache (ECC) • 512 kB TCM, sum of instruction and data
Memory	• 19 x 19 mm package: one x32 LPDDR interface (with inline ECC), operating at up to 6400MT/s in LPDDR5 mode or 4266 MT/s in LPDDR4X mode. • 15 x 15 mm package: one x32 LPDDR interface (with inline ECC), operating at up to 4266 MT/s in LPDDR5 mode or 4000 MT/s in LPDDR4X mode. • 3x uSDHC (SD3.0, SDIO3.0, eMMC5.1) • 8x LPI2C • 8x LPSPI • 2x I3C • 1x Octal SPI, including support for SPI NOR and SPI NAND memories • FlexSPI_FLR
Tightly Coupled Memory	1492 kB total, consisting of:

Table continues on the next page...

Table 1. Feature summary*...continued*

Subsystem	Features
	• 1024 kB from the NPU, which is available for use by the SoC when the NPU is idle. • 352 kB within the NOC central domain, shared across all cores • 96 kB in the vision section. • 16 kB in the display domain
Neural Processing Unit (NPU)	• 8 eTOPS at 1 GHz and can run at reduced performance at 800 MHz to save power. • 1 MByte of SRAM embedded within the NPU, but it is available for other SoC usage when not using for ML purposes.
Graphics	• Arm Mali-G310 Graphic Processing Unit (GPU) — 3D GPU supporting 64 GFLOPs FP32 — OpenGL® ES 3.2 — Vulkan® 1.3 — OpenCL 3.0
Video Processors	• 4Kp60 H.265 and H.264 encode and decode • 1x JPEG Encoder • 1x JPEG Decoder
Display Controller (up to 3 simultaneous displays)	• For 3 simultaneous displays (1x MIPI-DSI + 2x LVDS), both LVDS displays must have same resolution and timing. • 1x 350 MHz MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4kp30 or 3840 x 1440p60 • 2x 1080p60 LVDS Tx (2x 4-lane or 1x 8-lane) • 16 kByte of SRAM, but it is available for other SoC usage when not using for 2D blitter purposes
Camera and ISP	• 2x MIPI-CSI DPHY driving up to 10 Gbps each (2x 4-lane, 2.5 Gbps/lane and one mux'd with DSI) • ISP up to 500 Mpixels/s (1x 4Kp60, 2x 4Kp30, 4x 1080p60, or 8x 1080p30) • Up to 8x cameras with MIPI virtual channels • Supports RGB-IR camera • 96 kByte of SRAM, but it is available for other SoC usage when not using for ISP purposes
Audio	• 5x Synchronous Audio Interfaces (SAI) • 17-lane I2S TDM (32-bit at 768 kHz frequency) • SPDIF Rx and SPDIF Tx • 8-channel PDM Microphone Interface (MICFIL)

Table continues on the next page...

Table 1. Feature summary*...continued*

Subsystem	Features
	• 2 x Medium Quality Sound (MQS)
Connectivity	• 19 x 19 mm package with 2x 1-lane PCIe Gen 3.0 and 15 x 15 mm package with 1x 1-lane PCIe Gen3.0 • 1x USB3.0 Type C with PHY • 1x USB2.0 with PHY • 2x 1 Gbps Ethernet ports with Time Sensitive Networking (TSN) capabilities • 1x 10 Gbps Ethernet port with Time Sensitive Networking (TSN) capabilities for 19 x 19 mm package only • IEEE 1588 for sync; and EEE • 5x CAN-FD • 2x 32-pin FLEXIO interfaces (bus or serial I/O)
Low Speed Communication Peripherals	• 8x UART
Timer and PWMs	• 2x Low Power Periodical Interrupt Timers (LPIT) — 4-channel — 4 external trigger sources — Generic 32-bit resolution timer — Periodical interrupt generation • 6x Timer/PWM modules (TPM) — Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128 — 16-bit counter, support free-running counter or modulo counter mode, counting up or down — Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode • 2x Low-Power Timers (LPTMR) • 5x WatchDog modules (WDOG) • 1x System Counter (SYS_CTR) • 1x Timestamp Timer (TSTMR) • 1x General Purpose Timer (GPT)
GPIO and Pin Multiplexing	• General-purpose input/output (GPIO) modules with interrupt capability • Input/Output Multiplexing Controller (IOMUXC) to provide centralized pad control
Analog	• FRO Clock Generator (FRO_TUNER) • 2x Temperature Sensor (TEMPSENSE)

Table continues on the next page...

Table 1. Feature summary...*continued*

Subsystem	Features
	• 16-channel, 12-bit Analog-to-Digital Converter (SAR_ADC) • 1x Trigger Mux (TRGMUX) to configure the trigger inputs for various peripherals
Clocking	• CCM • OSC • LPCG
Safety	• Integrated functional safety • Targeting ISO26262 ASIL-B and IEC61508 SIL2 compliance
Security	• Trusted Resource Domain Controller (TRDC) — Supports up to 16 resource domains • Arm TrustZone® (TZ) architecture • Secure and trusted access control • EdgeLock™ Secure Enclave • Evolved on-die security with run-time attestation, silicon root of trust, trust provisioning, fine-grain key management augmented by extensive crypto services
System Debug	• Arm CoreSight® debug and trace architecture • Trace Port Interface Unit (TPIU) to support off-chip real-time trace • Support for 4-pin (JTAG) and SWD debug interfaces
Power management	• Supports PMIC integration to supply all power rails • Multiple power domains allow power gating of most digital and analog logic in low power mode • General Power Controller (GPC), several factors are involved in power management, not just a central controller
Package	• 15 x 15 mm FCBGA, 0.5 mm pitch • 19 x 19 mm FCBGA, 0.7 mm pitch

1.1 Ordering Information

Figure 1 describes the part number nomenclature, so the users can identify the characteristics of the specific part number.

Part Numbers See following slides for list of planned parts by family segment. Not every combination of package, temperature qualification, core count, and feature enablement is available.

Part Type	i.MX Family	Segment	A-Core Qty.	Temp. Qual.	Package	Reserved	A-Core Freq	Special Config	Silicon Revision
P	IMX95	9	6	A	VZ	X	N	A	C

Segment	Short Description	A-Cores Qty	ISP	NPU	GPU	VPU	Display Interfaces[8]	Safety Enab[2]	Temp. Qual.	Packages[3]
9	Full Featured /Vision	6 / 4	√	√	√	√	√		A/C/D[8]/X	VT/VZ[8]
8	Full Featured /Vision + Safety	6	√	√	√	√	√	ASIL-B SIL2[1]	A/X	VT/VZ
5	HMI	6 / 4		√	√	√	√		A/C/D/X	VT/VZ
4	HMI + Safety	6		√	√	√	√	ASIL-B SIL2[1]	A/X	VZ
3	Compute	6 / 4		√					A/C/D[8]/X	VT/VZ[8]

FCBGA Package Type	
VT	15 x 15 mm, 0.5 mm pitch, no lid
VY[6]	19 x 19 mm, 0.7mm pitch, lidded
VZ	19 x 19 mm, 0.7mm pitch, no lid

Cortex-A55 CPU Frequency	
Q	2.0 GHz[2]
N	1.8 GHz

Silicon Revision[4]	
A	Rev 1.0 (A0)
B	Rev 2.0 (A1)
C	Rev 3.0 (B0)

Special Configuration[5]	
A	SDP on USB1
B	SDP on USB2

Part Type	
P	Sample
M	Mass Production
S	Special

Cortex-A Cores	
6	6 Cores
4	4 Cores

Temperature Qualification	
A	Automotive: -40°C T_a to 125°C T_j
C	Industrial: -40°C T_a to 105°C T_j
D	Commercial 0°C T_a to 95°C T_j
X	Extended Industrial: -40°C T_a to 125°C T_j

1. NXP compliant paid safety SW - ASIL-B (IMX95-DP-ASIL) for Auto qual or SIL2 (IMX9-DP-SIL) for Ext Ind
2. Non-compliant building blocks for SIL available on all non-Auto PNs
3. 10Gb Ethernet is available on all VZ (19x19) packages but not VT (15x15) due to pin-mux restrictions.
4. A0 is obsolete. A1 is shipping and supported until B0 is available. B0 is the production revision.
5. See following slides for explanation.
6. Lidded availability discussed on a case-by-case basis
7. Some vision applications use the GPU, so consider Full Featured in that case
8. 2.0GHz A-Core frequency available in i.MX 95 19x19 package (VZ) with Commercial Qualification only and requires a suitable thermal solution to maintain operating environment between 0°C Ta and 95°C Tj in Super Overdrive mode

Figure 1. Part number nomenclature - i.MX 95

Table 2 shows the list of part numbers covered by this data sheet as of its publication. Please consult https://www.nxp.com/products/i.MX95 for a current list of all part numbers.

Table 2. Orderable part numbers

Part Number	Segment	A-Cores	Temp Qual	Package	A-Core Freq	Special Config	Silicon Rev	ISP	NPU	GPU	VPU	Display
MIMX9596CVZXNBC	Full	6	Industrial	19x19 No Lid	1.8GHz	SDP on USB2	B0	Y	Y	Y	Y	Y
MIMX9596CVZXNAC	Full	6	Industrial	19x19 No Lid	1.8GHz	SDP on USB1	B0	Y	Y	Y	Y	Y
MIMX9596CVTXNAC	Full	6	Industrial	15x15 No lid	1.8GHz	SDP on USB1	B0	Y	Y	Y	Y	Y
MIMX9594CVZXNBC	Full	4	Industrial	19x19 No Lid	1.8GHz	SDP on USB2	B0	Y	Y	Y	Y	Y

Table continues on the next page...

Table 2. Orderable part numbers*...continued*

Part Number	Segment	A-Cores	Temp Qual	Package	A-Core Freq	Special Config	Silicon Rev	ISP	NPU	GPU	VPU	Display
MIMX9594CVZXNAC	Full	4	Industrial	19x19 No Lid	1.8GHz	SDP on USB1	B0	Y	Y	Y	Y	Y
MIMX9594CVTXNAC	Full	4	Industrial	15x15 No lid	1.8GHz	SDP on USB1	B0	Y	Y	Y	Y	Y
MIMX9556CVZXNBC	HMI	6	Industrial	19x19 No Lid	1.8GHz	SDP on USB2	B0	N	Y	Y	Y	Y
MIMX9556CVZXNAC	HMI	6	Industrial	19x19 No Lid	1.8GHz	SDP on USB1	B0	N	Y	Y	Y	Y
MIMX9556CVTXNAC	HMI	6	Industrial	15x15 No lid	1.8GHz	SDP on USB1	B0	N	Y	Y	Y	Y
MIMX9556CVTXNBC	HMI	6	Industrial	15x15 No lid	1.8GHz	SDP on USB2	B0	N	Y	Y	Y	Y
MIMX9554CVZXNBC	HMI	4	Industrial	19x19 No Lid	1.8GHz	SDP on USB2	B0	N	Y	Y	Y	Y
MIMX9554CVZXNAC	HMI	4	Industrial	19x19 No Lid	1.8GHz	SDP on USB1	B0	N	Y	Y	Y	Y
MIMX9554CVTXNAC	HMI	4	Industrial	15x15 No lid	1.8GHz	SDP on USB1	B0	N	Y	Y	Y	Y
MIMX9536CVZXNBC	Compute	6	Industrial	19x19 No Lid	1.8GHz	SDP on USB2	B0	N	Y	N	N	N
MIMX9536CVZXNAC	Compute	6	Industrial	19x19 No Lid	1.8GHz	SDP on USB1	B0	N	Y	N	N	N
MIMX9536CVTXNBC	Compute	6	Industrial	15x15 No lid	1.8GHz	SDP on USB2	B0	N	Y	N	N	N
MIMX9534CVZXNBC	Compute	4	Industrial	19x19 No Lid	1.8GHz	SDP on USB2	B0	N	Y	N	N	N

Table continues on the next page...

Table 2. Orderable part numbers*...continued*

Part Number	Segment	A-Cores	Temp Qual	Package	A-Core Freq	Special Config	Silicon Rev	ISP	NPU	GPU	VPU	Display
MIMX9534CVZXNAC	Compute	4	Industrial	19x19 No Lid	1.8GHz	SDP on USB1	B0	N	Y	N	N	N
MIMX9534CVTXNAC	Compute	4	Industrial	15x15 No lid	1.8GHz	SDP on USB1	B0	N	Y	N	N	N

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/IMX or contact an NXP representative for details.

1.2 Part marking

Parts are marked as in the example shown in this figure.

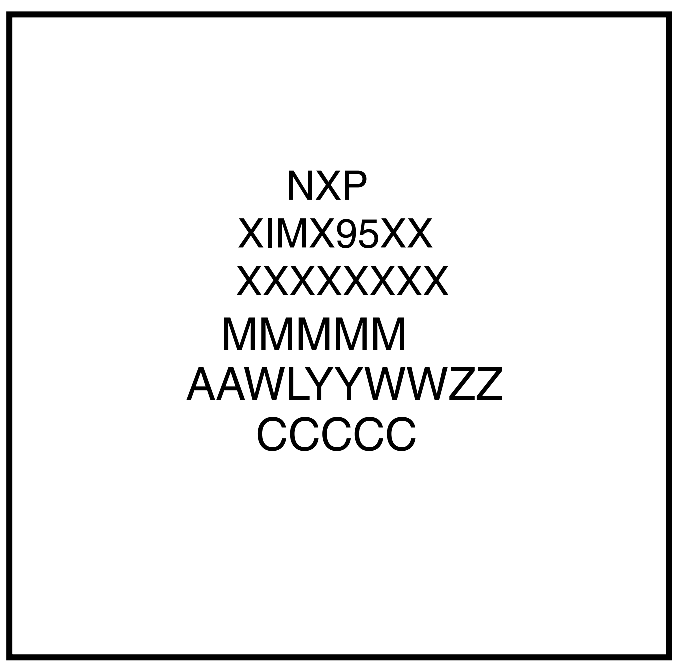


Figure 2. Part marking for FCBGA package

Legend:

- XIMX95XX is the first half of the part number
- XXXXXXXX is the second half of the part number (full part number is on one line for lidded packages)
- MMMMM is the mask number
- CCCCC is the country code
- AAWLYYWWZZ

— AA is the assembly lot ID
— WL is the wafer lot ID
— YY is year
— WW is work week
— ZZ is an additional identifier

2 Block Diagram

Figure 3 shows the functional modules in the i.MX 95 processor system.

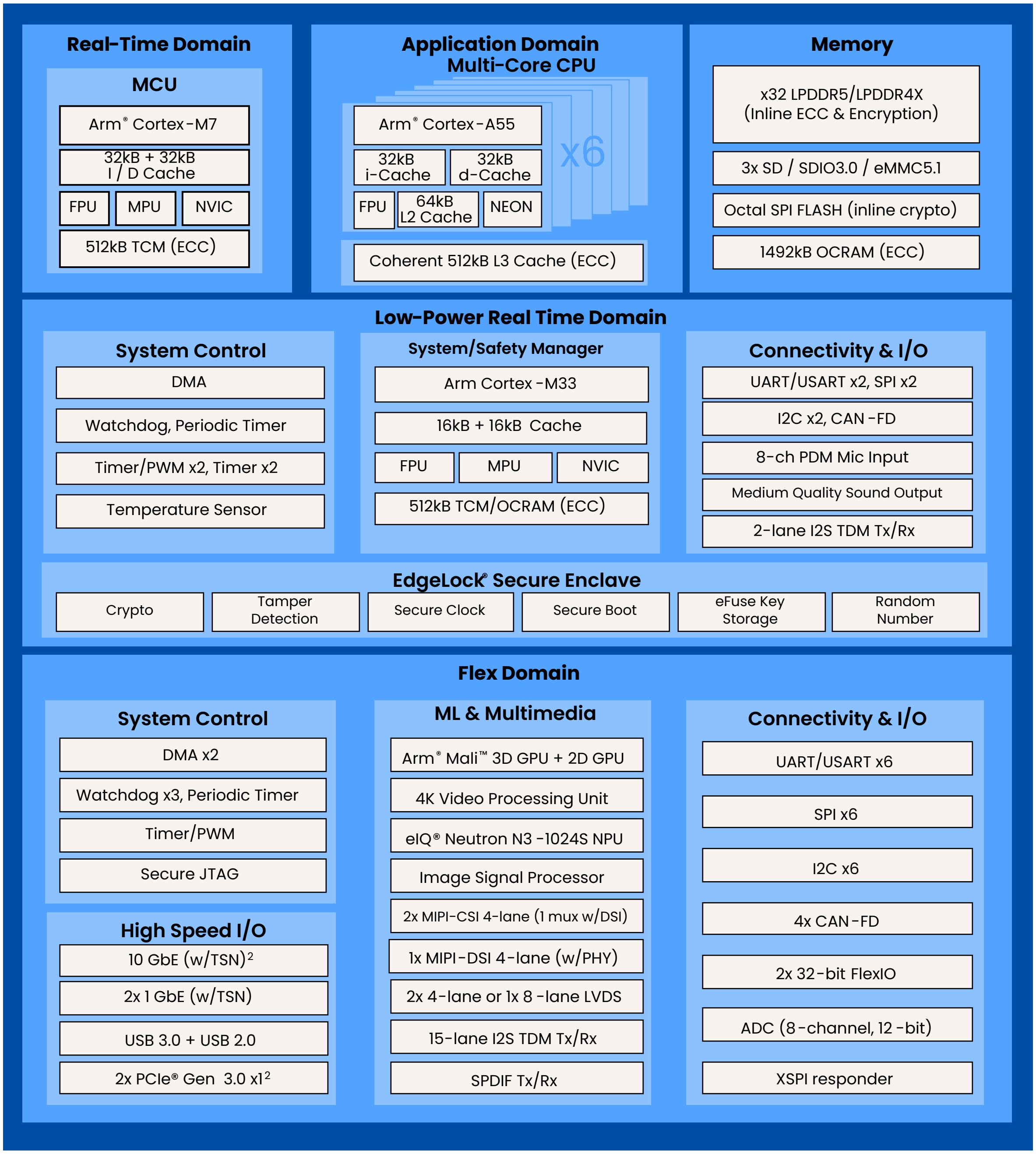


Figure 3. i.MX 95 system block diagram

Note:

1. *Above figure represents 19 x 19 mm package.*
2. *15 x 15 mm package supports 1 PCIe and does not have 10 GbE.*
3. *Some modules shown in this block diagram are not offered on all derivatives.*

3 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 95 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section, "Package information and contact assignments”. Signal descriptions are provided in the i.MX 95 Reference Manual (IMX95RM).

Table 3. Special signal considerations

Signal Name	Remarks
CLKIN1/CLKIN2	CLKIN1 and CLKIN2 are input pins without internal pull-up and pull-down.
NC	These signals are No Connect (NC) and should be unconnected in the application.
ONOFF	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
POR_B	POR_B has no internal pull-up/down resistor, and requires external pull-up resistor to NVCC_BBSM. It is recommended that POR_B is properly handled during power up/down. Please refer to the EVK design for details.
RTC_XTALI/ RTC_XTALO	RTC_XTALI and RTC_XTALO can be coupled to an external crystal element to generate 32.768K clock. Care must be taken to account parasitic capacitance of the pins in order to match the trimmed crystal assumptions for frequency accuracy. Care should also be taken to limit the parasitic leakage on or between RTC_XTALI and RTC_XTALO. This can debias the integrated amplifier resulting in reduced startup margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_ANA_1P8 level and the frequency shall be < 50 kHz under the typical conditions.
XTALI_24M/ XTALO_24M	The system requires a 24 MHz clock to operate. A 24 MHz crystal can be created by coupling an appropriately tuned quartz element to XTALI and XTALO. Care must be taken that the resulting oscillation frequency complies with the utilized serial interface standards such as PCIe and USB.

3.1 Unused input and output guidance

If a function of the i.MX 95 is not used, the I/Os and power rails of that function can be terminated to reduce overall board power.

Table 4. Unused function strapping recommendations for LVDS

Function	Pin name	Recommendations if unused
Single LVDS0	LVDS0_CLK_P, LVDS0_CLK_N, LVDS0_Dx_P, LVDS0_Dx_N	Not connected
Single LVDS1	LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N	Not connected
Both LVDS0 and LVDS1	LVDS0_CLK_P, LVDS0_CLK_N, LVDS0_Dx_P, LVDS0_Dx_N, LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N,	Not connected
	VDD_LVDS_1P8	Tie to ground using a 10K resistor

Table 5. Unused function strapping recommendations for MIPI

Function	Pin name	Recommendations if unused
MIPI_DSICSI1	MIPI_DSICSI1_CLK_P, MIPI_DSICSI1_CLK_N, MIPI_DSICSI1_DX_P, MIPI_DSICSI1_DX_N,	Not connected
MIPI_CSI1	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_DX_P, MIPI_CSI1_DX_N,	Not connected
Both MIPI_CSI1 and MIPI_DSICSI1	MIPI_REXT, MIPI_DSICSI1_CLK_P, MIPI_DSICSI1_CLK_N, MIPI_DSICSI1_DX_P, MIPI_DSICSI1_DX_N, MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_DX_P, MIPI_CSI1_DX_N,	Not connected
	VDD_MIPI_1P8, VDD_MIPI_0P8,	Tie to ground using a 10K resistor

Table 6. Unused function strapping recommendations for USB

Function	Pin name	Recommendations if unused
USB1	USB1_VBUS, USB1_DNU, USB1_D_P, USB1_D_N, USB1_TX0, USB1_RX0, USB1_TX1, USB1_RX1, USB1_TXRTUNE	Not connected
USB2	USB2_VBUS, USB2_ID, USB2_D_P, USB2_D_N, USB2_TXRTUNE	Not connected
Both USB1 and USB2	USB1_VBUS, USB1_DNU, USB1_D_P, USB1_D_N, USB1_TX0, USB1_RX0, USB1_TX1, USB1_RX1, USB1_TXRTUNE, USB2_VBUS, USB2_ID, USB2_D_P, USB2_D_N, USB2_TXRTUNE,	Not connected
	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Tie to ground using a 10K resistor

Table 7. Unused function strapping recommendations for PCIe

Function	Pin name	Recommendations if unused
Single PCIE1	PCIE1_TX0_P, PCIE1_TX0_N, PCIE1_RX0_P, PCIE1_RX0_N,	Not connected
	PCIE1_REF_PAD_CLK_P, PCIE1_REF_PAD_CLK_N	Tie to ground using a 10K resistor
Single PCIE2	PCIE2_TX0_P, PCIE2_TX0_N, PCIE2_RX0_P, PCIE2_RX0_N,	Not connected
	PCIE2_REF_PAD_CLK_P, PCIE2_REF_PAD_CLK_N	Tie to ground uisng a 10K resistor

Table continues on the next page...

Table 7. Unused function strapping recommendations for PCIe...*continued*

Function	Pin name	Recommendations if unused
Both PCIE1 and PCIE2	PCIE1_TX0_P, PCIE1_TX0_N, PCIE1_RX0_P, PCIE1_RX0_N, PCIE2_TX0_P, PCIE2_TX0_N, PCIE2_RX0_P, PCIE2_RX0_N, PCIE_RESREF	Not connected
	VDD_PCI_1P8, VDD_PCI_0P8	Tie to ground uisng a 10K resistor
	PCIE1_REF_PAD_CLK_P, PCIE1_REF_PAD_CLK_N, PCIE2_REF_PAD_CLK_P, PCIE2_REF_PAD_CLK_N	Tie to ground using a 10K resistor
	PCIE_REF_OUT_CLK_P, PCIE_REF_OUT_CLK_N[1]	Not connected

[1] PCIE_REF_OUT_CLK can be configured as *Disabled* when unused.

Table 8. Unused function strapping recommendations for Audio Transceiver

Function	Pin name	Recommendations if unused
Audio transceiver unused	AUD_AUX, AUD_P_UTIL, AUD_N_HPD	Not connected
	VDD_AUD_1P8	Should be supplied

Table 9. Unused function strapping recommendations for 10G ETH Serdes

Function	Pin name	Recommendations if unused
10G ETH Serdes	ETH_TX0_P, ETH_TX0_N, ETH_RX0_P, ETH_RX0_N, ETH_RESREF, ETH_REF_PAD_CLK_P, ETH_REF_PAD_CLK_N	Not connected
	VDD_ETH_1P8, VDD_ETH_0P8	Tie to ground using a 10K resistor

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 95 family of processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 10 for a quick reference to the individual tables and sections.

Table 10. i.MX 95 chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	See Absolute maximum ratings
Thermal resistance	See Thermal resistance

Table continues on the next page...

Table 10. i.MX 95 chip-level conditions...*continued*

For these characteristics, …	Topic appears …
Operating ranges	See Operating ranges
Clock sources	See Clock source
Power modes	See Power modes
Power supplies requirements and restrictions	See Power supplies requirements and restrictions

4.1.1 Absolute maximum ratings

CAUTION: Stresses beyond those listed in the following table may reduce the operating lifetime or cause immediate permanent damage to the device. The table below does not imply functional operation beyond those indicated in the operating ranges and parameters table.

Table 11. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_ARM	Core supplies input voltages	-0.3	—	1.12	V	—	—
VDD_SOC	Core supplies input voltages	-0.3	—	1.08	V	—	—
NVCC_SD2	IO supply for SD2	-0.3	—	3.96	V	—	—
VDD2H_DDR	DDR I/O supply voltage	-0.3	—	1.32	V	—	—
VDDQ_DDR	DDR I/O supply voltage	-0.3	—	0.72	V	—	—
VDD_DDR_0P8	DDR I/O supply voltage	-0.3	—	0.96	V	—	—
NVCC_CCM_DAP	CCM supply voltage [1]	-0.3	—	3.96	V	—	—
NVCC_BBSM_1P8	IO supply and IO Pre-driver supply for BBSM bank	-0.3	—	2.16	V	—	—
USB1_VBUS, USB2_VBUS	USB VBUS input detected	-0.3	—	3.96	V	—	—
VDD_USB_0P8	Power for USB OTG PHY	-0.3	—	0.96	V	—	—
VDD_USB_1P8	Power for USB OTG PHY	-0.3	—	2.16	V	—	—
VDD_USB_3P3	Power for USB OTG PHY	-0.3	—	3.96	V	—	—

Table continues on the next page...

Table 11. Absolute maximum ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_MIPI_0P8	MIPI PHY supply voltage	-0.3	—	0.96	V	—	—
VDD_MIPI_1P8	MIPI PHY supply voltage	-0.3	—	2.16	V	—	—
VDD_PCI_0P8	PCI PHY supply voltage	-0.3	—	0.96	V	—	—
VDD_PCI_1P8	PCI PHY supply voltage	-0.3	—	2.16	V	—	—
VDD_AUD_1P8	Audio transceiver supply voltage	-0.3	—	2.16	V	—	—
NVCC_GPIO, NVCC_WAKEUP, NVCC_AON, NVCC_ENET	GPIO supply voltage	-0.3	—	3.96	V	—	—
VDD_ETH_0P8	Digital supply for Ethernet PHY	-0.3	—	0.96	V	—	—
VDD_ETH_1P8	I/O voltage supply and analog high voltage power supply [1]	-0.3	—	2.16	V	—	—
VDD_LVDS_1P8	LVDS PHY supply voltage	-0.3	—	2.16	V	—	—
VDD_ANA_0P8	Analog core supply voltage	-0.3	—	0.96	V	—	—
VDD_ANA_1P8	Analog core supply voltage [1]	-0.3	—	2.16	V	—	—
VDD_ANAVDET_1P8	Analog core supply voltage	-0.3	—	2.16	V	—	—
Vin/Vout	Input/output voltage range [2]	-0.3	—	NVCC_XXX + 0.3	V	—	—
TSTORAGE	Storage temperature range	-55	—	150	°C	—	—

[1] This supply being incorrect can cause the IO pads to be misconfigured causing damage.
[2] Input Voltages to the GPIO must be no lower than -300mV and no higher than NVCC +300mV, where the NVCC is the GPIO supply operational voltage seen at the SoC. These offsets are inclusive of any DC offsets from the driving IC or AC transients (overshoots or undershoots) seen during signal switching

4.1.2 Electrostatic discharge and latch-up ratings

Table 12. Electrostatic discharge and latch-up ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHBM	Electrostatic Discharge (ESD): Human Body Model (HBM) [1]	-1000	—	1000	V	—	—
VCDM	Electrostatic Discharge (ESD): Charged Device Model (CDM) [2]	-250	—	250	V	—	—
ILAT	Latch UP (LU) Immunity level: Class II at 105 °C ambient [3]	-100	—	100	mA	—	—

[1] Determined according to JEDEC Standard JS001, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
[2] Determined according to JEDEC Standard JS002, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
[3] Determined according to JEDEC Standard JESD78, IC Latch-up Test.

4.1.3 Thermal resistance

4.1.3.1 15 x 15 mm FCBGA package thermal characteristics

Table 13 displays the 15 x 15 mm FCBGA package thermal resistance data.

Table 13. 15 x 15 mm FCBGA thermal resistance data

Rating	Board Type[1]	Symbol	Value	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	15.7	°C/W
Junction-to-Top of Package Thermal Characterization parameter[2]	JESD51-9, 2s2p	Ψ_{JT}	0.1	°C/W
Junction to Case Thermal Resistance[3]	N/A	$R_{\theta JC}$	0.2	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9). Test board has 40 vias under die shadow mapped according to BGA layout under die. Each vias is 0.2 mm in diameter and connects top layer with the first buried plane layer.
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment.
[3] Junction-to-Case (top) thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface temperature.

4.1.3.2 19 x 19 mm FCBGA package thermal characteristics

Table 14 displays the 19 x 19 mm FCBGA package thermal resistance data.

Table 14. 19 x 19 mm FCBGA thermal resistance data

Rating	Board type[1]	Symbol	Value		Unit
			Bare die	Lidded	
Junction to Ambient thermal resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	13.4	12.3	°C/W
Junction-to-Top of package thermal characterization parameter[2]	JESD51-9, 2s2p	Ψ_{JT}	0.1	0.4	°C/W
Junction to Case thermal resistance[3]	JESD51-9, 1s	$R_{\theta JC}$	0.2	0.6	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface.

4.1.4 Power architecture

The i.MX power architecture is designed with the expectation that a dedicated PMIC supplies all required power rails, ensuring compliance with stringent power-up and power-down sequencing requirements. While discrete component-based implementations are technically viable, they typically lead to increased BOM cost, greater design complexity, and a larger PCB footprint. In contrast, the proposed PMIC solution is BOM-optimized, minimizes board area by integrating multiple power functions into a single package, and simplifies system design by providing a validated, production-tested power management solution that inherently meets the voltage and sequencing specifications of the i.MX platform.

NVCC_BBSM_1P8 must be powered first and stay until the last.

Majority of the digital logic is supplied with two supplies: VDD_ARM and VDD_SOC.

- VDD_ARM is for the CORTEXAMIX.
- VDD_SOC is for the rest of the modules in SoC.

The VDD_SOC has following modes:

- Overdrive mode
- Nominal mode
- Underdrive mode
- Suspend mode

GPIO interfaces functionally only need to operate at 1.8 V. One exception is the SD card interface, which must support both 1.8 V and 3.3 V (for compatibility with legacy 3.3 V SD cards), as well as the “GPIO” pins that may be connected to a EXPI(2x20-pin Expansion interface) (which for compatibility with components in the ecosystem need to be able to support 3.3 V, while also needing to support 1.8 V for 1.8 V-optimized designs).

The DRAM controller and PHY have multiple external power supplies:

Table 15. Power supplies of the DRAM controller and PHY

Power supplies	Modules
VDD_SOC	SoC synthesized DRAM controller digital logic
VDD_ANA_0P8/VDD_DDR_0P8	DRAM PLL and PHY digital logic
VDD_ANA_1P8	DRAM PLL and PHY analog circuitry

Table continues on the next page...

Table 15. Power supplies of the DRAM controller and PHY*...continued*

Power supplies	Modules
VDD2H_DDR	DRAM PHY I/O supply (1.1 V for LPDDR4X and 1.05 V for LPDDR5)
VDDQ_DDR	DRAM PHY I/O supply (0.6 V for LPDDR4X and 0.5 V for LPDDR5)

For all the integrated analog modules, their 1.8 V analog power will be supplied externally through power pads. These supplies are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For the integrated LVDS PHY, PCIe PHY, and USB PHYs, their 3.3 V (where supported), 1.8 V and their digital power will be supplied externally through power pads. The powers to those PHYs are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For BBSM/RTC, the 1.8 V IO pre-driver supply and 1.8 V IO pad supply will also be supplied externally. The BBSM_LP core digital domain logic is supplied by an internal LDO.

Figure 4 is the power architecture diagram for the whole chip. Note that it only shows power supplies and does not show capacitors that may be required for internal LDO regulators.

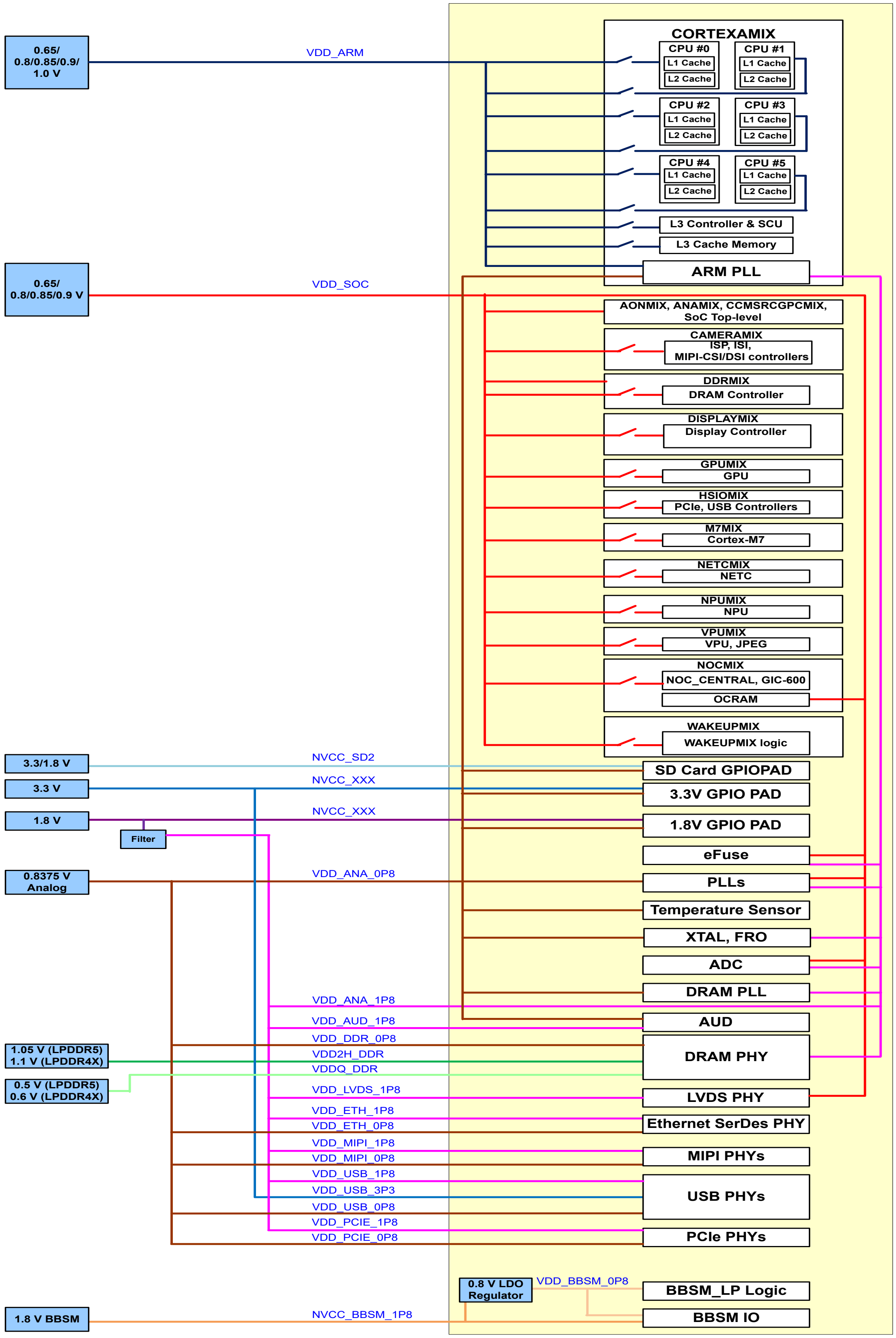


Figure 4. Power architecture of i.MX 95 family of processors

4.1.4.1 Ramp rate specifications

Table 16. Ramp rate specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD[VDD_SOC, VDD_ARM], VDD_ANA_0P8	Power supply for SoC logic, Cortext-A-55 core, PLLs, temperature sensor, and LVCMOS I/O	0.1	—	30	V/ms	Voltage level = 0.8 V	—
VDDQ_DDR / VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X PHY, LPDDR5/ LPDDR4X mode	0.1	—	5	V/ms	Voltage level = 0.6 V / 1.1 V	—
VDD_ANA_1P8/ VDD_ANAVDET_ 1P8/VREFH_1P8_ ADC	1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, ADC, and 24 MHz XTAL	0.1	—	5	V/ms	Voltage level = 1.8 V	—
VDD_USB_3P3	3.3 V supply for USB PHY	0.1	—	30	V/ms	Voltage level = 3.3 V	—
NVCC_XXX	Power supply for GPIO	0.1	—	5	V/ms	Voltage level = 1.8 V	—
NVCC_XXX	Power supply for GPIO	0.1	—	30	V/ms	Voltage level = 3.3 V	—
NVCC_BBSM_1P8	I/O supply for GPIO in BBSM bank	0.1	—	30	V/ms	Voltage level = 1.8 V	—

4.1.5 Power modes

This section introduces the power modes used in the i.MX 95.

4.1.5.1 Power mode definition

The i.MX 95 supports the following power modes:

- RUN Mode: All external power rails are on, the Cortex-A55 is active and running; other internal modules can be on/off based on application.
- Low Power RUN Mode: This mode is defined as a very low power run mode with all external power rails are on. In this mode, all the unnecessary power domain (MIX) can be off, except AONMIX and M7MIX. Cortex-M33 CPU in AONMIX runs System Manager and Cortex-M7 CPU in M7MIX handles all the computing and data processing. Cortex-A55 is power down and DRAM can be in self-refresh/retention mode. To use modules in other power domain, such as WAKEUPMIX, the user can turn on additional peripherals and related power as needed. Additional low power modes are also supported, but do not have power characterized in the Data Sheet. Refer to the Reference Manual for a full set of power management capabilities.
- IDLE Mode: This mode is defined as a mode, which the Cortex-A55 can automatically enter when there is no thread running and all high-speed devices are not active. The Cortex-A55 can be put into power gated state but with L3 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated, but still remains powered. Compared with RUN mode, all the external power rails from the PMIC remain the same and most of the modules still remain in their state, so the interrupt response in this mode is very small.

- SUSPEND Mode: This mode is defined as the most power saving mode where all the clocks are off (including the Cortex-M33 CPU, which is in AONMIX and cannot be power gated), all the unnecessary power supplies are off and all power gateable portions of the SoC are power gated. The Cortex-A55 CPUs and the Cortex-M7 CPU are fully power gated, all internal digital logic and analog circuit that can be powered down will be off, all PHYs are power gated. DRAM is set at self-refresh/retention mode. VDD_SOC (and related digital supply) voltage is reduced to the “Suspend mode” voltage. The exit time from this mode will be much longer than IDLE, but the power consumption will also be much lower.
- BBSM Mode: This mode is also called RTC mode. Only the power for the Battery Backed non-Secure Module (BBNSM) and Battery Backed Secure Module (BBSM) remain on to keep RTC, BBNSM and BBSM logic are alive.
- OFF Mode: All power rails are off.

Note: *Beyond the modes defined here, additional options can be configured in software, such as to adjust clock frequencies or gate clocks through the CCM programming model, or to adjust on-die power-gating through the SRC or GPC programming model, or to adjust the voltage supplied to the VDD_SOC and VDD_ARM supplies as per* Operating ranges *in the Data Sheet.*
Note: *These power modes are different than the voltage mode ranges.*

Table 17 summarizes the external power supply states in all the power modes.

Table 17. The power supply states

Power rail	OFF	BBSM	SUSPEND	IDLE	RUN/LP RUN	SUSPEND (With VDD_DDR_0P8 OFF)
NVCC_BBSM_1P8	OFF	ON	ON	ON	ON	ON
VDD_ARM	OFF	OFF	OFF or ON [1]	ON	ON	OFF or ON [1]
VDD_SOC	OFF	OFF	ON	ON	ON	ON
VDD2_DDR VDDQ_DDR	OFF	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON	ON
VDD_ANA_0P8 VDD_DDR_0P8 VDD_ETH_0P8 VDD_MIPI_0P8 VDD_PCI_0P8 VDD_USB_0P8	OFF	OFF	ON	ON	ON	ON[2]
VDD_ANA_1P8/ VDD_ANAVDET_1P8 VDD_AUD_1P8 VDD_ETH_1P8	OFF	OFF	ON	ON	ON	ON

Table continues on the next page...

Table 17. The power supply states...*continued*

Power rail	OFF	BBSM	SUSPEND	IDLE	RUN/LP RUN	SUSPEND (With VDD_DDR_0P8 OFF)
VDD_LVDS_1P8						
VDD_MIPI_1P8 VDD_PCI_1P8	OFF	OFF	ON	ON	ON	ON
VDD_USB_1P8 VDD_USB_3P3	OFF	OFF	ON	ON	ON	ON

[1] When SoC in a low power state, it can save more power when configuring PMIC to turn VDD_ARM off vs having the PMIC continue to supply VDD_ARM and rely on the on-die powergating around the CORTEXAMIX components.
[2] Only VDD_DDR_0P8 is OFF

4.1.5.2 Low power modes

The following table shows the state of each module in Idle mode, Suspend mode, and BBSM mode.

Table 18. Module states in low-power modes

Module	Idle	Suspend	BBSM
CCM LPM mode	Wait	Stop	N/A
Arm A55 CPU0*	Off	Off	Off
Shared L3 cache	On	Off	Off
CAMERAMIX DISPLAYMIX GPUMIX NPUMIX VPUMIX M7MIX	On as needed	Off	Off
DRAM controller and PHY	On	Off	Off
ARM_PLL	Off	Off	Off
DRAM_PLL	Off	Off	Off
SYSTEM_PLL1	On	Off	Off
XTAL	On	Off	Off
RTC	On	On	On
External DRAM device	Self-Refresh mode	Self-Refresh mode	Off
DRAM clock	266 MHz	Off	Off
AXI clock	133 MHz	Off	Off

Table continues on the next page...

Table 18. Module states in low-power modes*...continued*

Module	Idle	Suspend	BBSM
Module clocks	On as needed	Off	Off
GPIO wake-up	Yes	Yes	No
RTC wake-up	Yes	Yes	Yes
USB remote wake-up	Yes	No	No
Other wake-up source	Yes	No	No

4.1.5.3 Chip power in different Low Power modes

The table below shows power consumption in different LP modes.

Note: *To achieve this low power consumption values for I/O power rails in SUSPEND mode, it is recommended to configure the IOMUX of those pins to GPIO input and change the PAD control settings to pull-up or pull-down depends on the board design before entering SUSPEND mode.*

Table 19. BBSM Mode

Supply	Voltage (V)	Typical power (mw)[1]	Maximum power (mw)[1]
NVCC_BBSM_1P8	1.80	0.132	0.196

[1] The BBSM power numbers are based on bench measurement values with deviations derived from statistical limits.

Table 20. SUSPEND Mode

Supply	Voltage (V)	Typical power (mw)[1]	Maximum power (mw)[1]
VDDQ_DDR	0.50	0.030	0.140
VDD_SOC [2]	0.65	6.970	25.000
VDD_DDR_0P8[2]	0.80	9.740	36.000
VDD_ETH_0P8	0.80	0.690	1.870
VDD_MIPI_0P8	0.80	0.820	2.090
VDD_PCI_0P8	0.80	0.560	1.770
VDD_USB_0P8	0.80	0.480	1.530
VDD_ANA_0P8	0.80	0.540	0.950
VDD2H_DDR	1.05	0.170	0.180
NVCC_BBSM_1P8	1.80	0.190	0.270
NVCC_ENET	1.80	0.190	0.200
NVCC_WAKEUP	1.80	0.920	1.610
VDD_ANA_1P8	1.80	1.400	2.310
VDD_ANA_VDET_1P8	1.80	0.150	0.170
VDD_ETH_1P8	1.80	0.040	0.040
VDD_LVDS_1P8	1.80	0.050	0.100

Table continues on the next page...

Table 20. SUSPEND Mode*...continued*

Supply	Voltage (V)	Typical power (mw)[1]	Maximum power (mw)[1]
VDD_MIPI_1P8	1.80	0.010	0.030
VDD_PCI_1P8	1.80	0.020	0.040
VDD_USB_1P8	1.80	0.030	0.040
VDD_AUD_1P8	1.80	0.130	0.180
NVCC_CCM_DAP	3.30	0.650	1.010
NVCC_GPIO	3.30	2.460	2.980
NVCC_SD2	3.30	1.420	2.220
VDD_AON	3.30	1.960	2.170
VDD_USB_3P3	3.30	1.100	1.210
Total		30.72	84.11

[1] All power measurement numbers are collected at 25°C Tj based on characterization and values are use case dependent.
[2] VDD_SOC and VDD_DDR_0P8 power measurements are tested in production.

Table 21. SUSPEND Mode with DDR Off

Supply	Voltage (V)	Typical power (mw)[1]	Maximum power (mw)
VDDQ_DDR[2]	0.50	0.360	0.940
VDD_SOC[3]	0.65	6.970	25.000
VDD_DDR_0P8	0.00	0.000	0.000
VDD_ETH_0P8	0.80	0.690	1.870
VDD_MIPI_0P8	0.80	0.820	2.090
VDD_PCI_0P8	0.80	0.560	1.770
VDD_USB_0P8	0.80	0.480	1.530
VDD_ANA_0P8	0.80	0.540	0.950
VDD2H_DDR	1.05	0.170	0.180
NVCC_BBSM_1P8	1.80	0.190	0.270
NVCC_ENET	1.80	0.190	0.200
NVCC_WAKEUP	1.80	0.920	1.610
VDD_ANA_1P8	1.80	1.400	2.310
VDD_ANA_VDET_1P8	1.80	0.150	0.170
VDD_ETH_1P8	1.80	0.040	0.040
VDD_LVDS_1P8	1.80	0.050	0.100
VDD_MIPI_1P8	1.80	0.010	0.030
VDD_PCI_1P8	1.80	0.020	0.040
VDD_USB_1P8	1.80	0.030	0.040

Table continues on the next page...

Table 21. SUSPEND Mode with DDR Off*...continued*

Supply	Voltage (V)	Typical power (mw)[1]	Maximum power (mw)
VDD_AUD_1P8	1.80	0.130	0.180
NVCC_CCM_DAP	3.30	0.650	1.010
NVCC_GPIO	3.30	2.460	2.980
NVCC_SD2	3.30	1.420	2.220
VDD_AON	3.30	1.960	2.170
VDD_USB_3P3	3.30	1.100	1.210
Total		21.31	48.91

[1] All power measurement numbers are collected at 25°C Tj based on characterization and values are use case dependent.
[2] A small and innocuous increase in VDDQ_DDR current occurs when VDD_DDR_0P8 is powered down due to reverse biased diode voltage.
[3] VDD_SOC power measurements are tested in production.

4.1.6 Operating ranges

The following table provides the operating ranges of the i.MX 95 processors. For details about the power structure of processors, see the "Clock and Power Overview" chapter of the i.MX 95 Reference Manual (IMX95RM).

Table 22. Operating ranges

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_SOC	Power supply for SoC logic [1]	0.85	0.90	0.955	V	Power supply for SoC, overdrive mode	—
VDD_SOC	Power supply for SoC logic [1]	0.80	0.85	0.905	V	Power supply for SoC, nominal mode	—
VDD_SOC	Power supply for SoC logic [1]	0.76	0.80	0.85	V	Power supply for SoC, low drive mode	—
VDD_SOC	Power supply for SoC logic [1]	0.61	0.65	0.7	V	Power supply for SoC, suspend mode	—
VDD_ARM	Power supply for Cortex-A55 core [1]	0.85	0.90	0.955	V	Power supply for Cortex-A55, overdrive mode	—
VDD_ARM	Power supply for Cortex-A55 core [1]	0.80	0.85	0.905	V	Power supply for Cortex-A55, nominal mode	—
VDD_ARM	Power supply for Cortex-A55 core [1]	0.76	0.80	0.85	V	Power supply for Cortex-A55, low drive mode	—
VDD_ARM	Power supply for Cortex-A55 core [1][2]	0	0	0	V	Power supply for Cortex-A55, suspend mode	—
NVCC_BBSM_1P8	IO supply for GPIO in BBSM bank	1.65	1.8	1.95	V	—	—

Table continues on the next page...

Table 22. Operating ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_DDR_0P8	DDR supply for DDR PHY	0.795	0.8375	0.88	V	—	—
VDD_ETH_0P8	Digital supply for Ethernet PHY	0.795	0.8375	0.88	V	—	—
VDD_ETH_1P8	I/O voltage supply and analog high voltage power supply	1.71	1.8	1.89	V	—	—
VDD_ANA_0P8	Digital supply for PLLs, temperature sensor, and LVCMOS I/O	0.795	0.8375	0.88	V	—	—
VDD_ANA_1P8/ VDD_ANAVDET_ 1P8	1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, ADC, 24 MHz XTAL, and supply voltage for voltage detect	1.71	1.8	1.89	V	—	—
VDD_MIPI_0P8	Digital supply for MIPI PHY	0.795	0.8375	0.88	V	—	—
VDD_USB_0P8	Digital supply for USB PHYs	0.795	0.8375	0.88	V	—	—
VDD_USB_1P8	1.8 V supply for USB PHYs	1.71	1.8	1.89	V	—	—
VDD_USB_3P3	3.3 V supply for USB PHY (Vmax consistent with Vmax supported by NVCC GPIO supplies)	3.069	3.3	3.45	V	—	—
VDD_PCI_0P8	Digital supply for PCIe PHY	0.795	0.8375	0.88	V	—	—
VDD_PCI_1P8	1.8 V supply for PCIe PHY	1.71	1.8	1.89	V	—	—
VDD_LVDS_1P8	1.8 V supply for LVDS	1.71	1.8	1.89	V	—	—
VDD_MIPI_1P8	1.8 V supply for MIPI PHYs	1.71	1.8	1.89	V	—	—
VDD_AUD_1P8	1.8 V supply for audio transceiver	1.71	1.8	1.89	V	—	—

Table continues on the next page...

Table 22. Operating ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X PHY, LPDDR5 mode	1.01	1.05	1.12	V	—	—
VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X I/O, LPDDR4X mode	1.06	1.1	1.17	V	—	—
VDDQ_DDR	Voltage supply for LPDDR5/4X I/O, LPDDR5 Mode, ODT enabled or disabled	0.47	0.5	0.57	V	—	—
VDDQ_DDR	Voltage supply for LPDDR5/4X I/O, LPDDR4X Mode	0.57	0.6	0.65	V	—	—
NVCC_AON, NVCC_SD2, NVCC_GPIO, NVCC_GPIO_LD, NVCC_WAKEUP, NVCC_CCM_DAP, NVCC_ENET	Power supply for GPIO when it is in 1.8 V mode	1.65	1.8	1.95	V	—	—
NVCC_AON, NVCC_SD2, NVCC_GPIO, NVCC_GPIO_LD, NVCC_WAKEUP, NVCC_CCM_DAP, NVCC_ENET	Power supply for GPIO when it is in 3.3 V mode	3	3.3	3.45	V	—	—

[1] Voltages > Vtyp x 1.05 but < Vmax are only supported if using a PMIC supporting Automatic Voltage Positioning (AVP).
[2] When SoC in a low power state, it can save more power when configuring PMIC to turn VDD_ARM off vs having the PMIC continue to supply VDD_ARM and rely on the on-die powergating around the CORTEXAMIX components.

4.1.7 Temperature ranges specifications

Table 23. Temperature ranges specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tj	Junction temperature—Industrial [1][2][3]	-40	—	105	°C	—	—
Ta	Ambient temperature—Industrial [2]	-40	—	—	°C	—	—

[1] Tj minimum temperature supported at startup where Tj = Ta.
[2] See the application note, i.MX 95 Product Lifetime Usage Estimates for information on product lifetime (power-on hours) for this processor.
[3] Voltages > Vtyp x 1.05 but < Vmax are only supported if using a PMIC supporting Automatic Voltage Positioning (AVP).

4.1.8 Temperature Sensor

Table 24. Temperature Sensor

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tacc_V_25C	Temperature accuracy	-4	—	4	C	T from -40°C to 125°C, voltage trim at room temperature (25°C)	—

4.1.9 Maximum frequency of modules

The following table provides the maximum frequency of modules in the i.MX 95 family of processors.

Table 25. Maximum frequency of modules

Symbol	Low Drive mode	Nominal Drive mode	Overdrive mode	Unit
Cortex-A55 cores	900	1404	1800	MHz
DynamIQ Shared Unit (DSU)	750	1170	1500	MHz
Cortex-M33 core	166.67	250	333.33	MHz
Cortex-M7 core	400	667	800	MHz
EdgeLock® Secure Enclave	133.33	200	250	MHz
NPU	500	800	1000	MHz
DRAM (LPDDR5) 19 x 19 mm package	3200	4800	6400	MT/s
DRAM (LPDDR4X) 19 x 19 mm package	1866	2880	4266	MT/s
DRAM (LPDDR5) 15 x 15 mm package	1866	3200	4266	MT/s
DRAM (LPDDR4X) 15 x 15 mm package	1866	2800	4000	MT/s
ISP	333	500	667	MHz
ISI	333	500	667	MHz
3D GPU	500	800	1000	MHz
Display controller	400	667	800	MHz
VPU	333.33	500	666.67	MHz
JPEG	250	400	500	MHz

4.1.10 Clock source

This section introduces on-chip oscillator and external clock sources.

4.1.10.1 External input clock sources

The i.MX 95 processor is designed to function with quartz crystals to generate the frequencies necessary for operation. 24 MHz for the main clock source and 32.768 kHz for the real time clock. External clock can be injected into RTC_XTALI if the frequency precision and jitter precision are sufficient.

The XTAL input is used to synthesize all of the clocks in the system with the RTC_XTAL input contributing to time keeping and low frequency operations.

Table 26. External input clock sources

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fckil	RTC_XTALI Oscillator [1]	—	32.768	—	kHz	—	—

[1] External clock source or a crystal with the integrated oscillator amplifier. Recommended nominal frequency is 32.768 kHz.

4.1.10.1.1 Audio external clock frequency

Table 27 shows the maximum frequency of external clock.

Table 27. Audio external clock frequency

Symbol	Description	Frequency (Low drive mode)	Frequency (Nominal mode)	Frequency (Overdrive mode)	Unit
fext_clk	EXT_CLK maximum frequency[1]	133	200	200	MHz

[1] Audio EXT_CLK signal muxed on either pin SD2_VSELECT or PDM_BIT_STREAM1.

4.1.10.2 RTC_OSC

The following table shows the external input clock case for the RTC_XTAL oscillator.

Table 28. RTC_OSC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
f	Frequency	—	32.768	—	kHz	—	—
VIH	RTC_XTALI	0.9 x NVCC_BBSM_1P8	—	NVCC_BBSM_1P8	V	—	—
VIL	RTC_XTALI	0	—	0.1 x NVCC_BBSM_1P8	V	—	—
—	Duty cycle	45	—	55	%	—	—

For the case where an external clock is desired to be the source of the 32.768 kHz clock, the RTC_XTALI pin may be driven with the RTC_XTALO pin disconnected.

4.1.10.3 24 MHz quartz specification

Table 29. 24 MHz quartz specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fXTAL	Frequency	—	24	—	MHz	—	—
CLOAD	Cload	—	12	—	pF	—	—
DL	Drive level [1]	—	—	100	µW	—	—
ESR	ESR	—	—	120	Ω	—	—

[1] The drive level value specifies the oscillator drive capability. The selected crystal must be rated for an allowable drive level of at least 100 µW to ensure stable operation and long-term reliability.

4.1.10.4 32.768 kHz quartz specification

Table 30. 32.768 kHz quartz specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fXTAL	Frequency (crystal mode)	—	32.768	—	kHz	—	—
CLOAD	Cload	—	12.5	—	pF	—	—
ESR	ESR	—	—	90	KΩ	—	—
DL	Drive level (crystal mode) [1]	—	—	0.5	µW	—	—

[1] Actual working drive level depends on real design. Please contact crystal vendor for selecting drive level of crystal.

4.1.10.5 Free-running oscillator (FRO) specifications

The FRO is a trimmable 200 to 400 MHz low power, high accuracy internal oscillator, that can be used as a clock source for some i.MX 95 modules.

Table 31. Free-running oscillator (FRO) specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FCLK	Clock Frequency	200	—	400	MHz	Depending upon trim / VDDCORE > 0.7 V	—
FACC	Frequency Accuracy [1]	—	± 2.0	± 4.0	%	VDDCORE > 0.7 V / FCLK = 400 MHz / Open Loop	—
TSU	Startup Time	—	50	—	µs	Fast startup disabled	—

[1] Accuracy over temperature at lower frequencies may be worse.

4.1.11 Maximum supply currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.

To help illustrate the effect of the application on power consumption, data was collected while running consumer standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Table 32. Maximum supply currents

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_ARM	Power supply for Cortex-A55 core	—	—	5000	mA	—	—
VDD_SOC	Power supply for SoC logic	—	—	4400	mA	—	—
VDD_ANA_1P8	1.8 V supply for PLLs, temperature sensor, LVCMOS voltage detect reference, ADC, 24 MHz XTAL, LVDS, MIPI, and USB PHYS [1]	—	—	225	mA	—	—
VDD_*_PLL_0P8	Digital supply for Arm PLL and DRAM PLL	—	—	50	mA	—	—
VDD_*_PLL_1P8	1.8 V supply for Arm PLL and DRAM PLL	—	—	50	mA	—	—
NVCC_BBSM_1P8	I/O supply for GPIO in BBSM bank	—	—	2	mA	—	—
NVCC_<XXX>	Power supply for GPIO [1]	—	—	145	mA	—	—
VDDQ_DDR	Voltage supply for LPDDR5/ LPDDR4X [1]	—	—	Imax = N x C x V x (0.5 x F)	mA	—	—
VDD2H_DDR	Voltage supply for LPDDR5/LPDDR4X PHY, LPDDR5 mode	—	—	22	mA	6400 Mbps 32-bit PHY, 1 rank	—
VDD_DDR_0P8	DDR I/O supply voltage	—	—	800	mA	—	—
NVCC_CCM_DAP	CCM supply voltage	—	—	27.59	mA	—	—
VDD_ETH_0P8	Digital supply for Ethernet PHY	—	—	58.99	mA	—	—
VDD_ETH_1P8	I/O voltage supply and analog high voltage power supply	—	—	40	mA	—	—
VDD_ANAVDET_ 1P8	Supply voltage for voltage detect	—	—	9	mA	—	—

Table continues on the next page...

Table 32. Maximum supply currents*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_MIPI_1P8	1.8 V supply for MIPI PHYs	—	—	170	mA	For MIPI CSI 2-lane Rx PHY	—
VDD_MIPI_1P8	1.8 V supply for MIPI PHYs	—	—	5.0	mA	For MIPI DSI 4-lane Tx PHY	—
VDD_MIPI_0P8	Digital supply for MIPI PHYs	—	—	35.4	mA	For MIPI CSI 2-lane Rx PHY	—
VDD_MIPI_0P8	Digital supply for MIPI PHYs	—	—	42.2	mA	For MIPI DSI 4-lane Tx PHY	—
VDD_PCI_0P8	Digital supply for PCI	—	—	71	mA	PCIe Gen2	—
VDD_PCI_0P8	Digital supply for PCI	—	—	71	mA	PCIe Gen3	—
VDD_PCI_1P8	1.8 V supply for PCI	—	—	43	mA	PCIe Gen3	—
VDD_PCI_1P8	1.8 V supply for PCI	—	—	43	mA	PCIe Gen2	—
VDD_USB_0P8	0.8 V supply for USB PHY	—	—	17.99	mA	Per USB 2.0 PHY used	—
VDD_USB_1P8	1.8 V supply for USB PHY	—	—	13.7	mA	Per USB 2.0 PHY used	—
VDD_USB_3P3	3.3 V supply for USB PHY (Vmax consistent with Vmax supported by NVCC GPIO supplies)	—	—	7.25	mA	Per USB 2.0 PHY used	—
VDD_LVDS_1P8	1.8 V supply for LVDS interface [2]	—	—	9.49	mA	Total current of VDD_ LVDS_* supplies per each 4-lane LVDS interface	—
VDD_AUD_1P8	1.8 V supply for audio transceiver	—	—	0.1	mA	—	—
VDD_ANAx_0P8	Digital supply for PLLs, temperature sensor, LVCMOS I/O, MIPI, PCIe and USB PHYS	—	—	300	mA	—	—

[1] Where, N—Number of I/O pins supplied by the power line, C—Equivalent external capacitive load, V—I/O voltage, (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.
[2] Maximum dynamic current

4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting

- Irreversible damage to the processor (worst-case scenario)

Figure 5 and Figure 6 illustrates the power-up and power-down sequence of i.MX 95 processors.

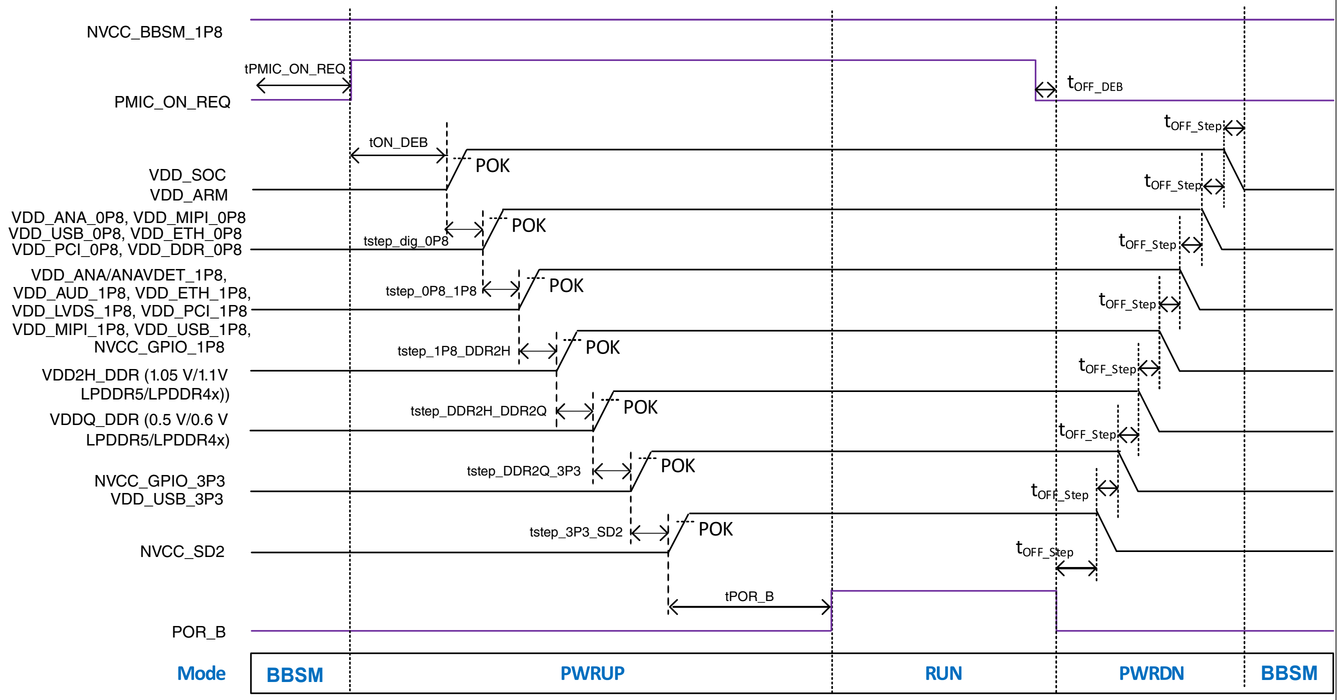
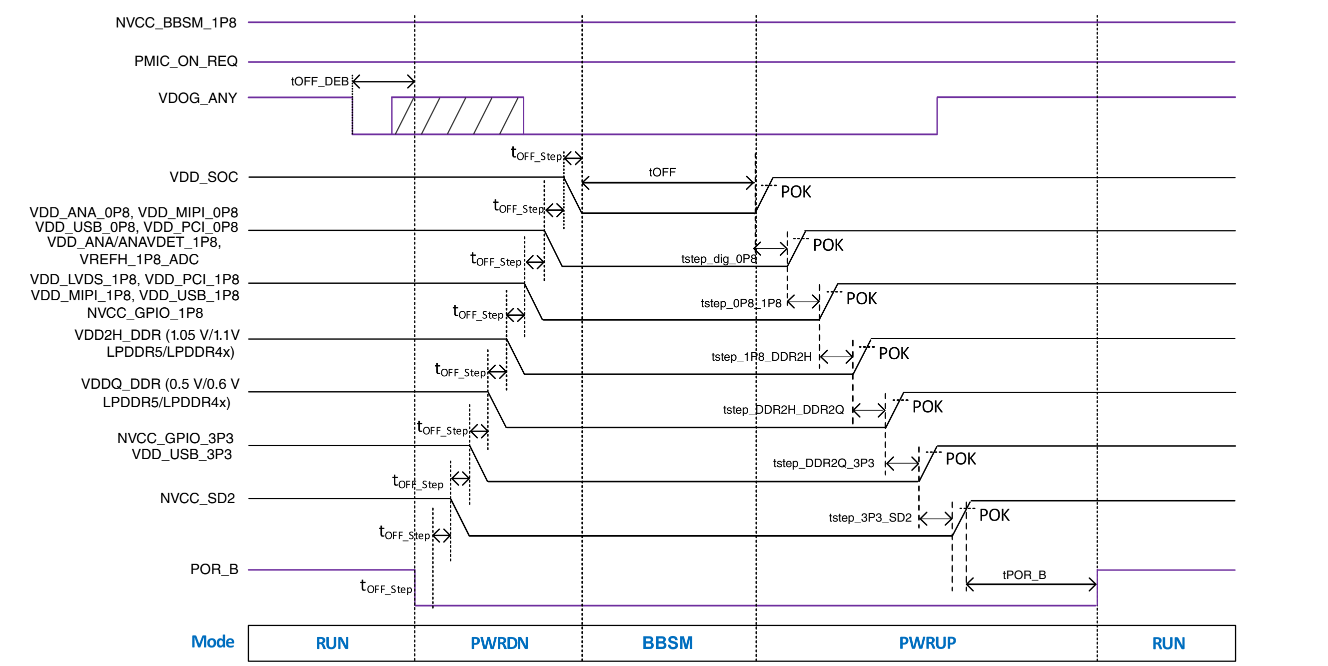


Figure 5. The power sequence of i.MX 95 processors



WDOG_ANY signal is routed to the PMIC and can be configured to initiate a cold reset (i.e., a repower cycle). The signal polarity and active level are programmable, depending on the specific PMIC implementation.

TOFF represents the power-down delay required for all power rails to fully discharge to 0 V.
The minimum TOFF duration depends on system loading conditions, the total on-board capacitance, and the PMIC's discharge capability.
This parameter is typically programmable and may vary based on the specific PMIC implementation.

Figure 6. The power sequence of i.MX95 processor after cold reset (WDOG_ANY event)

Note: *POR_B must be asserted whenever VDD_SOC is powered down, but NVCC_BBSM_1P8 is powered up (when the processor is in BBSM mode).*
Note: *PMIC has a provision to recycle BBSM supply in case of abrupt supply drop beyond the operating range causing WDOG events.*
Note: *All non-NXP PMICs must have functional safety feature that ensures cycling of all supply rails when SoC does not respond or is in indeterminant state.*

Power sequencing

1. Turn on NVCC_BBSM_1P8
2. [The SoC asserts PMIC_ON_REQ at this point in time.]
3. Turn on VDD_SOC digital voltage supplies.
4. Turn on VDD_ARM, either together with VDD_SOC or after VDD_SOC is stable.
   Note: *There is no sequence requirement between VDD_ARM and VDD_SOC.*
5. Turn on all VDD_*_0P8 analog, DDR, PHY, and PLL supplies.
   Note: *This step may be simultaneous with etither of the VDD_SOC and/or VDD_ARM supplies if desired.*
6. Turn on all remaining 1.8 V supplies. This includes VDD_*_1P8 analog, PHY and PLL supplies, and any NVCC_XXX I/O supplies that are being operated at 1.8 V.
7. Turn on DDR VDD2H supply.
8. Turn on DDR VDDQ supply.
   Note: *The i.MX SoC has no VDD2H vs VDDQ sequencing requirements, but generally VDDQ must come up after VDD2H to meet DRAM memory component specification.*
9. Turn on any 3.3 V supplies. This includes NVCC_XX I/O supplies that being operated at 3.3 V and VDD_USB_3P3.
   Note: *This 3.3 V supply step may be simultaneous with the DDR VDD2H or DDR VDDQ supplies if desired.*
10. Turn on NVCC_SD2, if NVCC_SD2 is being used for a dynamically switchable 1.8/3.3 V SD card voltage (booting initially at 3.3 V).
    Note: *If NVCC_SD2 is operating at a fixed 1.8 V-only or 3.3 V-only voltlage in a give system, then it may power up at the same time as other supplies of the same voltage.*
11. POR_B release (it should be asserted during the entire power-up sequence).

4.2.1 Power-up sequence

The power-up sequence is defined as follows:

Note: The power up sequence when exiting suspend mode follows the same steps, except that only the switchable supplies that were turned off during suspend mode are brought back up. Throughout this process, the POR_B input remains asserted high.

Table 33. Power-up sequence

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tPMIC_ON_Req	The time from when NVCC_BBSM_1P8 reaches its minimum operating range to when the SoC begins to assert PMIC_ON_REQ.	0	2	—	ms	—	—
tON_DEB	The time from when PMIC_ON_REQ	0	1	—	ms	—	—

Table continues on the next page...

Table 33. Power-up sequence*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	reaches its high-level output voltage (VOH) to when VDD_SOC begins to power-up.						
tOFF_DEB	The time from PMIC_ON_REQ reaches its low-level output voltage (VOL) to when VDD_SOC begins to power-down.	—	1.6	—	ms	—	—
(not shown in timing diagram)	The time from when VDD_SOC begins to power-up to when VDD_ARM begins to power-up.	0	0.5	—	ms	—	—
tstep_dig_0p8	The time from when the latter of VDD_SOC or VDD_ARM begins to power-up to when all VDD_*_0P8 analog, PHY and PLL supplies begin to power-up.	0	0.5	—	ms	—	—
tstep_0p8_1p8	The time from when the final VDD_*_0P8 analog, PHY and PLL supply begins to power-up to when 1.8 V supplies begin to power-up.	0.2	0.25	—	ms	—	—
tstep_1p8_ddr2h	The time from when the final 1.8V supply begins to power-up to when the DDR VDD2H supply begins to power-up.	0.4	0.5	—	ms	—	—
tstep_ddr2h_ddrq	The time from when the DDR VDD2H supply begins to power-up to when the DDR VDDQ	0	0.3	—	ms	—	—

Table continues on the next page...

Table 33. Power-up sequence...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	supply begins to power-up.						
tstep_ddrq_3p3	The time from when the DDR VDDQ supply begins to power-up to when any 3.3 V supply begins to power-up.	0	0.1	—	ms	—	—
tstep_3p3_sd2	If NVCC_SD2 is being used for a dynamically switchable 1.8/3.3V SD card voltage (booting initially at 3.3 V), then this represents the time from when the final 3.3 V supply begins to power-up to when NVCC_SD2 begins to power-up.	0	1	—	ms	—	—
tPOR_B	The time from when all supplies reach their minimum operating range to when POR_B may be released.	0	—	—	ms	—	—
tOFF_Step	The time between voltage rails powering down.	0	—	—	ms	—	—
tOFF	tOFF represents the power-down delay requirement for all power rails to fully discharge to 0V. [1][2]	500	—	—	ms	—	—

[1] The minimum tOFF duration depends on system loading conditions, the total on-board capacitance, and the PMIC's discharge capability
[2] This parameter is typically programmable and may vary based on the specific PMIC implementation

4.2.2 Power-down sequence

The power-down sequence is defined as follows:

- Turn off NVCC_BBSM_1P8 last
- Turn off VDD_SOC after the other (non-BBSM) power rails or at the same time as other (non-BBSM) rails
- No sequence for other power rails during power-down

Note : When switching off supply group 0 (NVCC_BBSM_1P8), VDD_BBSM_0P8_CAP must be fully discharged to 0 V before starting the next power-up sequence to ensure correct operation.

4.3 PLL electrical characteristics

Following sections introduce the Fractional-N (FracN) Phase-Locked Loops (PLL) and Low Noise PLL electrical characteristics.

4.3.1 Fracn PLL

Table 34. Fracn PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TLock	PLL lock time	-	-	100	µS	—	—
Fout	Output Clock Frequency [1]	9.8M	—	2.5G	Hz	—	—
FPLL_MOD	SSCG modulation frequency	30	-	64	kHz	@40MHz and 50MHz ref clk	—
ΔFPLL_MOD	SSCG modulation depth	-4*Fref*pfd	—	—	Hz	Down Spread	—

[1] This specification is PLL input reference clock frequency after pre-divider.

4.3.2 Low Noise PLL

Table 35. Low Noise PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TLock	PLL lock time	—	—	100	µs	—	—
FPLL_MOD	SSCG modulation frequency	30	—	64	KHz	at Fref_pfd < 40 MHz	—
ΔFPLL_MOD	SSCG modulation depth	-4*Fref*pfd	—	—	Hz	Down Spread	—

4.4 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR5 and LPDDR4X modes
- LVDS I/O

4.4.1 General purpose I/O (GPIO) DC parameters

The following tables show the DC parameters for GPIO pads. The parameters are guaranteed per the operating ranges table, unless otherwise noted.

Table 36. General purpose I/O (GPIO) DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH (1.8V)	High-level output voltage	0.8 x NVCC_xxx	—	NVCC_xxx	V	DSE = X1, IOH = 1.1mA DSE = X6, IOH = 6.6mA	—
VOL (1.8 V)	Low-level output voltage	0	—	0.2 x NVCC_xxx	V	DSE = X1, IOH = 1.1mA DSE = X6, IOH = 6.6mA	—
VOH (3.3 V)	High-level output voltage	0.8 x NVCC_xxx	—	NVCC_xxx	V	DSE = X1, IOH = 2mA DSE = X4, IOH = 8mA	—
VOL (3.3 V)	Low-level output voltage	0	—	0.2 x NVCC_xxx	V	DSE = X1, IOH = 2mA DSE = X4, IOH = 8mA	—
VIL	Low-level input voltage	0	—	0.3 x NVCC_xxx	V	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125°C	—
VIH	High-level input voltage	0.7 x NVCC_xxx	—	NVCC_xxx	V	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125°C	—
Rpd3.3v	Pull-down resistor	24	43	87	KΩ	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125°C	—
Rpu3.3v	Pull-up resistor	18	37	72	KΩ	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125°C	—
Rpd1.8v	Pull-down resistor	13	23	48	KΩ	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125°C	—
Rpu1.8v	Pull-up resistor	12	22	49	KΩ	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125°C	—

Note: For GPIO pads, when the supplies are ramp-up or/and below operating level, the pad state values are undefined.

Note: For PHY pads, the PAD state values are undefined before POR_B is asserted.

4.4.1.1 Additional leakage parameters

Table 37. Additional leakage parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIH	Leakage high	-5	—	5	μA	Non-PHY IO, 1.65 V -3.465 V, Temp = -40°C to 125°C | pad = VDDIO	—

Table continues on the next page...

Table 37. Additional leakage parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIL	Leakage low	-5	—	5	µA	Non-PHY IO, 1.65 V to 3.465 V, Temp = -40°C to 125°C | pad = VDDIO	—

4.4.2 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR4X/LPDDR5 operational modes. The DDR Memory Controller (DDRMC) is compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board’s DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX95 application processors.

4.4.3 DDR I/O output buffer impedance

The DDR output driver and ODT impedances are controlled across PVT using ZQ calibration procedure with a 120 Ω ±1% resistor connected to ground. Programmable drive strength and ODT impedance targets available in the NXP DDR tool are detailed in the device's IBIS model. Impedance deviation (calibration accuracy) is about approximately ±10% (maximum/minimum impedance) across PVT.

4.4.4 DDR pin I/O leakage DC parameters

Table 38. DDR pin I/O leakage DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOz	I/O leakage current [1][2]	—	—	±180	µA	—	—

[1] Refer to IBIS model for complete IV curve characteristics
[2] Output leakage is measured with all outputs disabled, 0 V ≤ Vout ≤ VddQ

4.4.5 LVDS DC electrical characteristics

Table 39. LVDS DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vod	Differential Voltage Output Voltage	0.25	—	0.45	V	Rload = 100 Ω	—
Voh	Output Voltage High	1.25	—	1.6	V	Rload = 100 Ω	—
Vol	Output Voltage Low	0.9	—	1.25	V	Rload = 100 Ω	—
Vos	Offset Static Voltage (i.e. Common mode voltage)	1.125	—	1.375	V	Rload = 100 Ω	—
Vosdiff	VOS (Ripple peak to peak)	—	—	25	mV	Rload = 100 Ω	—

Table continues on the next page...

Table 39. LVDS DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ISA ISB	Output short-circuited to GND [1]	—	—	4.2	mA	—	—
ISAB	Output short current [1]	—	—	4.2	mA	—	—

[1] This value is base on test.

4.5 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR5 and LPDDR4X modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 7 and Figure 8.

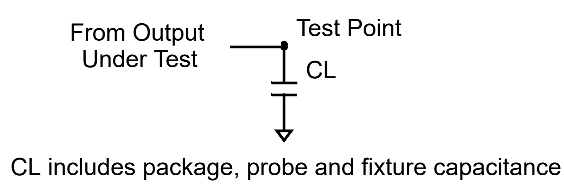


Figure 7. Load circuit for output

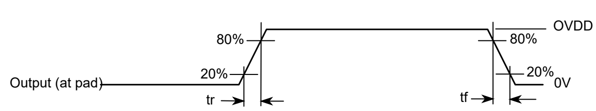


Figure 8. Output transition time waveform

4.5.1 General purpose I/O (GPIO) AC parameters

Table 40. General purpose I/O (GPIO) AC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tR	TX rise time	3950	—	5950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X1	—

Table continues on the next page...

Table 40. General purpose I/O (GPIO) AC parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tF	TX fall time	4140	—	5600	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X1	—
tR	TX rise time	1890	—	2820	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X2	—
tF	TX fall time	1790	—	2560	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X2	—
tR	TX rise time	675	—	1950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X3	—
tF	TX fall time	584	—	1730	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X3	—
tR	TX rise time	521	—	1320	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X4	—
tF	TX fall time	442	—	748	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X4	—
tR	TX rise time	454	—	742	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X5	—
tF	TX fall time	380	—	554	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X5	—
tR	TX rise time	419	—	639	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X6	—
tF	TX fall time	349	—	506	ps	Slew rate FSEL1 = 11b, Fast Slew Rate	—

Table continues on the next page...

Table 40. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						(1.62 V, 1.8 V, 1.98 V), Drive strength X6	
tR	TX rise time	4030	—	5790	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X1	—
tF	TX fall time	4410	—	6290	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X1	—
tR	TX rise time	1870	—	2950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength X2	—
tF	TX fall time	1900	—	3310	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X2	—
tR	TX rise time	774	—	1930	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X3	—
tF	TX fall time	719	—	2070	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X3	—
tR	TX rise time	598	—	1360	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X4	—
tF	TX fall time	490	—	1590	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength X4	—

4.5.2 DDR I/O AC electrical characteristics

The DDR I/O pads support LPDDR4X/LPDDR5 operational modes. The DDR Memory Controller (DDRMC) is compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX95 application processors.

4.5.3 LVDS AC timing specifications

Table 41. LVDS AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
f	Operating data rate	—	—	1155	Mbps	Rload = 100 Ω Vload = 2 pF Note: This is the maximum work condition of operating data rate.	—
Tfall	Vod fall time, 20 - 80%	—	—	0.3	UI (Unit Interval)	Rload = 100 Ω Vload = 2 pF Note: Measurement levels are 20% - 80% from output voltage.	—
Trise	Vod rise time, 20 - 80%	—	—	0.3	UI (Unit Interval)	Rload = 100 Ω Vload = 2 pF Note: Measurement levels are 20% - 80% from output voltage.	—
Tskew	Lane skew [1][2]	—	250	—	ps	Rload = 100 Ω, Cload = 2 pF	—

[1] Tskew is the differential time at Vod = 0 voltage between different channel.
[2] This value is absolute value and base on test.

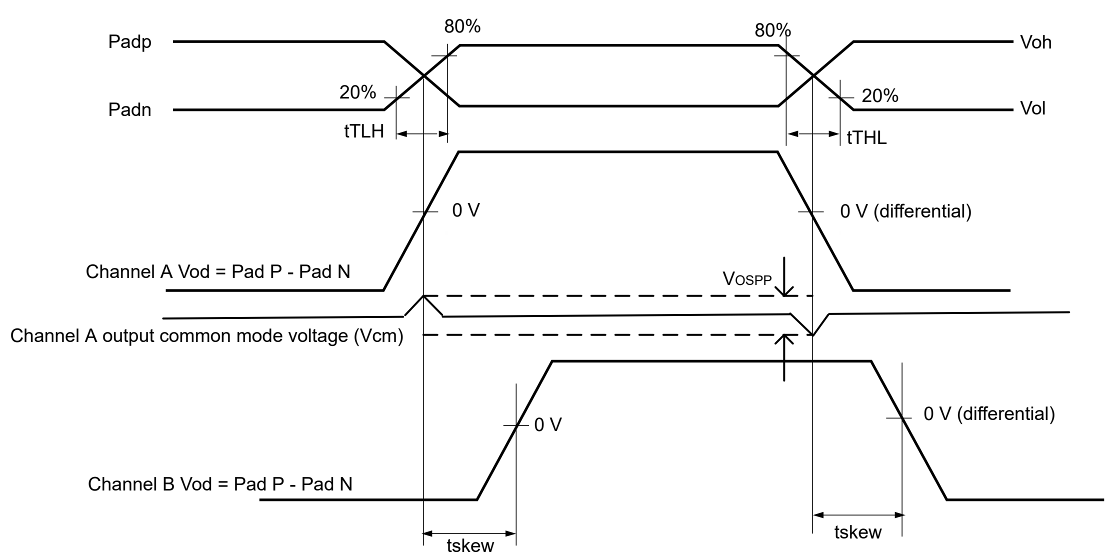


Figure 9. Output transition time waveform

4.6 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See *TIA/EIA STANDARD 644-A, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (2001)* for details.

4.7 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 95 processor.

4.7.1 Reset timings parameters

The following figure shows the reset timing and table lists the timing parameters.

Table 42. Reset timings parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CC1	Duration of POR_B to be qualified as valid. Note: POR_B rise/fall times must be 400 uS or less.	1	—	—	RTC_XTALI cycle	—	—

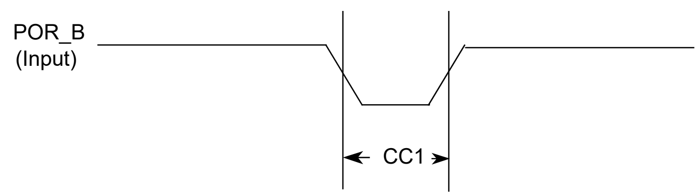


Figure 10. Reset timing diagram

4.7.2 JTAG timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Following table lists signal parameters.

Table 43. JTAG timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SJ0	JTAG_TCK frequency of operation [1][2][3][4]	—	—	50	MHz	—	—
SJ1	JTAG_TCK cycle time in crystal mode [1][2]	20	—	—	ns	—	—
SJ2	JTAG_TCK clock pulse width	10	—	—	ns	—	—

Table continues on the next page...

Table 43. JTAG timing parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	measured at VM [1][2][5]						
SJ3	JTAG_TCK rise and fall times [1][2]	—	—	3	ns	—	—
SJ4	Boundary scan input data set-up time [1][2]	15	—	—	ns	—	—
SJ5	Boundary scan input data hold time [1][2]	15	—	—	ns	—	—
SJ6	JTAG_TCK low to output data valid [1][2]	—	—	600	ns	—	—
SJ7	JTAG_TCK low to output high impedance [1][2]	—	—	600	ns	—	—
SJ8	JTAG_TMS, JTAG_TDI data set-up time [1][2]	5	—	—	ns	—	—
SJ9	JTAG_TMS, JTAG_TDI data hold time [1][2]	5	—	—	ns	—	—
SJ10	JTAG_TCK low to JTAG_TDO data valid [1][2]	—	—	14	ns	—	—
SJ11	JTAG_TCK low to JTAG_TDO high impedance [1][2]	—	—	14	ns	—	—
SJ14	JTAG_TCK low to JTAG_TDO data invalid [1][2]	1	—	—	ns	—	—

[1] Input timing assumes an input signal slew rate of 3 ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 Ω , unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance of the transmission line can be equal to the selected RDSON of the I/O pad output driver.
[3] TDC = target frequency of JTAG
[4] 50 MHz frequency is for the JTAG debug interface. For boundary scan, the maximum TCK frequency is 10 MHz.
[5] VM = mid-point voltage

Following figure depicts the JTAG test clock input timing.

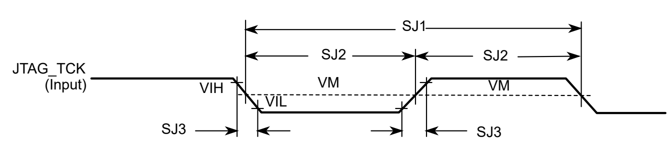


Figure 11. Test Clock Input Timing Diagram

Following figure depicts the JTAG boundary scan timing.

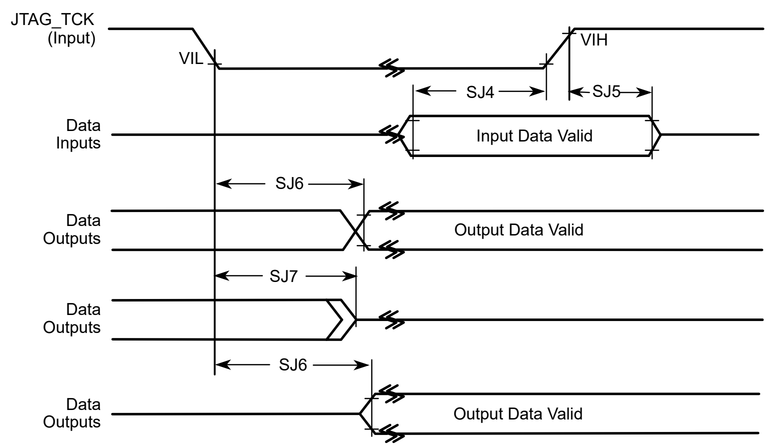


Figure 12. Boundary system (JTAG) timing diagram

Following figure depicts the JTAG test access port.

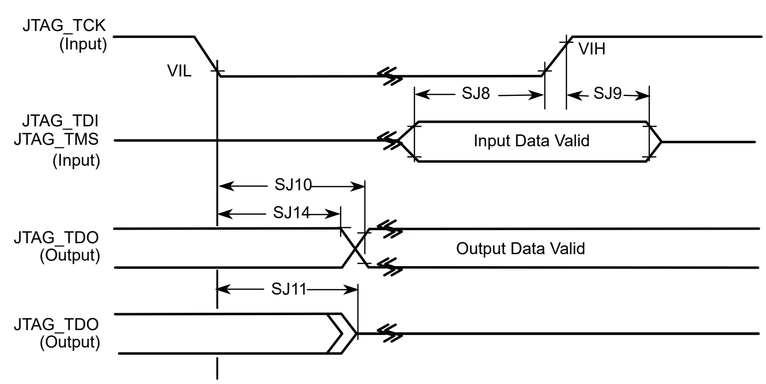


Figure 13. Test Access Port Timing Diagram

4.7.3 SWD timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Following table shows SWD timing.

Table 44. SWD timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S0	SWD_CLK frequency	—	—	50	MHz	—	—
S1	SWD_CLK cycle time	20	—	—	ns	—	—
S2	SWD_CLK pulse width	10	—	—	ns	—	—

Table continues on the next page...

Table 44. SWD timing parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S3	Input data setup time	5	—	—	ns	—	—
S4	Input data hold time	5	—	—	ns	—	—
S5	Output data valid time	—	—	14	ns	—	—
S6	Output high impedance time	—	—	14	ns	—	—
S7	Output data invalid time	0	—	—	ns	—	—

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ω , unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line can be equal to the selected RDSON of the I/O pad output.

Following figure depicts the SWD timing.

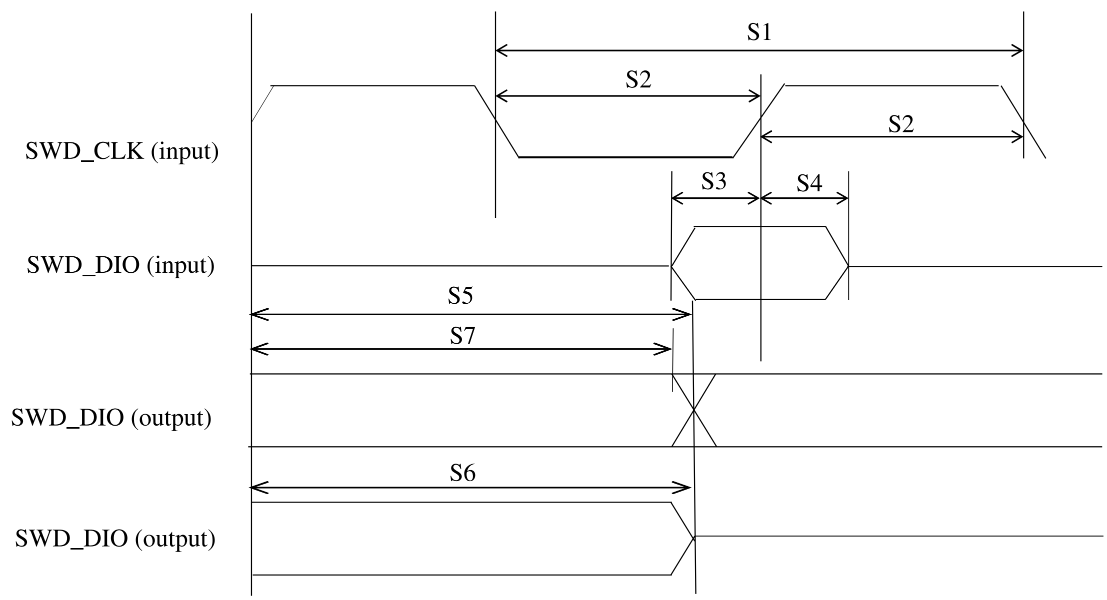


Figure 14. SWD timing

4.7.4 DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)

The i.MX95 Family of processors have been designed and tested to work with JEDEC JESD209—compliant LPDDR5/ LPDDR4X memory.

- JEDEC LPDDR4X Specification JESD209-4C, November 2019
- JEDEC LPDDR5 Specification JESD209-5A, January 2020

Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND, and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors:IMX9-PROCESSORS .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 45. DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Number of controllers (LPDDR4X)	—	—	1	—	—
—	Number of controllers (LPDDR5)	—	—	1	—	—
—	Number of channels (LPDDR4X)	—	—	2	—	—
—	Number of Chip Selects (LPDDR4X)	—	—	2	—	—
—	Bus Width	—	—	32	bit	—
—	Maximum Clock Frequency (LPDDR4X) [1]	—	—	4266	MT/s	—
—	Maximum Clock Frequency (LPDDR5) [2]	—	—	6400	MT/s	—

[1] Operating at up to 4000 MT/s for 15 x 15 mm package
[2] Operating at up to 4200 MT/s for 15 x 15 mm package

4.7.4.1 Clock/data/command/address pin allocations

These processors use generic names for clock, data, and command address bus.

4.8 Analog interfaces

This section introduces the timing and electrical parameters about analog interfaces of i.MX 95 processors.

4.8.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended resolution specifications.

4.8.1.1 SAR ADC

Table 46. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VADIN	ADC Input Voltage	VGND	—	VDD_ANA_1P8	V	on or off channels	—
fADCK	ADC Conversion Clock Frequency	20	—	80	MHz	—	—
Csample	Sample cycles	5.5	—	—	number of cycles	—	—
Ccompare	Fixed compare cycles	—	58	131.5	number of cycles	—	—
Cconversion	Clock conversion cycles	Cconversion = Csample + Ccompare	Cconversion = Csample + Ccompare	Cconversion = Csample + Ccompare	number of cycles	—	—
CAD_INPUT	ADC Input Capacitance	—	—	7	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Series Resistance	—	—	1.25	kΩ	—	—
DNL	ADC Differential Non-linearity	-1	-	2	LSB	after calibration	—
INL	ADC Integral Non-linearity	-3	-	3	LSB	after calibration	—
ENOB	Effective Number of Bits [1]	—	9	—	bits	input signal frequency = 1KHz	—
RAS	Analog source resistance	—	—	5	KΩ	—	—
Bandgap	Output voltage ready time for bandgap [2] [3]	—	1	—	μs	—	—

[1] The ADC performance for inputs ADC0_CH0 to ADC0_CH3 can be impacted by JTAG operation (pins TDI, TDO, TMS, TCK). Performance specification is not guaranteed for these ADC inputs under this condition.
[2] Output voltage ready time = the ready time is the waiting time after enabling the Vbg output buffer from BBSM before ADC can convert data
[3] Based on simulation test (for the value -1)

4.9 Audio

This section introduces the timing and electrical parameters about audio subsystem of I.MX 95 processor.

4.9.1 SAI switching specifications

This section provides the AC timings for the SAI in Controller (clocks driven) and Target (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR2[BCP] = 0, SAI_RCR2[BCP] = 0) and non inverted frame sync (SAI_TCR4[FSP]

= 0, SAI_RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

The SAI4 pins muxed with ENET2 and the SAI4 pins muxed with XSPI1 are mutually exclusive. It does not support a use case where some SAI4 pins are connected to ENET2 and other SAI4 pins are simultaneously connected to XSPI1.

SAI5 is supported entirely on SD3 or entirely on XSPI1 (but not multiplexed across both XSPI1 and SD3 pins). SAI5 is also supported with some pins on SD3 and others on XSPI1, as long as the non-data signals (SYNCs and/or BCLKs) are on the one interface (SD3 or XSPI1), and all TX_DATA pins are on the one interface (SD3 or XSPI1), and all RX_DATA pins are on the one interface (SD3 or XSPI1).

SAI2 is supported entirely on ENET pins (at up to maximum supported speeds). However, the SAI2 on XSPI1 pins are limited to no more than 25 MHz – the faster 50 MHz Controller Tx and 66.67 MHz Target Rx modes are supported by the SAI2 only on ENET2 pins.

4.9.1.1 SAI/I2S Controller mode timing (50 MHz)

To achieve 50 MHz for BCLK operation, clock must be set in feedback mode and TCR2[BCI] = 1 must be configured to enable it for the transmitter.

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 47. SAI/I2S Controller mode timing (50 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SAI_MCLK cycle time	20	—	—	ns	—	—
S2	SAI_MCLK pulse width high/low	40%	—	60%	MCLK period	—	—
S3	SAI_BCLK cycle time	20	—	—	ns	—	—
S4	SAI_BCLK pulse width high/low	40%	—	60%	BCLK period	—	—
S5	SAI_BCLK to SAI_FS output valid	—	—	3	ns	—	—
S6	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—	—
S7	SAI_BCLK to SAI_TXD valid	—	—	3	ns	—	—
S8	SAI_BCLK to SAI_TXD invalid	-2	—	—	ns	—	—
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	3	—	—	ns	—	—

Table continues on the next page...

Table 47. SAI/I2S Controller mode timing (50 MHz)...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—

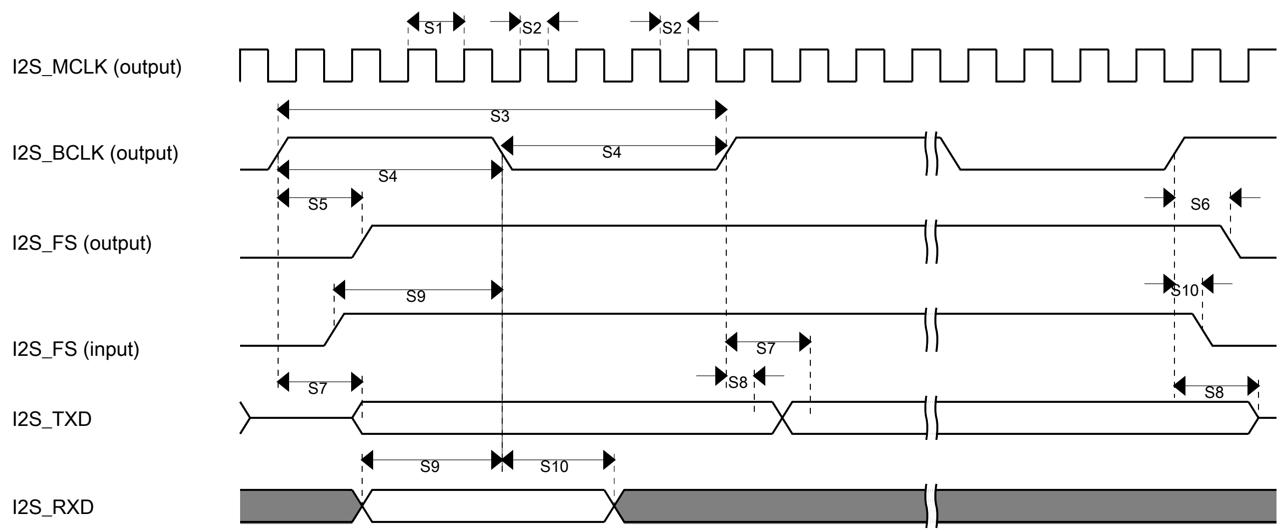


Figure 15. SAI timing-Controller modes

4.9.1.2 SAI/I2S Controller mode timing (25 MHz)

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 48. SAI/I2S Controller mode timing (25 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SAI_MCLK cycle time	40	—	—	ns	—	—
S2	SAI_MCLK pulse width high/low	40%	—	60%	MCLK period	—	—
S3	SAI_BCLK cycle time	40	—	—	ns	—	—
S4	SAI_BCLK pulse width high/low	40%	—	60%	BCLK period	—	—

Table continues on the next page...

Table 48. SAI/I2S Controller mode timing (25 MHz)...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S5	SAI_BCLK to SAI_FS output valid	—	—	3	ns	—	—
S6	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—	—
S7	SAI_BCLK to SAI_TXD valid	—	—	3	ns	—	—
S8	SAI_BCLK to SAI_TXD invalid	-2	—	—	ns	—	—
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK [1]	9.5	—	—	ns	—	—
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	—	ns	—	—

[1] SAI4 pins multiplexed over ENET2 when operating at 3.3 V I/O supply, this parameter value is 9.75 ns.

4.9.1.3 SAI/I2S Target mode timing (66 MHz)

To support 66 MHz for SAI Rx Target mode (input SAI Rx Clk, input SAI Rx Frame Sync, and input SAI Rx Data) for the following pins:

SAI2.RX_* pins multiplexed over ENET2

SAI5.RX_* pins multiplexed over SD3

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Table 49. SAI/I2S Target mode timing (66 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S11	SAI_BCLK cycle time (input)	15	—	—	ns	—	—
S12	SAI_BCLK pulse width high/low (input)	40%	—	60%	BCLK period	—	—
S13	SAI_FS input setup before SAI_BCLK	3	—	—	ns	—	—
S14	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—
S17	SAI_RXD setup before SAI_BCLK	3	—	—	ns	—	—
S18	SAI_RXD hold after SAI_BCLK	2	—	—	ns	—	—

4.9.1.4 SAI/I2S Target mode timing (25 MHz)

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 50. SAI/I2S Target mode timing (25 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S11	SAI_BCLK cycle time (input)	40	—	—	ns	—	—
S12	SAI_BCLK pulse width high/low (input)	40%	—	60%	BCLK period	—	—
S13	SAI_FS input setup before SAI_BCLK	3	—	—	ns	—	—
S14	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid [1]	—	—	9.5	ns	—	—
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	—	ns	—	—
S17	SAI_RXD setup before SAI_BCLK	3	—	—	ns	—	—
S18	SAI_RXD hold after SAI_BCLK	2	—	—	ns	—	—
S19	SAI_FS input assertion to SAI_TXD output valid3 [2]	—	—	15	ns	—	—

[1] SAI4 pins multiplexed over ENET2 when operating at 3.3 V I/O supply, this parameter value is 9.75 ns.
[2] Applies to first bit in each frame and only if the TCR4[FSE] bit is clear.

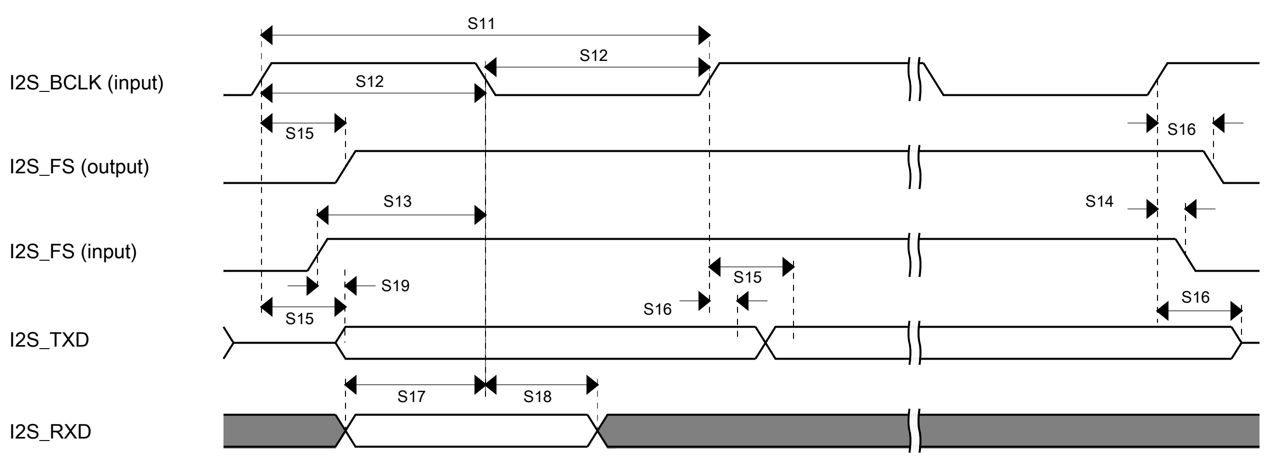


Figure 16. SAI timing-Target mode

4.9.1.5 SAI I/O specifications

Table 51. SAI I/O specifications

Mode	Pins	Clock	Frequency	Output	Input
Controller Tx	Any SAI interface multiplexes over ENET pins for a SAI instance is in NETCMIX. Any SAI interface does not multiplex over ENET pins for a SAI instance is not in NETCMIX.	TXC	50 MHz	TXD	—
		TXC	50 MHz	TXFS	—
	Any SAI interface multiplexes over ENET pins for a SAI instance is not in NETCMIX.	TXC	25 MHz	TXD	—
	Any SAI interface does not multiplex over ENET pins for a SAI instance is in NETCMIX.	TXC	25 MHz	TXFS	—
	Any	TXC	25 MHz	—	TXFS
Controller Rx	Any	RXC	25 MHz	—	RXD
		RXC	25 MHz	—	RXFS
		RXC	25 MHz	RXFS	—
	Any SAI interface multiplexes over ENET pins for a SAI instance is in NETCMIX. Any SAI interface does not multiplex over ENET pins	RXC Loopback Mode	50 MHz	—	RXD

Table continues on the next page...

Table 51. SAI I/O specifications...*continued*

Mode	Pins	Clock	Frequency	Output	Input
	for a SAI instance is not in NETCMIX.	RXC Loopback Mode	50 MHz	—	RXFS
Target Tx	Any	TXC	25 MHz	TXD	—
		TXC	25 MHz	TXFS	—
		TXC	25 MHz	—	TXFS
Target Rx	SAI2 multiplexes over Ethernet pins, or (for SoCs supporting SAI5 and SD3), SAI5 multiplexes over SD3 pins.	RXC	66.7 MHz	—	RXD
		RXC	66.7 MHz	—	RXFS
		RXC	25 MHz	RXFS	—
	Any SAI instance or pinmux location is not mentioned above.	RXC	25 MHz	—	RXD
		RXC	25 MHz	—	RXFS
		RXC	25 MHz	RXFS	—

4.9.2 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

The following table and figures show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Table 52. SPDIF timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns	—	—
—	Skew	—	—	1.5	ns	SPDIF_OUT output (Load = 50 pf)	—
—	Transition rising	—	—	24.2	ns	SPDIF_OUT output (Load = 50 pf)	—
—	Transition falling	—	—	31.3	ns	SPDIF_OUT output (Load = 50 pf)	—
—	Skew	—	—	1.5	ns	SPDIF_OUT output (Load = 30 pf)	—
—	Transition rising	—	—	13.6	ns	SPDIF_OUT output (Load = 30 pf)	—

Table continues on the next page...

Table 52. SPDIF timing parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Transition falling	—	—	18	ns	SPDIF_OUT output (Load = 30 pf)	—
srckp	Modulating Rx clock (SPDIF_SR_CLK) period	40	—	—	ns	—	—
srckph	SPDIF_SR_CLK high period	16	—	—	ns	—	—
srckpl	SPDIF_SR_CLK low period	16	—	—	ns	—	—
stclkp	Modulating Tx clock (SPDIF_ST_CLK) period	40	—	—	ns	—	—
stclkph	SPDIF_ST_CLK high period	16	—	—	ns	—	—
stclkpl	SPDIF_ST_CLK low period	16	—	—	ns	—	—

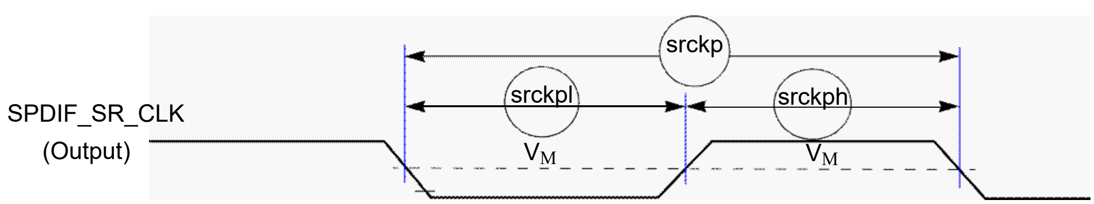


Figure 17. SPDIF_SR_CLK timing diagram

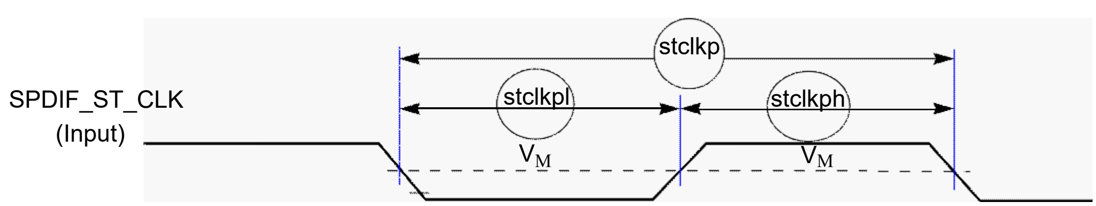


Figure 18. SPDIF_ST_CLK timing diagram

4.9.3 Timer/PDM Microphone interface timing parameters

Note: *These timing requirements apply only if the clock divider is enabled (PDM_CTRL2[CLKDIV] = 0), otherwise there are no special timing requirements.*

The PDM microphones must meet the setup and hold timing requirements shown in the following table. The "k" factor value in Table 53 depends on the selected quality mode as shown in Table 54.

Table 53. PDM timing parameters

Parameter	Value
trs, tfs	≤ floor (k x CLKDIV) -1 / PDM_CLK_ROOT rate [1]
trh, tfh	≥ 0

[1] Depending on K value, user must make sure floor (K x CLKDIV) > 1 to avoid timing problems.

Table 54. K factor value

Quality factor	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

Figure 19 illustrates the timing requirements for the PDM.

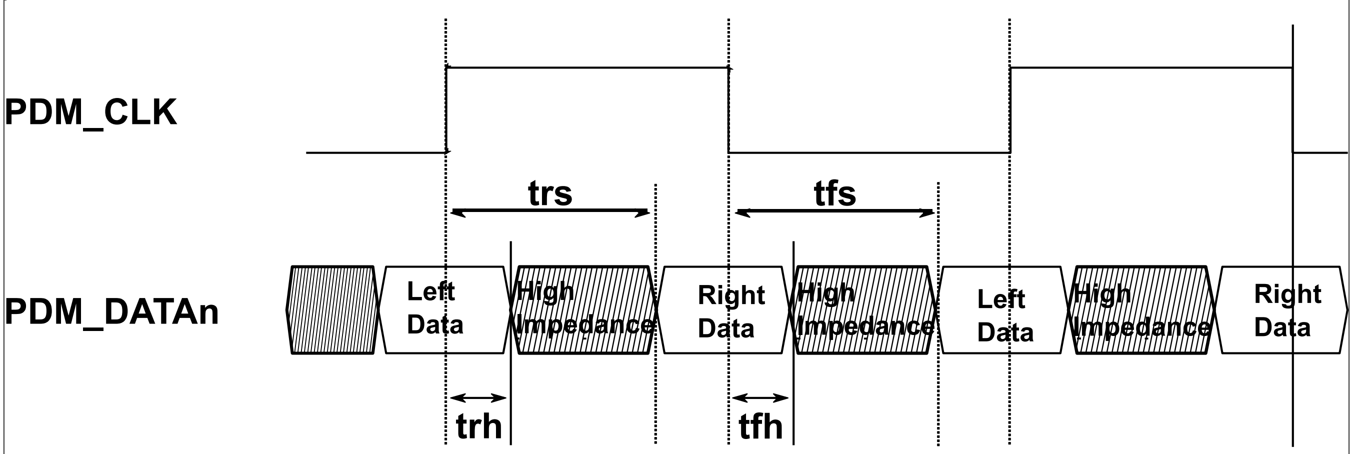


Figure 19. PDM input/output timing requirements

4.9.4 Medium Quality Sound (MQS) electrical specifications

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. Two outputs are asynchronous PWM pulses and their maximum frequency is 1/32 x mclk_frequency.

Table 55. Medium Quality Sound (MQS) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fmclk	Bit clock is used to generate the mclk.	—	24.576	66.5	MHz	—	—

Frequency of mclk depends on software settings.

See Section, General purpose I/O AC parameters for other electrical specifications.

4.10 Display and graphics

This section introduces the timing and electrical parameters about display and graphic interfaces.

4.10.1 MIPI D-PHY electrical characteristics

The i.MX 95 processors conform to the MIPI CSI-2 and D-PHY standards for protocol and electrical specifications.

Compatible with standards:

- MIPI Alliance Specification for Display Serial Interface Version 1.2 (MIPI DSI controller)
- MIPI Standard 1.2 for D-PHY (MIPI DSI D-PHY)
- Compatible with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 2.1

4.10.1.1 HS Transmitter DC parameters

Table 56. HS Transmitter DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VCMTX	HS transmitter static common-mode voltage	150	200	250	mV	(VP-VN)/2; Value when driven into a load impedance in the Zid range.
VOHHS	HS output high voltage	—	—	360	mV	Value when driven into a load impedance in the Zid range.
VOD	HS transmit absolute differential voltage	150	200	250	mV	—

4.10.1.2 HS Transmitter AC timing

Table 57. HS Transmitter AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition
TCLKP	HS Clock Period	0.8	—	25	ns	80 Ω ≤ RL ≤ 125 Ω
TSKEW[TX]	Data to clock skew	-0.15	—	0.15	UIinst	> 0.08Gbps, < 1Gbps
TSKEW[TX]	Data to clock skew	-0.2	—	0.2	UIinst	> 1Gbps, < 1.5Gbps
TSKEW[TLIS]	Data to clock skew	-0.2	—	0.2	UIinst	> 0.08Gbps, < 1Gbps
TSKEW[TLIS]	Data to clock skew	-0.1	—	0.1	UIinst	> 1Gbps, < 1.5Gbps

Table continues on the next page...

Table 57. HS Transmitter AC timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
TSKEW[TX] static	Static data to clock skew (TX)	-0.2	—	0.2	UIinst	> 1.5Gbps
TSKEW[TLIS] static	Static data to clock skew (channel)	-0.1	—	0.1	UIinst	> 1.5Gbps
TSKEW[TX] dynamic	Dynamic data to clock skew	-0.15	—	0.15	UIinst	> 1.5Gbps
TSKEWCAL initial	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	—	—	100	us	> 1.5Gbps
TSKEWCAL initial	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	2^15	—	—	UIinst	> 1.5Gbps
TSKEWCAL periodic	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	—	—	10	us	> 1.5Gbps
TSKEWCAL periodic	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	2^15	—	—	UIinst	> 1.5Gbps
ΔVCMTX(HF)	Common mode variations above 450 MHz	—	—	15	mV(RMS)	—
ΔVCMTX(LF)	Common mode variations between 50MHz - 450 MHz	—	—	25	mV(RMS)	—
trise_fall	20% - 80% rise and fall time	100	—	—	ps	Data rate <= 1.5Gbps
trise_fall	20% - 80% rise and fall time	—	—	0.4	UI	Data rate > 1.5Gbps
trise_fall	20% - 80% rise and fall time	50	—	—	ps	Data rate > 1.5Gbps
RATE[TX]	Transmit Serial Data Rate	80	—	2500	Mbps	per lane, 80 Ω ≤ RL ≤ 125 Ω

4.10.1.3 HS Receiver DC parameters

Table 58. HS Receiver DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VIDTH	Differential input high voltage	—	—	70	mV	Data rate <= 1.5Gbps
VIDTH	Differential input high voltage	—	—	40	mV	Data rate > 1.5Gbps
VIDTL	Differential input low voltage	-70	—	—	mV	Data rate <= 1.5Gbps
VIDTL	Differential input low voltage	-40	—	—	mV	Data rate > 1.5Gbps
VIHHS	Single-ended input high voltage	—	—	460	mV	—
VILHS	Single-ended input low voltage	-40	—	—	mV	—

Table continues on the next page...

Table 58. HS Receiver DC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VCMRX_DC	Input common-mode voltage	70	—	330	mV	—
ZID	Differential input impedance	80	100	125	Ohm	—

4.10.1.4 HS Receiver AC timing

Table 59. HS Receiver AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition
ΔVCMRX(HF)	HS common mode interference beyond 450 MHz	—	—	50	mV	Data rate > 1.5Gbps
ΔVCMRX(LF)	HS common mode interference between 50MHz and 450 MHz	-25	—	25	mV	Data rate > 1.5Gbps
RATE[RX]	Receive Serial Data Rate	80	—	2500	Mbps	80 Ω ≤ RL ≤ 125 Ω
TSKEW[RX] static	Static data to clock skew (RX) tolerance	-0.3	—	0.3	UIinst	> 1.5Gbps, < 2.5Gbps
TSETUP	Data to clock setup time	0.15	—	—	UIINST	> 0.08Gbps, <= 1Gbps
TSETUP	Data to clock setup time	0.2	—	—	UIINST	> 1Gbps, <= 1.5Gbps
THOLD	Clock to data hold time	0.15	—	—	UIINST	> 0.08Gbps, <= 1Gbps
THOLD	Clock to data hold time	0.2	—	—	UIINST	> 1Gbps, <= 1.5Gbps

4.10.1.5 LP Transmitter DC parameters

Table 60. LP Transmitter DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VOL	Output low voltage level	-50	—	50	mV	—
VOH	Output high voltage level	1.1	—	1.3	V	Data rate <= 1.5Gbps
VOH	Output high voltage level	0.95	—	1.3	V	Data rate > 1.5Gbps

4.10.1.6 LP Transmitter AC timing

Table 61. LP Transmitter AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition
Tflp, Tflp	LP 15%-85% signal rise/fall time	—	—	25	ns	—
tslew	Output slew rate	—	—	150	mV/ns	@CLOAD = 70pF
tslew_fall	Output slew rate (falling edge)	25	—	—	mV/ns	@CLOAD = 0pF - 70pF
tslew_rise	Output slew rate (rising edge)	25	—	—	mV/ns	@CLOAD = 0pF - 70pF
CLOAD	Output load capacitance	—	—	70	pF	—

4.10.1.7 LP Receiver DC parameters

Table 62. LP Receiver DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VIL-LP	Input low voltage	—	—	550	mV	—
VIH-LP	Input high voltage	740	—	—	mV	Data rate > 1.5Gbps
VIH-LP	Input high voltage	880	—	—	mV	Data rate <= 1.5Gbps
VHYST	Input hysteresis	25	—	—	mV	—

4.10.1.8 LP Receiver AC timing

Table 63. LP Receiver AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition
eSPIKE	LP input pulse rejection	—	—	300	V.ps	Time-voltage integration of a voltage spike above VIL in LP-0 state, or below VIH in LP-1 state. Receiver does not change state if maximum pulse specification is met.
TMIN_RX	LP minimum input pulse	20	—	—	ns	Minimum pulse width recognized by the receiver.
VINT	LP peak interference voltage	—	—	200	mV	—
fINT	LP interference frequency	450	—	—	MHz	—

4.11 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC5.1 (single data rate) timing, eMMC5.1/ SD3.0 (dual data rate) timing and SDR50/SDR104 AC timing.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.11.1.1 uSDHC DC electrical characteristics (NVCC_xxx = 1.8V)

For recommended operating conditions, see Recommended Operating Conditions

Table 64. uSDHC DC electrical characteristics (NVCC_xxx = 1.8V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage. [1]	0.7 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1]	—	—	0.3 x NVCC_xxx	V	—	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	uA	—	—
VOH	Output high voltage (IOH = -2mA at NVCC_xxx min)	NVCC_xxx - 0.45	—	—	V	—	—
VOL	Output low voltage (IOL = 2mA at NVCC_xxx min)	—	—	0.45	V	—	—

[1] The min VIL and max VI vlaues are based on the respective min and max VDD values found in Recommended Operating Conditions

4.11.1.2 uSDHC DC electrical characteristics (NVCC_xxx = 3.3V)

For recommended operating conditions, see Recommended Operating Conditions

Table 65. uSDHC DC electrical characteristics (NVCC_xxx = 3.3V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage [1]	0.625 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1]	—	—	0.25 x NVCC_xxx	V	—	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	uA	—	—
VOH	Output high voltage (IOH = -2mA at NVCC_xxx min)	0.75 x NVCC_xxx	—	—	V	—	—
VOL	Output low voltage (IOL = 2mA at NVCC_xxx min)	—	—	0.125 x NVCC_xxx	V	—	—

[1] The min VIL and max VI vlaues are based on the respective min and max VDD values found in Recommended Operating Conditions

4.11.1.3 uSDHC AC HS

Table 66. uSDHC AC HS

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	eMMC Low Speed 1.8V/3.3V	—	—	50	KHz	—	—
—	eMMC Full Speed/ High Speed 1.8v/ 3.3V	—	—	26/52	MHz	—	—
—	SD/SDIO SDR12/ SDR25 1.8V	—	—	25/50	MHz	—	—
—	SD/SDIO Identification Mode 3.3V	—	—	400	KHz	—	—
—	SD/SDIO Default Speed/High Speed 3.3V	—	—	25/50	MHz	—	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	2	ns	—	—
—	Duty Cycle distortion	45	—	55	%	—	—
tNIKHOX	Master output hold time (ns)	3.7	—	—	ns	—	—
tNIKHOV	Master output delay (ns)	—	—	12.8	ns	—	—
tNIIVKH	Input setup Time (ns)	2.8	—	—	ns	—	—
tNIIXKH	Input Hold Time (ns)	1.5	—	—	ns	—	—

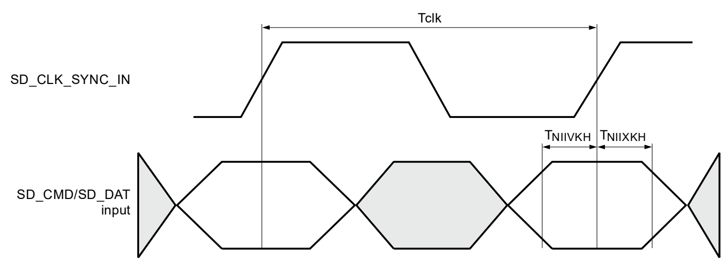


Figure 20. uSDHC AC HS timing

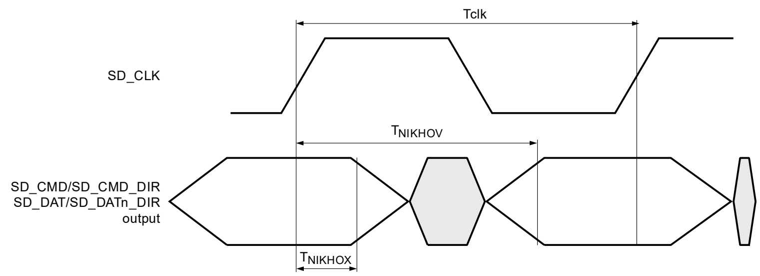


Figure 21. uSDHC AC HS timing 1

4.11.1.4 uSDHC AC DDR

Table 67. uSDHC AC DDR

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	eMMC High Speed DDR 1.8v	—	—	52	MHz	—	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	3	ns	—	—
—	Duty Cycle distortion	45	—	55	%	—	—
tNDKHOX	Master output hold time for SD_DATn (ns)	3	—	—	ns	—	—
tNDKHOV	Master output delay for SD_DATn (ns)	—	—	6.5	ns	—	—
tNDIVKH	Input setup Time for SD_DATn (ns)	2	—	—	ns	—	—
tNDIXKH	Input Hold Time for SD_DATn (ns)	1.5	—	—	ns	—	—
tNIKHOX	Master output hold time for SD_CMD (ns)	3.7	—	—	ns	—	—
tNIKHOV	Master output delay for SD_CMD (ns)	—	—	13	ns	—	—
tNIIVKH	Input setup Time for SD_CMD (ns)	5	—	—	ns	—	—
tNIIXKH	Input Hold Time for SD_CMD (ns)	1.5	—	—	ns	—	—

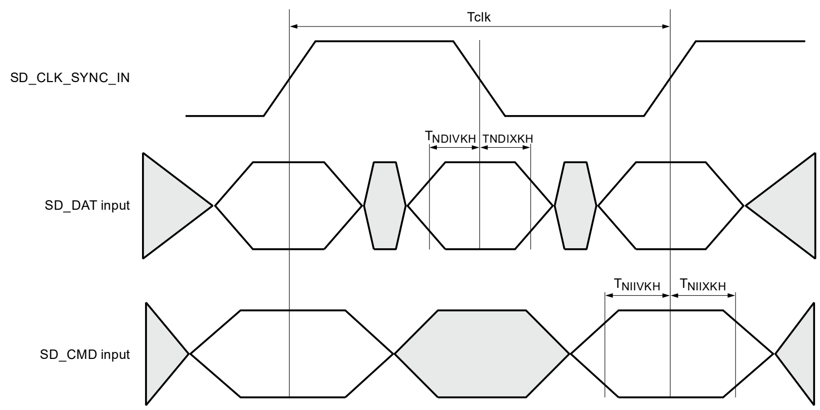


Figure 22. uSDHC AC DDR timing 1

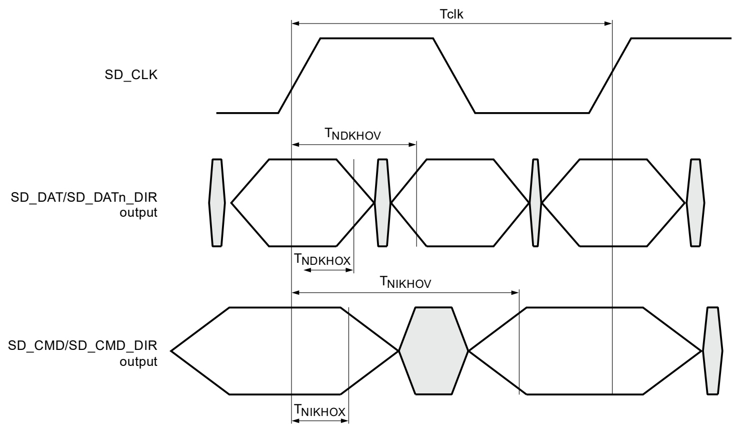


Figure 23. uSDHC AC DDR timing 2

4.11.1.5 uSDHC AC SDR50

Table 68. uSDHC AC SDR50

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	100	MHz	Nominal and Overdrive mode	—
tRISE/FALL	Clk Rise/Fall Time (ns)	—	—	2	ns	Nominal and Overdrive mode	—
—	Duty Cycle distortion	—	—	0.3	ns	Nominal and Overdrive mode	—
tNIKHOX	Master output hold time (ns)	1.2	—	—	ns	Nominal and Overdrive mode	—
tNIKHOV	Master output delay (ns)	—	—	6.6	ns	Nominal and Overdrive mode	—
tNDIVKH	Input setup Time for SD_DATn (ns)	2.1	—	—	ns	Nominal and Overdrive mode	—

Table continues on the next page...

Table 68. uSDHC AC SDR50*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tNDIXKH	Input Hold Time for SD_DATn (ns)	1.5	—	—	ns	Nominal and Overdrive mode	—

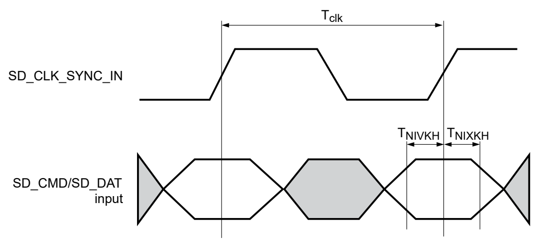


Figure 24. uSDHC AC SDR50 timing

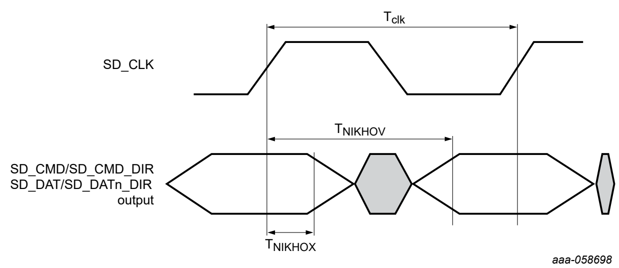


Figure 25. uSDHC AC SDR50 timing 2

4.11.1.6 uSDHC AC SDR104

Table 69. uSDHC AC SDR104

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	200	MHz	Nominal and Overdrive mode	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	1	ns	Nominal and Overdrive mode	—
—	Duty Cycle distortion	—	—	0.3	ns	Nominal and Overdrive mode	—
tNIKHOX	Master output hold time (ns)	1.2	—	—	ns	Nominal and Overdrive mode	—
tNIKHOV	Master output delay (ns)	—	—	3.1	ns	Nominal and Overdrive mode	—
tIDV	Input data window (UI)	0.5	—	—	UI	Nominal and Overdrive mode	—
Fsck	Max. Frequency (MHz)	—	—	133	MHz	Low drive mode	—

Table continues on the next page...

Table 69. uSDHC AC SDR104*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRISE/tFALL	Clk Rise/Fall Time (ns)	—	—	1	ns	Low drive mode	—
—	Duty cycle distortion	—	—	0.45	ns	Low drive mode	—
tNIKHOX	Master output hold time (ns)	1.35	—	—	ns	Low drive mode	—
tNIKHOV	Master output delay (ns)	—	—	5	ns	Low drive mode	—
tIDV	Input data window (UI)	0.5	—	—	UI	Low drive mode	—

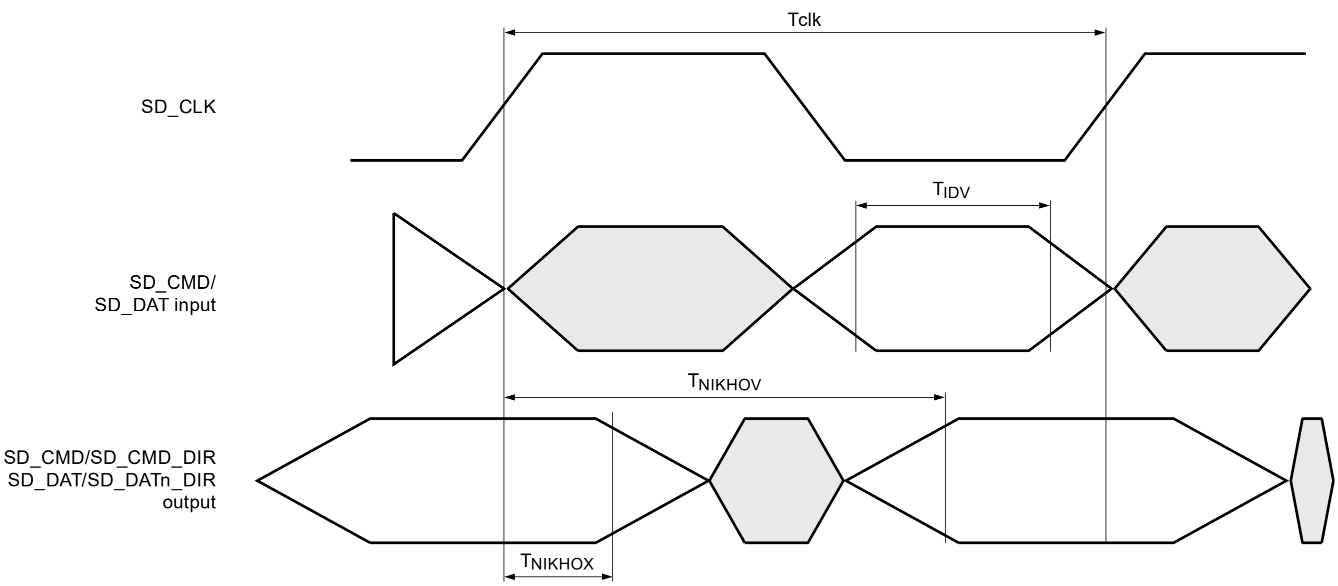


Figure 26. uSDHC AC SDR104 timing

4.11.1.7 uSDHC SDR HS 200 AC timing

Table 70. uSDHC SDR HS 200 AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	200	MHz	Nominal and Overdrive mode	—
tRISE/TFALL	Clk Rise/Fall Time (ns)	—	—	1	ns	Nominal and Overdrive mode	—
—	Duty Cycle Distortion	—	—	0.3	ns	Nominal and Overdrive mode	—

Table continues on the next page...

Table 70. uSDHC SDR HS 200 AC timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tNIKHOX	Master output hold time (ns)	1.4	—	—	ns	Nominal and Overdrive mode	—
tNIKHOV	Master output delay (ns)	—	—	3.1	ns	Nominal and Overdrive mode	—
tIDV	Input data window (UI)	0.475	—	—	UI	Nominal and Overdrive mode	—
Fsck	Max. Frequency (MHz)	—	—	133	MHz	Low drive mode	—
tRISE/tFALL	Clk Rise/Fall Time (ns)	—	—	1.5	ns	Low drive mode	—
—	Duty Cycle Distortion	—	—	0.45	ns	Low drive mode	—
tNIKHOX	Master output hold time (ns)	1.4	—	—	ns	Low drive mode	—
tNIKHOV	Master output delay (ns)	—	—	5	ns	Low drive mode	—
tIDV	Input data window (UI)	0.475	—	—	UI	Low drive mode	—

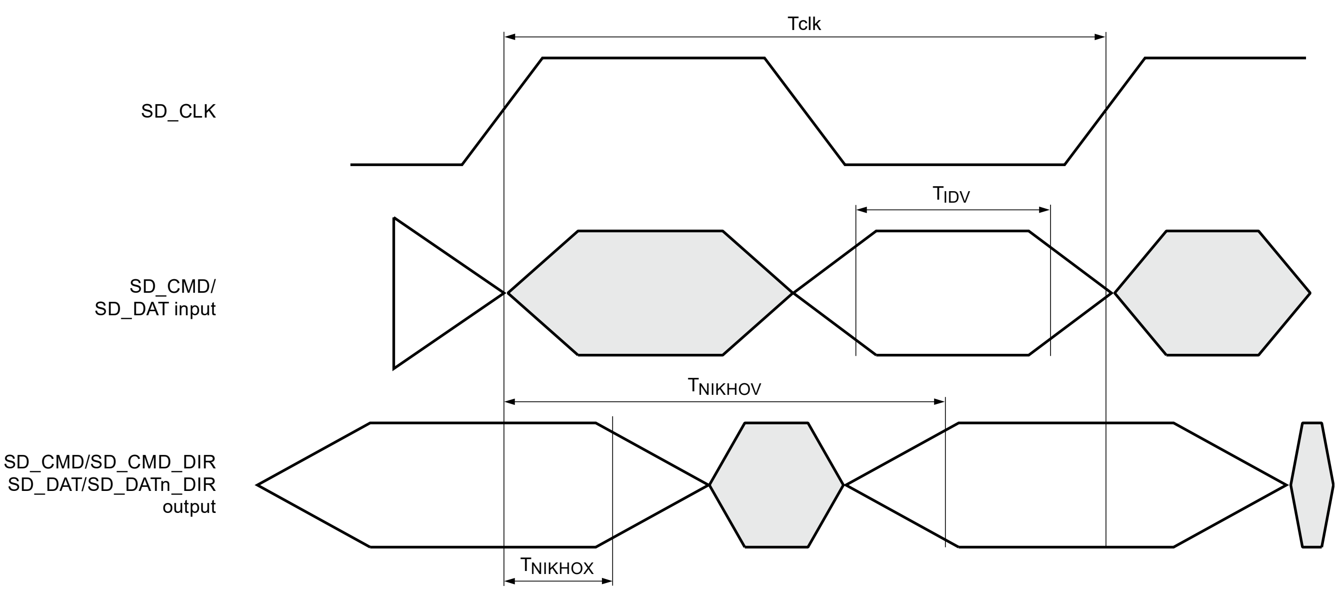


Figure 27. uSDHC AC HS200 timing

4.11.1.8 uSDHC DDR HS 400 AC timing

Table 71. uSDHC DDR HS 400 AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsck	Max. Frequency (MHz)	—	—	200	MHz	Nominal and Overdrive mode	—
—	Duty Cycle distortion	0	—	0.3	ns	Nominal and Overdrive mode	—
tCL	Clock low time	2.2	—	—	ns	Nominal and Overdrive mode	—
tCH	Clock high time	2.2	—	—	ns	Nominal and Overdrive mode	—
tSHKHOX	Master output hold time (ns)	0.6	—	—	ns	Nominal and Overdrive mode	—
tSHKHOV	Master output delay (ns)	—	—	1.85	ns	Nominal and Overdrive mode	—
tSHRQV	Data valid skew to DQS [1]	—	—	0.75	ns	Nominal and Overdrive mode	—
tSHRQHX	Data hold skew to DQS [1]	—	—	0.75	ns	Nominal and Overdrive mode	—
tSHRQV_CMD	Commad valid skew to DQS [1]	—	—	0.75	ns	Nominal and Overdrive mode	—
tSHRQHX_CMD	Command hold skew to DQS [1]	—	—	0.75	ns	Nominal and Overdrive mode	—
tSHDSPWS	DQS pulse width (ns)	1.9	—	—	ns	Nominal and Overdrive mode	—
Fsck	Max. Frequency (MHz)	—	—	133	MHz	Low Drive mode	—
—	Duty Cycle distortion	—	—	0.45	ns	Low Drive mode	—
tCL	Clock low time	3.3	—	—	ns	Low Drive mode	—
tCH	Clock high time	3.3	—	—	ns	Low Drive mode	—
tSHKHOX	Master output hold time (ns)	0.8	—	—	ns	Low Drive mode	—
tSHKHOV	Master output delay (ns)	—	—	2.95	ns	Low Drive mode	—
tSHRQV	Data valid skew to DQS	—	—	0.8	ns	Low Drive mode	—
tSHRQHX	Data hold skew to DQS	—	—	0.8	ns	Low Drive mode	—
tSHRQV_CMD	Command valid skew to DQS	—	—	0.8	ns	Low Drive mode	—

Table continues on the next page...

Table 71. uSDHC DDR HS 400 AC timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSHRQHX_CMD	Command hold skew to DQS	—	—	0.8	ns	Low Drive mode	—
tSHDSPWS	DQS pulse width (ns)	2.9	—	—	ns	Low Drive mode	—
—	DQS Duty Cycle distortion	—	—	0.3	ns	Nominal and Overdrive mode	—

[1] Board skew margin between DQS and DATA/CMD is considered as +/-50 ps in calculations

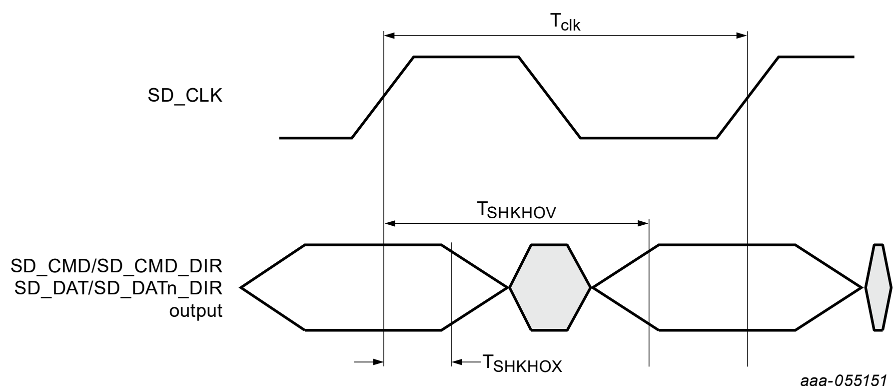


Figure 28. uSDHC AC HS400 timing

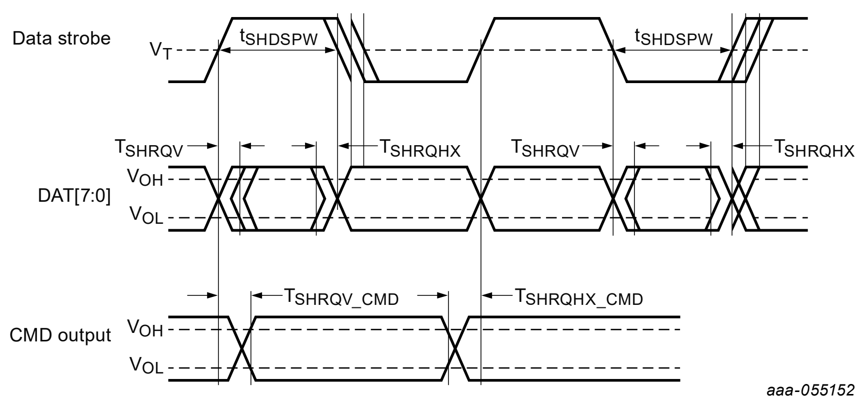


Figure 29. uSDHC AC HS400 timing 1

4.11.1.9 uSDHC supported modes

For SD:

- All SD 3.0 protocols are supported at full speeds on all three SDHC interfaces. This includes DS, HS, SDR12, SDR25, SDR50, SDR104, and DDR50.
- The maximum supported SDR frequency is 200 MHz which is covered in SDR104 mode, and maximum DDR frequency is 50 MHz as a part of DDR50 mode.

For eMMC:

- eMMC HS400 is only supported on SDHC1 as that is the only one with 8-bit interface.

- eMMC HS200 is supported on all three SDHC interfaces because this protocol supports both 4-bit mode and 8-bit mode, which can work on SDHC2 and SDHC3.
- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are also supported on all three SDHC interfaces.
- The maximum supported SDR frequency is 200 MHz which is covered in HS200 mode, and the maximum DDR frequency is 200 MHz as a part of HS400 mode.

uSDHC3 is multiplexing on GPIO_IO[27:22], below are the modes which are targeted:

- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are supported.
- SDR50 (100 MHz) and SDR104 (200 MHz) modes are NOT supported.
- eMMC HS400 and HS200 modes are NOT supported
- The maximum supported SDR and DDR frequency is 50 and 52 MHz

If I/O is supplied by 3.3 V, the maximum supported SDR/DDR frequency is 50/52 MHz

4.11.2 Ethernet controller (ENET)

Ethernet supports the following key features:

- Support ENET AVB
- Support IEEE 1588
- Support Energy Efficient Ethernet (EEE)
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation
- SGMII (1G and 2.5G), USXGMI, and XFI

The following sections describe the DC and AC electrical characteristics for the EMI, RMII, RGMII, and IEEE standard 1588 interfaces.

4.11.2.1 Ethernet Management Interface (EMI)

This section describes the electrical characteristics for the EMI interface.

4.11.2.1.1 Ethernet management interface AC Timing specifications

This table describes the EMI AC timing specifications

Table 72. Ethernet management interface AC Timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fMDC	Clock frequency [1]	—	0.664	2.5	MHz	—	—
tMGCH	MDC clock pulse width high	40	—	60	%	—	—
tMGCL	MDC clock pulse width low	40	—	40	%	—	—
tMDKHDX	MDC to MDIO output delay [2][3]	Y x tENET_CLK - 3	—	Y x tENET_CLK + 8	—	NEG=0	—

Table continues on the next page...

Table 72. Ethernet management interface AC Timing specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMDKHDX	MDC to MDIO output delay [2][3][4]	Y x tENET_CLK - 3	—	Y x tENET_CLK + 8	—	NEG=1	—
tMDDVKH	MDIO to MDC input setup time [5]	8	—	—	ns	—	—
tMDDXKH	MDIO to MDC input hold time	0	—	—	ns	—	—

[1] This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the MDC clock frequency.
[2] tENET_CLK = 333 Mhz max.
[3] MDIO timing is configurable by programming the EMDIO_CFG register fields. The default value of Y = 5. Y is the value determined by EMDIO_CFG[NEG], EMDIO_CFG[MDIO_HOLD], and MDIO[EHOLD]. The easiest way is to program NEG=1, then MDIO is driven at negative edge of MDC, satisfying both setup and hold time requirement of Ethernet PHY.
[4] For NEG=0: Y = (1+(2+6*EHOLD)*MDIO_HOLD) For NEG=1: Y= (MDIO_CLK_DIV + 1)
[5] The setup time tMDDVKH is measured at a) 470pf load @ 1.8V in open-drain mode b) 300pf load @ 1.8V in push-pull mode

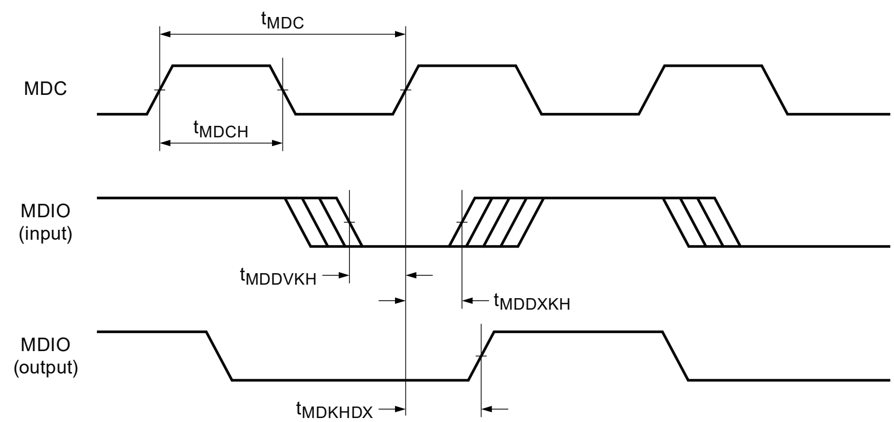


Figure 30. Ethernet management interface timing diagram

4.11.2.1.2 Ethernet management interface DC electrical characteristics at voltage rail =1.8V

This table provides the EMI DC electrical characteristics

Table 73. Ethernet management interface DC electrical characteristics at voltage rail =1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	0.7 x SUPPLY	—	—	V	—	—
VIL	Input low voltage	—	—	0.3 x SUPPLY	V	—	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±50	μA	—	—

Table continues on the next page...

Table 73. Ethernet management interface DC electrical characteristics at voltage rail =1.8V...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—	—

4.11.2.1.3 Ethernet reference clock

Tie any reference clock inputs that are not used to ground.

4.11.3 XFI

XFI Electricals are compatible with Electrical Specifications as defined in INF-8077i10 Gigabit Small Form Factor Pluggable Module Revision 4.5, August 31, 2005 which supports IEEE.Std-802.3ae

Table 74. XFI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval (mean)	96.96	96.97	96.979	ps	—	—
CTX	AC Coupling Capacitor [1]	—	100	—	nF	—	—
REXT	External Reference Resistor (RESREF) [2]	—	200	—	Ohms	—	—

[1] If lane is used for multiple Ethernet rates, then capacitor value must be chosen to accomodate highest rate.
[2] REXT requires 1% 100ppm/C precision resistor-to-ground on PC Board

4.11.3.1 XFI Transmitter DC Specifications

Table 75. XFI Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TX_Vdiff	Output Differential Voltage	360	—	770	mV	—	—
Zd	Reference Differential Impedance	85	100	115	Ohms	—	—

4.11.3.2 XFI Transmitter AC Specifications

Table 76. XFI Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tr/Tf	Output Rise/Fall Time (20% to 80%)	24	—	—	ps	—	—
Dj	Deterministic Jitter [1]	—	—	0.15	UI	—	—
Tj	Total Jitter [1]	—	—	0.3	UI	—	—
EM_X1	Eye Mask Time X1 [2]	—	—	0.15	UI	—	—
EM_X2	Eye Mask Time X2 [2]	—	—	0.4	UI	—	—
EM_Y1	Eye Mask Voltage Y1 [2]	180	—	—	mV	—	—
EM_Y2	Eye Mask Voltage Y2 [2]	—	—	385	mV	—	—

[1] In loop timing mode, includes jitter that transfers through the ASIC from the receiver during any valid operational input conditions.
[2] See Eye Mask Figure, Eye_Mask_TX, XFI SerDes Transmitter differential output

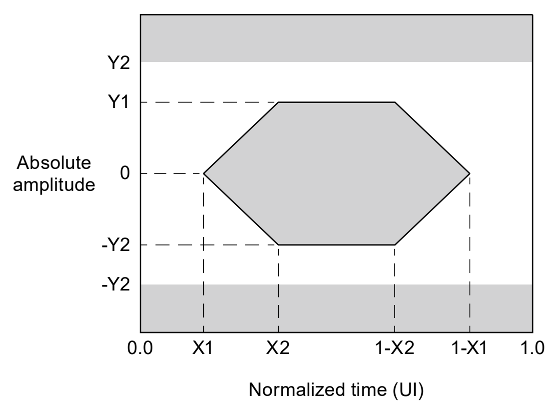


Figure 31. Eye_Mask_TX

4.11.3.3 XFI Receiver DC Specifications

Only a compliant transmitter passing through a compliant XFI channel is guaranteed for interoperability with the receiver.

Table 77. XFI Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ZRX-DC	Receiver reference Differential Impedance	85	100	115	Ω	—	—

4.11.3.4 SGMII

SGMII electrical specifications will be compatible with the 1000Base-KX electrical specifications based on IEEE802.3 Clause 70.7.

4.11.3.5 2.5G SGMII

2.5GSGMII Electricals are compatible with Electrical Specifications as defined in IEEE 802.3-2018, Clause 47 (XAUI)

Table 78. 2.5G SGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval (mean)	319.968	320	320.032	ps	—	—
CTX	AC Coupling Capacitor	—	4.7	—	nF	—	—
REXT	External Reference Resistor (RESREF) [1]	—	200	—	Ohms	—	—

[1] REXT requires 1% 100ppm/C precision resistor-to-ground on PC Board

4.11.3.5.1 2.5G SGMII Transmitter DC Specifications

Table 79. 2.5G SGMII Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDIFF_PK-PK	Differential peak-to-peak output voltage	—	—	1600	mVp-p	—	—
DC_CM_Volt	Absolute Output Voltage Limits	-0.4	—	2.3	V	—	—

4.11.3.5.2 2.5G SGMII Transmitter AC Specifications

Table 80. 2.5G SGMII Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Trise_fall_typ	Transmit Vod rise time (20-80%) [1]	—	35	—	ps	Measured on Typical Silicon at Nominal Voltages and Room Temperature	—
Dj_NE	Near End Deterministic Jitter	—	—	0.17	UI	Peak to Peak	—
Tj_NE	Near End Total jitter	—	—	0.35	UI	Peak to Peak	—
TEYE-A2_NE	Near End TX Eye Mask A2 Differential Amplitude overall UI	-800	—	800	mV	at BER = 1E-12	—

Table continues on the next page...

Table 80. 2.5G SGMII Transmitter AC Specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TEYE-A1_NE	Near End TX Eye Mask A1 Differential Amplitude at X2 UI	-400	—	400	mV	at BER = 1E-12	—
TEYE-X1_NE	Near End TX Eye Mask X1 jitter at 0 Differential Amplitude	—	—	0.175	UI	measured from 0UI and 1UI cross points at BER = 1E-12	—
TEYE-X2_NE	Near End TX Eye Mask X2 jitter at A1 Differential Amplitude	—	—	0.390	UI	measured from 0UI and 1UI cross points at BER = 1E-12	—
TEYE-X1_FE	Far End TX Eye Mask X1 jitter at 0 Differential Amplitude	—	—	0.275	UI	measured from 0UI and 1UI cross points at BER = 1E-12	—
TEYE-X2_FE	Far End TX Eye Mask X2 jitter at A1 Differential Amplitude	—	—	0.400	UI	measured from 0UI and 1UI cross points at BER = 1E-12	—

[1] Exception: transition time is faster than recommended

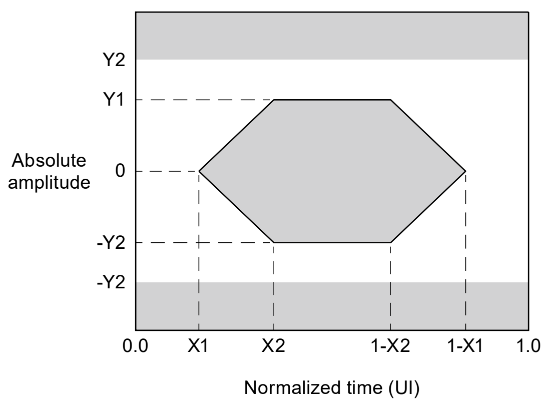


Figure 32. Transmitter Eye Mask

4.11.3.5.3 2.5G SGMII Receiver DC Specifications

Table 81. 2.5G SGMII Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VINdiffpk-pk	Differential Input Pk-Pk amplitude	—	—	1600	mVp-p	—	—

4.11.4 RGMII inteface

This section describes the electrical characteristics for the RGMII interface.

4.11.4.1 RGMII DC Electrical Characteristics at (voltage rail) ≥ 1.8V

The timings assume the following configuration: CTL[5:0] = 001111 and SL[1:0] = 11. Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (15 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver. RGMII timing specifications are only valid for 1.8 V nominal I/O pad supply voltage. The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver device

Timing is valid for RGMII unless stated otherwise.

Table 82. RGMII Electrical Characteristics at (voltage rail) ≥ 1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage [1]	0.7 x SUPPLY	—	—	V	—
VIL	Input low voltage [1]	—	—	0.3 x SUPPLY	V	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN) [2]	—	—	±50	μA	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA) [2]	SUPPLY - 0.2	—	—	V	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA) [2]	—	—	0.2	V	—

[1] The min VIL and max VIH values are based on the respective min and max (supply) values found in Recommended Operating Conditions.
[2] The symbol (supply) represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

4.11.4.2 RGMII AC Timing Specifications

Timing is valid for RGMII unless stated otherwise.

Table 83. RGMII AC Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSKRGTTX	Data to clock output skew (at transmitter) [1]	-500	0	500	ps	—	—
tSKRGTRX	Data to clock input skew (at receiver) [2]	1	—	2.6	ns	—	—
tRGT	Clock period duration [3]	7.2	8	8.8	ns	—	—
tRGTHtRGT	Duty cycle for 10BASE-T and 100BASE-TX [3][4]	40	50	60	%	—	—
tRGTHtRGTgig	Duty cycle for Gigabit	45	60	55	%	—	—

Table continues on the next page...

Table 83. RGMII AC Timing Specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRGTR-HP	Rise time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	0.75	ns	—	—
tRGTR-OpenAlliance	Rise time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	1	ns	—	—
tRGTF-HP	Fall time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	0.75	ns	—	—
tRGTF-OpenAlliance	Fall time (20%-80%) SUPPLY = 1.8V [5][6]	—	—	1	ns	—	—

[1] The frequency of RGMII input clk should not exceed the frequency of RGMII output clk by more than 300 ppm.
[2] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
[3] For 10 and 100 Mbps, tRGT scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
[4] Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.
[5] Applies to inputs and outputs.
[6] The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

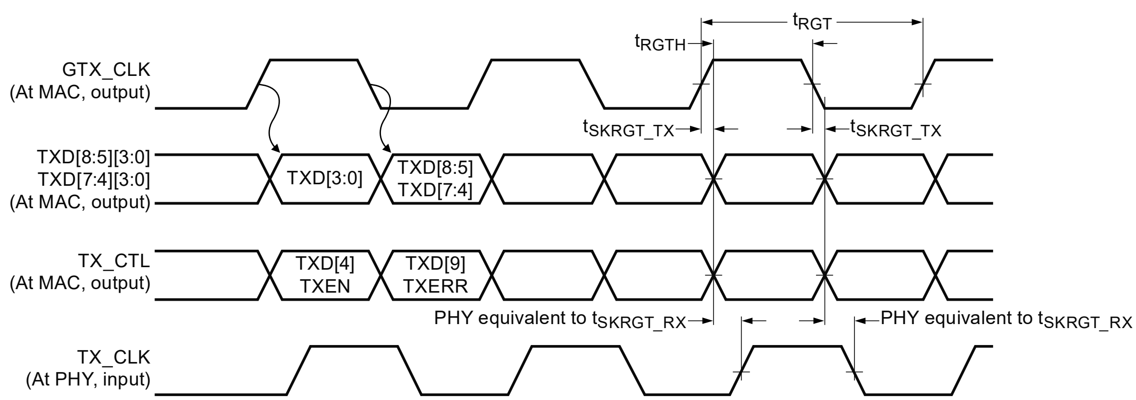


Figure 33. AC Transmit timing and multiplexing diagrams

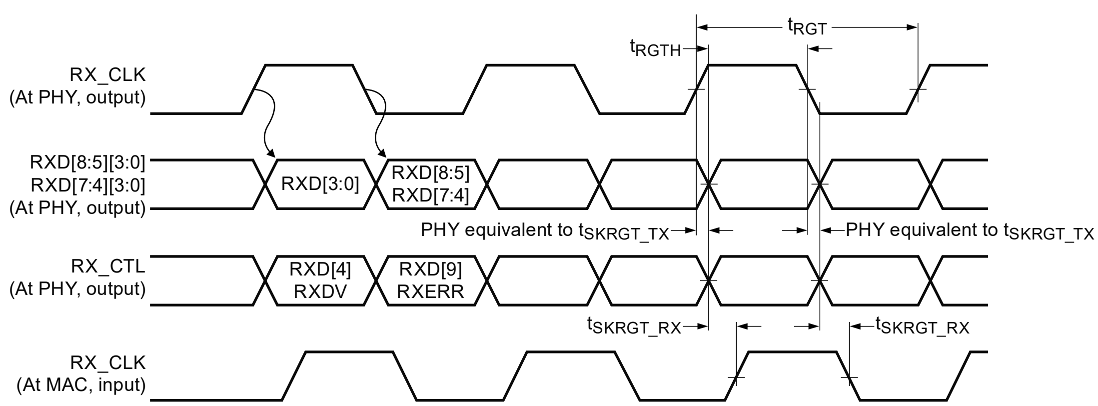


Figure 34. Receive timing and multiplexing diagram

4.11.5 RMII interface

This section describes the electrical characteristics for the RMII interface.

4.11.5.1 RMII DC Electrical Characteristics at voltage rail = 3.3V

Timing is valid for RMII unless stated otherwise.

Table 84. RMII DC Electrical Characteristics at voltage rail = 3.3V

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	2	—	—	V	—	—
VIL	Input low voltage	—	—	0.8	V	—	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±5	μA	—	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—	—

4.11.5.2 RMII DC Electrical Characteristics at voltage rail =1.8V

Timing is valid for RMII unless stated otherwise.

Table 85. RMII DC Electrical Characteristics at voltage rail =1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	0.7 x SUPPLY	—	—	V	—	—
VIL	Input low voltage	—	—	0.3 x SUPPLY	V	—	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±50	μA	—	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—	—

4.11.5.3 RMII AC Timing Specifications

Timing is valid for RMII unless stated otherwise.

Table 86. RMII AC Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tRMT	TX Clock period duration	15	20	25	ns	—	—
tRMTH	TX Clock Duty cycle for 10BASE-T and 100BASE-TX	35	50	65	%	—	—
tRMTR	TX Rise time (20%-80%)	1	—	5	ns	—	—
tRGTF	TX Fall time (20%-80%)	1	—	5	ns	—	—
tRMTJ	TX Clock peak-to-peak jitter	—	—	250	ps	—	—
tRMTDX	TX Clock to Data/ TX_EN Delay	2	—	14	ns	—	—
tRMRDV	RXD/CRS_DV/ RXER to Clock rising edge, setup time	4	—	—	ns	—	—
tRMRDX	Clock rising edge to RXD/CRS_DV/ RXER, hold time	2	—	—	ns	—	—

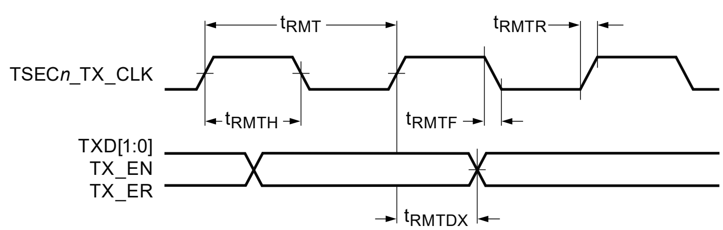


Figure 35. Transmit AC timing diagram

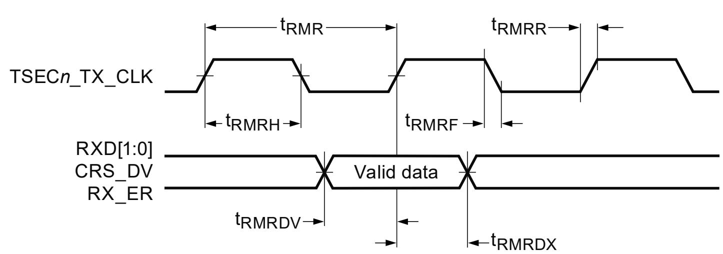


Figure 36. Receive AC timing diagram

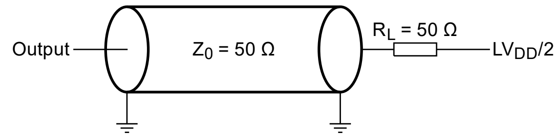


Figure 37. eTSEC AC Test Load

4.11.6 10-Gbit/s ETH clock connectivity

One ETH SerDes interface can support up to 10.3125 Gbit/s with XFI, USXGMII, and SGMII protocols. AC coupling capacitors are required on TX or RX and external 156.25 MHz clock input is required for ETH_REF_PAD_CLK_P/N. The HCSL level can be used directly to the PAD. AC-coupled and common mode termination is needed for the LVDS level input.

Table 87. 10-Gbit/s ETH clock connectivity

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fREF_O	Reference clock frequency offset	-100	—	100	ppm	—	—
RJ_REF_CLK	Reference clock random jitter	—	—	1	ps	Integrated RJ from 12 kHz to 20 MHz	—
RJ_REF_CLK	Reference clock random jitter	—	—	0.8	ps	Integrated RJ from 2 MHz to 20 MHz	—
DJ_REF_CLK	Reference clock deterministic jitter	—	—	1.7	ps	0.75-10 MHz	—
DJ_REF_CLK	Reference clock deterministic jitter	—	—	3.4	ps	0.2-50 MHz	—
DC	Duty cycle	40	—	60	%	—	—
VCM_IL	Common mode input level	0	—	0.8	V	Differential inputs	—
VDIFF_PP	Differential input swing	100	—	—	mVpp	—	—

4.11.7 1000Base-KX

1000Base-KX Electricals are compatible with Electrical Specifications as defined in IEEE 802.3, Clause 70 and is intended for Backplane Applications

4.11.7.1 1000Base-KX Transmitter DC Specifications

Table 88. 1000Base-KX Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDIFF_PK-PK	Differential peak-to-peak output voltage	800	—	1600	mV	—	—

4.11.7.2 1000Base-KX Transmitter AC Specifications

Table 89. 1000Base-KX Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Trise_fall_typ	Transition Time (20% - 80%) [1]	—	25	—	ps	Measured on Typical Silicon at Nominal Voltages and Room Temperature	—
Dj	Deterministic Jitter (Max pk-pk)	—	—	0.1	UI	—	—
Rj	Random jitter	—	—	0.15	UI	—	—
Tj	Total jitter (Max pk-pk at BER 1E-12)	—	—	0.25	UI	—	—
TEYE-X1	TX Eye Mask X1 Time at 0mV Differential Amplitude	—	—	0.125	UI	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—
TEYE-X2	TX Eye Mask X2 Time at +/-A1 Differential Amplitude	—	—	0.325	UI	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—
TEYE-A2	TX Eye Mask A2 Differential Amplitude overall UI	-800	—	800	mV	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—
TEYE-A1	TX Eye Mask A1 Differential Amplitude at X2 UI	-400	—	400	mV	See Eye Mask Figure at TP1, Specified at BER = 1E-12	—

[1] Trise_fall is faster than specified.

Trise_fall is faster than specified.

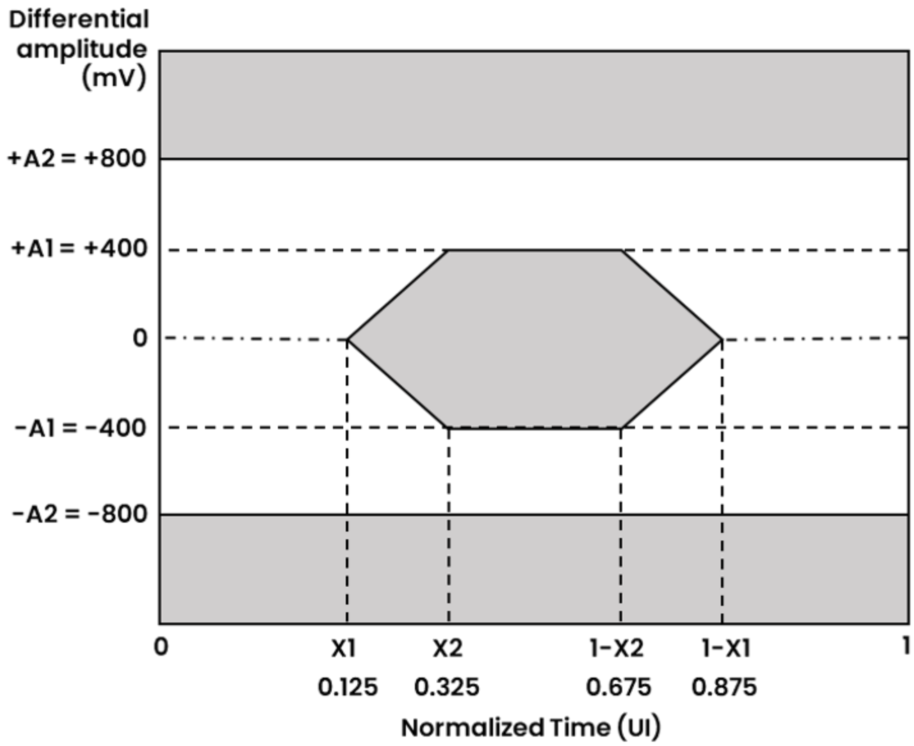


Figure 38. Eye Mask TP1

Table 90. 1000Base-KX Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VINdiffpk-pk	Differential Input Pk-Pk amplitude	—	—	1600	mV	—	—

4.11.8 USXGMII

USXGMII (10G-SXGMII) is specified in CISCO USXGMII Multiport Copper PHY specification EDCS-1517762 v2.15. The electrical specifications are defined to be compatible with 10GBASE-KR electrical characteristics as defined in section 72.7 and Annex 69B of the IEEE 802.3-2008 with No FEC and as modified in CISCO USXGMII Single-port Copper PHY specification EDCS-1150953 v2.2. NXP USXGMII SerDes PHY only supports AC-Coupled links

Table 91. USXGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval (mean)	96.96	96.97	96.979	ps	10.3125 GBd	—
CTX	AC Coupling Capacitor	—	100	—	nF	—	—
REXT	External Reference Resistor (RESREF) [1]	—	200	—	Ohms	—	—

[1] REXT requires 1% 100ppm/C precision resistor-to-ground on PC Board

4.11.8.1 USXGMII Transmitter DC Specifications

NXP's USXGMII PHY Transmitter supports 3-Tap Equalization. Transmitter Equalization must be optimized for the specific channel in use. It is advised that this optimization be done using the IBIS-AMI models. Optimization can also be performed in hardware. As no automatic adaptation is used for the transmitter selection should be chosen as a single setting that works for all PVT cases.

Table 92. USXGMII Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDIFF_PK-PK	Differential peak-to-peak output voltage	—	—	1200	mV	—	—

4.11.8.2 USXGMII Transmitter AC Specifications

Table 93. USXGMII Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Trise_fall	Transition Time (20% - 80%) [1]	24	—	47	ps	—	—
Dj	Deterministic Jitter (pk-pk)	—	—	0.15	UI	—	—
DCD	Duty Cycle Distortion (pk-pk)	—	—	0.035	UI	—	—
Rj	Random jitter	—	—	0.15	UI	—	—
Tj	Total jitter (pk-pk)	—	—	0.28	UI	—	—

[1] Trise_fall is faster than specified.

4.11.8.3 USXGMII Receiver DC Specifications

Table 94. USXGMII Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VINdiffpk-pk	Differential Input Pk-Pk amplitude	—	—	1200	mV	—	—

4.11.8.4 USXGMII Receiver AC Specifications

Table 95. USXGMII Receiver AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
BER	Bit Error Ratio	—	—	1E-12	—	—	—

4.12 WDOG Reset timing parameters

The table lists the WDOG reset timing parameters.

Table 96. WDOG Reset timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CC3	Duration of WDOG_ANY Assertion	1	—	—	RTC_XTALI cycle	—	—

Note: RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

The following figure shows the WDOG reset timing.

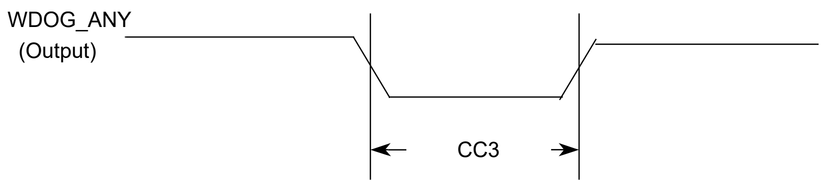


Figure 39. WDOGx_B timing diagram

4.13 IEEE1588 interface

The following table describes the IEEE Std 1588 electrical characteristics.

Table 97. IEEE1588 interface

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tT1588CLK	TMR_1588_CLK_IN clock period	5	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKH/ tT1588CLK	TMR_1588_CLK_IN duty cycle	40	50	60	%	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKINJ	TMR_1588_CLK_IN peak-to-peak jitter	—	—	250	ps	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKINR	Rise time TMR_1588_CLK_IN (20% to 80%)	1.0	—	2.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKINF	Fall time TMR_1588_CLK_IN (80% to 20%)	1.0	—	2.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKOUT	TMR_1588_CLK_OUT clock period	2 x t1588CLK	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588CLKOTH/ tT1588CLKOUT	TMR_1588_CLK_OUT duty cycle	30.0	50.0	70.0	%	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—

Table continues on the next page...

Table 97. IEEE1588 interface*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tT1588OV	TMR_1588_CLK_OUT to TMR_1588_PULSE_OUT1/2,TMR_1588_ALARM_OUT1/2 valid	0.5	—	4.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—
tT1588TRIGH	TMR_1588_TRIG_IN1/2 pulse width	2 x t1588CLK	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11	—

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

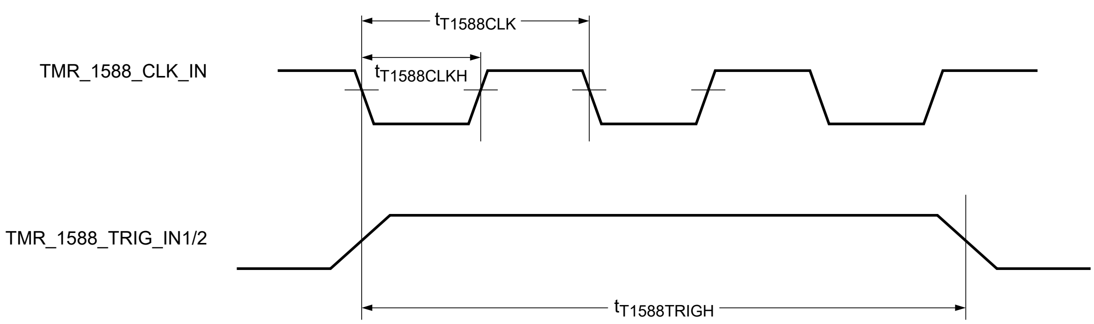
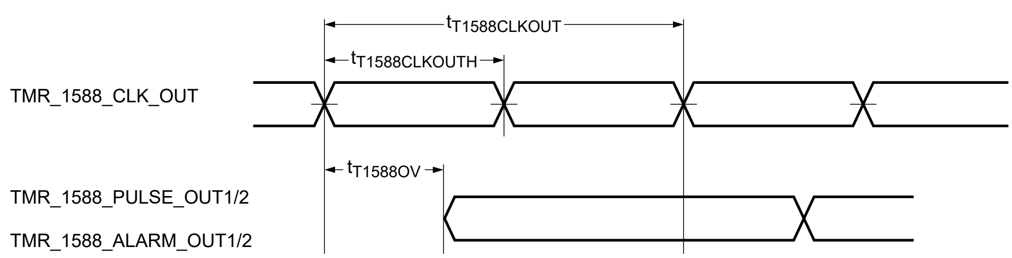


Figure 40. IEEE 1588 input AC timing



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 41. IEEE 1588 output AC timing

4.14 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with Controller and Peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% VDD and 80% VDD thresholds, unless noted, as well as input signal transitions of 3 ns and a 25 pF maximum load on all LPSPI pins.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.14.1 LPSPI DC electrical characteristics

Table 98. LPSPI DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage [1] [2]	0.7 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1] [2]	—	—	0.3 x NVCC_xxx	V	—	—
IIN/IOZ	Input/Output leakage current [1]	-5	—	5	μA	—	—
VOH	Output high voltage [1]	NVCC_xxx - 0.45	—	—	V	IOH = -2 mA at NVCC_xxx min	—
VOL	Output low voltage [1]	—	—	0.45	V	IOL = 2 mA at NVCC_xxx min	—

[1] For recommended operating conditions, see Recommended Operating Conditions.
[2] The minimum VIL and maximum VI values are based on the respective minimum and maximum VDD values found in Recommended Operating Conditions.

4.14.2 LPSPI Controller mode AC timing specifications

Table 99. LPSPI Controller mode AC timing specifications

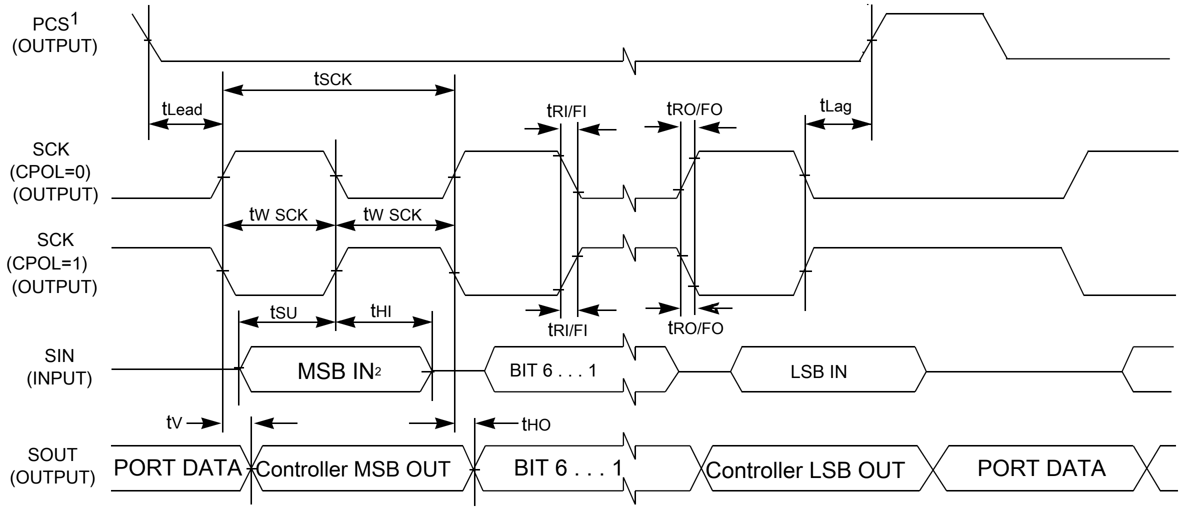
Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	Frequency of LPSPI clock root [1][2][3]	—	—	30	MHz	—	—
fSCK	Frequency of LPSPI clock root [4]	—	—	60	MHz	—	—
tSCK	SCK period [5]	2 x tperiph	—	—	ns	—	—
tLead	Enable lead time	1	—	—	tperiph	—	—
tLag	Enable lag time	1	—	—	tperiph	—	—
tWSCK	Clock (SCK) high or low time	tSCK / 2 - 3	—	tSCK / 2 + 3	ns	—	—
tSU	Data setup time (inputs) [6]	8	—	—	ns	When operating at 3.3 V I/O supply, this parameter value is 9 ns.	—
tHI	Data hold time (inputs) [6]	0	—	—	ns	—	—
tV	Data valid (after SCK edge)	—	—	2.5	ns	—	—

Table continues on the next page...

Table 99. LPSPI Controller mode AC timing specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHO	Data hold time (outputs)	-2.5	—	—	ns	—	—
tRI/FI	Rise/Fall time input	—	—	3	ns	—	—
tRO/FO	Rise/Fall time output	—	—	3	ns	—	—

[1] Input timing assumes an input signal slew rate of 3 ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
[3] The clock driver in the LPSPI module for fperiph must guaranteed this limit is not exceeded.
[4] In controller loopback mode when LPSPI_CFGR1[SAMPLE] bit is 1.
[5] tperiph = 1000 / fperiph
[6] If LPSPI_CFGR1[SAMPLE] bit is 1, the data setup time (inputs) / data hold time (inputs) specifications are same with the one in Peripheral mode.



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

38

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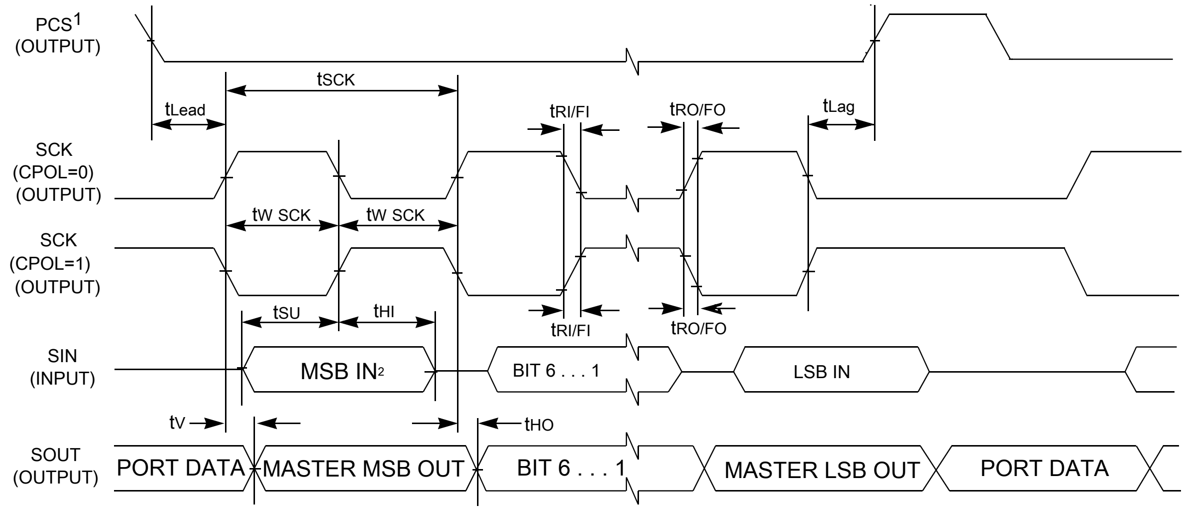
Figure 42. LPSPI Controller mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

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Figure 43. LPSPI Controller mode timing (CPHA = 1)

4.14.3 LPSPI Peripheral mode AC timing specifications

Table 100. LPSPI Peripheral mode AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	Frequency of LPSPI clock root [1][2]	—	—	30	MHz	—	—
tSCK	SCK period [3]	2 x tperiph	—	—	ns	—	—
tLead	Enable lead time	1	—	—	tperiph	—	—
tLag	Enable lag time	1	—	—	tperiph	—	—
tWSCK	Clock (SCK) high or low time	tSCK / 2 - 5	—	tSCK / 2 + 5	ns	—	—
tSU	Data setup time (inputs)	3	—	—	ns	—	—
tHI	Data hold time (inputs)	3	—	—	ns	—	—
ta	Peripheral access time [4]	—	—	20	ns	—	—
tdis	Peripheral MISO disable time [5]	—	—	20	ns	—	—
tV	Data valid (after SCK edge)	—	—	8	ns	When operating at 3.3 V I/O supply, this parameter value is 9 ns.	—
tHO	Data hold time (outputs)	0	—	—	ns	—	—

[1] Input timing assumes an input signal slew rate of 3 ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
[3] tperiph = 1000 / fperiph
[4] Time to data active from high-impedance state
[5] Hold time to high-impedance state

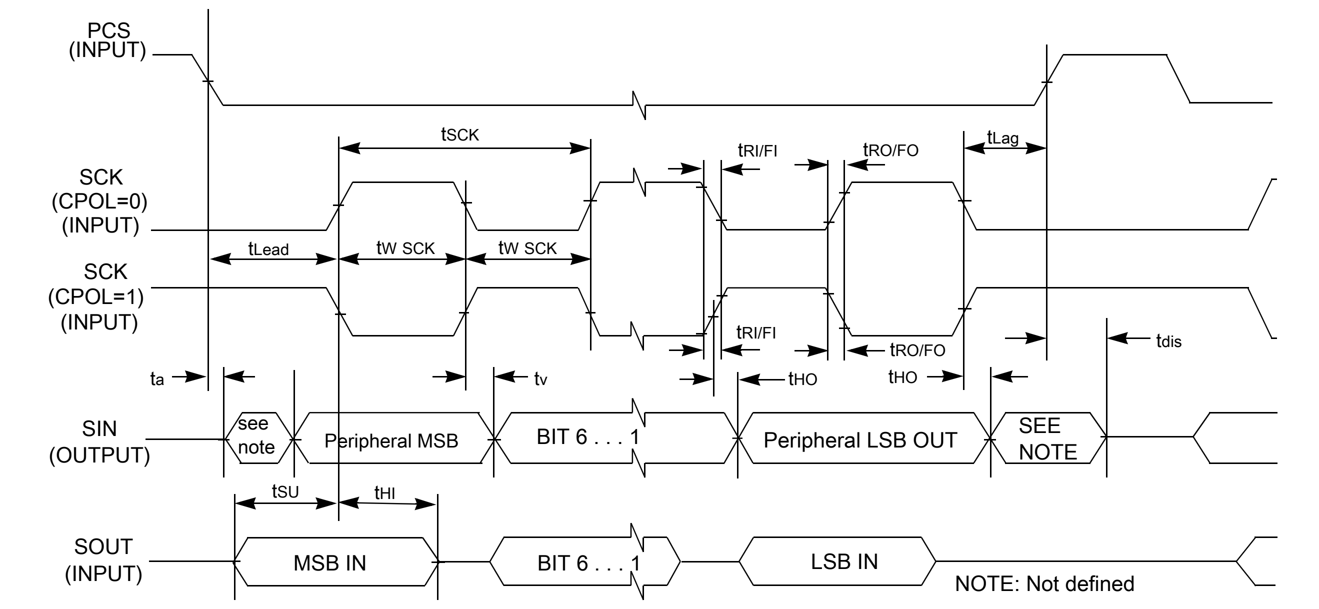

Figure 44. LPSPI Peripheral mode timing (CPHA = 0)

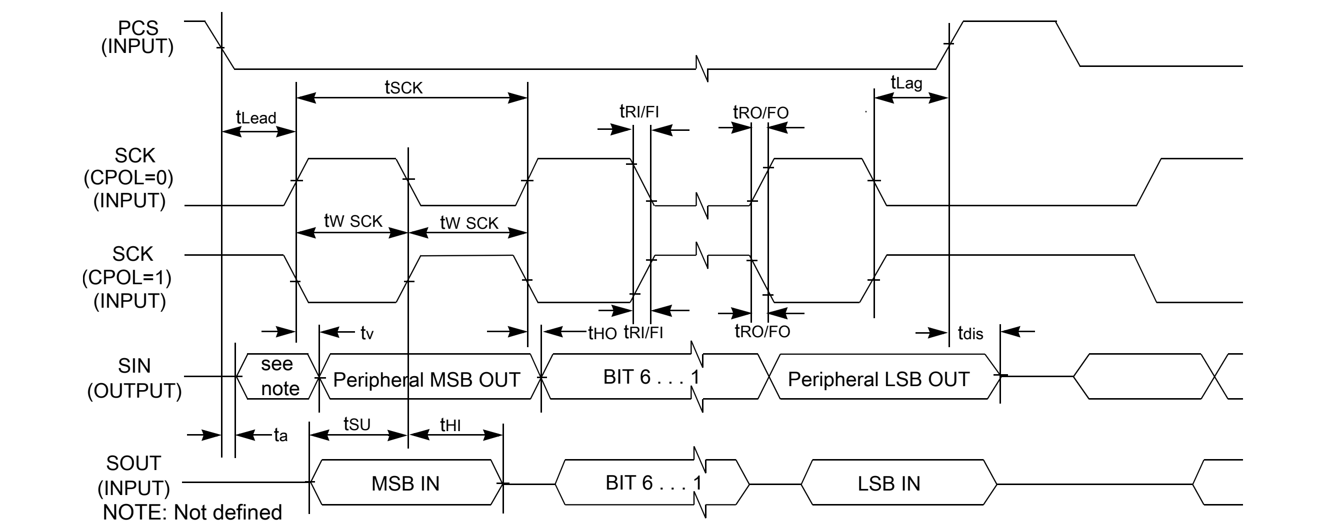

Figure 45. LPSPI Peripheral mode timing (CPHA = 1)

4.15 LPI2C timing parameters

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target.

Table 101. LPI2C timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIH_SC	Input Start condition hold time	2	—	—	MODULE_CLK cycle	—	—

Table continues on the next page...

Table 101. LPI2C timing parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCL	Input Clock low time	8	—	—	MODULE_CLK cycle	—	—
tIH	Input Data hold time	0	—	—	ns	SDA transitions after SCL falling edge	—
tCH	Input Clock high time	4	—	—	MODULE_CLK cycle	—	—
tISU	Input Data setup time (standard mode)	250	—	—	ns	SDA transitions before SCL rising edge	—
tISU_F	Input Data setup time (fast mode)	100	—	—	ns	SDA transitions before SCL rising edge	—
tISU_RSC	Input Start condition setup time (repeated start condition)	2	—	—	MODULE_CLK cycle	—	—
tISU_SC	Input Start condition setup time	2	—	—	MODULE_CLK cycle	—	—
tOH_SC	Output Start condition hold time	6	—	—	MODULE_CLK cycle	—	—
tCL	Output Clock low time	10	—	—	MODULE_CLK cycle	—	—
tRISE	SDA/SCL rise time	—	—	100	ns	SRE[2:0] = 110	—
tOH	Output Data hold time	7	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
tFALL	SDA/SCL fall time	—	—	100	ns	SRE[2:0] = 110	—
tCH	Output Clock high time	10	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
tOSU	Output Data setup time	2	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
tOSU_RSC	Output repeated start condition setup time	20	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—

Table continues on the next page...

Table 101. LPI2C timing parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOSU_SC	Output start condition setup time	11	—	—	MODULE_CLK cycle	SRE[2:0] = 110	—
fSCL	SCL clock frequency: Standard mode (Sm) [1][2]	0	—	100	kHz	—	—
fSCL	SCL clock frequency: Fast mode (Fm) [1][2]	0	—	400	kHz	—	—
fSCL	SCL clock frequency: Fast mode Plus (Fm++) [1][2]	0	—	1000	kHz	—	—
fSCL	SCL clock frequency: High speed mode (Hs-mode) [1][2]	0	—	3400	kHz	—	—
fSCL	SCL clock frequency: Ultra Fast mode (Ufm) [1][2]	0	—	5000	kHz	—	—

[1] For more details, see UM10204 I2C-bus specification and user manual.
[2] Standard, Fast, Fast+, and Ultra Fast modes are supported; High speed mode (HS) in target mode.

4.16 CAN network AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has two CAN modules available. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Please see General purpose I/O (GPIO) AC parameters for timing parameters.

Table 102. CAN-FD electrical specifications

Parameters	FlexCAN (Classical and FD)	Unit
Minimum operating frequency	20/40	MHz
Maximum Baud Rate	8/8	Mbps
TXD Rise time wcs	4/4	ns
TXD Fall time wcs	4/4	ns
RXD Rise time wcs	4/4	ns

Table continues on the next page...

Table 102. CAN-FD electrical specifications*...continued*

Parameters	FlexCAN (Classical and FD)	Unit
RXD Fall time wcs	4/4	ns
TXD	3.3/3.3	V
RXD	3.3/3.3	V
Internal delay wcs	100/50	ns
TX PAD delay wcs	25/25	ns
RX PAD delay wcs	10/10	ns
TX routing delay wcs	5/5	ns
RX routing delay wcs	5/5	ns
Transceiver loop delay wcs	250/250	ns
Total loop delay	395/345	ns

4.17 Pulse Width (PWM) timing parameters

This section describes the output timing parameters of the TPM.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

The following table lists the PWM timing parameters.

Table 103. Pulse Width (PWM) timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	PWM Module Clock Frequency	0	—	83.3	MHz	—	—
P1	PWM output pulse width high	12	—	—	ns	—	—
P2	PWM output pulse width low	12	—	—	ns	—	—

The following figure depicts the timing of the PWM.

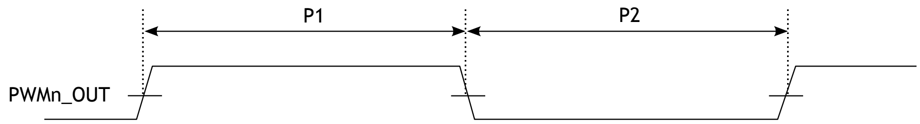

Figure 46. TPM timing

4.18 FlexSPI timing parameters

The FlexSPI interface can work in SDR or DDR modes. FlexSPI*n*_MCR0[RXCLKSRC] = 0 and FlexSPI*n*_MCR0[RXCLKSRC] = 1 configurations are supported when I/O is supplied by 3.3 V and 1.8 V, while FlexSPI*n*_MCR0[RXCLKSRC] = 3 configuration is supported when I/O is supplied by 1.8 Vonly.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. CLock transition measured at mid-supply.

Input timing assumes an input signal slew rate of 1 ns (20%/80%) and Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, un-terminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.18.1 FlexSPI PADs grouping

See Table 124 for SPI1_* PAD muxing.

See Table 104 for SD1/SD3_* PAD muxing.

Table 104. SD1/SD3_* PAD muxing

Signal name	Pad name
FlexSPIA_SS1_B	SD1_DATA3
FlexSPIA_DATA4	SD1_DATA4
FlexSPIA_DATA5	SD1_DATA5
FlexSPIA_DATA6	SD1_DATA6
FlexSPIA_DATA7	SD1_DATA7
FlexSPIA_DQS	SD1_STROBE
FlexSPIA_SCLK	SD3_CLK
FlexSPIA_SS0_B	SD3_CMD
FlexSPIA_DATA0	SD3_DATA0

Table continues on the next page...

Table 104. SD1/SD3_* PAD muxing...*continued*

Signal name	Pad name
FlexSPIA_DATA1	SD3_DATA1
FlexSPIA_DATA2	SD3_DATA2
FlexSPIA_DATA3	SD3_DATA3

4.18.2 FlexSPI DC electrical characteristics

Table 105. FlexSPI DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage	0.7 x NVCC_xxx	—	—	V	The min VIL and max VIH values are based on the respective min and max OVIN values found in Recommended Operating Conditions.	—
VIL	Input low voltage	—	—	0.3 x NVCC_xxx	V	The min VIL and max VIH values are based on the respective min and max OVIN values found in Recommended Operating Conditions.	—
VOH	Output low voltage (IOH = 100 µA)	0.85 x NVCC_xxx	—	—	V	—	—
VOL	Output high voltage (IOH = -100 µA)	—	—	0.15 x NVCC_xxx	V	—	—
IIN	Input current	—	—	±50	µA	(0V ≤ VIN ≤ OVDD) The symbol OVIN represents the input voltage of the supply referenced in Recommended Operating Conditions	—

4.18.3 FlexSPI input/read timing

There are four sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)

- Dummy read strobe generated by FlexSPI controller and looped back through the SCK pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x2)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

4.18.3.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC]

4.18.3.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Figure 47 depicts the FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2.

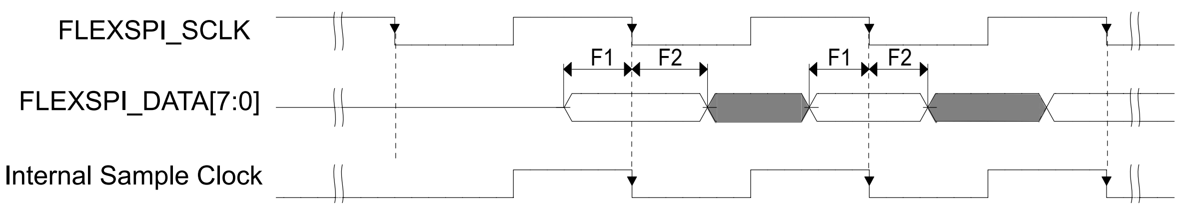

Figure 47. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X0, 0X1, 0x2

Note:

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.18.3.1.2 FlexSPI input timing in SDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Table 106. FlexSPI input timing in SDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation [1]	—	—	66	MHz	Nominal and Overdrive mode	—
F1	Setup time for incoming data	6	—	—	ns	Nominal and Overdrive mode	—
F2	Hold time for incoming data	0	—	—	ns	Nominal and Overdrive mode	—
—	Frequency of operation	—	—	50	MHz	Low drive mode	—
F1	Setup time for incoming data	7	—	—	ns	Low drive mode	—
F2	Hold time for incoming data	0	—	—	ns	Low drive mode	—

[1] The maximum frequency supported is 50 MHz when NVCC_xxx operating at 3.3 V.

4.18.3.1.3 FlexSPI input timing in SDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Table 107. FlexSPI input timing in SDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation [1]	—	—	166	MHz	Nominal and Overdrive mode	—
F1	Setup time for incoming data	1.2	—	—	ns	Nominal and Overdrive mode	—
F2	Hold time for incoming data	1	—	—	ns	Nominal and Overdrive mode	—
—	Frequency of operation [1]	—	—	100	MHz	Low drive mode	—
F1	Setup time for incoming data	2	—	—	ns	Low drive mode	—
F2	Hold time for incoming data	1	—	—	ns	Low drive mode	—

[1] The maximum frequency supported is 50 MHz when NVCC_xxx operating at 3.3 V.

4.18.3.2 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC]

4.18.3.2.1 FlexSPI input timing in DDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Table 108. FlexSPI input timing in DDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation	—	—	33	MHz	Nominal, Overdrive, and Low drive mode	—
F1	Setup time for incoming data	6	—	—	ns	Nominal, Overdrive, and Low drive mode	—
F2	Hold time for incoming data	0	—	—	ns	Nominal, Overdrive, and Low drive mode	—

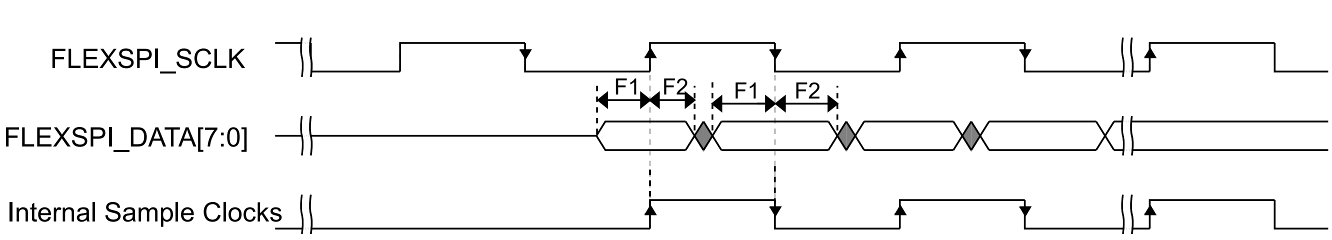

Figure 48. FlexSPI input timing in DDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

4.18.3.2.2 FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Table 109. FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation [1]	—	—	83	MHz	Nominal and Overdrive mode	—
F1	Setup time for incoming data	1.2	—	—	ns	Nominal and Overdrive mode	—
F2	Hold time for incoming data	1	—	—	ns	Nominal and Overdrive mode	—
—	Frequency of operation [1]	—	—	66	MHz	Low drive mode	—
F1	Setup time for incoming data	1.7	—	—	ns	Low drive mode	—
F2	Hold time for incoming data	1	—	—	ns	Low drive mode	—

[1] The maximum frequency supported is 50 MHz when NVCC_xxx operating at 3.3 V.

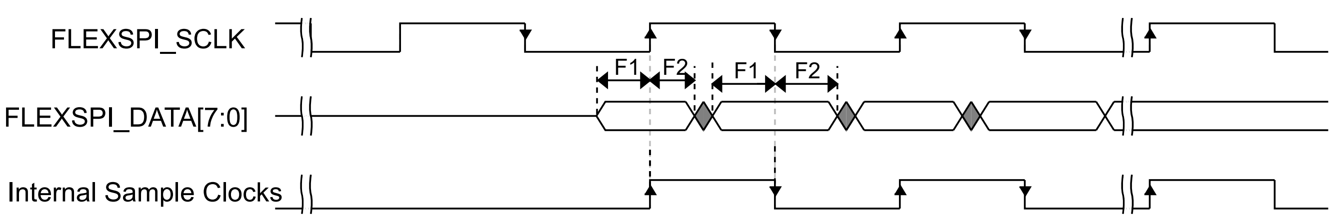

Figure 49. FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

4.18.3.2.3 FlexSPI input timing in DDR mode with RXCLKSRC = 0x3 in FlexSPIn_MCR0 register

Table 110. FlexSPI input timing in DDR mode with RXCLKSRC = 0x3 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation [1]	—	—	200	MHz	Nominal and Overdrive mode	—
tIH_DQS	Input hold time (w.r.t DQS) [1]	1.725	—	—	ns	Nominal and Overdrive mode	—
tISU_DQS	Input setup time (w.r.t DQS) [1]	-0.525	—	—	ns	Nominal and Overdrive mode	—
—	Frequency of operation	—	—	133	MHz	Low drive mode	—

Table continues on the next page...

Table 110. FlexSPI input timing in DDR mode with RXCLKSRC = 0x3 in FlexSPIn_MCR0 register*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIH_DQS	Setup time for incoming data	2.65	—	—	ns	Low drive mode	—
tISU_DQS	Hold time for incoming data	-0.75	—	—	ns	Low drive mode	—

[1] These timing specifications are valid only for 1.8 V nominal I/O pad supply voltage. For 3.3 V I/O supply, see the FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (Low drive mode).

The maximum frequency supported is 50 MHz when NVCC_xxx operating at 3.3 V.

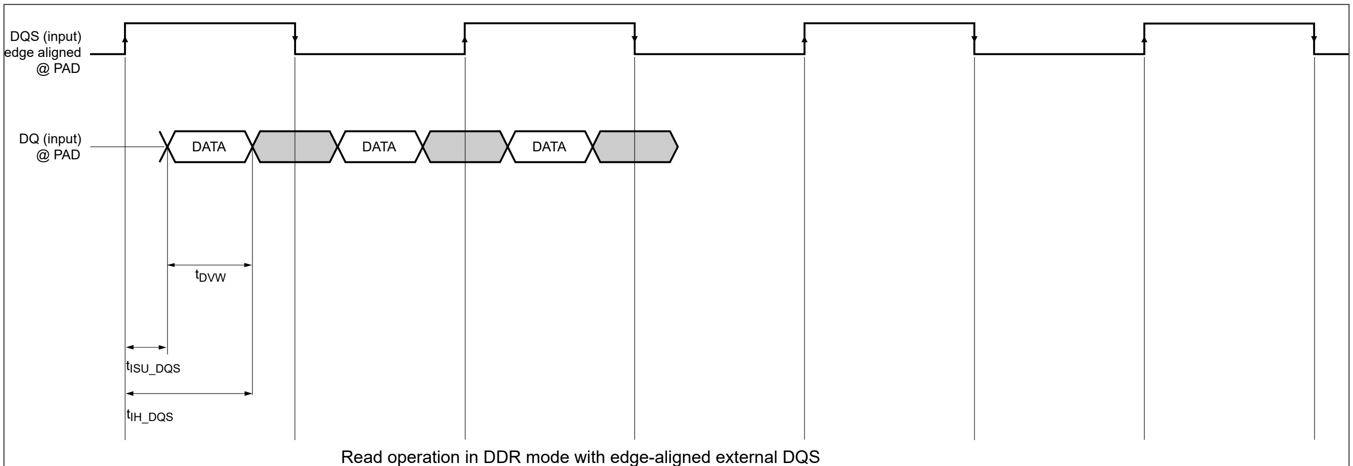

Figure 50. FlexSPI input timing in DDR mode where RXCLKSRC = 0x3 in FlexSPIn_MCR0 register

4.18.4 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.18.4.1 FlexSPI output timing in SDR mode

Table 111. FlexSPI output timing in SDR mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation [1][2][3]	—	—	200	MHz	Nominal and Overdrive mode	—
Tck	SCK clock period [1]	5	—	—	ns	Nominal and Overdrive mode	—
TDVO	Output data valid time [1]	—	—	0.6	ns	Nominal and Overdrive mode	—
TDHO	Output data hold time [1]	-0.6	—	—	ns	Nominal and Overdrive mode	—

Table continues on the next page...

Table 111. FlexSPI output timing in SDR mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TCSS	Chip select output setup time [1]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Nominal and Overdrive mode	—
TCSH	Chip select output hold time [1]	(TCSH x Tck) - 0.6	—	—	SCLK	Nominal and Overdrive mode	—
—	Frequency of operation [3]	—	—	133	MHz	Low drive mode	—
Tck	SCK clock period	7.5	—	—	ns	Low drive mode	—
TDVO	Output data valid time	—	—	2	ns	Low drive mode	—
TDHO	Output data hold time	-2	—	—	ns	Low drive mode	—
TCSS	Chip select output setup time [4]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Low drive mode	—
TCSH	Chip select output hold time [4]	(TCSH x Tck) -2	—	—	SCLK	Low drive mode	—

[1] These timing specifications are valid only for 1.8 V nominal I/O pad supply voltage. For 3.3 V I/O supply, see the FlexSPI SDR output timing in SDR mode (Low drive mode).
[2] The actual maximum frequency supported is limited by the FlexSPIn _MCR0[RXCLKSRC] configuration used, see the FlexSPI SDR input timing specifications.
[3] The maximum frequency supported is 50 MHz when NVCC_xxx operating at 3.3 V.
[4] TCSS and TCSH are configured by the FlexSPI n _FLSHAxCR1 register. See i.MX 95 Applications Processor Reference Manual (IMX95RM) for more details.

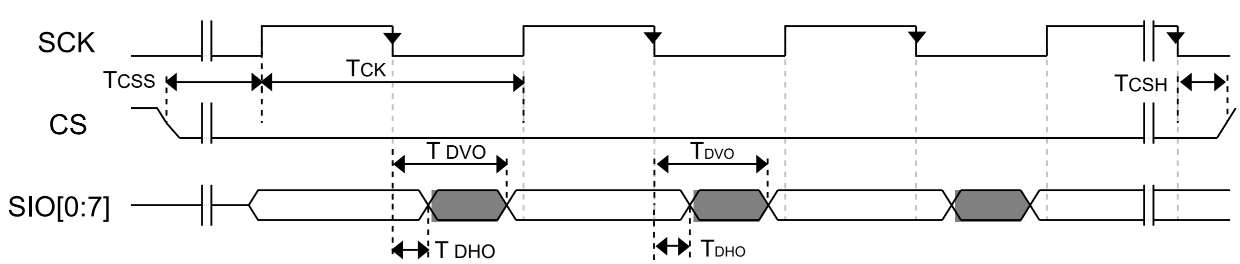

Figure 51. FlexSPI output timing in SDR mode

4.18.4.2 FlexSPI output timing in DDR mode

Table 112. FlexSPI output timing in DDR mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Frequency of operation [1][2][3]	—	—	200	MHz	Nominal and Overdrive mode	—

Table continues on the next page...

Table 112. FlexSPI output timing in DDR mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tck	SCK clock period [1]	5	—	—	ns	Nominal and Overdrive mode	—
TDVO	Output data valid time [1]	—	—	1.815	ns	Nominal and Overdrive mode	—
TDHO	Output data hold time [1]	0.615	—	—	ns	Nominal and Overdrive mode	—
TCSS	Chip select output setup time [1][4]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Nominal and Overdrive mode	—
TCSH	Chip select output hold time [1][4]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Nominal and Overdrive mode	—
—	Frequency of operation [2][3]	—	—	133	MHz	Low drive mode	—
Tck	SCK clock period	7.5	—	—	ns	Low drive mode	—
TDVO	Output data valid time	—	—	2.75	ns	Low drive mode	—
TDHO	Output data hold time	0.9	—	—	ns	Low drive mode	—
TCSS	Chip select output setup time [4]	(TCSS + 0.5) x Tck - 0.9	—	—	SCLK	Low drive mode	—
TCSH	Chip select output hold time [4]	(TCSS + 0.5) x Tck - 0.9	—	—	SCLK	Low drive mode	—

[1] These timing specifications are valid only for 1.8 V nominal IO pad supply voltage. For 3.3 V I/O supply, see Table. FlexSPI output timing in DDR mode (Low drive mode).
[2] The actual maximum frequency supported is limited by the FlexSPIn_MCR0[RXCLKSRC] configuration used, see the FlexSPI DDR input timing specifications.
[3] The maximum frequency supported is 50 MHz when NVCC_xxx operating at 3.3 V.
[4] TCSS and TCSH are configured by the FlexSPIn_FLSHAxCR1 register. See i.MX 95 Applications Processor Reference Manual (IMX95RM) for more details.

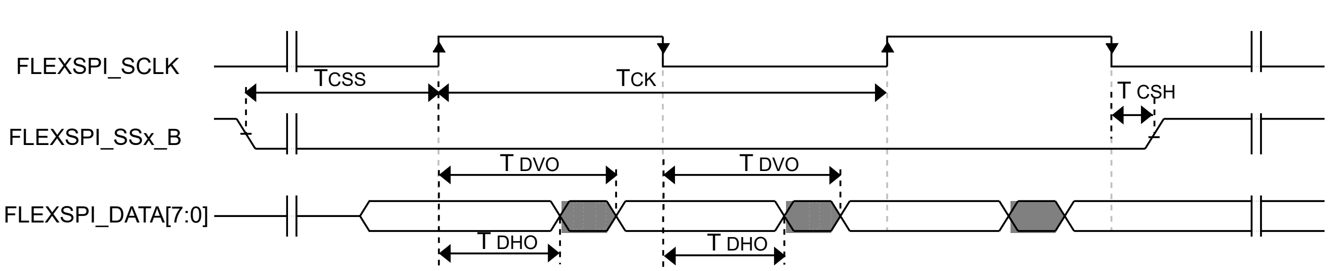

Figure 52. FlexSPI output timing in DDR mode

4.19 FlexSPI_FLR Specifications

Tested on samples basis and specified through design and characterization data. TA = 25 ℃, VCC = 3.0 V.

4-byte address alignment for Quad Read: read address start from A1, A 0 = 0,0

For details about FlexSPI Follower specifications, please refer to https://www.winbond.com.

4.20 LPUART I/O configuration and timing parameters

Please refer to General purpose I/O (GPIO) AC parameters.

4.21 Flexible I/O controller (FLEXIO) specifications

4.21.1 Flexible I/O controller (FlexIO) DC electrical characteristics

Table 113. Flexible I/O controller (FlexIO) DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high voltage [1] [2]	0.7 x NVCC_xxx	—	—	V	—	—
VIL	Input low voltage [1] [2]	—	—	0.3 x NVCC_xxx	V	—	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	μA	—	—
VOH	Output high voltage (IOH = -2mA at NVCC_xxx min)	NVCC_xxx - 0.45	—	—	V	—	—
VOL	Output high voltage (IOL = 2mA at NVCC_xxx min)	—	—	0.45	V	—	—

[1] For recommended operating conditions, see Recommended Operating Conditions.
[2] The min VIL and max VIH values are based on the respective min and max VDD values found in Recommended Operating Conditions.

4.21.2 Flexible I/O controller (FlexIO) AC timing characteristics

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

The following table shows FlexIO timing specifications.

Table 114. Flexible I/O controller (FlexIO) AC timing characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tODS	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle [1]	0	—	12	ns	—	—
tIDS	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle [1]	0	—	12	ns	—	—

[1] Assume pinx muxed on same VDD_IO domain with the load

4.22 USB PHY parameters

Implemented PHYs are compatible with following standards.

- *Universal Serial Bus Revision 3.0 Specification (including ECNs and errata)*
- *Universal Serial Bus Revision 2.0 Specification (including ECNs and errata)*

4.22.1 USB2.0 specifications

4.22.1.1 USB 2.0 DC electrical characteristics

Table 115. USB 2.0 DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH	Output High voltage	2.8	—	—	V	VDD ≥3.0 V	—
VOL	Output Low voltage	—	—	0.8	V	VDD ≥3.0 V	—
VCRS	Output Crossover Point	1.3	—	2	V	—	—
ZDRV	Output impedance	28	36	44	Ω	Driving High	—
ZDRV	Output impedance	28	36	44	Ω	Driving Low	—
RPU	Pull-up resistance	1.425	1.5	1.575	kΩ	Full speed (D + Pull-up)	—
TR	Output Rise time	4	—	20	ns	Full speed	—
TF	Output Fall time	4	—	20	ns	Full speed	—
VDI	Differential Input Sensitivity	0.2	—	—	V	| (D+) - (D-) |	—

Table continues on the next page...

Table 115. USB 2.0 DC electrical characteristics*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VCM	Differential Input Common mode range	0.8	—	2.5	V	—	—
IL	Input leakage current	—	< 1.0	—	µA	Pullups Disabled	—

4.22.1.2 USB 2.0 AC timing specifications

Table 116. USB 2.0 AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FREF_OFFSET	Reference clock frequency offset	-300	—	300	ppm	—	—
JRMSREF_CLK	Reference clock random jitter (RMS) [1][2]	—	—	3	ps	—	—
DJREF_CLK	Reference clock cycle-to-cycle jitter [3]	—	—	150	ps	—	—
tKHK/tSYSCLK	Reference clock duty cycle	40	—	60	%	—	—
fSYSCLK	Reference clock frequency	—	24	—	MHz	—	—

[1] 1.5 MHz to Nyquist frequency. For example, 100 MHz reference clock, the Nyquist frequency is 50 MHz.
[2] The peak-to-peak Rj specification is calculated at 14.069 times the RJRMS for 10 - 12 BER.
[3] DJ across all frequencies.

4.22.2 USB 3.0 spcifications

4.22.2.1 USB 3.0 DC electrical characteristics

Table 117. USB 3.0 DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vtx-diff-pp	Differential output voltage [1]	800.0	1000.0	1200.0	mVp-p	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
Vtx-diff-pp-low	Low power differential output voltage [1]	400.0	—	1200.0	mVp-p	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
Vtx-de_ratio	Transmit de-emphasis [1]	3.0	—	4.0	dB	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
ZdiffTX	Differential impedance [1]	72.0	100.0	120.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—

Table continues on the next page...

Table 117. USB 3.0 DC electrical characteristics*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RTX-DC	Transmit common mode impedance [1]	18.0	—	30.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
TTX-CM-DCACTIVEIDLEDELTA	Absolute DC common mode voltage bteween U1 and U0 [1]	—	—	200.0	mV	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
VTX-IDLEDIFF-DC	DC electrical idle differential output voltage [1]	0	0	10.0	mV	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
RRX-DIFF-DC	Differential receiver input impedance [1]	72.0	100.0	120.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
RRX-DC	Receiver DC common mode impedance [1]	18.0	—	30.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
ZRX-HIGHIMP-dc	DC input CM input impedance for V > 0 during reset or power down [1][2][3]	25000.0	—	—	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—
VTRXIDLE-IDLE-DET-DIFFpp	LPFS detect threshold [1]	100.0	—	300.0	mV	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V	—

[1] For operating conditions, see Recommended Operating Conditions.
[2] Below the minimum is noise. Must wake up above the maximum.
[3] Each USBx_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor.

4.22.2.2 USB 3.0 AC timing specifications

Table 118. USB 3.0 AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fUSB	Speed	—	5.0	—	Gb/s	—	—
TTX-EYE	Transmitter eye [1]	0.625	—	—	UI	—	—
UI_TX	Unit interval (Transmitter) [2]	199.94	200.0	200.06	ps	—	—
UI_RX	Unit interval (Receiver) [2]	199.94	200.0	200.06	ps	—	—
tPeriod	Period (LFPS) [3]	20.0	—	100.0	ns	—	—
Vtx-diff-pp-lfps	Peak-to-peak differential amplitude (LFPS) [3]	800.0	—	1200.0	mV	—	—
trise/fall	Rise and fall time (LFPS) [3]	—	—	4.0	ns	—	—
DC LFPS	Duty cycle (LFPS) [3]	40.0	—	60.0	%	—	—

[1] To be measured at Silicon pad
[2] UI does not account for SSC-caused variations.
[3] Measured at compliance TP1. See the Figure. Transmit normative setup for details. Our SoCs guarantee these spec unless the board is designed properly

4.22.3 Pad/Package/Board connections

The USBx_VBUS pin cannot directly connect to the 5 V VBUS voltage on the USB2.0 link.

Each USBx_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor from 5V VBUS or an external 1KΩ resistor from 3.3V.

The USB 2.0 PHY uses USBx_TXRTUNE and an external resistor to calibrate the USBx_DP/DN 45 Ω source impedance. The external resistor value is 200 Ω 1% precision on each of USBx_TXRTUNE pad to ground.

4.23 PCIe 3.0 PHY parameters

The PCIe interface is designed to be compatible with PCIe specification Gen3 x1 lane and supports the *PCIe Base Specification Rev 3.0 Version 1.0, Section 4.3*.

4.23.1 PCIe

PCIe Electricals are compatible with the PCIe Base Specification Rev 3.0 Version 1.0, Section 4.3

Table 119. PCIe

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval [1]	399.88	—	400.12	ps	2.5GT/s	—
UI	Unit Interval [1]	199.94	—	200.06	ps	5GT/s	—
UI	Unit Interval [1]	124.9625	—	125.0375	ps	8GT/s	—
CTX	AC Coupling Capacitor [2]	75	—	265	nF	2.5GT/s, 5GT/s	—
CTX	AC Coupling Capacitor [2]	176	—	265	nF	8GT/s	—
REXT	External Reference Resistor (RESREF)	—	200	—	Ohms	—	—

[1] The specified UI is equivalent to a tolerance of +/- 300ppm for each Reference Clock Source. Period does not account for SSC induced variations.
[2] All platforms that have transmitters supporting 8.0 GT/s must implement the 176 nf to 265 nF CTX value. Platforms operating at 2.5 or 5.0 GT/s only may increase that range to 75 nf to 265 nF.

REXT requires 1% 100ppm/C precision resistor-to-ground on PC Board

The specified UI is equivalent to a tolerance of +/- 300ppm for each Reference Clock Source. Period does not account for SSC induced variations. This parameter is measured by Validation as part of Transmitter AC Specifications. It is listed here in overview section as min/max also define reference clock allowed ppm offset.

All platforms that have transmitters supporting 8.0 GT/s must implement the 176 nf to 265 nF CTX value. Platforms operating at 2.5 or 5.0 GT/s only may increase that range to 75 nf to 265 nF.

4.23.2 PCIE Transmitter DC Specifications

Table 120. PCIE Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VTX-DIFF-PP	Differential p-p Tx voltage swing	800	—	1200	mVPP	2.5GT/s, 5GT/s	—
VTX-FS-NO-EQ	Full swing TX Voltage with no TX EQ	800	—	1300	mVPP	8GT/s	—
VTX-DIFF-PP-LOW	Low power differential p-p Tx voltage swing	400	—	1200	mVPP	2.5GT/s, 5GT/s	—
VTX-RS-NO-EQ	Reduced swing TX voltage with no TX eQ	—	—	1300	mVPP	8GT/s	—

4.23.3 PCIE Transmitter AC Specifications

Table 121. PCIE Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
BWTX-PKG-PLL-TYP	Typical TX PLL Bandwidth	—	8.85	—	MHz	2.5GT/s	—
PKGTX-PLL-TYP	Typical TX PLL Peaking	—	0.64	—	dB	2.5GT/s	—
BWTX-PKG-PLL-TYP	Typical TX PLL Bandwidth	—	9.55	—	MHz	5GT/s	—
PKGTX-PLL-TYP	Typical TX PLL Peaking	—	0.59	—	dB	5GT/s	—
BWTX-PKG-PLL-TYP	Typical TX PLL Bandwidth	—	4.30	—	MHz	8GT/s	—
PKGTX-PLL-TYP	Typical TX PLL Peaking	—	0.63	—	dB	8GT/s	—
TTX-EYE	Transmitter Eye including all jitter sources	0.75	—	—	UI	2.5GT/s, 5GT/s	—

4.23.4 PCIE Receiver DC Specifications

Table 122. PCIE Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VRX-DIFF-PP-CC	Differential peak-peak voltage for	0.175	—	1.2	V	2.5GT/s	—

Table continues on the next page...

Table 122. PCIE Receiver DC Specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	common Refclk RX architecture						
VRX-DIFF-PP-CC	Differential peak-peak voltage for common Refclk RX architecture	0.12	—	1.2	V	5GT/s	—

4.23.5 PCIE Reference Clock Output Specifications

PCIe Reference Clock Output Electricals are compatible with the PCIe Base Specification Rev 3.0 Version 1.0, Section 4.3.7

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

i.MX 95 supports three different boot modes:

- Normal Boot Mode
- Boot from Internal Fuse Mode
- Serial Download Boot Mode

Three different boot modes can be selected via different boot mode pins or overridden by fuses.

i.MX 95 has one kind of boot type:

- Low Power Boot (LPB): only M33 core is running after POR.

For detailed boot mode configuration, see the "Fusemap" and the "System Boot" chapter in i.MX 95 Reference Manual (IMX95RM).

5.1 Boot mode configuration pins

There are four boot mode pins used to select boot mode.

Table 123. Fuses and associated pins used for boot

BOOT_MODE [3:0]	Functions
X000	Boot from Internal Fueses
X001	Serial Download
X010	uSDHC1 8-bit eMMC5.1
X011	uSDHC2 4-bit SD3.0
X100	FlexSPI Serial NOR
X101	FlexSPI Serial NAND

Table continues on the next page...

Table 123. Fuses and associated pins used for boot*...continued*

BOOT_MODE [3:0]	Functions
X110	Reserved
X111	Reserved

- HW samples the boot CFG pins before ROM starts, these pins should be mapped to Boot CFG pins by default.
- Once HW samples the boot CFG pins and stores the boot CFG in CMC register, the register should be latched and reflecting the pins status.

Additional boot options are also supported for both Normal Boot Mode and Internal Fuse mode:

- All boot modes support for a range of speeds, timings, and protocol formats;
- eMMC boot can be supported from any USDHC1 only, while SD boot can be supported from any USDHC instance 1 or 2;
- Serial NOR boot supports 1-bit, 4-bit, and 8-bit mode;
- Serial NAND boot supports 1-bit, 4-bit, and 8-bit mode (8-bit Serial NAND)

BOOT_MODE pins are multiplexed over other functional pins. The functional I/O that multiplexed with these pins must be selected subject to two criteria:

- Functional I/O must not be used if they are inputs to the SoC, which could potentially be constantly driven by external components. Such functional mode driving may interfere with the need for the board to pull these pins a certain way while POR is asserted.
- Functional I/O must not be used if they are outputs of the SoC, which will be connected to components on the board that may misinterpret the signals as valid signals if they are toggled (such as, the board drives them while POR is asserted).

5.2 Boot devices interfaces allocation

i.MX 95 supports three kinds of boot devices:

- Primary Boot Device

  The Primary boot device is selected by Boot Mode fuses if boot mode is boot from Internal Fuses. Otherwise, it can be selected by Boot Mode pins. The valid primary boot device options are SD/eMMC/FlexSPI NOR/SPI NAND. The valid options also depend on the Boot Type and other fuses configuration.
- Recovery Boot Device

  After failure of booting from Primary Boot Device, i.MX 95 tries to boot from another boot source. The recovery boot device is only from SPI1 or SPI2.
- Serial Download Boot Device

  Cortex-M33 supports serial download mode via USB1 and USB2.

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 124. Boot through FlexSPI

Signal name	Pad name	Alt
FlexSPIA_DATA0	XSPI1_DATA0	ALT0

Table continues on the next page...

Table 124. Boot through FlexSPI*...continued*

Signal name	Pad name	Alt
FlexSPIA_DATA1	XSPI1_DATA1	ALT0
FlexSPIA_DATA2	XSPI1_DATA2	ALT0
FlexSPIA_DATA3	XSPI1_DATA3	ALT0
FlexSPIA_DQS	XSPI1_DQS	ALT0
FlexSPIA_SS0_B	XSPI1_SS0_B	ALT0
FlexSPIA_SS1_B	XSPI1_SS1_B	ALT0
FlexSPIA_SCLK	XSPI1_DATA0	ALT0
FlexSPIA_DATA4	XSPI1_DATA4	ALT0
FlexSPIA_DATA5	XSPI1_DATA5	ALT0
FlexSPIA_DATA6	XSPI1_DATA6	ALT0
FlexSPIA_DATA7	XSPI1_DATA7	ALT0

Table 125. Boot through uSDHC1

Signal name	PAD name	ALT
USDHC1_CMD	SD1_CMD	ALT0
USDHC1_CLK	SD1_CLK	ALT0
USDHC1_DATA0	SD1_DATA0	ALT0
USDHC1_DATA1	SD1_DATA1	ALT0
USDHC1_DATA2	SD1_DATA2	ALT0
USDHC1_DATA3	SD1_DATA3	ALT0
USDHC1_DATA4	SD1_DATA4	ALT0
USDHC1_DATA5	SD1_DATA5	ALT0
USDHC1_DATA6	SD1_DATA6	ALT0
USDHC1_DATA7	SD1_DATA7	ALT0
USDHC1_RESET	SD1_DATA5	ALT2

Table 126. Boot through uSDHC2

Signal name	PAD name	ALT
USDHC2_CMD	SD2_CMD	ALT0
USDHC2_CLK	SD2_CLK	ALT0
USDHC2_DATA0	SD2_DATA0	ALT0
USDHC2_DATA1	SD2_DATA1	ALT0
USDHC2_DATA2	SD2_DATA2	ALT0
USDHC2_DATA3	SD2_DATA3	ALT0
USDHC2_RESET	SD2_RESET_B	ALT0
USDHC2_VSELECT	SD2_VSELECT	ALT0

Table 127. Boot through SPI1

Signal name	PAD name	ALT
SPI1_PCS1	PDM_BIT_STREAM0	ALT2
SP11_SIN	SAI1_TXC	ALT2
SPI1_SOUT	SAI1_RXD0	ALT2
SPI1_SCK	SAI1_TXD0	ALT2
SPI1_PCS0	SAI1_TXFS	ALT2

Table 128. Boot through SPI2

Signal name	PAD name	ALT
SPI2_PCS1	PDM_BIT_STREAM1	ALT2
SP12_SIN	UART1_RXD	ALT2
SPI2_SOUT	UART2_RXD	ALT2
SPI2_SCK	UART2_TXD	ALT2
SPI2_PCS0	UART1_TXD	ALT2

Note: *USB1 interfaces are dedicated pins, thus no IOMUX options.*

6 Package information and functional contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 15 x 15 mm package information

This section includes the 15 x 15 mm package contact assignment information and mechanical package drawing.

6.1.1 15 x 15 mm, 0.5 mm pitch, ball matrix

Figure 53 shows the top, bottom, and side views of the 15 x 15 mm FCBGA package.

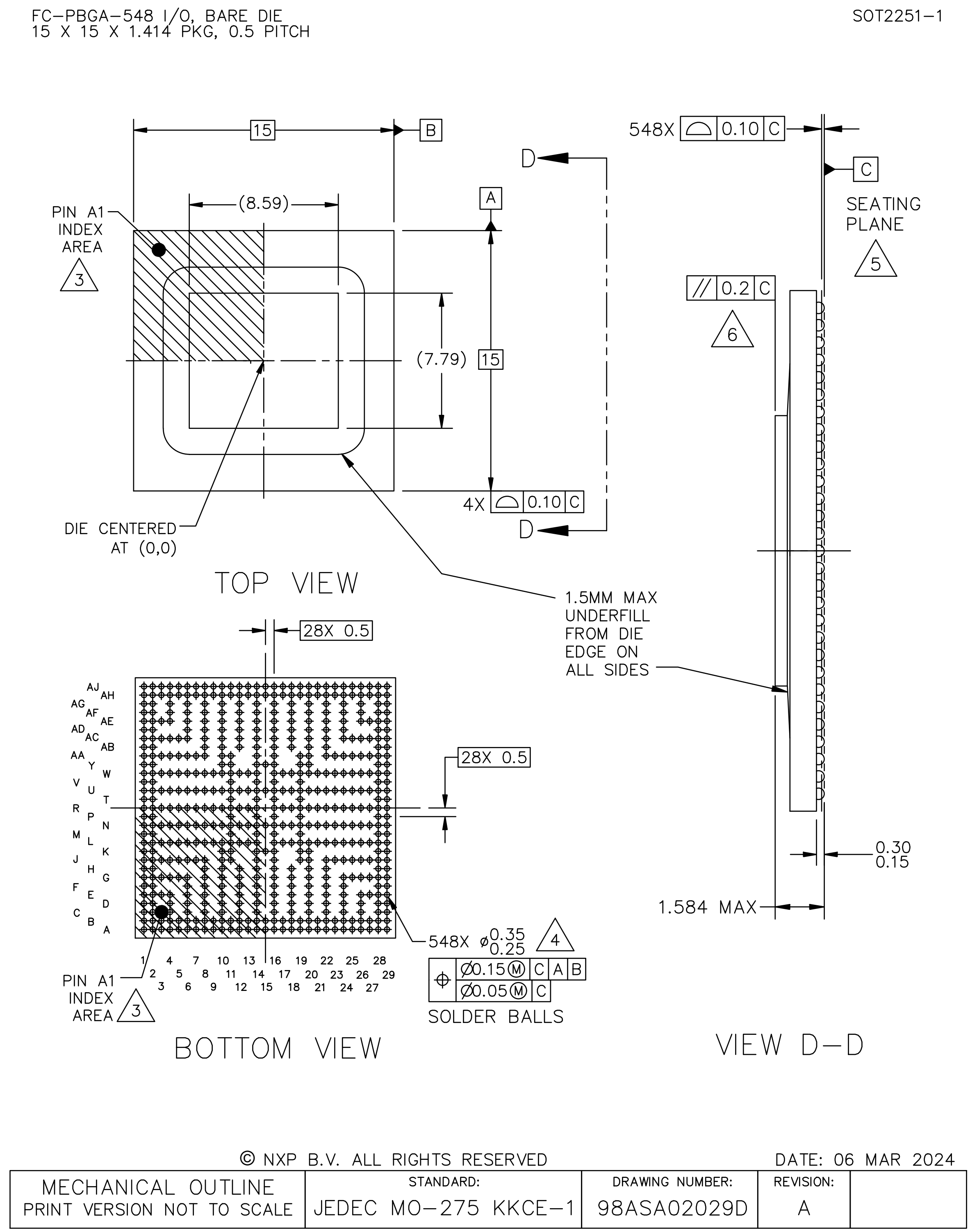

Figure 53. 15 x 15 mm FCBGA, case x package Top, Bottom, and Side Views

6.1.2 15 x 15 mm supplies contact assignments and functional contact assignments

See attached the excel file "imx95_pinmux_pinlist" for details.

6.1.3 15 x 15 mm, 0.5 mm pitch, ball map

See attached the excel file "i.mx95_15mm_ballmap" for details.

6.2 19 x 19 mm package information

This section includes the 19 x 19 mm package contact assignment information and mechanical package drawing.

6.2.1 19 x 19 mm, 0.7 mm pitch, ball matrix

Figure 54 and Figure 55 shows the top, bottom, and side views of the 19 x 19 mm FCBGA package.

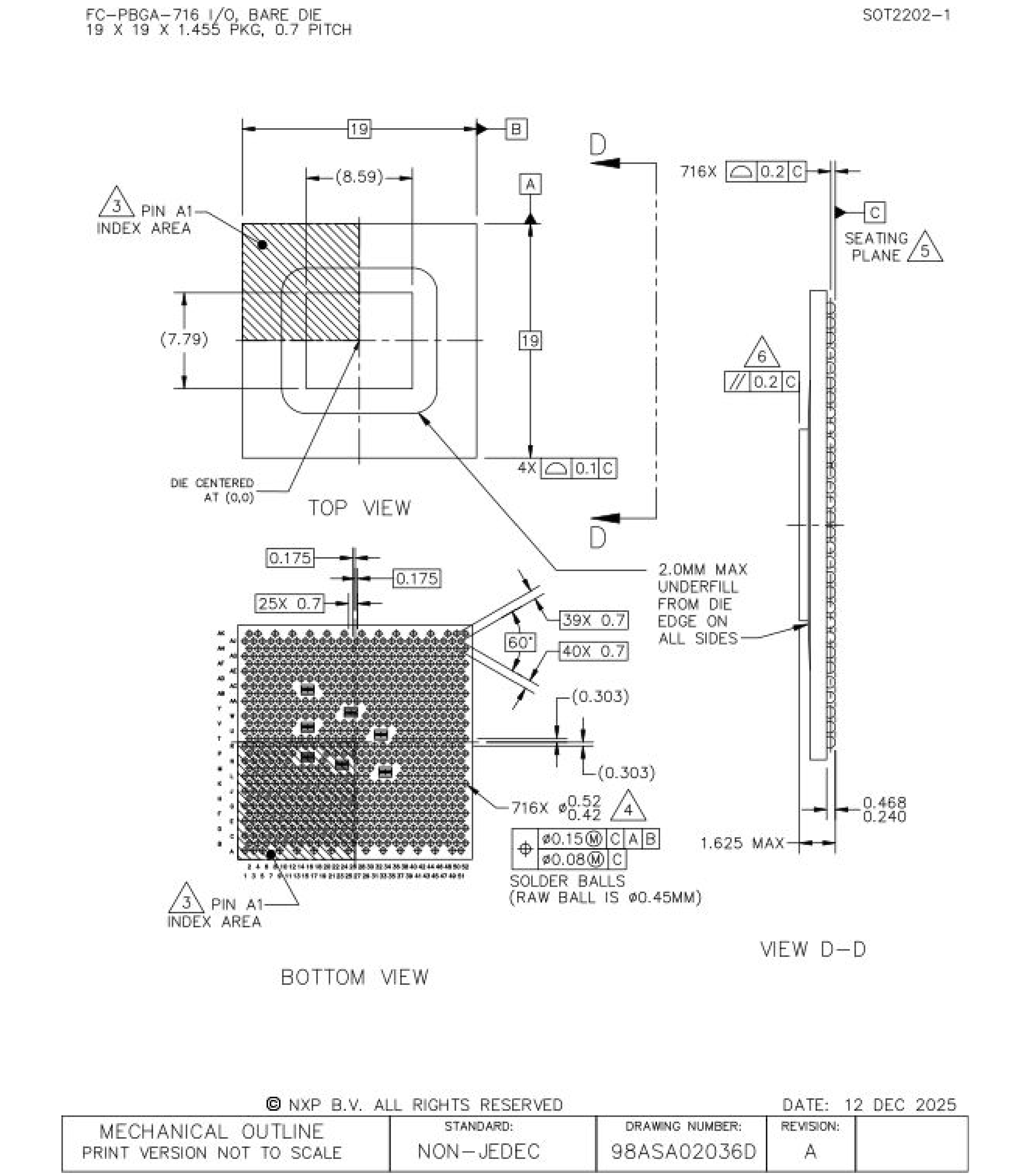

Figure 54. 19 x 19 mm FCBGA, case x package Top, Bottom, and Side Views

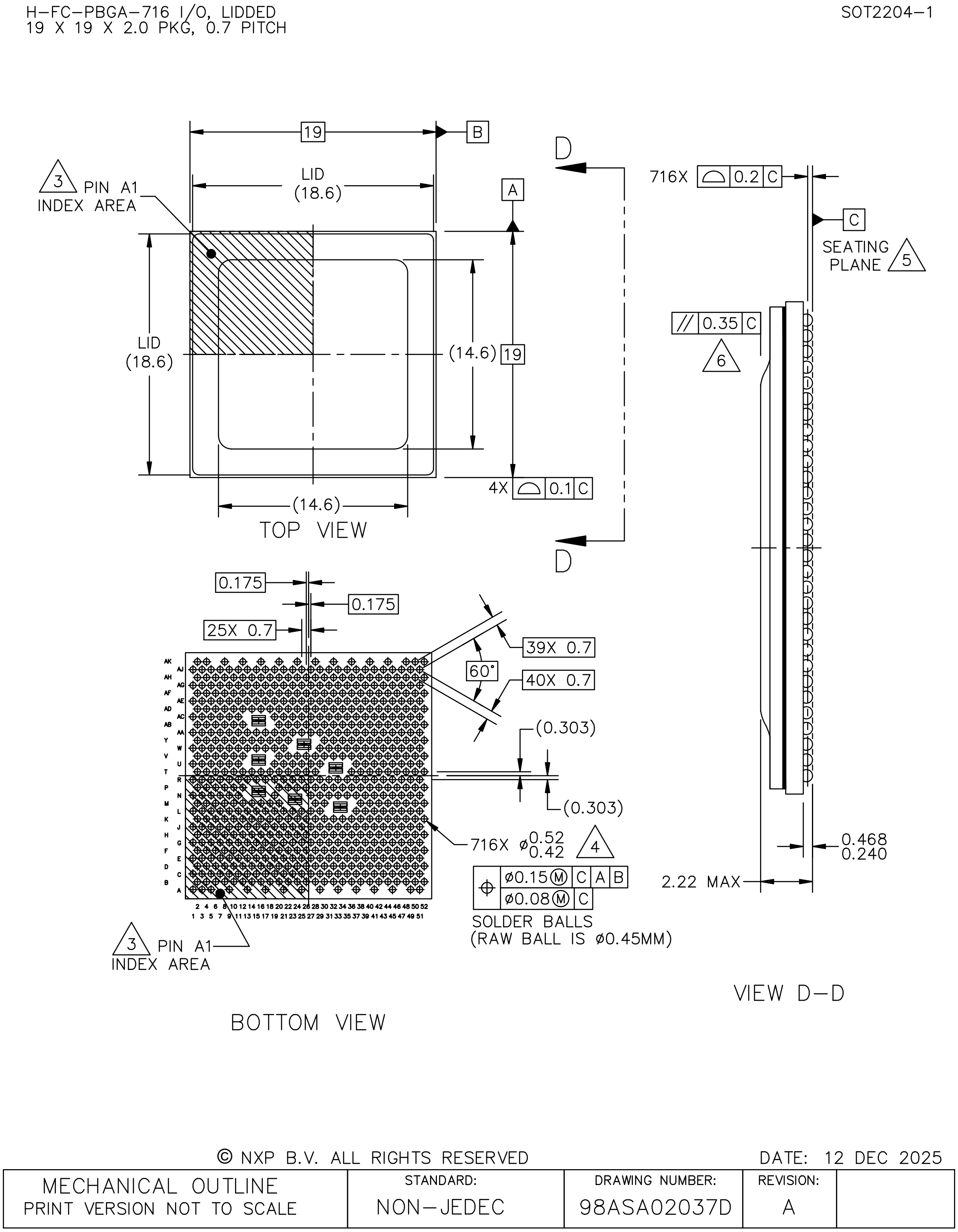

Figure 55. 19 x 19 mm FCBGA (Lidded), case x package Top, Bottom, and Side Views

6.2.2 19 x 19 mm supplies contact assignments and functional contact assignments

See attached the excel file "imx95_pinlist_ver1" for details.

6.2.3 19 x 19 mm, 0.7 mm pitch, ball map

See attached the excel file "i.mx95_19mm_ballmap" for details.

7 Revision History

Table 129 provides a revision history for this data sheet.

Table 129. Data Sheet document revision history

Document ID	Release date	Description
IMX95IEC v.8.0	7 April 2026	Product Data Sheet Initial Public Release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Contents

Date of release: 7 April 2026
Document identifier: IMX95IEC