IMXRT700EC

i.MX RT700 Crossover Microcontroller Data Sheet

Rev. 6 — 30 October 2025 Product data sheet

- This document provides electrical specifications for i.MX RT700 Crossover Microcontroller family.
- For functional characteristics and the programming model, see i.MX RT700 Crossover Microcontroller Reference Manual.

1 Introduction

The i.MX RT700 chip contains a rich set of peripherals within multiple functional chip domains. These domains include core complexes, DSPs, on-chip SRAM, and several high-bandwidth interfaces to access off-chip flash. The chip is architected to be low-power by using advanced clock and power gating techniques, Dynamic Voltage Frequency Scaling (DVFS), and independent power control of specific chip domains. The chip features many highlights, including NXP's eIQ™ Neutron NPU for accelerating machine learning models supported by the eIQ Toolkit, a vector graphics processing unit (VGPU), and a 24-bit Sigma-Delta ADC.

1.1 Features

The following table shows the chip features organized by functions.

Table 1. i.MX RT700 features

Feature	Module	Description
Arm platform and debug	CPU0	• One Compute Domain CPU - Arm Cortex-M33 processor with Trustzone and built-in: — Nested Vectored Interrupt Controller (NVIC): NVIC (CPU0) implement a relocatable vector table supporting external interrupts, a single non-maskable interrupt (NMI), and priority levels. — Non-maskable interrupt (NMI) input — Memory Protection Unit (MPU): MPUs (CPU0) provides support for eight unified protection regions, overlapping protection regions with ascending region priority, and access permissions. MPU mismatches and permission violations invoke the Hard Fault handler. — Hardware Floating Point Unit (FPU): FPU (CPU0) is single-precision floating point computation unit compliant to the IEEE Standard for Floating-Point Arithmetic (IEEE 754). — ETM Trace — System Tick Timer (SysTick): See the ARMv8M Architecture Reference Manual for more information about this system timer.
	CPU1	• One Sense Domain CPU - Arm Cortex-M33 co-processor with Trustzone and built-in: — Nested Vectored Interrupt Controller (NVIC) — Non-maskable interrupt (NMI) input — Memory Protection Unit (MPU) — Hardware Floating Point Unit (FPU) — System Tick Timer (SysTick) ***Note:*** *The configuration of CPU1 does not include ETM.*
	Performance Monitor (CMX_PERFMON)	• Four CMX_PERFMONs (System Cache, Code Cache, XSPI0,1 Cache) - contain counters that you can configure to count events, which can be used to monitor the performance of a CPU, cache, or memory. You can configure CMX_PERFMON to select the events to be counted for

Table continues on the next page...

Table 1. i.MX RT700 features*...continued*

		each counter. An additional instruction counter is available to count CPU instruction fetches.
	Cache Memory Controller (XCACHE)	• Two XCACHEs (System Cache, Code Cache) - general-purpose AMBA AHB bus protocol caches that provide lower latency access to slower memories.
	Memory Map Unit (MMU)	• Three MMUs - remap AHB bus access address to another address indicated by MMU Look Up Table (LUT) SRAM. The remapped address in LUT SRAM can be configured via the internal register bus. • MMU modules are implemented separate from XSPI.
	Semaphores2 (SEMA42)	• Three SEMA42s - memory-mapped modules that provide robust hardware support needed in multi-core systems for implementing semaphores and provide a simple mechanism to achieve "lock and unlock" operations via a single write access. The hardware semaphore modules provide hardware-enforced gates as well as other useful system functions related to the gating mechanisms.
	Messaging Unit (MU)	• Five MUs - enable two processors on a chip to communicate and coordinate by passing messages (e.g. data, status, and control) through the MU interfaces. MUs also provide the ability for one processor to signal the other processor using interrupts.
	Debug Mailbox (DBGMB)	• One DBGMB outlines the debug capabilities implemented in this chip.
Chip IO	IO PAD Controller (IOPCTL)	• Three IOPCTLs provide IO pad control functions. Each port pin PIOm_n has one IOPCTL register assigned to control the characteristics of the pin.
	Pin Interrupt and Pattern Match (PINT)	• Two PINTs provide interrupt functionality for a selected set of GPIO pins.
	General-Purpose Input/ Output (GPIO)	• Eleven GPIOs - communicate to the processor core via a zero wait-state interface for maximum pin performance. • Up to 217 general purpose I/O (GPIO) pins with configurable pull-up/ pull-down resistors, and adjustable output driver slew rates. • Ports can be set, clear, toggle in bitwise • Mirrored, secure GPIO. • Individual GPIO pins can be used as edge and level-sensitive interrupt sources, each with its own interrupt vector. • All GPIO pins can contribute to one of two ganged (OR'd) interrupts from the GPIO module. • A group of up-to 8 GPIO pins (from Port0/1) can be selected for Boolean pattern matching which can generate interrupts and/or drive a "pattern-match" output.

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Table 1. i.MX RT700 features*...continued*

Clock, power, and reset	Power Management Controller (PMC)	One PMC interfacing to CPU0 (PMC0) and CPU1 (PMC1), manages the hardware functions and connections that support the internal LDO supply and external PMIC supply interface for the VDD1, VDD2, VDDN, and VDD 1.8 V domains. Subsystem Features: • Five VDDIO supplies (can be shared or independent) • Body biasing consists of applying a voltage to the target transistors' back terminal to control their threshold voltage. — Asymmetric Forward Body Bias (AFBB) allows for higher performance while minimizing the increase in leakage current. — Reverse body bias (RBB) reduces the leakage current consumption but also performance. So, it is used only for logic that is not clocked. — Normal Body Bias (NBB) is used during active operation for powering down the SRAM reverse body bias generators.
	Clock Controller (CLKCTL)	• Five CLKCTLs (2 Sense, 2 Common, 1 Media) - contain and configure clock sources for peripherals and CPUs. • Crystal Oscillator (XTALOSC) 24 MHz source • Main System PLL: — Allows CPU maximum frequency operation without the need for a high-frequency crystal. Main System PLL may be run from an FRO, XTALOSC, or the CLKIN pin. — 4 PFD outputs provide flexible clock source to various peripherals. • Audio PLL for the audio and other modules.
	System Controller (SYSCON)	• Five SYSCONs (2 Sense, 2 Common, 1 Media) provide controls and configures the system and peripherals for the multiple functions.
	Sleep Controller (SLEEPCON)	• Two SLEEPCONs (1 Sense, 1 Common) - programmable low-power controllers to save power for applications.
	Reset Controller (RSTCTL)	• Five RSTCTLs (2 Sense, 2 Common, 1 Media) control module resets.
	FRO Clock Generator (FRO)	• Two programmable internal 150-325 MHz FROs (FRO0 and FRO2) with ±1% accuracy. • One fixed 192 MHz FRO (FRO1) with ±1% accuracy. • Optionally, a fast startup routine can be activated
	Frequency Measurement (FREQME)	• One FREQME accurately measures the frequency of an on-chip or off-chip target clock using a selectable on-chip reference clock.
	Nano Power 32 kHz Oscillator (OSC32KNP)	• One OSC32KNP - an analog interface to an external oscillator to provide a 32.768 kHz (32k) clock and includes a digital module to configure the analog interface, and monitor the 32k clock stability.

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Table 1. i.MX RT700 features*...continued*

	Real Time Clock Subsystem (RTC_SS)	• Two RTC_SSs provide wakeup timers and miscellaneous functions for RTC modules
	Real Time Clock (RTC)	• Two RTCs, RTC0 (CPU0, controller) and RTC1 (CPU1, target) • low-power module that provides time keeping and calendaring functions. RTC can also be used to provide additional security measures and compensate against variations in the 32 kHz oscillator source. • Contains an independent power supply and dedicated oscillator. • Integrated wake-up timer can be used to wake the device up from low-power modes. • The RTC resides in the Always-on voltage domain. • 32 kHz real-time clock (RTC) oscillator that can optionally be used as a system clock.
Security	EdgeLock Secure (ELS)	• One ELS - a security subsystem supporting a wide range of cryptographic algorithms and provides strong key isolation from the rest of the chip.
On-chip memory	RAM Arbiter	• The 7.5 MB of SRAM is split as 5.5 MB in the compute domain and 2 MB in the sense domain. 7.5 MB of SRAM accessible by the VDD2_COMP , DMA engines, and bus controllers.
	Misc	• Additional SRAMs - uSDHC FIFOs, GPU, Display controller, MIPI PHY, and XSPI caches, PKC, M33 caches, NPU • Up to 96 KB of cache (32 KB instruction / 64 KB data) on the HiFi 4 DSP interface to shared system RAM • 16 kbits OTP Fuses • Up to 256 KB ROM memory for factory-programmed drivers and APIs
External memories and mass storage	Ultra Secured Digital Host Controller (uSDHC)	• Two SD/eMMC memory card interfaces with dedicated DMA controllers. One interface supports eMMC 5.0 with HS400/DDR operation.
	External Serial Peripheral Interface (XSPI)	• Three XSPI (octal/quad) Flash interfaces and x16 PSRAM memories: up to 400 MHz DDR/200 MHz SDR (at least 166 MHz at 1.0 V) with 32 KB cache for 2 out of 3 XSPI interfaces, XPI2 can ran up to 250 MHz in both SDR and DDR mode. • Two of the XSPI modules (XSPI0 and XSPI1) include on-the-fly encryption/decryption for execute-in-place, address-remapping to support dual-image boot, and garbage collection capabilities. DMA supported.
	Cache Controller (CACHE64_CTRL)	• Two CACHE64_CTRLs - cache memory controllers and blocks of high-speed memory locations that contain address information (commonly known as a tag) and its associated data. CACHE64_CTRLs decrease the average time of a memory access.

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Table 1. i.MX RT700 features*...continued*

	CACHE64 Policy Select (CACHE64_POLSEL)	• Two CACHE64_POLSELs monitor incoming bus addresses to define the policy that the cache controllers (CACHE64_CTRL) use. CACHE64_POLSELs and the cache controllers work in tandem with each other.
Images, graphics, video, and ML processing	Neural Processing Unit (NPU)	• One NPU- a Neural Network (NN) processing accelerator to accelerate NN matrix computations by deploying parallel Multiply Accumulate (MAC) blocks.
	JPEG Decoder (JPEGDEC)	• One JPEGDEC - a high-performance JPEG decoder for still image and video decompression applications.
	JPEG Decoder Wrapper (JPGDECWRP)	• One JPEGDECWRP - provides the bus interface and DMA engine for JPEGDEC.
	PNG Decoder (PNGDEC)	• One PNGDEC - decodes pictures in the PNG source format.
	Vector Graphics Processing Unit (VGPU)	• One VGPU - 2.5D VGPU provides a high-performance/area UI-based graphic core to enable hardware acceleration of the OpenVG API and display vector graphics on a variety of consumer devices, running at frequencies up to 325 MHz.
Display	Mobile Industry Processor Interface and Display Serial Interface Controller (MIPI_DSI_HOST)	• One MIPI_DSI provides an interface that allows communication with MIPI_DSI_HOST-compliant peripherals. • Supports transfer rates up to 895.1 Mbps with two lanes.
	LCD Interface (LCDIF)	• One LCDIF - a high-performance, low-power display processor unit (DPU), which outputs video and graphic streams from a single output panel with up to 720p display resolution.
Audio	HiFi 4 DSP Platform (HiFi 4)	• Compute Domain DSP CPU - HiFi 4 DSP is an audio engine with a highly optimized audio digital signal processor (DSP), with an extended set of instructions for linear algebra, running at frequencies up to 325 MHz. • Up to 128 KB of HiFi 4 DSP local TCM RAM (64 KB instruction / 64 KB data). These RAMs can be accessed by the M33 or the DMA engines via the inbound PIF port.
	HiFi 1 DSP Platform (HiFi 1)	• Sense Domain DSP CPU - HiFi 1 is low-power audio DSP, running at frequencies up to 250 MHz.
	EZH-V with DSP extensions	• EZ Handler RISC-V (EZH-V) Event / Algorithm Handler with 32 KB EZH code RAM and 64-bit I/D TCM.
	Sigma Delta Analog-to-Digital Converter (SDADC)	• One SDADC- a low-power high-performance audio ADC module that supports analog microphones, line inputs, and enables acoustic noise and echo cancellation.

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Table 1. i.MX RT700 features*...continued*

	PDM Microphone Interface (MICFIL)	• One MICFIL - delivers audio from microphones to the processor in several applications • Supports up to 8 channels with associated decimators and Hardware Voice Activation Detector. • Supports DMA.
	Synchronous Audio Interface (SAI)	• Four SAIs - provide interfaces that support full-duplex serial digital audio interfaces with frame synchronization formats such as I2S, AC97, TDM, and Codec/DSP interfaces.
Connectivity	Universal Serial Bus Controller (USB)	• One high speed USB (USB0) — provides high-performance USB functionality that conforms to Universal Serial Bus Specification, Rev. 2.0. — USB high-speed host/device controller with on-chip PHY and dedicated DMA controller • One high speed eUSB (USB1) — provides high-performance USB functionality that conforms to Universal Serial Bus Specification, Rev. 2.0 and Embedded Universal Serial Bus 2.0 (eUSB) electrical specification. — eUSB high-speed host/device controller with dedicated DMA controller and on-chip PHY supports both native and repeater modes
	Universal Serial Bus 2.0 PHY (USBPHY)	• One USBPHY - interfaces with the USB host and device system at a low-speed (LS) rate of 1.5 Mbit/s, full-speed (FS) rate of 12 Mbit/s, or USB 2.0 highspeed (HS) rate of 480 Mbit/s.
	USB Device Charger Detection Module (USBDCD)	• One USBDCD - works with the USB transceiver to detect whether the USB device is attached to a charging port, either a Dedicated Charging Port (DCP) or a Charging Downstream Port (CDP).
Low-speed Communications	Flexible I/O (FLEXIO)	• One FLEXIO - emulates of a variety of serial/parallel communication protocols. • Flexible 16-bit timers with support for a variety of trigger, reset, enable, and disable conditions. • Can be configured to provide a parallel interface to an LCD
	Low-Power Flexible Communications Interface (LP_FLEXCOMM)	• Eighteen configurable Universal Serial Interface LP_FLEXCOMM modules. LP_FLEXCOMM 0-13 are used for the VDD2_COMP domain, and LP_FLEXCOMM 17-20 are for the VDD1_SENSE domain. Each module contains an integrated FIFO and has DMA support. Each of the eighteen modules can be configured as: — Low-Power Universal Asynchronous Receive/Transmit (LPUART) with asynchronous transmit and receive.

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Table 1. i.MX RT700 features*...continued*

		— Low-Power Serial Peripheral Interface (LPSPI) controller or responder, with up to four peripheral chip selects. — Low-Power Inter-Integrated Circuit (LPI2C) with separate controller and responder functions. • Two additional high-speed LPSPI interfaces supporting 50 MHz operation (LP_FLEXCOMM 14 and 16) • One additional LPI2C interface with pseudo open-drain pads (LP_FLEXCOMM15) for PMIC application and used as controller only.
	Improved Inter-Integrated Circuit (I3C)	• Four I3C bus interfaces, that act as an extension of the I2C bus protocol supporting higher speeds.
Timers	Micro-Tick Timer (UTICK)	• Two UTICKs (one for Compute domain and one for Sense domain) - 31-bit timers that each provides a fixed time interval between interrupts. • Ultra-low power micro-tick timer running from the watchdog oscillator, with capture capability for timestamping. • UTICK can be used to wake up the chip from Sleep mode and Deep Sleep mode.
	Standard Counter/ Timers (CTIMER)	• Eight (5 in the Compute domain and 3 in the Sense domain) standard 32-bit Counter/Timers modules with PWM capability
	OS Event Timer (OSTIMER)	• One 64-bit OSTIMER interfaces to CPU0, CPU1, HiFi 1 DSP and HiFi 4 DSP with individual match/capture and interrupt generation logic.
	SCTimer (SCT)	• One 32-bit SCT- multi-purpose timer with extensive event-generation, match/compare, and complex PWM and output control features with minimal or no CPU intervention. — 10 general-purpose/PWM outputs, 8 general-purpose inputs — Supports DMA and can trigger external DMA events — Supports fractional match values for high resolution
	Multi-Rate Timer (MRT)	• Two (one for Compute Domain and one for Sense Domain) 24-bit multi-rate timer modules with 4 channels each capable of generating repetitive interrupts at different, programmable frequencies.
	Windowed Watchdog Timer (WWDT)	• Four WWDTs, each with a dedicated watchdog oscillator (1 MHz LPOSC), which help reset or interrupt an erroneous microcontroller within a programmable timer.
Analog	Analog-to-Digital Converter (ADC)	• One ADC - a low-power 16-bit successive approximation ADC with sampling rates up to 35k samples per second with an enhanced ADC controller • Supports up to 14 single-ended channels or 7 differential channels • DMA supported.
	Comparator (ACMP)	• One ACMP - provides a circuit for comparing two analog input voltages.

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Table 1. i.MX RT700 features...*continued*

Interconnects, crossbars and DMA	Input Multiplexing (INPUTMUX)	• Two INPUTMUXes - provide signal routing for internal peripherals.
	Enhanced Direct Memory Access (eDMA)	• Four eDMAs, each with a general purpose DMA engine, capable of performing complex data transfers with minimal intervention from a host controller. — eDMA can be configured such that one pair is secure and the other non-secure. — eDMA can also be configured as one pair dedicated for the control CPUs and the other for the DSPs.
	Crossbar Switch Lite (AXBS_Lite)	• AXBS_Lite connects bus controllers and bus targets using a crossbar switch structure.
	Peripheral Bridge (AIPS_Lite)	• AIPS_Lite converts the crossbar switch interface to an interface that can access most of the target peripherals on this chip.
	Peripheral Bridge (PBRIDGE2)	• PBRIDGE2 converts an AMBA AHB interface to a peripheral interface.
Temperature range (ambient)	-30 °C to 85 °C	

1.2 Ordering Information

Table 2 shows orderable part numbers covered by this data sheet.

Table 2. Orderable part numbers

Orderable Part Number[1]	DSP[2]	Graphics[3]	SRAM (MB)	FlexComm	Package
MIMXRT735SGAWBR	-	No	5	18[4]	WLCSP256[5]
MIMXRT758SGAWBR	-	Yes	7.5	18[4]	WLCSP256[5]
MIMXRT798SGAWBR	HiFi 4	Yes	7.5	18[4]	WLCSP256[5]
MIMXRT735SGFOB(R)	-	No	5	18[6]	FOWLP324[7]
MIMXRT758SGFOB(R)	-	Yes	7.5	18[6]	FOWLP324[7]
MIMXRT798SGFOB(R)	HiFi 4	Yes	7.5	18[6]	FOWLP324[7]

[1] As marked on package
[2] HiFi 1 DSP is always enabled.
[3] GPU, JPEG Decoder, and PNG Decoder
[4] FlexComm0 does not support P2, P3, P4, P5, P6 pins, FlexComm4 does not support P5, P6 pins, FlexComm5 does not support P5, P6 pins, FlexComm6 does not support P4, P5, P6 pins, and FlexComm20 does not support P2, P5, P6 pins. VREFH_ANA18, VDD1V2_EUSB, and VDD1V8_EUSB are not available on WLCSP package.
[5] 256-pin wafer level chip scale package
[6] FlexComm4 does not support P5 pin and FlexComm20 does not support P2, P5, P6 pins.
[7] 324-pin Fan-out wafer-level package

Table 3. Device revision number

Device Mask Set Number	SILICONREV_ID	JTAG_IDCODE
0P77N	0x000B0000	0x288CC01D

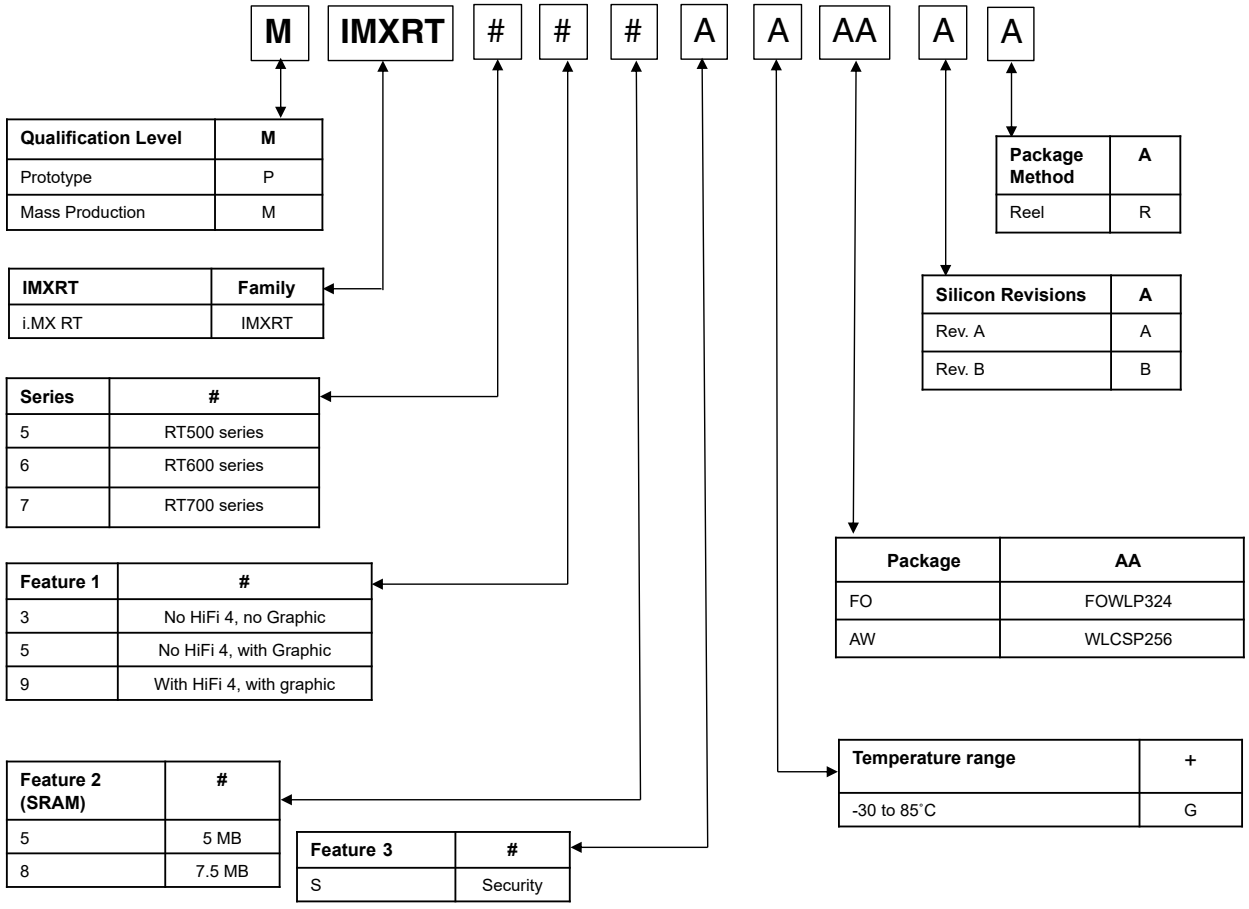

Figure 1. Part number nomenclature - i.MX RT700

Table 4. Related Resources

Type	Description
Reference Manual	The *i.MX RT700 Crossover Microcontrollers Reference Manual* contains a comprehensive description of the structure and function (operation) of a device.
Security Reference Manual	The *i.MX RT700 Security Reference Manual* provides an overview of the chip security components, explaining the purposes and features of each of them.
Data Sheet	Refers to this document which includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.

1.3 Package marking

Package marking for i.MX RT700 microcontrollers consist of four sets of identifiers as following sections.

Please provide this information to your local NXP representative for further details.

1.3.1 WLCSP package marking

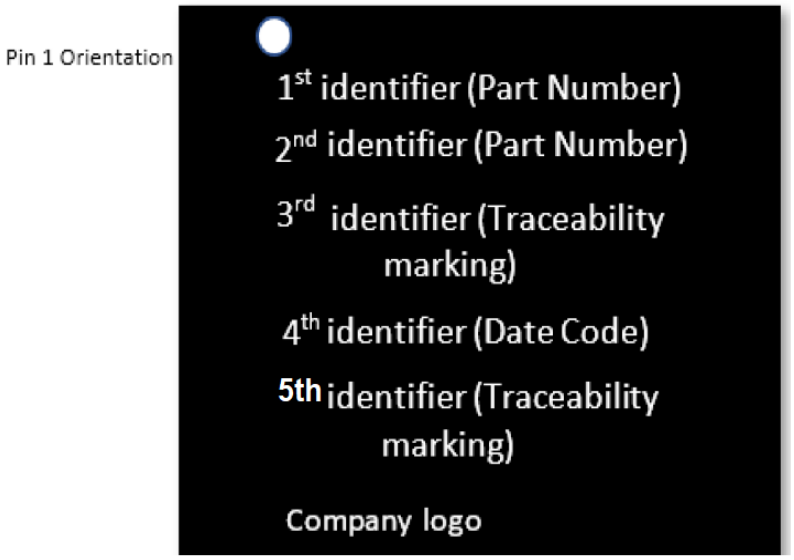

Figure 2. WLCSP package markings

- The first identifier defines the Part Number and is composed of 11 characters ("IMX" is not marked on first line due to limited space).
- The second identifier defines the last portion of the Part Number and is composed of 4 characters.
- The third identifier and fifth identifier define the Traceability markings.
- The fourth identifier defines the Date Code for the week of manufacture is a subset of the standard 8 character format.

The standard date code format is “xxxxYYWW”:

- The leading digits represented by “x” can be ignored and “YYWW” indicate the Date Code.
- “YY" represents an encoding of the calendar year (for example, 23 corresponds to year 2023).
- “WW” represents an encoding of the work week within the calendar year (for example, 07 corresponds to work week 7).

1.3.2 FOWLP package marking

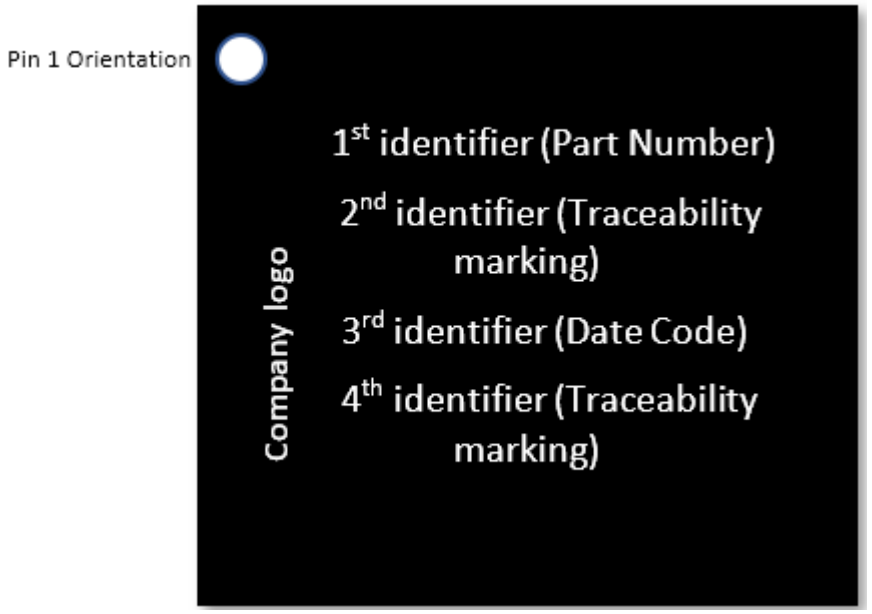

Figure 3. FOWLP package markings

- The first identifier defines the Part Number and is composed of 11 characters ("IMX" and "R" are not marked on first line due to limited space).
- The second and fourth identifiers define the Traceability markings.
- The third identifier defines the Date Code for the week of manufacture is a subset of the standard five characters format.

The standard date code format is “xYYWW”:

- The leading digits represented by “x” can be ignored and “YYWW” indicate the Date Code.
- “YY" represents an encoding of the calendar year (for example, 23 corresponds to year 2023).
- “WW” represents an encoding of the work week within the calendar year (for example, 07 corresponds to work week 7).

2 Architectural overview

The RT700 is architected for sustained low power operation while supporting advanced peripherals and secure applications. The chip is a general purpose MCU, but is well-suited for IoT and wearable applications.

It has five independent chip domains (Compute, Sense, Common, DSP, Media), two of which serve as the primary processing domains – the Compute and Sense Domains. The Compute and Sense Domains each have a Cortex-M33 processor, co-located with a DSP, and an extensive set of peripherals, which include a Machine Learning module (NPU), a Graphics module (VGPU), and an advanced security subsystem (ELS). Each domain also has access to various global SoC resources, including shared system RAM, analog modules, and GPIO.

2.1 Block Diagram

Figure 4 shows the detailed block diagram of i.MX RT700 processors.

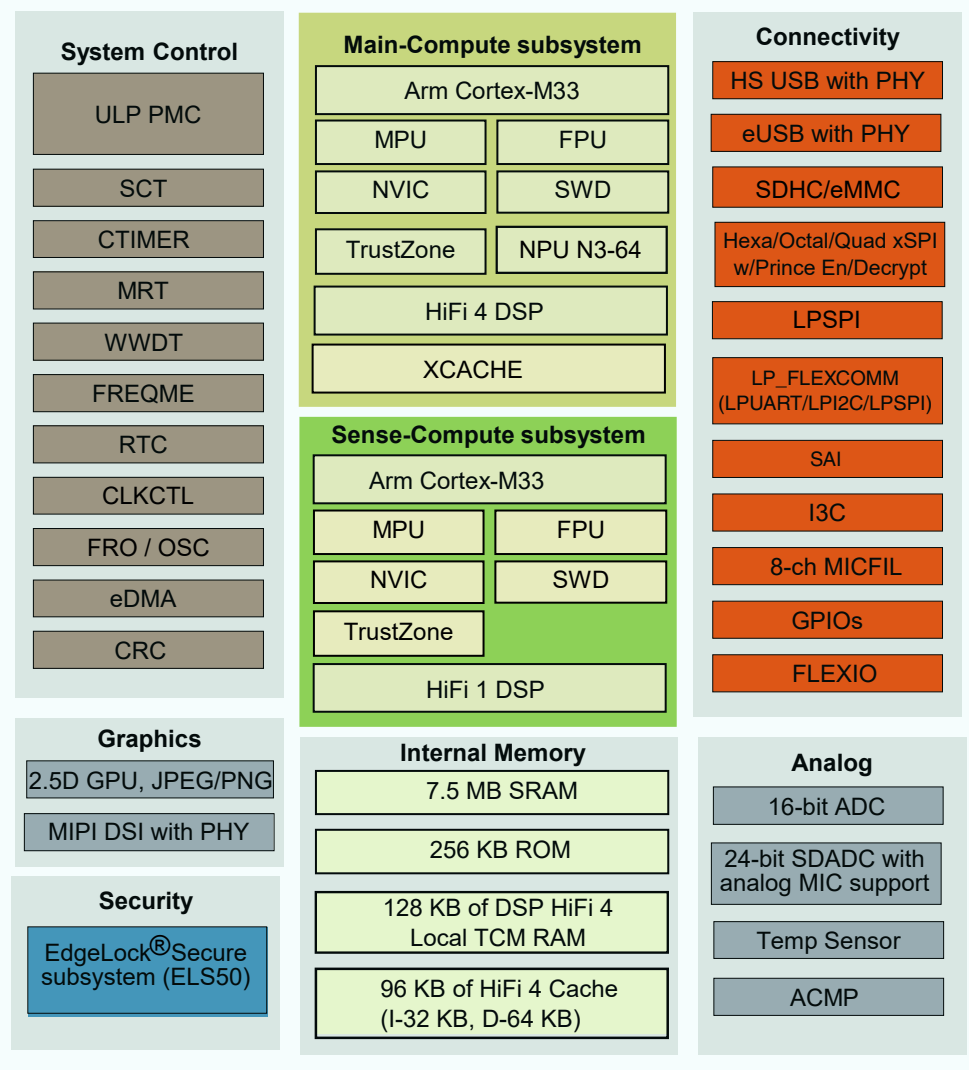

Figure 4. i.MX RT700 system block diagram

2.2 Shared system SRAM

The entire system SRAM space (The compute M33 accesses memory through caches, while the sense M33 has single cycle access) of up to 7.5 MB is divided into 30 separate partitions, which are accessible to all bus controllers residing in the Compute domain, including the M33 processor, HiFi 4 DSP, and DMA controllers. The Sense-Compute domain M33 processor is able to access the shared system SRAM through a system or code bus as well. The M33 processor can access 7.5 MB for data and only 2 MB of shared SRAM for code. The HiFi 1 DSP can access 2 MB of shared SRAM.

Under software control, each of the 30 individual SRAM partitions can be used exclusively as code or as data, dedicated to either CPU or shared among the various controllers. Each partition can be independently placed in a low-power retention mode or powered off entirely.

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX RT700 processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the processors. See Table 5 for a quick reference to the individual tables and sections.

Table 5. Chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum voltage and current ratings	Absolute maximum voltage and current ratings
Thermal handling ratings	Thermal handling ratings
Moisture handling ratings	Moisture handling ratings
ESD handling ratings	ESD handling ratings
Thermal characteristics	Thermal characteristics
General operating conditions	General operating conditions
I/O parameters	I/O parameters

3.1.1 Thermal handling ratings

Table 6. Thermal handling ratings

Symbol	Description	Min	Typ	Max	Unit
TSTG	Storage temperature [1]	–55	—	150	°C
TSDR	Solder temperature, lead-free [2]	—	—	260	°C

[1] Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
[2] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

3.1.2 Moisture handling ratings

Table 7. Moisture handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
MSL	Moisture sensitivity level (WLCSP) [1]	—	—	1	—	—
MSL	Moisture sensitivity level (FOWLP) [1]	—	—	3	—	—

[1] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

3.1.3 ESD handling ratings

Table 8. ESD handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VHBM	Electrostatic discharge voltage, human body model [1]	-2000	—	2000	V	—

Table continues on the next page...

Table 8. ESD handling ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VCDM	Electrostatic discharge voltage, charged-device model [2]	-500	—	500	V	—
ILAT	Latch-up current at ambient temperature of 85 °C [3]	-100	—	100	mA	—

[1] Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) .
[2] Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components .
[3] Determined according to JEDEC Standard JESD78, IC Latch-Up Test .

3.1.4 Absolute maximum voltage and current ratings

Stress beyond those listed under the following table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 9. Absolute maximum voltage and current ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD1	Supply voltage for core logic in Sense domain [1][2]	-0.3	—	1.32	V	On-chip regulator not used. PMC_ POWERCFG[LDO1PD] = 1. Power supplied by an off-chip power management IC (PMIC).
VDD2	Supply voltage for core logic in Main compute domain [1][2]	-0.3	—	1.32	V	On-chip regulator not used. PMC_ POWERCFG[LDO2PD] = 1. Power supplied by an off-chip power management IC (PMIC).
VDDN	Supply voltage for media and common peripherals [1][2]	-0.3	—	1.32	V	On-chip regulator not used. PMC_ POWERCFG[DCDCPD] = 1. Power supplied by an off-chip power management IC (PMIC).
VDD1V8	1.8 V Supply voltage for PMC [1] [2]	-0.3	—	1.98	V	—
VDD1V8_AO	1.8 V supply voltage for “Always on” logic [1][2]	-0.3	—	1.98	V	—
VDD1V8_DCDC	1.8 V supply voltage for on-chip DCDC [1][2]	-0.3	—	1.98	V	—
VDD1V8_MIPI	1.8 V supply voltage for MIPI [1] [2]	-0.3	—	1.98	V	—

Table continues on the next page...

Table 9. Absolute maximum voltage and current ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VREF_LDO	PMC (LDO) reference voltage [1][2]	-0.3	—	1.98	V	—
VDDA_1V8	1.8 V supply voltage for on-chip analog modules (such as SAR-ADC and SD-ADC) [1][2]	-0.3	—	1.98	V	—
VDDIO_0	I/O supply voltage for GPIO0, GPIO1, GPIO3, GPIO7, GPIO8, GPIO9, and GPIO10 [1][2]	-0.3	—	1.98	V	—
VDDIO_2	I/O supply voltage for GPIO2 [1][2]	-0.3	—	3.96	V	—
VDDIO_4	I/O supply voltage for GPIO4 [1][2]	-0.3	—	1.98	V	—
VDDIO_5	I/O supply voltage for GPIO5 [1][2]	-0.3	—	1.98	V	—
VDDIO_6	I/O supply voltage for GPIO6 [1][2]	-0.3	—	1.98	V	—
VDDIO_AO	I/O supply voltage for PMIC_MODE0, PMIC_MODE1, PMIC_IRQN [1][2]	-0.3	—	1.98	V	—
VDD1V2_EUSB	1.2 V supply voltage for eUSB PHY [1][2][3]	-0.3	—	1.32	V	—
VDD1V8_EUSB	1.8 V supply voltage for eUSB PHY [1][2][3]	-0.3	—	1.98	V	—
VDD3V3_USB	3.3 V supply voltage for USB PHY [1][2]	-0.3	—	3.96	V	—
VREFH_ANA18	1.8 V supply voltage for VREF [1][3]	-0.3	—	1.98	V	—
USB0_VBUS_DETECT	USB VBUS detection [1]	-0.3	—	5.5	V	—
IDD	Supply current (WCLSP256) [1][4]	—	—	150	mA	per supply pin (1.8 V), 1.71 V ≤ VDDIO < 1.89 V 1.71 V ≤ VDDIO < 3.6 V
IDD	Supply current (FOWLP324) [1][4]	—	—	150	mA	per supply pin (1.8 V), 1.71 V ≤ VDDIO < 1.89 V 1.71 V ≤ VDDIO < 3.6 V
IDD	Supply current (WCLSP256) [1][4]	—	—	50	mA	per supply pin (1.2 V), 1.1 V ≤ VDDIO < 1.2 V
IDD	Supply current (FOWLP324) [1][4]	—	—	50	mA	per supply pin (1.2 V), 1.1 V ≤ VDDIO < 1.2 V

Table continues on the next page...

Table 9. Absolute maximum voltage and current ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
ISS	Supply current (WCLSP256) [1] [4]	—	—	150	mA	per supply pin (1.8 V), 1.71 V ≤ VDDIO < 1.89 V 1.71 V ≤ VDDIO < 3.6 V
ISS	Supply current (FOWLP324) [1] [4]	—	—	150	mA	per supply pin (1.8 V), 1.71 V ≤ VDDIO < 1.89 V 1.71 V ≤ VDDIO < 3.6 V
ISS	Supply current (WCLSP256) [1] [4]	—	—	50	mA	per supply pin (1.2 V), 1.1 V ≤ VDDIO < 1.2 V
ISS	Supply current (FOWLP324) [1] [4]	—	—	50	mA	per supply pin (1.2 V), 1.1 V ≤ VDDIO < 1.2 V
Ptot(pack)	Total power dissipation (per package) [1][5]	—	—	2.74	W	WLCSP 256, based on package heat transfer, not device power consumption
Ptot(pack)	Total power dissipation (per package) [1][5]	—	—	3.2	W	FOWLP 324, based on package heat transfer, not device power consumption

[1] In accordance with the Absolute Maximum Rating System (IEC 60134). The following applies to the limiting values: This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted. The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed.
[2] Voltage above the maximum operating voltage and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.
[3] VREFH_ANA18, VDD1V2_EUSB, and VDD1V8_EUSB are not available on WLCSP package.
[4] The peak current cannot exceed the total supply current.
[5] Determined in accordance to JEDEC JESD51-2A natural convection environment (still air).

3.1.5 Thermal specifications

3.1.5.1 Thermal operating requirements

Table 10. Thermal operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
TJ	Die junction temperature	-30	—	95	°C	—
Tamb	Ambient temperature [1]	-30	—	85	°C	—

[1] Maximum Tamb can be exceeded only if the user ensures that TJ does not exceed maximum TJ. The simplest method to determine TJ is: TJ = Tamb + $R_{\theta JA}$ × chip power dissipation.

3.1.5.2 Thermal characteristics

The following tables show the package thermal characteristics.

Table 11. Thermal resistance

Symbol	Rating	Board type[1]	Value	Unit
FOWLP324 Package				
$R_{\theta JA}$	Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	23.4	°C/W
Ψjt	Junction to Package Top Thermal Resistance[2]	JESD51-9, 2s2p	0.1	°C/W
WLCSP256 Package				
$R_{\theta JA}$	Junction to Ambient Thermal Resistanc[2]	JESD51-9, 2s2p	27.4	°C/W
Ψjt	Junction to Package Top Thermal Resistance[2]	JESD51-9, 2s2p	0.1	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

3.1.6 General operating conditions

Table 12. General operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
COMPUTE_MAIN_CLK	CPU0 (Compute Cortex-M33) clock frequency	—	—	325	MHz	—
SENSE_MAIN_CLK	CPU1 (Sense Cortex-M33) clock frequency	—	—	250	MHz	—
DSP_CLK	HiFi 4 DSP clock frequency	—	—	325	MHz	—
SENSE_DSP_CLK	HiFi 1 DSP clock frequency	—	—	250	MHz	—
GPU_FCLK	GPU clock frequency	—	—	325	MHz	—
VDD1V8_MIPI	1.8 V supply voltage for MIPI [1]	1.71	1.8	1.89	V	—
VREF_LDO	PMC (LDO) reference voltage [1]	1.71	1.8	1.89	V	—
VDD1V8	1.8 V supply voltage for PMC [1]	1.71	1.8	1.89	V	—
VDD1V8_AO	1.8 V supply voltage for “Always on” logic [1]	1.71	1.8	1.89	V	—
VDD1V8_DCDC	1.8 V supply voltage for on-chip DCDC [1]	1.71	1.8	1.89	V	—
VDDA_1V8	1.8 V supply voltage for on-chip analog modules (such as ADC and SDADC) [1]	1.71	1.8	1.89	V	—

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Table 12. General operating conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDIO_0	I/O supply voltage for GPIO0, GPIO1, GPIO3, GPIO7, GPIO8, GPIO9, and GPIO10 [1]	1.71	1.8	1.89	V	—
VDDIO_2	I/O supply voltage for GPIO2 [1]	1.71	1.8/3.3	3.6	V	PADVRANGE[VRANGE] == 00 (continuous mode)
VDDIO_2	I/O supply voltage for GPIO2 [1]	1.71	1.8	1.89	V	PADVRANGE[VRANGE] == 01 (1.8 V only mode)
VDDIO_2	I/O supply voltage for GPIO2 [1]	3.0	3.3	3.6	V	PADVRANGE[VRANGE] == 10 (3.3 V only mode)
VDDIO_4	I/O supply voltage for GPIO4 [1]	1.71	1.8	1.89	V	GPIO_BANK4_CFG[BANK4_CFG] == 0 (1.8 V mode)
VDDIO_4	I/O supply voltage for GPIO4 [1]	1.1	1.2	1.3	V	GPIO_BANK4_CFG[BANK4_CFG] == 1 (1.2 V mode)
VDDIO_5	I/O supply voltage for GPIO5 [1]	1.71	1.8	1.89	V	GPIO_BANK5_CFG[BANK5_CFG] == 0 (1.8 V mode)
VDDIO_5	I/O supply voltage for GPIO5 [1]	1.1	1.2	1.3	V	GPIO_BANK5_CFG[BANK5_CFG] == 1 (1.2 V mode)
VDDIO_6	I/O supply voltage for GPIO6 [1]	1.71	1.8	1.89	V	GPIO_BANK6_CFG[BANK6_CFG] == 0 (1.8 V mode)
VDDIO_6	I/O supply voltage for GPIO6 [1]	1.1	1.2	1.3	V	GPIO_BANK6_CFG[BANK6_CFG] == 1 (1.2 V mode)
VDDIO_AO	I/O supply voltage for PMIC_MODE0, PMIC_MODE1, PMIC_IRQN [1]	1.71	1.8	1.89	V	—
VDD1V2_EUSB	1.2 V supply voltage for eUSB PHY [1][2]	1.1	1.2	1.3	V	—
VDD1V8_EUSB	1.8 V supply voltage for eUSB PHY [1][2]	1.71	1.8	1.89	V	—
VDD3V3_USB	3.3 V supply voltage for USB PHY [1][3][4]	3.0	3.3	3.6	V	—
VREFH_ANA18	1.8 V supply voltage for VREFH [1][2]	1.71	1.8	1.89	V	—

Table continues on the next page...

Table 12. General operating conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
USB0_VBUS_DETECT	USB0_VBUS detection [1][3][4]	4.0 or 3.0	5.0	5.5	V	—
fotp_clk (fipg_clk/HW_OCOTP_CLK_DIV[DIV])	OTP clock frequency	—	—	120	MHz	For OTP programming only

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.
[2] VREFH_ANA18, VDD1V2_EUSB and VDD1V8_EUSB are not available on WLCSP package.
[3] The USB PHY provides two options for reporting VBUS valid back to the USB controller: A programmable internal VBUS_VALID comparator (the default option), or an alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V; USBPHY_USB1_VBUS_DETECTn[VBUSVALID_SEL] selects which option is used.
[4] If the VBUS_VALID comparator is used, USBPHY_USB0_VBUS_DETECTn[VBUSVALID_THRESH] determines the threshold voltage for a valid VBUS. The programmable range is 4.0 V to 4.4 V (default).

3.1.6.1 VDD1, VDD2, and VDDN operating conditions when using an external supply for VDD1 and VDD2

The operating condition specifications in the table below apply when both the VDD1 and VDD2 power are supplied from an external source.

When performing any OTP read or write function, the VDD2 voltage must be set to 1.0 V or higher when using external supply for VDD1 and VDD2.

Table 13. VDD1, VDD2, and VDDN operating conditions when using an external supply for VDD1 and VDD2

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD1	Supply voltage for core logic in the Sense domain	1.1	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 250 MHz
VDD1	Supply voltage for core logic in the Sense domain: Regular operation	1.0	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 205 MHz
VDD1	Supply voltage for core logic in the Sense domain: This is the voltage during initial boot. If an external supply is used, then it must be within this voltage range for power-up. After the application is running, the external voltage can be changed. The BOOT_SPEED fuse option should not be used to select boot at a different voltage.	1.0	—	1.1	V	Start-up voltage. Active mode - SENSE_MAIN_CLK up to 205 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.9	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 160 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.8	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB

Table continues on the next page...

Table 13. VDD1, VDD2, and VDDN operating conditions when using an external supply for VDD1 and VDD2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						mode - SENSE_MAIN_CLK up to 100 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.7	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 45 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.63	—	1.155	V	Deep Sleep mode using RBB
VDD1	Supply voltage for core logic in the Sense domain	0.5	—	1.155	V	Deep Sleep Async mode using RBB
VDD1	Supply voltage for core logic in the Sense domain	0.5	—	1.155	V	Full Deep Sleep Retention (FDSR) mode
VDD2	Supply voltage for core logic in the Main compute domain	1.1	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 325 MHz
VDD2	Supply voltage for core logic in the Main compute domain: Regular operation	1.0	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 250 MHz
VDD2	Supply voltage for core logic in the Main compute domain: This is the voltage during initial boot. If an external supply is used, then it must be within this voltage range for power-up. After the application is running, the external voltage can be changed. The BOOT_SPEED fuse option should not be used to select boot at a different voltage.	1.0	—	1.1	V	Start-up voltage. Active mode - COMPUTE_MAIN_CLK up to 250 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.9	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 192 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.8	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 110 MHz

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Table 13. VDD1, VDD2, and VDDN operating conditions when using an external supply for VDD1 and VDD2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD2	Supply voltage for core logic in the Main compute domain	0.7	—	1.155	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 45 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.63	—	1.155	V	Deep Sleep mode using RBB
VDD2	Supply voltage for core logic in the Sense domain	0.5	—	1.155	V	Deep Sleep Async mode using RBB
VDD2	Supply voltage for core logic in the Main compute domain	0.5	—	1.155	V	Deep Sleep Retention mode (all VDD2 domains in DSR or FDSR)
VDDN	Supply voltage for media and common peripherals [1][2]	1.1	—	1.155	V	Start-up voltage. Active mode, VDDN required to be 1.1 V at the startup, later it can be set to 1.0 V.
VDDN	Supply voltage for media and common peripherals [2]	1.0	—	1.155	V	Active mode or Sleep mode or Deep Sleep or Compute Deep Sleep Async: where VDDN = 1.0 V min, VDD1 and VDD2 can be 1.0 V, 0.9 V, 0.8 V, 0.7 V for external supply.
VDDN	Supply voltage for media and common peripherals [2]	0.6	—	1.155	V	Dual Deep Sleep Async or FDSR

[1] This is the voltage during initial boot. If an external supply is used, then it must be within this voltage range for power-up. After the application is running, the external voltage can be changed. The BOOT_SPEED fuse option should not be used to select boot at a different voltage.

[2] VDDN voltage must be equal or greater than VDD1 and VDD2.

3.1.6.2 VDD1, VDD2, and VDDN operating conditions when using on-chip LDO for VDD1 and VDD2

The operating condition specifications in the table below apply when the on-chip LDOs or SCPCs are used to supply VDD1 and/or VDD2.

Table 14. VDD1, VDD2, and VDDN operating conditions when using on-chip LDO for VDD1 and VDD2

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD1	Supply voltage for core logic in the Sense domain [1]	1.0	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 205 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.9	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB

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Table 14. VDD1, VDD2, and VDDN operating conditions when using on-chip LDO for VDD1 and VDD2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						mode - SENSE_MAIN_CLK up to 160 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.8	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 100 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.7	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - SENSE_MAIN_CLK up to 45 MHz
VDD1	Supply voltage for core logic in the Sense domain	0.5	—	1.05	V	Full Deep Sleep Retention (FDSR) mode
VDD2	Supply voltage for core logic in the Main compute domain [1]	1.0	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 250 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.9	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 192 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.8	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 110 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.7	—	1.05	V	Active, Sleep, or Deep Sleep all in AFBB mode - COMPUTE_MAIN_CLK up to 45 MHz
VDD2	Supply voltage for core logic in the Main compute domain	0.5	—	1.05	V	Deep Sleep Retention mode (all VDD2 domains in DSR or FDSR)
VDDN	Supply voltage for media and common peripherals [2]	1.1	—	1.15	V	Start-up voltage. Active mode, VDDN required to be 1.1 V at the startup, later it can be set to 1.0 V.
VDDN	Supply voltage for media and common peripherals [2]	1.0	—	1.155	V	Active mode or Sleep mode or Compute

Table continues on the next page...

Table 14. VDD1, VDD2, and VDDN operating conditions when using on-chip LDO for VDD1 and VDD2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						Deep Sleep Async: where VDDN = 1.0 V min, VDD1 and VDD2 can be 0.8 V or 0.7 V for internal LDO supply.
VDDN	Supply voltage for media and common peripherals [2]	0.7	—	1.155	V	Deep Sleep mode, Deep Sleep Retention mode, Deep Sleep Async mode using RBB (all VDDN and VDD2 domains in DSR or FDSR)
VDDN	Supply voltage for media and common peripherals [2]	0.6	—	1.155	V	FDSR when using SCPC to power VDD1 and VDD2.

[1] In LDO Bypass mode
[2] VDDN voltage must be greater than VDD1 and VDD2 to account for LDO regulator drop and accuracy.

3.1.7 I/O parameters

3.1.7.1 Fail Safe GPIO (FSGPIO) DC parameters

PIO2, PIO8, PIO9, PIO10, and PMIC_I2C are Fail Safe pads.

Table 15. Fail Safe GPIO (FSGPIO) DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	High-level output voltage: Full Output Drive enabled [1]	VDDIO_x - 0.5	—	VDDIO_x	V	IOH = -10 mA (1.71 V to 1.98 V), IOH = -9 mA (3.0 V to 3.6 V)
VOH	High-level output voltage: Normal Output Drive enabled [1]	VDDIO_x - 0.5	—	VDDIO_x	V	IOH = -5 mA (1.71 V to 1.98 V), IOH = -4.5 mA (3.0 V to 3.6 V)
VOL	Low-level output voltage: Full Output Drive enabled [1]	—	—	0.5	V	IOH = 10 mA (1.71 V to 1.98 V), IOH = 10 mA (3.0 V to 3.6 V)
VOL	Low-level output voltage: Normal Output Drive enabled [1]	—	—	0.5	V	IOH = 5 mA (1.71 V to 1.98 V), IOH = 5 mA (3.0 V to 3.6 V)
VIH	High-level input voltage [1]	0.8 x VDDIO_x	—	VDDIO_x	V	1.71 V to 1.98 V
VIH	High-level input voltage [1]	0.7 x VDDIO_x	—	VDDIO_x	V	3.0 V to 3.6 V
VIL	Low-level input voltage [1]	0	—	0.3 x VDDIO_x	V	1.71 V to 1.98 V

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Table 15. Fail Safe GPIO (FSGPIO) DC parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VIL	Low-level input voltage [1]	0	—	0.2 x VDDIO_x	V	3.0 V to 3.6 V
Vhyst	Input Hysteresis voltage [1]	0.06 x VDDIO_x	—	—	V	1.71 V to 3.6 V
Iin	Input current [1]	-1	—	1	µA	VI = 0, VI = VDDIO_X; and On-Chip Pull-up and Pull-down resistor are disabled.
R Pull Up	Pull-up resistance	25	33	50	KΩ	1.71 V to 3.6 V
R Pull Down	Pull-down resistance	25	33	50	KΩ	1.71 V to 3.6 V

[1] The VDDIO Range Select (PADVRANGE) can be used to select desired I/O voltage range used in application. Please refer to i.MX RT700 Crossover Microcontroller Reference Manual for further details.

3.1.7.2 High Speed GPIO DC parameters

PIO0, PIO1, PIO3, PIO4, PIO5, PIO6, and PIO7 are High Speed pads.

Table 16. High Speed GPIO DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	High-level output voltage at VDDIO_n [1][2]	0.8 x VDDIO_n	—	—	V	1.8 V: -1 mA at DRIVE 00b, -2 mA at DRIVE 01b; -2 mA at DRIVE 10b; -2 mA at DRIVE 11b
VOL	Low-level output voltage at VDDIO_n [1][2]	—	—	0.2 x VDDIO_n	V	1.8V: 1 mA at DRIVE 00b; 2 mA at DRIVE = 01b; 2 mA at DRIVE = 10b; 2 mA at DRIVE = 11b
IOH	Output current capability at 1.8 V VDDIO_n [1][2]	—	—	-1	mA	DRIVE = 00b; VDDIO_n = 1.8 V range, measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.8 V VDDIO_n [1][2]	—	—	-1.5	mA	DRIVE = 01b; VDDIO_n = 1.8 V range, measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.8 V VDDIO_n [1][2]	—	—	-2	mA	DRIVE = 10b; VDDIO_n = 1.8 V range, measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.8 V VDDIO_n [1][2]	—	—	-3	mA	DRIVE = 11b; VDDIO_n = 1.8 V range,

Table continues on the next page...

Table 16. High Speed GPIO DC parameters*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.2 V VDDIO_n [1][2]	—	—	-0.6	mA	DRIVE = 00b; VDDIO_n = 1.2 V range, measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.2 V VDDIO_n [1][2]	—	—	-0.9	mA	DRIVE = 01b; VDDIO_n = 1.2 V range, measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.2 V VDDIO_n [1][2]	—	—	-1.2	mA	DRIVE = 10b; VDDIO_n = 1.2 V range, measure at 0.8 x VDDIO_n
IOH	Output current capability at 1.2 V VDDIO_n [1][2]	—	—	-1.8	mA	DRIVE = 11b; VDDIO_n = 1.2 V range, measure at 0.8 x VDDIO_n
IOL	Output low sink current capability at 1.8 V VDDIO_n [1][2]	1	—	—	mA	DRIVE = 00b; VDDIO_n = 1.8 V range, measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.8 V VDDIO_n [1][2]	1.5	—	—	mA	DRIVE = 01b; VDDIO_n = 1.8 V range, measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.8 V VDDIO_n [1][2]	2	—	—	mA	DRIVE = 10b; VDDIO_n = 1.8 V range, measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.8 V VDDIO_n [1][2]	3	—	—	mA	DRIVE = 11b; VDDIO_n = 1.8 V range, measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.2 V VDDIO_x [1][2]	0.6	—	—	mA	DRIVE = 00b; VDDIO_n = 1.2 V, range measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.2 V VDDIO_x [1][2]	0.9	—	—	mA	DRIVE = 01b; VDDIO_n = 1.2 V, range measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.2 V VDDIO_x [1][2]	1.2	—	—	mA	DRIVE = 10b; VDDIO_n = 1.2 V, range

Table continues on the next page...

Table 16. High Speed GPIO DC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						measure at 0.2 x VDDIO_n
IOL	Output low sink current capability at 1.2 V VDDIO_x [1][2]	1.8	—	—	mA	DRIVE = 11b; VDDIO_n = 1.2 V, range measure at 0.2 x VDDIO_n
VIH	High-level input voltage	0.7 x VDDIO_n	—	—	V	All voltage range
VIL	Low-level input voltage	—	—	0.3 x VDDIO_n	V	All voltage range
Vhyst	Hysteresis voltage	100	—	—	mV	All voltage range
Cin	Input Capacitance	—	2.9	—	pF	1.8 V VDDIO_n
Rpu	Pull-up Resistance	10	—	50	KΩ	All voltage range
Rpd	Pull-down Resistance	10	—	50	KΩ	All voltage range

[1] Drive setting can be set using the IOPTL register (bit 13 to 12) to select transmitter current drive.
[2] The VDDIO Range Select (PADVRANGE) can be used to select desired IO voltage range used in application. Please refer to i.MX RT700 Crossover Microcontroller Reference Manual for further details.

3.1.7.3 FSGPIO AC parameters

The AC parameters of FSGPIO are presented in the Table 17 respectively.

Table 17. FSGPIO AC specifications

NO.	Characteristic	Min	Typ	Max	Unit	Condition
1	f_{max}	—	—	60	MHz	Cload = 15 pF
2	Vpeak on pad	—	—	3.85	V	—
3	Pad rise/fall time: Normal Output Drive enabled, Standard mode enabled (Slew Rate)	—	—	3	ns	1.71 V to 1.98 V (Cload = 15 pF)
		—	—	6	ns	3.0 V to 3.6 V (Cload = 15 pF)
4	Pad rise/fall time: Normal Output Drive enabled, Slow mode enabled (Slew Rate)	—	—	6	ns	1.71 V to 1.98 V (Cload = 15 pF)
		—	—	12	ns	3.0 V to 3.6 V (Cload = 15 pF)
5	Pad rise/fall time: Full Output Drive enabled, Standard mode enabled (Slew Rate)	—	—	2.5	ns	1.71 V to 1.98 V (Cload = 15 pF)

Table continues on the next page...

Table 17. FSGPIO AC specifications...*continued*

NO.	Characteristic	Min	Typ	Max	Unit	Condition
		—	—	5	ns	3.0 V to 3.6 V (Cload = 15 pF)
6	Pad rise/fall time: Full Output Drive enabled, Slow mode enabled (Slew Rate)	—	—	5	ns	1.71 V to 1.98 V (Cload = 15 pF)
		—	—	10	ns	3.0 V to 3.6 V (Cload = 15 pF)

Note:

In 3.3 V mode:

If the I/O toggling frequency is lower than 25 MHz, it is recommended to use high range mode for better power consumption.

In 1.8 V mode:

It is recommended to use low range mode for better power consumption and better performance.

3.1.8 Power consumption operating behavior

The CoreMark application used for the bench measurements below uses IAR C/C++ compiler for ARM ver 8.40.2. Compiler settings are High speed, no size constraints and optimization level is none. Power and low power configurations are done using the power API form the SDK software package available on nxp.com.

3.1.8.1 CPU0 CM33 CoreMark, Sense Deep Sleep

The table below provides typical current numbers where CPU0 in the compute domain is running CoreMark and the sense domain is in Deep Sleep.

COMPUTE_MAIN_CLK is sourced from FRO0 running at the frequency indicated for each row. HiFi 4 DSP is powered down, and HiFi 1 is stalled.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.1 V. VDD1 = 0.63 V.

Body Bias: VDD2 AFBB, VDD2SRAM NBB, VDD1 RBB, VDD1SRAM RBB, VDDN RBB.

Data and code are located in SRAM partition 8.

Table 18. CPU0 CM33 CoreMark, Sense Deep Sleep

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD2	VDD2 supply current [1]	—	30.43	—	mA	COMPUTE_MAIN_CLK = 325 MHz, VDD2 = 1.1 V
IVDD2	VDD2 supply current [1]	—	20.85	—	mA	COMPUTE_MAIN_CLK = 250 MHz, VDD2 = 1.0 V

Table continues on the next page...

Table 18. CPU0 CM33 CoreMark, Sense Deep Sleep*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD2	VDD2 supply current [1]	—	14.27	—	mA	COMPUTE_MAIN_CLK = 192 MHz, VDD2 = 0.9 V
IVDD2	VDD2 supply current [1]	—	7.69	—	mA	COMPUTE_MAIN_CLK = 110 MHz, VDD2 = 0.8 V
IVDD2	VDD2 supply current [1]	—	3.15	—	mA	COMPUTE_MAIN_CLK = 45 MHz, VDD2 = 0.7 V
IVDD1	VDD1 supply current [1]	—	36.7	—	µA	—
IVDDN	VDDN supply current [1]	—	19.4	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	82.9	—	µA	FRO0 = 325 MHz
IVDD1V8	VDD1V8 supply current [1]	—	65.2	—	µA	FRO0 = 250 MHz
IVDD1V8	VDD1V8 supply current [1]	—	52.5	—	µA	FRO0 = 192 MHz
IVDD1V8	VDD1V8 supply current [1][2]	—	58.5	—	µA	FRO0 = 220 MHz
IVDD1V8	VDD1V8 supply current [1][3]	—	50.0	—	µA	FRO0 = 180 MHz
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][4]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][4]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][4]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[2] FRO is divided by 2 to get the 110 MHz COMPUTE_MAIN_CLK
[3] FRO is divided by 4 to get the 45 MHz COMPUTE_MAIN_CLK
[4] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

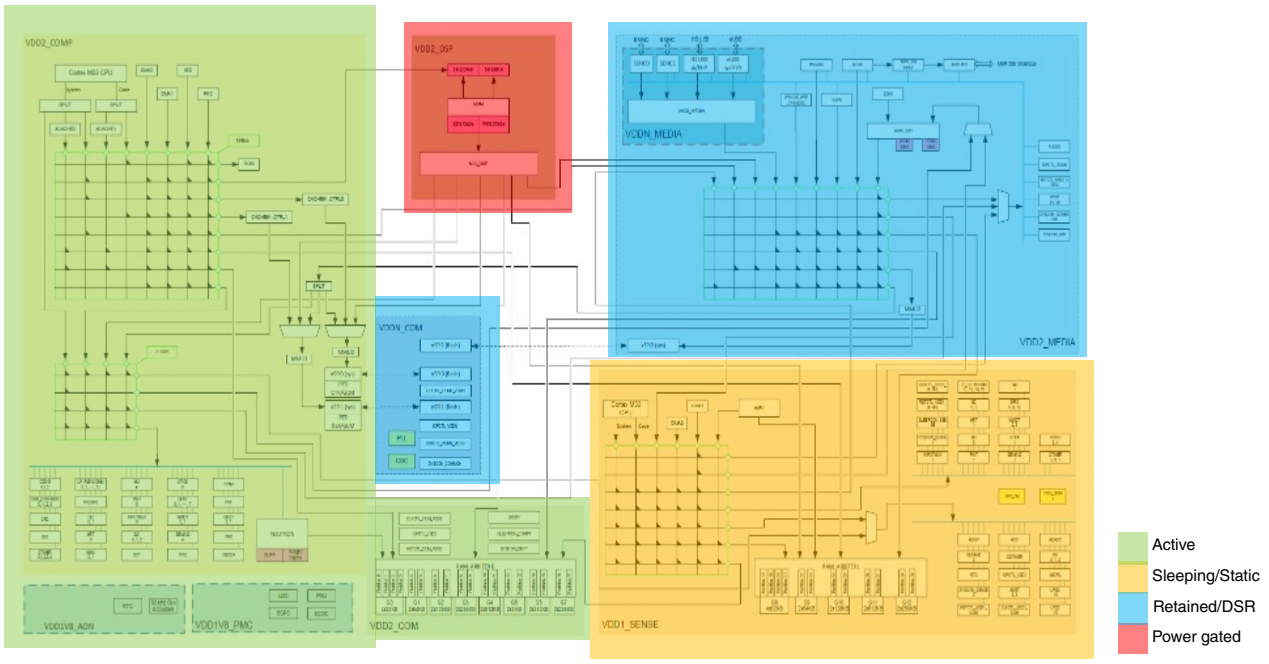


Figure 5. CPU0 CoreMark Sense Deep Sleep

3.1.8.2 CPU0 CM33 Sleep, Sense Deep Sleep

The table below provides typical current numbers where CPU0 in the compute domain is in Sleep and the sense domain is in Deep Sleep.

COMPUTE_MAIN_CLK is sourced from FRO0 running at the frequency indicated for each row. HiFi 4 DSP is powered down, and HiFi 1 DSP is stalled.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.1 V. VDD1 = 0.63 V.

Body Bias: VDD2 AFBB, VDD2SRAM NBB, VDD1 RBB, VDD1SRAM RBB, VDDN RBB.

Data and code are located in SRAM partition 8.

Table 19. CPU0 CM33 Sleep, Sense Deep Sleep

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD2	VDD2 supply current [1]	—	15.69	—	mA	COMPUTE_MAIN_CLK = 325 MHz, VDD2 = 1.1 V
IVDD2	VDD2 supply current [1]	—	10.62	—	mA	COMPUTE_MAIN_CLK = 250 MHz, VDD2 = 1.0 V
IVDD2	VDD2 supply current [1]	—	7.22	—	mA	COMPUTE_MAIN_CLK = 192 MHz, VDD2 = 0.9 V

Table continues on the next page...

Table 19. CPU0 CM33 Sleep, Sense Deep Sleep...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD2	VDD2 supply current [1]	—	4.12	—	mA	COMPUTE_MAIN_CLK = 110 MHz, VDD2 = 0.8 V
IVDD2	VDD2 supply current [1]	—	1.87	—	mA	COMPUTE_MAIN_CLK = 45 MHz, VDD2 = 0.7 V
IVDD1	VDD1 supply current [1]	—	36.7	—	µA	—
IVDDN	VDDN supply current [1]	—	19.4	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	82.9	—	µA	FRO0 = 325 MHz
IVDD1V8	VDD1V8 supply current [1]	—	65.2	—	µA	FRO0 = 250 MHz
IVDD1V8	VDD1V8 supply current [1]	—	52.5	—	µA	FRO0 = 192 MHz
IVDD1V8	VDD1V8 supply current [1][2]	—	58.5	—	µA	FRO0 = 220 MHz
IVDD1V8	VDD1V8 supply current [1][3]	—	50.0	—	µA	FRO0 = 180 MHz
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][4]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][4]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][4]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples
[2] FRO is divided by 2 to get the 110 MHz COMPUTE_MAIN_CLK
[3] FRO is divided by 4 to get the 45 MHz COMPUTE_MAIN_CLK
[4] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

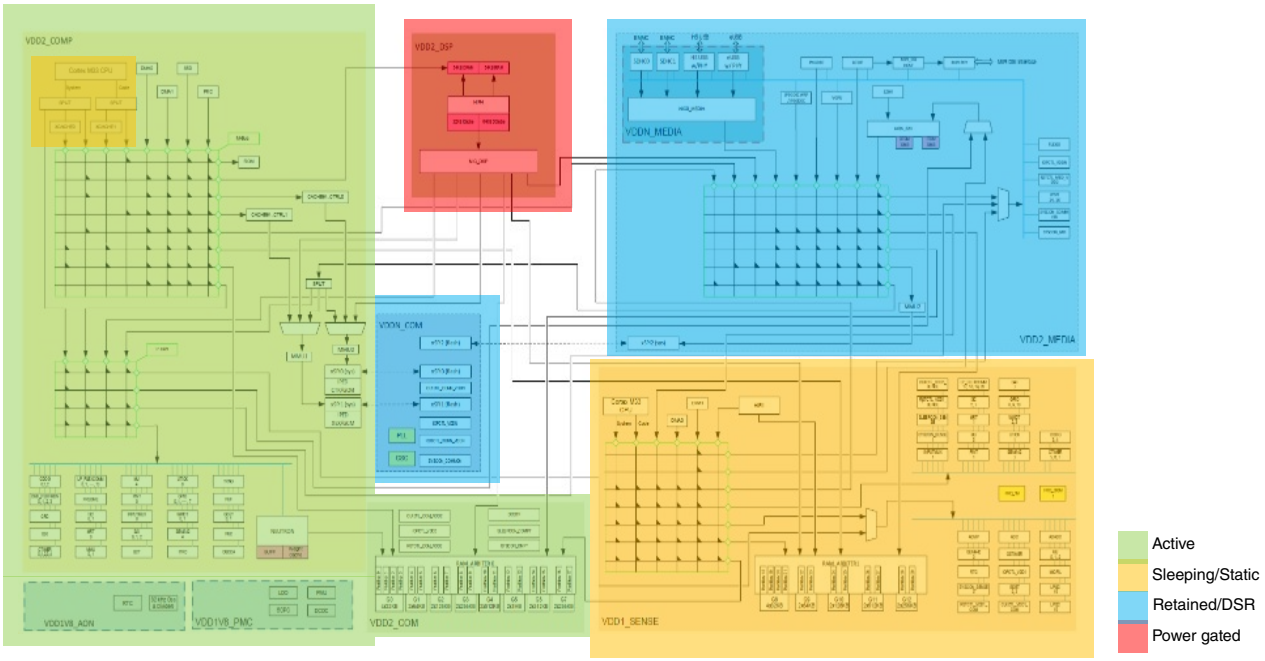


Figure 6. CPU0 Sleep, Sense Deep Sleep

3.1.8.3 Compute DSR, CPU1 CM33 CoreMark

The table below provides typical current numbers where the compute domain is in DSR and CPU1 in the sense domain is running CoreMark.

SENSE_MAIN_CLK is sourced from FRO2 running at the frequency indicated for each row. HiFi 4 DSP is powered down, and HiFi 1 DSP is stalled.

Body Bias: VDD2 RBB, VDD2SRAM RBB, VDD1 AFBB, VDD1SRAM NBB, VDDN RBB.

Data and code are located in SRAM partition 22.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.1 V. VDD2 = 0.5 V.

Table 20. Compute DSR, CPU1 CM33 CoreMark

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	16.02	—	mA	SENSE_MAIN_CLK = 250 MHz, voltage = 1.1 V
IVDD1	VDD1 supply current [1]	—	11.69	—	mA	SENSE_MAIN_CLK = 205 MHz, voltage = 1.0 V
IVDD1	VDD1 supply current [1]	—	8.12	—	mA	SENSE_MAIN_CLK = 160 MHz, voltage = 0.9 V

Table continues on the next page...

Table 20. Compute DSR, CPU1 CM33 CoreMark...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	4.80	—	mA	SENSE_MAIN_CLK = 100 MHz, voltage = 0.8 V
IVDD1	VDD1 supply current [1]	—	2.15	—	mA	SENSE_MAIN_CLK = 45 MHz, voltage = 0.7 V
IVDD2	VDD2 supply current [1]	—	24.9	—	µA	—
IVDDN	VDDN supply current [1]	—	19.4	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	65.2	—	µA	FRO2 = 250 MHz
IVDD1V8	VDD1V8 supply current [1]	—	55.3	—	µA	FRO2 = 205 MHz
IVDD1V8	VDD1V8 supply current [1]	—	46.0	—	µA	FRO2 = 160 MHz
IVDD1V8	VDD1V8 supply current [1][2]	—	54.3	—	µA	FRO2 = 200 MHz
IVDD1V8	VDD1V8 supply current [1][3]	—	50.1	—	µA	FRO2 = 180 MHz
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][4]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][4]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][4]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[2] FRO is divided by 2 to get the 100 MHz COMPUTE_MAIN_CLK
[3] FRO is divided by 4 to get the 45 MHz COMPUTE_MAIN_CLK
[4] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

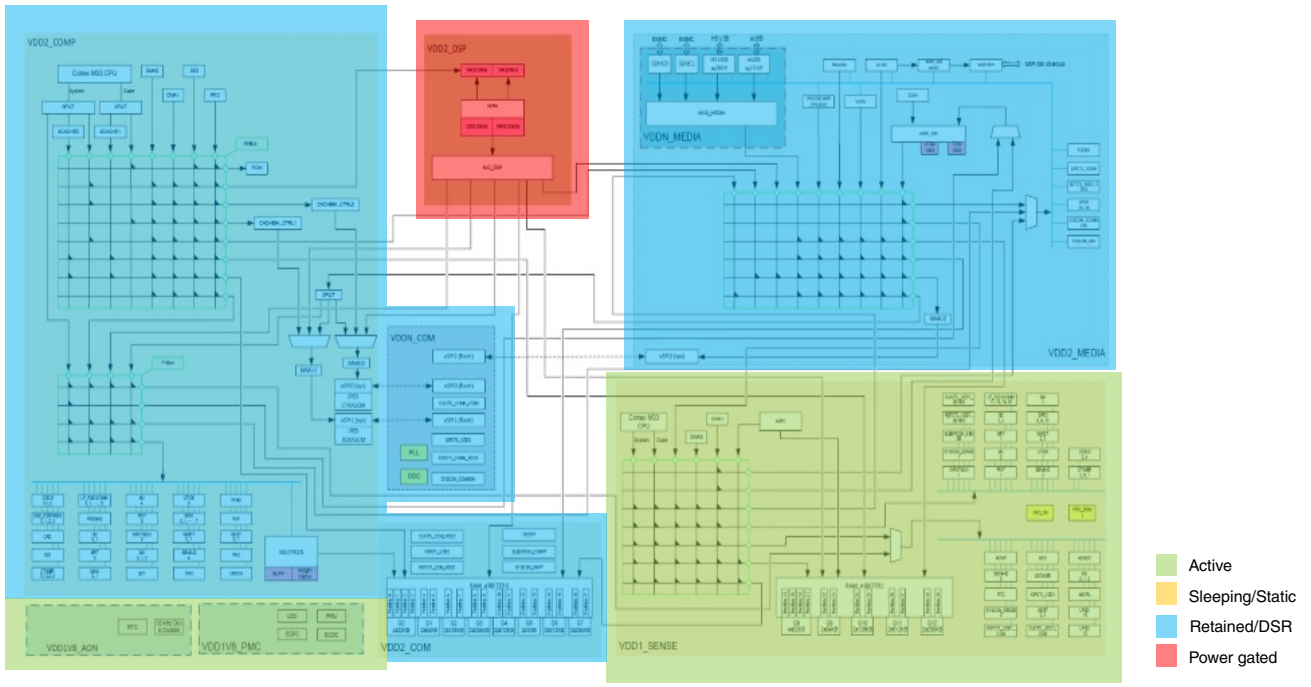


Figure 7. Compute DSR, Sense CoreMark

3.1.8.4 Compute DSR, CPU1 CM33 Sleep

The table below provides typical current numbers where the compute domain is in DSR and CPU1 in the sense domain is in Sleep.

SENSE_MAIN_CLK is sourced from FRO2 running at the frequency indicated for each row. HiFi4 is powered down, and HiFi 1 DSP is stalled.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.1 V. VDD2 = 0.5 V.

Body Bias: VDD2 RBB, VDD2SRAM RBB, VDD1 AFBB, VDD1SRAM NBB, VDDN RBB.

Data and code are located in SRAM partition 22.

Table 21. Compute DSR, CPU1 CM33 Sleep

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	6.73	—	mA	SENSE_MAIN_CLK = 250 MHz, VDD2 = 1.1 V
IVDD1	VDD1 supply current [1]	—	4.85	—	mA	SENSE_MAIN_CLK = 205 MHz, VDD2 = 1.0 V
IVDD1	VDD1 supply current [1]	—	3.35	—	mA	SENSE_MAIN_CLK = 160 MHz, VDD2 = 0.9 V

Table continues on the next page...

Table 21. Compute DSR, CPU1 CM33 Sleep*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	2.15	—	mA	SENSE_MAIN_CLK = 100 MHz, VDD2 = 0.8 V
IVDD1	VDD1 supply current [1]	—	1.09	—	mA	SENSE_MAIN_CLK = 45 MHz, VDD2 = 0.7 V
IVDD2	VDD2 supply current [1]	—	24.9	—	µA	—
IVDDN	VDDN supply current [1]	—	19.4	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	65.2	—	µA	FRO2 = 250 MHz
IVDD1V8	VDD1V8 supply current [1]	—	55.3	—	µA	FRO2 = 205 MHz
IVDD1V8	VDD1V8 supply current [1]	—	46.0	—	µA	FRO2 = 160 MHz
IVDD1V8	VDD1V8 supply current [1][2]	—	54.3	—	µA	FRO2 = 200 MHz
IVDD1V8	VDD1V8 supply current [1][3]	—	50.1	—	µA	FRO2 = 180 MHz
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][4]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][4]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][4]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[2] FRO is divided by 2 to get the 100 MHz COMPUTE_MAIN_CLK
[3] FRO is divided by 4 to get the 45 MHz COMPUTE_MAIN_CLK
[4] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

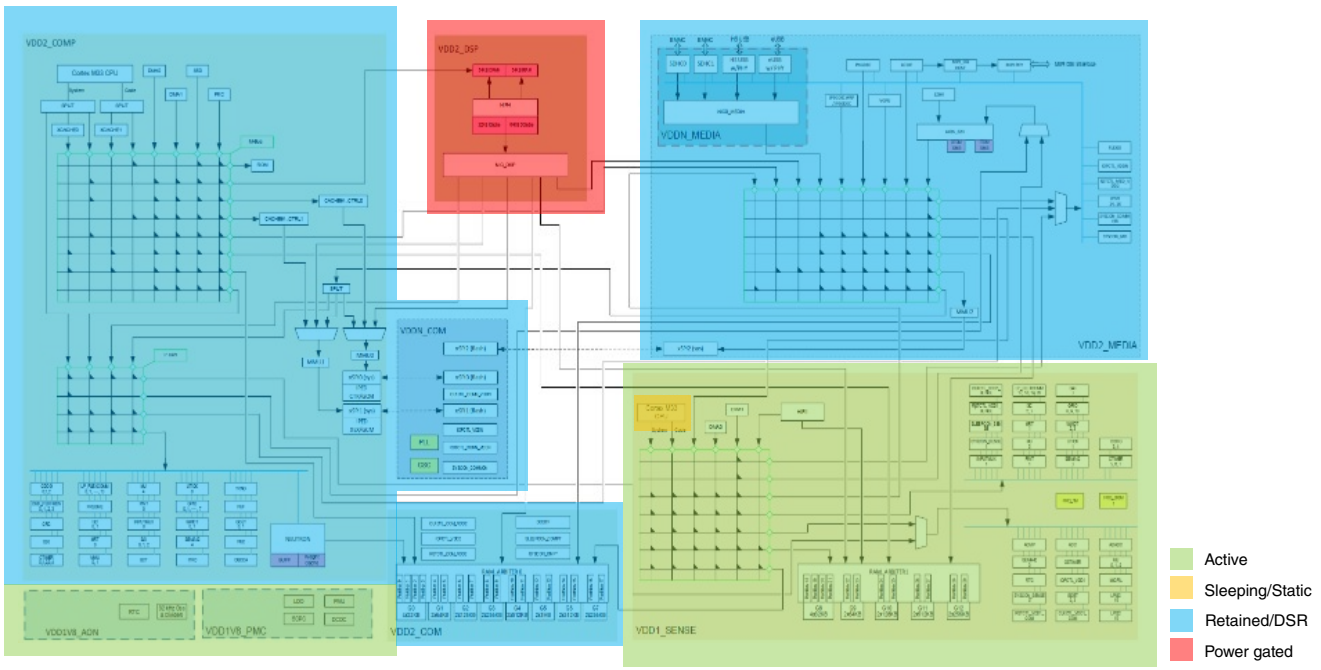


Figure 8. Compute DSR CPU1 Sleep

3.1.8.5 CPU0 CM33 Sleep, Sense Deep Sleep, HiFi 4 DSP FFT, HiFi 1 DSP stalled

The table below provides typical current numbers where CPU0 in the compute domain is in Sleep, the sense domain is in Deep Sleep, HiFi 4 DSP runs FFT, and HiFi 1 DSP is stalled.

DSP_CLK is sourced from FRO0 running at the frequency indicated for each row. COMPUTE_MAIN_CLK is 1 MHz sourced from 1M_LPOSC.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.1 V. VDD1 = 0.63 V.

Body Bias: VDD2 AFBB, VDD2SRAM NBB, VDD1 RBB, VDD1SRAM RBB, VDDN RBB.

HiFi 4 DSP data and code are located in SRAM partition 14.

Table 22. CPU0 CM33 Sleep, Sense Deep Sleep, HiFi 4 DSP FFT, HiFi 1 DSP stalled

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD2	VDD2 supply current [1]	—	87.52	—	mA	DSP_CLK = 325 MHz, VDD2 = 1.1 V
IVDD2	VDD2 supply current [1]	—	61.05	—	mA	DSP_CLK = 250 MHz, VDD2 = 1.0 V
IVDD2	VDD2 supply current [1]	—	41.87	—	mA	DSP_CLK = 192 MHz, VDD2 = 0.9 V
IVDD2	VDD2 supply current [1]	—	21.81	—	mA	DSP_CLK = 110 MHz, VDD2 = 0.8 V

Table continues on the next page...

Table 22. CPU0 CM33 Sleep, Sense Deep Sleep, HiFi 4 DSP FFT, HiFi 1 DSP stalled...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD2	VDD2 supply current [1]	—	8.27	—	mA	DSP_CLK = 45 MHz, VDD2 = 0.7 V
IVDD1	VDD1 supply current [1]	—	44	—	µA	—
IVDDN	VDDN supply current [1]	—	19.4	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	84.4	—	µA	FRO0 = 325 MHz
IVDD1V8	VDD1V8 supply current [1]	—	66.7	—	µA	FRO0 = 250 MHz
IVDD1V8	VDD1V8 supply current [1]	—	54.0	—	µA	FRO0 = 192 MHz
IVDD1V8	VDD1V8 supply current [1][2]	—	60.0	—	µA	FRO0 = 220 MHz
IVDD1V8	VDD1V8 supply current [1][3]	—	51.5	—	µA	FRO0 = 180 MHz
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][4]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][4]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][4]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[2] FRO is divided by 2 to get the 110 MHz COMPUTE_MAIN_CLK
[3] FRO is divided by 4 to get the 45 MHz COMPUTE_MAIN_CLK
[4] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

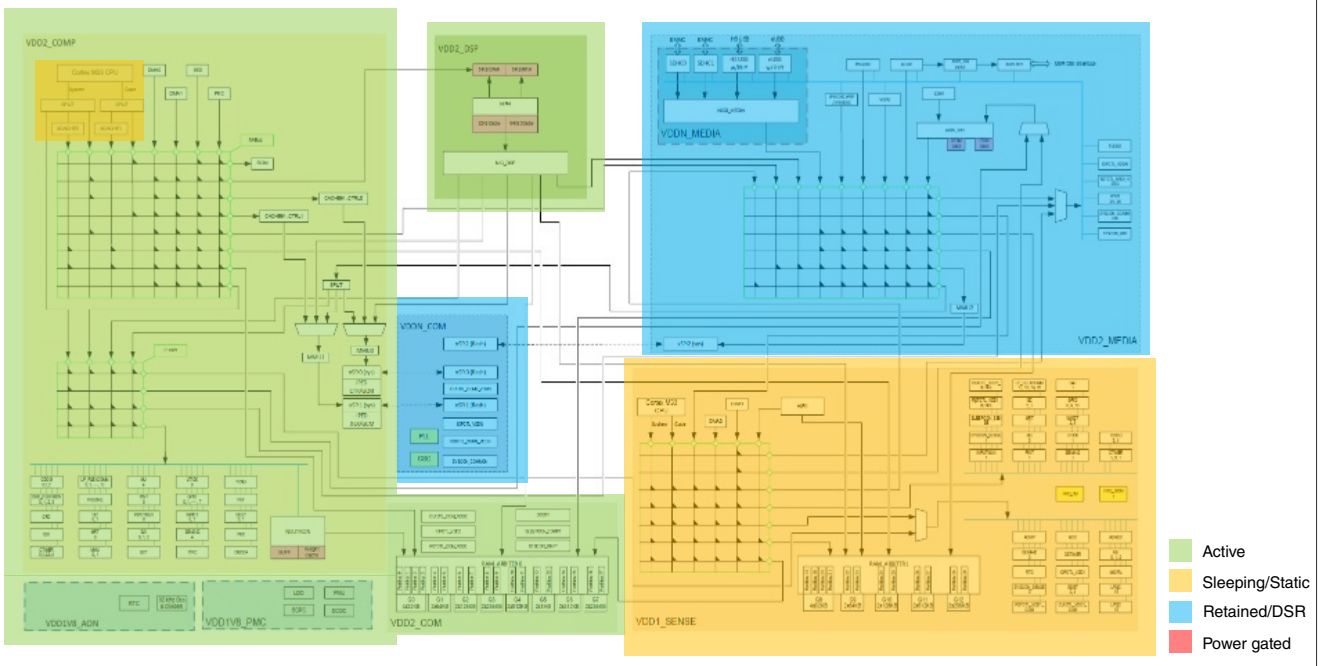


Figure 9. CPU0 CM33 Sleep, CPU1 Deep Sleep, HiFi 4 DSP FFT, HiFi 1 DSP stalled

3.1.8.6 Compute DSR, CPU1 CM33 Sleep, HiFi 4 DSP OFF, HiFi 1 DSP FFT

The table below provides typical current numbers where the compute domain is in DSR, and CPU1 in the sense domain is in Sleep, HiFi 4 DSP is powered down, and HiFi 1 DSP runs FFT.

SENSE_DSP_CLK is sourced from FRO2 running at the frequency indicated for each row. SENSE_MAIN_CLK is 1 MHz sourced from 1M_LPOSC.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.1 V. VDD2 = 0.5 V.

Body Bias: VDD2 RBB, VDD2SRAM RBB, VDD1 AFBB, VDD1SRAM NBB, VDDN RBB.

HiFi 1 DSP data and code are located in SRAM partition 27.

Table 23. Compute DSR, CPU1 CM33 Sleep, HiFi 4 DSP OFF, HiFi 1 DSP FFT

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	32.03	—	mA	SENSE_DSP_CLK = 250 MHz, VDD1 = 1.1 V
IVDD1	VDD1 supply current [1]	—	23.46	—	mA	SENSE_DSP_CLK = 205 MHz, VDD1 = 1.0 V
IVDD1	VDD1 supply current [1]	—	16.29	—	mA	SENSE_DSP_CLK = 160 MHz, VDD1 = 0.9 V

Table continues on the next page...

Table 23. Compute DSR, CPU1 CM33 Sleep, HiFi 4 DSP OFF, HiFi 1 DSP FFT*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	9.26	—	mA	SENSE_DSP_CLK = 100 MHz, VDD1 = 0.8 V
IVDD1	VDD1 supply current [1]	—	3.87	—	mA	SENSE_DSP_CLK = 45 MHz, VDD1 = 0.7 V
IVDD2	VDD2 supply current [1]	—	24.9	—	µA	—
IVDDN	VDDN supply current [1]	—	19.4	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	66.8	—	µA	FRO2 = 250 MHz
IVDD1V8	VDD1V8 supply current [1]	—	56.9	—	µA	FRO2 = 205 MHz
IVDD1V8	VDD1V8 supply current [1]	—	47.5	—	µA	FRO2 = 160 MHz
IVDD1V8	VDD1V8 supply current [1][2]	—	55.8	—	µA	FRO2 = 200 MHz
IVDD1V8	VDD1V8 supply current [1][3]	—	51.6	—	µA	FRO2 = 180 MHz
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][4]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][4]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][4]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[2] FRO is divided by 2 to get the 100 MHz COMPUTE_MAIN_CLK
[3] FRO is divided by 4 to get the 45 MHz COMPUTE_MAIN_CLK
[4] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

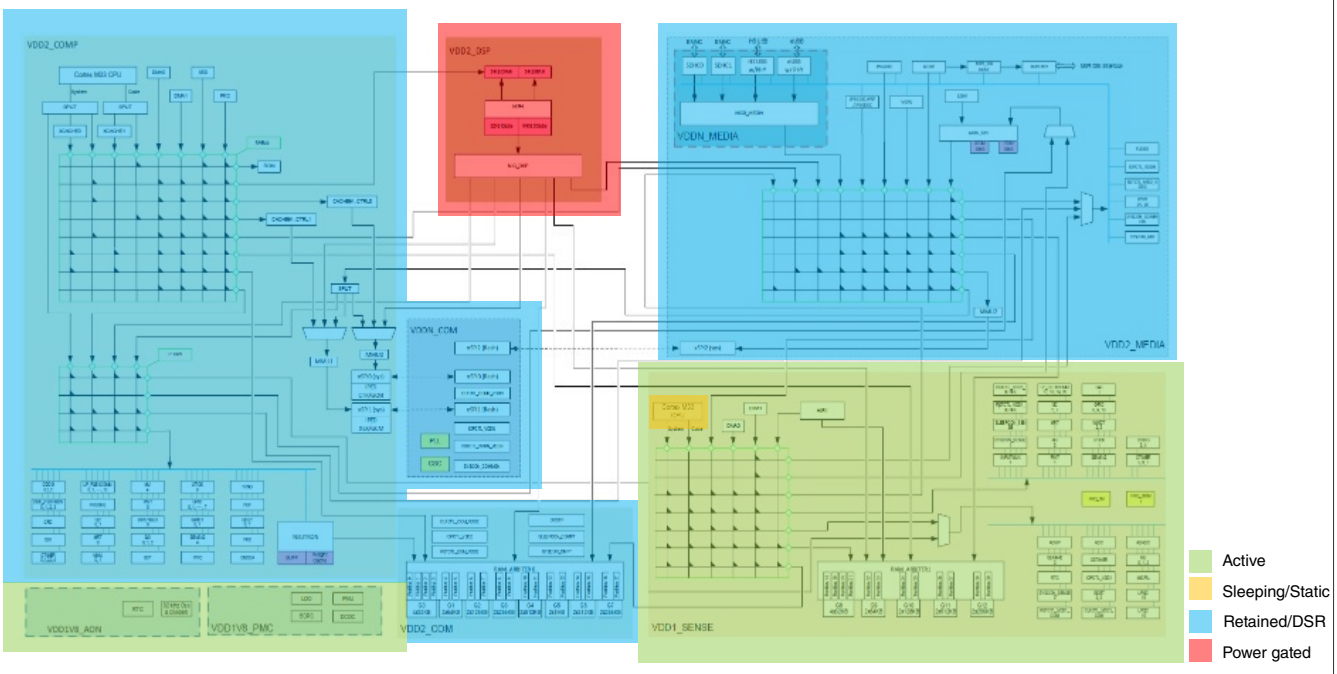


Figure 10. Compute DSR, CPU1 CM33 Sleep, HiFi 4 DSP OFF, HiFi 1 DSP FFT

3.1.8.7 Compute and Sense Dual Deep Sleep mode

The table below provides typical current numbers where compute and sense domain are in Deep Sleep mode.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 1.0 V. VDD2 = VDD1 = 0.63 V.

Body Bias: VDD2 RBB, VDD2SRAM RBB, VDD1 RBB, VDD1SRAM RBB, VDDN RBB.

Table 24. Compute and Sense Dual Deep Sleep mode

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	24	—	µA	SRAM (2 MB) retained. Array ON, periphery OFF
IVDD2	VDD2 supply current [1]	—	76	—	µA	SRAM (5.5 MB) retained. Array ON, periphery OFF
IVDDN	VDDN supply current [1]	—	13.5	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	9	—	µA	—
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.95	—	µA	OSC32K ON
IVDDIO_0	VDDIO supply current [1]	—	3	—	µA	—

Table continues on the next page...

Table 24. Compute and Sense Dual Deep Sleep mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][2]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][2]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][2]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through automatic test measurements using typical samples. Guaranteed by characterization, not tested in production.

[2] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

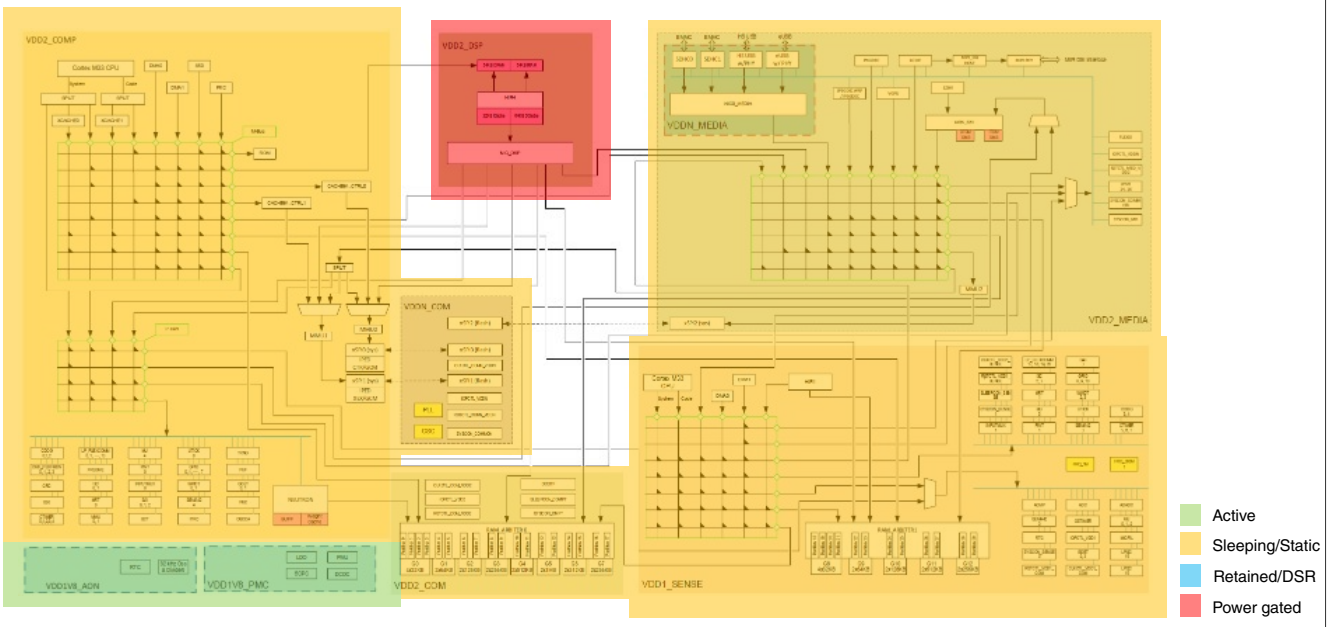


Figure 11. Compute and Sense Dual Deep Sleep

3.1.8.8 Compute and Sense Deep Sleep Async

The table below provides typical current numbers where compute and sense domain are in Deep Sleep Async.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 0.6 V. VDD2 = VDD1 = 0.5 V.

Body Bias: VDD2 RBB, VDD2SRAM RBB, VDD1 RBB, VDD1SRAM RBB, VDDN RBB.

Table 25. Compute and Sense Deep Sleep Async

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	13	—	µA	SRAM (2 MB) retained. Array ON, periphery OFF
IVDD2	VDD2 supply current [1]	—	40	—	µA	SRAM (5.5 MB) retained. Array ON, periphery OFF
IVDDN	VDDN supply current [1]	—	1.5	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	9	—	µA	—
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.95	—	µA	OSC32K ON
IVDDIO_0	VDDIO supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][2]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][2]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][2]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Maximum values are characterized through automatic test measurements using typical samples. Guaranteed by characterization, not tested in production.

[2] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

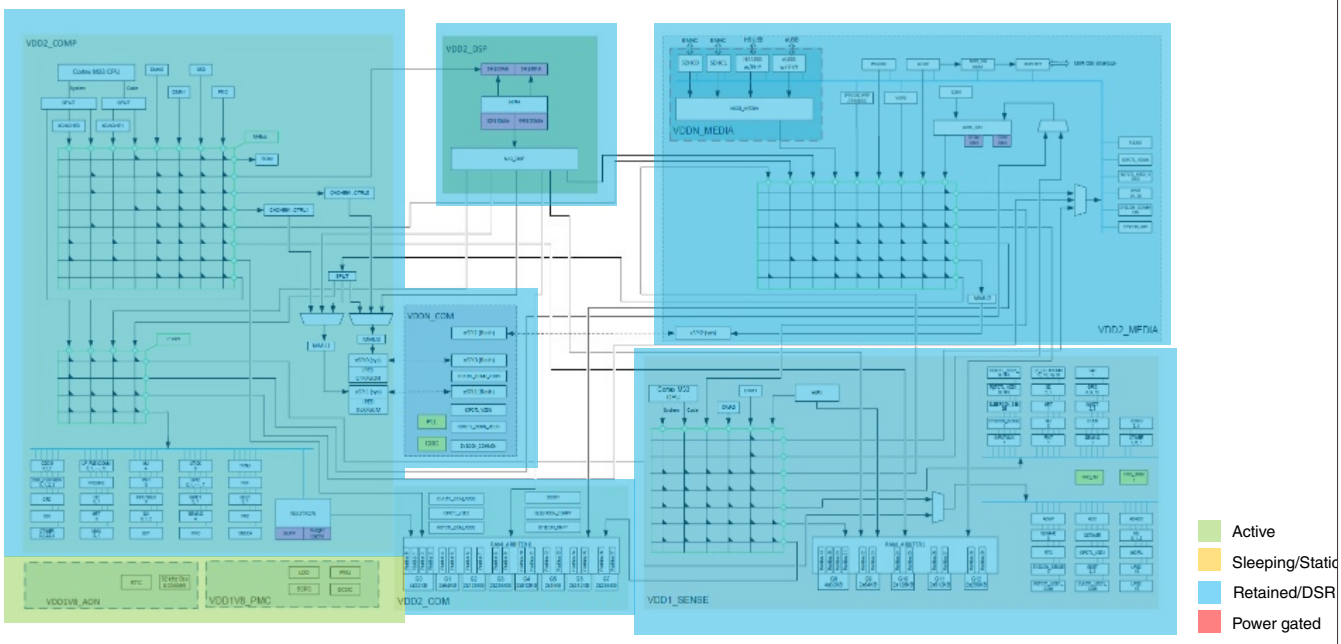


Figure 12. Compute and Sense Deep Sleep Async

3.1.8.9 Full DSR mode (FDSR)

The table below provides typical current numbers where the chip is in Full DSR (FDSR) mode.

Current is measured using an external supply for VDD2, VDD1, and VDDN (internal LDOs disabled). VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDIO_0/2/4/5/6 = VDD1V8_EUSB = VDDA_1V8 = VDD1V8_MIPI = VREFH_ANA18 = 1.8 V. VDD3V3_USB = 3.3 V. VDD1V2_EUSB = 1.2 V. VDDN = 0.6 V. VDD2 = VDD1 = 0.50 V.

Body Bias: VDD2 RBB, VDD2SRAM RBB, VDD1 RBB, VDD1SRAM RBB, VDDN RBB.

Table 26. Full DSR mode (FDSR)

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	9	—	µA	SRAM (2 MB) powered. Array ON, periphery OFF
IVDD2	VDD2 supply current [1]	—	30	—	µA	SRAM (5.5 MB) powered. Array ON, periphery OFF
IVDDN	VDDN supply current [1]	—	0.6	—	µA	—
IVDD1V8	VDD1V8 supply current [1]	—	9	—	µA	—
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.95	—	µA	OSC32K ON
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—

Table continues on the next page...

Table 26. Full DSR mode (FDSR)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDDIO_2	VDDIO_2 supply current [1]	—	0.2	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][2]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][2]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][2]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Maximum values are characterized through automatic test measurements using typical samples. Guaranteed by characterization, not tested in production.

[2] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

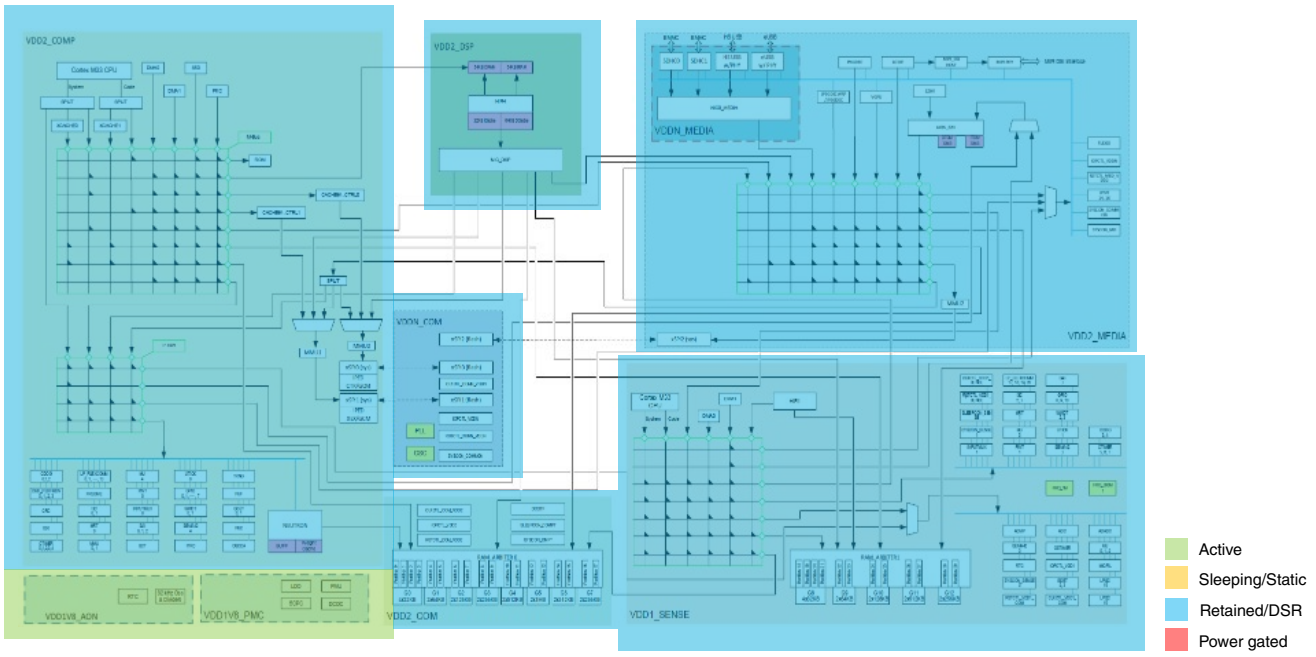


Figure 13. Full Deep Sleep Retention mode

3.1.8.10 Deep Power Down mode (DPD)

The table below provides typical current numbers where the chip is in Deep Power Down mode.

VDD1, VDD2, and VDDN are shut-off. VDD1V8_AO = VDDIO_AO = VDD1V8 = VDDA_1V8 = VDDIO_0/2/4/5/6 = 1.8 V.

Table 27. Deep Power Down mode (DPD)

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	0	—	µA	Shut-off
IVDD2	VDD2 supply current [1]	—	0	—	µA	Shut-off
IVDDN	VDDN supply current [1]	—	0	—	µA	Shut-off
IVDD1V8	VDD1V8 supply current [1]	—	9	—	µA	—
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.95	—	µA	OSC32K ON
IVDDIO_0	VDDIO_0 supply current [1]	—	3	—	µA	—
IVDDIO_2	VDDIO_2 supply current [1]	—	0.02	—	µA	—
IVDDIO_4	VDDIO_4 supply current [1]	—	0.6	—	µA	—
IVDDIO_5	VDDIO_5 supply current [1]	—	0.6	—	µA	—
IVDDIO_6	VDDIO_6 supply current [1]	—	0.4	—	µA	—
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.3	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0.1	—	µA	—
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0.1	—	µA	—
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][2]	—	0.01	—	µA	—
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][2]	—	0.05	—	µA	—
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	1	—	µA	—
IVREFH_ANA18	VREFH_ANA18 supply current [1][2]	—	0.01	—	µA	—

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through automatic test measurements using typical samples.

[2] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

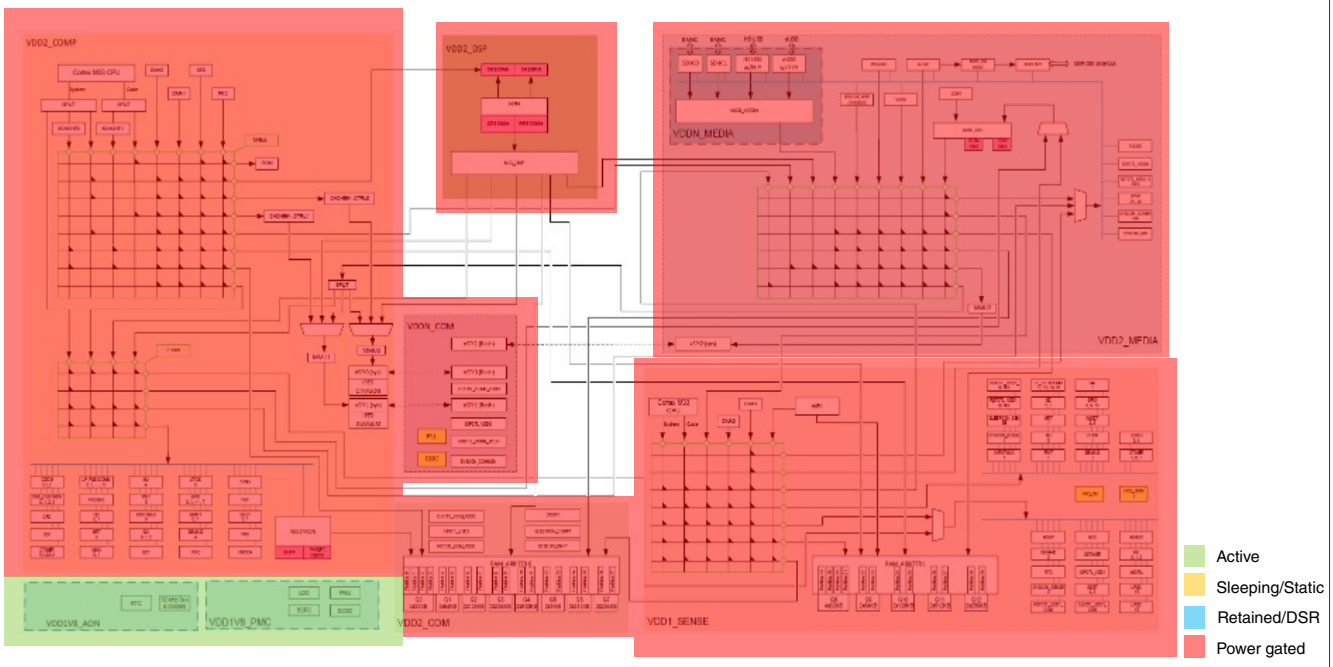


Figure 14. Deep Power Down (DPD) mode

3.1.8.11 Full Deep Power Down mode (FDPD)

The table below provides typical current numbers where the chip is in Full Deep Power Down mode.

VDD1V8_AO = 1.8 V. VDD1, VDD2, VDDN, VDD1V8, VDDIO_0/2/4/5/6, VDDIO_AO, VDDA_1V8, VDD1V8_MIPI, VDD1V2_EUSB, VDD1V8_EUSB, VDD3V3_USB, VREFH_ANA18 are shut-off.

Table 28. Full Deep Power Down mode (FDPD)

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDD1	VDD1 supply current [1]	—	0	—	µA	Shut-off
IVDD2	VDD2 supply current [1]	—	0	—	µA	Shut-off
IVDDN	VDDN supply current [1]	—	0	—	µA	Shut-off
IVDD1V8	VDD1V8 supply current [1]	—	0	—	µA	Shut-off
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.80	—	µA	OSC32K OFF
IVDD1V8_AO	VDD1V8_AO supply current [1]	—	0.95	—	µA	OSC32K ON
IVDDIO_0	VDDIO_0 supply current [1]	—	0	—	µA	Shut-off
IVDDIO_2	VDDIO_2 supply current [1]	—	0	—	µA	Shut-off
IVDDIO_4	VDDIO_4 supply current [1]	—	0	—	µA	Shut-off
IVDDIO_5	VDDIO_5 supply current [1]	—	0	—	µA	Shut-off
IVDDIO_6	VDDIO_6 supply current [1]	—	0	—	µA	Shut-off

Table continues on the next page...

Table 28. Full Deep Power Down mode (FDPD)...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IVDDIO_AO	VDDIO_AO supply current [1]	—	0.1	—	µA	—
IVDDA_1V8	VDDA_1V8 supply current [1]	—	0	—	µA	Shut-off
IVDD1V8_MIPI	VDD1V8_MIPI supply current [1]	—	0	—	µA	Shut-off
IVDD1V2_EUSB	VDD1V2_EUSB supply current [1][2]	—	0	—	µA	Shut-off
IVDD1V8_EUSB	VDD1V8_EUSB supply current [1][2]	—	0	—	µA	Shut-off
IVDD3V3_USB	VDD3V3_USB supply current [1]	—	0	—	µA	Shut-off
IVREFH_ANA18	VREFH_ANA18 supply current [1][2]	—	0	—	µA	Shut-off

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through automatic test measurements using typical samples.

[2] VREFH_ANA18, VDD1V2_EUSB, VDD1V8_EUSB are not available on WLCSP package. VREFH_ANA18 is connected to VDDA_1V8 on the WLCSP, so the sum of IVREFH_ANA18 and IVDDA_1V8 is the expected value for the WLCSP. EUSB is not supported in the WLCSP package, so the EUSB currents do not migrate to a different supply.

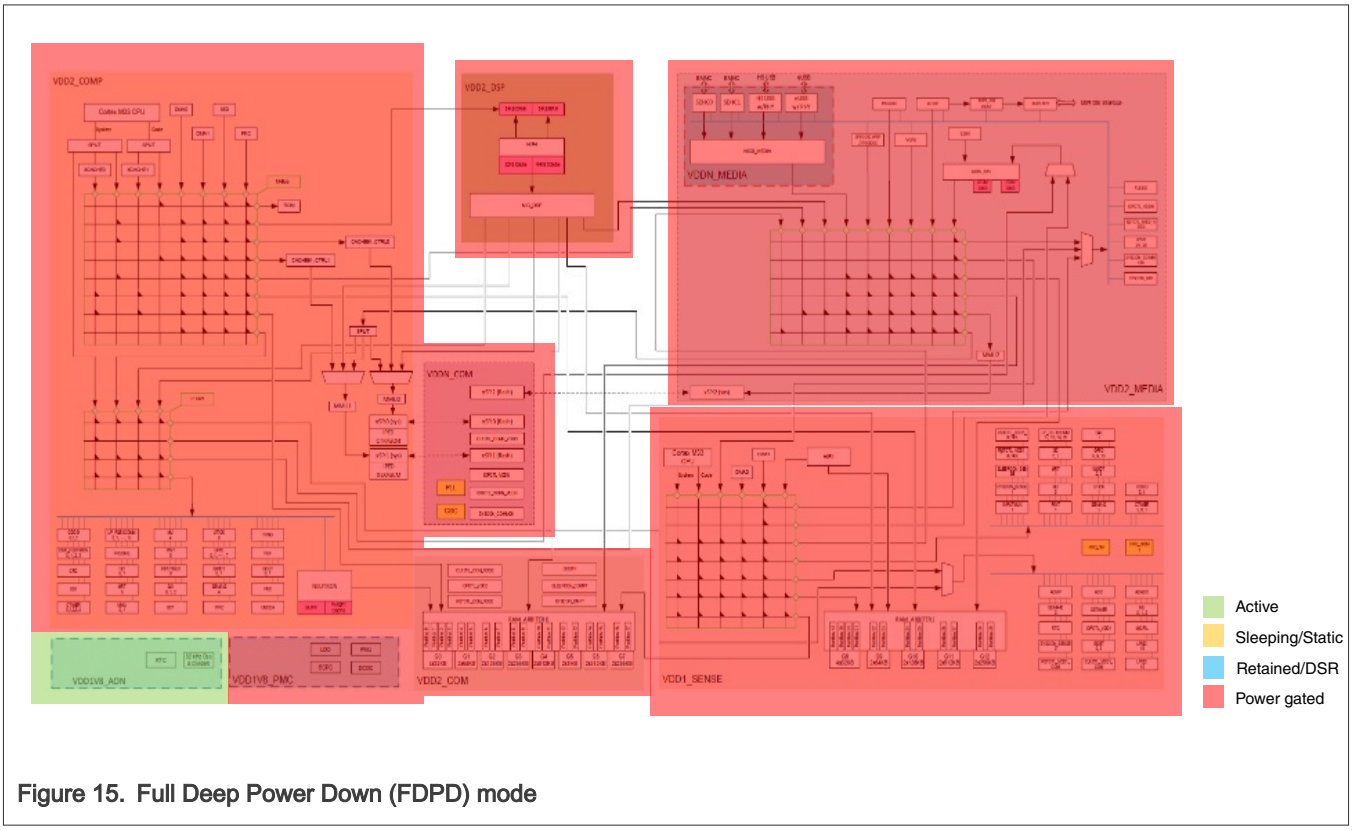


Figure 15. Full Deep Power Down (FDPD) mode

3.1.9 CoreMark data

Compiler settings: IAR C/C++ Compiler for Arm ver 9.40.2, optimization level 3, optimized for time on.

Arm Cortex-M33 in active mode, CoreMark code executed from SRAM (CPU0- P0, P4, and P16; CPU1- P18 and P26).

Table 29. CoreMark data

Symbol	Description	Min	Typ	Max	Unit	Condition
—	CoreMark Score: Arm Cortex-M33 in CPU0	—	3.97329	—	(Iterations/s) / MHz	PLL or FRO clock, XCACHE enabled, COMPUTE_MAIN_CLK = 325/297/264/198 MHz
—	CoreMark Score: Arm Cortex-M33 in CPU0	—	2.87139	—	(Iterations/s) / MHz	PLL or FRO clock, XCACHE disabled, COMPUTE_MAIN_CLK = 297 MHz
—	CoreMark Score: Arm Cortex-M33 in CPU1	—	4.00072	—	(Iterations/s) / MHz	FRO2 clock, SENSE_MAIN_CLK = 100 MHz

3.1.10 Wake-up time

Test condition: Low power configurations are completed with using the power API from the SDK software package available on nxp.com. Code runs from SRAM. The CPU0 core clock is sourced from FRO0. The CPU1 core clock is sourced from LPOSC. The wake-up time measured is the time between when PMIC_IRQN pin is triggered to wake the device up from the low power modes and when a GPIO output pin is set next to the WFI instruction. Device is powered by PMIC. The Mode Delay value (PMC_POWERCFG[MODEDLY]) is configured to 00b for a shorter wait time. PMIC ramp speed for Buck1(VDD2) (BUCK1CTRL[B1_RAMP]) is configured to 00b for a faster ramp. FRO Fast Startup bit (FRO_CNFG1[FSTUPEN]) is set to 1b for "FRO fast start", and 0b for "FRO normal start".

Following table lists the wake-time from different modes.

Table 30. Wake-up time

Symbol	Description	Min	Typ	Max	Unit	Condition
twake	CPU0 wake-up time	—	96	—	ns	From Sleep mode
twake	CPU0 wake-up time	—	140	—	µs	From Deep sleep mode, FRO0 normal start
twake	CPU0 wake-up time	—	96	—	µs	From Deep sleep mode, FRO0 fast start
twake	CPU0 wake-up time	—	60	—	µs	From Deep sleep mode, FRO0 on
twake	CPU0 wake-up time	—	187	—	µs	From Deep sleep retention mode
twake	CPU0 wake-up time	—	142	—	µs	From Sleep mode
twake	CPU1 wake-up time	—	191	—	µs	From Deep sleep mode, LPOSC off
twake	CPU1 wake-up time	—	96	—	µs	From Deep sleep mode, LPOSC on
twake	CPU1 wake-up time	—	223	—	µs	From Deep sleep retention mode

3.2 System power and clocks

3.2.1 Power sequence

3.2.1.1 Power-up sequence

Following power-up sequence must be followed for i.MX RT700 microcontrollers:

1. VDD1V8_AO must power up before or with VDD1V8.
2. VDD1V8 ramp up.
    a. If internal DCDC is used, VDD1V8_DCDC can share power source as VDD1V8.
3. VDDN (1.1 V by default) starts to ramp up.
    a. For internal DCDC use case, VDDN is supplied by LX_DCDC via a inductance, DCDC is configured to 1.1 V output by default. VDDN (LX_DCDC) ramp up in 50 µs after VDD1V8_DCDC ramp up.
    b. For external PMIC solution, VDDN is 1.1 V by default.
4. VDD1 (1.0 V) and VDD2 (1.0) ramp up by internal LDO.
   Note: *Internal LDO is on by default if VDD1 and VDD2 are supplied by external PMIC. User need to disable internal LDOs after system boot up.*
   Note: *Internal LDO is configured to VDD1 = 1.0 V, VDD2 = 1.0 V, external PMIC must follow this configuration.*
5. POR exit after VDDN, VDD1, and VDD2 stable.
6. FRO enabled and it starts clock generation operation.
7. Assert RESETN pin.
8. Fuse load.
9. After fuse load successfully, de-assert RESETN pin, external circuit can still assert RESETN pin to hold the reset stage.
10. Once RESETN pin is de-asserted, release system reset.
11. System boot up from ROM.

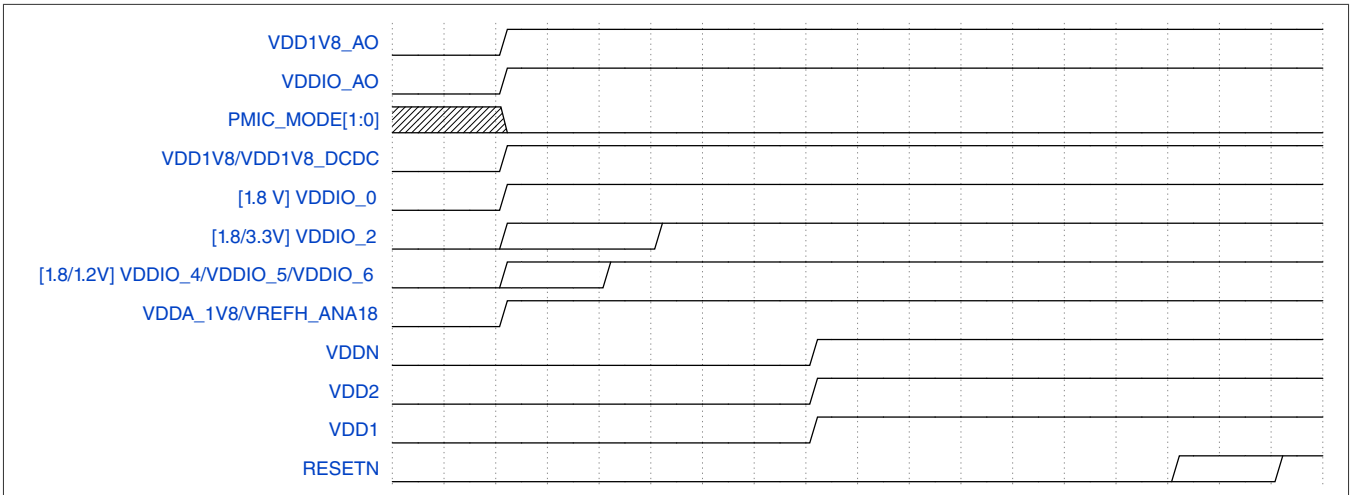


Figure 16. Power-up sequence using internal DCDC and internal LDO

Note: *VREFH_ANA18 is not available on WLCSP package.*
Note: *VDD3V3_USB, VDD1V8_EUSB, VDD1V2_EUSB can power ON or OFF at any time.*

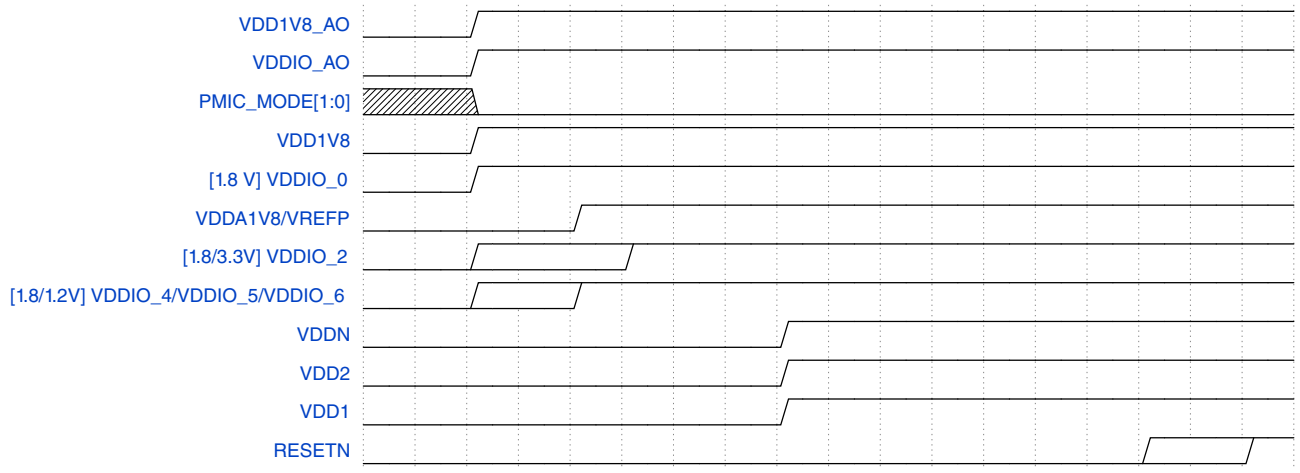


Figure 17. Power-up sequence using PMIC

3.2.1.2 Power-down sequence

When using external PMIC, power down the rails in following sequence: VDD1/VDD2, VDDN, and then VDD1V8.

For internal LDO, put device in full deep power-down mode and then switch off main power supply

3.2.2 Power Management Controller (PMC) specifications

Table 31. Power Management Controller (PMC) specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
TEMPS_ ACCURACY	Temp sensor accuracy	-3	—	+3	°C	At field after single-temperature calibration
POR_VDD1V8_D	POR VDD1V8 de-assertion (rise) threshold trimmed	1.598	1.637	1.677	V	Bandgap trimmed value
POR_VDD1V8_A	POR VDD1V8 assertion (fall) threshold trimmed	1.576	1.615	1.654	V	Bandgap trimmed value
HVD_VDD1V8_A	HVD VDD1V8 assertion (rise) threshold trimmed	2.066	2.115	2.165	V	Bandgap trimmed value
HVD_VDD1V8_D	HVD VDD1V8 de-assertion (fall) threshold trimmed	2.036	2.085	2.134	V	Bandgap trimmed value
POR_VDD_T_ ACCURACY	POR accuracy for VDD1, VDD2, VDDN trimmed	POR x -2% -7mV	—	POR x +2% +7mV	—	Bandgap trimmed value
POR_VDD_HYS	Hysteresis for POR on VDD1, VDD2, and VDDN	27	30	33	mV	—
POR_VDD_ ASSERTION_ RANGE	POR assertion range for VDD1, VDD2, and VDDN	0.4	—	0.71	V	Nominal steps not accounting for variance, 32 steps, 10 mV

Table continues on the next page...

Table 31. Power Management Controller (PMC) specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
HVD_VDD_A	HVD VDD1, VDD2, VDDN assertion (rise) threshold trimmed	1.218	1.25	1.282	V	Bandgap trimmed value
HVD_VDD_D	HVD VDD1, VDD2, VDDN de-assertion (fall) threshold trimmed	1.189	1.22	1.252	V	Bandgap trimmed value
LVD_VDD_T_ ACCURACY	LVD accuracy for VDD1, VDD2, VDDN trimmed	LVD x -2% -7mV	—	LVD x +2% +7mV	—	Bandgap trimmed value
LVD_VDD_HYS	Hysteresis for LVD on VDD1, VDD2, and VDDN	27	30	33	mV	—
LVD_VDD_ ASSERTION_ RANGE	LVD assertion range for VDD1, VDD2, and VDDN	0.5	—	1.13	V	Nominal steps not accounting for variance, 64 steps, 10 mV

3.2.3 PMC LVD specifications

3.2.3.1 Rising LVD trip point for POR (Untrimmed default rising trip)

Table 32. Rising LVD trip point for POR (Untrimmed default rising trip)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	VDD1/VDD2	885	930	975	mV	—
—	VDDN	924	970	1016	mV	—

3.2.3.2 Rising LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)

Table 33. Rising LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{LVD_R0}	Level0 rising (*lvl* = 0)	512	530	548	mV	—
V_{LVD_R1}	Level0 rising (*lvl* = 1)	522	540	558	mV	—
V_{LVD_R2}	Level0 rising (*lvl* = 2)	532	550	568	mV	—
V_{LVD_R3}	Level0 rising (*lvl* = 3)	542	560	578	mV	—
V_{LVD_R4}	Level0 rising (*lvl* = 4)	552	570	588	mV	—
V_{LVD_R5}	Level0 rising (*lvl* = 5)	561	580	599	mV	—
V_{LVD_R6}	Level0 rising (*lvl* = 6)	571	590	609	mV	—
V_{LVD_R7}	Level0 rising (*lvl* = 7)	581	600	619	mV	—
V_{LVD_R8}	Level0 rising (*lvl* = 8)	591	610	629	mV	—
V_{LVD_R9}	Level0 rising (*lvl* = 9)	601	620	639	mV	—

Table continues on the next page...

Table 33. Rising LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{LVD_R10}	Level0 rising (*lvl* = 10)	610	630	650	mV	—
V_{LVD_R11}	Level0 rising (*lvl* = 11)	620	640	660	mV	—
V_{LVD_R12}	Level0 rising (*lvl* = 12)	630	650	670	mV	—
V_{LVD_R13}	Level0 rising (*lvl* = 13)	640	660	680	mV	—
V_{LVD_R14}	Level0 rising (*lvl* = 14)	650	670	690	mV	—
V_{LVD_R15}	Level0 rising (*lvl* = 15)	659	680	701	mV	—
V_{LVD_R16}	Level0 rising (*lvl* = 16)	669	690	711	mV	—
V_{LVD_R17}	Level0 rising (*lvl* = 17)	679	700	721	mV	—
V_{LVD_R18}	Level0 rising (*lvl* = 18)	689	710	731	mV	—
V_{LVD_R19}	Level0 rising (*lvl* = 19)	699	720	741	mV	—
V_{LVD_R20}	Level0 rising (*lvl* = 20)	708	730	752	mV	—
V_{LVD_R21}	Level0 rising (*lvl* = 21)	718	740	762	mV	—
V_{LVD_R22}	Level0 rising (*lvl* = 22)	728	750	772	mV	—
V_{LVD_R23}	Level0 rising (*lvl* = 23)	738	760	782	mV	—
V_{LVD_R24}	Level0 rising (*lvl* = 24)	748	770	792	mV	—
V_{LVD_R25}	Level0 rising (*lvl* = 25)	757	780	803	mV	—
V_{LVD_R26}	Level0 rising (*lvl* = 26)	767	790	813	mV	—
V_{LVD_R27}	Level0 rising (*lvl* = 27)	777	800	823	mV	—
V_{LVD_R28}	Level0 rising (*lvl* = 28)	787	810	833	mV	—
V_{LVD_R29}	Level0 rising (*lvl* = 29)	797	820	843	mV	—
V_{LVD_R30}	Level0 rising (*lvl* = 30)	806	830	854	mV	—
V_{LVD_R31}	Level0 rising (*lvl* = 31)	816	840	864	mV	—
V_{LVD_R32}	Level0 rising (*lvl* = 32)	826	850	874	mV	—
V_{LVD_R33}	Level0 rising (*lvl* = 33)	836	860	884	mV	—
V_{LVD_R34}	Level0 rising (*lvl* = 34)	846	870	894	mV	—
V_{LVD_R35}	Level0 rising (*lvl* = 35)	855	880	905	mV	—
V_{LVD_R36}	Level0 rising (*lvl* = 36)	865	890	915	mV	—
V_{LVD_R37}	Level0 rising (*lvl* = 37)	875	900	925	mV	—
V_{LVD_R38}	Level0 rising (*lvl* = 38)	885	910	935	mV	—
V_{LVD_R39}	Level0 rising (*lvl* = 39)	895	920	945	mV	—
V_{LVD_R40}	Level0 rising (*lvl* = 40)	904	930	956	mV	—
V_{LVD_R41}	Level0 rising (*lvl* = 41)	914	940	966	mV	—

Table continues on the next page...

Table 33. Rising LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{LVD_R42}	Level0 rising (*lvl* = 42)	924	950	976	mV	—
V_{LVD_R43}	Level0 rising (*lvl* = 43)	934	960	986	mV	—
V_{LVD_R44}	Level0 rising (*lvl* = 44)	944	970	996	mV	—
V_{LVD_R45}	Level0 rising (*lvl* = 45)	953	980	1007	mV	—
V_{LVD_R46}	Level0 rising (*lvl* = 46)	963	990	1017	mV	—
V_{LVD_R47}	Level0 rising (*lvl* = 47)	973	1000	1027	mV	—
V_{LVD_R48}	Level0 rising (*lvl* = 48)	983	1010	1037	mV	—
V_{LVD_R49}	Level0 rising (*lvl* = 49)	993	1020	1047	mV	—
V_{LVD_R50}	Level0 rising (*lvl* = 50)	1002	1030	1058	mV	—
V_{LVD_R51}	Level0 rising (*lvl* = 51)	1012	1040	1068	mV	—
V_{LVD_R52}	Level0 rising (*lvl* = 52)	1022	1050	1078	mV	—
V_{LVD_R53}	Level0 rising (*lvl* = 53)	1032	1060	1088	mV	—
V_{LVD_R54}	Level0 rising (*lvl* = 54)	1042	1070	1098	mV	—
V_{LVD_R55}	Level0 rising (*lvl* = 55)	1051	1080	1109	mV	—
V_{LVD_R56}	Level0 rising (*lvl* = 56)	1061	1090	1119	mV	—
V_{LVD_R57}	Level0 rising (*lvl* = 57)	1071	1100	1129	mV	—
V_{LVD_R58}	Level0 rising (*lvl* = 58)	1081	1110	1139	mV	—
V_{LVD_R59}	Level0 rising (*lvl* = 59)	1091	1120	1149	mV	—
V_{LVD_R60}	Level0 rising (*lvl* = 60)	1100	1130	1160	mV	—
V_{LVD_R61}	Level0 rising (*lvl* = 61)	1110	1140	1170	mV	—
V_{LVD_R62}	Level0 rising (*lvl* = 62)	1120	1150	1180	mV	—
V_{LVD_R63}	Level0 rising (*lvl* = 63)	1130	1160	1190	mV	—

3.2.3.3 Falling LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)

Table 34. Falling LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{LVD_F0}	Level0 falling (*lvl* = 0)	483	500	517	mV	—
V_{LVD_F1}	Level1 falling (*lvl* = 1)	493	510	527	mV	—
V_{LVD_F2}	Level2 falling (*lvl* = 2)	503	520	537	mV	—
V_{LVD_F3}	Level3 falling (*lvl* = 3)	512	530	548	mV	—
V_{LVD_F4}	Level4 falling (*lvl* = 4)	522	540	558	mV	—
V_{LVD_F5}	Level5 falling (*lvl* = 5)	532	550	568	mV	—
V_{LVD_F6}	Level6 falling (*lvl* = 6)	542	560	578	mV	—

Table continues on the next page...

Table 34. Falling LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{LVD_F7}	Level7 falling (*lvl* = 7)	552	570	588	mV	—
V_{LVD_F8}	Level8 falling (*lvl* = 8)	561	580	599	mV	—
V_{LVD_F9}	Level9 falling (*lvl* = 9)	571	590	609	mV	—
V_{LVD_F10}	Level10 falling (*lvl* = 10)	581	600	619	mV	—
V_{LVD_F11}	Level11 falling (*lvl* = 11)	591	610	629	mV	—
V_{LVD_F12}	Level12 falling (*lvl* = 12)	601	620	639	mV	—
V_{LVD_F13}	Level13 falling (*lvl* = 13)	610	630	650	mV	—
V_{LVD_F14}	Level14 falling (*lvl* = 14)	620	640	660	mV	—
V_{LVD_F15}	Level15 falling (*lvl* = 15)	630	650	670	mV	—
V_{LVD_F16}	Level16 falling (*lvl* = 16)	640	660	680	mV	—
V_{LVD_F17}	Level17 falling (*lvl* = 17)	650	670	690	mV	—
V_{LVD_F18}	Level18 falling (*lvl* = 18)	659	680	701	mV	—
V_{LVD_F19}	Level19 falling (*lvl* = 19)	669	690	711	mV	—
V_{LVD_F20}	Level20 falling (*lvl* = 20)	679	700	721	mV	—
V_{LVD_F21}	Level21 falling (*lvl* = 21)	689	710	731	mV	—
V_{LVD_F22}	Level22 falling (*lvl* = 22)	699	720	741	mV	—
V_{LVD_F23}	Level23 falling (*lvl* = 23)	708	730	752	mV	—
V_{LVD_F24}	Level24 falling (*lvl* = 24)	718	740	762	mV	—
V_{LVD_F25}	Level25 falling (*lvl* = 25)	728	750	772	mV	—
V_{LVD_F26}	Level26 falling (*lvl* = 26)	738	760	782	mV	—
V_{LVD_F27}	Level27 falling (*lvl* = 27)	748	770	792	mV	—
V_{LVD_F28}	Level28 falling (*lvl* = 28)	757	780	803	mV	—
V_{LVD_F29}	Level29 falling (*lvl* = 29)	767	790	813	mV	—
V_{LVD_F30}	Level30 falling (*lvl* = 30)	777	800	823	mV	—
V_{LVD_F31}	Level31 falling (*lvl* = 31)	787	810	833	mV	—
V_{LVD_F32}	Level32 falling (*lvl* = 32)	797	820	843	mV	—
V_{LVD_F33}	Level33 falling (*lvl* = 33)	806	830	854	mV	—
V_{LVD_F34}	Level34 falling (*lvl* = 34)	816	840	864	mV	—
V_{LVD_F35}	Level35 falling (*lvl* = 35)	826	850	874	mV	—
V_{LVD_F36}	Level36 falling (*lvl* = 36)	836	860	884	mV	—
V_{LVD_F37}	Level37 falling (*lvl* = 37)	846	870	894	mV	—
V_{LVD_F38}	Level38 falling (*lvl* = 38)	855	880	905	mV	—

Table continues on the next page...

Table 34. Falling LVD trip point for POR (Trimmed for VDD1/VDD2/VDDN)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{LVD_F39}	Level39 falling (*lvl* = 39)	865	890	915	mV	—
V_{LVD_F40}	Level40 falling (*lvl* = 40)	875	900	925	mV	—
V_{LVD_F41}	Level41 falling (*lvl* = 41)	885	910	935	mV	—
V_{LVD_F42}	Level42 falling (*lvl* = 42)	895	920	945	mV	—
V_{LVD_F43}	Level43 falling (*lvl* = 43)	904	930	956	mV	—
V_{LVD_F44}	Level44 falling (*lvl* = 44)	914	940	966	mV	—
V_{LVD_F45}	Level45 falling (*lvl* = 45)	924	950	976	mV	—
V_{LVD_F46}	Level46 falling (*lvl* = 46)	934	960	986	mV	—
V_{LVD_F47}	Level47 falling (*lvl* = 47)	944	970	996	mV	—
V_{LVD_F48}	Level48 falling (*lvl* = 48)	953	980	1007	mV	—
V_{LVD_F49}	Level49 falling (*lvl* = 49)	963	990	1017	mV	—
V_{LVD_F50}	Level50 falling (*lvl* = 50)	973	1000	1027	mV	—
V_{LVD_F51}	Level51 falling (*lvl* = 51)	983	1010	1037	mV	—
V_{LVD_F52}	Level52 falling (*lvl* = 52)	993	1020	1047	mV	—
V_{LVD_F53}	Level53 falling (*lvl* = 53)	1002	1030	1058	mV	—
V_{LVD_F54}	Level54 falling (*lvl* = 54)	1012	1040	1068	mV	—
V_{LVD_F55}	Level55 falling (*lvl* = 55)	1022	1050	1078	mV	—
V_{LVD_F56}	Level56 falling (*lvl* = 56)	1032	1060	1088	mV	—
V_{LVD_F57}	Level57 falling (*lvl* = 57)	1042	1070	1098	mV	—
V_{LVD_F58}	Level58 falling (*lvl* = 58)	1051	1080	1109	mV	—
V_{LVD_F59}	Level59 falling (*lvl* = 59)	1061	1090	1119	mV	—
V_{LVD_F60}	Level60 falling (*lvl* = 60)	1071	1100	1129	mV	—
V_{LVD_F61}	Level61 falling (*lvl* = 61)	1081	1110	1139	mV	—
V_{LVD_F62}	Level62 falling (*lvl* = 62)	1091	1120	1149	mV	—
V_{LVD_F63}	Level63 falling (*lvl* = 63)	1100	1130	1160	mV	—

3.2.4 DCDC electrical specifications

Table 35. DCDC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Vlx_dcdc	Output voltage	0.5	—	1.1	V	—
—	Output voltage accuracy	-5	—	5	%	—
Iload	Output current (HP mode)	—	—	250	mA	—
Iload_lp	Output Current (LP mode)	—	—	200	µA	Cyclic wakeup mode

Table continues on the next page...

Table 35. DCDC electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Il,max	Maximum inductor current	—	450	—	mA	—
η	Efficiency	—	92	—	%	VDD1V8_DCDC = 1.8 V, Vout = 1.1 V, Iload = 150 mA
Fsw	Switching frequency [1]	—	2.2	—	MHz	VDD1V8_DCDC = 1.8 V, Vout = 1.1 V, Iload = 150 mA
Cout	Output Capacitance	3.76	4.7	9.4	µF	—
L	Inductance	1.76	2.2	2.64	µH	—
Ioc_hp	Overcurrent detection threshold (HP mode)	—	—	250	mA	—
Ioc_lp	Overcurrent detection threshold (LP mode)	—	—	25	mA	—

[1] The DCDC will automatically switch between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) based on the DCDC load. At higher loads (Iload~ 150 mA), CCM mode is used. For lower loads, DCM mode is used.

3.2.5 Switched Capacitor Power Converter (SCPC) electrical specifications

Table 36. Switched Capacitor Power Converter (SCPC) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Vout	Output range	0.50	0.52	0.54	V	—
Vout_ripple	Output voltage ripple	—	< 20	—	mVpp	—
Iload_scpc_150u	Output current in VDD_SENSE domain	—	—	150	µA	—
Iload_scpc_300u	Output current in VDD_COMP domain	—	—	300	µA	—
η	Power efficiency	—	65	—	%	—
Ioc_scpc_150u	Overcurrent detection in VDD_SENSE domain	150	—	—	µA	—
Ioc_scpc_300u	Overcurrent detection in VDD_COMP domain	300	—	—	µA	—

3.2.6 LDO VDD2 250 mA regulator specifications

LDO VDD2 250 mA regulator is used to provide power for VDD2.

Table 37. LDO VDD2 250 mA regulator specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Cload	Load capacitor	0.8	1	1.2	µF	—
Ivdd_hp	Current consumption at room temperature	—	300	—	µA	HP mode

Table continues on the next page...

Table 37. LDO VDD2 250 mA regulator specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdd_byp	Current consumption at room temperature	—	—	5	µA	Bypass mode
Ivdd_lp	Current consumption at room temperature	—	—	5	µA	LP mode
Vout	Programmable output voltage range	0.5	—	1.0	V	Regulation mode
Vout_step	Programmable output voltage step	—	12.5	—	mV	Regulation mode
Vout_acc	Output voltage accuracy	-5	—	+5	%	HP/LP mode
Vout_byp	Output voltage range in bypass mode	0.8	—	1.05	V	—
Vreg_drop	Voltage drop between input voltage and output voltage in regulation mode	100	—	—	mV	—
Vby_drop	Voltage drop between input voltage and output voltage in bypass mode	—	—	50	mV	Iload < 250 mA
Ileak	Leakage current of power device in off mode	—	—	200	nA	25°C VDDN = 0.8 V Vout = 0 V
Iouthp	Output current capability in HP regulation mode or bypass mode	—	—	250	mA	0.9 < Vout < 1.0
Iouthp	Output current capability in HP regulation mode or bypass mode	—	—	160	mA	0.8 < Vout < 0.9
Iouthp	Output current capability in HP regulation mode	—	—	80	mA	0.7 < Vout < 0.8
Iouthp	Output current capability in HP regulation mode	—	—	30	mA	0.6 < Vout < 0.7
Iouthp	Output current capability in HP regulation mode	—	—	3	mA	0.5 < Vout < 0.6
Ioutlp	Output current capability in LP regulation mode	—	—	5	mA	0.6 < Vout < 0.8
Ioutlp	Output current capability in LP regulation mode	—	—	3	mA	0.5 < Vout < 0.6
LR	Load regulation	—	—	40	µV/mA	Regulation mode
Vout_ripple	Output voltage ripple	—	—	5	mV	HP regulation mode / Peak-to-peak value
Vout_ripple	Output voltage ripple	—	—	15	mV	LP regulation mode / Peak-to-peak value

Table continues on the next page...

Table 37. LDO VDD2 250 mA regulator specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
PSRR	Power rejection ration in regulation mode	—	60	—	dB	DC
PSRR	Power rejection ration in regulation mode	—	40	—	dB	From DC to 2 MHz
RR	Output voltage ramping rate	50	—	—	mV/µs	Ramp up
RR	Output voltage ramping rate	—	Iout/ Cload	—	mV/µs	Ramp down
Iinrush	Output current limitation	—	—	180	mA	—

3.2.7 LDO VDD1 50 mA regulator specifications

LDO VDD1 50 mA regulator is used to provide power for VDD1.

Table 38. LDO VDD1 50 mA regulator specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Cload	Load capacitor	0.8	1	1.2	µF	—
Ivdd_hp	Current consumption at room temperature	—	300	—	µA	HP mode
Ivdd_byp	Current consumption at room temperature	—	—	5	µA	Bypass mode
Ivdd_lp	Current consumption at room temperature	—	—	5	µA	LP regulation mode
Vout	Programmable output voltage range	0.5	—	1	V	Regulation mode
Vout_step	Programmable output voltage step	—	12.5	—	mV	Regulation mode
Vout_acc	Output voltage accuracy	95	—	105	%	HP/LP mode
Vout_byp	Output voltage range in bypass mode	0.8	—	1.05	V	—
Vreg_drop	Voltage drop between input voltage and output voltage in regulation mode	100	—	—	mV	—
Vby_drop	Voltage drop between input voltage and output voltage in bypass mode	—	—	50	mV	Iload < 50 mA
Ileak	Leakage current of power device in off mode	—	—	40	nA	25 °C VDDN = 0.8 V, Vout = 0 V
Iouthp	Output current capability in HP regulation mode/bypass mode	—	—	50	mA	0.9 < Vout < 1.0

Table continues on the next page...

Table 38. LDO VDD1 50 mA regulator specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Iouthp	Output current capability in HP regulation mode/bypass mode	—	—	32	mA	0.8 < Vout < 0.9
Iouthp	Output current capability in HP regulation mode	—	—	16	mA	0.7 < Vout < 0.8
Iouthp	Output current capability in HP regulation mode	—	—	6	mA	0.6 < Vout < 0.7
Iouthp	Output current capability in HP regulation mode	—	—	0.6	mA	0.5 < Vout < 0.6
Ioutlp	Output current capability in LP regulation mode	—	—	1	mA	0.6 < Vout < 0.8
Ioutlp	Output current capability in LP regulation mode	—	—	0.6	mA	0.5 < Vout < 0.6
LR	Load regulation	—	—	200	µV/mA	Regulation mode
PSRR	Power rejection ratio in regulation mode	—	60	—	dB	DC
PSRR	Power rejection ratio in regulation mode	—	40	—	dB	From DC to 2 MHz
Vpowerok	Power ok flag trip point	—	Vout - 0.05	—	V	—
RR	Output voltage ramping rate	10	—	—	mV/µs	Ramp up
RR	Output voltage ramping rate	—	Iout/ Cload	—	mV/µs	Ramp down
Iinrush	Output current limitation	—	—	36	mA	—

3.2.8 Recommended NXP PMIC

NXP PMIC PCA9422 is recommended as the external power supply option for RT700 family. For more information about PCA9422, please visit the PCA9422 product webpage or contact with NXP local representative.

3.2.9 Free-running oscillator (FRO) specifications

AFBB is enabled. The logic in VDD1/VDD2 domain requires higher VDD1/VDD2 voltage to be clocked at a certain frequency. See General operating conditions for specific Max Freq vs VDDCORE limits.

Typical ratings are not guaranteed. The values listed are at room temperature (25°C), nominal supply voltages.

Table 39. Free-running oscillator (FRO) specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD1V8	VDD1V8 Analog supply voltage	1.71	1.8	1.89	V	—
VDD1/VDD2	VDD1/VDD2 Digital supply voltage	0.7	0.8	1.155	V	—
FFRO0/2	FRO0 and FRO2 frequency	150	—	325	MHz	—

Table continues on the next page...

Table 39. Free-running oscillator (FRO) specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
FFRO1	FRO1 fixed frequency [1]	—	192	—	MHz	—
ΔfFRO0/1/2	Frequency deviation: 1T trim (Open loop, using software algorithm) [2]	-2.5	—	+2.5	%	—
ΔfFRO0/1/2	Frequency deviation: User trim closed loop (Closed loop, using built-in FRO Autotuner) using accurate clock source	-1	—	+1	%	—
FDIV	Divided clocks [3]	18.75	—	150	MHz	—
DCCLK	Duty cycle full frequency	40	50	60	%	—
DCDIV	Duty cycle divided frequencies	45	50	55	%	—
TSU	Startup time in Normal mode	—	100	—	µs	Fast startup disabled
TSU	Startup time	—	50	—	µs	Fast startup enabled
IDD	Current consumption	—	100	—	µA	VDD current @ 325 MHz
JP	RMS period jitter	—	25	—	ps	@ 325 MHz / supply ripple = ±20 mV

[1] This specification is only a simulation result, not a test result.
[2] Results may vary based on application board and SMT profile. NXP recommends customers perform application-level FRO trim to attain best FRO accuracy.
[3] The oscillator has 5 frequency outputs: f, f/2, f/3, f/6, and f/8.

3.2.10 Crystal oscillator (XTAL OSC)

Table 40. Crystal oscillator (XTAL OSC)

Symbol	Description	Min	Typ	Max	Unit	Condition
Fosc	Oscillator crystal or resonator frequency	4	—	32	MHz	—
VIH	Input high voltage (XTALINSYS pin in External bypass clock mode)	VDD1V8 - 0.5	—	VDD1V8	V	—
VIL	Input low voltage (XTALINSYS pin in External bypass clock mode)	VSS	—	0.5	V	—
Ivdda (low power mode)	Analog supply current	—	1	—	mA	32 MHz Low-power mode
Ivdda (high gain mode)	Analog supply current	—	2	—	mA	32 MHz High-gain mode
RF	Feedback resistor	—	N/A	—	—	Low-power mode
RF	Feedback resistor	—	1	—	MΩ	High-gain mode

Table continues on the next page...

Table 40. Crystal oscillator (XTAL OSC)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Rs	Series resistor [1]	—	0	—	Ω	4/8/16/20/30 MHz resonator; If drive level exceeds the spec of crystal, a small Rs can be added
CxCy	XTALINSYS and XTALOUTSYS load capacitance [1]	—	—	—	—	—
tdcy	Duty-cycle of the output clock	40	50	60	%	—
Vpp	Peak-peak amplitude of oscillation	—	0.8	—	V	Low-power mode
Vpp	Peak-peak amplitude of oscillation	0.75 x VDD1V8	VDD1V8	—	V	High-gain mode
tstart	Startup time	—	4	—	ms	8 MHz Low-power mode
tstart	Startup time	—	3	—	ms	8 MHz High-gain mode
tstart	Startup time	—	0.2	—	ms	32 MHz Low-power mode
tstart	Startup time	—	0.2	—	ms	32 MHz High-gain mode

[1] See crystal or resonator manufacturer's recommendation

3.2.11 32K Crystal oscillator

Typical ratings are not guaranteed. The values listed are at room temperature (25 ° C), nominal supply voltages.

Table 41. 32K Crystal oscillator

Symbol	Description	Min	Typ	Max	Unit	Condition
FOSC32K	OSC32K Output Frequency	—	32.768	—	kHz	—
IDDLP	Supply current	—	50	—	nA	Low power mode
IDDHP	Supply current	—	575	—	nA	High power mode
CXTAL	Internal Cap Load at XTAL pin	0	—	30	pF	—
CEXTAL	Internal Cap Load at EXTAL pin	0	—	30	pF	—
tSTARTUP	Start-Up time [1]	—	—	2	s	—
ESRLP	ESR limit @ low power mode [2]	—	—	50	kΩ	—
ESRHP	ESR limit @ high power mode [2]	—	—	120	kΩ	—
VPP	Peak-to-Peak amplitude of oscillation [3]	0.7	—	VDD1V8_AO	V	With oscillator bypass mode enabled

[1] Proper PCB layout procedures must be followed to achieve specifications.
[2] The ESR of the crystal shall never exceed the maximum limit.
[3] In bypass mode, using an input square wave only on XTALIN32KHZ with XTALOUT32KHZ floating.

3.2.12 Internal low-power oscillator (LPOSC)

The LPOSC is trimmed to ± 10% accuracy over the entire voltage and temperature range.

1.71 V ≤ V DD ≤ 1.89 V.

Table 42. Internal low-power oscillator (LPOSC)

Symbol	Description	Min	Typ	Max	Unit	Condition
fosc (RC)	LPOSC clock frequency	0.9	1	1.1	MHz	—

3.2.13 Main PLL and Audio PLL electrical specifications

Table 43. Main PLL and Audio PLL electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Clock output range [1]	80	—	528	MHz	—
IDD	Supply current	—	—	5	mA	1.8 V supply
IDD	Supply current	—	—	0.5	mA	Digital supply
—	Reference clock	—	24	—	MHz	—
—	Lock time	—	—	11250	Reference cycles	—
—	Period jitter (p2p)	—	50	—	ps	—
—	PFD period jitter (p2p)	—	100	—	ps	—
—	Duty cycle	45	—	55	%	—

[1] See Table General operating conditions for specific Max Freq vs VDD1 and VDD2 limits.

3.2.14 Clock root frequencies

Following table lists the clock roots frequencies of RT700 when operating in active / sleep modes (AFBB).

3.2.14.1 CLKCTL0 clock roots frequencies

Table 44. CLKCTL0 clock roots frequencies

Symbol	Description	Min	Typ	Max	Unit	Condition
COMPUTE_MAIN_CLK	CPU clock for VDD2_COMP domain	—	—	45	MHz	VDD2 ≥ 0.7 V
COMPUTE_MAIN_CLK	CPU clock for VDD2_COMP domain	—	—	110	MHz	VDD2 ≥ 0.8 V
COMPUTE_MAIN_CLK	CPU clock for VDD2_COMP domain	—	—	192	MHz	VDD2 ≥ 0.9 V
COMPUTE_MAIN_CLK	CPU clock for VDD2_COMP domain	—	—	250	MHz	VDD2 ≥ 1.0 V
COMPUTE_MAIN_CLK	CPU clock for VDD2_COMP domain	—	—	325	MHz	VDD2 ≥ 1.1 V
DSP_CLK	HiFi 4 DSP clock for VDD2_DSP domain	—	—	45	MHz	VDD2 ≥ 0.7 V

Table continues on the next page...

Table 44. CLKCTL0 clock roots frequencies*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
DSP_CLK	HiFi 4 DSP clock for VDD2_DSP domain	—	—	110	MHz	VDD2 ≥ 0.8 V
DSP_CLK	HiFi 4 DSP clock for VDD2_DSP domain	—	—	192	MHz	VDD2 ≥ 0.9 V
DSP_CLK	HiFi 4 DSP clock for VDD2_DSP domain	—	—	250	MHz	VDD2 ≥ 1.0 V
DSP_CLK	HiFi 4 DSP clock for VDD2_DSP domain	—	—	325	MHz	VDD2 ≥ 1.1 V
COMMON_RAM_CLK	Clock of RAM in VDD2_COM domain for asynchronous access	—	—	45	MHz	VDD2 ≥ 0.7 V
COMMON_RAM_CLK	Clock of RAM in VDD2_COM domain for asynchronous access	—	—	110	MHz	VDD2 ≥ 0.8 V
COMMON_RAM_CLK	Clock of RAM in VDD2_COM domain for asynchronous access	—	—	192	MHz	VDD2 ≥ 0.9 V
COMMON_RAM_CLK	Clock of RAM in VDD2_COM domain for asynchronous access	—	—	250	MHz	VDD2 ≥ 1.0 V
COMMON_RAM_CLK	Clock of RAM in VDD2_COM domain for asynchronous access	—	—	325	MHz	VDD2 ≥ 1.1 V
XSPI0_FCLK	Clock for XSPI0	—	—	400	MHz	For all VDDN voltages.
XSPI1_FCLK	Clock for XSPI1	—	—	400	MHz	For all VDDN voltages.
COMPUTE_SYSTICK_FCLK	Systick clock for VDD2_COMP domain	—	—	33	MHz	For all VDD2 voltages
COMPUTE_TPIU_CLK	Functional clock for the TPIU	—	—	33	MHz	VDD2 ≥ 0.7 V
COMPUTE_TPIU_CLK	Functional clock for the TPIU	—	—	77	MHz	VDD2 ≥ 0.8 V
COMPUTE_TPIU_CLK	Functional clock for the TPIU	—	—	158	MHz	VDD2 ≥ 0.9 V
COMPUTE_TPIU_CLK	Functional clock for the TPIU	—	—	230	MHz	VDD2 ≥ 1.0 V
COMPUTE_TPIU_CLK	Functional clock for the TPIU	—	—	310	MHz	VDD2 ≥ 1.1 V
SCT_FCLK	Functional clock for the SCT	—	—	33	MHz	VDD2 ≥ 0.7 V
SCT_FCLK	Functional clock for the SCT	—	—	230	MHz	VDD2 ≥ 0.8 V

Table continues on the next page...

Table 44. CLKCTL0 clock roots frequencies*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
SCT_FCLK	Functional clock for the SCT	—	—	230	MHz	VDD2 ≥ 0.9 V
SCT_FCLK	Functional clock for the SCT	—	—	230	MHz	VDD2 ≥ 1.0 V
SCT_FCLK	Functional clock for the SCT	—	—	400	MHz	VDD2 ≥ 1.1 V
SAI012_CLK	Functional clock for the SAI0-SAI2	—	—	33	MHz	VDD2 ≥ 0.7 V
SAI012_CLK	Functional clock for the SAI0-SAI2	—	—	91	MHz	VDD2 ≥ 0.8 V
SAI012_CLK	Functional clock for the SAI0-SAI2	—	—	100	MHz	VDD2 ≥ 0.9 V
SAI012_CLK	Functional clock for the SAI0-SAI2	—	—	100	MHz	VDD2 ≥ 1.0 V
SAI012_CLK	Functional clock for the SAI0-SAI2	—	—	310	MHz	VDD2 ≥ 1.1 V
I3C01_PCLK	Functional clock for the I3C0 and I3C1 P-CLK	—	—	33	MHz	VDD2 ≥ 0.7 V
I3C01_PCLK	Functional clock for the I3C0 and I3C1 P-CLK	—	—	85	MHz	VDD2 ≥ 0.8 V
I3C01_PCLK	Functional clock for the I3C0 and I3C1 P-CLK	—	—	100	MHz	VDD2 ≥ 0.9 V
I3C01_PCLK	Functional clock for the I3C0 and I3C1 P-CLK	—	—	100	MHz	VDD2 ≥ 1.0 V
I3C01_PCLK	Functional clock for the I3C0 and I3C1 P-CLK	—	—	310	MHz	VDD2 ≥ 1.1 V
I3C01_FCLK	Functional clock for the I3C0 and I3C1	—	—	25	MHz	For all VDD2 voltages
UTICK0_FCLK	UTICK0 clock	—	—	33	MHz	VDD2 ≥ 0.7 V
UTICK0_FCLK	UTICK0 clock	—	—	121	MHz	VDD2 ≥ 0.8 V
UTICK0_FCLK	UTICK0 clock	—	—	225	MHz	VDD2 ≥ 0.9 V
UTICK0_FCLK	UTICK0 clock	—	—	230	MHz	VDD2 ≥ 1.0 V
UTICK0_FCLK	UTICK0 clock	—	—	310	MHz	VDD2 ≥ 1.1 V
CTIMER0-4_FCLK	CTIMER0-4 clocks	—	—	33	MHz	VDD2 ≥ 0.7 V
CTIMER0-4_FCLK	CTIMER0-4 clocks	—	—	101	MHz	VDD2 ≥ 0.8 V
CTIMER0-4_FCLK	CTIMER0-4 clocks	—	—	200	MHz	VDD2 ≥ 0.9 V
CTIMER0-4_FCLK	CTIMER0-4 clocks	—	—	230	MHz	VDD2 ≥ 1.0 V
CTIMER0-4_FCLK	CTIMER0-4 clocks	—	—	310	MHz	VDD2 ≥ 1.1 V
FLEXCOMM0-13_FCLK	LP_FLEXCOMM0-13 clocks	—	—	33	MHz	VDD2 ≥ 0.7 V

Table continues on the next page...

Table 44. CLKCTL0 clock roots frequencies*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
FLEXCOMM0-13_FCLK	LP_FLEXCOMM0-13 clocks	—	—	86	MHz	VDD2 ≥ 0.8 V
FLEXCOMM0-13_FCLK	LP_FLEXCOMM0-13 clocks	—	—	100	MHz	VDD2 ≥ 0.9 V
FLEXCOMM0-13_FCLK	LP_FLEXCOMM0-13 clocks	—	—	100	MHz	VDD2 ≥ 1.0 V
FLEXCOMM0-13_FCLK	LP_FLEXCOMM0-13 clocks	—	—	310	MHz	VDD2 ≥ 1.1 V
COMM2_CLKOUT	Clock out of VDD2_COM	—	—	250	MHz	For all VDD2 voltages
WDT0-1_FCLK	Clock for WWDT0-1	—	—	1	MHz	For all VDD2 voltages

3.2.14.2 CLKCTL1 clock roots frequencies

Table 45. CLKCTL1 clock roots frequencies

Symbol	Description	Min	Typ	Max	Unit	Condition
SENSE_DSP_CLK	DSP CPU clock of VDD1_SENSE domain	—	—	45	MHz	VDD1 ≥ 0.7 V
SENSE_DSP_CLK	DSP CPU clock of VDD1_SENSE domain	—	—	100	MHz	VDD1 ≥ 0.8 V
SENSE_DSP_CLK	DSP CPU clock of VDD1_SENSE domain	—	—	160	MHz	VDD1 ≥ 0.9 V
SENSE_DSP_CLK	DSP CPU clock of VDD1_SENSE domain	—	—	205	MHz	VDD1 ≥ 1.0 V
SENSE_DSP_CLK	DSP CPU clock of VDD1_SENSE domain	—	—	250	MHz	VDD1 ≥ 1.1 V
SENSE_SYSTICK_FCLK	Systick clock for VDD1_SENSE domain	—	—	33	MHz	For all VDD1 voltages
SAI3_CLK	Clock for SAI3	—	—	33	MHz	VDD1 ≥ 0.7 V
SAI3_CLK	Clock for SAI3	—	—	91	MHz	VDD1 ≥ 0.8 V
SAI3_CLK	Clock for SAI3	—	—	100	MHz	VDD1 ≥ 0.9 V
SAI3_CLK	Clock for SAI3	—	—	100	MHz	VDD1 ≥ 1.0 V
SAI3_CLK	Clock for SAI3	—	—	200	MHz	VDD1 ≥ 1.1 V
I3C23_FCLK	Clock for I3C2 and I3C3	—	—	25	MHz	For all VDD1 voltages
UTICK1_FCLK	Clock for UTICK1 clock	—	—	33	MHz	VDD1 ≥ 0.7 V
UTICK1_FCLK	Clock for UTICK1 clock	—	—	100	MHz	VDD1 ≥ 0.8 V
UTICK1_FCLK	Clock for UTICK1 clock	—	—	100	MHz	VDD1 ≥ 0.9 V
UTICK1_FCLK	Clock for UTICK1 clock	—	—	100	MHz	VDD1 ≥ 1.0 V

Table continues on the next page...

Table 45. CLKCTL1 clock roots frequencies...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
UTICK1_FCLK	Clock for UTICK1 clock	—	—	100	MHz	VDD1 ≥ 1.1 V
CTIMER5-7_FCLK	CTIMER5-7 clocks	—	—	33	MHz	VDD1 ≥ 0.7 V
CTIMER5-7_FCLK	CTIMER5-7 clocks	—	—	100	MHz	VDD1 ≥ 0.8 V
CTIMER5-7_FCLK	CTIMER5-7 clocks	—	—	100	MHz	VDD1 ≥ 0.9 V
CTIMER5-7_FCLK	CTIMER5-7 clocks	—	—	100	MHz	VDD1 ≥ 1.0 V
CTIMER5-7_FCLK	CTIMER5-7 clocks	—	—	200	MHz	VDD1 ≥ 1.1 V
FLEXCOMM17-20_FCLK	FLEXCOMM17-20 clocks	—	—	33	MHz	VDD1 ≥ 0.7 V
FLEXCOMM17-20_FCLK	FLEXCOMM17-20 clocks	—	—	88	MHz	VDD1 ≥ 0.8 V
FLEXCOMM17-20_FCLK	FLEXCOMM17-20 clocks	—	—	100	MHz	VDD1 ≥ 0.9 V
FLEXCOMM17-20_FCLK	FLEXCOMM17-20 clocks	—	—	100	MHz	VDD1 ≥ 1.0 V
FLEXCOMM17-20_FCLK	FLEXCOMM17-20 clocks	—	—	300	MHz	VDD1 ≥ 1.1 V
WDT2-3_FCLK	Clock for WWDT2-3	—	—	1	MHz	For all VDD1 voltages

3.2.14.3 CLKCTL2 clock roots frequencies

Table 46. CLKCTL2 clock roots frequencies

Symbol	Description	Min	Typ	Max	Unit	Condition
COMMON_VDDN_CLK	Clock for VDDN_COM domain	—	—	230	MHz	For all VDDN voltages
OSC_CLK_USB	Clock for USB0	—	—	24	MHz	For all VDDN voltages
OSC_CLK_EUSB	Clock for USB1 (eUSB) [1]	—	—	24	MHz	For all VDDN voltages

[1] EUSB pins are not available on WLCSP package.

3.2.14.4 CLKCTL3 clock roots frequencies

Table 47. CLKCTL3 clock roots frequencies

Symbol	Description	Min	Typ	Max	Unit	Condition
SENSE_MAIN_CLK/SENSE_MAIN_CLK1	Clock for VDD1_SENSE domain	—	—	45	MHz	VDD1 ≥ 0.7 V
SENSE_MAIN_CLK/SENSE_MAIN_CLK1	Clock for VDD1_SENSE domain	—	—	100	MHz	VDD1 ≥ 0.8 V

Table continues on the next page...

Table 47. CLKCTL3 clock roots frequencies*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
SENSE_MAIN_CLK/SENSE_MAIN_CLK1	Clock for VDD1_SENSE domain	—	—	160	MHz	VDD1 ≥ 0.9 V
SENSE_MAIN_CLK/SENSE_MAIN_CLK1	Clock for VDD1_SENSE domain	—	—	205	MHz	VDD1 ≥ 1.0 V
SENSE_MAIN_CLK/SENSE_MAIN_CLK1	Clock for VDD1_SENSE domain	—	—	250	MHz	VDD1 ≥ 1.1 V
SENSE_RAM_CLK	Clock for RAM in VDD1_SENSE domain	—	—	45	MHz	VDD1 ≥ 0.7 V
SENSE_RAM_CLK	Clock for RAM in VDD1_SENSE domain	—	—	110	MHz	VDD1 ≥ 0.8 V
SENSE_RAM_CLK	Clock for RAM in VDD1_SENSE domain	—	—	192	MHz	VDD1 ≥ 0.9 V
SENSE_RAM_CLK	Clock for RAM in VDD1_SENSE domain	—	—	250	MHz	VDD1 ≥ 1.0 V
SENSE_RAM_CLK	Clock for RAM in VDD1_SENSE domain	—	—	325	MHz	VDD1 = 1.1 V
SDADC_FCLK	Clock for SDADC	—	—	25	MHz	For all VDD1 voltages
SARADC_FCLK	Clock for ADC	—	—	16.5	MHz	VDD1 ≥ 0.7 V
SARADC_FCLK	Clock for ADC	—	—	43	MHz	VDD1 ≥ 0.8 V
SARADC_FCLK	Clock for ADC	—	—	81	MHz	VDD1 ≥ 0.9 V
SARADC_FCLK	Clock for ADC	—	—	100	MHz	VDD1 ≥ 1.0 V
SARADC_FCLK	Clock for ADC	—	—	140	MHz	VDD1 ≥ 1.1 V
OSEVENT_FCLK	Clock for OSTIMER	—	—	33	MHz	VDD1 ≥ 0.7 V
OSEVENT_FCLK	Clock for OSTIMER	—	—	86	MHz	VDD1 ≥ 0.8 V
OSEVENT_FCLK	Clock for OSTIMER	—	—	100	MHz	VDD1 ≥ 0.9 V
OSEVENT_FCLK	Clock for OSTIMER	—	—	100	MHz	VDD1 ≥ 1.0 V
OSEVENT_FCLK	Clock for OSTIMER	—	—	200	MHz	VDD1 ≥ 1.1 V
MICFIL_FCLK	Clock for MICFIL	—	—	25	MHz	VDD1 ≥ 0.7 V
MICFIL_FCLK	Clock for MICFIL	—	—	62	MHz	VDD1 ≥ 0.8 V
MICFIL_FCLK	Clock for MICFIL	—	—	100	MHz	VDD1 ≥ 0.9 V
MICFIL_FCLK	Clock for MICFIL	—	—	100	MHz	VDD1 ≥ 1.0 V
MICFIL_FCLK	Clock for MICFIL	—	—	200	MHz	VDD1 ≥ 1.1 V
LPI2C_FCLK	Clock for LP_FLEXCOMM5	—	—	33	MHz	VDD1 ≥ 0.7 V

Table continues on the next page...

Table 47. CLKCTL3 clock roots frequencies*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LPI2C_FCLK	Clock for LP_FLEXCOMM5	—	—	94	MHz	VDD1 ≥ 0.8 V
LPI2C_FCLK	Clock for LP_FLEXCOMM5	—	—	100	MHz	VDD1 ≥ 0.9 V
LPI2C_FCLK	Clock for LP_FLEXCOMM5	—	—	100	MHz	VDD1 ≥ 1.0 V
LPI2C_FCLK	Clock for LP_FLEXCOMM5	—	—	250	MHz	VDD1 ≥ 1.1 V
SENSE_CLKOUT	Clock out for VDD1_SENSE	—	—	250	MHz	For all VDD1 voltages

3.2.14.5 CLKCTL4 clock roots frequencies

Table 48. CLKCTL4 clock roots frequencies

Symbol	Description	Min	Typ	Max	Unit	Condition
MEDIA_MAIN_CLK	Clock for VDD2_MEDIA domain	—	—	45	MHz	VDD2 ≥ 0.7 V
MEDIA_MAIN_CLK	Clock for VDD2_MEDIA domain	—	—	110	MHz	VDD2 ≥ 0.8 V
MEDIA_MAIN_CLK	Clock for VDD2_MEDIA domain	—	—	192	MHz	VDD2 ≥ 0.9 V
MEDIA_MAIN_CLK	Clock for VDD2_MEDIA domain	—	—	250	MHz	VDD2 ≥ 1.0 V
MEDIA_MAIN_CLK	Clock for VDD2_MEDIA domain	—	—	325	MHz	VDD2 ≥ 1.1 V
MEDIA_VDDN_CLK	Clock for VDDN_MEDIA domain	—	—	250	MHz	VDDN ≥ 1.0 V
MEDIA_VDDN_CLK	Clock for VDDN_MEDIA domain	—	—	325	MHz	VDDN ≥ 1.1 V
XSPI2_FCLK	Clock for XSPI2	—	—	500	MHz	For all VDDN voltages
SDIO0_FCLK	Clock for SDIO0	—	—	400	MHz	For all VDDN voltages
SDIO1_FCLK	Clock for SDIO1	—	—	400	MHz	For all VDDN voltages
GPU_FCLK	Clock for vGPU	—	—	169	MHz	VDD2 ≥ 0.9 V
GPU_FCLK	Clock for vGPU	—	—	230	MHz	VDD2 ≥ 1.0 V
GPU_FCLK	Clock for vGPU	—	—	325	MHz	VDD2 ≥ 1.1 V
DCPIXEL_FCLK	Clock for LCDIF	—	—	325	MHz	For all VDD2 voltages
DPHY_BIT_CLK	Clock for MIPI_DSI_HOST PHY bit clock	—	—	285	MHz	VDD2 ≥ 0.9 V
DPHY_BIT_CLK	Clock for MIPI_DSI_HOST PHY bit clock	—	—	500	MHz	VDD2 ≥ 1.0 V
DPHY_BIT_CLK	Clock for MIPI_DSI_HOST PHY bit clock	—	—	500	MHz	VDD2 ≥ 1.1 V
DPHY_RXTX_CLK	Clock for MIPI_DSI_HOST PHY Rx/Tx clock	—	—	62.5	MHz	VDD2 ≥ 0.9 V
DPHY_RXTX_CLK	Clock for MIPI_DSI_HOST PHY Rx/Tx clock	—	—	62.5	MHz	VDD2 ≥ 1.0 V

Table continues on the next page...

Table 48. CLKCTL4 clock roots frequencies*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
DPHY_RXTX_CLK	Clock for MIPI_DSI_HOST PHY Rx/Tx clock	—	—	100	MHz	VDD2 ≥ 1.1 V
FLEXIO_FCLK	Clock for FLEXIO	—	—	33	MHz	VDD2 ≥ 0.7 V
FLEXIO_FCLK	Clock for FLEXIO	—	—	92	MHz	VDD2 ≥ 0.8 V
FLEXIO_FCLK	Clock for FLEXIO	—	—	175	MHz	VDD2 ≥ 0.9 V
FLEXIO_FCLK	Clock for FLEXIO	—	—	230	MHz	VDD2 ≥ 1.0 V
FLEXIO_FCLK	Clock for FLEXIO	—	—	340	MHz	VDD2 ≥ 1.1 V
LPSPI14/16_FCLK	Clock for LP_FLEXCOMM14/16	—	—	33	MHz	VDD2 ≥ 0.7 V
LPSPI14/16_FCLK	Clock for LP_FLEXCOMM14/16	—	—	94	MHz	VDD2 ≥ 0.8 V
LPSPI14/16_FCLK	Clock for LP_FLEXCOMM14/16	—	—	150	MHz	VDD2 ≥ 0.9 V
LPSPI14/16_FCLK	Clock for LP_FLEXCOMM14/16	—	—	150	MHz	VDD2 ≥ 1.0 V
LPSPI14/16_FCLK	Clock for LP_FLEXCOMM14/16	—	—	300	MHz	VDD2 ≥ 1.1 V
USB_WAKE_CLK	Clock for USB0	—	—	24	MHz	For all VDDN voltages
EUSB_WAKE_CLK	Clock for USB1 (eUSB)	—	—	24	MHz	For all VDDN voltages

3.2.14.6 Clock sources frequencies

Table 49. Clock sources frequencies

Symbol	Description	Min	Typ	Max	Unit	Condition
DFRO_0_MAX	The maximum clock frequency for DFRO0	—	—	192	MHz	VDD2 ≥ 0.7 V
DFRO_0_MAX	The maximum clock frequency for DFRO0	—	—	192	MHz	VDD2 ≥ 0.8 V
DFRO_0_MAX	The maximum clock frequency for DFRO0	—	—	237	MHz	VDD2 ≥ 0.9 V
DFRO_0_MAX	The maximum clock frequency for DFRO0	—	—	300	MHz	VDD2 ≥ 1.0 V
DFRO_0_MAX	The maximum clock frequency for DFRO0	—	—	325	MHz	VDD2 ≥ 1.1 V
DFRO_1_MAX	The maximum clock frequency for DFRO1	—	—	192	MHz	For al VDD2 voltages
DFRO_2_MAX	The maximum clock frequency for DFRO2	—	—	192	MHz	VDD1 ≥ 0.7 V
DFRO_2_MAX	The maximum clock frequency for DFRO2	—	—	192	MHz	VDD1 ≥ 0.8 V
DFRO_2_MAX	The maximum clock frequency for DFRO2	—	—	231	MHz	VDD1 ≥ 0.9 V

Table continues on the next page...

Table 49. Clock sources frequencies...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
DFRO_2_MAX	The maximum clock frequency for DFRO2	—	—	300	MHz	VDD1 ≥ 1.0 V
DFRO_2_MAX	The maximum clock frequency for DFRO2	—	—	325	MHz	VDD1 ≥ 1.1 V
MAIN_PLL_VCO	VCO for main PLL	—	—	528	MHz	VDDN ≥ 1.0 V
MAIN_PLL_PFD0	PFD0 for main PLL	—	—	600	MHz	VDDN ≥ 1.0 V
MAIN_PLL_PFD1	PFD1 for main PLL	—	—	600	MHz	VDDN ≥ 1.0 V
MAIN_PLL_PFD2	PFD2 for main PLL	—	—	600	MHz	VDDN ≥ 1.0 V
MAIN_PLL_PFD3	PFD3 for main PLL	—	—	600	MHz	VDDN ≥ 1.0 V
AUDIO_PLL_VCO	VCO for Audio PLL	—	—	528	MHz	VDDN ≥ 1.0 V
AUDIO_PLL_PFD0	PFD0 of Audio PLL	—	—	600	MHz	VDDN ≥ 1.0 V
AUDIO_PLL_PFD1	PFD1 of Audio PLL	—	—	600	MHz	VDDN ≥ 1.0 V
AUDIO_PLL_PFD2	PFD2 of Audio PLL	—	—	600	MHz	VDDN ≥ 1.0 V
AUDIO_PLL_PFD3	PFD3 of Audio PLL	—	—	600	MHz	VDDN ≥ 1.0 V

3.3 System modules

3.3.1 Reset timings parameters

Table 50. Reset timings parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
CC1	Duration of RESETN to be qualified as valid	40	—	—	ns	—
Tr	RESETN rise time	—	—	5	ns	—
Tr	RESETN fall time	—	—	5	ns	—

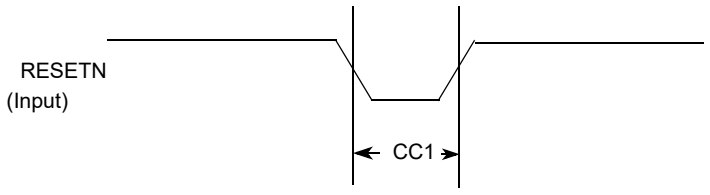


Figure 18. Reset timing diagram

3.3.2 Serial Wire Debug (SWD) timing specifications

VDDIO_0 = 1.71 V to 1.89 V; CL = 20 pF balanced loading on all pins; Input slew = 1.5 ns, SLEWRATE setting = standard mode for all pins; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 51. Serial Wire Debug (SWD) timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
J1	SWCLK frequency of operation	—	—	50	MHz	VDD2 ≥ 1.0 V
J1	SWCLK frequency of operation	—	—	33	MHz	VDD2 ≥ 0.9 V / 0.8 V
J1	SWCLK frequency of operation	—	—	25	MHz	VDD2 ≥ 0.7 V
J2	Clock cycle time	20	—	—	ns	VDD2 ≥ 1.0 V
J2	Clock cycle time	30	—	—	ns	VDD2 ≥ 0.9 V / 0.8 V
J2	Clock cycle time	40	—	—	ns	VDD2 ≥ 0.7 V
J3	SWCLK clock pulse width: Serial wire debug	10	—	—	ns	VDD2 ≥ 1.0 V
J3	SWCLK clock pulse width: Serial wire debug	15	—	—	ns	VDD2 ≥ 0.9 V / 0.8 V
J3	SWCLK clock pulse width: Serial wire debug	20	—	—	ns	VDD2 ≥ 0.7 V
J4	SWCLK rise and fall times	—	—	3	ns	All voltages
J9	SWDIO input data setup time to SWCLK rise	5	—	—	ns	VDD2 ≥ 1.0 V
J9	SWDIO input data setup time to SWCLK rise	15	—	—	ns	VDD2 ≥ 0.9 V / 0.8 V
J9	SWDIO input data setup time to SWCLK rise	25	—	—	ns	VDD2 ≥ 0.7 V
J10	SWDIO input data hold time after SWCLK rise	1	—	—	ns	VDD2 ≥ 1.0 V, 0.9 V / 0.8 V, 0.7 V
J11	SWCLK high to SWDIO data valid	—	—	37	ns	All voltages
J12	SWCLK high to SWDIO high-Z	1	—	—	ns	All voltages

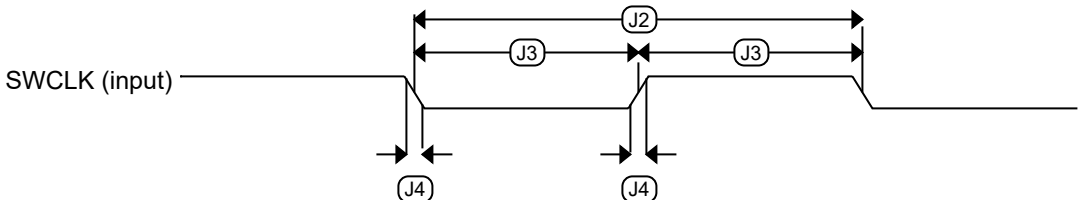


Figure 19. Serial wire clock input timing

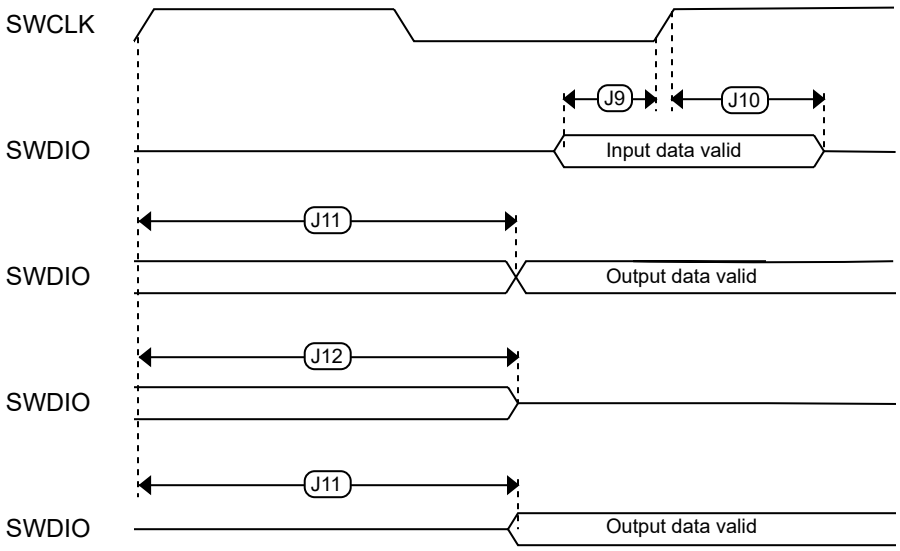


Figure 20. Serial wire data timing

3.3.3 JTAG timing specifications

VDDIO_0 = 1.71 V to 1.89 V; CL = 20 pF balanced loading on all pins; Input slew = 1.5 ns, SLEWRATE setting = standard mode for all pins; DRIVE = Normal output drive; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 52. JTAG timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
J1	TCK frequency of operation: Boundary Scan	0	—	25	MHz	—
J2	TCK cycle period	1000/J1	—	—	ns	—
J3	TCK clock pulse width: Boundary Scan	20	—	—	ns	—
J4	TCK rise and fall times	—	—	3	ns	—
J5	Boundary scan input data setup time to TCK rise	5	—	—	ns	—
J6	Boundary scan input data hold time after TCK rise	5	—	—	ns	—
J7	TCK low to boundary scan output data valid	—	—	15.2	ns	—
J8	TCK low to boundary scan output high-Z	—	—	15.2	ns	—
J13	TRSTN assert time	100	—	—	ns	—

Table continues on the next page...

Table 52. JTAG timing specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
J14	TRSTN setup time (negation) to TCK high	8	—	—	ns	—

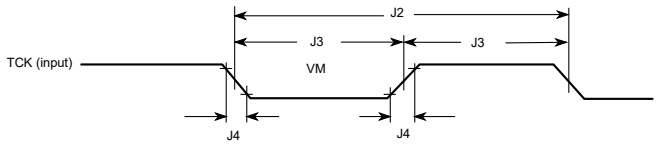


Figure 21. Test clock input timing

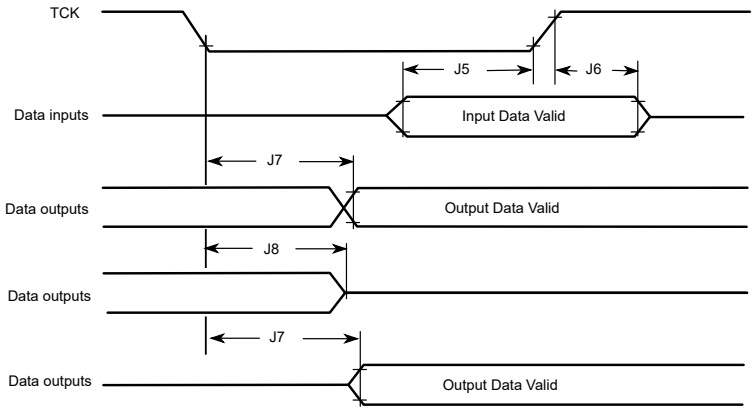


Figure 22. Boundary scan (JTAG) timing

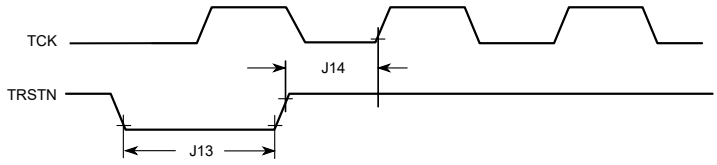


Figure 23. TRSTN timing

3.4 External memory interface

3.4.1 Dynamic characteristics: XSPI interface

3.4.1.1 XSPI interface SDR Mode

VDDIO_x = 1.71 V to 1.89 V; VDDIO_x = 1.1 V to 1.3 V, CL = 10 pF balanced loading on all pins, VDDN = 1.0 V to 1.15 V, DRIVE = Normal output drive, Input skew = 1 ns, parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 53. XSPI interface SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency for all pins: 1.2 V and 1.8 V I/O mode	—	—	50	MHz	MCR[DQS_FA_SEL] = 1
fclk	Clock frequency of XSPI0: 1.2 V I/O mode	—	—	166	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI1: 1.2 V I/O mode	—	—	166	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI2: 1.2 V I/O mode	—	—	200	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI0: 1.8 V I/O mode	—	—	200	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI1: 1.8 V I/O mode	—	—	200	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI2: 1.8 V I/O mode	—	—	250	MHz	MCR[DQS_FA_SEL] = 3
tDS	Data set-up time: 1.2 V and 1.8 V I/O mode	12	—	—	ns	MCR[DQS_FA_SEL] = 1 (internal dummy read strobe and loopbacked internally)
tDS	Data set-up time: XSPI0/1 1.8 V I/O mode 200 MHz	1.1	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDS	Data set-up time: XSPI2 1.8 V I/O mode 250 MHz	1	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDS	Data set-up time: XSPI0/1 1.2 V I/O mode 166 MHz	1.1	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDS	Data set-up time: XSPI2 1.2 V I/O mode 200 MHz	1	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: 1.2 V and 1.8 V I/O mode	0	—	—	ns	MCR[DQS_FA_SEL] = 1 (internal dummy read strobe and loopbacked internally)
tDH	Data hold time: XSPI0/1 1.8 V I/O mode 200 MHz	0.9	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: XSPI2 1.8 V I/O mode 250 MHz	0.9	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)

Table continues on the next page...

Table 53. XSPI interface SDR Mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tDH	Data hold time: XSPI0/1 1.2 V I/O mode 166 MHz	0.9	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: XSPI2 1.2 V I/O mode 200 MHz	0.9	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tV(Q)	Data output valid time: XSPI0/1 1.8 V I/O mode 200 MHz	1.5	—	3.5	ns	—
tV(Q)	Data output valid time: XSPI2 1.8 V I/O mode 250 MHz	1.0	—	3.0	ns	—
tV(Q)	Data output valid time: XSPI0/1 1.2 V I/O mode 166 MHz	1.5	—	3.5	ns	—
tV(Q)	Data output valid time: XSPI2 1.2 V I/O mode 200 MHz	1.0	—	3.0	ns	—

Following is the XSPI timing diagram for SDR input timing modes.

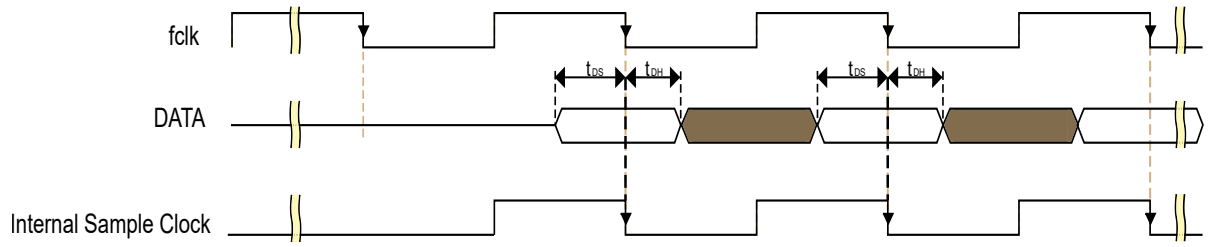


Figure 24. SDR mode input timing (DQS_FA_SEL = 1)

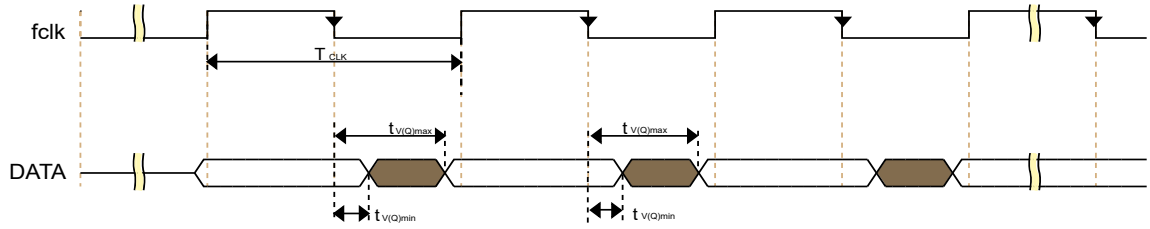


Figure 25. SDR mode output timing

3.4.1.2 XSPI interface DDR Mode

VDDIO_x = 1.71 V to 1.89 V; VDDIO_x = 1.1 V to 1.3 V, CL = 5 pF balanced loading on all pins, VDDN = 1.0 V to 1.15 V, DRIVE = Normal output drive, Input skew = 1 ns, SLEW setting = standard mode for all pins, parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 54. XSPI interface DDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency for all XSPI instances	—	—	20	MHz	MCR[DQS_FA_SEL] = 1
fclk	Clock frequency for all XSPI instances: 1.8 V I/O mode	—	—	80	MHz	—
fclk	Clock frequency of XSPI0 for all XSPI instances: 1.8 V I/O mode	—	—	200	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI1 for all XSPI instances: 1.8 V I/O mode	—	—	200	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI2 for all XSPI instances: 1.8 V I/O mode	—	—	250	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI0 for all XSPI instances: 1.2 V I/O mode	—	—	166	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI1 for all XSPI instances: 1.2 V I/O mode	—	—	166	MHz	MCR[DQS_FA_SEL] = 3
fclk	Clock frequency of XSPI2 for all XSPI instances: 1.2 V I/O mode	—	—	200	MHz	MCR[DQS_FA_SEL] = 3
tDS	Data set-up time: 1.2 V and 1.8 V I/O mode	12	—	—	ns	MCR[DQS_FA_SEL] = 1 (internal dummy read strobe and loopbacked internally)
tDS	Data set-up time: 1.2 V and 1.8 V I/O mode	1.25	—	—	ns	—
tDS	Data set-up time: XSPI0/1 1.8 V I/O mode 200 MHz	0.7	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDS	Data set-up time: XSPI2 1.8 V I/O mode 250 MHz	0.48	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDS	Data set-up time: XSPI0/1 1.2 V I/O mode 166 MHz	0.7	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDS	Data set-up time: XSPI2 1.2 V I/O mode 200 MHz	0.48	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: 1.2 V and 1.8 V I/O mode	0	—	—	ns	MCR[DQS_FA_SEL] = 1 (internal dummy read strobe and loopbacked internally)
tDH	Data hold time: 1.2 V and 1.8 V I/O mode	1	—	—	ns	—

Table continues on the next page...

Table 54. XSPI interface DDR Mode*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tDH	Data hold time: XSPI0/1 1.8 V mode 200 MHz	0.6	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: XSPI2 1.8 V mode 250 MHz	0.4	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: XSPI0/1 1.2 V mode 166 MHz	0.6	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tDH	Data hold time: XSPI2 1.2 V mode 200 MHz	0.4	—	—	ns	MCR[DQS_FA_SEL] = 3 (external DQS, Flash provides read strobe)
tV(Q)	Data output valid time: XSPI0/1 1.8 V I/O mode 200 MHz	0.6	—	1.9	ns	—
tV(Q)	Data output valid time: XSPI2 1.8 V I/O mode 250 MHz	0.4	—	1.6	ns	—
tV(Q)	Data output valid time: XSPI0/1 1.2 V I/O mode 166 MHz	0.6	—	1.9	ns	—
tV(Q)	Data output valid time: XSPI2 1.2 V I/O mode 200 MHz	0.4	—	1.6	ns	—

Following are the XSPI timing diagrams for DDR input and output timing modes.

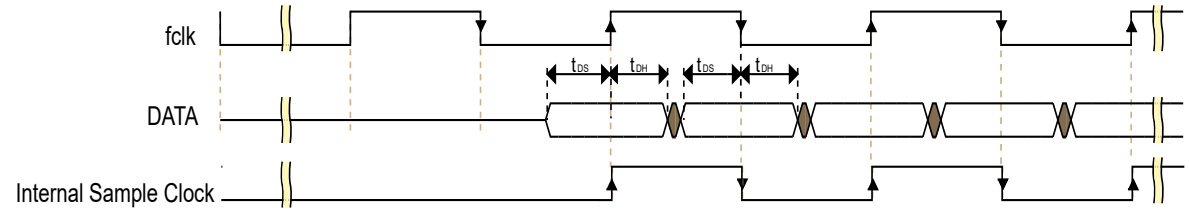


Figure 26. DDR mode input timing (DQS_FA_SEL = 1 or 2)

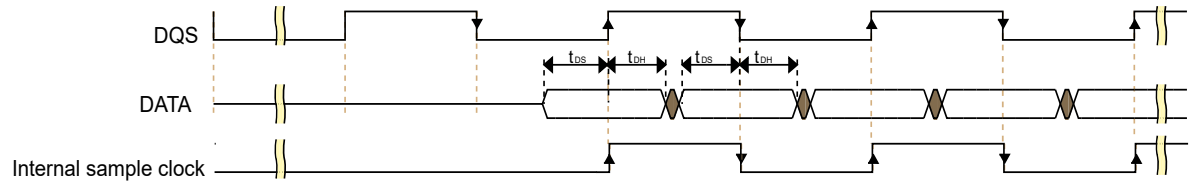


Figure 27. DDR mode input timing (DQS_FA_SEL = 3)

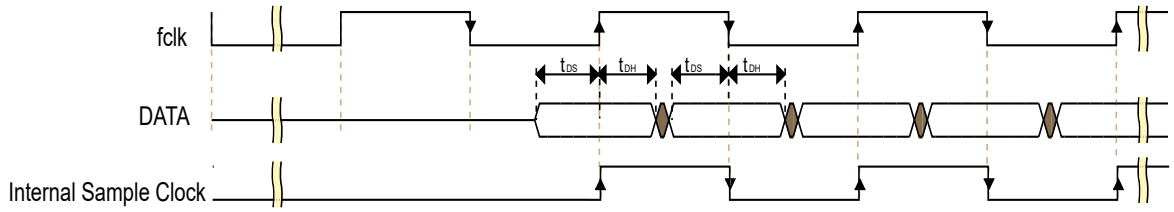


Figure 28. DDR mode output timing

3.4.2 Ultra Secured Digital Host Controller (uSDHC)

3.4.2.1 SD/MMC and SDIO characteristics (Default Speed (DS), High Speed (HS) SDR-12 and SDR-25)

VDDN = 1.0 V to 1.155 V; VDDIO_x = 1.71 V to 1.89 V; VDDN = 1.0 V to 1.155 V; CL = 10 pF balanced loading on all pins. DLL_CTRL = 0x200, Drive = Full Output Drive, Input slew = 1 ns, Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 55. SD/MMC and SDIO characteristics (Default Speed (DS), High Speed (HS) SDR-12 and SDR-25)

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	12.5	MHz	On pin CLK; data transfer mode. DS/ SDR-12 (12.5 MB/s)
fclk	Clock frequency	—	—	25	MHz	On pin CLK; data transfer mode. HS/ SDR-25 (25 MB/s)
tsu(D)	Data input set-up time	7.5	—	—	ns	On pins DATA as inputs
tsu(D)	Data input set-up time	7.5	—	—	ns	On pins CMD as inputs
th(D)	Data input hold time	1.0	—	—	ns	On pins DATA as inputs
th(D)	Data input hold time	1.0	—	—	ns	On pins CMD as inputs
tv(Q)	Data output valid time	—	—	7.5	ns	On pins DATA as outputs
tv(Q)	Data output valid time	—	—	7.5	ns	On pins CMD as outputs

3.4.2.2 SD/MMC and SDIO characteristics SDR-50, SDR-104, HS200 (MMC)

VDDN = 1.0 V to 1.155 V; VDDIO_x = 1.71 V to 1.89 V; CL = 10 pF balanced loading on all pins. DLL_CTRL = 0x200, Drive = Full Output Drive, Input slew = 1 ns, Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 56. SD/MMC and SDIO characteristics SDR-50, SDR-104, HS200 (MMC)

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	100	MHz	On pin CLK; data transfer mode, SDR-50 (50 MB/s)

Table continues on the next page...

Table 56. SD/MMC and SDIO characteristics SDR-50, SDR-104, HS200 (MMC)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	200	MHz	On pin CLK; data transfer mode, SDR-104 (104 MB/s)
fclk	Clock frequency	—	—	200	MHz	On pin CLK; data transfer mode, HS200 (MMC) (200 MB/s)
tsu(D)	Data input set-up time	7.5	—	—	ns	On pins DATA as inputs
tsu(D)	Data input set-up time	7.5	—	—	ns	On pins CMD as inputs
th(D)	Data input hold time	0	—	—	ns	On pins DATA as inputs
th(D)	Data input hold time	0	—	—	ns	On pins CMD as inputs
tv(Q)	Data output valid time	0	—	7.5	ns	On pins DATA as outputs
tv(Q)	Data output valid time	0	—	7.5	ns	On pins CMD as outputs

3.4.2.3 SD/MMC and SDIO characteristics DDR-50, HS DDR (MMC)

VDDN = 1.0 V to 1.155 V; VDDIO_x = 1.71 V to 1.89 V; CL = 10 pF balanced loading on all pins. DLL_CTRL = 0x200, Drive = Full Output Drive, Input slew = 1 ns, Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 57. SD/MMC and SDIO characteristics DDR-50, HS DDR (MMC)

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	50	MHz	On pin CLK; data transfer mode, DDR-50 (50 MB/s)
fclk	Clock frequency	—	—	52	MHz	On pin CLK; data transfer mode, HS DDR (104 MB/s)
tsu(D)	Data input set-up time	4.8	—	—	ns	On pins DATA as inputs
tsu(D)	Data input set-up time	4.8	—	—	ns	On pins CMD as inputs
th(D)	Data input hold time	0	—	—	ns	On pins DATAn as inputs
th(D)	Data input hold time	0	—	—	ns	On pins CMD as inputs
tv(Q)	Data output valid time	0	—	5.0	ns	On pins DATA as outputs
tv(Q)	Data output valid time	0	—	5.0	ns	On pins CMD as outputs

3.4.2.4 SD/MMC and SDIO characteristics HS-400 (MMC))

VDDN = 1.0 V to 1.155 V; VDDIO_x = 1.71 V to 1.89 V; CL = 10 pF balanced loading on all pins, DLL_CTRL = 0x200, Drive = Full Output Drive, Input slew = 1 ns, Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 58. SD/MMC and SDIO characteristics HS-400 (MMC))

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	200	MHz	On pin CLK; data transfer mode, HS-400 (400 MB/s)
tsu(D)	Data input set-up time	0.5	—	—	ns	On pins DATA as inputs
tsu(D)	Data input set-up time	0.5	—	—	ns	On pins CMD as inputs
th(D)	Data input hold time	0	—	—	ns	On pins DATAn as inputs
th(D)	Data input hold time	0	—	—	ns	On pins CMD as inputs
tv(Q)	Data output valid time	0	—	1.0	ns	On pins DATA as outputs
tv(Q)	Data output valid time	0	—	1.0	ns	On pins CMD as outputs

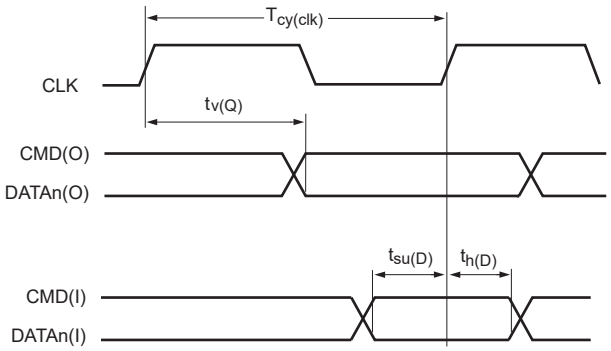


Figure 29. SD/MMC and SDIO timing

3.5 Display and graphics

3.5.1 LCDIF characteristics

CL = 15 pF balanced loading on all pins; SLEWRATE setting = standard mode; DRIVE = Normal Output Drive; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 59. LCDIF characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	62.5	MHz	On pin LCD_DOTCLK, VDD2 = 1.0 V / 0.9 V

Table continues on the next page...

Table 59. LCDIF characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
fclk	Clock frequency	—	—	28.75	MHz	On pin LCD_DOTCLK; VDD2 = 0.8 V
tV(Q)	Data output valid time	2	—	10	ns	On all LCD output pins, VDD2 = 1.0 V
tV(Q)	Data output valid time	2.8	—	13.9	ns	On all LCD output pins, VDD2 = 0.9 V
tV(Q)	Data output valid time	3.4	—	26.8	ns	On all LCD output pins, VDD2 = 0.8 V

3.5.2 MIPI DSI timing

The i.MX RT700 conforms to the MIPI D-PHY electrical specifications MIPI DSI Version 1.01 and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DCS version 1.0a at protocol layer) for MIPI display port x2 lanes.

3.6 Analog characteristics

3.6.1 ADC

3.6.1.1 16-bit ADC operating conditions

Table 60. 16-bit ADC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
VREFH_ANA18	Reference voltage High [1]	1	—	VDDA_1V8	V	—
VREFL	Reference voltage Low [1]	VSSA	—	VSSA	V	—
VADIN	Input voltage	VREFL	1.8	1.89	V	—
CSMP	Sample cycles [2]	3.5	—	131.5	Cycles	—
FADCK	ADC conversion clock frequency	6	—	84	MHz	16b Mode
FADCK	ADC conversion clock frequency	6	—	84	MHz	12b Mode
CCONV	Conversion cycles	24	—	152	Cycles	16b Mode
CCONV	Conversion cycles	19	—	147	Cycles	12b Mode
RCONV	Conversion Rate	—	—	3	MS/s	16b Mode, FADCK = 84 MHz, STS = 010
RCONV	Conversion Rate	—	—	4	MS/s	12b Mode, FADCK = 84 MHz, STS = 001
RCONV_int	Maximum Conversion Rate for internal channels	—	—	0.55	MS/s	FADCK = 84 MHz, STS = 111
CADIN	Input Capacitance	—	3.8	4.75	pF	1.8 V mode (CSCALE = 1)

Table continues on the next page...

Table 60. 16-bit ADC operating conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
RADIN	Input Resistance	—	—	1.27	kΩ	1.8 V mode (CSCALE = 1)
CP	Parasitic Capacitance [3]	—	3	5	pF	—
RAS	Analog source Resistance [1][4]	—	—	5	kΩ	—

[1] VREFH_ANA18 and VREFL are not available on WLCSP package. VREFH_ANA18 is connected internally to VDDA_1V8. VREFL is connected internally to VSSA.
[2] Must meet min TSMP
[3] Includes Pad, Pin
[4] This resistance is external to the MCU. To achieve the best results, the analog source resistance should be kept as low as possible.

3.6.1.2 16-bit ADC electrical characteristics

Table 61. 16-bit ADC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
IDDAD	Current consumption [1][2]	—	75	—	µA	Power Enabled (PWREN = 1) No Conversions
IDDAD	Current consumption [3]	—	470	—	µA	12b, Single-Enabled Mode
IDDAD	Current consumption [4]	—	730	—	µA	12-bit, Differential or Dual-SE Mode
IDDAD	Current consumption [3]	—	730	—	µA	16-bit, Single-Enabled Mode
IDDAD	Current consumption [4]	—	1250	—	µA	16-bit, Differential or Dual-SE Mode
IDDTS	Temperature sensor supply current	—	60	—	µA	Temp sensor adder
TSMP_REQ	Required sample time [5]	See note	—	—	ns	Use equation based on RAS, RADIN, CADIN, CAS, CP, and desired accuracy
TAZ_REQ	Required Auto-Zero time [6]	65.5	—	—	ns	12b Mode
TAZ_REQ	Required Auto-Zero time [7]	89.3	—	—	ns	16b Mode
TSMP	Sample time [8]	See note	—	—	ns	External inputs
TSMP_INT	Internal channel sample time	1.5	—	—	µs	Internal inputs
DNL	Differential Nonlinearity	—	—	±3	LSB	16b Mode
INL	Integral Nonlinearity	—	—	±16	LSB	16b Mode
EO	Offset Error [9][10][11]	—	—	±0.01	%FSR	16b Mode, VADIN = VREFL
EG	Gain Error [9][10][11]	—	—	±0.03	%FSR	16b Mode, VADIN = VREFH

Table continues on the next page...

Table 61. 16-bit ADC electrical characteristics*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
TUE	Total Unadjusted Error	—	—	±32	LSB	16b Mode
ENOBDIFF	ENOB, 16b Differential Mode [9]	—	15.1	—	—	23.4 KS/s (Fadc = 84 MHz, AVGS = 0111)
ENOBDIFF	ENOB, 16b Differential Mode [9]	—	13.3	—	—	0.75 MS/s (Fadc = 84 MHz, AVGS = 0010)
ENOBDIFF	ENOB, 16b Differential Mode [9]	—	12.5	—	—	3 MS/s (Fadc = 84 MHz, AVGS = 0000)
ENOBSE	ENOB, 16b Single Ended Mode [9]	—	15.0	—	—	23.4 KS/s (Fadc = 84 MHz, AVGS = 0111)
ENOBSE	ENOB, 16b Single Ended Mode [9]	—	12.6	—	—	0.75 MS/s (Fadc = 84 MHz, AVGS = 0010)
ENOBSE	ENOB, 16b Single Ended Mode [9]	—	11.8	—	—	3 MS/s (Fadc = 84 MHz, AVGS = 0000)
THD	THD	—	92	—	dB	16b Mode
SFDR	SFDR	—	90	—	dB	16b Mode
DNL	Differential Nonlinearity [12]	—	—	±1	LSB	12b Mode
INL	Integral Nonlinearity	—	—	±1.5	LSB	12b Mode
EO	Offset Error [9][10][11][13]	—	—	±0.05	%FSR	12b Mode, VADIN = VREFL
EG	Gain Error [14]	—	—	±0.05	%FSR	12b Mode, VADIN = VREFH
ENOBDIFF	ENOB, 12b Differential Mode [9]	—	12.1	—	—	0.9 MS/s (Fadc = 84 MHz, AVGS = 0010)
ENOBDIFF	ENOB, 12b Differential Mode [9]	—	11.6	—	—	3.65 MS/s (Fadc = 84 MHz, AVGS = 0000)
ENOBSE	ENOB, 12b Single Ended Mode [9]	—	11.5	—	—	0.9 MS/s (Fadc = 84 MHz, AVGS = 0010)
ENOBSE	ENOB, 12b Single Ended Mode [9]	—	11.0	—	—	3.65 MS/s (Fadc = 84 MHz, AVGS = 0000)
THD	THD	—	88	—	dB	12b Mode
SFDR	SFDR	—	89	—	dB	12b Mode
TSU	Start-up time [15]	1	—	—	µs	—
ETS	Temperature Sensor Error	—	±1	±2.5	°C	T = -40°C to 105°C
A	Slope factor constant	—	—	786	—	—
B	Offset constant	—	—	314	—	—
α	Bandgap constant	—	—	11.12	—	—

[1] All accuracy numbers assume the ADC is calibrated with VREFH = VDDA and using a high speed dedicated input channel.
[2] Typical values assume VDDA = 1.8 V, Temp = 25°C, fADCK = 84 MHz unless otherwise stated. Typical values are for reference only, and are not tested in production.

[3] 84 MHz clock, CTYPE = 0X
[4] 84 MHz clock, CTYPE = 1X
[5] TSMP_REQ = B * ln(2) * [RAS * (CAS + CP + CADIN) + (RAS+RADCtotal) * CADIN], B = desired sampling accuracy in bits
[6] 5.5 cycles at 84 MHz
[7] 7.5 cycles at 84 MHz
[8] TSMP = max (TSMP_REQ, TAZ_REQ)
[9] Fin = 1 kHz
[10] For 3.6 V tolerant input channels
[11] FSR = VREFH - VREFL
[12] Monotonic with no missing codes in 12b Mode
[13] Offset error is same as ZSE, error measured at 0 V with zero scale.
[14] Gain error is FSE - ZSE (same as FSE - EO)
[15] Delay required

3.6.1.3 16-bit ADC input impedance equivalent circuit diagram

There is an additional R_{IOMUX} of 350 Ω (from 295 Ω to 405 Ω) resistance if an input goes through the MUX inside the IO and C_P of 3 pF as shown in Figure 30.

To calculate the sample request time, using the following equation where $R_{ADCtotal} = R_{ADIN} + R_{IOMUX}$, R_{IOMUX} = 350 Ω, C_p = 3 pF as shown in Figure 30.

$T_{SMP\_REQ} = B * ln(2) * [R_{AS} * (C_{AS} + C_P + C_{ADIN}) + (R_{AS} + R_{ADCtotal}) * C_{ADIN}]$

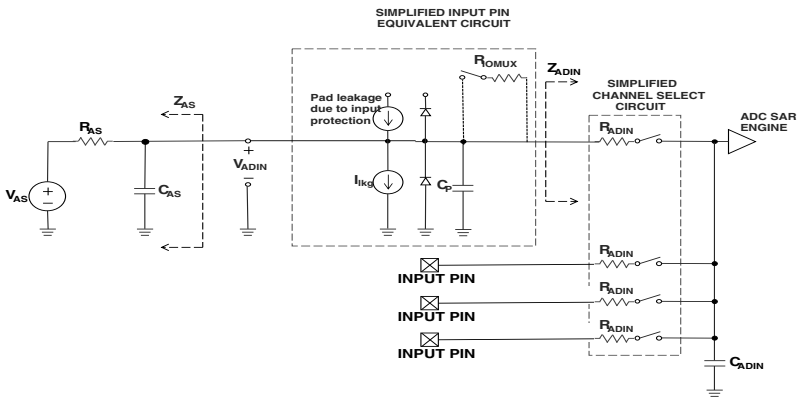


Figure 30. ADC input impedance equivalent circuit diagram

3.6.1.4 24-bit SDADC characteristics

3.6.1.4.1 24-bit SD ADC general static characteristics

Table 62. 24-bit SD ADC general static characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDA_1V8	Analog supply voltage as LDO input supply voltage [1]	1.71	1.8	1.89	V	—
VDD1	Digital supply voltage	0.6	0.9	1.155	V	—
tstart_up	Start-up time when all bias voltages, references are at functional value and bitstream starts to toggle [1]	5	10	15	µs	Supply voltage is between pre-defined min/max values and stable. adcp_power_ enable or adcn_power_

Table continues on the next page...

Table 62. 24-bit SD ADC general static characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						enable changes from '0' to '1'

[1] Based on simulation, not tested in production.

3.6.1.4.2 24-bit ADC single-ended input mode

Table 63. 24-bit ADC single-ended input mode

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdda_mod	Modulator Analog supply current	81	109	150	µA	adcp_power_enable or adcn_power_enable = '1', diff_enable = 0
Ioff_mod	Power down current of modulator	—	0.1	0.2	µA	adcp_power_enable = '0' and adcn_power_ enable = '0'
Rin	Average input impedance (Vin-rms / Iin-rms) [1]	14	20	26	kΩ	Vin-rms = 0 dBFS
VOOB	Allowed out-of-band interference signal amplitude	—	—	10	mVp	—
Vin	Full-scale single-ended input voltage	0.475	0.5	0.525	Vrms	Scale with Vvdda
OSR	Oversampling Ratio	—	512	—	—	fs-nyquist = 48 kHz
Fs	ADC clock frequency	—	24.576	—	MHz	—
fchop	Internal chopping frequency	—	24.576	—	MHz	—
SNR	Signal to Noise Ratio [2][3]	89.3	91.1	92.1	dBA	VIN = 0 dBFS, BW = 24 kHz
THD	Total Harmonic Distortion [2][3]	-89.3	-88	-85.1	dB	VIN = 0 dBFS
IdleTone	Idle tones in band	—	—	-100	dB	—
CrossTalk	Channel cross-talk	—	—	-90	dB	—
Inbal	Gain matching between channels (mostly important for left and right)	—	—	0.2	dB	VIN = 0 dBFS
PSRR	Power supply rejection ratio	60	—	—	dB	PSRR of ADC + LDO 25 mVpp 1 kHz test signal; 10 mVpp 2 MHz
AliasRej	Aliasing rejection [2]	40	—	—	dB	Valias = -60 dBFS at frequencies around Fs

[1] Typical, minimum, and maximum values are dependent of the spread of poly resistor
[2] 0 dBFS refers to Vin = 0.5 Vrms (SE), Vin = 1 Vrms (differential)
[3] Doublecp_ena = 0, Halflf_ena = 0, Halfcp_ena = 1, Doublelf_ena = 1,PTAT_CUR_SETTING = 5. 1M resistor between input of SD ADC and ground.

3.6.1.4.3 24-bit SD ADC differential input mode

Table 64. 24-bit SD ADC differential input mode

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdda_mod	Modulator Analog supply current	82	109	156	µA	adcp_power_enable = '1', adcn_power_enable = "1", and diff_enable = '1'
Ioff_mod	Power down current of modulator	—	0.1	0.2	µA	adcp_power_enable = '0' and adcn_power_ enable = '0'
Rin	Average input impedance (Vin-rms / Iin-rms), per input (pos and min)	14	20	26	kΩ	Vin-rms = 0 dBFS
VOOB	Allowed out-of-band interference signal amplitude at fOOB = N x fchop, N = 2, 4, 6, ...	—	—	10	mV	fOOB = N x fchop, N = 2, 4, 6, ...
Vin	Full-scale differential input voltage	0.95	1	1.05	Vrms	Scale with Vvdda
OSR	Oversampling Ratio	—	512	—	—	fs-nyquist = 48 kHz
Fs	ADC clock frequency	—	24.576	—	MHz	—
fchop	Internal chopping frequency	—	24.576	—	MHz	—
SNR	Signal to Noise Ratio [1][2]	90.6	92.3	94.2	dBA	VIN = 0 dBFS, BW = 24 kHz
THD	Total Harmonic Distortion [1][2]	-89.3	-86.7	-84.5	dB	VIN = 0 dBFS
IdleTone	Idle tones in band	—	—	-100	dB	—
CrossTalk	Channel cross-talk	—	—	-90	dB	—
Inbal	Gain matching between channels (mostly important for left and right) [1]	—	—	0.2	dB	VIN = 0 dBFS
PSRR	Power supply rejection ratio	60	—	—	dB	PSRR of ADC + LDO 25 mVpp 1 kHz test signal; 10 mVpp 2 MHz
CMRR	CMRR	60	—	—	—	—
AliasRej	Aliasing rejection [1]	40	—	—	dB	Valias = -60 dBFS at frequencies around Fs

[1] 0 dBFS refers to Vin = 0.5 Vrms (SE), Vin = 1 Vrms (differential)
[2] Doublecp_ena = 0, Halflf_ena = 0, Halfcp_ena = 1, Doublelf_ena = 1,PTAT_CUR_SETTING = 5. 1M resistor between input of SD ADC and ground.

3.6.1.4.4 24-bit SD ADC Decimation filter

Table 65. 24-bit SD ADC Decimation filter

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdd_dec	Filter Current consumption	—	38	—	µA	vdd = 0.8 V, fs-nyquist = 48 kHz
—	Latency: maximum time delay from analog input to digital decimator output	—	700	—	µs	fs-nyquist = 48 kHz
vdec_pas_rip	Pass band ripple	—	±0.5	—	dB	0...0.44 x fs-nyquist
—	Stop band	—	-70	—	dB	> 0.55 x fs-nyquist
—	Stop band	—	-30	—	dB	> 0.55 x fs-nyquist
—	Volume control range	-63.5	—	24	dB	—
—	Dynamic range	—	120	—	dB	> 0.4 x fs-nyquist
—	In-band droop	—	±0.5	—	dB	> 0.4 x fs-nyquist

3.6.1.4.5 24-bit SD ADC DC Loop filter

Table 66. 24-bit SD ADC DC Loop filter

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdd_dc	Filter Current consumption	—	27	—	µA	dcloop_p_enable = '1', Vdd = 0.8 V
Vdcloop_range	Common mode correction range w.r.t. Vcm of 0.75 V	-0.71	—	0.71	V	—
tdcloop	DC loop time constant	—	100	—	ms	—
Ivdda_dc	DC loop time Filter Analog current consumption	—	50	—	µA	dcloop_p_enable = '1'

3.6.2 Analog comparator characteristics

Table 67. Analog comparator characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
Vdd	Analog supply voltage	1.62	1.8	1.98	V	—
Vddlv	Digital supply voltage	0.6	1.1	1.3	V	—
Ivdd	High speed supply current	—	400	—	µA	—
Ivddlv	Low power mode supply current	—	1	—	µA	—
VAIO	Analog input offset	—	—	20	mV	—
VH	Hysteresis voltage (01)	—	10	—	mV	—
VH	Hysteresis voltage (10)	—	20	—	mV	—
VH	Hysteresis voltage (11)	—	30	—	mV	—

Table continues on the next page...

Table 67. Analog comparator characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VCMPOH	CMP output high	VDD - 0.5	—	—	V	—
VCMPOL	CMP output low	—	—	0.5	V	—
TDHS	Propagation delay in HS mode	—	—	50	ns	—
TDLS	Propagation delay in LS mode	—	—	5	µs	—
INL	DAC8B INL	-1	—	1	LSB	—
DNL	DAC8B DNL	-1	—	1	LSB	—

3.6.3 Temperature Detector specifications

Table 68. Temperature Detector specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Accuracy at room temperature [1]	-4	—	+4	°C	—

[1] Based on simulation, not tested in production.

3.7 Communication interfaces

3.7.1 LPUART interface characteristics

Please see I/O parameters.

Excluding delays introduced by external device and PCB, the maximum bit rates of 6.25 Mbit/s in asynchronous mode can be achieved.

3.7.2 Flexible I/O controller (FLEXIO)

CL = 15 pF balanced loading on all pins; SLEWRATE setting = standard mode; DRIVE = Normal output drive; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 69. Flexible I/O controller (FLEXIO)

Symbol	Description	Min	Typ	Max	Unit	Condition
tODS	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle [1]	0	—	2	ns	—
tIDS	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle [1]	0	—	2	ns	—

[1] See Table CLKCTL4 clock roots frequencies, which lists the frequencies of FLEXIO_FCLK at different VDD2 voltages.

3.7.3 I2C-bus

1.71 V ≤ VDD ≤ 1.89 V.

Table 70. Dynamic characteristic: I2C-bus pins[1]

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL clock frequency	0	—	100	kHz	Standard-mode
		0	—	400	kHz	Fast-mode
		0	—	1	MHz	Fast-mode Plus
tLOW	LOW period of the SCL clock [2]	4.7	—	—	µs	Standard-mode
		1.3	—	—	µs	Fast-mode
		0.5	—	—	µs	Fast-mode Plus
tHIGH	HIGH period of the SCL clock [2]	4.0	—	—	µs	Standard-mode
		0.6	—	—	µs	Fast-mode
		0.26	—	—	µs	Fast-mode Plus
tHD; DAT	Data hold time [3][4][5]	0	—	—	µs	Standard-mode
		0	—	—	µs	Fast-mode
		0	—	—	µs	Fast-mode Plus
tSU; DAT	Data set-up time [6][7]	250	—	—	ns	Standard-mode
		100	—	—	ns	Fast-mode
		50	—	—	ns	Fast-mode Plus

[1] Guaranteed by design. Not tested in production.
[2] The MSTTIME register allows programming of certain times for the clock (SCL) high and low times. Please see i.MX RT700 Low-Power Crossover MCU Reference Manual for further details.
[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
[4] Ensure SCL drops below 0.3 VDD on falling edge before SDA crosses into the indeterminate range of 0.3 VDD to 0.7 VDD.
Note: *For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (VDD) to 0.3 VDD should be used to insert a delay of the SDA transition with respect to SCL.*
[5] The maximum tHD;DAT could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of tVD; DAT or tVD; ACK by a transition time. This maximum must only be met if the device does not stretch the LOW period (tLOW) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
[6] A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system but the requirement tSU;DAT = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr(max) + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
[7] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

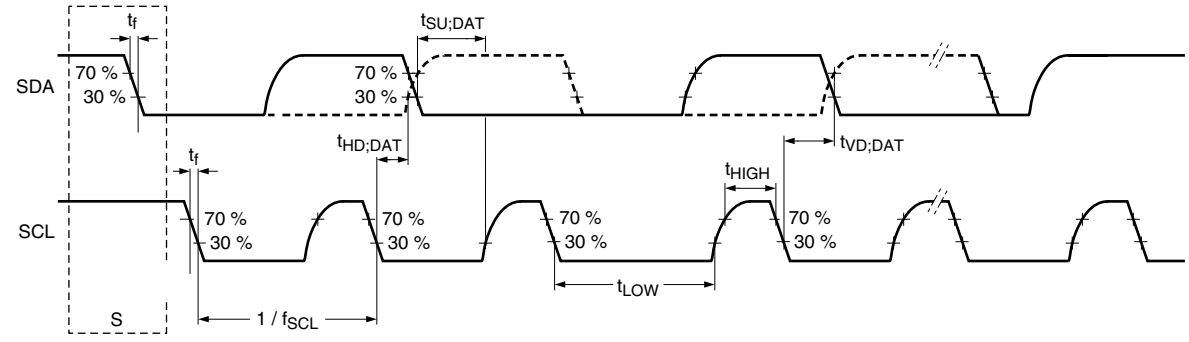


Figure 31. I2C bus pins clock timing

[1]

[1] See Table 17 about Fall-time specifications.

3.7.4 I3C Push-Pull Timing Parameters for SDR Mode

VDDIO_x = 1.71 V to 1.89 V. CL = 50 pF balanced loading on all pins; Input slew = 1 ns, SLEWRATE = standard mode; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 71. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0.01	12.5	12.9	MHz	FSCL = 1 / (tDIG_L + tDIG_H)
tDIG_L	SCL Clock Low Period [1][2]	32	—	—	ns	—
tDIG_H	SCL Clock High Period [1]	32	—	—	ns	—
tSCO	Clock in to Data Out for Target [3][4]	—	—	12	ns	—
tCR	SCL Clock Rise Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tCF	SCL Clock Fall Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Target [6]	0	—	—	—	Applicable for target and controller loopback modes
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	N/A	ns	Applicable for target and controller loopback modes

[1] tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
[2] As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.
[3] Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Controller to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.
[4] Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Controller may be a Target in a multi-Controller system, and thus shall also adhere to this requirement
[5] The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
[6] tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Controller mode vs. Target mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

Note: To assure I3C2 and I3C3 to function correctly, SLEWRATE bit of the IOCTL register must be set to 1 for corresponding SCL pin (PIO8_15 for I3C2 and PIO8_22 for I3C3).

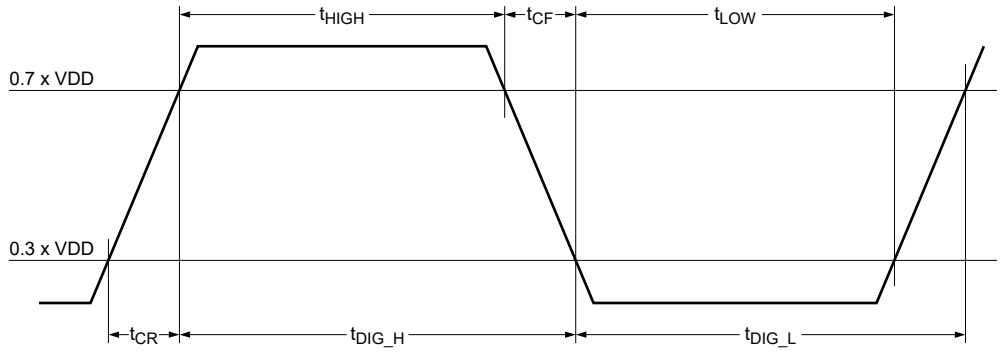


Figure 32. tDIG_H and tDIG_L

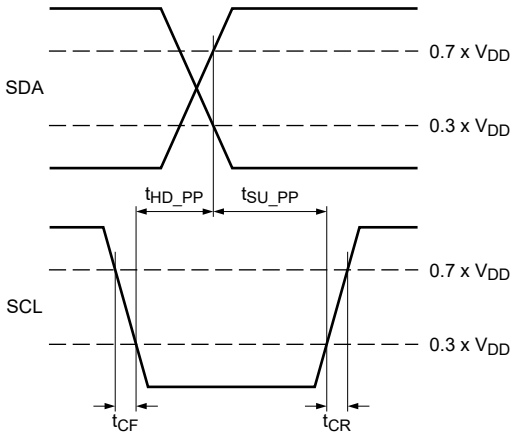


Figure 33. Controller out timing

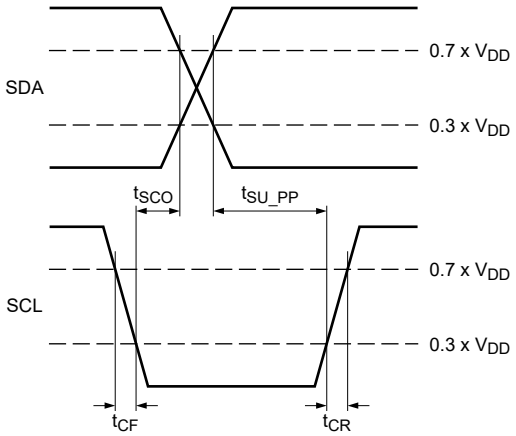


Figure 34. Target out timing

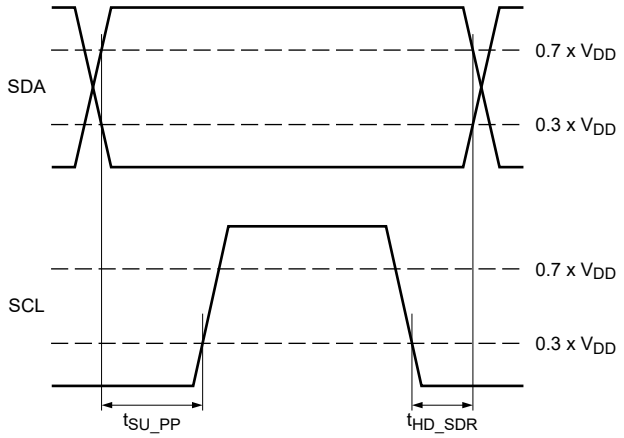


Figure 35. Controller SDR timing

3.7.5 SAI/I2S-bus interface

For clock information about SAI/I2S, see Clock root frequencies.

VDDIO_x = 1.71 V to 1.89 V. CL = 15 pF balanced loading on all pins; SLEWRATE = standard mode; Transmitter current setting = 100, 60, 50, or 30Ω; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

3.7.5.1 SAI/I2S Controller mode timing

Table 72. SAI/I2S Controller mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	20 (40)	—	—	ns	VDD2/VDD1 ≥ 1.0 V
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	20 (40)	—	—	ns	VDD2/VDD1 ≥ 0.9 V
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	21.9 (43.8)	—	—	ns	VDD2/VDD1 ≥ 0.8 V
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	—	ns	VDD2/VDD1 ≥ 0.7 V
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	—	—	10 (20)	ns	VDD2/VDD1 ≥ 1.0 V
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	—	—	10 (20)	ns	VDD2/VDD1 ≥ 0.9 V
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	—	—	10.9 (21.8)	ns	VDD2/VDD1 ≥ 0.8 V
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	—	—	40	ns	VDD2/VDD1 ≥ 0.7 V
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	—	8.4	ns	VDD2/VDD1 ≥ 1.0 V

Table continues on the next page...

Table 72. SAI/I2S Controller mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	—	8.4	ns	VDD2/VDD1 ≥ 0.9 V
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	—	12.2	ns	VDD2/VDD1 ≥ 0.8 V
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	—	48.4	ns	VDD2/VDD1 ≥ 0.7 V
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid	0	—	—	ns	All VDD2/VDD1 voltages
S7	I2S_TX_BCLK to I2S_TXD valid	—	—	8.4	ns	VDD2/VDD1 ≥ 1.0 V
S7	I2S_TX_BCLK to I2S_TXD valid	—	—	8.4	ns	VDD2/VDD1 ≥ 0.9 V
S7	I2S_TX_BCLK to I2S_TXD valid	—	—	12.2	ns	VDD2/VDD1 ≥ 0.8 V
S7	I2S_TX_BCLK to I2S_TXD valid	—	—	48.4	ns	VDD2/VDD1 ≥ 0.7 V
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	—	ns	All VDD2/VDD1 voltages
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	14	—	—	ns	VDD2/VDD1 ≥ 1.0 V
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	16	—	—	ns	VDD2/VDD1 ≥ 0.9 V
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	22	—	—	ns	VDD2/VDD1 ≥ 0.8 V
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	54	—	—	ns	VDD2/VDD1 ≥ 0.7 V
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	—	ns	All VDD2/VDD1 voltages

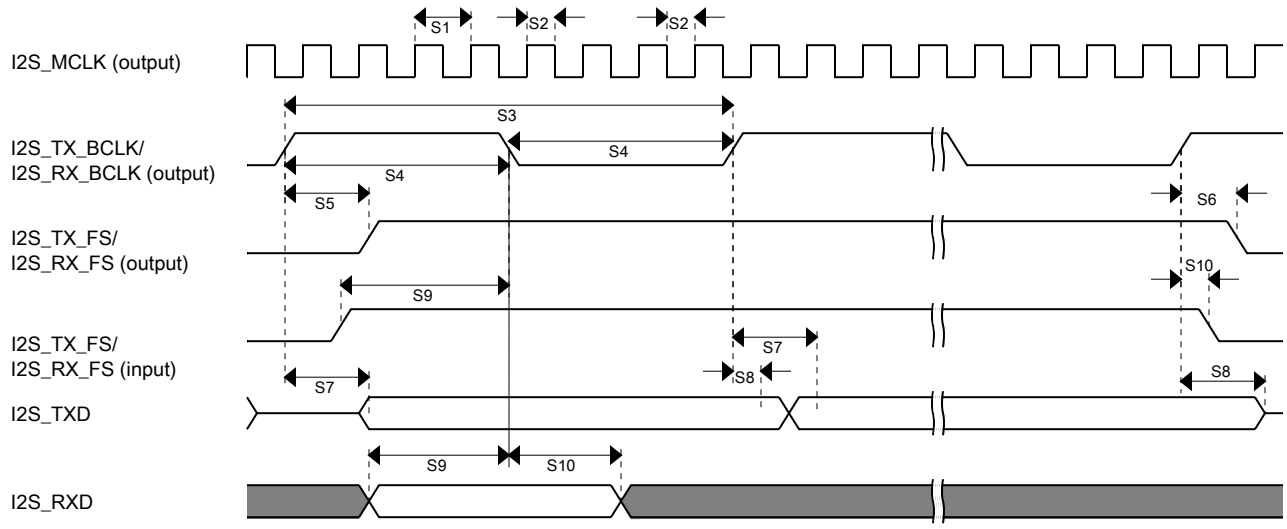


Figure 36. I2S/SAI timing - Controller mode

3.7.5.2 I2S/I2S Target mode timing

Table 73. I2S/I2S Target mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
S11	I2S_TX_MCLK/I2S_RX_BCLK cycle time (output)	40	—	—	ns	VDD1/VDD2 ≥ 1.0 V
S11	I2S_TX_MCLK/I2S_RX_BCLK cycle time (output)	40	—	—	ns	VDD1/VDD2 ≥ 0.9 V
S11	I2S_TX_MCLK/I2S_RX_BCLK cycle time (output)	43.8	—	—	ns	VDD1/VDD2 ≥ 0.8 V
S11	I2S_TX_MCLK/I2S_RX_BCLK cycle time (output)	100	—	—	ns	VDD1/VDD2 ≥ 0.7 V
S12	I2S_TX_MCLK/I2S_RX_BCLK pulse width high/low (input)	45%	—	55%	MCLK period	—
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/ I2S_RX_BCLK	6	—	—	ns	—
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/ I2S_RX_BCLK	2	—	—	ns	—
S15	I2S_TX_BCLK to I2S_TXD/ I2S_TX_FS output valid	—	—	18.5	ns	VDD1/VDD2 ≥ 1.0 V
S15	I2S_TX_BCLK to I2S_TXD/ I2S_TX_FS output valid	—	—	18.5	ns	VDD1/VDD2 ≥ 0.9 V

Table continues on the next page...

Table 73. I2S/I2S Target mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
S15	I2S_TX_BCLK to I2S_TXD/ I2S_TX_FS output valid	—	—	20	ns	VDD1/VDD2 ≥ 0.8 V
S15	I2S_TX_BCLK to I2S_TXD/ I2S_TX_FS output valid	—	—	51.5	ns	VDD1/VDD2 ≥ 0.7 V
S16	I2S_TX_BCLK to I2S_TXD/ I2S_TX_FS output invalid	0	—	—	ns	—
S17	I2S_RXD setup before I2S_RX_BCLK	6	—	—	ns	—
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	—	ns	—
S19	I2S_TX_FS input assertion to I2S_TXD output valid [1]	—	—	18.5	ns	—

[1] Applies to first in each frame and only if the TCR4[FSE] bit is clear.

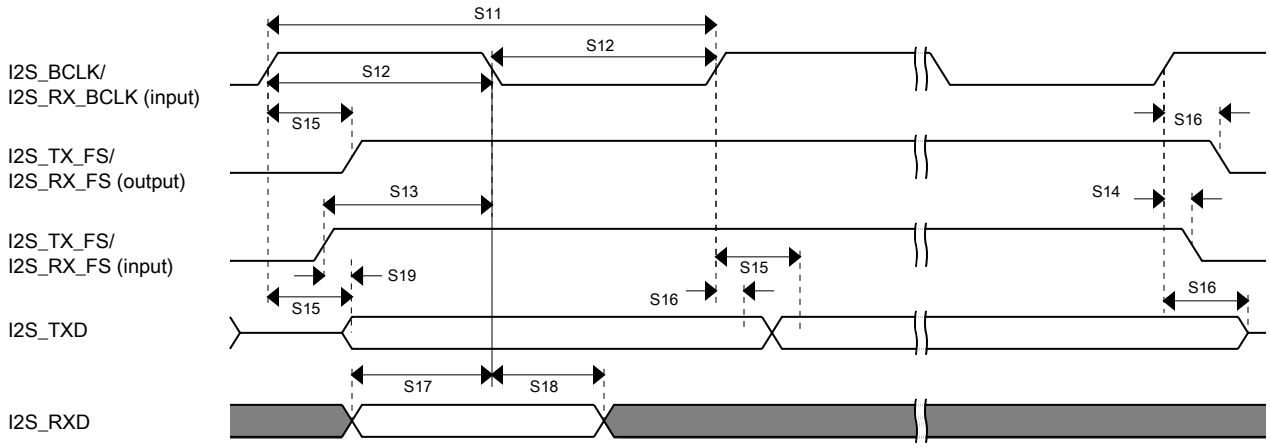


Figure 37. I2S/SAI timing - Target mode

3.7.6 LPSPI interface

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, respective domain main clocks, and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI controller mode (transmit/receive) is 33 Mbit/s. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI target mode (receive) is 33 Mbit/s and for SPI peripheral mode (transmit) is 15 Mbit/s.

Standard LPSPI—Configurable via the Flexcomm (LPSPI0-13 in Compute Domain & LPSPI17-20 in the Sense Domain)

3.7.6.1 LPSPI DC electrical specifications

Table 74. LPSPI DC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
f	LPSPI controller in Compute/ Sense domain	—	—	33	MHz	VDD2/VDD1 ≥ 1.0 V
f	LPSPI controller in Compute/ Sense domain	—	—	8	MHz	VDD2/VDD1 ≥ 0.7 V
f	LPSPI target transmit/receive in Compute/Sense domain	—	—	33	MHz	VDD2/VDD1 ≥ 1.0 V
f	LPSPI target transmit/receive in Compute/Sense domain	—	—	8	MHz	VDD2/VDD1 ≥ 0.7 V

3.7.6.2 LPSPI Controller mode timing (LP_FLEXCOMM0-13, 17-20)

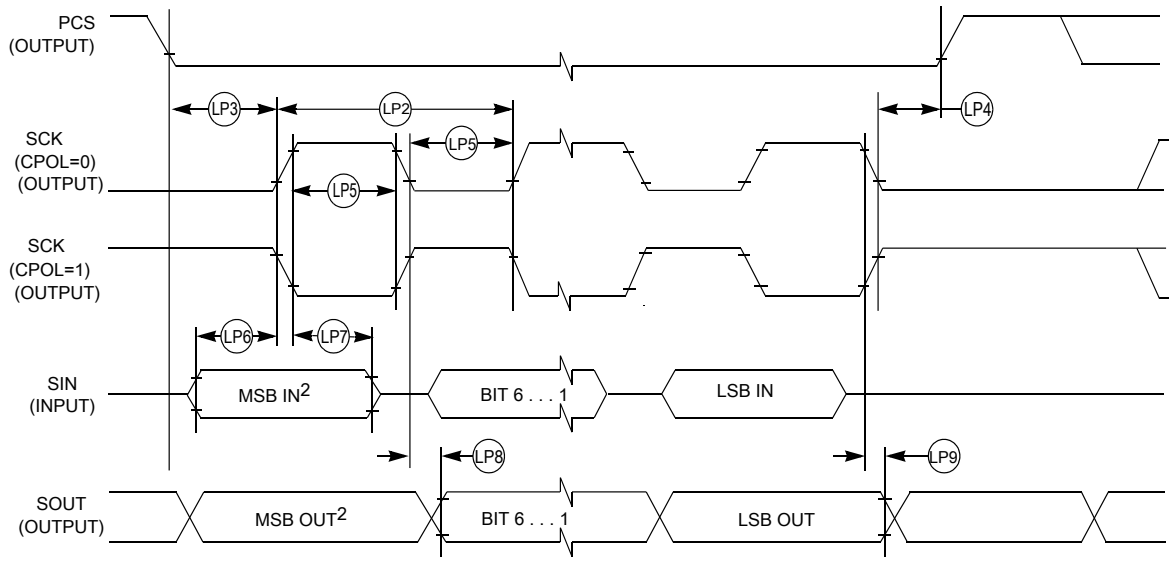
CL = 15 pF balanced loading on all pins; Input slew = 1 ns, SLEWRATE = standard mode for all pins; DRIVE = Normal output drive. Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 75. LPSPI Controller mode timing (LP_FLEXCOMM0-13, 17-20)

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency [1]	—	—	33	MHz	—
LP2	SCK period [2]	2 x tperiph	—	2048 x tperiph	ns	—
LP3	Enable lead time	1/2	—	—	tperiph	—
LP3	Enable lag time	1/2	—	—	tperiph	—
LP5	Clock (SCK) high or low time	tSCK / 2 - 3	—	tSCK / 2	ns	—
LP6	Data setup time (inputs)	8.6	—	—	ns	VDD2/VDD1 ≥ 0.8 V
LP6	Data setup time (inputs)	53	—	—	ns	VDD2/VDD1 ≥ 0.7 V
LP7	Data hold time (inputs)	2	—	—	ns	—
LP8	Data valid (after SCK edge)	—	—	9.6	ns	VDD2/VDD1 ≥ 1.0 V
LP8	Data valid (after SCK edge)	—	—	10.6	ns	VDD2/VDD1 ≥ 0.9 V
LP8	Data valid (after SCK edge)	—	—	11.8	ns	VDD2/VDD1 ≥ 0.8 V
LP8	Data valid (after SCK edge)	—	—	56	ns	VDD2/VDD1 ≥ 0.7 V
LP9	Data hold time (outputs)	0	—	—	ns	—

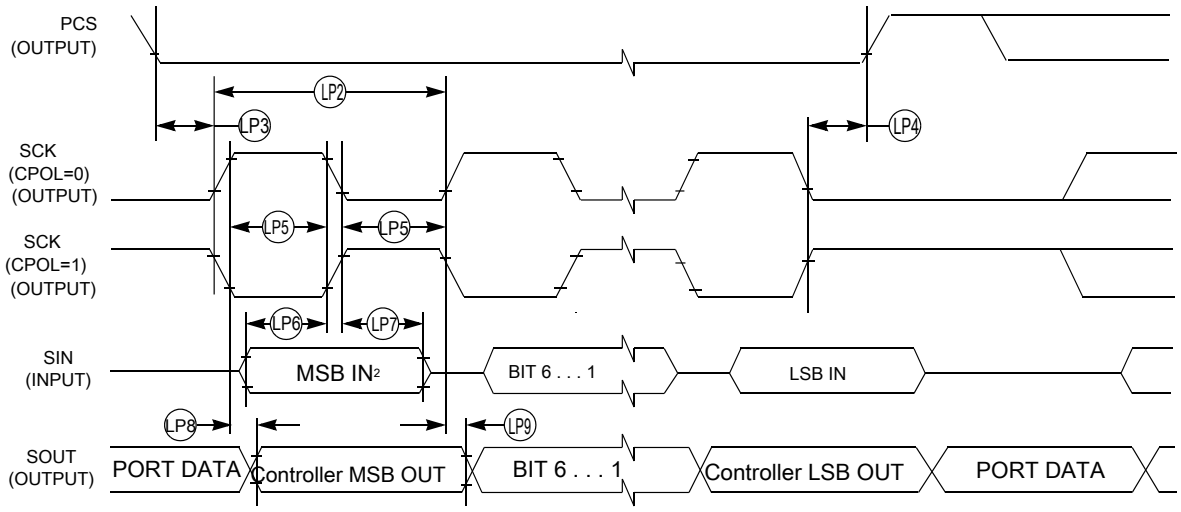
[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LP_FLEXCOMM peripheral functional clock.

[2] tperiph = 1 / fperiph



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 38. LPSPI Controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 39. LPSPI Controller mode timing (CPHA = 1)

3.7.6.3 LPSPI Peripheral mode timing (LP_FLEXCOMM0-13, 17-20)

VDDIO_x = 1.71 V to 1.89 V. VDDIO_X (X = 4,5,6) = 1.14 V to 1.89 V; CL = 15 pF balanced loading on all pins; Input slew = 1 ns, SLEWRATE = standard mode for all pins; Parameters sampled at the 50% level of the rising or falling edge. Based on simulation, not tested in production.

Table 76. LPSPI Peripheral mode timing (LP_FLEXCOMM0-13, 17-20)

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency [1]	—	—	33	MHz	—

Table continues on the next page...

Table 76. LPSPI Peripheral mode timing (LP_FLEXCOMM0-13, 17-20)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP2	SPSCK period	4 x tperiph	—	2048 x tperiph	ns	—
LP3	Enable lead time [2]	1	—	—	tperiph	—
LP4	Enable lag time [2]	1	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSPSCK / 2 - 5	—	tSPSCK / 2	ns	—
LP6	Data setup time (inputs)	3	—	—	ns	VDD2/VDD1 ≥ 1.0 V
LP6	Data setup time (inputs)	4	—	—	ns	VDD2/VDD1 ≥ 0.9 V
LP6	Data setup time (inputs)	9	—	—	ns	VDD2/VDD1 ≥ 0.8 V
LP6	Data setup time (inputs)	35	—	—	ns	VDD2/VDD1 ≥ 0.7 V
LP7	Data hold time (inputs)	3.8	—	—	ns	—
LP8	Peripheral access time [2][3]	—	—	tperiph	ns	—
LP9	Peripheral MISO disable time [2] [4]	—	—	tperiph	ns	—
LP10	Data valid (after SPSCK edge)	—	—	12.8	ns	VDD2/VDD1 ≥ 1.0 V
LP10	Data valid (after SPSCK edge)	—	—	13.4	ns	VDD2/VDD1 ≥ 0.9 V
LP10	Data valid (after SPSCK edge)	—	—	20.6	ns	VDD2/VDD1 ≥ 0.8 V
LP10	Data valid (after SPSCK edge)	—	—	45	ns	VDD2/VDD1 ≥ 0.7 V
LP11	Data hold time (outputs)	0	—	—	ns	—

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LP_FLEXCOMM peripheral functional clock.
[2] t periph = 1 / fperiph
[3] Time to data active from high-impedance state
[4] Hold time to high-impedance state

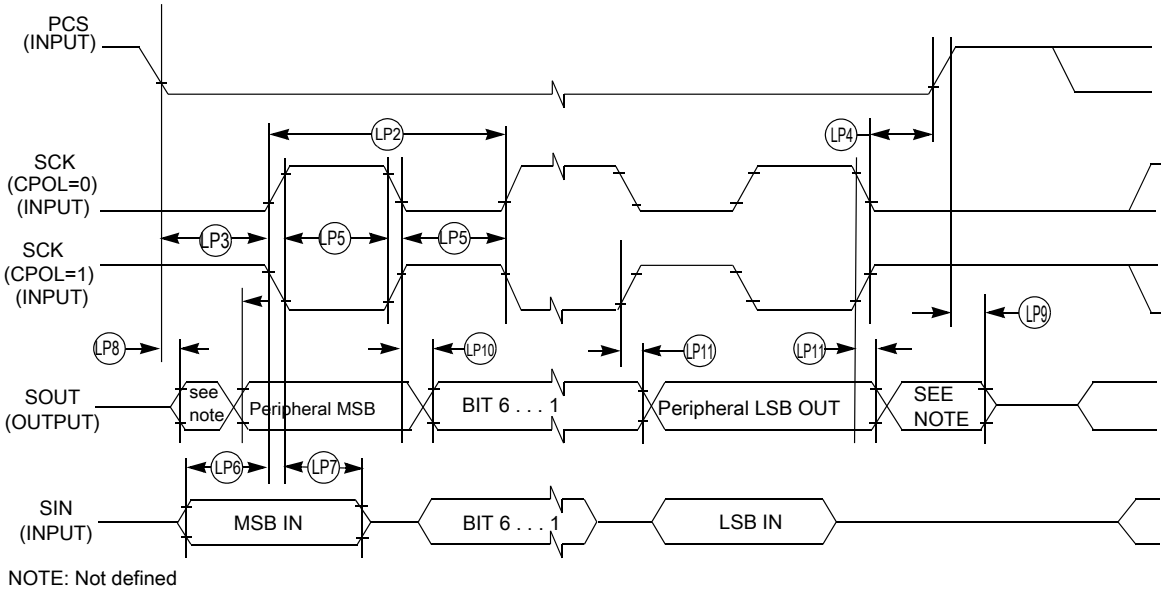


Figure 40. LPSPI Peripheral mode timing (CPHA = 0)

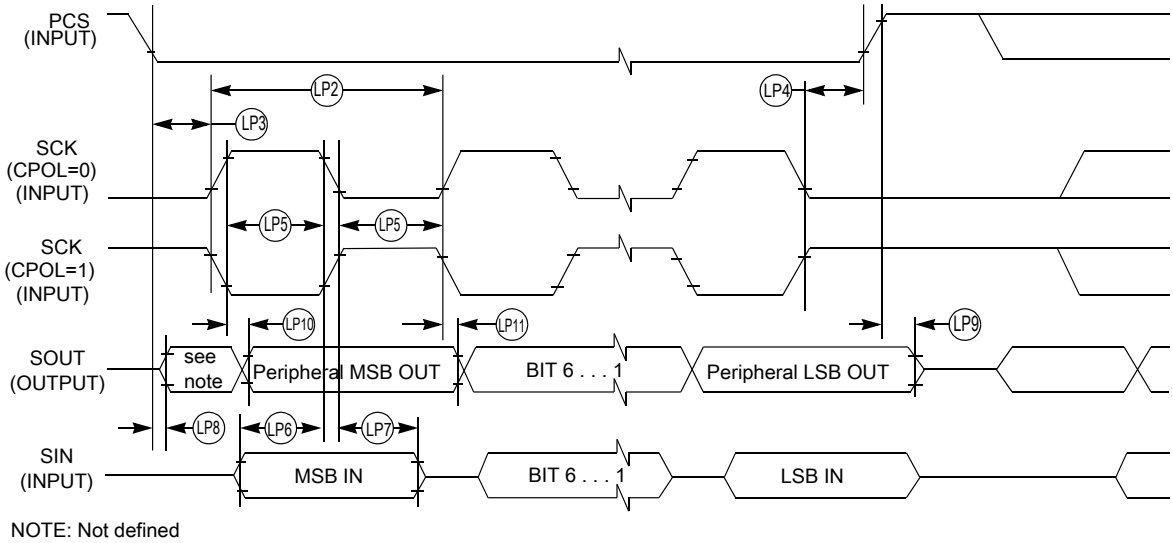


Figure 41. LPSPI Peripheral mode timing (CPHA = 1)

3.7.7 High-Speed SPI interface

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, media domain main clock (media_main_clk), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI controller mode (transmit/receive) is 60 Mbit/s. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI target mode (receive) is 60 Mbit/s and for SPI target mode (transmit) is 30 Mbit/s

3.7.7.1 High-Speed SPI interface Controller Mode timing

VDDIO_x = 1.71 V to 1.89 V. VDDIO_x = 1.71 V to 1.89 V. CL = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEWRATE = standard mode; Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

High-Speed SPI interfaces refer to LPSPI14 and LPSPI16.

Table 77. High-Speed SPI interface Controller Mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
f	SPI controller frequency in Media domain	—	—	60	MHz	VDD2 ≥ 1.0 V
f	SPI controller frequency in Media domain	—	—	12	MHz	VDD2 ≥ 0.7 V
Tcy(clk)	Clock cycle time	16.67	—	—	ns	—
tDS	Data setup time	3	—	—	ns	VDD2 ≥ 1.0 V
tDS	Data setup time	3.6	—	—	ns	VDD2 ≥ 0.9 V
tDS	Data setup time	7.6	—	—	ns	VDD2 ≥ 0.8 V
tDS	Data setup time	32	—	—	ns	VDD2 ≥ 0.7 V
tDH	Data hold time	2	—	—	ns	—
tV(Q)	Data output valid time	—	—	4.5	ns	VDD2 ≥ 1.0 V
tV(Q)	Data output valid time	—	—	4.5	ns	VDD2 ≥ 0.9 V
tV(Q)	Data output valid time	—	—	7.7	ns	VDD2 ≥ 0.8 V
tV(Q)	Data output valid time	—	—	36	ns	VDD2 ≥ 0.7 V
tH(Q)	Data output hold time	0	—	—	ns	—

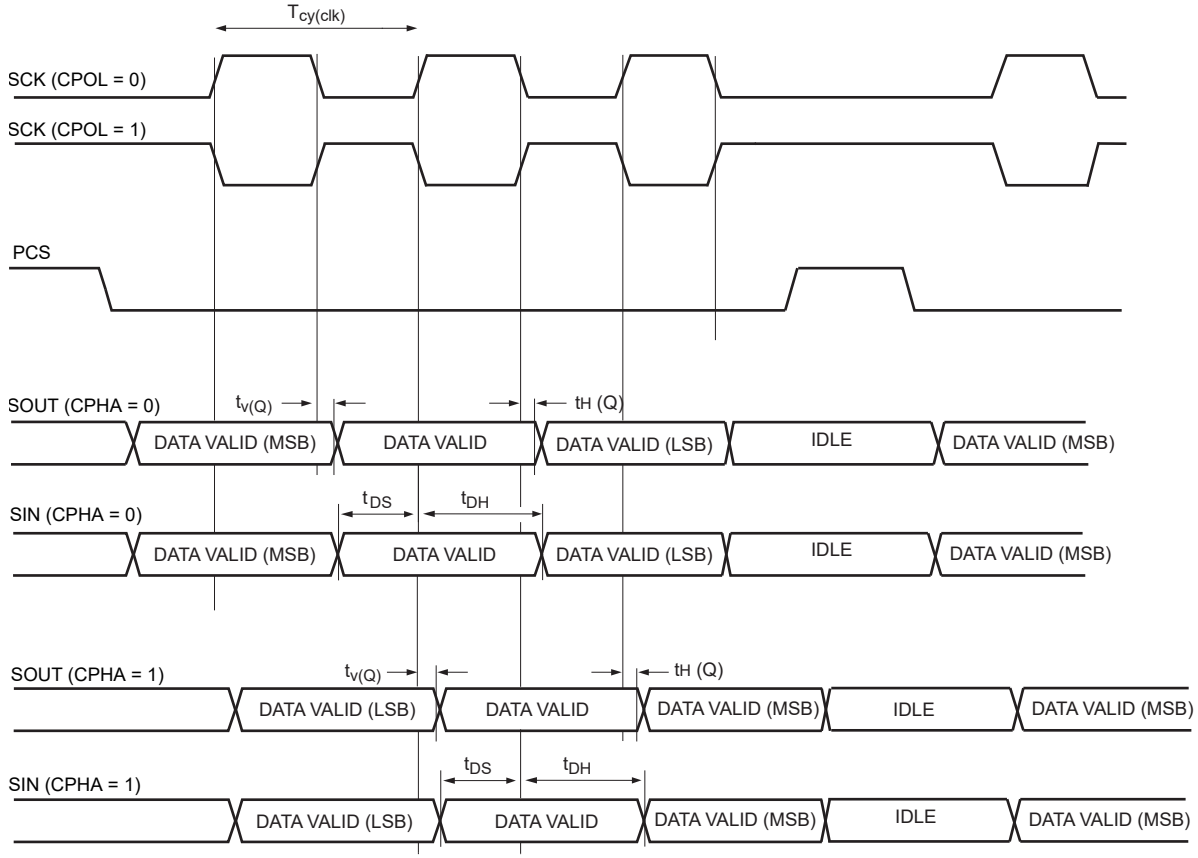


Figure 42. SPI Controller timing

3.7.7.2 High-Speed SPI interface Peripheral Mode timing

VDDIO_x = 1.71 V to 1.89 V. CL = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEWRATE = standard mode; Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

HS SPI interfaces refer to LPSPI 14 and LPSPI 16.

Table 78. High-Speed SPI interface Peripheral Mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
f	SPI peripheral receive in Media domain	—	—	60	MHz	VDD2 ≥ 1.0 V
f	SPI peripheral receive in Media domain	—	—	12	MHz	VDD2 ≥ 0.7 V
f	SPI peripheral transmit in Media domain	—	—	30	MHz	VDD2 ≥ 1.0 V
f	SPI peripheral transmit in Media domain	—	—	12	MHz	VDD2 ≥ 0.7 V
Tcy(clk)	Clock cycle time [1]	16.67	—	—	ns	SPI Peripheral receive mode

Table continues on the next page...

Table 78. High-Speed SPI interface Peripheral Mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Tcy(clk)	Clock cycle time [1]	33.33	—	—	ns	SPI Peripheral transmit mode
tDS	Data setup time [1]	3	—	—	ns	VDD2 ≥ 1.0 V
tDS	Data setup time [1]	3	—	—	ns	VDD2 ≥ 0.9 V
tDS	Data setup time [1]	6	—	—	ns	VDD2 ≥ 0.8 V
tDS	Data setup time [1]	32	—	—	ns	VDD2 ≥ 0.7 V
tDH	Data hold time [1]	3.8	—	—	ns	—
tV(Q)	Data output valid time [1]	—	—	12.8	ns	VDD2 ≥ 1.0 V
tV(Q)	Data output valid time [1]	—	—	12.8	ns	VDD2 ≥ 0.9 V
tV(Q)	Data output valid time [1]	—	—	15.8	ns	VDD2 ≥ 0.8 V
tV(Q)	Data output valid time [1]	—	—	35	ns	VDD2 ≥ 0.7 V
tH(Q)	Data output hold time [1]	0	—	—	ns	—

[1] Based on simulation; not tested in production.

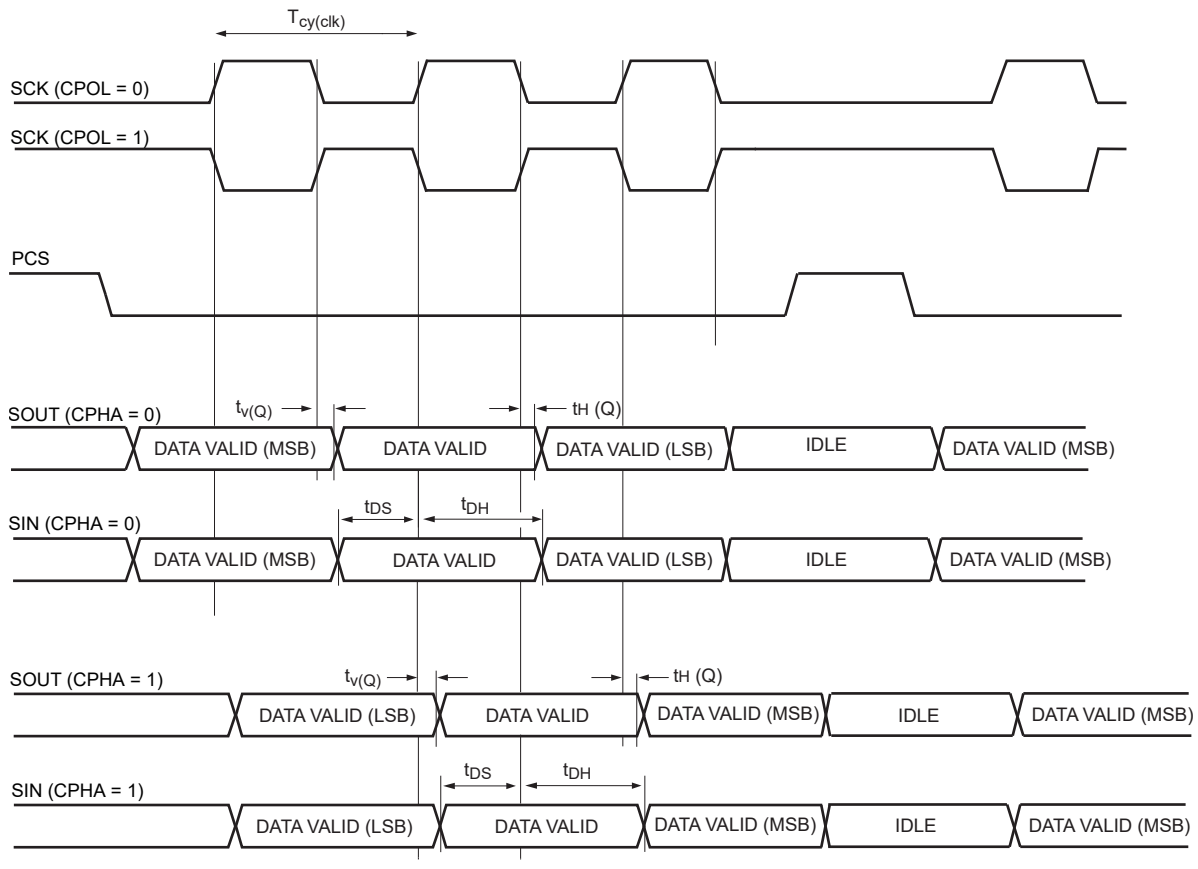


Figure 43. SPI Peripheral timing

3.7.8 PDM Microphone interface (MICFIL) timing parameters

The PDM microphones must meet the setup and hold timing requirements shown in Table 79 and Figure 44. The "k" factor value in Table 79 depends on the selected quality mode as shown in Table 80.

Note: *These timing requirements apply only if the clock divider is enabled (PDM_CTRL2[CLKDIVDIS] = 0), otherwise there are no special timing requirements.*

Table 79. PDM timing parameters

Parameter	Value
Time Rise Setup (trs), Time Fall Setup (tfs)	≤ floor (k x CLKDIV) -1 / PDM_CLK_ROOT rate [1]
Time Rise Hold (trh), TIme Fall Hold (tfh)	≥ 0

[1] Depending on value of "K", you must ensure that floor (K x CTRL_2[CLKDIV]) > 1 to avoid timing problems.

Table 80. K factor value

Quality factor	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

Figure 44 illustrates the timing requirements for the PDM.

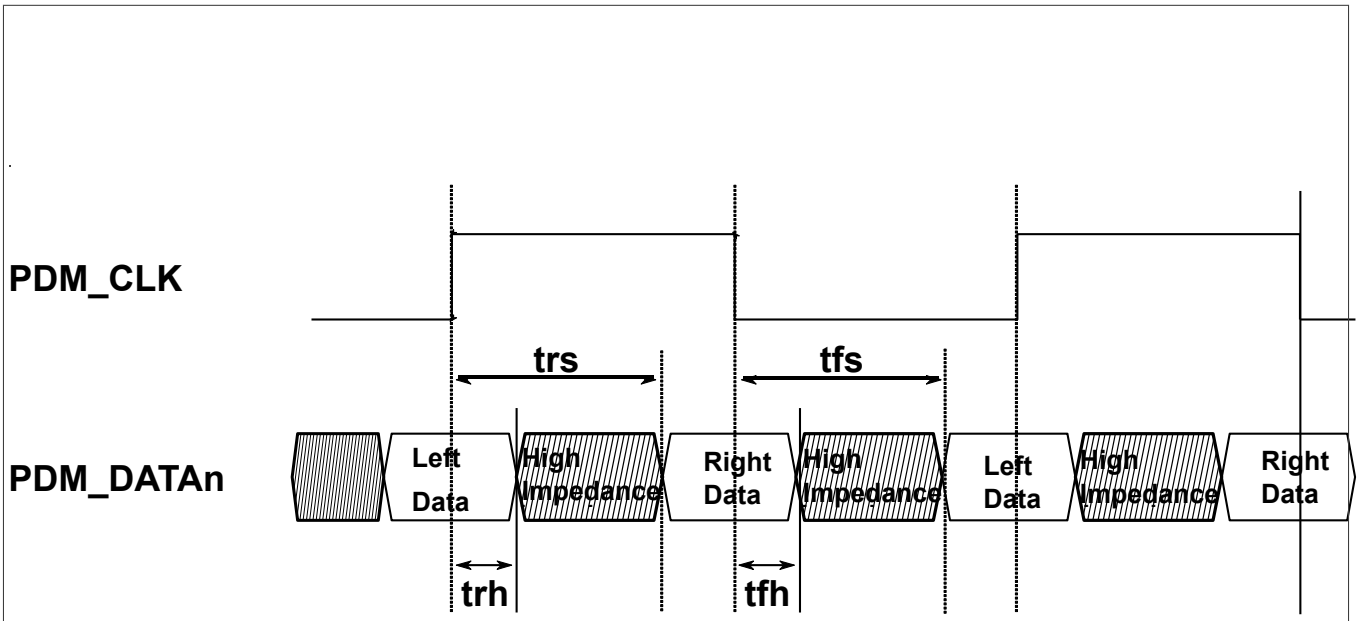


Figure 44. PDM input/output timing requirements

For more detailed information, see Section Functional description of *i.MX RT700 Crossover Microcontrollers Reference Manual* (IMXRT700RM).

3.7.9 USB interface characteristics

This section describes the USB0 and eUSB host and device with on-chip PHY. The High Speed/Full Speed (HS/FS) USB meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification. eUSB supports standard USB2.0 devices.

3.7.9.1 USB High Speed Transceiver and PHY specifications

This section describes the High Speed USB PHY parameters. The high speed PHY is capable of full speed signaling as well.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes

— Applies to: Universal Serial Bus Specification, Revision 2.0

- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - — Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - — Revision 1.2, December 7, 2010

USB0_VBUS_DETECT pin is a detector function and complies with the above specifications without needing any external voltage division components.

Note: *To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS.*

3.7.9.2 USB DCD electrical specifications

Table 81. USB DCD electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDP_SRC, VDM_SRC	USB_DP and USB_DM source voltages (up to 250 µA)	0.5	—	0.7	V	—
VLGC	Logic threshold	0.8	—	2	V	—
IDP_SRC	USB_DP source current	7	10	13	µA	—
IDM_SINK, IDP_SINK	USB_DM and USB_DP sink currents	25	—	175	µA	—
RDM_DWN	D-pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ	—
VDAT_REF	Data detect voltage	0.25	0.33	0.4	V	—

3.8 Timer modules

3.8.1 SCTimer/PWM output timing

CL = 20 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50% level of the rising or falling edge.

Table 82. SCTimer/PWM output timing

Symbol	Description	Min	Typ	Max	Unit	Condition
tsk(o)	Output skew time	—	—	2.8	ns	—

4 Pinouts

4.1 FOWLP package information

4.1.1 FOWLP package pinouts

Table 83 shows the list of contact assignments of FOWLP package.

Table 83. FOWLP package pin assignments

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
J1	PIO0_0	PIO0_0	PIO0_0	LP_FLEXCOMM8_P2	SCT0_GPIN0	SCT0_OUT0	CTIMER_C_INP9	SAI0_RX_BCLK	SAI1_TX_BCLK	—
J2	PIO0_1	PIO0_1	PIO0_1	LP_FLEXCOMM8_P3	SCT0_GPIN1	SCT0_OUT1	CTIMER0_MAT0	SAI0_RX_SYNC	SAI1_RX_DATA	—
J3	PIO0_2	PIO0_2	PIO0_2	LP_FLEXCOMM8_P4	SCT0_GPIN2	SCT0_OUT2	CTIMER0_MAT1	SAI0_RX_DATA	—	LP_FLEXCOMM9_P0
J4	PIO0_3	PIO0_3	PIO0_3	LP_FLEXCOMM4_P0	SCT0_GPIN3	SCT0_OUT3	CTIMER0_MAT2	SAI0_TX_BCLK	—	—
K4	PIO0_4	PIO0_4	PIO0_4	LP_FLEXCOMM4_P1	SCT0_GPIN4	SCT0_OUT4	CTIMER0_MAT3	SAI0_TX_DATA	—	—
K3	PIO0_5	PIO0_5	PIO0_5	LP_FLEXCOMM4_P4	SCT0_GPIN5	SCT0_OUT5	CTIMER2_MAT0	SAI0_TX_SYNC	MCLK	LP_FLEXCOMM9_P1
J5	PIO0_6	PIO0_6	PIO0_6	LP_FLEXCOMM4_P2	SCT0_GPIN6	SCT0_OUT6	CTIMER_C_INP10	LP_FLEXCOMM8_P0	—	—
K5	PIO0_7	PIO0_7	PIO0_7	LP_FLEXCOMM4_P3	SCT0_GPIN7	SCT0_OUT7	CTIMER_C_INP11	LP_FLEXCOMM8_P1	—	—
L7	PIO0_9	PIO0_9	PIO0_9	LP_FLEXCOMM4_P6	SCT0_GPIN1	SCT0_OUT1	CTIMER0_MAT0	LP_FLEXCOMM1_P5	—	—
L6	PIO0_10	PIO0_10	PIO0_10	LP_FLEXCOMM5_P0	SCT0_GPIN4	SCT0_OUT4	CTIMER1_MAT0	CTIMER_C_INP0	SAI2_RX_DATA	—
L4	PIO0_11	PIO0_11	PIO0_11	LP_FLEXCOMM5_P1	SCT0_GPIN5	SCT0_OUT5	CTIMER1_MAT1	SAI2_TX_BCLK	—	—
L5	PIO0_12	PIO0_12	PIO0_12	LP_FLEXCOMM5_P2	SCT0_GPIN6	SCT0_OUT6	CTIMER1_MAT2	SAI2_TX_DATA	—	—
L3	PIO0_13	PIO0_13	PIO0_13	LP_FLEXCOMM5_P3	SCT0_GPIN7	SCT0_OUT7	CTIMER1_MAT3	SAI2_TX_SYNC	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
L1	PIO0_14	PIO0_14	PIO0_14	LP_FLEXCOMM5_P4	SCT0_GPIN0	SCT0_OUT8	CTIMER_C_INP2	SAI2_RX_DATA	CLKOUT_VDD2	—
L2	PIO0_15	PIO0_15	PIO0_15	LP_FLEXCOMM5_P5	SCT0_GPIN2	SCT0_OUT2	CTIMER_C_INP3	SAI2_RX_BCLK	LP_FLEXCOMM2_P5	—
M6	PIO0_16	PIO0_16	PIO0_16	LP_FLEXCOMM5_P6	SCT0_GPIN3	SCT0_OUT3	CTIMER0_MAT1	SAI2_RX_SYNC	LP_FLEXCOMM2_P6	—
N6	PIO0_17	PIO0_17	PIO0_17	LP_FLEXCOMM6_P5	SCT0_GPIN0	SCT0_OUT0	CTIMER2_MAT0	SAI1_RX_BCLK	—	—
M7	PIO0_18	PIO0_18	PIO0_18	LP_FLEXCOMM6_P6	SCT0_GPIN1	SCT0_OUT1	CTIMER2_MAT1	SAI1_RX_DATA	—	—
M8	PIO0_19	PIO0_19	PIO0_19	LP_FLEXCOMM6_P2	SCT0_GPIN2	SCT0_OUT2	CTIMER2_MAT2	SAI1_RX_SYNC	—	—
M9	PIO0_20	PIO0_20	PIO0_20	LP_FLEXCOMM6_P3	SCT0_GPIN3	SCT0_OUT3	CTIMER2_MAT3	SAI1_TX_BCLK	—	—
M2	PIO0_21	PIO0_21	PIO0_21	LP_FLEXCOMM6_P0	SCT0_GPIN6	SCT0_OUT6	CTIMER_C_INP4	SAI1_TX_DATA	MCLK	—
M3	PIO0_22	PIO0_22	PIO0_22	LP_FLEXCOMM6_P1	SCT0_GPIN4	SCT0_OUT4	CTIMER_C_INP5	SAI1_TX_SYNC	CLKOUT_VDD2	—
N4	PIO0_31	PIO0_31	PIO0_31	LP_FLEXCOMM0_P0	UTICK0_CAP2	SCT0_OUT8	CTIMER4_MAT0	—	—	—
N5	PIO1_0	PIO1_0	PIO1_0	LP_FLEXCOMM0_P1	—	SCT0_OUT9	CTIMER4_MAT1	—	—	—
T7	PIO1_2	PIO1_2	PIO1_2	LP_FLEXCOMM0_P3	SCT0_GPIN0	SCT0_OUT6	CTIMER4_MAT3	LP_FLEXCOMM9_P5	CLKOUT_VDD1	—
P6	PIO1_3	PIO1_3	PIO1_3	LP_FLEXCOMM0_P4	SCT0_GPIN1	SCT0_OUT7	CTIMER_C_INP8	LP_FLEXCOMM9_P6	32KHZ_CLKOUT	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
T4	PIO1_4	PIO1_4	PIO1_4	LP_FLEXCOMM0_P5	SCT0_GPIN2	SCT0_OUT8	CTIMER1_MAT0	LP_FLEXCOMM9_P3	—	—
T3	PIO1_5	PIO1_5	PIO1_5	LP_FLEXCOMM0_P6	SCT0_GPIN3	SCT0_OUT9	CTIMER1_MAT1	LP_FLEXCOMM9_P4	—	—
N2	PIO1_6	PIO1_6	PIO1_6	LP_FLEXCOMM1_P4	SCT0_GPIN4	SCT0_OUT0	CTIMER_C_INP12	I3C1_PUR	32KHZ_CLKOUT	—
N3	PIO1_7	PIO1_7	PIO1_7	LP_FLEXCOMM1_P0	SCT0_GPIN5	SCT0_OUT1	CTIMER_C_INP13	I3C1_SDA	—	—
N1	PIO1_8	PIO1_8	PIO1_8	LP_FLEXCOMM1_P1	SCT0_GPIN6	SCT0_OUT2	CTIMER_C_INP14	I3C1_SCL	—	—
T5	PIO1_9	PIO1_9	PIO1_9	LP_FLEXCOMM1_P2	SCT0_GPIN7	SCT0_OUT3	CTIMER_C_INP15	CLKIN	CLKOUT_VDD1	—
T2	PIO1_10	PIO1_10	PIO1_10	LP_FLEXCOMM1_P3	UTICK0_CAP3	—	CTIMER2_MAT1	TRACECLK	CLKOUT_VDD1	—
R2	PIO1_11	PIO1_11	PIO1_11	LP_FLEXCOMM2_P0	—	—	CTIMER2_MAT2	TRACEDATA0	—	—
R1	PIO1_12	PIO1_12	PIO1_12	LP_FLEXCOMM2_P1	SCT0_GPIN3	SCT0_OUT9	CTIMER1_MAT1	TRACEDATA1	—	—
R3	PIO1_13	PIO1_13	PIO1_13	LP_FLEXCOMM2_P4	UTICK0_CAP1	—	CTIMER2_MAT3	TRACEDATA2	32KHZ_CLKOUT	—
P3	PIO1_14	PIO1_14	PIO1_14	LP_FLEXCOMM2_P2	—	—	CTIMER3_MAT0	TRACEDATA3	—	—
T6	PIO1_15	PIO1_15	PIO1_15	LP_FLEXCOMM2_P3	—	—	CTIMER3_MAT1	CLKIN	—	—
P5	PIO1_16	PIO1_16	PIO1_16	LP_FLEXCOMM3_P2	—	—	CTIMER3_MAT2	I3C0_PUR	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
R4	PIO1_17	PIO1_17	PIO1_17	LP_FLEXCOMM3_P1	USB0_OVERCURRENTN	—	CTIMER3_MAT3	I3C0_SCL	—	—
R5	PIO1_18	PIO1_18	PIO1_18	LP_FLEXCOMM3_P0	USB0_PORTPWRN	—	CTIMER4_MAT0	I3C0_SDA	—	—
P7	PIO1_19	PIO1_19	PIO1_19	LP_FLEXCOMM3_P3	MCLK	FREQME_GPIO_B_CLK	CTIMER4_MAT1	—	—	—
H2	PIO2_0	PIO2_0	PIO2_0	—	USB0_OVERCURRENTN	—	EZH_PIO0	FLEXIO_D0	—	LCD_DBI_CSX_AB
G2	PIO2_1	PIO2_1	PIO2_1	—	USB0_PORTPWRN	—	EZH_PIO1	FLEXIO_D1	—	LCD_DBI-DCX-AB
H3	PIO2_2	PIO2_2	PIO2_2	LPSPI16_SOUT	—	—	EZH_PIO2	FLEXIO_D2	LCD_ENABLE	LCD_DBI-DATA_OEN
G1	PIO2_3	PIO2_3	PIO2_3	LPSPI16_SCK	—	—	EZH_PIO3	FLEXIO_D3	LCD_DOTCLK	LCD_DBI-RWDX
G3	PIO2_4	PIO2_4	PIO2_4	LPSPI16_SIN	—	—	EZH_PIO4	FLEXIO_D4	LCD_HSYNC	LCD_DBI-WRX
J6	PIO2_5	PIO2_5	PIO2_5	LPSPI16_PCS0	—	—	EZH_PIO5	FLEXIO_D5	LCD_VSYNC	LCD_DBI-E
H6	PIO2_6	PIO2_6	PIO2_6	LPSPI16_PCS3	—	—	EZH_PIO6	FLEXIO_D6	LCD_D0	LCD_DBI-D0
G6	PIO2_7	PIO2_7	PIO2_7	LPSPI16_PCS2	—	—	EZH_PIO7	FLEXIO_D7	LCD_D1	LCD_DBI-D1
G4	PIO2_8	PIO2_8	PIO2_8	LPSPI16_PCS1	—	—	EZH_PIO8	FLEXIO_D8	LCD_D2	LCD_DBI-D2
G5	PIO2_9	PIO2_9	PIO2_9	—	—	—	EZH_PIO9	FLEXIO_D9	LCD_D3	LCD_DBI-D3
F5	PIO2_10	PIO2_10	PIO2_10	—	—	—	EZH_PIO10	FLEXIO_D10	LCD_D4	LCD_DBI-D4
F3	PIO2_11	PIO2_11	PIO2_11	—	—	—	EZH_PIO11	FLEXIO_D11	LCD_D5	LCD_DBI-D5
E3	PIO2_12	PIO2_12	PIO2_12	—	—	—	EZH_PIO12	FLEXIO_D12	LCD_D6	LCD_DBI-D6

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
E4	PIO2_13	PIO2_13	PIO2_13	—	—	—	EZH_PIO 13	FLEXIO_ D13	LCD_D7	LCD_DBI-D7
D4	PIO2_14	PIO2_14	PIO2_14	—	—	—	EZH_PIO 14	FLEXIO_ D14	LOW_FR EQ_CLK OUT	—
D3	PIO2_15	PIO2_15	PIO2_15	—	—	—	EZH_PIO 15	FLEXIO_ D15	LOW_FR EQ_CLK OUT_N	—
E1	PIO3_0	PIO3_0	PIO3_0	LPSPI14_ SOUT	—	—	EZH_PIO 16	—	—	—
E2	PIO3_1	PIO3_1	PIO3_1	LPSPI14_ SCK	—	—	EZH_PIO 17	—	—	—
D2	PIO3_2	PIO3_2	PIO3_2	LPSPI14_ SIN	—	—	EZH_PIO 18	—	—	—
C3	PIO3_3	PIO3_3	PIO3_3	LPSPI14_ PCS0	—	—	EZH_PIO 19	—	—	—
K6	PIO3_4	PIO3_4	PIO3_4	LPSPI14_ PCS3	LP_FLEX COMM0_ P4	LP_FLEX COMM3_ P2	EZH_PIO 20	—	—	—
K7	PIO3_5	PIO3_5	PIO3_5	LPSPI14_ PCS2	LP_FLEX COMM0_ P5	LP_FLEX COMM3_ P3	EZH_PIO 21	—	—	—
J7	PIO3_6	PIO3_6	PIO3_6	LPSPI14_ PCS1	LP_FLEX COMM0_ P6	LP_FLEX COMM9_ P2	EZH_PIO 22	I3C0_PU R	—	—
H7	PIO3_7	PIO3_7	PIO3_7	LP_FLEX COMM0_ P2	—	LP_FLEX COMM5_ P5	EZH_PIO 23	—	—	—
G7	PIO3_8	PIO3_8	PIO3_8	LP_FLEX COMM0_ P3	—	LP_FLEX COMM5_ P6	EZH_PIO 24	—	—	—
G8	PIO3_9	PIO3_9	PIO3_9	LP_FLEX COMM6_ P2	—	LP_FLEX COMM3_ P4	EZH_PIO 25	—	—	—
G9	PIO3_10	PIO3_10	PIO3_10	LP_FLEX COMM6_ P3	USB0_O VERCUR RENTN	LP_FLEX COMM3_ P5	EZH_PIO 26	—	—	—
F9	PIO3_11	PIO3_11	PIO3_11	LP_FLEX COMM6_ P4	USB0_P ORTPWR N	LP_FLEX COMM9_ P3	EZH_PIO 27	I3C1_PU R	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
D8	PIO4_0	PIO4_0	PIO4_0	XSPI2_SS0_N	LP_FLEXCOMM8_P0	—	—	—	—	—
D9	PIO4_1	PIO4_1	PIO4_1	XSPI2_DATA0	LP_FLEXCOMM8_P1	—	—	—	LCD_D20	—
C11	PIO4_2	PIO4_2	PIO4_2	XSPI2_DATA1	LP_FLEXCOMM8_P2	—	—	—	LCD_D21	—
C10	PIO4_3	PIO4_3	PIO4_3	XSPI2_DATA2	LP_FLEXCOMM8_P3	—	—	—	LCD_D22	—
C9	PIO4_4	PIO4_4	PIO4_4	XSPI2_DATA3	LP_FLEXCOMM8_P4	—	—	—	LCD_D23	—
A10	PIO4_5	PIO4_5	PIO4_5	XSPI2_DQS0	LP_FLEXCOMM8_P5	—	—	—	—	—
C8	PIO4_6	PIO4_6	PIO4_6	XSPI2_DATA4	LP_FLEXCOMM8_P6	—	—	—	LCD_D16	—
C13	PIO4_7	PIO4_7	PIO4_7	XSPI2_DATA5	LP_FLEXCOMM9_P0	—	—	—	LCD_D17	—
B12	PIO4_8	PIO4_8	PIO4_8	XSPI2_DATA6	LP_FLEXCOMM9_P1	—	—	—	LCD_D18	—
C12	PIO4_9	PIO4_9	PIO4_9	XSPI2_DATA7	LP_FLEXCOMM9_P2	—	—	—	LCD_D19	—
B10	PIO4_10	PIO4_10	PIO4_10	XSPI2_SCLK0	LP_FLEXCOMM9_P3	—	—	—	—	—
B11	PIO4_11	PIO4_11	PIO4_11	XSPI2_SCLK0_N	LP_FLEXCOMM9_P4	XSPI2_SS1_N	—	—	—	—
F11	PIO4_12	PIO4_12	PIO4_12	XSPI2_DATA8	LP_FLEXCOMM9_P5	—	—	—	LCD_D8	LCD_DBI-D8

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
E8	PIO4_13	PIO4_13	PIO4_13	XSPI2_DATA9	LP_FLEXCOMM9_P6	—	—	—	LCD_D9	LCD_DBI-D9
E12	PIO4_14	PIO4_14	PIO4_14	XSPI2_DATA10	LP_FLEXCOMM10_P0	—	—	—	LCD_D10	LCD_DBI-D10
E10	PIO4_15	PIO4_15	PIO4_15	XSPI2_DATA11	LP_FLEXCOMM10_P1	—	—	—	LCD_D11	LCD_DBI-D11
F10	PIO4_16	PIO4_16	PIO4_16	XSPI2_DQS1	LP_FLEXCOMM10_P2	—	—	—	—	—
F12	PIO4_17	PIO4_17	PIO4_17	XSPI2_DATA12	LP_FLEXCOMM10_P3	—	—	—	LCD_D12	LCD_DBI-D12
E9	PIO4_18	PIO4_18	PIO4_18	XSPI2_DATA13	LP_FLEXCOMM10_P4	—	—	—	LCD_D13	LCD_DBI-D13
D12	PIO4_19	PIO4_19	PIO4_19	XSPI2_DATA14	LP_FLEXCOMM10_P5	—	—	—	LCD_D14	LCD_DBI-D14
D10	PIO4_20	PIO4_20	PIO4_20	XSPI2_DATA15	LP_FLEXCOMM10_P6	—	—	—	LCD_D15	LCD_DBI-D15
H13	PIO5_0	PIO5_0	PIO5_0	XSPI1_SS0_N	LP_FLEXCOMM13_P4	—	—	—	—	—
H17	PIO5_1	PIO5_1	PIO5_1	XSPI1_DATA0	LP_FLEXCOMM13_P5	—	—	—	—	—
H18	PIO5_2	PIO5_2	PIO5_2	XSPI1_DATA1	LP_FLEXCOMM13_P6	—	—	—	—	—
F18	PIO5_3	PIO5_3	PIO5_3	XSPI1_DATA2	LP_FLEXCOMM13_P0	—	—	—	—	—
F16	PIO5_4	PIO5_4	PIO5_4	XSPI1_DATA3	LP_FLEXCOMM13_P1	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
G16	PIO5_5	PIO5_5	PIO5_5	XSPI1_DQS0	LP_FLEXCOMM13_P2	—	—	—	—	—
E16	PIO5_6	PIO5_6	PIO5_6	XSPI1_DATA4	LP_FLEXCOMM12_P3	—	—	—	—	—
K16	PIO5_7	PIO5_7	PIO5_7	XSPI1_DATA5	LP_FLEXCOMM12_P0	—	—	—	—	—
H16	PIO5_8	PIO5_8	PIO5_8	XSPI1_DATA6	LP_FLEXCOMM12_P1	—	—	—	—	—
J16	PIO5_9	PIO5_9	PIO5_9	XSPI1_DATA7	LP_FLEXCOMM12_P2	—	—	—	—	—
F17	PIO5_10	PIO5_10	PIO5_10	XSPI1_SCLK0	LP_FLEXCOMM13_P3	—	—	—	—	—
G17	PIO5_11	PIO5_11	PIO5_11	XSPI1_SCLK0_N	LP_FLEXCOMM12_P4	XSPI1_SS1_N	—	—	—	—
K15	PIO5_12	PIO5_12	PIO5_12	XSPI1_DATA8	LP_FLEXCOMM12_P5	—	—	—	—	—
H15	PIO5_13	PIO5_13	PIO5_13	XSPI1_DATA9	LP_FLEXCOMM12_P6	—	—	—	—	—
M13	PIO5_14	PIO5_14	PIO5_14	XSPI1_DATA10	LP_FLEXCOMM11_P0	—	—	—	—	—
J14	PIO5_15	PIO5_15	PIO5_15	XSPI1_DATA11	LP_FLEXCOMM11_P1	—	—	—	—	—
J15	PIO5_16	PIO5_16	PIO5_16	XSPI1_DQS1	LP_FLEXCOMM11_P2	—	—	—	—	—
K13	PIO5_17	PIO5_17	PIO5_17	XSPI1_DATA12	LP_FLEXCOMM11_P3	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
H14	PIO5_18	PIO5_18	PIO5_18	XSPI1_DATA13	LP_FLEXCOMM11_P4	—	—	—	—	—
L13	PIO5_19	PIO5_19	PIO5_19	XSPI1_DATA14	LP_FLEXCOMM11_P5	—	—	—	—	—
k14	PIO5_20	PIO5_20	PIO5_20	XSPI1_DATA15	LP_FLEXCOMM11_P6	—	—	—	—	—
D16	PIO6_0	PIO6_0	PIO6_0	XSPI0_SCLK0_N	LP_FLEXCOMM7_P2	—	—	—	—	—
D17	PIO6_1	PIO6_1	PIO6_1	XSPI0_SCLK0	LP_FLEXCOMM10_P0	—	—	—	—	—
G11	PIO6_2	PIO6_2	PIO6_2	XSPI0_SS0_N	LP_FLEXCOMM10_P1	—	—	—	—	—
F13	PIO6_3	PIO6_3	PIO6_3	XSPI0_DATA0	LP_FLEXCOMM10_P2	—	—	—	—	—
D14	PIO6_4	PIO6_4	PIO6_4	XSPI0_DATA1	LP_FLEXCOMM10_P3	—	—	—	—	—
C15	PIO6_5	PIO6_5	PIO6_5	XSPI0_DATA2	LP_FLEXCOMM10_P4	—	—	—	—	—
E13	PIO6_6	PIO6_6	PIO6_6	XSPI0_DATA3	LP_FLEXCOMM10_P5	—	—	—	—	—
D15	PIO6_7	PIO6_7	PIO6_7	XSPI0_DQS0	LP_FLEXCOMM10_P6	—	—	—	—	—
G13	PIO6_8	PIO6_8	PIO6_8	XSPI0_DATA4	LP_FLEXCOMM13_P0	LP_FLEXCOMM11_P2	—	—	—	—
F15	PIO6_9	PIO6_9	PIO6_9	XSPI0_DATA5	LP_FLEXCOMM13_P1	LP_FLEXCOMM11_P3	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
E14	PIO6_10	PIO6_10	PIO6_10	XSPI0_DATA6	LP_FLEXCOMM13_P2	LP_FLEXCOMM11_P0	—	—	—	—
F14	PIO6_11	PIO6_11	PIO6_11	XSPI0_DATA7	LP_FLEXCOMM13_P3	LP_FLEXCOMM11_P1	—	—	—	—
G10	PIO6_12	PIO6_12	PIO6_12	XSPI0_SS1_N	—	—	—	—	—	—
B6	PIO7_0	PIO7_0	PIO7_0	SDHC0_CLK	LP_FLEXCOMM3_P4	LP_FLEXCOMM7_P6	—	—	—	—
C7	PIO7_1	PIO7_1	PIO7_1	SDHC0_CMD	LP_FLEXCOMM3_P5	LP_FLEXCOMM7_P5	—	—	—	—
F7	PIO7_2	PIO7_2	PIO7_2	SDHC0_DATA4	LP_FLEXCOMM12_P0	—	—	—	—	—
F6	PIO7_3	PIO7_3	PIO7_3	SDHC0_DATA5	LP_FLEXCOMM12_P1	—	—	—	—	—
E6	PIO7_4	PIO7_4	PIO7_4	SDHC0_DATA6	LP_FLEXCOMM12_P2	—	—	—	—	—
D6	PIO7_5	PIO7_5	PIO7_5	SDHC0_DATA7	LP_FLEXCOMM12_P3	—	—	—	—	—
B7	PIO7_6	PIO7_6	PIO7_6	SDHC0_DATA0	LP_FLEXCOMM12_P4	—	—	—	—	—
B8	PIO7_7	PIO7_7	PIO7_7	SDHC0_DATA1	LP_FLEXCOMM12_P5	—	—	—	—	—
C6	PIO7_8	PIO7_8	PIO7_8	SDHC0_DATA2	LP_FLEXCOMM12_P6	LP_FLEXCOMM7_P3	—	—	—	—
A6	PIO7_9	PIO7_9	PIO7_9	SDHC0_DATA3	LP_FLEXCOMM3_P6	LP_FLEXCOMM7_P4	—	—	—	—
E5	PIO7_10	PIO7_10	PIO7_10	SDHC0_WR_PRT	LP_FLEXCOMM1_P0	—	—	SDHC0_DS	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
C5	PIO7_11	PIO7_11	PIO7_11	SDHC0_CARD_DET_N	LP_FLEXCOMM1_P1	—	—	—	—	—
F8	PIO7_12	PIO7_12	PIO7_12	SDHC0_RESET_N	LP_FLEXCOMM1_P2	—	—	—	—	—
P15	PIO7_13	PIO7_13	PIO7_13	SDHC1_DATA4	LP_FLEXCOMM1_P3	—	—	—	—	—
P14	PIO7_14	PIO7_14	PIO7_14	SDHC1_DATA5	LP_FLEXCOMM7_P0	—	—	—	—	—
M14	PIO7_15	PIO7_15	PIO7_15	SDHC1_DATA6	LP_FLEXCOMM7_P1	—	—	—	—	—
M15	PIO7_16	PIO7_16	PIO7_16	SDHC1_DATA7	LP_FLEXCOMM7_P2	—	—	—	—	—
L17	PIO7_17	PIO7_17	PIO7_17	SDHC1_CLK	LP_FLEXCOMM2_P0	—	—	—	—	—
L16	PIO7_18	PIO7_18	PIO7_18	SDHC1_CMD	LP_FLEXCOMM2_P1	—	—	—	—	—
M17	PIO7_19	PIO7_19	PIO7_19	SDHC1_DATA0	LP_FLEXCOMM1_P4	LP_FLEXCOMM7_P3	—	—	—	—
M18	PIO7_20	PIO7_20	PIO7_20	SDHC1_DATA1	LP_FLEXCOMM1_P5	LP_FLEXCOMM2_P4	—	—	—	—
K18	PIO7_21	PIO7_21	PIO7_21	SDHC1_DATA2	LP_FLEXCOMM1_P6	LP_FLEXCOMM2_P5	—	—	—	—
K17	PIO7_22	PIO7_22	PIO7_22	SDHC1_DATA3	LP_FLEXCOMM2_P2	—	—	—	—	—
N14	PIO7_23	PIO7_23	PIO7_23	SDHC1_WR_PRT	LP_FLEXCOMM2_P3	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
G12	PIO7_24	PIO7_24	PIO7_24	SDHC1_CARD_DET_N	LP_FLEXCOMM13_P4	—	—	—	—	—
H12	PIO7_25	PIO7_25	PIO7_25	SDHC1_RESET_N	LP_FLEXCOMM13_P5	LP_FLEXCOMM2_P6	—	—	—	—
U12	PIO8_0	JTAG_TCK/SWCLK	PIO8_0	LP_FLEXCOMM17_P5	CTIMER_S_INP0	—	—	JTAG_TCK/SWCLK	—	—
T12	PIO8_1	JTAG_TMS/SWDIO	PIO8_1	LP_FLEXCOMM17_P6	CTIMER5_MAT0	—	—	JTAG_TMS/SWDIO	—	—
U11	PIO8_2	JTAG_TDI	PIO8_2	LP_FLEXCOMM17_P2	CTIMER5_MAT1	—	—	JTAG_TDI	—	—
V11	PIO8_3	JTAG_TD0/SWO	PIO8_3	LP_FLEXCOMM17_P3	CTIMER_S_INP1	UTICK1_CAP0	—	JTAG_TD0/SWO	—	—
V13	PIO8_4	JTAG_TRSTN	PIO8_4	LP_FLEXCOMM17_P4	CTIMER5_MAT2	MCLK	—	JTAG_TRSTN	—	—
U13	PIO8_5	PIO8_5	PIO8_5	LP_FLEXCOMM17_P0	CTIMER5_MAT3	CTIMER_S_INP0	—	—	—	—
T13	PIO8_6	PIO8_6	PIO8_6	LP_FLEXCOMM17_P1	CTIMER6_MAT0	—	CMP0_OUT	—	—	—
M16	PIO8_7	PIO8_7	PIO8_7	LP_FLEXCOMM18_P0	CTIMER6_MAT1	—	—	—	—	—
T11	PIO8_8	PIO8_8	PIO8_8	LP_FLEXCOMM18_P1	CTIMER_S_INP2	—	—	—	—	—
N13	PIO8_9	PIO8_9	PIO8_9	LP_FLEXCOMM18_P2	CTIMER_S_MAT2	—	—	—	—	—
N12	PIO8_10	PIO8_10	PIO8_10	LP_FLEXCOMM18_P3	CTIMER_S_INP3	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
N11	PIO8_11	PIO8_11	PIO8_11	LP_FLEXCOMM18_P4	CTIMER6_MAT3	UTICK1_CAP1	LP_FLEXCOMM17_P4	—	—	—
P11	PIO8_12	PIO8_12	PIO8_12	LP_FLEXCOMM18_P5	CTIMER7_MAT0	CTIMER_S_INP1	LP_FLEXCOMM17_P2	—	—	—
R11	PIO8_13	PIO8_13	PIO8_13	LP_FLEXCOMM18_P6	CTIMER7_MAT1	CTIMER_S_INP3	LP_FLEXCOMM17_P3	—	—	—
R10	PIO8_14	PIO8_14	PIO8_14	LP_FLEXCOMM19_P0	CTIMER7_MAT2	SAI3_TX_SYNC	I3C2_SDA	—	—	—
T10	PIO8_15	PIO8_15	PIO8_15	LP_FLEXCOMM19_P1	CTIMER7_MAT3	SAI3_TX_BCLK	I3C2_SCL	—	—	—
T9	PIO8_16	PIO8_16	PIO8_16	LP_FLEXCOMM19_P2	CTIMER_S_INP4	SAI3_TX_DATA	I3C2_PUR	—	—	—
U9	PIO8_17	PIO8_17	PIO8_17	LP_FLEXCOMM19_P3	CTIMER_S_INP5	SAI3_RX_SYNC	—	—	—	—
P10	PIO8_18	PIO8_18	PIO8_18	LP_FLEXCOMM19_P4	CTIMER5_MAT0	CTIMER_S_INP4	—	—	—	—
P9	PIO8_19	PIO8_19	PIO8_19	LP_FLEXCOMM19_P5	CTIMER5_MAT1	CTIMER_S_INP6	CMP0_OUT	—	—	—
T8	PIO8_20	PIO8_20	PIO8_20	LP_FLEXCOMM19_P6	CTIMER_S_INP7	UTICK1_CAP2	I3C3_PUR	—	—	—
R9	PIO8_21	PIO8_21	PIO8_21	LP_FLEXCOMM20_P3	CTIMER5_MAT0	LP_FLEXCOMM3_P0	I3C3_SDA	—	—	—
N9	PIO8_22	PIO8_22	PIO8_22	LP_FLEXCOMM20_P4	CTIMER5_MAT1	LP_FLEXCOMM3_P1	I3C3_SCL	—	—	—
N16	PIO8_23	PIO8_23	PIO8_23	SAI3_RX_BCLK	CTIMER5_MAT2	LP_FLEXCOMM19_P0	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P16	PIO8_24	PIO8_24	PIO8_24	SAI3_RX_DATA	CTIMER5_MAT3	LP_FLEXCOMM19_P1	—	—	—	—
J13	PIO8_25	PIO8_25	PIO8_25	SAI3_RX_SYNC	CTIMER6_MAT0	LP_FLEXCOMM19_P2	—	—	—	—
J12	PIO8_26	PIO8_26	PIO8_26	SAI3_TX_BCLK	CTIMER6_MAT1	LP_FLEXCOMM19_P3	—	—	—	—
K12	PIO8_27	PIO8_27	PIO8_27	SAI3_TX_DATA	CTIMER6_MAT2	LP_FLEXCOMM19_P4	—	—	—	—
L12	PIO8_28	PIO8_28	PIO8_28	SAI3_TX_SYNC	CTIMER6_MAT3	LP_FLEXCOMM19_P5	—	—	—	—
P13	PIO8_30	PIO8_30	PIO8_30	LP_FLEXCOMM20_P0	CTIMER_S_INP9	UTICK1_CAP3	—	—	—	—
R13	PIO8_31	PIO8_31	PIO8_31	LP_FLEXCOMM20_P1	CTIMER7_MAT0	—	—	—	—	—
R17	PIO10_0	PIO10_0	PIO10_0	—	—	—	—	PDM_CLK	—	—
T17	PIO10_1	PIO10_1	PIO10_1	—	—	—	—	PDM_DATA01	—	—
P18	PIO10_2	PIO10_2	PIO10_2	—	—	—	—	PDM_DATA23	—	—
P17	PIO10_3	PIO10_3	PIO10_3	—	—	—	—	PDM_DATA45	—	—
R15	PIO10_4	PIO10_4	PIO10_4	—	—	—	—	PDM_DATA67	—	—
R16	PIO10_5	PIO10_5	PIO10_5	—	—	CMP0_OUT	—	—	—	—
T14	PIO10_6	PIO10_6	PIO10_6	—	—	—	—	—	—	—
T15	PIO10_7	PIO10_7	PIO10_7	—	—	—	—	—	—	—
U18	PIO10_8	PIO10_8	PIO10_8	—	—	—	—	PDM_CLK	—	—
T18	PIO10_9	PIO10_9	PIO10_9	—	—	—	—	PDM_DATA01	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
U15	PIO10_12	PIO10_12	PIO10_12	—	—	—	—	PDM_DATA67	—	—
V15	PIO10_13	PIO10_13	PIO10_13	—	—	—	—	PDM_CLK	—	—
M12	PIO10_14	PIO10_14	PIO10_14	—	—	—	—	PDM_DATA01	—	—
M11	PIO10_15	PIO10_15	PIO10_15	—	—	—	—	PDM_DATA23	—	—
M10	PIO10_16	PIO10_16	PIO10_16	—	—	—	—	PDM_DATA45	—	—
N10	PIO10_17	PIO10_17	PIO10_17	—	—	—	—	PDM_DATA67	—	—
A17	EUSB_DM	EUSB_DM	—	—	—	—	—	—	—	—
A16	EUSB_DP	EUSB_DM	—	—	—	—	—	—	—	—
V8	LX_DCDC	LX_DCDC	—	—	—	—	—	—	—	—
B3	MIPI_DSI_CLKN	MIPI_DSI_CLKN	—	—	—	—	—	—	—	—
B2	MIPI_DSI_CLKP	MIPI_DSI_CLKP	—	—	—	—	—	—	—	—
B4	MIPI_DSI_D0N	MIPI_DSI_D0N	—	—	—	—	—	—	—	—
A4	MIPI_DSI_D0P	MIPI_DSI_D0P	—	—	—	—	—	—	—	—
B1	MIPI_DSI_D1N	MIPI_DSI_D1N	—	—	—	—	—	—	—	—
A2	MIPI_DSI_D1P	MIPI_DSI_D1P	—	—	—	—	—	—	—	—
U8	PMIC_I2C_SCL	PMIC_I2C_SCL	—	—	—	—	—	—	—	—
U7	PMIC_I2C_SDA	PMIC_I2C_SDA	—	—	—	—	—	—	—	—
N8	PMIC_IRQN	PMIC_IRQN	—	—	—	—	—	—	—	—
N7	PMIC_MODE0	PMIC_MODE0	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
R7	PMIC_MODE1	PMIC_MODE1	—	—	—	—	—	—	—	—
U3	RESETN	RESETN	—	—	—	—	—	—	—	—
C18	USB0_DM	USB0_DM	—	—	—	—	—	—	—	—
B18	USB0_DP	USB0_DP	—	—	—	—	—	—	—	—
C16	USB0_VBUS_DETECT	USB0_VBUS_DETECT	—	—	—	—	—	—	—	—
A15	VDD1V8_EUSB	VDDIV8_EUSB	—	—	—	—	—	—	—	—
U10, V10	VDD1	VDD1	—	—	—	—	—	—	—	—
C4	VDD1V1_MIPI_CAP	VDD1V1_MIPI_CAP	—	—	—	—	—	—	—	—
B16	VDD1V2_EUSB	VDD1V2_EUSB	—	—	—	—	—	—	—	—
A13, B13	VDD1V8	VDD1V8	—	—	—	—	—	—	—	—
U4, V4	VDD1V8_AO	VDD1V8_AO	—	—	—	—	—	—	—	—
V7	VDD1V8_DCDC	VDD1V8_DCDC	—	—	—	—	—	—	—	—
C2	VDD1V8_MIPI	VDD1V8_MIPI	—	—	—	—	—	—	—	—
L18	VDD2_0	VDD2_0	—	—	—	—	—	—	—	—
U6, V6	VDD2_1	VDD2_1	—	—	—	—	—	—	—	—
K1, K2	VDD2_2	VDD2_2	—	—	—	—	—	—	—	—
C1	VDD2_3	VDD2_3	—	—	—	—	—	—	—	—
A8	VDD2_4	VDD2_4	—	—	—	—	—	—	—	—
D18	VDD3V3_USB	VDD3V3_USB	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
V16	VDDA_1V8	VDDA_1V8	—	—	—	—	—	—	—	—
N17, N18	VDDIO_0_0	VDDIO_0_0	—	—	—	—	—	—	—	—
U14, V14	VDDIO_0_1	VDDIO_0_1	—	—	—	—	—	—	—	—
M1, T1	VDDIO_0_2	VDDIO_0_2	—	—	—	—	—	—	—	—
D1	VDDIO_0_3	VDDIO_0_3	—	—	—	—	—	—	—	—
A7	VDDIO_0_4	VDDIO_0_4	—	—	—	—	—	—	—	—
F1, F2	VDDIO_2	VDDIO_2	—	—	—	—	—	—	—	—
A9, A12, B9	VDDIO_4	VDDIO_4	—	—	—	—	—	—	—	—
J17, J18	VDDIO_5	VDDIO_5	—	—	—	—	—	—	—	—
E17, E18	VDDIO_6	VDDIO_6	—	—	—	—	—	—	—	—
U1	VDDIO_AO	VDDIO_AO	—	—	—	—	—	—	—	—
U5	VDDN_0	VDDN_0	—	—	—	—	—	—	—	—
C17, D13	VDDN_1	VDDN_1	—	—	—	—	—	—	—	—
T16	VREF_LDO	VREF_LDO	—	—	—	—	—	—	—	—
U16	VREFH_ANA18	VREFH_ANA18	—	—	—	—	—	—	—	—
U17	VREFL_ANA	VREFL_ANA	—	—	—	—	—	—	—	—
A1, A3, A5, A11, A18, B5, B17,	VSS	VSS	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
D5, D7, D11, E7, E11, E15, F4, G14, G15, G18, H1, H4, H5, H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, L14, L15, M4, M5, N15, P1, P2, P4, P8, P12, R6, R8, R12, R14, R18, U2, V1, V5, V12										

Table continues on the next page...

Table 83. FOWLP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
V9	VSS_DCDC	VSS_DCDC	—	—	—	—	—	—	—	—
B15	VSS_EUSB	VSS_EUSB	—	—	—	—	—	—	—	—
V17, V18	VSSA_0	VSSA_0	—	—	—	—	—	—	—	—
C14	VSSA_1	VSSA_1	—	—	—	—	—	—	—	—
V2	XTALIN32KHZ	XTALIN32KHZ	—	—	—	—	—	—	—	—
A14	XTALINSYS	XTALINSYS	—	—	—	—	—	—	—	—
V3	XTALOUT32KHZ	XTALOUT32KHZ	—	—	—	—	—	—	—	—
B14	XTALOUTSYS	XTALOUTSYS	—	—	—	—	—	—	—	—

4.1.2 FOWLP package ball map

See attached the excel file "i.MXRT700 Ball map" for details.

4.2 WLCSP package information

4.2.1 WLCSP package pinout

Table 84 shows the list of functional contact assignments of WLCSP package.

Table 84. WLCSP package pin assignments

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
G14	PIO0_0	PIO0_0	PIO0_0	LP_FLEXCOMM8_P2	SCT0_GPIN0	SCT0_OUT0	CTIMER_C_INP9	SAI0_RX_BCLK	SAI1_TX_BCLK	—
G12	PIO0_1	PIO0_1	PIO0_1	LP_FLEXCOMM8_P3	SCT0_GPIN1	SCT0_OUT1	CTIMER0_MAT0	SAI0_RX_SYNC	SAI1_RX_DATA	—
G13	PIO0_2	PIO0_2	PIO0_2	LP_FLEXCOMM8_P4	SCT0_GPIN2	SCT0_OUT2	CTIMER0_MAT1	SAI0_RX_DATA	—	LP_FLEXCOMM9_P0
H14	PIO0_3	PIO0_3	PIO0_3	LP_FLEXCOMM4_P0	SCT0_GPIN3	SCT0_OUT3	CTIMER0_MAT2	SAI0_TX_BCLK	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
H15	PIO0_4	PIO0_4	PIO0_4	LP_FLEXCOMM4_P1	SCT0_GPIN4	SCT0_OUT4	CTIMER0_MAT3	SAI0_TX_DATA	—	—
H16	PIO0_5	PIO0_5	PIO0_5	LP_FLEXCOMM4_P4	SCT0_GPIN5	SCT0_OUT5	CTIMER2_MAT0	SAI0_TX_SYNC	MCLK	LP_FLEXCOMM9_P1
K10	PIO0_6	PIO0_6	PIO0_6	LP_FLEXCOMM4_P2	SCT0_GPIN6	SCT0_OUT6	CTIMER_C_INP10	LP_FLEXCOMM8_P0	—	—
K9	PIO0_7	PIO0_7	PIO0_7	LP_FLEXCOMM4_P3	SCT0_GPIN7	SCT0_OUT7	CTIMER_C_INP11	LP_FLEXCOMM8_P1	—	—
F14	PIO0_10	PIO0_10	PIO0_10	LP_FLEXCOMM5_P0	SCT0_GPIN4	SCT0_OUT4	CTIMER1_MAT0	CTIMER_C_INP0	SAI2_RX_DATA	—
F15	PIO0_11	PIO0_11	PIO0_11	LP_FLEXCOMM5_P1	SCT0_GPIN5	SCT0_OUT5	CTIMER1_MAT1	SAI2_TX_BCLK	—	—
G15	PIO0_12	PIO0_12	PIO0_12	LP_FLEXCOMM5_P2	SCT0_GPIN6	SCT0_OUT6	CTIMER1_MAT2	SAI2_TX_DATA	—	—
F16	PIO0_13	PIO0_13	PIO0_13	LP_FLEXCOMM5_P3	SCT0_GPIN7	SCT0_OUT7	CTIMER1_MAT3	SAI2_TX_SYNC	—	—
G16	PIO0_14	PIO0_14	PIO0_14	LP_FLEXCOMM5_P4	SCT0_GPIN0	SCT0_OUT8	CTIMER_C_INP2	SAI2_RX_DATA	CLKOUT_VDD2	—
C14	PIO0_19	PIO0_19	PIO0_19	LP_FLEXCOMM6_P2	SCT0_GPIN2	SCT0_OUT2	CTIMER2_MAT2	SAI1_RX_SYNC	—	—
F12	PIO0_20	PIO0_20	PIO0_20	LP_FLEXCOMM6_P3	SCT0_GPIN3	SCT0_OUT3	CTIMER2_MAT3	SAI1_TX_BCLK	—	—
E13	PIO0_21	PIO0_21	PIO0_21	LP_FLEXCOMM6_P0	SCT0_GPIN6	SCT0_OUT6	CTIMER_C_INP4	SAI1_TX_DATA	MCLK	—
D13	PIO0_22	PIO0_22	PIO0_22	LP_FLEXCOMM6_P1	SCT0_GPIN4	SCT0_OUT4	CTIMER_C_INP5	SAI1_TX_SYNC	CLKOUT_VDD2	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
H11	PIO0_31	PIO0_31	PIO0_31	LP_FLEXCOMM0_P0	UTICK0_CAP2	SCT0_OUT8	CTIMER4_MAT0	—	—	—
G11	PIO1_0	PIO1_0	PIO1_0	LP_FLEXCOMM0_P1	—	SCT0_OUT9	CTIMER4_MAT1	—	—	—
G10	PIO1_6	PIO1_6	PIO1_6	LP_FLEXCOMM1_P4	SCT0_GPIN4	SCT0_OUT0	CTIMER_C_INP12	I3C1_PUR	32KHZ_CLKOUT	—
D14	PIO1_7	PIO1_7	PIO1_7	LP_FLEXCOMM1_P0	SCT0_GPIN5	SCT0_OUT1	CTIMER_C_INP13	I3C1_SDA	—	—
E14	PIO1_8	PIO1_8	PIO1_8	LP_FLEXCOMM1_P1	SCT0_GPIN6	SCT0_OUT2	CTIMER_C_INP14	I3C1_SCL	—	—
D11	PIO1_9	PIO1_9	PIO1_9	LP_FLEXCOMM1_P2	SCT0_GPIN7	SCT0_OUT3	CTIMER_C_INP15	CLKIN	CLKOUT_VDD1	—
C16	PIO1_10	PIO1_10	PIO1_10	LP_FLEXCOMM1_P3	UTICK0_CAP3	—	CTIMER2_MAT1	TRACECLK	CLKOUT_VDD1	—
C15	PIO1_11	PIO1_11	PIO1_11	LP_FLEXCOMM2_P0	—	—	CTIMER2_MAT2	TRACEDATA0	—	—
C13	PIO1_12	PIO1_12	PIO1_12	LP_FLEXCOMM2_P1	SCT0_GPIN3	SCT0_OUT9	CTIMER1_MAT1	TRACEDATA1	—	—
D16	PIO1_13	PIO1_13	PIO1_13	LP_FLEXCOMM2_P4	UTICK0_CAP1	—	CTIMER2_MAT3	TRACEDATA2	32KHZ_CLKOUT	—
D15	PIO1_14	PIO1_14	PIO1_14	LP_FLEXCOMM2_P2	—	—	CTIMER3_MAT0	TRACEDATA3	—	—
H10	PIO1_15	PIO1_15	PIO1_15	LP_FLEXCOMM2_P3	—	—	CTIMER3_MAT1	CLKIN	—	—
H9	PIO1_16	PIO1_16	PIO1_16	LP_FLEXCOMM3_P2	—	—	CTIMER3_MAT2	I3C0_PUR	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
E11	PIO1_17	PIO1_17	PIO1_17	LP_FLEXCOMM3_P1	USB0_OVERCURRENTN	—	CTIMER3_MAT3	I3C0_SCL	—	—
E12	PIO1_18	PIO1_18	PIO1_18	LP_FLEXCOMM3_P0	USB0_PORTPWRN	—	CTIMER4_MAT0	I3C0_SDA	—	—
H13	PIO2_0	PIO2_0	PIO2_0	—	USB0_OVERCURRENTN	—	EZH_PIO0	FLEXIO_D0	—	LCD_DBI_CSX_AB
J13	PIO2_1	PIO2_1	PIO2_1	—	USB0_PORTPWRN	—	EZH_PIO1	FLEXIO_D1	—	LCD_DBI-DCX-AB
J14	PIO2_2	PIO2_2	PIO2_2	LPSPI16_SOUT	—	—	EZH_PIO2	FLEXIO_D2	LCD_ENABLE	LCD_DBI-DATA_OEN
K14	PIO2_3	PIO2_3	PIO2_3	LPSPI16_SCK	—	—	EZH_PIO3	FLEXIO_D3	LCD_DOTCLK	LCD_DBI-RWDX
K16	PIO2_4	PIO2_4	PIO2_4	LPSPI16_SIN	—	—	EZH_PIO4	FLEXIO_D4	LCD_HSYNC	LCD_DBI-WRX
H12	PIO2_5	PIO2_5	PIO2_5	LPSPI16_PCS0	—	—	EZH_PIO5	FLEXIO_D5	LCD_VSYNC	LCD_DBI-E
J12	PIO2_6	PIO2_6	PIO2_6	LPSPI16_PCS3	—	—	EZH_PIO6	FLEXIO_D6	LCD_D0	LCD_DBI-D0
J11	PIO2_7	PIO2_7	PIO2_7	LPSPI16_PCS2	—	—	EZH_PIO7	FLEXIO_D7	LCD_D1	LCD_DBI-D1
L11	PIO2_8	PIO2_8	PIO2_8	LPSPI16_PCS1	—	—	EZH_PIO8	FLEXIO_D8	LCD_D2	LCD_DBI-D2
K15	PIO2_9	PIO2_9	PIO2_9	—	—	—	EZH_PIO9	FLEXIO_D9	LCD_D3	LCD_DBI-D3
L15	PIO2_10	PIO2_10	PIO2_10	—	—	—	EZH_PIO10	FLEXIO_D10	LCD_D4	LCD_DBI-D4
L14	PIO2_11	PIO2_11	PIO2_11	—	—	—	EZH_PIO11	FLEXIO_D11	LCD_D5	LCD_DBI-D5
M15	PIO2_12	PIO2_12	PIO2_12	—	—	—	EZH_PIO12	FLEXIO_D12	LCD_D6	LCD_DBI-D6
M16	PIO2_13	PIO2_13	PIO2_13	—	—	—	EZH_PIO13	FLEXIO_D13	LCD_D7	LCD_DBI-D7

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
M14	PIO2_14	PIO2_14	PIO2_14	—	—	—	EZH_PIO 14	FLEXIO_ D14	LOW_FR EQ_CLK OUT	—
L9	PIO2_15	PIO2_15	PIO2_15	—	—	—	EZH_PIO 15	FLEXIO_ D15	LOW_FR EQ_CLK OUT_N	—
L13	PIO3_0	PIO3_0	PIO3_0	LPSPI14_ SOUT	—	—	EZH_PIO 16	—	—	—
L12	PIO3_1	PIO3_1	PIO3_1	LPSPI14_ SCK	—	—	EZH_PIO 17	—	—	—
N14	PIO3_2	PIO3_2	PIO3_2	LPSPI14_ SIN	—	—	EZH_PIO 18	—	—	—
P14	PIO3_3	PIO3_3	PIO3_3	LPSPI14_ PCS0	—	—	EZH_PIO 19	—	—	—
N9	PIO4_0	PIO4_0	PIO4_0	XSPI2_S S0_N	LP_FLEX COMM8_ P0	—	—	—	—	—
P7	PIO4_1	PIO4_1	PIO4_1	XSPI2_D ATA0	LP_FLEX COMM8_ P1	—	—	—	LCD_D20	—
R6	PIO4_2	PIO4_2	PIO4_2	XSPI2_D ATA1	LP_FLEX COMM8_ P2	—	—	—	LCD_D21	—
P8	PIO4_3	PIO4_3	PIO4_3	XSPI2_D ATA2	LP_FLEX COMM8_ P3	—	—	—	LCD_D22	—
P9	PIO4_4	PIO4_4	PIO4_4	XSPI2_D ATA3	LP_FLEX COMM8_ P4	—	—	—	LCD_D23	—
N8	PIO4_5	PIO4_5	PIO4_5	XSPI2_D QS0	LP_FLEX COMM8_ P5	—	—	—	—	—
R9	PIO4_6	PIO4_6	PIO4_6	XSPI2_D ATA4	LP_FLEX COMM8_ P6	—	—	—	LCD_D16	—
P5	PIO4_7	PIO4_7	PIO4_7	XSPI2_D ATA5	LP_FLEX COMM9_ P0	—	—	—	LCD_D17	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
R5	PIO4_8	PIO4_8	PIO4_8	XSPI2_DATA6	LP_FLEXCOMM9_P1	—	—	—	LCD_D18	—
P6	PIO4_9	PIO4_9	PIO4_9	XSPI2_DATA7	LP_FLEXCOMM9_P2	—	—	—	LCD_D19	—
R7	PIO4_10	PIO4_10	PIO4_10	XSPI2_SCLK0	LP_FLEXCOMM9_P3	—	—	—	—	—
T6	PIO4_11	PIO4_11	PIO4_11	XSPI2_SCLK0_N	LP_FLEXCOMM9_P4	XSPI2_SS1_N	—	—	—	—
M6	PIO4_12	PIO4_12	PIO4_12	XSPI2_DATA8	LP_FLEXCOMM9_P5	—	—	—	LCD_D8	LCD_DBI-D8
M9	PIO4_13	PIO4_13	PIO4_13	XSPI2_DATA9	LP_FLEXCOMM9_P6	—	—	—	LCD_D9	LCD_DBI-D9
M5	PIO4_14	PIO4_14	PIO4_14	XSPI2_DATA10	LP_FLEXCOMM10_P0	—	—	—	LCD_D10	LCD_DBI-D10
L8	PIO4_15	PIO4_15	PIO4_15	XSPI2_DATA11	LP_FLEXCOMM10_P1	—	—	—	LCD_D11	LCD_DBI-D11
L6	PIO4_16	PIO4_16	PIO4_16	XSPI2_DQS1	LP_FLEXCOMM10_P2	—	—	—	—	—
N6	PIO4_17	PIO4_17	PIO4_17	XSPI2_DATA12	LP_FLEXCOMM10_P3	—	—	—	LCD_D12	LCD_DBI-D12
M8	PIO4_18	PIO4_18	PIO4_18	XSPI2_DATA13	LP_FLEXCOMM10_P4	—	—	—	LCD_D13	LCD_DBI-D13
N4	PIO4_19	PIO4_19	PIO4_19	XSPI2_DATA14	LP_FLEXCOMM10_P5	—	—	—	LCD_D14	LCD_DBI-D14
L7	PIO4_20	PIO4_20	PIO4_20	XSPI2_DATA15	LP_FLEXCOMM10_P6	—	—	—	LCD_D15	LCD_DBI-D15

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
M4	PIO5_0	PIO5_0	PIO5_0	XSPI1_SS0_N	LP_FLEXCOMM13_P4	—	—	—	—	—
L3	PIO5_1	PIO5_1	PIO5_1	XSPI1_DATA0	LP_FLEXCOMM13_P5	—	—	—	—	—
K2	PIO5_2	PIO5_2	PIO5_2	XSPI1_DATA1	LP_FLEXCOMM13_P6	—	—	—	—	—
N3	PIO5_3	PIO5_3	PIO5_3	XSPI1_DATA2	LP_FLEXCOMM13_P0	—	—	—	—	—
N2	PIO5_4	PIO5_4	PIO5_4	XSPI1_DATA3	LP_FLEXCOMM13_P1	—	—	—	—	—
M3	PIO5_5	PIO5_5	PIO5_5	XSPI1_DQS0	LP_FLEXCOMM13_P2	—	—	—	—	—
P2	PIO5_6	PIO5_6	PIO5_6	XSPI1_DATA4	LP_FLEXCOMM12_P3	—	—	—	—	—
J1	PIO5_7	PIO5_7	PIO5_7	XSPI1_DATA5	LP_FLEXCOMM12_P0	—	—	—	—	—
J2	PIO5_8	PIO5_8	PIO5_8	XSPI1_DATA6	LP_FLEXCOMM12_P1	—	—	—	—	—
k3	PIO5_9	PIO5_9	PIO5_9	XSPI1_DATA7	LP_FLEXCOMM12_P2	—	—	—	—	—
L2	PIO5_10	PIO5_10	PIO5_10	XSPI1_SCLK0	LP_FLEXCOMM13_P3	—	—	—	—	—
L1	PIO5_11	PIO5_11	PIO5_11	XSPI1_SCLK0_N	LP_FLEXCOMM12_P4	XSPI1_SS1_N	—	—	—	—
J4	PIO5_12	PIO5_12	PIO5_12	XSPI1_DATA8	LP_FLEXCOMM12_P5	—	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
J3	PIO5_13	PIO5_13	PIO5_13	XSPI1_DATA9	LP_FLEXCOMM12_P6	—	—	—	—	—
H4	PIO5_14	PIO5_14	PIO5_14	XSPI1_DATA10	LP_FLEXCOMM11_P0	—	—	—	—	—
K5	PIO5_15	PIO5_15	PIO5_15	XSPI1_DATA11	LP_FLEXCOMM11_P1	—	—	—	—	—
J6	PIO5_16	PIO5_16	PIO5_16	XSPI1_DQS1	LP_FLEXCOMM11_P2	—	—	—	—	—
J5	PIO5_17	PIO5_17	PIO5_17	XSPI1_DATA12	LP_FLEXCOMM11_P3	—	—	—	—	—
L5	PIO5_18	PIO5_18	PIO5_18	XSPI1_DATA13	LP_FLEXCOMM11_P4	—	—	—	—	—
H5	PIO5_19	PIO5_19	PIO5_19	XSPI1_DATA14	LP_FLEXCOMM11_P5	—	—	—	—	—
K4	PIO5_20	PIO5_20	PIO5_20	XSPI1_DATA15	LP_FLEXCOMM11_P6	—	—	—	—	—
T11	PIO7_0	PIO7_0	PIO7_0	SDHC0_CLK	LP_FLEXCOMM3_P4	LP_FLEXCOMM7_P6	—	—	—	—
P10	PIO7_1	PIO7_1	PIO7_1	SDHC0_CMD	LP_FLEXCOMM3_P5	LP_FLEXCOMM7_P5	—	—	—	—
M10	PIO7_2	PIO7_2	PIO7_2	SDHC0_DATA4	LP_FLEXCOMM12_P0	—	—	—	—	—
L10	PIO7_3	PIO7_3	PIO7_3	SDHC0_DATA5	LP_FLEXCOMM12_P1	—	—	—	—	—
N12	PIO7_4	PIO7_4	PIO7_4	SDHC0_DATA6	LP_FLEXCOMM12_P2	—	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
N13	PIO7_5	PIO7_5	PIO7_5	SDHC0_DATA7	LP_FLEXCOMM12_P3	—	—	—	—	—
R11	PIO7_6	PIO7_6	PIO7_6	SDHC0_DATA0	LP_FLEXCOMM12_P4	—	—	—	—	—
R10	PIO7_7	PIO7_7	PIO7_7	SDHC0_DATA1	LP_FLEXCOMM12_P5	—	—	—	—	—
P12	PIO7_8	PIO7_8	PIO7_8	SDHC0_DATA2	LP_FLEXCOMM12_P6	LP_FLEXCOMM7_P3	—	—	—	—
P11	PIO7_9	PIO7_9	PIO7_9	SDHC0_DATA3	LP_FLEXCOMM3_P6	LP_FLEXCOMM7_P4	—	—	—	—
M11	PIO7_10	PIO7_10	PIO7_10	SDHC0_WR_PRT	LP_FLEXCOMM1_P0	—	—	SDHC0_DS	—	—
M12	PIO7_11	PIO7_11	PIO7_11	SDHC0_CARD_DET_N	LP_FLEXCOMM1_P1	—	—	—	—	—
N10	PIO7_12	PIO7_12	PIO7_12	SDHC0_RESET_N	LP_FLEXCOMM1_P2	—	—	—	—	—
J7	PIO7_13	PIO7_13	PIO7_13	SDHC1_DATA4	LP_FLEXCOMM1_P3	—	—	—	—	—
J8	PIO7_14	PIO7_14	PIO7_14	SDHC1_DATA5	LP_FLEXCOMM7_P0	—	—	—	—	—
K7	PIO7_15	PIO7_15	PIO7_15	SDHC1_DATA6	LP_FLEXCOMM7_P1	—	—	—	—	—
K8	PIO7_16	PIO7_16	PIO7_16	SDHC1_DATA7	LP_FLEXCOMM7_P2	—	—	—	—	—
G1	PIO7_17	PIO7_17	PIO7_17	SDHC1_CLK	LP_FLEXCOMM2_P0	—	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
F3	PIO7_18	PIO7_18	PIO7_18	SDHC1_CMD	LP_FLEXCOMM2_P1	—	—	—	—	—
G2	PIO7_19	PIO7_19	PIO7_19	SDHC1_DATA0	LP_FLEXCOMM1_P4	LP_FLEXCOMM7_P3	—	—	—	—
F2	PIO7_20	PIO7_20	PIO7_20	SDHC1_DATA1	LP_FLEXCOMM1_P5	LP_FLEXCOMM2_P4	—	—	—	—
H3	PIO7_21	PIO7_21	PIO7_21	SDHC1_DATA2	LP_FLEXCOMM1_P6	LP_FLEXCOMM2_P5	—	—	—	—
G3	PIO7_22	PIO7_22	PIO7_22	SDHC1_DATA3	LP_FLEXCOMM2_P2	—	—	—	—	—
K6	PIO7_23	PIO7_23	PIO7_23	SDHC1_WR_PRT	LP_FLEXCOMM2_P3	—	—	—	—	—
G7	PIO7_25	PIO7_25	PIO7_25	SDHC1_RESET_N	LP_FLEXCOMM13_P5	LP_FLEXCOMM2_P6	—	—	—	—
A6	PIO8_0	JTAG_TCK/SWCLK	PIO8_0	LP_FLEXCOMM17_P5	CTIMER_S_INP0	—	—	JTAG_TCK/SWCLK	—	—
B6	PIO8_1	JTAG_TMS/SWDIO	PIO8_1	LP_FLEXCOMM17_P6	CTIMER5_MAT0	—	—	JTAG_TMS/SWDIO	—	—
B7	PIO8_2	JTAG_TDI	PIO8_2	LP_FLEXCOMM17_P2	CTIMER5_MAT1	—	—	JTAG_TDI	—	—
B8	PIO8_3	JTAG_TD0/SWO	PIO8_3	LP_FLEXCOMM17_P3	CTIMER_S_INP1	UTICK1_CAP0	—	JTAG_TD0/SWO	—	—
C5	PIO8_4	JTAG_TRSTN	PIO8_4	LP_FLEXCOMM17_P4	CTIMER5_MAT2	MCLK	—	JTAG_TRSTN	—	—
C6	PIO8_5	PIO8_5	PIO8_5	LP_FLEXCOMM17_P0	CTIMER5_MAT3	CTIMER_S_INP0	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
C4	PIO8_6	PIO8_6	PIO8_6	LP_FLEXCOMM17_P1	CTIMER6_MAT0	—	CMP0_OUT	—	—	—
F4	PIO8_7	PIO8_7	PIO8_7	LP_FLEXCOMM18_P0	CTIMER6_MAT1	—	—	—	—	—
C7	PIO8_8	PIO8_8	PIO8_8	LP_FLEXCOMM18_P1	CTIMER_S_INP2	—	—	—	—	—
H6	PIO8_9	PIO8_9	PIO8_9	LP_FLEXCOMM18_P2	CTIMER_S_MAT2	—	—	—	—	—
F6	PIO8_10	PIO8_10	PIO8_10	LP_FLEXCOMM18_P3	CTIMER_S_INP3	—	—	—	—	—
E6	PIO8_11	PIO8_11	PIO8_11	LP_FLEXCOMM18_P4	CTIMER6_MAT3	UTICK1_CAP1	LP_FLEXCOMM17_P4	—	—	—
D7	PIO8_12	PIO8_12	PIO8_12	LP_FLEXCOMM18_P5	CTIMER7_MAT0	CTIMER_S_INP1	LP_FLEXCOMM17_P2	—	—	—
E7	PIO8_13	PIO8_13	PIO8_13	LP_FLEXCOMM18_P6	CTIMER7_MAT1	CTIMER_S_INP3	LP_FLEXCOMM17_P3	—	—	—
C8	PIO8_14	PIO8_14	PIO8_14	LP_FLEXCOMM19_P0	CTIMER7_MAT2	SAI3_TX_SYNC	I3C2_SDA	—	—	—
C9	PIO8_15	PIO8_15	PIO8_15	LP_FLEXCOMM19_P1	CTIMER7_MAT3	SAI3_TX_BCLK	I3C2_SCL	—	—	—
C10	PIO8_16	PIO8_16	PIO8_16	LP_FLEXCOMM19_P2	CTIMER_S_INP4	SAI3_TX_DATA	I3C2_PUR	—	—	—
A8	PIO8_17	PIO8_17	PIO8_17	LP_FLEXCOMM19_P3	CTIMER_S_INP5	SAI3_RX_SYNC	—	—	—	—
F8	PIO8_18	PIO8_18	PIO8_18	LP_FLEXCOMM19_P4	CTIMER5_MAT0	CTIMER_S_INP4	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
D8	PIO8_19	PIO8_19	PIO8_19	LP_FLEXCOMM19_P5	CTIMER5_MAT1	CTIMER_S_INP6	CMP0_OUT	—	—	—
E8	PIO8_20	PIO8_20	PIO8_20	LP_FLEXCOMM19_P6	CTIMER_S_INP7	UTICK1_CAP2	I3C3_PUR	—	—	—
E9	PIO8_21	PIO8_21	PIO8_21	LP_FLEXCOMM20_P3	CTIMER5_MAT0	LP_FLEXCOMM3_P0	I3C3_SDA	—	—	—
D9	PIO8_22	PIO8_22	PIO8_22	LP_FLEXCOMM20_P4	CTIMER5_MAT1	LP_FLEXCOMM3_P1	I3C3_SCL	—	—	—
E3	PIO8_23	PIO8_23	PIO8_23	SAI3_RX_BCLK	CTIMER5_MAT2	LP_FLEXCOMM19_P0	—	—	—	—
F5	PIO8_24	PIO8_24	PIO8_24	SAI3_RX_DATA	CTIMER5_MAT3	LP_FLEXCOMM19_P1	—	—	—	—
G8	PIO8_25	PIO8_25	PIO8_25	SAI3_RX_SYNC	CTIMER6_MAT0	LP_FLEXCOMM19_P2	—	—	—	—
G9	PIO8_26	PIO8_26	PIO8_26	SAI3_TX_BCLK	CTIMER6_MAT1	LP_FLEXCOMM19_P3	—	—	—	—
E2	PIO8_30	PIO8_30	PIO8_30	LP_FLEXCOMM20_P0	CTIMER_S_INP9	UTICK1_CAP3	—	—	—	—
E1	PIO8_31	PIO8_31	PIO8_31	LP_FLEXCOMM20_P1	CTIMER7_MAT0	—	—	—	—	—
C1	PIO10_0	PIO10_0	PIO10_0	—	—	—	—	PDM_CLK	—	—
B1	PIO10_1	PIO10_1	PIO10_1	—	—	—	—	PDM_DATA01	—	—
C2	PIO10_2	PIO10_2	PIO10_2	—	—	—	—	PDM_DATA23	—	—
D3	PIO10_3	PIO10_3	PIO10_3	—	—	—	—	PDM_DATA45	—	—
D4	PIO10_4	PIO10_4	PIO10_4	—	—	—	—	PDM_DATA67	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
D5	PIO10_5	PIO10_5	PIO10_5	—	—	CMP0_OUT	—	—	—	—
A4	PIO10_6	PIO10_6	PIO10_6	—	—	—	—	—	—	—
B4	PIO10_7	PIO10_7	PIO10_7	—	—	—	—	—	—	—
B2	PIO10_8	PIO10_8	PIO10_8	—	—	—	—	PDM_CLK	—	—
B3	PIO10_9	PIO10_9	PIO10_9	—	—	—	—	PDM_DATA01	—	—
E5	PIO10_12	PIO10_12	PIO10_12	—	—	—	—	PDM_DATA67	—	—
F7	PIO10_13	PIO10_13	PIO10_13	—	—	—	—	PDM_CLK	—	—
A11	LX_DCDC	LX_DCDC	—	—	—	—	—	—	—	—
R15	MIPI_DSI_CLKN	MIPI_DSI_CLKN	—	—	—	—	—	—	—	—
R14	MIPI_DSI_CLKP	MIPI_DSI_CLKP	—	—	—	—	—	—	—	—
R13	MIPI_DSI_D0N	MIPI_DSI_D0N	—	—	—	—	—	—	—	—
T13	MIPI_DSI_D0P	MIPI_DSI_D0P	—	—	—	—	—	—	—	—
R16	MIPI_DSI_D1N	MIPI_DSI_D1N	—	—	—	—	—	—	—	—
T15	MIPI_DSI_D1P	MIPI_DSI_D1P	—	—	—	—	—	—	—	—
B10	PMIC_I2C_SCL	PMIC_I2C_SCL	—	—	—	—	—	—	—	—
B11	PMIC_I2C_SDA	PMIC_I2C_SDA	—	—	—	—	—	—	—	—
F9	PMIC_IRQN	PMIC_IRQN	—	—	—	—	—	—	—	—
F10	PMIC_MODE0	PMIC_MODE0	—	—	—	—	—	—	—	—
F11	PMIC_MODE1	PMIC_MODE1	—	—	—	—	—	—	—	—
B14	RESETN	RESETN	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
R1	USB0_DM	USB0_DM	—	—	—	—	—	—	—	—
T2	USB0_DP	USB0_DP	—	—	—	—	—	—	—	—
P3	USB0_VBUS_DETECT	USB0_VBUS_DETECT	—	—	—	—	—	—	—	—
A9, B9	VDD1	VDD1	—	—	—	—	—	—	—	—
P13	VDD1V1_MIPI_CAP	VDD1V1_MIPI_CAP	—	—	—	—	—	—	—	—
C11, R4, T4	VDD1V8	VDD1V8	—	—	—	—	—	—	—	—
B16	VDD1V8_AO	VDD1V8_AO	—	—	—	—	—	—	—	—
A12	VDD1V8_DCDC	VDD1V8_DCDC	—	—	—	—	—	—	—	—
P15	VDD1V8_MIPI	VDD1V8_MIPI	—	—	—	—	—	—	—	—
A13, B13	VDD2_0	VDD2_0	—	—	—	—	—	—	—	—
J15, J16	VDD2_1	VDD2_1	—	—	—	—	—	—	—	—
P16	VDD2_2	VDD2_2	—	—	—	—	—	—	—	—
T10	VDD2_3	VDD2_3	—	—	—	—	—	—	—	—
H1, H2	VDD2_4	VDD2_4	—	—	—	—	—	—	—	—
P1	VDD3V3_USB	VDD3V3_USB	—	—	—	—	—	—	—	—
A3	VDDA_1V8	VDDA_1V8	—	—	—	—	—	—	—	—
A5, B5	VDDIO_0_0	VDDIO_0_0	—	—	—	—	—	—	—	—
F1	VDDIO_0_1	VDDIO_0_1	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
R12, T12	VDDIO_0_2	VDDIO_0_2	—	—	—	—	—	—	—	—
E15, E16	VDDIO_0_3	VDDIO_0_3	—	—	—	—	—	—	—	—
N15, N16	VDDIO_2	VDDIO_2	—	—	—	—	—	—	—	—
R8, T5, T8	VDDIO_4	VDDIO_4	—	—	—	—	—	—	—	—
M1, M2	VDDIO_5	VDDIO_5	—	—	—	—	—	—	—	—
C12	VDDIO_AO	VDDIO_AO	—	—	—	—	—	—	—	—
B12	VDDN_0	VDDN_0	—	—	—	—	—	—	—	—
N1, N5	VDDN_1	VDDN_1	—	—	—	—	—	—	—	—
C3	VREF_LDO	VREF_LDO	—	—	—	—	—	—	—	—
A1, A7, A16, B15, D1, D2, D6, D10, D12, E4, E10, F13, G4, G5, G6, H7, H8, J9, J10, K1, K11, K12, K13, L4, L16,	VSS	VSS	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 84. WLCSP package pin assignments*...continued*

Pin number	Pin name	Default	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
M7, M13, N7, N11, R2, T1, T7, T9, T14, T16										
A10	VSS_DCDC	VSS_DCDC	—	—	—	—	—	—	—	—
A2	VSSA_0	VSSA_0	—	—	—	—	—	—	—	—
P4	VSSA_1	VSSA_1	—	—	—	—	—	—	—	—
A15	XTALIN32KHZ	XTALIN32KHZ	—	—	—	—	—	—	—	—
R3	XTALINSYS	XTALINSYS	—	—	—	—	—	—	—	—
A14	XTALOUT32KHZ	XTALOUT32KHZ	—	—	—	—	—	—	—	—
T3	XTALOUTSYS	XTALOUTSYS	—	—	—	—	—	—	—	—

4.2.2 WLCSP package ball map

See attached the excel file "i.MXRT700 Ball map" for details.

4.3 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
256-pin WLCSP	98ASA01940D
324-pin FOWLP	98ASA02039D

4.4 Termination of unused pins

The following table shows how to terminate pins on functions that are not used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

By default, unused pins with GPIO functions are tri-stated with the input buffer disabled and can remain floating.

All power pins in the domains listed below must be connected to the recommended voltage.

Table 85. Termination of unused pins

Function	Pin Name	Default state[1]	Recommended termination of unused pins
GPIO	All PIOn pins (FSGPIO)	Z	Can be left unconnected if configured by software as an output with pull-up disabled and driven LOW.
GPIO	All PIOn pins (FSGPIO1V21V8)	Most are Z, a few are PU	Can be left unconnected if configured by software as an output with pull-up disabled and driven LOW.
PMIC Control	PMIC_I2C_SCL and PMIC_I2C_SDA	Z	Leave unconnected
PMIC Control	PMIC_IRQN	I, Z	Tie to VDD1V8_AO
PMIC Control	PMIC_MODE1 and PMIC_MODE0	O	Leave unconnected
Control	RESETN	I	100k Ω pull-up resistor to VDDIO_AO
Oscillator	XTALIN32KHZ	I	Tie to ground
Oscillator	XTALOUT32KHZ	—	Leave unconnected
Oscillator	XTALINSYS	I	Tie to ground
Oscillator	XTALOUTSYS	—	Leave unconnected
eUSB	EUSB_DM / EUSB_DP	—	EUSB_DM and EUSB_DP can be left unconnected. If the eUSB interface is not used, these pins can be left unconnected except in deep power-down mode where they must be externally pulled low. When the eUSB PHY is disabled, the pins are floating.
eUSB	VDD1V2_EUSB[2]	—	Tie to ground
eUSB	VDD1V8_EUSB[2]	—	Tie to ground
USB0	USB0_DM and USB0_DP	—	Can be left unconnected. If the eUSB interface is not used, these pins can be left unconnected except in deep power-down mode where they must be externally pulled low. When the eUSB PHY is disabled, the pins are floating

Table continues on the next page...

Table 85. Termination of unused pins...*continued*

Function	Pin Name	Default state[1]	Recommended termination of unused pins
USB0	USB0_VBUS	—	Leave unconnected
USB0	VDD3V3_USB	—	Leave unconnected
MIPI_DSI	MIPI_DSI_CLKN and MIPI_DSI_CLKP	—	Leave unconnected
	MIPI_DSI_D0N and MIPI_DSI_D0P	—	10 KΩ resistor to ground
	MIPI_DSI_D1N and MIPI_DSI_D1P	—	10 KΩ resistor to ground
Analog	VREFH_ANA18	—	Tie to VDDA_1V8 analog supply
Analog	VREFL_ANA	—	Tie to VSS
SDADC	VREF_LDO	—	Leave unconnected
SARADC	VDDA_1V8	—	Tie to 1.8 V supply
Power	VDDIO_X	—	Leave unconnected
Power	VSSA	—	Tie to VSS

[1] Z = high impedance; I = Input; O = Output
[2] VDD1V2_EUSB and VDD1V8_EUSB are not available on WLCSP package.

4.5 Pin states in different power modes

Table 86. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down	Full DSR
All PIOn pins	As configured in IOPCTL[1]. Default is Z (input, pull-up, and pull-down disabled), except for a few pins where the pull-up and input are enabled.			Floating	Floating

[1] Default and programmed pin states are retained in sleep and deep-sleep.

5 Power supply for pins

The following table shows the GPIOs belonging to the specific VDDIO groups and VDD1V8_AO domain.

Table 87. Power supply for pins

Pin	GPIO pins
VDDIO_0 (1.8 V only)	PIO0_0 to PIO0_31 (High Speed) PIO1_0 to PIO1_19 (High Speed) PIO3_0 to PIO3_14 (High Speed) PIO7_0 to PIO7_25 (High Speed)

Table continues on the next page...

Table 87. Power supply for pins...*continued*

Pin	GPIO pins
	PIO8_0 to PIO8_31 (Fail Safe) PIO9_0 to PIO9_2 (Fail Safe) PIO10_0 to PIO10_17 (Fail Safe) PMIC_I2C_SDA and PMIC_I2C_SCL (Fail Safe)
VDDIO_2 (1.8 V or 3.3 V)	PIO2_0 to PIO2_15 (Fail Safe)
VDDIO_4 (1.2 V and 1.8 V)	PIO4_0 to PIO4_20 (High Speed)
VDDIO_5 (1.2 V and 1.8 V)	PIO5_0 to PIO5_20 (High Speed)
VDDIO_6 (1.2 V or 1.8 V)	PIO6_0 to PIO6_12 (Hihg Speed)
VDD1V8_AO	PMIC_MODE1 PMIC_MODE0 PMIC_IRQN

6 Revision History

Table 88 provides a revision history for this data sheet.

Table 88. Data Sheet document revision history

Rev. Number	Date	Substantive Change(s)
IMXRT700EC V 6.0	10/30/2025	• Removed the CPU0/CPU1 column and added footnotes in Table 2 • Updated the symbol of fotp_clk in Table 12 • Updated the Condition column of Table 13 and Table 14 • Added a footnote in Table 15 and Table 16 • Updated descriptions of CPU0 CM33 Sleep, Sense Deep Sleep, HiFi 4 DSP FFT, HiFi 1 DSP stalled • Updated descriptions of footnotes of Table 28 • Added Figure 17 • Updated the maximum value of Vout_byp in Table 37 and Table 38 • Updated descriptions of Serial Wire Debug (SWD) timing specifications • Updated f, tDS, and tDH in Table 53 • Updated the Condition column of Table 59 • Updated VDDA_1V8 and VDD1 of Table 62 • Updated descriptions of Flexible I/O controller (FLEXIO)

Table continues on the next page...

Table 88. Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Added SDADC and SARADC in Table 85
IMXRT700EC V 5.0	09/12/2025	• Updated descriptions of PMC and RAM Arbiter in Table 1 • Added a footnote in Table 2 • Updated Table 3 • Updated Feature 1, Feature 3, and Temperature range in Figure 1 • Updated descriptions of package marking in Package marking • Updated VDD1V8_EUSB and added power consumption values in Table 9 • Updated conditions of VDDIO_x and added USB0_VBUS_DETECT in Table 12 • Added OTP descriptions in VDD1, VDD2, and VDDN operating conditions when using an external supply for VDD1 and VDD2 • Updated condition and added 1.0 V for VDD1/VDD2 in Table 14 • Updated Fail Safe GPIO (FSGPIO) DC parameters and High Speed GPIO DC parameters • Removed Section Output impedance • Added FSGPIO AC parameters • Updated the settings of HiFi 4 / HiFi 1 DSP and added two footnotes in CPU0 CM33 CoreMark, Sense Deep Sleep • Updated the settings of HiFi 4 / HiFi 1 DSP and added two footnotes in CPU0 CM33 Sleep, Sense Deep Sleep • Added two footnotes in Table 20 • Added two footnotes in Table 21 • Updated the settings of DSP_CLK / COMPUTE_MAIN_CLK and added two footnotes in Table 22 • Updated the settings of HiFi 4 DSP, SENCE_DSP_CLK / SENSE_MAIN_CLK and added two footnotes in Table 23 • Updated the descriptions of Compute and Sense Dual Deep Sleep mode • Updated IVDD1 / IVDD2 and the descriptions of footnotes in Table 25 • Updated IVDD1 / IVDD2 and the descriptions of footnotes in Table 26 • Updated IVDDIO_6, IVDDA_1V8, IVDD3V3_USB, IVREFH_ANA18, and footnotes in Table 27 • Updated IVDDIO_6 and footnotes in Table 28 • Updated the descriptions of Condition in Table 30 • Updated POR_VDD_T_ACCURACY and LVD_VDD_T_ACCURACY in Table 31

Table continues on the next page...

Table 88. Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Added PMC LVD specifications • Updated output voltage, Cout, Inductance, Ioc_hp, Ioc_lp, and Condition in Table 35 • Updated the output range in Table 36 • Updated Figure 16 and removed Power-up sequence using PMIC • Added Recommended NXP PMIC • Updated the descriptions, the digital supply voltage, IDD, and JP in Table 39 • Updated VIH and Vpp in Table 40 • Updated the clock output range in Table 43 • Updated COMM2_CLKOUT in Table 44 • Updated SENSE_CLKOUT in Table 47 • Updated DCPPIXEL_FCLK and DPHY_BIT_CLK in Table 48 • Updated the descriptions of Condition in Table 51 • Added descriptions of Table 52 • Updated descriptions of Table 53 • Updated Table 54 • Updated descriptions of Table 55 • Updated descriptions of Table 56 • Updated descriptions of Table 57 • Updated descriptions of Table 58 • Updated descriptions of LCDIF characteristics • Updated RCONV and CADIN in Table 60 • Updated TAZ_REQ in Table 61 • Updated VDDA_1V8 in Table 62 • Updated descriptions of Table 69 • Updated I2C-bus • Updated description of I3C Push-Pull Timing Parameters for SDR Mode • Updated descriptions of SAI/I2S Controller mode timing • Updated the condition of Table 74 • Updated descriptions of LPSPI Controller mode timing (LP_FLEXCOMM0-13, 17-20) • Updated descriptions of LPSPI Peripheral mode timing (LP_FLEXCOMM0-13, 17-20)

Table continues on the next page...

Table 88. Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated descriptions and frequency condition in High-Speed SPI interface Controller Mode timing • Updated descriptions and condition in High-Speed SPI interface Peripheral Mode timing • Removed FOWLP and WLCSP package outline • Added Obtaining package dimensions • Updated eUSB in Table 85 • Updated descriptions of GPIO pins in Table 87
IMXRT700EC V 4.0	07/01/2025	• Updated Introduction • Updated descriptions about PMC in Table 1 • Added Ordering Information • Added FOWLP package in Package marking • Updated Table 9 • Updated Table 10 • Added FOWLP package in Table 11 • Updated Table 12 • Updated Table 13 • Updated Table 14 • Updated Table 15 • Updated High Speed GPIO DC parameters • Updated Power consumption operating behavior • Updated Table 29 • Updated Wake-up time • Updated Table 31 • Updated Table 35 • Updated Table 36 • Updated Table 37 • Updated Table 39 • Updated Crystal oscillator (XTAL OSC) • Updated Table 41 • Updated Internal low-power oscillator (LPOSC) • Updated Table 43 • Updated Table 51

Table continues on the next page...

Table 88. Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated JTAG timing specifications • Updated Dynamic characteristics: XSPI interface • Updated Ultra Secured Digital Host Controller (uSDHC) • Updated Table 60 and Table 61 • Updated 24-bit SDADC characteristics • Updated Table 67 • Updated Flexible I/O controller (FLEXIO) • Updated I3C Push-Pull Timing Parameters for SDR Mode • Updated SAI/I2S Controller mode timing • Updated LPSPI interface • Updated High-Speed SPI interface • Added FOWLP package information • Updated Table 85 • Updated Table 87
IMXRT700EC V 2.0	03/07/2025	• Updated the descriptions of CPU0, CLKCTL, FRO, XSPI, HiFi 4 DSP, HIFI 1 DSP, MICFIL in Table 1, added the temperature range in Table 1 • Removed Order information • Removed i.MX RT700 module list • Updated Table 9 • Updated Thermal characteristics • Updated Table 12 • Updated VDD1, VDD2, and VDDN operating conditions when using an external supply for VDD1 and VDD2 and VDD1, VDD2, and VDDN operating conditions when using on-chip LDO for VDD1 and VDD2 • Updated Fail Safe GPIO (FSGPIO) DC parameters, Table 16, and Output impedance • Updated Power consumption operating behavior • Updated CoreMark data • Updated Wake-up time • Added Clock root frequencies • Updated LDO VDD2 250 mA regulator specifications • Updated LDO VDD1 50 mA regulator specifications • Updated Power-up sequence

Table continues on the next page...

Table 88. Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated Table 39 • Updated Table 42 • Added Clock root frequencies • Updated Table 51 • Updated Table 59 • Updated Table 69 • Removed the second ETS parameter from 16-bit ADC electrical characteristics • Updated 24-bit SDADC characteristics • Removed Section Temperature Sensor and added Temperature Detector specifications • Updated SAI/I2S-bus interface • Updated LPSPI interface • Updated High-Speed SPI interface • Updated PDM Microphone interface (MICFIL) timing parameters • Updated WLCSP package ball map
IMXRT700EC V 1.0	03/2024	Initial version

Legal information

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Document status[1][2]	Product status[3]	Definition
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