IW416

Dual-band 1x1 Wi-Fi 4 and Bluetooth Combo SoC

Rev. 8.0 — 24 September 2025 **Product data sheet**

1 Product overview

The IW416 is a highly integrated Wi-Fi 4 and Bluetooth System-on-Chip (SoC) enabling a low-cost connectivity solution. Supporting a 1x1 SISO Wi-Fi operation in the 2.4 GHz and the 5 GHz band, the SoC provides a full-feature Wi-Fi subsystem with a peak PHY date rate of 150 Mbit/s. In addition to classic Bluetooth features, the IW416 enables Bluetooth capabilities including Low Energy (LE), LE long range, LE 2 Mbps, and Periodic Advertising Sync Transfer (PAST).

With integrated transmit (TX) PAs, receive (RX) LNAs and TX/RX switches for the Wi-Fi and Bluetooth radios, the IW416 simplifies design allowing quick integration of either dual or single-antenna operation. The dual-antenna configuration enables simultaneous Wi-Fi and Bluetooth operation. With the single-antenna configuration, simultaneous 5 GHz Wi-Fi and Bluetooth is supported. In the 2.4 GHz band, the single-antenna configuration allows arbitrated transmit and receive operation of Wi-Fi and Bluetooth.

Promoting synergistic operation, the IW416 implements advanced Wi-Fi and Bluetooth co-existence hardware in conjunction with algorithms to optimize collaborative performance. In addition, support for external radio co-existence is provided through an external interface.

Available in both HVQFN68 and WLCSP76 packages with two operating temperature ranges of 0 to 70°C and -40 to 85°C, the IW416 supports SDIO host interface for the Wi-Fi radio and UART host interface for the Bluetooth radio.

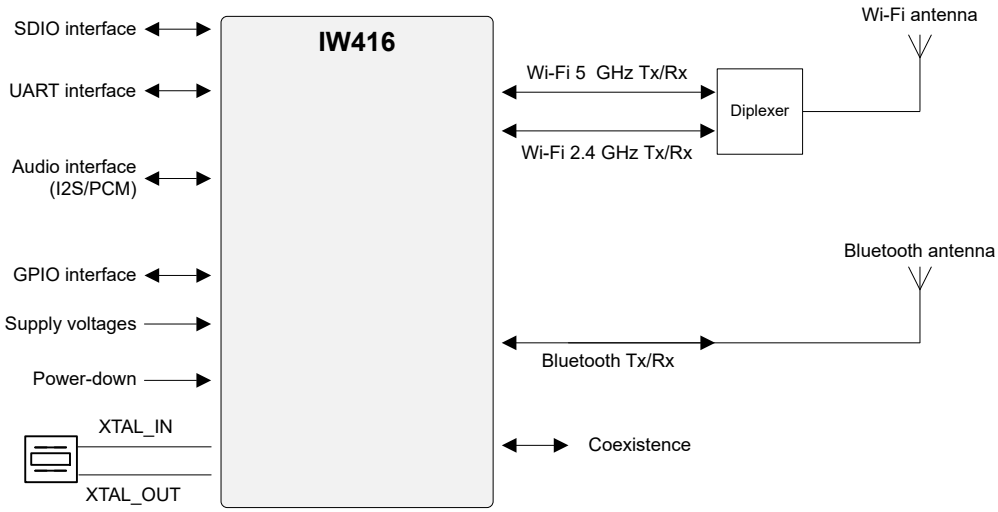

Figure 1. Application block diagram

Note: *More application details in IW416 Design Guide (AN13125)*

1.1 Applications

- Smart home: Voice assist device, smart printer, smart speaker, home automation gateway, and IP camera
- Industrial and building automation
- Asset management
- Retail/POS
- Healthcare and medical devices
- Smart city

1.2 Wi-Fi key features

- Support 802.11 a/b/g/n
- Dual band: 2.4 GHz and 5 GHz
- Single stream 802.11n with 20 MHz and 40 MHz channels
- Up to MCS7 data rates (150 Mbit/s)
- Dynamic Rapid Channel Switching (DRCS) for simultaneous operation in 2.4 GHz and 5 GHz bands
- Packet Traffic Arbiter (PTA) interface to coexist with an external radios. The external radio can be 802.15.4 or other radios.
- Security: WPA3, WPA2, WPA2-WPA mixed mode

1.3 Bluetooth key features

- Supports Bluetooth 5.1 (Class 1/Class 2) and Bluetooth Low Energy features
- Bluetooth 5.2 certified
- Long range - 4x coverage
- 2 Mbit/s data rate - 2x faster
- Improved advertisement capability - enables more IoT services
- I2S and PCM audio interfaces
- AES security[1]

1.4 Host interfaces

Wi-Fi and Bluetooth host interface options

Table 1. Host interface options

Wi-Fi	Bluetooth
SDIO 3.0	UART

1 Refer to IW416 errata sheet (ES_IW416)

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1.5 Operating characteristics

- Supply voltages: 1.05V, 1.8V, and 2.2V
- Operating temperature ranges:
  - Commercial: 0 to 70°C
  - Industrial: -40 to 85°C

1.6 General features

- Package options
  - HVQFN68 (68 pins, 0.4 mm pitch, 8 mm x 8 mm x 0.85 mm body)
  - WLCSP76 (76 terminals, 0.35 mm pitch, 3.95 mm x 3.565 mm x 0.495 mm body)
- Simultaneous Wi-Fi and Bluetooth operation supported with dual antenna configuration
  - Shared Wi-Fi and Bluetooth operation with single antenna is possible
- Power saving features
  - Efficient power management system
  - Sleep and standby modes
  - Deep-sleep mode
- Independent ARM-based Wi-Fi and Bluetooth CPUs
  - Wi-Fi CPU: 160 MHz clock speed
  - Bluetooth CPU: 128 MHz clock speed
- Memory:
  - Internal SRAM
  - Boot ROM
  - OTP memory to store the MAC address and calibration data
- Peripheral Interface
  - General-Purpose I/O (GPIO) interface

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1.7 Internal block diagram

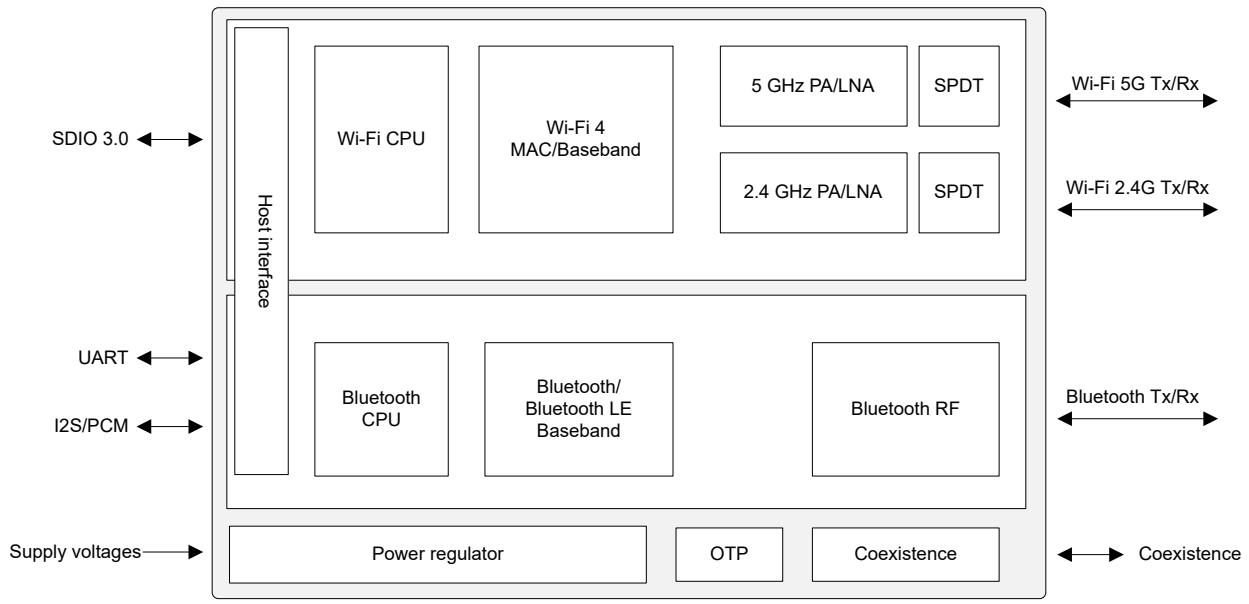

Figure 2. Internal block diagram

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2 Ordering information

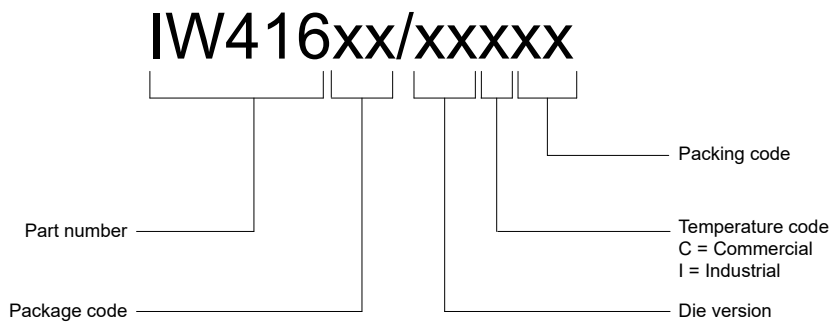

Figure 3. Part numbering scheme

Table 2. Part order codes

Part order code	Package type	Operating temperature range	Packing
IW416HN/A1CK	HVQFN68 - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Commercial	Tray
IW416HN/A1CMP	HVQFN68 - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Commercial	Tape and Reel
IW416HN/A1IK	HVQFN68 - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Industrial	Tray
IW416HN/A1IMP	HVQFN68 - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Industrial	Tape and Reel
IW416UK/A1CZ	WLCSP76 - 3.95 x 3.565 x 0.495 mm, with 0.35 mm pitch	Commercial	Tape and Reel
IW416UK/A1IZ	WLCSP76 - 3.95 x 3.565 x 0.495 mm, with 0.35 mm pitch	Industrial	Tape and Reel

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3 Wi-Fi subsystem

3.1 IEEE 802.11 standards

- 802.11n maximum data rates up to 72 Mbit/s (20 MHz channel bandwidth), 150 Mbit/s (40 MHz channel bandwidth)
- 802.11a/g/b backward compatibility
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement[2]
- 802.11n block acknowledgment extension
- 802.11r fast hand-off for AP roaming[2]
- 802.11u Hotspot 2.0 (STA mode only)
- 802.11v TIM frame transmission/reception[2]
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode

3.2 Wi-Fi MAC

The Wi-Fi MAC has the following features:

- Simultaneous peer-to-peer and infrastructure modes
- RTS/CTS for operation under DCF
- Duplicate frame detection
- On-chip TX and RX FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU RX (de-aggregation) and TX (aggregation)
- 20/40 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgment extension
- Dynamic frequency selection
- TIM frame transmission/reception
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames

2 Available through Host Supplicant

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3.3 Wi-Fi baseband

The Wi-Fi baseband has the following features:

- 802.11n 1x1 SISO
- Bandwidth supported:
  - 20 MHz
  - 20 in 40 MHz (upper and lower)
  - 40 MHz
  - 20 MHz duplicate
- 802.11n modulation coding scheme (MCS) 0-7 and MCS 32 (HT duplicate mode)
- 802.11n 400 ns and 800 ns guard interval
- Dynamic frequency selection (radar detection)
  - Enhanced radar detection for long and short pulse radar
  - Enhanced AGC scheme for DFS channel
- Radio resource measurement
- Optional 802.11n SISO features:
  - 20/40 MHz coexistence
  - 1 spatial stream STBC reception
  - Short guard interval
  - RIFS on receive path for 802.11n packets
  - 802.11n greenfield TX/RX
- Power save features

3.4 Wi-Fi radio

The Wi-Fi radio has the following features:

- Integrated direct-conversion radio
- 20 MHz and 40 MHz channel bandwidths

Wi-Fi RX path

- On-chip LNA with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

Wi-Fi TX path

- Internal PA with power control
- Optimized TX gain distribution for linearity and noise performance

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Radio channel frequencies

The Wi-Fi RF radio integrates all the necessary functions for transmit and receive operation.

The channel frequencies are controlled through an internal bus and software programmable.

Table 3 lists the supported channels (20 MHz).

Table 3. Supported channels (20 MHz)

Channel	Frequency (GHz)
1	2.412
2	2.417
3	2.422
4	2.427
5	2.432
6	2.437
7	2.442
8	2.447
9	2.452
10	2.457
11	2.462
12	2.467
13	2.472
--	--
36	5.180
40	5.200
44	5.220
48	5.240
52	5.260
56	5.280
60	5.300
64	5.320
100	5.500
104	5.520
108	5.540
112	5.560
116	5.580
120	5.600
124	5.620
128	5.640
132	5.660

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Table 3. Supported channels (20 MHz)*...continued*

Channel	Frequency (GHz)
136	5.680
140	5.700
144	5.720
149	5.745
153	5.765
157	5.785
161	5.805
165	5.825

Table 4 lists the supported channels (40 MHz).

Table 4. Supported channels (40 MHz)

Channel	Frequency (GHz)
1–5	2.422
2–6	2.427
3–7	2.432
4–8	2.437
5–9	2.442
6–10	2.447
7–11	2.452
8-12	2.457
9-13	2.462
—	—
36–40	5.190
44–48	5.230
52–56	5.270
60–64	5.310
100–104	5.510
108–112	5.550
116–120	5.590
124–128	5.630
132–136	5.670
149–153	5.755
157–161	5.795

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3.5 Wi-Fi encryption

- AES/CCMP as part of the 802.11i security standard (WPA3, WPA2, WPA2-WPA mixed mode)
- AES/CMAC as part of the 802.11w security standard

3.6 Wi-Fi host interfaces

- SDIO 3.0 device interface

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4 Bluetooth subsystem

4.1 Bluetooth 2.4 GHz TX/RX

- Bluetooth 5.1 features
- Bluetooth Class 2 and Bluetooth Class 1
- Single-ended, shared TX/RX path for Bluetooth
- PCM interface for voice applications
- Baseband and radio basic data rate (BDR)/enhanced data rate (EDR) packet types—1 Mbit/s (GFSK), 2 Mbit/s (π/4-DQPSK), and 3 Mbit/s (8DPSK)
- Fully functional Bluetooth baseband—adaptive frequency hopping (AFH), forward error correction, header error control, access code correlation, Cyclic Redundancy Check (CRC), encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) using packet error rate (PER)
- Interlaced scan for faster connection setup
- Simultaneous active Asynchronous Connection-Less (ACL) connection support
- Automatic ACL packet type selection
- Full central and peripheral piconet support
- Scatternet support
- Standard UART HCI transport layer
- HCI layer to integrate with profile stack
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power-saving mechanisms (hold, sniff modes, and sniff sub-rating)
- Enhanced Power Control (EPC)
- Channel Quality Driven data rate (CQDDR)
- Wide-band Speech (WBS) support (2 WBS link)
- Encryption (AES) support[3]

3 Refer to IW416 errata sheet (ES_IW416).

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4.2 Bluetooth Low Energy (LE)

- Broadcaster, observer, central, and peripheral roles
- Supports link layer topology to be central and peripheral (connects up to 16 links)
- Wi-Fi/Bluetooth coexistence protocol support
- Shared RF with BDR/EDR
- Encryption (AES) support[4]
- Intelligent Adaptive Frequency Hopping (AFH)
- LE Privacy 1.2
- LE Secure Connection [4]
- LE Data Length Extension
- LE Advertising Extension
- LE 2 Mbps
- LE Long Range
- Periodic Advertising Sync Transfer(PAST)
- Advertising Channel Index

4.3 Bluetooth host interfaces

- High-Speed UART interface up to 3 Mbit/s

4.4 Audio interfaces

4.4.1 I2S interface

- I2S (Inter-IC Sound) interface for audio data connection to analog-to-digital converter (ADC)
- Central and peripheral modes for I2S, MSB, and LSB audio interfaces
- 3-state I2S interface compatibility
- I2S pins shared with PCM pins

4.4.2 PCM interface

The PCM interface is used to exchange audio data between the host and the Bluetooth functional block.

- Central or peripheral mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- PCM short frame and long frame synchronization [5]
- 3-state PCM interface capability
- PCM pins shared with I2S pins

4 Refer to IW416 errata sheet (ES_IW416).

5 In PCM central mode, PCM long frame synchronization is 1 clock wide. In PCM peripheral mode, PCM central long frame synchronization pattern is supported.

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4.4.2.1 Protocol description

The PCM interface supports short frame sync. Figure 4 shows an example of a PCM interface with 4 signals.

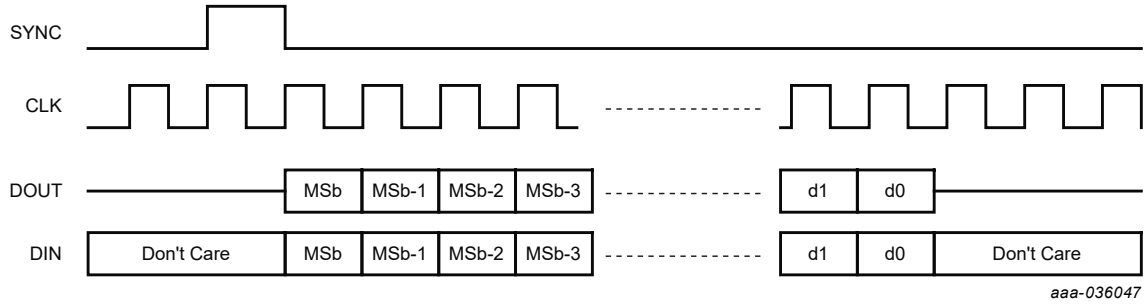

Figure 4. PCM Short Frame Sync

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5 Coexistence

5.1 Antenna configurations

The IW416 supports two antenna configurations: single-antenna and dual-antenna configurations.

5.1.1 Dual-antenna configuration

The two separate antennas allow simultaneous independent operation of the Wi-Fi and Bluetooth radios.

5.1.2 Single-antenna configuration

With the single-antenna configuration, simultaneous 5 GHz Wi-Fi and Bluetooth is supported. In the 2.4 GHz band, the single-antenna configuration allows arbitrated transmit and receive operation of Wi-Fi and Bluetooth.

Table 5 shows the supported TX and/or RX operations with the IW416 single-antenna configuration.

Table 5. Wi-Fi and Bluetooth/Bluetooth LE supported TX and or RX operations - Single-antenna configuration

Row #	Bluetooth/ Bluetooth LE	Wi-Fi 2.4 GHz	Wi-Fi 5 GHz
1	TX	—	TX/RX
2	—	TX	—
3	RX	—	—
4	—	RX	—
5	RX	—	TX/RX

In single-antenna configuration:

- Wi-Fi 2.4 GHz TX and Bluetooth TX operations are arbitrated (rows 1 and 2)
- Wi-Fi 2.4 GHz RX and Bluetooth RX operations are arbitrated (rows 3 and 4)
- Wi-Fi 5 GHz TX/RX and Bluetooth RX or TX operations are simultaneous (rows 1 and 5)

5.2 Central hardware packet traffic arbiter

The central hardware packet traffic arbiter arbitrates the transmit and/or receive operations between the on-chip Wi-Fi and Bluetooth radios as per the supported hardware configuration. See Section 5.1.

In addition to the on-chip radios, the central hardware packet traffic arbiter arbitrates one external radio. Refer to Section 5.3.

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5.3 Coexistence with an external radio

WCI-2 and PTA external coexistence interfaces are used for the coexistence with an external radio.

WCI-2 external coexistence interface

WCI-2 is the two-wire wireless coexistence interface 2 protocol defined in the Bluetooth Core Specification (Vol 7 Part C).

Figure 5 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW416.

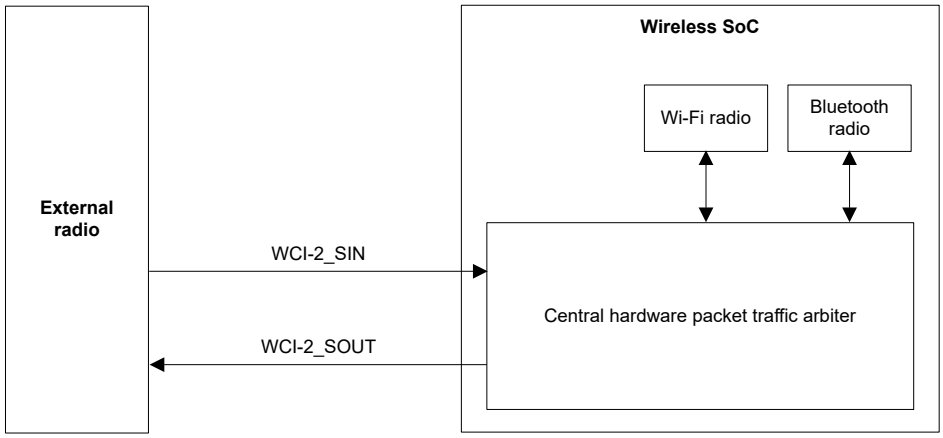

Figure 5. Hardware coexistence interface - WCI-2 coexistence interface

Note: *Refer to Section 6.5.9 for the description of WCI-2 coexistence interface signals.*

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PTA external coexistence interface

Figure 6 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW416.

Note: *The PCM interface and the PTA external coexistence interface share the same multi-function pins (MFP). Refer to Section 6.5.2 "General purpose I/O (GPIO) (MFP)" for more details. As such, when PCM interface is used, WCI-2 is the only interface available for coexistence with an external radio.*

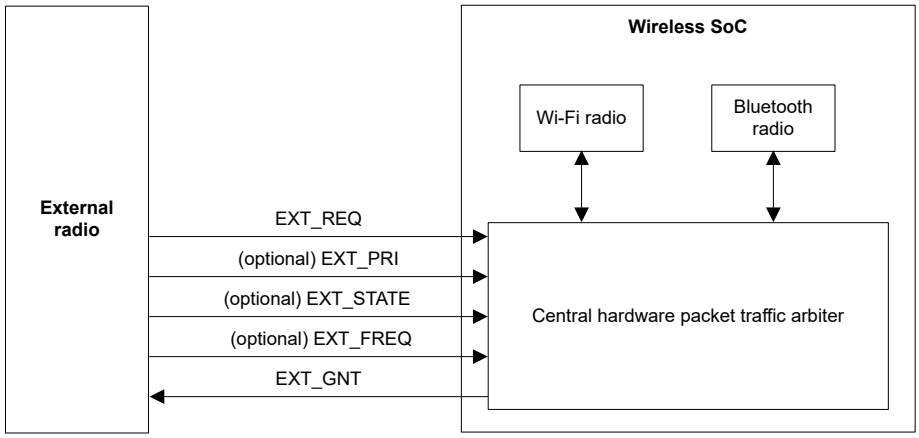

Figure 6. Hardware coexistence interface - PTA external coexistence interface

Note: *Refer to:*

- *Section 6.5.8 for the description of PTA external coexistence interface signals*
- *The application note Coexistence Overview for IW416 (AN13372) for more information on the coexistence feature*

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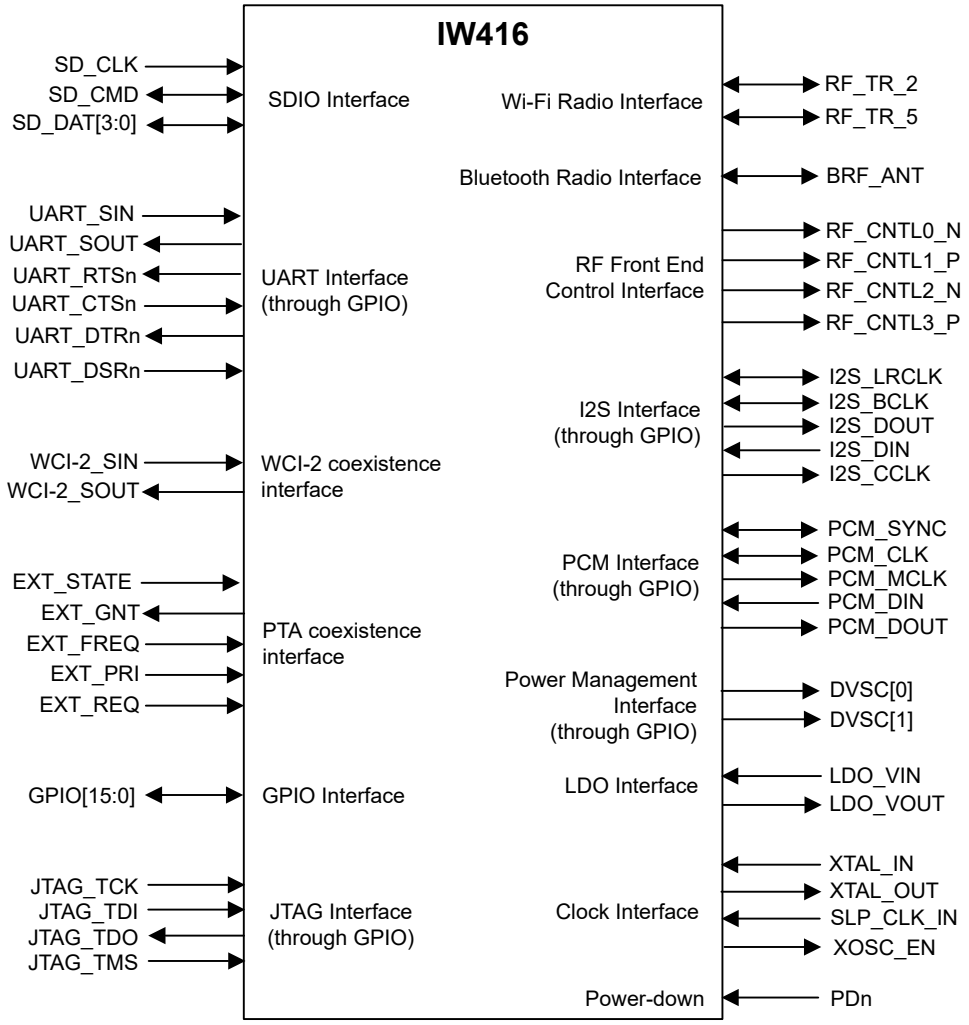
6 Pin information

6.1 Signal diagram

Figure 7 shows the signals for the device. Some signals are muxed through GPIO.



Signals may be muxed. See Section 6.5 "Pin description".

Figure 7. Signal diagram

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6.2 Pin assignment - HVQFN68 package

Note that some pins have muxed signals. See Section 6.5 "Pin description".

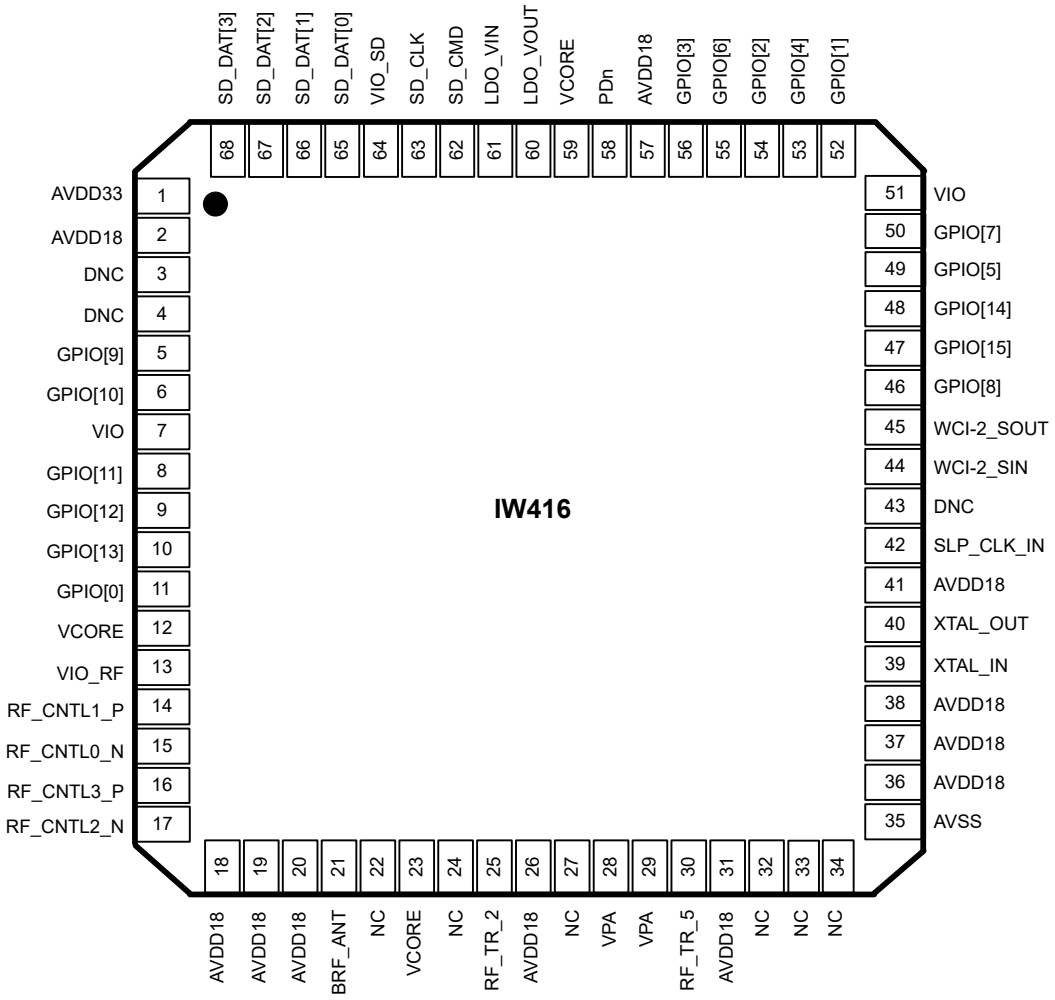

Figure 8. Pin assignment (package top view) - HVQFN68

Note: *See Section 10.10 "Reference clock specifications" for electrical specifications. See Section 11.3 "Package marking" for more information on package marking and pin 1 location.*

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6.2.1 Pin list by number - HVQFN68 package

The following table shows the pin list sorted by pin number.

Table 6. Pin list by number - HVQFN68 package

Pin number	Pin name	Power	Type
1	AVDD33	—	Power
2	AVDD18	—	Power
3	DNC	—	DNC
4	DNC	—	DNC
5	GPIO[9]	VIO	I/O
6	GPIO[10]	VIO	I/O
7	VIO	—	Power
8	GPIO[11]	VIO	I/O
9	GPIO[12]	VIO	I/O
10	GPIO[13]	VIO	I/O
11	GPIO[0]	VIO	I/O
12	VCORE	—	Power
13	VIO_RF	—	Power
14	RF_CNTL1_P	VIO_RF	O
15	RF_CNTL0_N	VIO_RF	O
16	RF_CNTL3_P	VIO_RF	O
17	RF_CNTL2_N	VIO_RF	O
18	AVDD18	—	Power
19	AVDD18	—	Power
20	AVDD18	—	Power
21	BRF_ANT	AVDD18	A, I/O
22	NC	—	NC
23	VCORE	—	Power
24	NC	—	NC
25	RF_TR_2	AVDD18	A, I/O
26	AVDD18	—	Power
27	NC	—	NC
28	VPA	—	Power
29	VPA	—	Power
30	RF_TR_5	AVDD18	A, I/O
31	AVDD18	—	Power
32	NC	—	NC
33	NC	—	NC
34	NC	—	NC

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Table 6. Pin list by number - HVQFN68 package*...continued*

Pin number	Pin name	Power	Type
35	AVSS	—	Ground
36	AVDD18	—	Power
37	AVDD18	—	Power
38	AVDD18	—	Power
39	XTAL_IN	AVDD18	A, I/O
40	XTAL_OUT	AVDD18	A, I/O
41	AVDD18	—	Power
42	SLP_CLK_IN	AVDD18	I
43	DNC	--	DNC
44	WCI-2_SIN	AVDD18	I
45	WCI-2_SOUT	AVDD18	O
46	GPIO[8]	VIO	I/O
47	GPIO[15]	VIO	I/O
48	GPIO[14]	VIO	I/O
49	GPIO[5]	VIO	I/O
50	GPIO[7]	VIO	I/O
51	VIO	—	Power
52	GPIO[1]	VIO	I/O
53	GPIO[4]	VIO	I/O
54	GPIO[2]	VIO	I/O
55	GPIO[6]	VIO	I/O
56	GPIO[3]	VIO	I/O
57	AVDD18	—	Power
58	PDn	AVDD18	I
59	VCORE	—	Power
60	LDO_VOUT	—	Power
61	LDO_VIN	—	Power
62	SD_CMD	VIO_SD	I/O
63	SD_CLK	VIO_SD	I
64	VIO_SD	—	Power
65	SD_DAT[0]	VIO_SD	I/O
66	SD_DAT[1]	VIO_SD	I/O
67	SD_DAT[2]	VIO_SD	I/O
68	SD_DAT[3]	VIO_SD	I/O

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6.2.1 Pin list by name - HVQFN68 package

The following table shows the pin list sorted by pin name.

Table 7. Pin by name - HVQFN68 package

Pin name	Pin number	Power	Type
AVDD18	2	—	Power
AVDD18	18	—	Power
AVDD18	19	—	Power
AVDD18	20	—	Power
AVDD18	26	—	Power
AVDD18	31	—	Power
AVDD18	36	—	Power
AVDD18	37	—	Power
AVDD18	38	—	Power
AVDD18	41	—	Power
AVDD18	57	—	Power
AVDD33	1	—	Power
AVSS	35	—	Ground
BRF_ANT	21	AVDD18	A, I/O
DNC	3	—	DNC
DNC	4	—	DNC
DNC	43	—	DNC
GPIO[0]	11	VIO	I/O
GPIO[1]	52	VIO	I/O
GPIO[10]	6	VIO	I/O
GPIO[11]	8	VIO	I/O
GPIO[12]	9	VIO	I/O
GPIO[13]	10	VIO	I/O
GPIO[14]	48	VIO	I/O
GPIO[15]	47	VIO	I/O
GPIO[2]	54	VIO	I/O
GPIO[3]	56	VIO	I/O
GPIO[4]	53	VIO	I/O
GPIO[5]	49	VIO	I/O
GPIO[6]	55	VIO	I/O
GPIO[7]	50	VIO	I/O
GPIO[8]	46	VIO	I/O
GPIO[9]	5	VIO	I/O
LDO_VIN	61	—	Power

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Table 7. Pin by name - HVQFN68 package*...continued*

Pin name	Pin number	Power	Type
LDO_VOUT	60	—	Power
NC	22	—	NC
NC	24	—	NC
NC	27	—	NC
NC	32	—	NC
NC	33	—	NC
NC	34	—	NC
PDn	58	AVDD18	I
RF_CNTL0_N	15	VIO_RF	O
RF_CNTL1_P	14	VIO_RF	O
RF_CNTL2_N	17	VIO_RF	O
RF_CNTL3_P	16	VIO_RF	O
RF_TR_2	25	AVDD18	A, I/O
RF_TR_5	30	AVDD18	A, I/O
SD_CLK	63	VIO_SD	I
SD_CMD	62	VIO_SD	I/O
SD_DAT[0]	65	VIO_SD	I/O
SD_DAT[1]	66	VIO_SD	I/O
SD_DAT[2]	67	VIO_SD	I/O
SD_DAT[3]	68	VIO_SD	I/O
SLP_CLK_IN	42	AVDD18	I
VCORE	12	—	Power
VCORE	23	—	Power
VCORE	59	—	Power
VIO	7	—	Power
VIO	51	—	Power
VIO_RF	13	—	Power
VIO_SD	64	—	Power
VPA	28	—	Power
VPA	29	—	Power
WCI-2_SIN	44	AVDD18	I
WCI-2_SOUT	45	AVDD18	O
XTAL_IN	39	AVDD18	A, I/O
XTAL_OUT	40	AVDD18	A, I/O

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6.3 Bump locations - WLCSP76 package

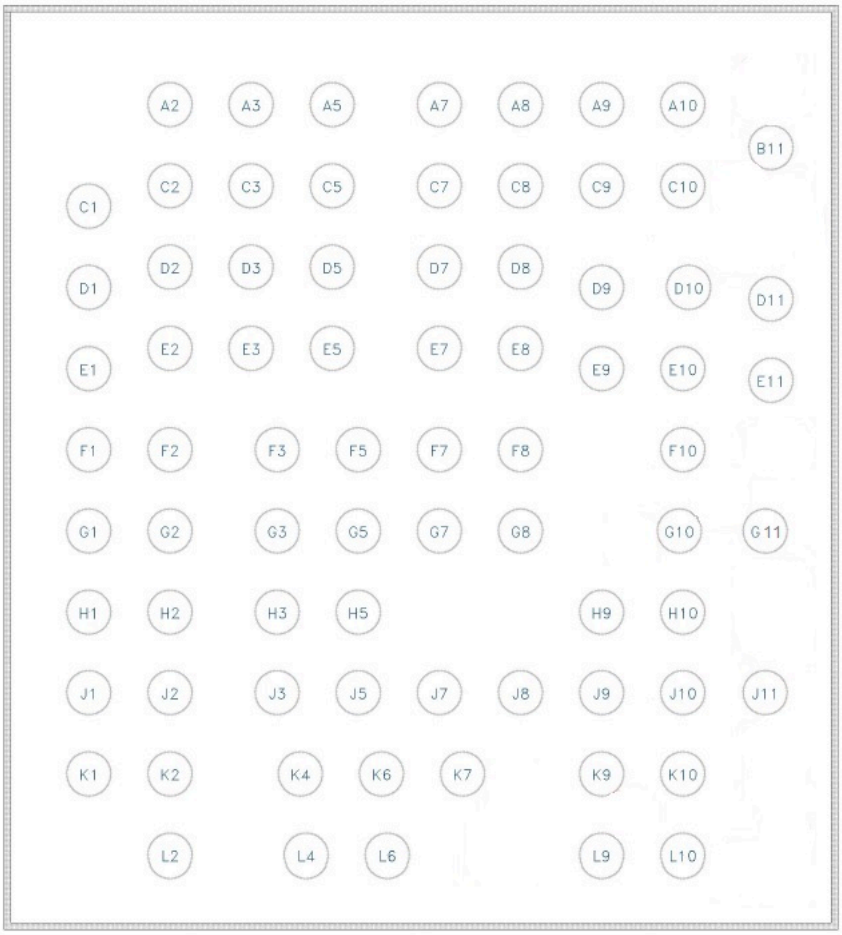

Figure 9. Bump locations - WLCSP76 (non-bump side view, bumps down)

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6.3.1 Bump positions relative to die center - WLCSP76

Table 8. Bump names and locations on WLCSP76 top view

Alpha-numeric designation	Signal name	Bump location relative to die center (non-bump side view)	
		X (um)	Y (um)
A2	SD_DAT[1]	-1080.696	1562.352
A3	SD_DAT[3]	-730.696	1562.352
A5	VIO	-380.696	1562.352
A7	VIO_RF	81.805	1562.352
A8	RF_CNTL1_P	431.805	1562.352
A9	AVDD18	781.805	1562.352
A10	AVDD18	1131.805	1562.352
B11	VSS	1506.805	1377.352
C1	LDO_VIN	-1430.696	1124.852
C2	VIO_SD	-1080.696	1212.352
C3	SD_DAT[2]	-730.696	1212.352
C5	VCORE	-380.696	1212.352
C7	GPIO[0]	81.805	1212.352
C8	VSS	431.805	1212.352
C9	VSS	781.805	1212.352
C10	VSS	1131.805	1212.352
D1	LDO_VOUT	-1430.696	774.852
D2	SD_CLK	-1080.696	862.352
D3	SD_DAT[0]	-730.696	862.352
D5	GPIO[10]	-380.696	862.352
D7	GPIO[13]	81.805	862.352
D8	RF_CNTL0_N	431.805	862.352
D9	RF_CNTL3_P	781.805	774.852
D10	VSS	1156.805	774.852
D11	BRF_ANT	1506.805	724.852
E1	VCORE	-1430.696	424.852
E2	SD_CMD	-1080.696	512.352
E3	VSS	-730.696	512.352
E5	GPIO[9]	-380.696	512.352
E7	GPIO[11]	81.805	512.352
E8	GPIO[12]	431.805	512.352
E9	RF_CNTL2_N	781.805	424.852
E10	VSS	1131.805	424.852

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Table 8. Bump names and locations on WLCSP76 top view*...continued*

Alpha-numeric designation	Signal name	Bump location relative to die center (non-bump side view)	
		X (um)	Y (um)
E11	AVDD18	1506.805	374.852
F1	VSS	-1430.696	74.852
F2	GPIO[3]	-1080.696	74.852
F3	GPIO[7]	-618.196	74.852
F5	VSS	-268.196	74.852
F7	WCI-2_SOUT	81.805	74.852
F8	WCI-2_SIN	431.805	74.852
F10	VSS	1131.805	74.852
G1	GPIO[6]	-1430.696	-275.148
G2	GPIO[4]	-1080.696	-275.148
G3	GPIO[5]	-618.196	-275.148
G5	GPIO[14]	-268.196	-275.148
G7	SLP_CLK_IN	81.805	-275.148
G8	DNC	431.805	-275.148
G10	AVDD18	1116.805	-275.148
G11	RF_TR_2	1481.805	-275.148
H1	PDn	-1430.696	-625.148
H2	GPIO[1]	-1080.696	-625.148
H3	GPIO[8]	-618.196	-625.148
H5	VSS	-268.196	-625.148
H9	VCORE	781.805	-625.148
H10	VSS	1131.805	-625.148
J1	AVDD18	-1430.696	-975.148
J2	VSS	-1080.696	-975.148
J3	AVDD18	-618.196	-975.148
J5	VSS	-268.196	-975.148
J7	VSS	81.805	-975.148
J8	VSS	431.805	-975.148
J9	VSS	781.805	-975.148
J10	VPA	1131.805	-975.148
J11	RF_TR_5	1481.805	-975.148
K1	GPIO[2]	-1430.696	-1325.148
K2	VIO	-1080.696	-1325.148
K4	XTAL_OUT	-518.196	-1325.148
K6	VSS	-168.196	-1325.148

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Table 8. Bump names and locations on WLCSP76 top view*...continued*

Alpha-numeric designation	Signal name	Bump location relative to die center (non-bump side view)	
		X (um)	Y (um)
K7	AVDD18	181.805	-1325.148
K9	VSS	781.805	-1325.148
K10	VSS	1131.805	-1325.148
L2	GPIO[15]	-1080.696	-1675.148
L4	XTAL_IN	-493.196	-1675.148
L6	AVDD18	-143.195	-1675.148
L9	AVDD18	781.805	-1675.148
L10	VSS	1131.805	-1675.148

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6.4 Pin types

Table 9. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A,O	Analog output
A, I/O	Analog input/output
NC	No connect
DNC	Do not connect
Power	Power
Ground	Ground

6.5 Pin description

6.5.1 Pin states

The pin states information provided in the tables includes:

- **No Pad Power State** indicates the state when there is no power
- **PwrDwn State** denotes the power-down state in default configuration. Many pads have programmable power-down values, which can be set by firmware.
- **Reset State** is the state after the power-on-reset state and before the hardware state (HW State)
- **HW State** (hardware state) is the state after boot code finishes and before firmware download begins (firmware may change the pin state). HW State may differ based on the pin muxing/strap setting. For example, for UART_RTSn and UART_SOUT, the boot code will enable the UART interface when the device is in mode, making the HW states output high and output low, respectively.
- **PwrDwn Prog** indicates if the power-down state can be programmed
- **Internal PU/PD** columns indicates the following:
  - Type of PU/PD (weak vs nominal)
  - The polarity (PU vs. PD)

  The internal pull-up or pull-down applies when the pin is in input mode
- **PU** denotes whether the pull-up can be programmed or not
- **PD** denotes whether the pull-down can be programmed or not
- Pull-up and pull-down are only effective when the pad is in input mode
- After firmware is downloaded, the pads (GPIO, RF control, and so on) are programmed in functional mode per the functionality of the pins

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6.5.2 General purpose I/O (GPIO) (MFP)

Table 10. GPIO[1] (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[15]	VIO	3-state	input	input	drive high	yes	nominal PU	yes	yes
GPIO mode: GPIO[15] (input/output) **JTAG mode**: JTAG_TMS - JTAG test mode select (input). See Section 6.5.13 "JTAG interface". **Reset recovery mode**: Independent software reset for Bluetooth subsystem (input)									
GPIO[14]	VIO	3-state	input	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[14] (input/output) **JTAG mode**: JTAG_TCK - JTAG test clock (input). See Section 6.5.13 "JTAG interface". **Reset recovery mode**: Independent software reset for Wi-Fi subsystem (input)									
GPIO[13]	VIO	3-state	input	input	drive high	yes	nominal PU	yes	yes
GPIO mode: GPIO[13] (input/output) **UART mode**: UART_DTRn - UART data-terminal-ready (output). See Section 6.5.6 "UART host interface". **Out-of-band wake-up mode**: Host to IW416 Wi-Fi wake-up (input)									
GPIO[12]	VIO	3-state	input	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[12] (input/output) **UART mode**: UART_DSRn - UART data-set-ready (input) (active low).See Section 6.5.6 "UART host interface". **Out-of-band wake-up mode**: Host to IW416 Bluetooth wake-up (input)									
GPIO[11]	VIO	3-state	output	input	drive high	yes	weak PU	yes	yes
GPIO mode: GPIO[11] (input/output) This pin is used as a configuration pin: CON[8] (input) See Section 6.6 "Configuration pins". **UART mode**: UART_RTSn - UART request-to-send (output) (active low). See Section 6.5.6 "UART host interface".									
GPIO[10]	VIO	3-state	input	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[10] (input/output) **UART mode**: UART_SOUT - UART serial (output). See Section 6.5.6 "UART host interface".									
GPIO[9]	VIO	3-state	output	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[9] (input/output) **UART mode**: UART_SIN - UART serial (input). See Section 6.5.6 "UART host interface".									
GPIO[8]	VIO	3-state	input	input	drive low	yes	weak PU	yes	yes
GPIO mode: GPIO[8] (input/output) This pin is used as a configuration pin: CON[7] (input) See Section 6.6 "Configuration pins". **UART mode**: UART_CTSn - UART clear-to-send input signal (input, active low). See Section 6.5.6 "UART host interface".									
GPIO[7]	VIO	3-state	input	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[7] (input/output) **PCM mode**: PCM_SYNC - PCM frame sync (input if peripheral, output if central). See Section 6.5.7 "Audio interface". **I2S mode**: I2S_LRCLK - I2S left-right clock (input if peripheral, output if central). See Section 6.5.7 "Audio interface". **PTA coexistence mode**: EXT_REQ - Request from the external radio (input). See Section 6.5.8 "PTA coexistence interface".									

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Table 10. GPIO[1] (MFP)...*continued*

Pins may be Multi-Functional Pins (MFP).

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[6]	VIO	3-state	input	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[6] (input/output) **PCM mode**: PCM_CLK - PCM data clock (input if peripheral, output if central). See Section 6.5.7 "Audio interface". **I2S mode**: I2S_BCLK - I2S bit clock (input if peripheral, output if central). See Section 6.5.7 "Audio interface". **PTA coexistence mode**: EXT_PRI - External radio priority signal (input). See Section 6.5.8 "PTA coexistence interface".									
GPIO[5]	VIO	3-state	input	input	3-state	yes	weak PU	yes	yes
GPIO mode: GPIO[5] (input/output) **PCM mode**: PCM_DIN[2] - PCM receive signal (input). See Section 6.5.7 "Audio interface". **I2S mode**: I2S_DOUT/I2S_DIN - I2S transmit/receive signal (output/input) (depending on the configuration). See Section 6.5.7 "Audio interface". **PTA coexistence mode**: EXT_GNT - External radio grant signal (output). See Section 6.5.8 "PTA coexistence interface".									
GPIO[4]	VIO	3-state	output	input	3-state	yes	nominal PU	yes	yes
GPIO mode: GPIO[4] (input/output) **PCM mode**: PCM_DOUT[3] - PCM transmit signal (output). See Section 6.5.7 "Audio interface". **I2S mode**: I2S_DOUT/I2S_DIN (depending on the configuration. If GPIO[5] is configured as I2S_DIN, then GPIO[4] is set as I2S_DOUT, and vice-verse). See Section 6.5.7 "Audio interface". **PTA coexistence mode**: EXT_FREQ - External radio frequency signal (input). See Section 6.5.8 "PTA coexistence interface". **Out-of-band wake-up mode**: IW416 Bluetooth to host wake-up signal (output)[4]									
GPIO[3]	VIO	3-state	input	input	3-state	yes	weak PU	yes	yes
GPIO mode: GPIO[3] (input/I/Ooutput) **Power management mode**: DVSC[1], Digital voltage scaling control (output) **JTAG mode:** JTAG_TDO, JTAG test data (output). See Section 6.5.13 "JTAG interface". **PCM mode**: PCM_MCLK (output) - PCM clock signal (output, optional). See Section 6.5.7 "Audio interface". **I2S mode**: I2S_CCLK - I2S clock (output, optional). See Section 6.5.7 "Audio interface".									
GPIO[2]	VIO	3-state	input	input	3-state	yes	weak PU	yes	yes
GPIO mode: GPIO[2] (input/output) **Power management mode**: DVSC[0], Digital voltage scaling control (output) **JTAG mode:** JTAG_TDI, JTAG test data (input). See Section 6.5.13 "JTAG interface".									
GPIO[1]	VIO	3-state	input	input	3-state	yes	weak PU	yes	yes
GPIO mode: GPIO[1] (input/output) This pin is used as a configuration pin: CON[9] (input). See Section 6.6 "Configuration pins". **PTA coexistence mode**: EXT_STATE - External radio state signal (input). See Section 6.5.8 "PTA coexistence interface". **Out-of-band wake-up mode**: IW416 Wi-Fi to host wake-up signal (output)									
GPIO[0]	VIO	3-state	output	output	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[0] (input/output) **Oscillator enable mode**: XOSC_EN (output) (active high). See Section 6.5.10 "Clock interface".									

[1] Not all GPIO pins can be used for Host-to-SoC wake-up signals.
[2] The function can be swapped with GPIO[4] using a software command without affecting the hardware connection.
[3] The function can be swapped with GPIO[5] using a software command without affecting the hardware connection.
[4] If PCM and UART interfaces are used in application, use GPIO[0] as alternative for this wake-up signa

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6.5.3 Wi-Fi/Bluetooth radio interface

Table 11. Wi-Fi/Bluetooth radio interface

Pin Name	Type	Supply	Description
RF_TR_2	A, I/O	AVDD18	Wi-Fi Transmit/Receive (2.4 GHz)
RF_TR_5	A, I/O	AVDD18	Wi-Fi Transmit/Receive (5 GHz)
BRF_ANT	A, I/O	AVDD18	Bluetooth Transmit/Receive

6.5.4 Wi-Fi RF front-end control interface

Table 12. Wi-Fi RF front-end control interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/PD	PU	PD
RF_CNTL0_N	VIO_RF	tristate	input	output	drive low	yes	weak PU	no	no
RF Control 0—RF Control Output Low (output) This pin is used as a configuration pin: CON[0] (input) See Section 6.6 "Configuration pins".									
RF_CNTL1_P	VIO_RF	tristate	input	output	drive high	yes	weak PU	no	no
RF Control 1—RF Control Output High (output) This pin is used as a configuration pin: CON[6] (input)									
RF_CNTL2_N	VIO_RF	tristate	input	output	drive low	yes	weak PU	no	no
RF Control 2—RF Control Output Low (output) This pin is used as a configuration pin: CON[1] (input) See Section 6.6 "Configuration pins".									
RF_CNTL3_P	VIO_RF	tristate	input	output	drive high	yes	weak PU	no	no
RF Control 3—RF Control Output High (output) This pin is used as a configuration pin: CON[5] (input) See Section 6.6 "Configuration pins".									

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6.5.5 SDIO host interface (MFP)

Table 13. SDIO host i (MFP)

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Clock input **SDIO 1-bit mode**: Clock input									
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Command/response (input/output) **SDIO 1-bit mode**: Command line (input/output)									
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[3] **SDIO 1-bit mode**: Reserved									
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[2] or read wait (optional) **SDIO 1-bit mode**: Read wait (optional)									
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[1] **SDIO 1-bit mode**: Interrupt									
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[0] **SDIO 1-bit mode**: Data line									

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6.5.6 UART host interface

Table 14. UART host interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
UART_SIN	I	VIO	UART serial input signal - muxed with GPIO[9]
UART_SOUT	O	VIO	UART serial output signal - muxed with GPIO[10]
UART_RTSn	O	VIO	UART request-to-send output signal (active low) - muxed with GPIO[11]
UART_CTSn	I	VIO	UART clear-to-send input signal (active low) - muxed with GPIO[8]
UART_DTRn	O	VIO	UART data-terminal-ready output signal (active low) - muxed with GPIO[13]
UART_DSRn	I	VIO	UART data-set-ready input signal (active low) - muxed with GPIO[12]

6.5.7 Audio interface

Table 15. Audio interface pins (MFP)

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
PCM_DIN	I	VIO	PCM audio codec output data (for recording) - muxed with GPIO[4]/ GPIO[5]
PCM_DOUT	O	VIO	PCM audio codec input data (for playback) - muxed with GPIO[4]/ GPIO[5]
PCM_SYNC	I/O	VIO	PCM sync pulse signal - muxed with GPIO[7] . Central mode: output . Peripheral mode: input
PCM_CLK	I/O	VIO	PCM clock signal - muxed with GPIO[6] . Central mode: output . Peripheral mode: input
PCM_MCLK	O	VIO	PCM codec main clock signal (optional) - muxed with GPIO[3] Optional clock used for some codecs. Derived from PCM_CLK.
I2S_DIN	I	VIO	I2S audio codec output data (for recording) - muxed with GPIO[4]/ GPIO[5], depending on the configuration.
I2S_DOUT	O	VIO	I2S audio codec input data (for playback) - muxed with GPIO[4]/ GPIO[5], depending on the configuration.
I2S_LRCLK	I/O	VIO	I2S audio left/right clock - muxed with GPIO[7] . Central mode: output . Peripheral mode: input
I2S_BCLK	I/O	VIO	I2S audio bit clock - muxed with GPIO[6] . Central mode: output . Peripheral mode: input
I2S_CCLK	O	VIO	I2S codec main clock (optional) - muxed with GPIO[3] Optional clock used for some codecs. Derived from I2S_BCLK.

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6.5.8 PTA coexistence interface

Table 16. PTA coexistence interface (MFP)

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
EXT_STATE	I	VIO	External radio state input signal - muxed with GPIO[1] External radio traffic direction (TX/RX): • 1: TX • 0: RX
EXT_GNT	O	VIO	External radio grant output signal - muxed with GPIO[5]
EXT_FREQ	I	VIO	External radio frequency input signal - muxed with GPIO[4] Frequency overlap between external radio and Wi-Fi: • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
EXT_PRI	I	VIO	External radio input priority signal - muxed with GPIO[6] Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also have TX/RX info following the priority info if EXT_STATE is not used.
EXT_REQ	I	VIO	Request from the external radio - muxed with GPIO[7]

6.5.9 WCI-2 coexistence interface

Table 17. WCI-2 coexistence interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/PD	PU	PD
WCI-2_SIN	AVDD18	tristate	input	input	tristate	no	weak PU	yes	yes
WCI-2_SIN (input)									
WCI-2_SOUT	AVDD18	tristate	output	output	tristate	no	weak PU	yes	yes
WCI-2_SOUT (output)									

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6.5.10 Clock interface

Table 18. Clock interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
XTAL_IN	AVDD18	–	–	–	–	–	–	–	–
Reference clock input The reference clock signal frequency must be 26 MHz or 40 MHz from an external crystal or external crystal oscillator. The power consumption in sleep mode is lower with an external crystal compared to an external crystal oscillator when an external sleep clock is not used. See Section 10.10 "Reference clock specifications".									
XTAL_OUT	AVDD18	–	–	–	–	–	–	–	–
Connect this pin to an external crystal when an external crystal is used. When an external crystal oscillator is used, connect this pin to ground with resistance less than 100 Ω.									
SLP_CLK_IN	AVDD18	tristate	input	input	tristate	no	nominal PU	yes	yes
Sleep clock input (optional) Used for lower power operation in sleep mode. • An external sleep clock of 32.768 kHz can be used to reduce the current consumption in sleep mode. • If no external sleep clock is used, leave this pin floating (DNC).									
XOSC_EN	VIO	–	–	–	–	–	–	–	–
Oscillator enable (output) (active high) XOSC_EN signal can be used ONLY when an external sleep clock is used. Used to enable an external oscillator. 0 = disable external oscillator 1 = enable external oscillator ***Note:*** *Muxed with GPIO[0].*									

6.5.11 Power down (PDn) pin

Table 19. Power down (PDn) pin

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
PDn	AVDD18	--	--	--	--	--	--	--	--
Full power-down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.8V to 4.5V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin.									

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6.5.12 Power supply and ground

Table 20. Power and ground pins

Pin Name	Type	Description
VCORE	Power	1.05V core power supply
VIO	Power	1.8V/3.3V digital I/O power supply
VIO_SD	Power	1.8V/3.3V digital I/O SDIO power supply ***Note:*** *1. For SDIO 2.0, VIO_SD must be 3.3 V* *2. For SDIO 3.0, VIO_SD must be 1.8 V*
VIO_RF	Power	1.8V/3.3V analog I/O RF power supply
AVDD33	Power	3.3V analog power supply
AVDD18	Power	1.8V analog power supply
VPA	Power	2.2V analog power supply
LDO_VIN	Power	LDO voltage input (1.8V)
LDO_VOUT	Power	LDO voltage output
AVSS	Ground	Ground
NC	NC	No Connect
DNC	DNC	Do Not Connect Do not connect these pins. Leave these pins floating.

6.5.13 JTAG interface

Table 21. JTAG interface pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
JTAG_TDO	O	VIO	JTAG test data output signal - muxed with GPIO[3]
JTAG_TDI	I	VIO	JTAG test data input signal - muxed with GPIO[2]
JTAG_TMS	I	VIO	JTAG test mode select input signal - muxed with GPIO[15]
JTAG_TCK	I	VIO	JTAG test clock input signal - muxed with GPIO[14]

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6.6 Configuration pins

The table below shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function.

To set a configuration bit to 0, attach a 50 kΩ–100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 22. Configuration pins

Configuration bits	Pin name	Configuration function
CON[9]	GPIO[1]	Reserved Set to 111.
CON[8]	GPIO[11]	
CON[7]	GPIO[8]	
CON[6]	RF_CNTL1_P	Reserved Set to 1.
CON[5]	RF_CNTL3_P	Reference clock frequency select 1 = 26 MHz (default) 0 = 40 MHz
CON[1]	RF_CNTL2_N	Host configuration options (see Table 23). No hardware impact. Software reads and boots accordingly. See the table below. ***Note:*** *The boot code needs to use the strap value to set the correct boot sequence.*
CON[0]	RF_CNTL0_N	

Table 23 shows the host configuration options.

Table 23. Host configuration options

RF_CNTL2_N/ CON[1]	RF_CNTL0_N/ CON[0]	Wi-Fi	Bluetooth/ Bluetooth LE	Number of SDIO functions
1	0	SDIO	UART	1 (Wi-Fi)
Others	Others	Reserved	Reserved	—

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7 Power information

The table in Section 6.5.12 "Power supply and ground" shows the required voltage levels for each rail and PDn input signal.

7.1 Power modes

The IW416 power modes reflect the combination of the respective state of Wi-Fi and Bluetooth subsystems.

Table 24 shows the device power modes, Wi-Fi and Bluetooth states, and associated Wi-Fi and Bluetooth CPU status.

Refer to Section 10.6 "Current consumption" for the power consumption values of Wi-Fi and Bluetooth subsystems.

Table 24. Device power modes

Device mode	Wi-Fi state	Bluetooth state	Wi-Fi CPU status	Bluetooth CPU status
Wi-Fi and Bluetooth active	Active	Active	Active	Active
Standby/idle	Standby/idle	Standby/idle	Active	Active
Wi-Fi active	Active	Sleep	Active	WFI [1]
Bluetooth active	Sleep	Active	WFI	Active
Sleep	Sleep	Sleep	WFI	WFI
Deep-sleep[2]	Deep-sleep	Deep-sleep	--	--

[1] Wait for Interrupt: the ARM-based CPU is in low-power standby state.
[2] Memory placed in low-power retention mode.

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7.2 Power-up sequence

The IW416 VCORE is supplied through an external PMIC. The PDn pin of the IW416 is tied to 1.8V. The ramp-up is controlled by the Host using PMIC_EN, the input enable pin of the power regulator.

The power configuration is detailed in Section 7.2.1 "Configuration—VCORE from PMIC" and Section 7.2.2 "Power-up sequence timing" shows the power-up timing.

7.2.1 Configuration—VCORE from PMIC

- VCORE from PMIC
- PMIC_EN ramps up from Host 3.3V or Host GPIO pin
- PDn supplied from AVDD18 (follow AVDD18; PDn is connected 1.8V supply)
- External VPA/AVDD18 from PMIC
- External VIO/VIO_RF from Host (1.8V/3.3V)

Table 25. Configuration—VCORE from PMIC [1]

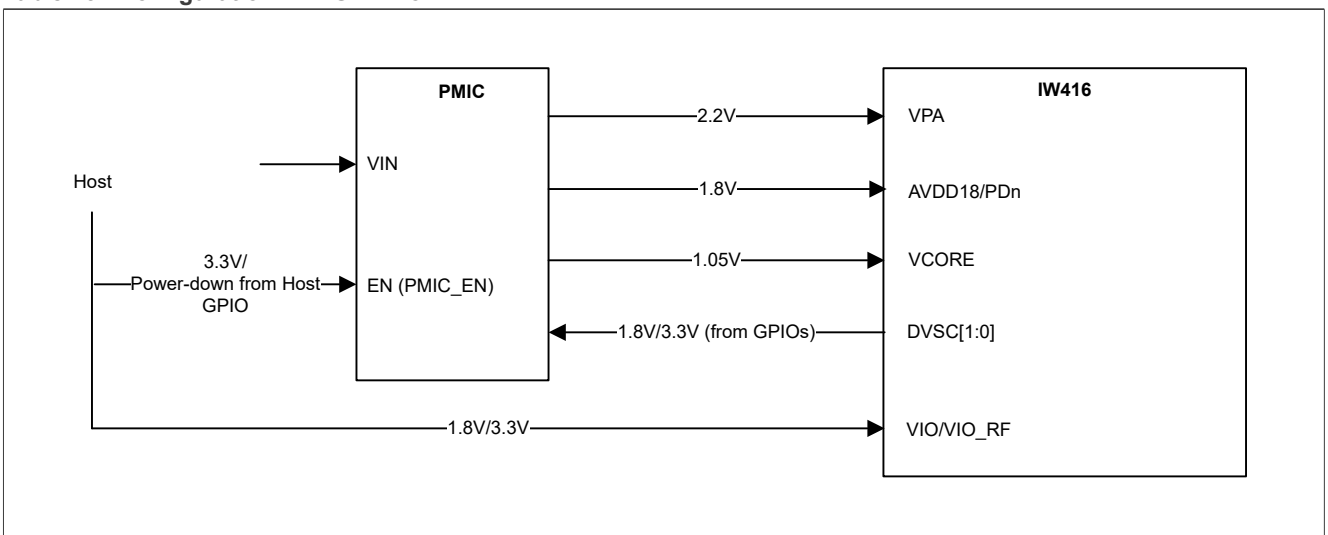

Figure 10. Configuration—VCORE from PMIC

[1] A minimum time of 100 ms is required after PMIC_EN is deasserted (=0) and before it is asserted (=1).

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7.2.2 Power-up sequence timing

- VPA must be good (90%) before AVDD18 starts ramping up.
- AVDD18 must be good (90%) before VCORE starts ramping up.

Figure 11 shows the power-up sequence.

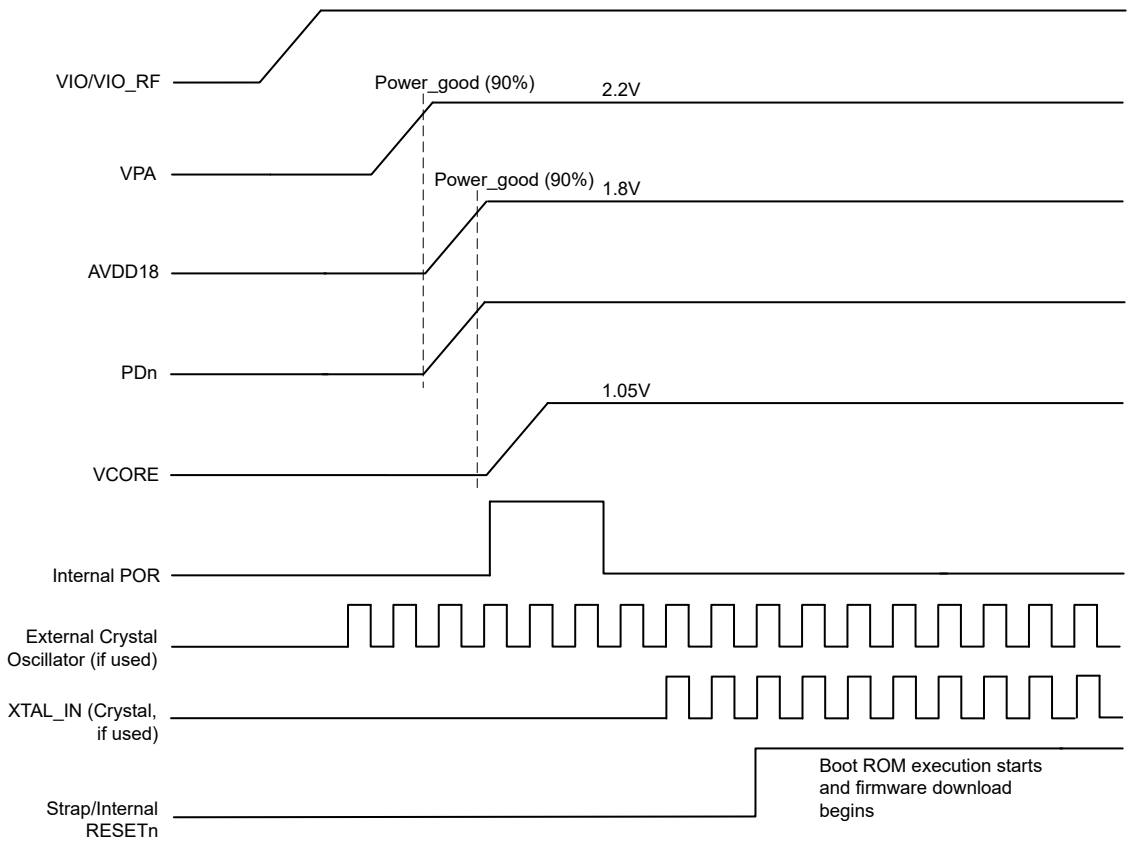

Figure 11. Power-up sequence

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7.3 Power-down sequence

It is recommended:

- To ramp down AVDD18 after VPA ramps down
- To discharge all of the power supplies to less than 0.2V to reduce leakage.

PDn must be asserted when powering down the device.

Figure 12 shows the power-down sequence.

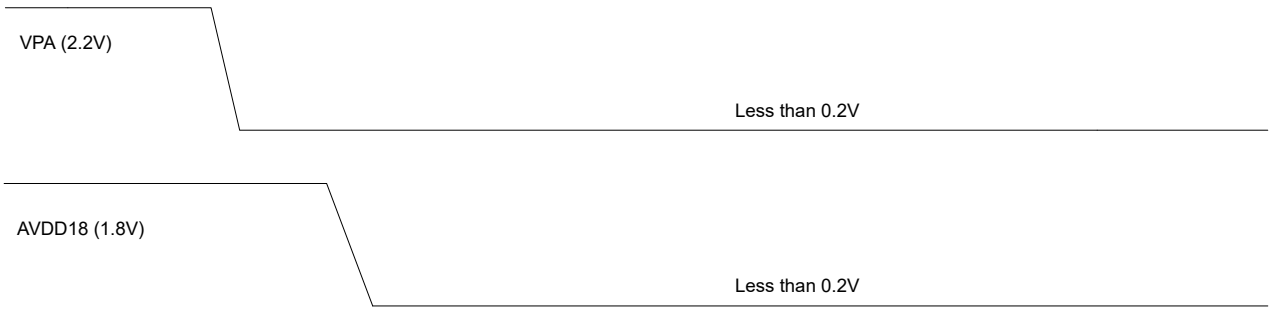

Figure 12. Power-down sequence

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7.4 Leakage optimization

For applications not using Wi-Fi and Bluetooth, the device can be put into a low-leakage mode of operation. Two methods are available to set the device to low-leakage mode:

- Using PDn pin
  The power-down state provides the lowest leakage mode of operation. Assert PDn low to enter power-down. If firmware is not downloaded, the device must be kept in power-down mode to reduce the leakage.
- Powering off all the rails
  Alternatively, all the power rails can be powered off. In this case, the state of the PDn pin is irrelevant.

7.5 Deep sleep

When a programmable power regulator is used to supply VCORE, the IW416 may use the power management interface to reduce VCORE to approximately 0.8V to reduce power consumption in deep sleep mode.

7.6 Reset

The IW416 is reset to its default operating state under any of the following conditions:

- Internal Power-On Reset (POR): POR is triggered when the device receives power and VCORE and AVDD18 supplies are good. See Section 7.2 "Power-up sequence".
- Software/firmware reset: software/firmware issues a reset.
- External PDn pin assertion: the device is reset when the PDn input pin is <0.5 V and transitions from low to high.

See Section 10.11 "Power down (PDn) pin specifications" for the electrical specifications.

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8 Absolute maximum ratings

CAUTION: The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 26. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCORE	Core power supply	-	1.15	V
VIO	1.8 V/3.3 V digital I/O power supply	-	2.2	V
		-	4.0	V
VIO_SD	1.8 V/3.3 V digital I/O power supply	-	2.2	V
		-	4.0	V
VIO_RF	1.8 V/3.3 V digital I/O power supply	-	2.2	V
		-	4.0	V
AVDD18	1.8 V analog power supply	-	1.98	V
VPA	2.2 V analog power supply	-	2.3	V
AVDD33	3.3 V analog power supply	-	3.96	V
LDO_VIN	LDO input voltage supply	-	2.0	V
$T_{STORAGE}$	Storage temperature	-55	+125	°C

Table 27. Limiting values

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)[1]	-2	+2	kV
		charged device model (CDM)[2]	-500	+500	V

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002

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9 Recommended operating conditions

Note: *Operation beyond the recommended operating conditions is neither recommended nor guaranteed.*

Table 28. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCORE	1.05V core power supply	Active mode	1.018	1.05	1.10	V
VIO	1.8V/3.3V digital I/O power supply	—	1.62	1.8	1.98	V
		—	2.97	3.3	3.47	V
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	—	1.62	1.8	1.98	V
		—	2.97	3.3	3.47	V
VIO_RF	1.8V/3.3V I/O power supply	—	1.62	1.8	1.98	V
		—	2.97	3.3	3.47	V
AVDD18	1.8V analog power supply	—	1.71	1.8	1.89	V
VPA	2.2V analog power supply	—	2.09	2.2	2.26	V
AVDD33	3.3V analog power supply	—	3.14	3.3	3.46	V
LDO_VIN	LDO input voltage supply	—	1.71	1.8	1.89	V
T_A	Ambient operating temperature	Commercial	0	—	70	°C
T_A	Ambient operating temperature	Industrial	-40	-	85	°C
T_J	Junction temperature	—	—	—	125	°C

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10 Electrical specifications

10.1 GPIO/LED interface specifications

The GPIO pins are powered by VIO voltage supply.

10.1.1 VIO DC characteristics

10.1.1.1 1.8V operation

Table 29. DC electrical characteristics—1.8V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

10.1.1.2 3.3V operation

Table 30. DC electrical characteristics—3.3V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

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10.2 RF front-end control interface specifications

10.2.1 VIO_RF DC characteristics

10.2.1.1 1.8V operation

Table 31. DC electrical characteristics—1.8V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_RF	--	VIO_RF+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_RF-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

10.2.1.2 3.3V operation

Table 32. DC electrical characteristics—3.3V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_RF	--	VIO_RF+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_RF-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

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10.3 Wi-Fi radio specifications

The Wi-Fi radio interface pins are powered by AVDD18.

10.3.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port.

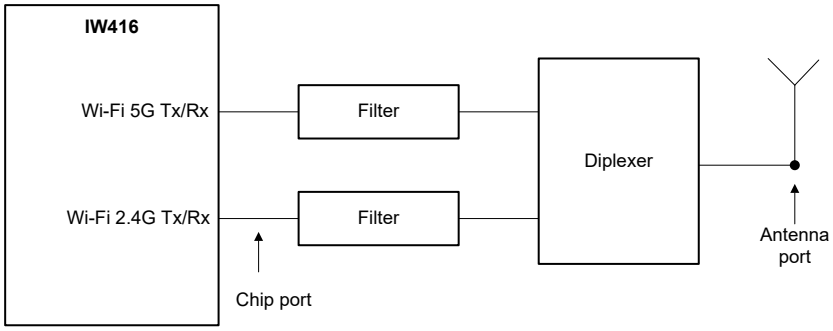

Figure 13. RF performance measurement points

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10.3.2 2.4 GHz Wi-Fi receive performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.*

Table 33. 2.4 GHz Wi-Fi receive performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	—	2484	MHz
Maximum RX input level	Maximum RX input level without device damage	—	—	2	dBm
Receiver sensitivity 802.11b	1 Mbit/s	—	-99	—	dBm
	2 Mbit/s	—	-95	—	dBm
	5.5 Mbit/s	—	-94	—	dBm
	11 Mbit/s	—	-91	—	dBm
Receiver sensitivity 802.11g	6 Mbit/s	—	-92	—	dBm
	9 Mbit/s	—	-92	—	dBm
	12 Mbit/s	—	-91	—	dBm
	18 Mbit/s	—	-89	—	dBm
	24 Mbit/s	—	-86	—	dBm
	36 Mbit/s	—	-83	—	dBm
	48 Mbit/s	—	-78	—	dBm
	54 Mbit/s	—	-77	—	dBm
Receiver sensitivity 802.11n HT20[1]	MCS0	—	-92	—	dBm
	MCS1	—	-90	—	dBm
	MCS2	—	-87	—	dBm
	MCS3	—	-84	—	dBm
	MCS4	—	-81	—	dBm
	MCS5	—	-76	—	dBm
	MCS6	—	-75	—	dBm
	MCS7	—	-73[2]	—	dBm
Receiver sensitivity 802.11n HT40[1]	MCS0	—	-89	—	dBm
	MCS1	—	-87	—	dBm
	MCS2	—	-84	—	dBm
	MCS3	—	-82	—	dBm
	MCS4	—	-78	—	dBm
	MCS5	—	-74	—	dBm
	MCS6	—	-72	—	dBm
	MCS7	—	-71	—	dBm

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Table 33. 2.4 GHz Wi-Fi receive performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Receiver maximum input level 802.11	802.11b	—	5	—	dBm
	802.11g	—	-4	—	dBm
	MCS0-4	—	-2	—	dBm
	MCS5	—	-4	—	dBm
	MCS6	—	-5	—	dBm
	MCS7	—	-8	—	dBm
Receiver adjacent channel interference rejection (ACI) 802.11b	1Mbit/s	—	41	—	dB
	2Mbit/s	—	39	—	dB
	5.5Mbit/s	—	38	—	dB
	11Mbit/s	—	37	—	dB
Receiver adjacent channel interference rejection (ACI) 802.11g	6Mbit/s	—	31	—	dB
	9Mbit/s	—	30	—	dB
	12Mbit/s	—	28	—	dB
	18Mbit/s	—	29	—	dB
	24Mbit/s	—	26	—	dB
	36Mbit/s	—	23	—	dB
	48Mbit/s	—	19	—	dB
	54Mbit/s	—	21	—	dB
Receiver adjacent channel interference rejection (ACI) 802.11n HT20	MCS0	—	31	—	dB
	MCS1	—	28	—	dB
	MCS2	—	31	—	dB
	MCS3	—	30	—	dB
	MCS4	—	27	—	dB
	MCS5	—	25	—	dB
	MCS6	—	24	—	dB
	MCS7	—	23	—	dB
Receiver adjacent channel interference rejection (ACI) 802.11n HT40	MCS0	—	28	—	dB
	MCS1	—	27	—	dB
	MCS2	—	24	—	dB
	MCS3	—	23	—	dB
	MCS4	—	19	—	dB
	MCS5	—	16	—	dB
	MCS6	—	14	—	dB
	MCS7	—	12	—	dB

[1] With BCC waveform
[2] De-sense of ~1 dB at 2417 MHz

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10.3.3 5 GHz Wi-Fi receive performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, averaged over one channel per sub-band, and at the chip port.*

Table 34. 5 GHz Wi-Fi receive performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	5 GHz—IEEE 802.11n/a	5150	—	5850	MHz
Maximum receiver input level	Maximum receive input level without device damage	—	—	2	dBm
Receiver sensitivity 802.11a	6 Mbit/s	—	-90	—	dBm
	9 Mbit/s	—	-90	—	dBm
	12 Mbit/s	—	-89	—	dBm
	18 Mbit/s	—	-87	—	dBm
	14 Mbit/s	—	-85	—	dBm
	36 Mbit/s	—	-81	—	dBm
	48 Mbit/s	—	-77	—	dBm
	54 Mbit/s	—	-75	—	dBm
Receiver sensitivity 802.11n HT20[1]	MCS0	—	-90	—	dBm
	MCS1	—	-87	—	dBm
	MCS2	—	-85	—	dBm
	MCS3	—	-82	—	dBm
	MCS4	—	-79	—	dBm
	MCS5	—	-75	—	dBm
	MCS6	—	-73	—	dBm
	MCS7	—	-71	—	dBm
Receiver sensitivity 802.11n HT40[1]	MCS0	—	-86	—	dBm
	MCS1	—	-85	—	dBm
	MCS2	—	-82	—	dBm
	MCS3	—	-79	—	dBm
	MCS4	—	-76	—	dBm
	MCS5	—	-72	—	dBm
	MCS6	—	-70	—	dBm
	MCS7	—	-69	—	dBm
Receiver maximum input level 802.11	802.11a 6-36 Mbit/s	—	0	—	dBm
	802.11a 48-54 Mbit/s	—	-5	—	dBm
	MCS0-4	—	-1	—	dBm
	MCS5	—	-5	—	dBm
	MCS6	—	-6	—	dBm
	MCS7	—	-9	—	dBm

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Table 34. 5 GHz Wi-Fi receive performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Receiver adjacent channel interference rejection (ACI) 802.11a	6 Mbit/s	—	30	—	dB
	9 Mbit/s	—	28	—	dB
	12 Mbit/s	—	28	—	dB
	18 Mbit/s	—	26	—	dB
	24 Mbit/s	—	23	—	dB
	36 Mbit/s	—	19	—	dB
	48 Mbit/s	—	16	—	dB
	54 Mbit/s	—	15	—	dB
Receiver adjacent channel interference rejection (ACI) 802.11n HT20	MCS0	—	28	—	dB
	MCS1	—	25	—	dB
	MCS2	—	22	—	dB
	MCS3	—	22	—	dB
	MCS4	—	17	—	dB
	MCS5	—	14	—	dB
	MCS6	—	12	—	dB
	MCS7	—	10	—	dB
Receiver adjacent channel interference rejection (ACI) 802.11n HT40	MCS0	—	29	—	dB
	MCS1	—	27	—	dB
	MCS2	—	24	—	dB
	MCS3	—	24	—	dB
	MCS4	—	19	—	dB
	MCS5	—	17	—	dB
	MCS6	—	14	—	dB
	MCS7	—	12	—	dB

[1] With BCC waveform

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10.3.4 2.4 GHz Wi-Fi transmit performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.*

Table 35. 2.4 GHz Wi-Fi transmit performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	—	2484	MHz
Transmit I/Q suppression with IQ calibration	I/Q suppression at chip output	—	-45	—	dBc
Transmit power (EVM and mask compliant) 20 MHz	802.11b	—	21	—	dBm
	OFDM BPSK	—	19	—	dBm
	OFDM QPSK	—	19	—	dBm
	OFDM 16-QAM	—	19	—	dBm
	OFDM 64-QAM	—	19	—	dBm
Transmit power (EVM and mask compliant) 40 MHz	OFDM BPSK	—	19	—	dBm
	OFDM QPSK	—	19	—	dBm
	OFDM 16-QAM	—	18	—	dBm
	OFDM 64-QAM	—	18	—	dBm
Transmit output power level control range	—	—	21[1]	—	dB
Transmit output power control step	—	—	1	—	dB
Transmit output power accuracy	—	—	1.5	—	dB
Transmit carrier suppression	802.11n MCS7 HT40, at 17 dBm	—	46	—	dB

[1] 0-21 dBm. For 802.11b data rates, TX power range is 8-21 dBm

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10.3.5 5 GHz Wi-Fi transmit performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.*

Table 36. 5 GHz Wi-Fi transmit performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	5 GHz—IEEE 802.11n/a	5150	–	5850	MHz
Transmit I/Q suppression with IQ calibration	I/Q suppression at chip output	–	-45	–	dBc
Transmit power (EVM and mask compliant) 20 MHz	OFDM BPSK	–	20	–	dBm
	OFDM QPSK	–	20	–	dBm
	OFDM 16-QAM	–	20	–	dBm
	OFDM 64-QAM	–	19	–	dBm
Transmit power (EVM and mask compliant) 40 MHz	OFDM BPSK	–	19	–	dBm
	OFDM QPSK	–	19	–	dBm
	OFDM 16-QAM	–	19	–	dBm
	OFDM 64-QAM	–	18	–	dBm
Transmit output power level control range	–	–	20[1]	–	dB
Transmit output power control step	–	–	1	–	dB
Transmit output power accuracy	–	–	1.5	–	dB
Transmit carrier suppression	802.11n MCS7 HT40, at 16 dBm	–	51	–	dB

[1] 0-20 dBm

10.3.6 Local oscillator

Table 37. Local oscillator

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Phase noise	Measured at 2.438 GHz at 100 kHz offset	–	-103	–	dBc/Hz
	Measured at 5.501 GHz at 100 kHz offset	–	-100	–	dBc/Hz
Integrated RMS phase noise at RF output (from 10 kHz–10 MHz)	Reference clock frequency = 26 MHz (2.4 GHz)	–	0.35	–	degrees
	Reference clock frequency = 26 MHz (5 GHz)	–	0.65	–	degrees
Frequency resolution	–	0.02	–	–	kHz

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10.4 Bluetooth radio specifications

The Bluetooth radio interface pin is powered by AVDD18 voltage supply.

10.4.1 Bluetooth/Bluetooth LE receive performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 38. Bluetooth/Bluetooth LE receive performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
Input IP3 (@ maximum gain of 72 dB)	—	—	-19	—	dBm
Out-of-band blocking	30–2000 MHz	—	-12.5	—	dBm
	2–2.399 GHz	—	-12.4	—	dBm
	2.484–3 GHz	—	-18	—	dBm
	3–12.75 GHz	—	-2.6	—	dBm
RSSI Range	Resolution = 1 dB	—	-90	0	dBm
Sensitivity[1] (RCV/CA/01/C, RCV/CA/02/C, RCV/CA/07/C)	DH5	—	-97	—	dBm
	2DH5	—	-96	—	dBm
	3DH5	—	-89.5	—	dBm
Bluetooth LE sensitivity [1] [2] (RFPHY/RCV/BV-01-C, RFPHY/RCV/BV-08-C, RFPHY/RCV/BV-26-C, RFPHY/RCV/BV-27-C)	LE 1 Mbit/s	—	-98	—	dBm
	LE 2 Mbit/s	—	-96	—	dBm
	LE coded 500 kbit/s (S = 2)	—	-100	—	dBm
	LE coded 125 kbit/s (S = 8)	—	-106	—	dBm

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Table 38. Bluetooth/Bluetooth LE receive performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
C/I performance (RCV/CA/03/C & RCV/CA/09/C)[3]	DH1- Co-Channel interference, C/I co-channel	—	10	—	dB
	DH1- Adjacent (1 MHz) interference, C/I 1 MHz	—	-9	—	dB
	DH1- Adjacent (2 MHz) interference, C/I 2 MHz	—	-45	—	dB
	DH1- Adjacent (2 MHz) interference, C/I >= 3 MHz	—	-52	—	dB
	DH1- Image frequency interference, C/I image channel	—	-29	—	dB
	DH1- Adjacent (1 MHz) interference to in-band mirror frequency, C/I image ± 1 MHz	—	-44	—	dB
	2DHx- Co-channel interference, C/I co-channel	—	9	—	dB
	2DHx- Adjacent (1 MHz) interference, C/I 1 MHz	—	-11	—	dB
	2DHx- Adjacent (2 MHz) interference, C/I 2 MHz	—	-45	—	dB
	2DHx- Adjacent (2 MHz) interference, C/I >= 3 MHz	—	-50	—	dB
	2DHx- Image frequency interference, C/I image channel	—	-29	—	dB
	2DHx- Adjacent (1 MHz) interference to in-band mirror frequency, C/I image ± 1 MHz	—	-45	—	dB
	3DHx- Co-channel interference, C/I co-channel	—	15	—	dB
	3DHx- Adjacent (1 MHz) interference, C/I 1 MHz	—	-7	—	dB
	3DHx- Adjacent (2 MHz) interference, C/I 2 MHz	—	-39	—	dB
	3DHx- Adjacent (2 MHz) interference, C/I >= 3 MHz	—	-44	—	dB
	3DHx- Image frequency interference, C/I image channel	—	-23	—	dB
	3DHx- Adjacent (1 MHz) interference to in-band mirror frequency, C/I image ± 1 MHz	—	-38	—	dB

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Table 38. Bluetooth/Bluetooth LE receive performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
C/I performance (RCV/BV/03/C, RCV/BV/09/C, RCV/BV/28/C and RDC/BV/29/C)	LE 1 Mbit/s - Co-channel interference, C/I co-channel	—	8.5	—	dB
	LE 1 Mbit/s- Adjacent (1 MHz) interference, C/I 1 MHz	—	-5	—	dB
	LE 1 Mbit/s- Adjacent (2 MHz) interference, C/I 2 MHz	—	-42	—	dB
	LE 1 Mbit/s- Adjacent (2 MHz) interference, C/I >= 3 MHz	—	-50	—	dB
	LE 1 Mbit/s- Image frequency interference, C/I image channel	—	-30.5	—	dB
	LE 1 Mbit/s- Adjacent (1 MHz) interference to in-band mirror frequency, C/I image ± 1 MHz	—	-38.5	—	dB
	LE 2 Mbit/s- Co-channel interference, C/I co-channel	—	6	—	dB
	LE 2 Mbit/s- Adjacent (2 MHz) interference, C/I 2 MHz	—	-24.5	—	dB
	LE 2 Mbit/s- Adjacent (4 MHz) interference, C/I 4 MHz	—	-51	—	dB
	LE 2 Mbit/s- Adjacent (6 MHz) interference, C/I >= 6 MHz	—	-52.5	—	dB
	LE 2 Mbit/s- Image frequency Interference C/I image channel	—	-30	—	dB
	LE 2 Mbit/s- Adjacent (2 MHz) interference to in-band mirror frequency, C/I image ± 2 MHz	—	-37	—	dB
	LE coded 500 kbit/s (S = 2)- Co-channel interference, C/I co-channel	—	7.5	—	dB
	LE coded 500 kbit/s (S = 2)- Adjacent (1 MHz) interference, C/I 1 MHz	—	-8	—	dB
	LE coded 500 kbit/s (S = 2)- Adjacent (2 MHz) interference, C/I 2 MHz	—	-47.5	—	dB
	LE coded 500 kbit/s (S = 2)- Adjacent (2 MHz) interference, C/I > = 3 MHz	—	-55.5	—	dB
	LE coded 500 kbit/s (S = 2)- Image frequency interference, C/I image channel	—	-32	—	dB

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Table 38. Bluetooth/Bluetooth LE receive performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
C/I performance (RCV/CA/09/C) (continued)	LE coded 500 kbit/s (S = 2)- Adjacent (1 MHz) interference to in-band mirror frequency, C/I image ± 1 MHz	—	-41	—	dB
	LE coded 125 kbit/s (S = 8)- Co-channel interference, C/I co channel	—	7	—	dB
	LE coded 125 kbit/s (S = 8)- Adjacent (1 MHz) interference, C/I 1 MHz	—	-9	—	dB
	LE coded 125 kbit/s (S = 8)- Adjacent (2 MHz) interference, C/I 2 MHz	—	-51	—	dB
	LE coded 125 kbit/s (S = 8)- Adjacent (3 MHz) interference, C/I >= 3 MHz	—	-61	—	dB
	LE coded 125 kbit/s (S = 8)- Image frequency Interference, C/I image channel	—	-33	—	dB
	LE coded 125 kbit/s (S = 8)- Adjacent (1 MHz) interference to in-band mirror frequency, C/I image ± 1 MHz	—	-42	—	dB

[1] De-rated at 2418 MHz, 2444 MHz and 2470 MHz. Compliant with BT SIG requirements.
[2] Measured with packet length of 255 bytes and TX impairments set to Dirty TX ON, following Bluetooth RF test specifications.
[3] Primary/reference channels: 2405 MHz, 2441 MHz, and 2477 MHz. Average value across the three channels.

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10.4.2 Bluetooth/Bluetooth LE transmit performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 39. Bluetooth/Bluetooth LE transmit performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
Output power	Class 1 without external PA—BDR	—	13	—	dBm
	Class 1 without external PA—EDR	—	10	—	dBm
Gain range	Class 1 without external PA	—	30	—	dB
Gain resolution	—	—	0.5	—	dB
Spurious emission (BDR) (in-band)	±500 kHz	—	-20	—	dBc
	±2 MHz	—	-33	—	dBm
	±3 MHz	—	-45	—	dBm
Spurious emission (EDR) (in-band)	±1 MHz	—	-26	—	dBc
	±2 MHz	—	-29	—	dBm
	±3 MHz	—	-40	—	dBm
Spurious emission (out-of-band)	30–88 MHz	—	-65	-41.25	dBm
	88–960 MHz	—	-65	-41.25	
	0.96–20 GHz All frequencies in this range < -41.25 dBm, except at 2x Bluetooth channel frequency. Measured at pin without external filter.	—	-23	-18	
	Restricted—2.38–2.39 GHz	—	-55	-41.25	
	Restricted—2.4835–2.6 GHz	—	-50	-41.25	
Out-of-band/ Cellular band noise	GSM850 (869–894 MHz)	—	-140	—	dBm/Hz
	GSM900 (925–960 MHz)	—	-140	—	
	GSM DCS (1805–1880 MHz)	—	-135	—	
	GSM PCS (1930–1990 MHz)	—	-135	—	
	GPS (1575.42 ±1.023 MHz)	—	-140	—	
	WCDMA Band I (2110–2170 MHz)	—	-130	—	
	WCDMA Band V (869–894 MHz)	—	-140	—	

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Table 39. Bluetooth/Bluetooth LE transmit performance...*continued*

Parameter	Conditions	Min	Typ	Max	Unit
Bluetooth classic					
Transmit output power (TRM/CA/01/C)	BDR	—	13	—	dBm
	EDR	—	10	—	dBm
Power control (TRM/CA/03/C)[1]	—	—	3 to 6.4	—	dB
Frequency range (TRM/CA/04/C)	Low range	—	2401	—	MHz
	High range	—	2481	—	MHz
-20 dB bandwidth (TRM/CA/05/C)	DH5 packets	—	957	—	kHz
Modulation characteristics (TRM/CA/07/C)	Delta F1 avg	—	166	—	kHz
	Delta F2 max threshold	—	100	—	%
	Delta F2/Delta F1	—	0.9	—	—
	Delta F2 avg	—	149	—	kHz
Initial carrier frequency tolerance (ICTF) test (TRM/CA/08/C)	DH1 packets	—	-11	—	kHz
Carrier frequency drift (TRM/CA/09/C)	Max Drift - DH1	—	-16	—	kHz
	Drift rate - DH1	—	±1.5[2]	—	kHz
	Max Drift - DH3	—	-17	—	kHz
	Drift rate - DH3	—	-2[3]	—	kHz
	Max drift - DH5	—	-16	—	kHz
	Drift rate - DH5	—	±2[4]	—	kHz
EDR relative power (TRM/CA/10/C)	2DH5 (DPSK/GFSK)	—	-0.2	—	dB
	3DH5 (DPSK/GFSK)	—	-0.2	—	dB
EDR carrier frequency stability and modulation accuracy (TRM/CA/11/C)	2DH5 peak DEVM	—	0.14	—	%
	2DH5 RMS DEVM	—	0.05	—	%
	3DH5 Peak DEVM	—	0.16	—	%
	3DH5 RMS DEVM	—	0.06	—	%
Diff. phase encoding (TRM/CA/12/C)	2DH5	—	100	—	%
	3DH5	—	100	—	%

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Table 39. Bluetooth/Bluetooth LE transmit performance...*continued*

Parameter	Conditions	Min	Typ	Max	Unit
Bluetooth LE					
Bluetooth LE output power (TRM/-LE/CA/01/C)	LE 1 Mbit/s	—	12	—	dBm
	LE 2 Mbit/s	—	12	—	dBm
	LE coded 500 kbit/s (S = 2)	—	12	—	dBm
	LE coded 125 kbit/s (S = 8)	—	12	—	dBm
Bluetooth LE modulation characteristics (TRM-LE/CA/05/C)	Delta F1 avg - LE 1 Mbit/s	—	253	—	kHz
	Delta F2/Delta F1- LE 1 Mbit/s	—	1	—	—
	Delta F2 avg- LE 1 Mbit/s	—	223	—	kHz
	Delta F1 avg - LE 2 Mbit/s	—	505	—	kHz
	Delta F2/Delta F1- LE 2 Mbit/s	—	1	—	—
	Delta F2 avg- LE 2 Mbit/s	—	460	—	kHz
Bluetooth LE carrier frequency drift (TRM-LE/CA/06/C)	Max drift - LE 1 Mbit/s	—	-9	—	kHz
	Drift rate - LE 1 Mbit/s	—	1	—	kHz
	Max drift - LE 2 Mbit/s	—	-12	—	kHz
	Drift rate - LE 2 Mbit/s	—	1	—	kHz
	Max drift - LE coded 500 kbit/s (S = 2)	—	-6	—	kHz
	Drift rate - LE coded 500 kbit/s (S = 2)	—	-5	—	kHz
	Max Drift - LE coded 125 kbit/s (S = 8)	—	-6	—	kHz
	Drift rate - LE coded 125 kbit/s (S = 8)	—	-5	—	kHz
Frequency accuracy (TRM-LE/CA/BV-06-C)	LE 1 Mbit/s	—	-15	—	kHz
	LE 2 Mbit/s	—	-15	—	kHz
	LE coded 500 kbit/s (S = 2)	—	-15	—	kHz
	LE coded 125 kbit/s (S = 8)	—	-15	—	kHz

[1] Specifies the minimum and maximum transmit power step size. As per Bluetooth SIG specification, min step size = 2 dB and max step size = 8 dB
[2] As per Bluetooth SIG specification, the lower limit is -20 kHz and the upper limit is +20 kHz.
[3] Calculated over 50 us - Bluetooth SIG specification.
[4] As per Bluetooth SIG specification, the lower limit is -40 kHz and the upper limit is +40 kHz.

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10.5 External coexistence interface specifications

10.5.1 WCI-2 coexistence interface specifications

10.5.1.1 WCI-2 interface

WCI-2 is a simplified 2-wire UART interface defined in Bluetooth Core Spec Vol 7 Part C.

Figure 14 shows UART waveform.

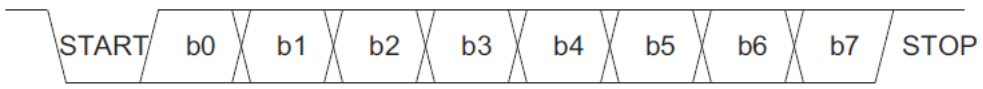

Figure 14. UART waveform

Figure 15 illustrates WCI-2 hardware coexistence interface between IW416 and the external radio.

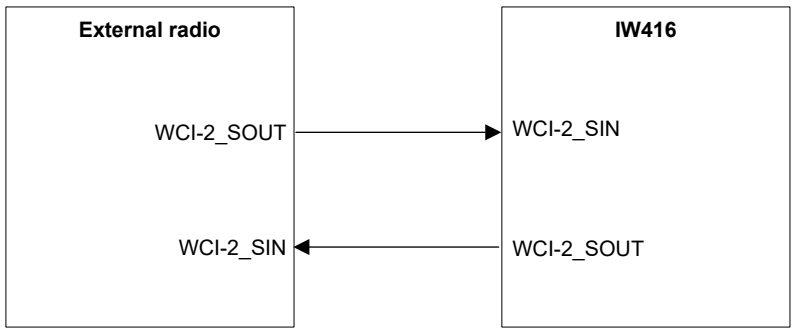

Figure 15. WCI-2 coexistence interface

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10.5.1.2 WCI-2 messages

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for request and grant, where:

- The real time message from the external radio to IW416 indicates the request to operate (Figure 16)
  - MWS_RX=1 indicates an external radio request to RX
  - MWS_TX=1 indicates an external radio request to TX

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	FRAME_SYNC	MWS_RX	MWS_TX	MWS_PATTERN[0]	MWS_PATTERN[1]

Figure 16. Type 0: Real time signaling message - external radio to IW416

- The external radio can send an optional second message following the real time message to indicate the traffic priority using the vendor specific message (Figure 17). Otherwise, the priority is set via a BCA register.

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	1	1	0	MWS_TX_PRI[0]	MWS_TX_PRI[1]	MWS_RX_PRI[0]	MWS_RX_PRI[1]

Figure 17. Type 7: Vendor specific message - external radio to IW416

- The real time message from IW416 to the external radio indicates the arbitration results (Figure 18):
  - BT_RX_Pri = 1: the Bluetooth radio RX wins the arbitration and is in operation
  - BT_TX_On = 1: the Bluetooth radio TX wins the arbitration and is in operation
  - 802_RX_Pri = 1: Wi-Fi RX wins the arbitration and is in operation
  - 802_TX_On = 1: Wi-Fi TX wins the arbitration and is in operation
  - Otherwise, the external radio is granted

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	BT_RX_PRI	BT_TX_ON	802_RX_PRI	802_TX_ON	RFU

Figure 18. Type 0: Real time signaling message - IW416 to external radio

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WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for other purposes, such as:

- Transport control message from IW416 to the external radio to request real time message upon wake up (Figure 19)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	1	Resend_real_time	RFU	RFU	RFU	RFU

Figure 19. Type 1: Transport control message time signaling message - IW416 to external radio

- MWS inactivity duration message from the external radio to IW416 indicates the inactivity duration to IW416 before going to sleep (Figure 20)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	1	1	Duration[0]	Duration[1]	Duration[2]	Duration[3]	Duration[4]

Figure 20. MWS inactivity duration message

- MWS scan frequency message from the external radio to IW416 indicates the external radio scan frequency to IW416 (Figure 21)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	0	0	Freq[0]	Freq[1]	Freq[2]	Freq[3]	Freq[4]

Figure 21. Type 5: MWS scan frequency message

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10.5.1.3 WCI-2 signal waveform format

The messaging is based on a standard UART format.

Figure 22 shows the waveform for the transmit signal (UART_SOUT to UART_SIN).

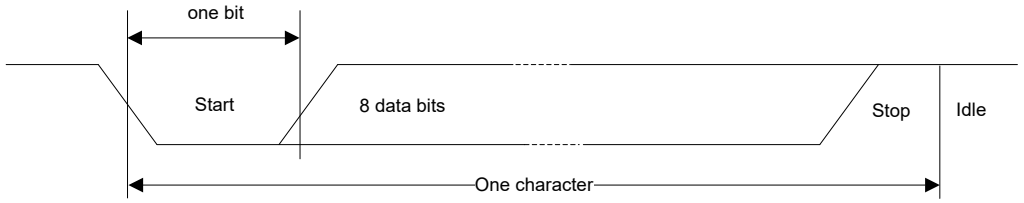

Figure 22. WCI-2 transmit signal waveform

Table 40. WCI-2 interface transport settings

Parameter	Range	Note
Baud rate	921600 ~ 4000000	Baud
Data bits	8	LSB first
Parity bits	0	No parity
Stop bit	1	One stop bit
Flow control	No	No flow control

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10.5.2 PTA interface coexistence specifications

This section illustrates how the central hardware packet traffic arbiter samples the interface signals. The sampling is based on which interface signals are being used.

Figure 23 shows PTA coexistence interface signal timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority ready at Request signal assertion
- Output: grant

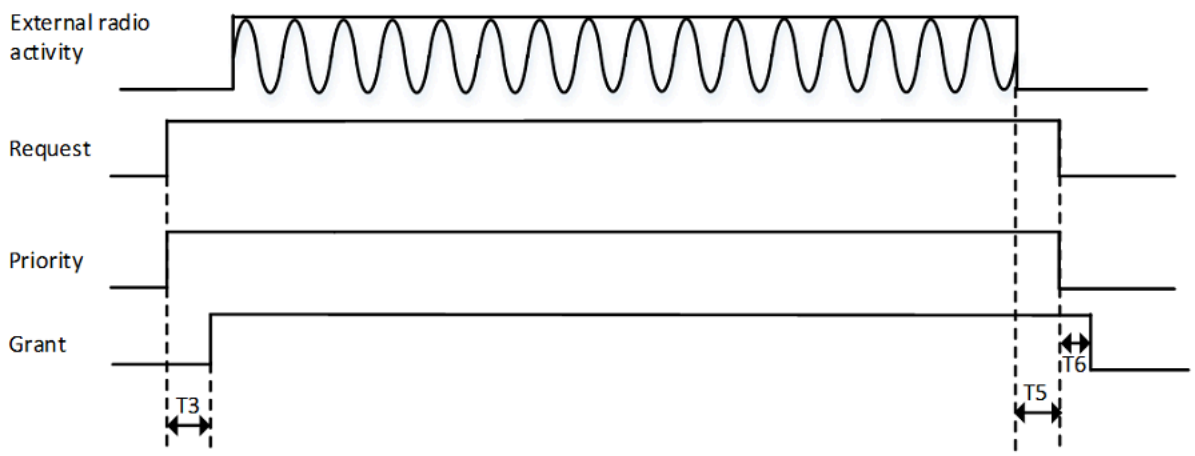

Figure 23. PTA coexistence interface timing diagram - Example 1

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Figure 24 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, state
  - Priority signal and State signal are ready at Request signal assertion
- Output: grant

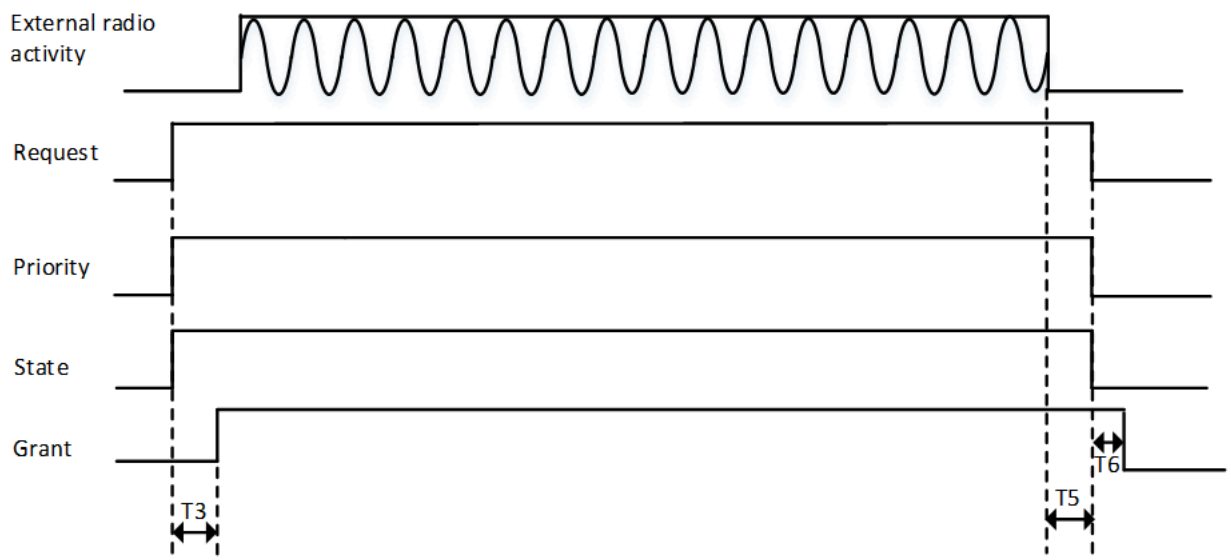

Figure 24. PTA coexistence interface timing diagram - Example 2

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Figure 25 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, frequency, state
  - Priority, State, and Frequency ready at Request assertion
- Output: grant

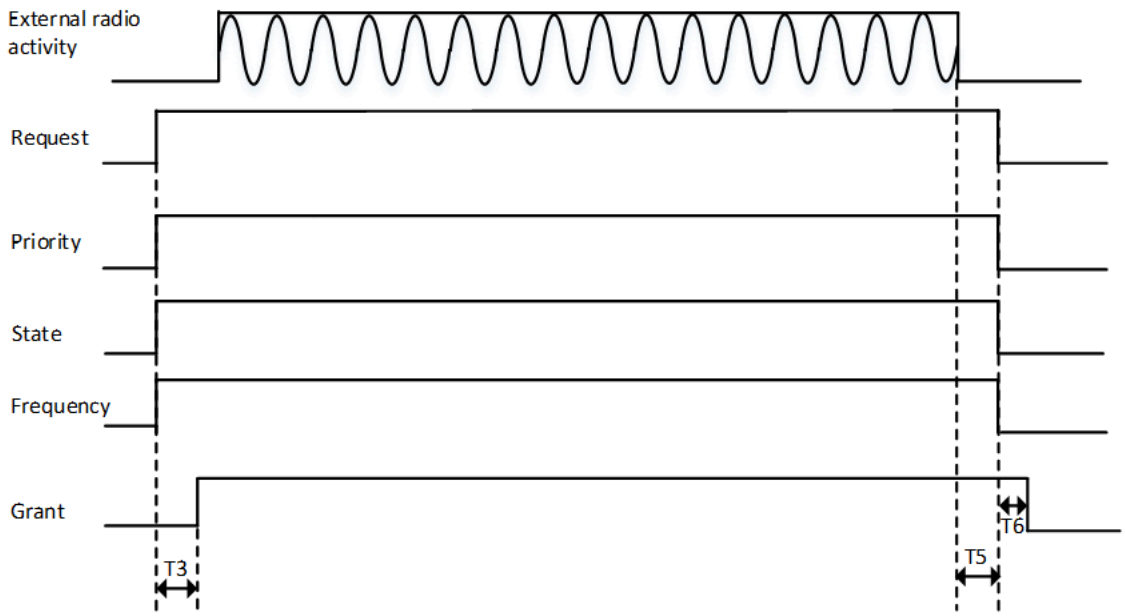

Figure 25. PTA coexistence interface timing diagram - Example 3

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Figure 26 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority signal is ready at Request signal assertion
- Output: grant
  - Grant signal is de-asserted before Request signal de-assertion due to a traffic abort caused by other traffic with higher priority

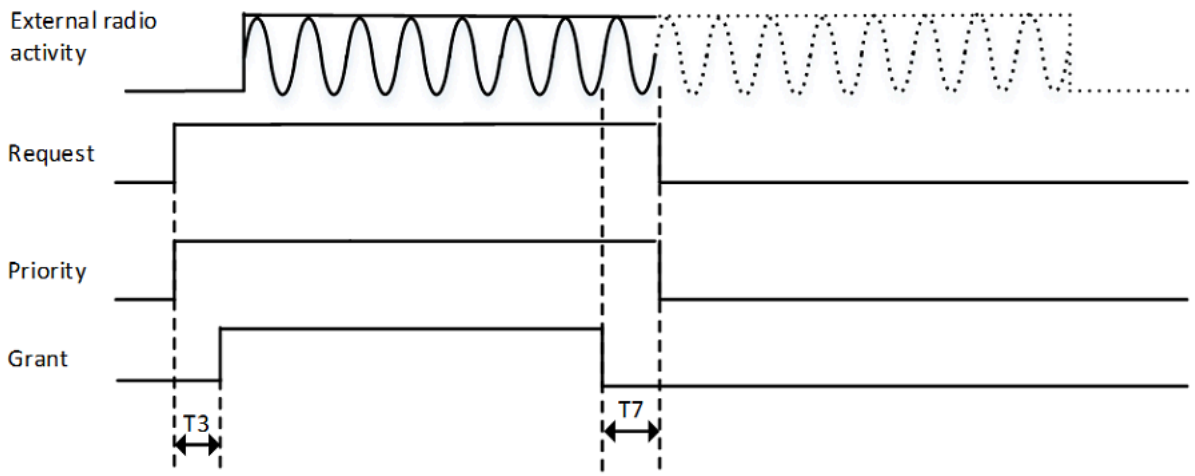

Figure 26. PTA coexistence interface timing diagram - Example 4

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Figure 27 shows PTA coexistence interface timing diagram for the example where:

- Input: request and priority
  - Priority pin is sampled three times to obtain two priority bits and TX/RX info. No input from State pin.
- Output: grant

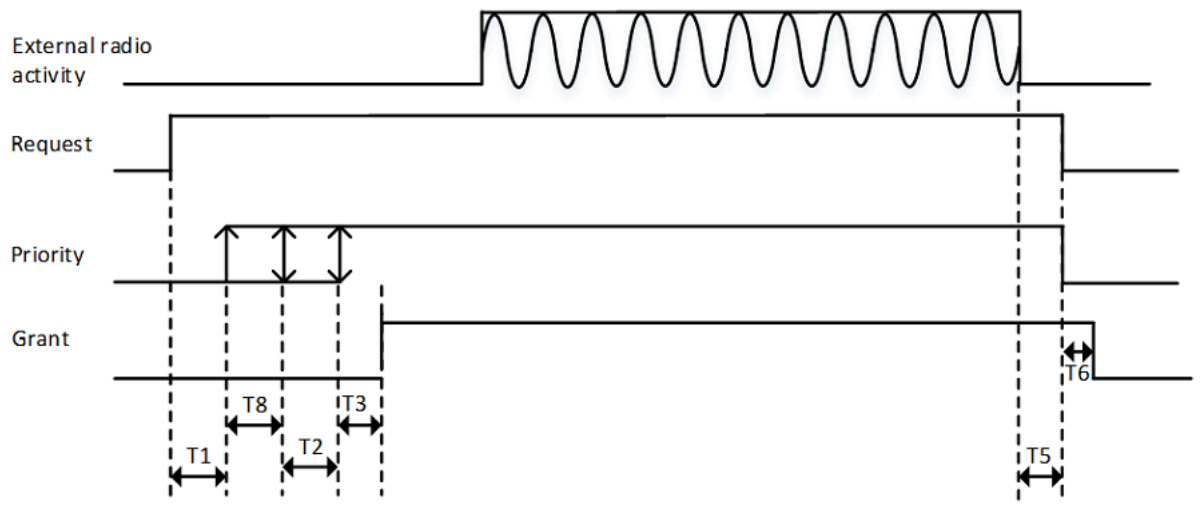

Figure 27. PTA coexistence interface timing diagram - Example 5

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Table 41 provides the timing specifications for PTA coexistence interface signals.

Table 41. PTA coexistence interface signal timing data

Paramete	Conditions	Min	Typ.	Max	Unit
T1[1]	Priority[0] is sampled on Priority pin at T1 from Request assertion.	0	—	100	µs
T8[1]	Optional: priority[1], if present on Priority pin, is sampled at T1+T8 from Request assertion.	0.025	—	100	µs
T2[1]	Optional: TX/RX Info, if present on Priority pin, is sampled at T1+T2 (one priority bit on Priority pin) or T1+T8+T2 (two priority bits on Priority pin) from Request assertion.	0.025	—	100	µs
T3[2]	Time from all information available to BCA to grant decision ready	0.1	—	0.4	µs
T5[2]	The Request signal de-asserts T5 after the last symbol is done	—	—	—	µs
T6[2]	The Grant signal de-asserts T6 after the Request de-assertion	0.1	—	0.3	µs
T7[2]	The Request signal de-asserts T7 after the grant de-assertion due to a traffic abort.	—	—	—	µs

[1] Valid for serially sampled Priority pin
[2] Valid for all implementations

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10.6 Current consumption

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and typical value.*

Table 42. Current consumption values

Mode	Conditions	VPA	AVDD18	VCORE	VIO (3.3 V)	Unit
Sleep mode						
Power down	—	0.003	0.04	0.4	0	mA
Wi-Fi and Bluetooth in deep-sleep mode	—	0.005	0.025	0.44	0.03	mA
Bluetooth LE [1]						
Bluetooth LE advertise	Interval = 1.28 s	0.005	0.06	0.28	0.03	mA
Bluetooth LE scan	Interval = 1.28 s, window = 11.25 ms	0.005	0.14	0.4	0.03	mA
Bluetooth LE link	Master mode, interval=1.28 s	0.005	0.145	0.49	0.03	mA
Bluetooth LE peak transmit	@ 0 dBm, 1 Mbit/s	0.005	27	19	0.24	mA
Bluetooth LE peak transmit	@ 4 dBm, 1 Mbit/s	0.005	31	19	0.24	mA
Bluetooth LE peak transmit	@ 7 dBm, 1 Mbit/s	0.005	50	19	0.24	mA
Bluetooth LE peak transmit	@ 10 dBm, 1 Mbit/s	0.005	66	19	0.24	mA
Bluetooth LE peak receive	1 Mbit/s	0.005	16	20	0.24	mA
Bluetooth[1]						
Bluetooth page scan	--	0.005	0.19	0.46	0.03	mA
Bluetooth page and inquiry scan	--	0.005	0.3	0.6	0.03	mA
Bluetooth ACL link	Master sniff mode interval=1.28s	0.005	0.12	0.4	0.03	mA
Bluetooth ACL link	Master sniff mode interval = 500 ms	0.005	0.24	0.64	0.03	mA
Bluetooth ACL	Data pump, DH1	0.005	11.8	13.1	0.24	mA
Bluetooth ACL	Data pump, 2-DH3	0.005	19.2	15.4	0.24	mA
Bluetooth ACL	Data pump, 3-DH5	0.005	21.6	16.1	0.24	mA
Bluetooth SCO HV3 peak transmit	@ 0 dBm	0.005	26	19	0.24	mA
Bluetooth SCO HV3 peak transmit	@ 4 dBm	0.005	31	19	0.24	mA
Bluetooth SCO HV3 peak transmit	@ 10 dBm	0.005	67	19	0.24	mA
Bluetooth SCO HV3 peak transmit	@ 13 dBm	0.005	88	19	0.24	mA
Bluetooth SCO HV3 peak receive	--	0.005	15.5	20	0.24	mA
Bluetooth peak transmit	@ 0 dBm, DH5	0.005	26	19	0.24	mA
Bluetooth peak transmit	@ 4 dBm, DH5	0.005	31	19	0.24	mA
Bluetooth peak transmit	@ 10 dBm, DH5	0.005	67	19	0.24	mA
Bluetooth peak transmit	@ 13 dBm, DH5	0.005	88	19	0.24	mA
Bluetooth peak receive	DH5	0.005	15.5	20	0.24	mA

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Table 42. Current consumption values...*continued*

Mode	Conditions	VPA	AVDD18	VCORE	VIO (3.3 V)	Unit
IEEE power save[2]						
IEEE-PS_2GHz-Legacy (DTIM-1)	Beacon interval : 100 msec 5G basic rate for beacon TX: 6 Mbit/s 2G basic rate for beacon TX: 1 Mbit/s	0.005	0.94	1.18	0.03	mA
IEEE-PS_2GHz-Legacy (DTIM-3)		0.005	0.33	0.7	0.03	mA
IEEE-PS_2GHz-Legacy (DTIM-5)		0.005	0.21	0.59	0.03	mA
IEEE-PS_2GHz-Legacy (DTIM-10)		0.005	0.17	0.55	0.03	mA
IEEE-PS_5GHz-Legacy (DTIM-1)		0.005	0.75	0.91	0.03	mA
IEEE-PS_5GHz-Legacy (DTIM-3)		0.005	0.26	0.62	0.03	mA
IEEE-PS_5GHz-Legacy (DTIM-5)		0.005	0.19	0.55	0.03	mA
IEEE-PS_5GHz-Legacy (DTIM-10)		0.005	0.12	0.52	0.03	mA
Wi-Fi 2.4 GHz receive idle mode[2]						
802.11b, 11 Mbit/s	—	0.005	40	26	0.24	mA
802.11g, 54 Mbit/s	—	0.005	40	26	0.24	mA
802.11n, 20 MHz MCS7	—	0.005	40	26	0.24	mA
802.11n, 40 MHz MCS7	—	0.005	40	34	0.24	mA
Wi-Fi 5 GHz receive idle mode[2]						
802.11a, 54 Mbit/s	—	0.005	60	27	0.24	mA
802.11n, 20 MHz	—	0.005	60	27	0.24	mA
802.11n, 40 MHz	—	0.005	72	35	0.24	mA
Wi-Fi 2.4 GHz receive mode[2]						
802.11b, 11 Mbit/s	—	0.005	33	27	0.24	mA
802.11g, 54 Mbit/s	—	0.005	37	38	0.24	mA
802.11n, 20 MHz MCS7	—	0.005	35	47	0.24	mA
802.11n, 40 MHz MCS7	—	0.005	36	60	0.24	mA
Wi-Fi 5 GHz receive mode[2]						
802.11a, 54 Mbit/s	—	0.005	50	39	0.24	mA
802.11n, 20 MHz MCS7	—	0.005	50	48	0.24	mA
802.11n, 40 MHz MCS7	—	0.005	60	60	0.24	mA
Wi-Fi 2.4 GHz transmit mode[2] (TX referred to pin)						
802.11b, 1 Mbit/s @ 20 dBm	—	313	95	88	0.24	mA
802.11b, 11 Mbit/s @ 20 dBm	—	323	95	90	0.24	mA
802.11g, 54 Mbit/s @ 20 dBm	—	311	96	95	0.24	mA
802.11n, 20 MHz MCS0 @ 20 dBm	—	311	96	98	0.24	mA
802.11n, 20 MHz MCS7 @ 20 dBm	—	311	96	98	0.24	mA
802.11n, 40 MHz MCS0 @ 20 dBm	—	325	97	105	0.24	mA
802.11n, 40 MHz MCS7 @ 20 dBm	—	325	97	105	0.24	mA

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Table 42. Current consumption values...*continued*

Mode	Conditions	VPA	AVDD18	VCORE	VIO (3.3 V)	Unit
Wi-Fi 5 GHz transmit mode[2] (TX referred to pin)						
802.11a, 6 Mbit/s @ 19 dBm	—	274	158	99	0.24	mA
802.11a, 54 Mbit/s @ 19 dBm	—	278	157	103	0.24	mA
802.11n, 20 MHz MCS0 @ 19 dBm	—	272	158	100	0.24	mA
802.11n, 20 MHz MCS7 @ 19 dBm	—	280	158	102	0.24	mA
802.11n, 40 MHz MCS0 @ 17 dBm	—	227	155	105	0.24	mA
802.11n, 40 MHz MCS7 @ 17 dBm	—	227	157	115	0.24	mA
Peak current						
Peak current during device initialization	--	862	224	141	0.24	mA

[1] Wi-Fi in deep-sleep mode
[2] Bluetooth in deep-sleep mode

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10.7 SDIO host interface specifications

The SDIO host interface pins are powered by VIO_SD voltage supply.

See Section 10.7.1 "VIO_SD DC characteristics" for specifications.

The SDIO electrical specifications are identical for 4-bit SDIO and 1-bit SDIO transfer modes.

10.7.1 VIO_SD DC characteristics

Table 43. VIO_SD requirements

SDIO version	Specifications	Maximum frequency	VIO_SD value
SDIO 2.0	Default speed	25 MHz	3.3 V
	High speed	50 MHz	3.3 V
SDIO 3.0	SDR12	25 MHz	1.8 V
	SDR25	50 MHz	1.8 V
	SDR50	100 MHz	1.8 V
	DDR50	50 MHz	1.8 V

10.7.1.1 1.8V operation

Table 44. DC electrical characteristics—1.8V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	–	0.7*VIO_SD	–	VIO_SD+0.4	V
V_{IL}	Input low voltage	–	-0.4	–	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	–	100	–	–	mV
V_{OH}	Output high voltage	–	VIO_SD-0.4	–	–	V
V_{OL}	Output low voltage	–	–	–	0.4	V

10.7.1.2 3.3V operation

Table 45. DC electrical characteristics—3.3V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	–	0.7*VIO_SD	–	VIO_SD+0.4	V
V_{IL}	Input low voltage	–	-0.4	–	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	–	100	–	–	mV
V_{OH}	Output high voltage	–	VIO_SD-0.4	–	–	V
V_{OL}	Output low voltage	–	–	–	0.4	V

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10.7.2 Default speed, high-speed modes

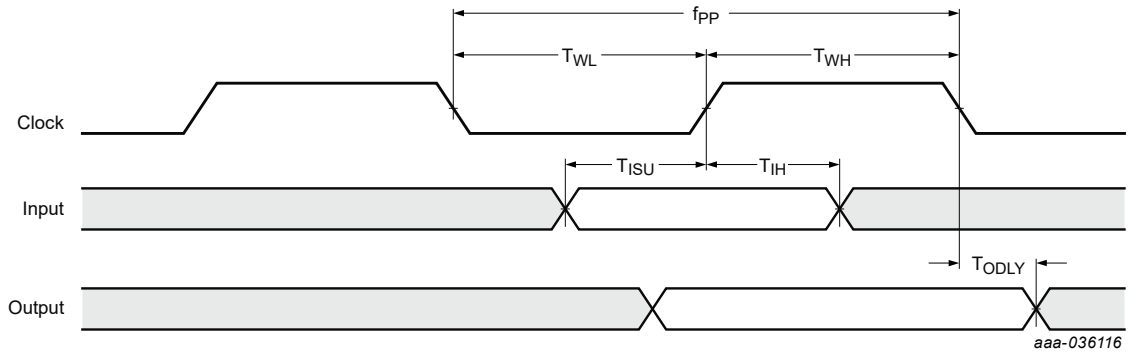

Figure 28. SDIO protocol timing diagram—Default speed mode

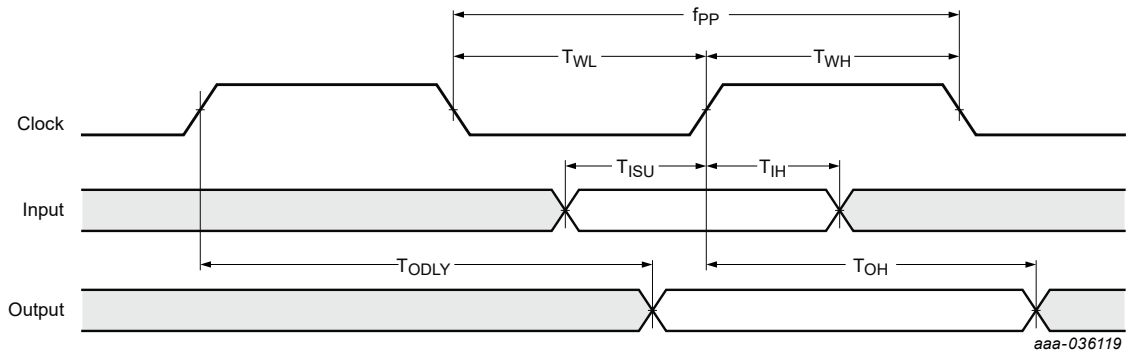

Figure 29. SDIO protocol timing diagram—High-speed mode

Table 46. SDIO timing data—Default speed, high-speed modes

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	–	25	MHz
		High-speed	0	–	50	MHz
T_{WL}	Clock low time	Normal	10	–	–	ns
		High-speed	7	–	–	ns
T_{WH}	Clock high time	Normal	10	–	–	ns
		High-speed	7	–	–	ns
T_{ISU}	Input setup time	Normal	5	–	–	ns
		High-speed	6	–	–	ns
T_{IH}	Input hold time	Normal	5	–	–	ns
		High-speed	2	–	–	ns
T_{ODLY}	Output delay time	Normal	–	–	14	ns
	CL ≤ 40 pF (1 card)	High-speed	–	–	14	ns

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Table 46. SDIO timing data—Default speed, high-speed modes*...continued*

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{OH}	Output hold time	High-speed	2.5	–	–	ns

10.7.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

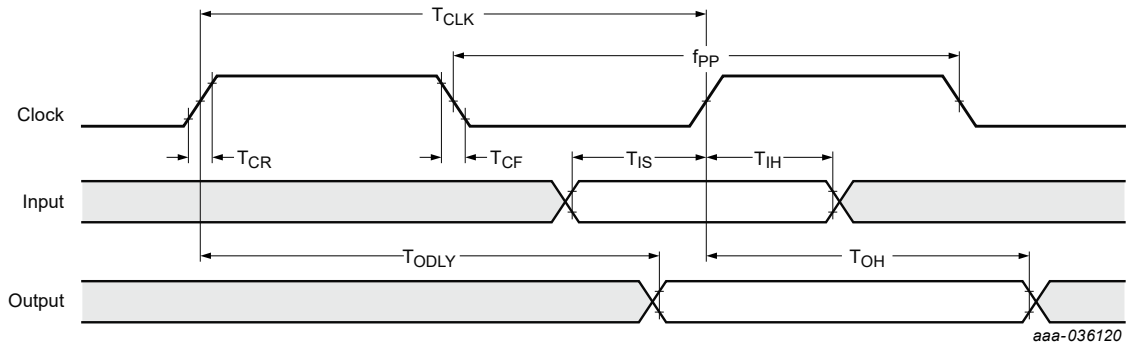

Figure 30. SDIO protocol timing diagram—SDR12, SDR25, SDR50 modes (up to 100MHz) (1.8V)

Table 47. SDIO timing data——SDR12, SDR25, SDR50 modes (up to 100MHz) (1.8V)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR12/25/50	25	–	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	–	–	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	–	–	ns
T_{CLK}	Clock time	SDR12/25/50	10	–	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	–	–	$0.2*T_{CLK}$	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25/50	–	–	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	–	–	ns

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10.7.4 DDR50 mode (50MHz) (1.8V)

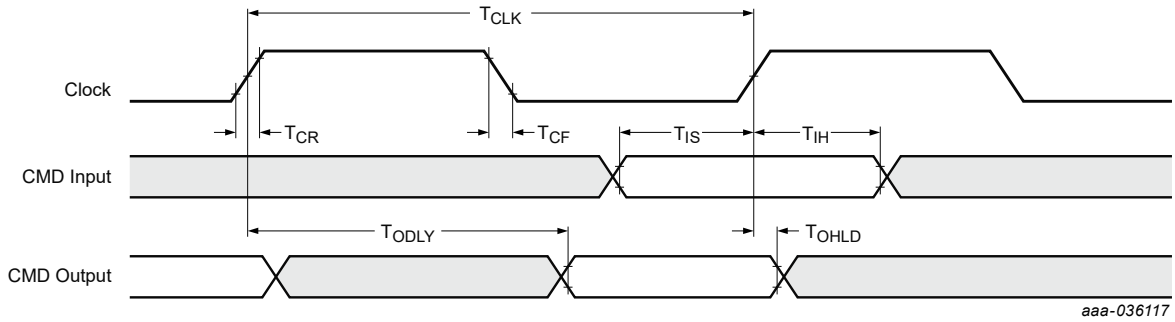

Figure 31. SDIO CMD timing diagram—DDR50 mode (50MHz)

In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

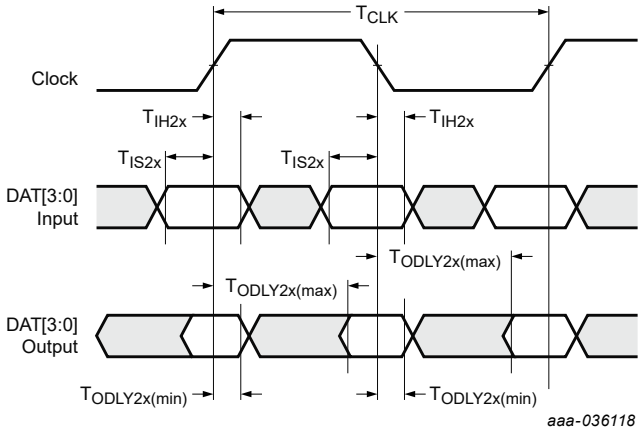

Figure 32. SDIO DAT[3:0] timing diagram—DDR50mode

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Table 48. SDIO timing data—DDR50 mode (50MHz)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	–	–	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	–	–	0.2*T_{CLK}	ns
Clock Duty	–	DDR50	45	–	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	–	–	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	–	–	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	–	–	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	–	–	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	–	–	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	–	–	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	–	–	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	–	–	ns

10.7.5 SDIO internal pull-up/pull-down specifications

Table 49. SDIO internal pull-up/pull-down specifications

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance	–	60	90	120	kΩ

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10.8 High-speed UART specifications

The UART TX and RX pins are powered by VIO voltage supply.

See Section 10.1.1 "VIO DC characteristics" for DC specifications.

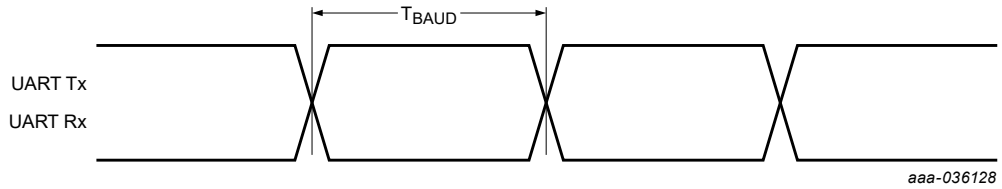

Figure 33. UART timing diagram

Table 50. UART timing data [1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26 MHz or 40 MHz reference clock	250	–	–	ns

[1] The acceptable deviation from the UART RX target baud rate is ±3%.

10.9 Audio interface specifications

The device has two audio interfaces: I2S interface and PCM interface.

10.9.1 I2S interface specifications

The I2S pins are powered by VIO voltage supply. See Section 10.1.1 "VIO DC characteristics" for the specifications.

10.9.2 PCM interface specifications

The PCM pins are powered by VIO voltage supply. See Section 10.1.1 "VIO DC characteristics" for specifications.

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Central mode

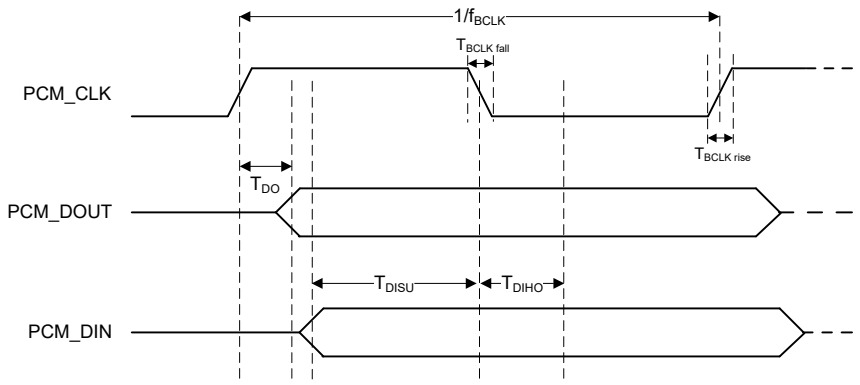

Figure 34. PCM timing specification diagram for data signals—central mode

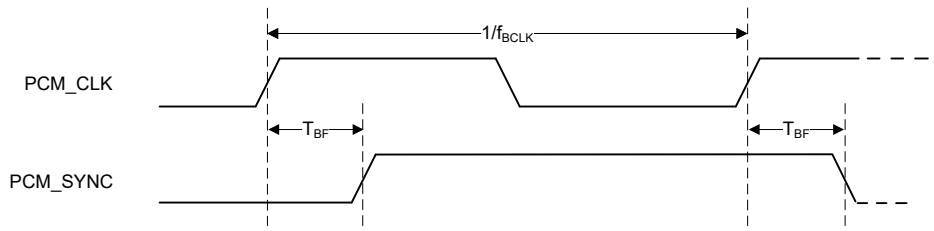

Figure 35. PCM timing specification diagram for PCM_SYNC signal—central mode

Table 51. PCM timing specification data—central mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	–	2	2/2.048	2.048	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	–	0.4	0.5	0.6	–
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	–	–	3	–	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	–	–	–	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	–	20	–	–	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	–	15	–	–	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	–	–	–	15	ns

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Peripheral mode

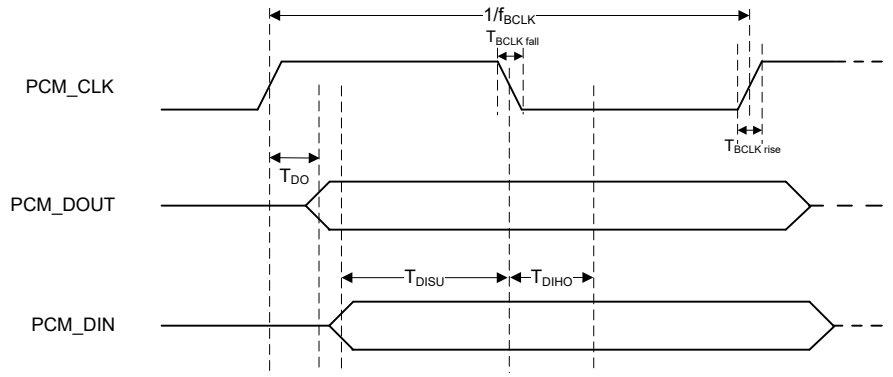

Figure 36. PCM timing specification diagram for data signals—peripheral mode

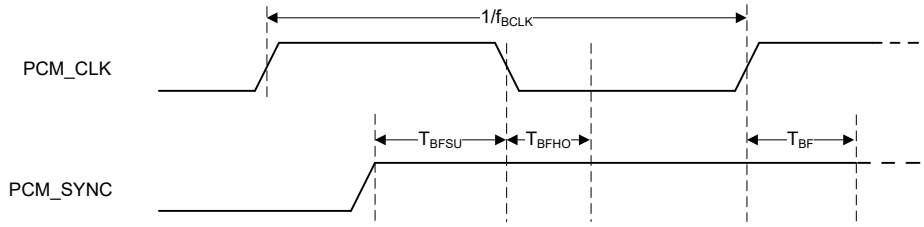

Figure 37. PCM timing specification diagram for PCM_SYNC signal—peripheral mode

Table 52. PCM timing specification data—peripheral mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	–	0.512	2/2.048	4	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	–	0.4	0.5	0.6	–
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	–	–	3	–	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	–	–	–	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	–	15	–	–	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	–	10	–	–	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	–	15	–	–	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	–	10	–	–	ns

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10.10 Reference clock specifications

10.10.1 External crystal oscillator specifications

Note: *The reference clock from the external crystal oscillator requires a CMOS input signal.*

Table 53. Clock DC specifications [1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Single-ended high-level voltage	–	–	–	1.8	V
Single-ended low-level voltage	–	0	–	–	V
Clock amplitude (pk-pk)	–	0.5	–	1	V
Mid-point slope	–	125	–	–	MV/s

[1] AC-coupling capacitor is integrated into the SoC.

Table 54. 26 MHz clock timing

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO26 period	–	38.46 - 20 ppm	38.46	38.46 + 20 ppm	ns
XO26 rise time	–	–	–	5.00	ns
XO26 fall time	–	–	–	5.00	ns
XO26 duty cycle	–	48.05	50	51.95	%

Table 55. 40 MHz clock timing

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO40 period	–	25.00 - 20 ppm	25.00	25.00 + 20 ppm	ns
XO40 rise time	–	–	–	2.00	ns
XO40 fall time	–	–	–	2.00	ns
XO40 duty cycle	–	47	50	53	%

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Table 56. Phase noise—2.4 GHz operation

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	–	–	-126	dBc/Hz
	Offset = 10 kHz	–	–	-137	dBc/Hz
	Offset = 100 kHz	–	–	-145	dBc/Hz
	Offset > 1 MHz	–	–	-145	dBc/Hz
Fref = 40 MHz	Offset = 1 kHz	–	–	-126	dBc/Hz
	Offset = 10 kHz	–	–	-137	dBc/Hz
	Offset = 100 kHz	–	–	-145	dBc/Hz
	Offset > 1 MHz	–	–	-145	dBc/Hz

Table 57. Phase noise—5 GHz operation

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	–	–	-130	dBc/Hz
	Offset = 10 kHz	–	–	-150	dBc/Hz
	Offset = 100 kHz	–	–	-156	dBc/Hz
	Offset > 1 MHz	–	–	-156	dBc/Hz
Fref = 40 MHz	Offset = 1 kHz	–	–	-130	dBc/Hz
	Offset = 10 kHz	–	–	-150	dBc/Hz
	Offset = 100 kHz	–	–	-156	dBc/Hz
	Offset > 1 MHz	–	–	-156	dBc/Hz

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10.10.2 External crystal specifications

Table 58. External crystal specifications

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fundamental frequencies	—	—	26 (40)	—	MHz
Resonance mode	—	—	A1, Fundamental	—	—
Equivalent differential load capacitance	—	—	8	—	pF
Shunt capacitance	—	—	2	—	pF
Frequency tolerance	Over process at 25ºC	—	±10	—	ppm
Frequency stability	Over operating temperature	—	±10	—	ppm
Aging	—	—	±2	—	ppm/5 years
Series resistance (ESR)	26 MHz	—	—	60	Ω
	40 MHz	—	—	60	Ω
Insulation resistance	at DC 100V	500	—	—	MΩ
Drive level	—	150	—	—	µW

10.10.3 External sleep clock specifications

Table 59. External sleep clock specifications [1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Min	Typ	Max	Unit
Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)	–	32.768	–	kHz
Phase noise requirement (@ 100 kHz)	–	-125	–	dBc/Hz
Cycle jitter	–	1.5	–	ns (RMS)
Slew rate limit (10-90%)	–	–	100	ns
Duty cycle tolerance	20	–	80	%

[1] Voltage input level = 1.8V. See Section 10.1.1 "VIO DC characteristics".

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10.11 Power down (PDn) pin specifications

10.11.1 PDn asserted low—All power supplies good

Figure 38 and Table 60 show the specifications for the PDn signal when it is asserted (low) while all power supplies to the device are good.

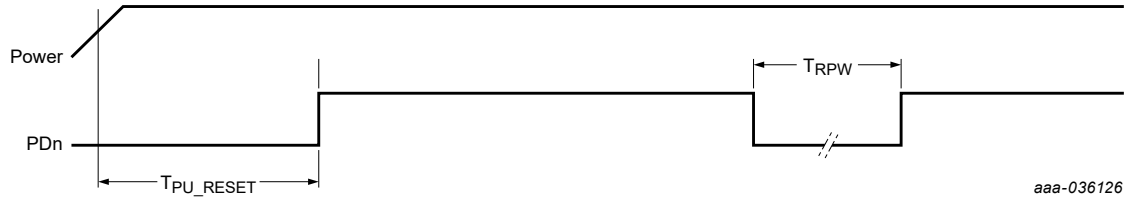

Figure 38. PDn pin (Power-down) timing—Power remains high at PDn assertion

Table 60. PDn pin (Power Down) specifications—Power remains high at PDn assertion

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	–	0	–	–	ms
T_{RPW}	PDn pulse width	–	50 [1]	–	–	µs
V_{IH}	Input high voltage	–	1.4	–	4.5	V
V_{IL}	Input low voltage	–	-0.4	–	0.5	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

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10.11.2 PDn asserted low—One or more power supplies ramp down

Figure 39 and Table 61 show the specifications for the PDn signal when it is asserted (low) while 1 or more of the power supplies (including VCORE) ramps down. When the integrated LDO is used, VCORE will ramp down when PDn is asserted.

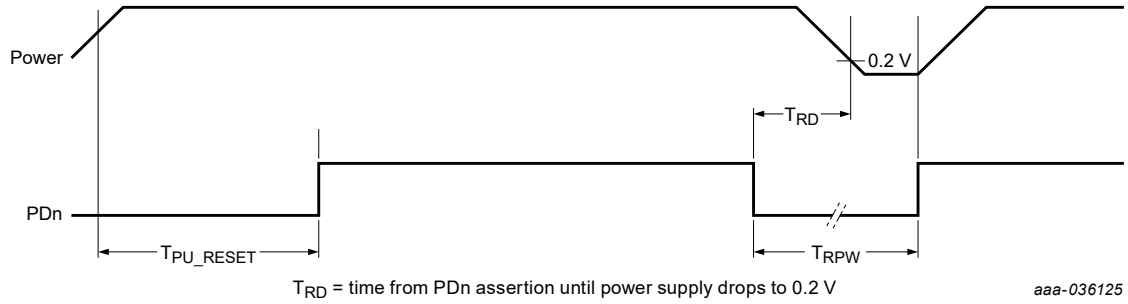

Figure 39. PDn pin (Power Down) timing—Power ramps down at PDn assertion

Table 61. PDn pin (Power Down) specifications—Power ramps down at PDn assertion

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	–	0	–	–	ms
T_{RPW}	PDn pulse width	–	T_{RD} [1]	–	–	µs
V_{IH}	Input high voltage	–	1.4	–	4.5	V
V_{IL}	Input low voltage	–	-0.4	–	0.5	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

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10.12 Configuration pin specifications

For a list of configuration pins, see Section 6.6 "Configuration pins".

Table 62. Configuration pin specifications [1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal weak pull-up resistance	Around 1 ms following any reset	–	800	–	kΩ
Internal nominal pull-up resistance	Around 1 ms following any reset	–	100	–	kΩ

[1] After approximately 1 ms, the configuration pins become functional pins.

10.13 JTAG interface specifications

JTAG interface pins are powered by VIO voltage supply.

See Section 10.1.1 "VIO DC characteristics" for specifications.

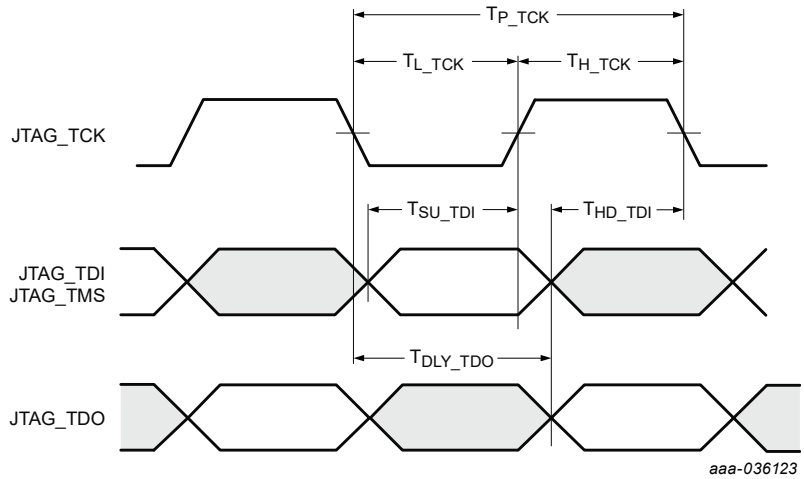

Figure 40. JTAG timing diagram

Table 63. JTAG timing data [1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_TCK}	TCK period	--	40	--	--	ns
T_{H_TCK}	TCK high	--	12	--	--	ns
T_{L_TCK}	TCK low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO delay	--	0	--	15	ns

[1] Does not apply to JTAG enabled by the JTAG_TMS pin.

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11 Package information

11.1 Package thermal conditions

11.1.1 HVQFN68 thermal conditions

Table 64. Package thermal conditions—HVQFN68

Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	28.4	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 1 meter/sec air flow	27.6	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 2 meter/sec air flow	26.1	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 3 meter/sec air flow	25.3	°C/W
ψ_{JT}	Thermal characteristic parameter Junction to top-center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top-center of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	0.44	°C/W
ψ_{JB}	Thermal characteristic parameter Junction to bottom surface, center of PCB. $\psi_{JB} = (T_J - T_B)/P$ T_B = surface temperature of PCB	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	15.4	°C/W
θ_{JC}	Thermal resistance Junction to case of the package. $\theta_{JC} = (T_J - T_C)/ P_{TOP}$ T_C = temperature on top-center of package P_{TOP} = power dissipation from top of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	13.0	°C/W
θ_{JB}	Thermal resistance Junction to board of package. $\theta_{JB} = (T_J - T_B)/ P_{BOTTOM}$ P_{BOTTOM} = power dissipation from bottom of package to PCB surface	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	15.6	°C/W

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11.1.2 WLCSP76 thermal conditions

Table 65. Package thermal conditions—WLCSP76

Symbol	Rating	Board type[1]	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance[2]	JESD51-9, 2s2p	37.6	°C/W
$R_{\psi JT}$	Junction to top of package thermal characterization parameter[2]	JESD51-9, 2s2p	1.3	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-9).

[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

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11.2 Package mechanical drawing

Table 66. Package information

Package name	Link to package information on NXP website
HVQFN68	SOT2107-1
WLCSP76	SOT2073-1

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11.2.1 HVQFN68 mechanical drawing

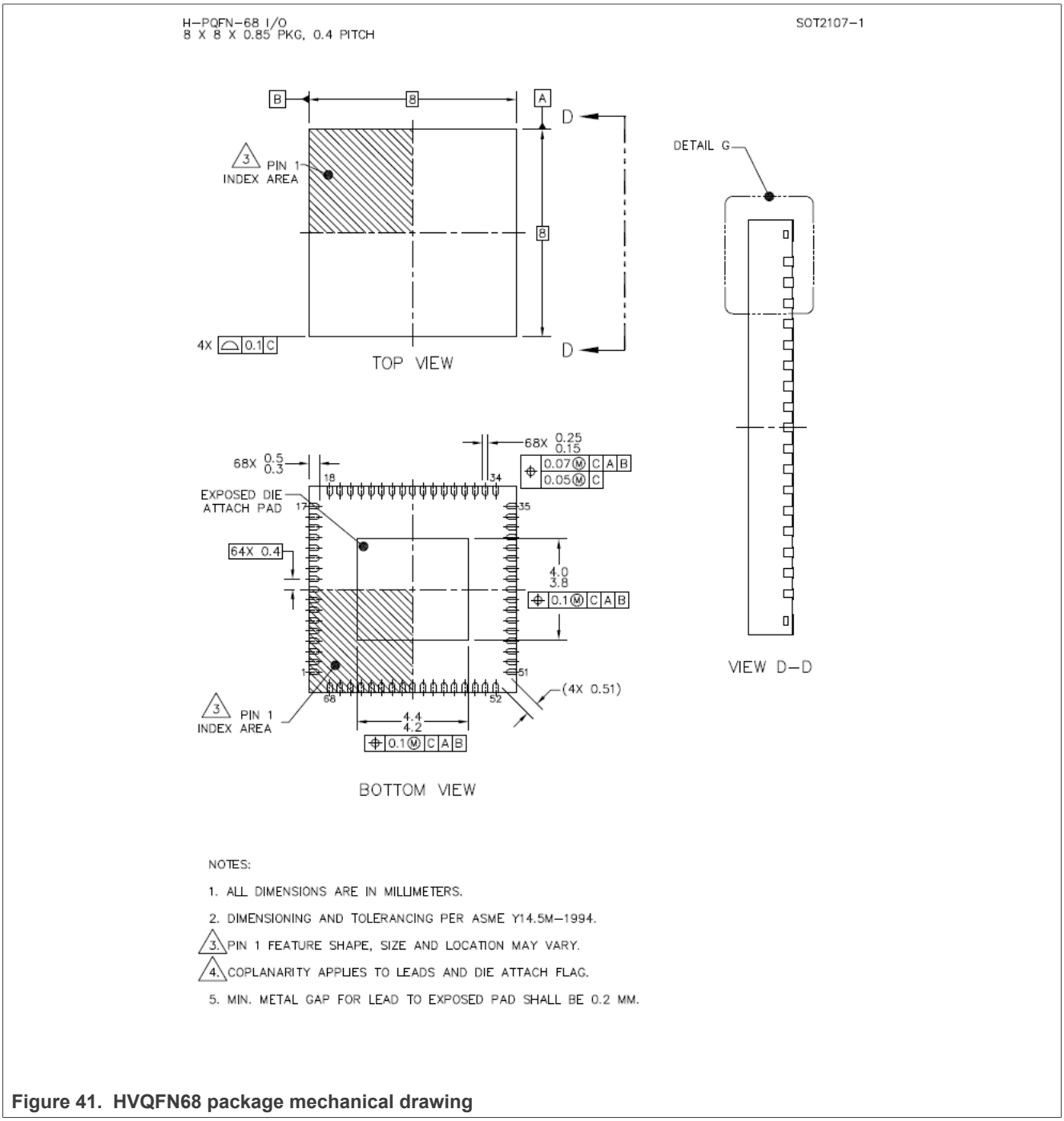

Figure 41. HVQFN68 package mechanical drawing

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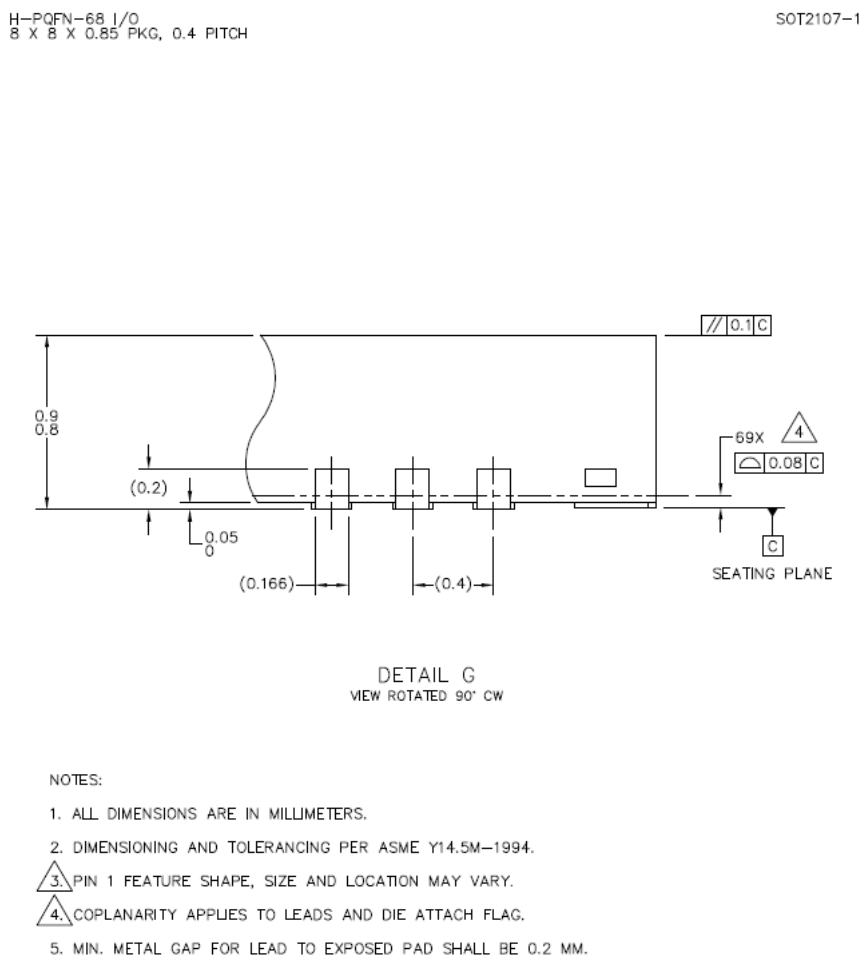

Figure 42. HVFQN68 package mechanical drawing - Detail G

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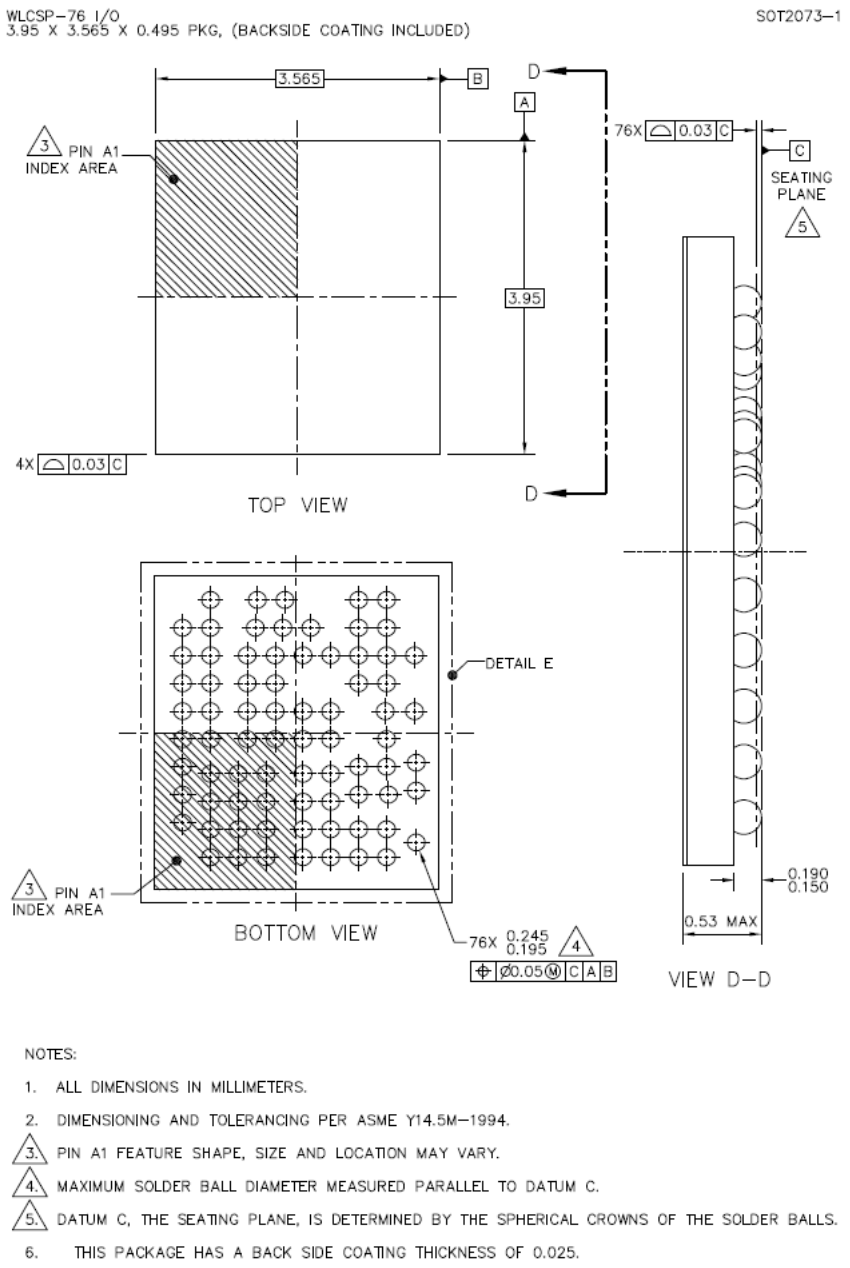
11.2.2 WLCSP76 mechanical drawing



Backside coating included

Figure 43. WLCSP76 package mechanical drawing

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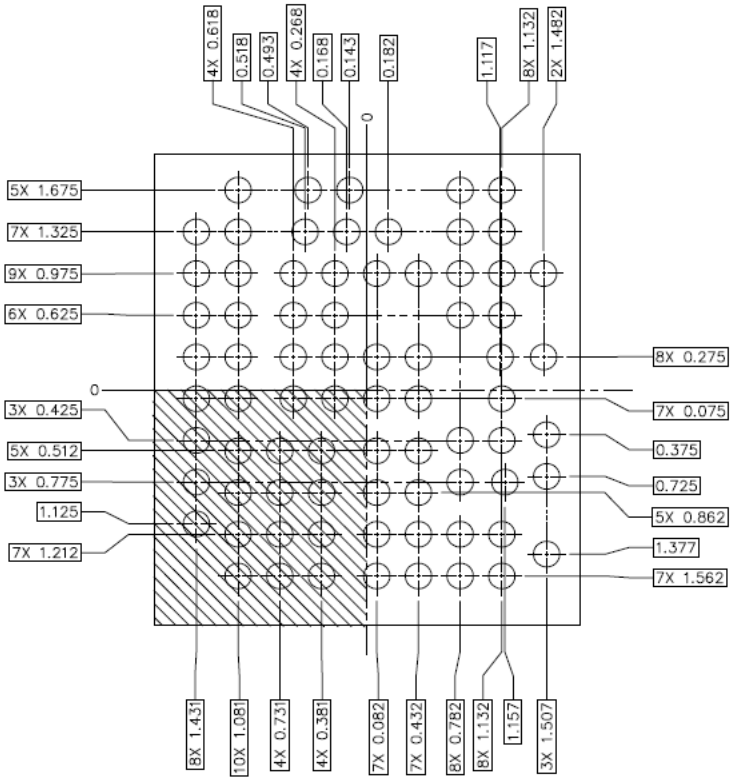

DETAIL E

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Backside coating included

Figure 44. WLCSP76 package mechanical drawing - Detail E

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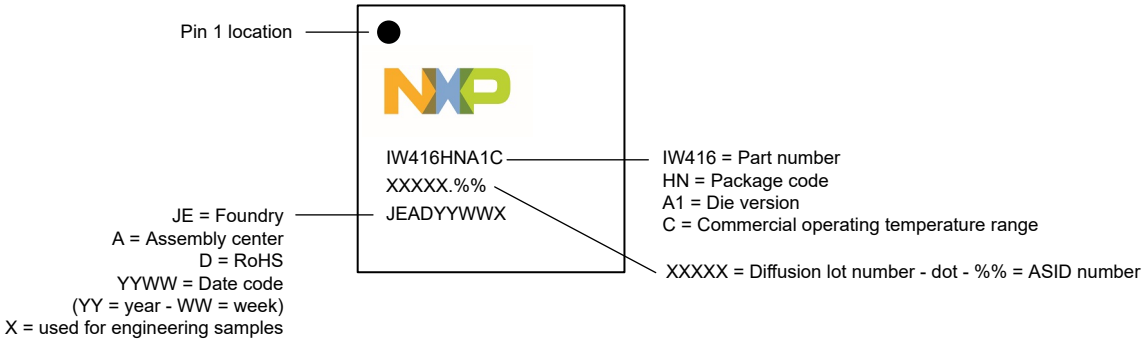
11.3 Package marking

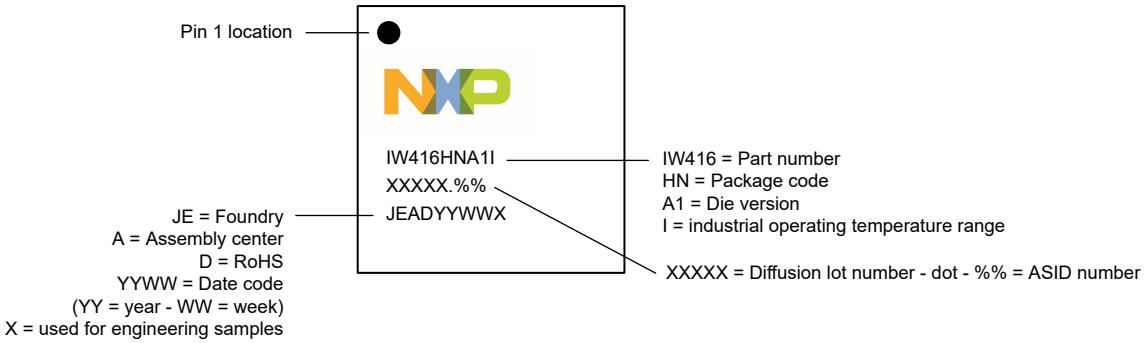
11.3.1 HVFQN68 marking

Figure 45 and Figure 46 show the location of pin 1 and describe each line of the package marking on HVQFN68.



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 45. Package marking and pin 1 location—HVQFN68, commercial operating temperature



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 46. Package marking and pin 1 location—HVQFN68, industrial operating temperature

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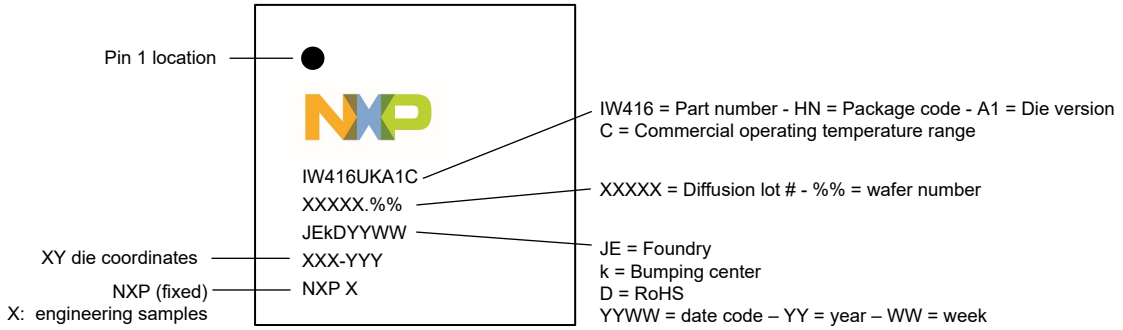
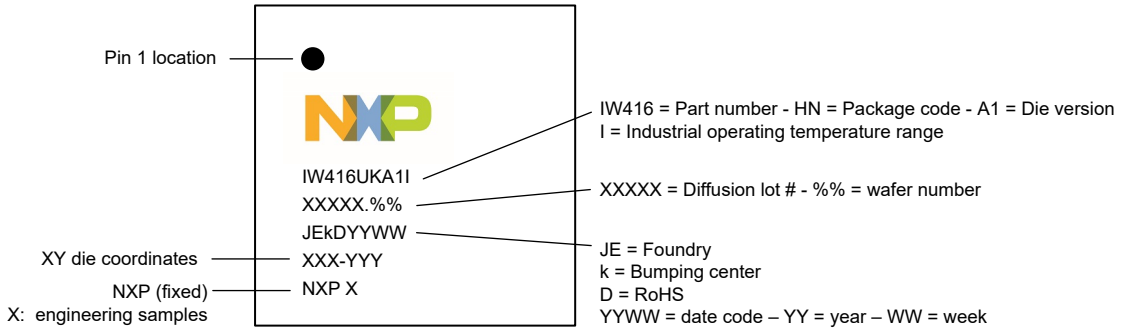
11.3.2 WLCSP76 marking

Figure 47 and Figure 48 show the location of pin 1 and describes each line of the package marking on the WLCSP76.



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 47. Package marking and pin 1 location—WLCSP76, commercial operating temperature range



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 48. Package marking and pin 1 location—WLCSP76, industrial operating temperature range

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12 Abbreviations

Table 67. Abbreviations

Abbreviation	Definition
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AFH	Adaptive frequency hopping
AGC	Automatic gain control
AP	Access point
Arm	Advanced RISC machine
BDR	Basic data rate
BRF	Bluetooth RF unit
CMD	Command
CRC	Cyclic redundancy check
CTS	Clear to send
DAC	Digital-to-analog converter
DCF	Distributed coordination function
DFS	Dynamic frequency selection
DMA	Direct memory access
DQPSK	Differential quadrature phase shift keying
DTIM	Delivery traffic indication message
FIFO	First in first out
GPIO	General purpose input/output
HT	High throughput
HVQFN	Thermal enhanced very thin quad flat package
HW	Hardware
I/Q	In-phase/quadrature
IEEE	Institute of electrical and electronics engineers
JEDEC	Joint electronic device engineering council
JTAG	Joint test action group
LE	Low energy
LED	Light emitting diode
LNA	Low noise amplifier
LSB	Least significant byte
LTE	Long term evolution
MAC	Media/medium access controller
MCS	Modulation and coding scheme
MFP	Multi functional pin

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Table 67. Abbreviations...*continued*

Abbreviation	Definition
MIMO	Multiple input multiple output
MPDU	MAC protocol data unit
MSB	Most significant byte
MU-MIMO	Multi user MIMO
MWS	Mobile wireless system Multimedia wireless system
OFDM	Orthogonal frequency division multiplexing
OTP	One time programmable
PA	Power amplifier
PCM	Pulse code modulation
PDn	Power down
PHY	Physical layer
POS	Point of sale
PSK	Pre shared keys
PTA	Packet traffic arbitration
QAM	Quadrature amplitude modulation
QFN	Quad flat non-leaded package
RF	Radio frequency
RIFS	Reduced inter frame space
RSSI	Receiver signal strength indication
RTC	Real time clock
RTS	Request to send
SISO	Single input single output
SoC	System-on-chip
STA	Station
TWT	Target wake-up time
UART	Universal asynchronous receiver/transmitter
WBS	Wide band speech
WCI-2	Wireless coexistence interface 2
WEP	Wired equivalent privacy
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless local area network
WLCSP	Wafer level chip scale package
WPA	Wi-Fi protected access
WPA2	Wi-Fi protected access 2
WPA2-PSK	Wi-Fi protected access 2 - pre shared key

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Table 67. Abbreviations*...continued*

Abbreviation	Definition
WPA3	Wi-Fi protected access 3
WPA-PSK	Wi-Fi protected access - pre shared key

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13 Revision history

Table 68. Revision history

Document ID	Release date	Description
IW416 v.8.0	24 September 2025	Product data sheet • Section 1 "Product overview" and document title: removed the Bluetooth version. • Section 3.4 "Wi-Fi radio": updated the list of supported channels (40 MHz). • Section 7.3 "Power-down sequence": updated. • Section 12 "Abbreviations": updated. • Section 13 "Revision history": changed the format.
IW416 v.7.0	5 September 2024	Product data sheet **Pin information** • Table 6 "Pin list by number - HVQFN68 package": removed the double entry for pin 5 (DNC). **Electrical specifications** • Section 10.10.2 "External crystal specifications": changed the typical value of "Equivalent differential load capacitance".
IW416 v.6.0	3 March 2023	Product data sheet **Product overview** • Section 1.2 "Wi-Fi key features": updated the description of PTA external coexistence interface • Section 1.3 "Bluetooth key features": . Updated the first item about Bluetooth version . Added a note to *AES security* **Bluetooth subsystem** • Section 4.1 "Bluetooth 2.4 GHz TX/RX": replaced *Bluetooth* with *Bluetooth 5.1 features* • Section 4.1 "Bluetooth 2.4 GHz TX/RX": added a note to *Encryption (AES) support* • Section 4.1 "Bluetooth 2.4 GHz TX/RX": added a note to *Encryption (AES) support* and *LE Secure Connection* **Coexistence** • Section 5 "Coexistence ": updated **Electrical specifications** • Section 10.5 "External coexistence interface specifications": added • Section 10.5.1 "WCI-2 coexistence interface specifications": added • Replaced the section *PTA coexistence interface specifications* with Section 10.5.2 "PTA interface coexistence specifications" • Section 10.4.1 "Bluetooth/Bluetooth LE receive performance": added the note [2] and updated the description of Bluetooth LE RX sensitivity parameter

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Table 68. Revision history...*continued*

Document ID	Release date	Description
IW416 v.5.0	15 December 2021	Product data sheet **Overall document** • Updated Bluetooth 5.1 to Bluetooth • Renamed PTA interface and WCI-2 interface as PTA coexistence interface and WCI-2 coexistence interface. Updated sections: – Section 5 "Coexistence " – Section 6.1 "Signal diagram" – Section 6.5.8 "PTA coexistence interface" – Section 6.5.9 "WCI-2 coexistence interface" – *PTA coexistence interface specifications* **Product overview** • Section 1 "Product overview": . First paragraph: replaced [In addition to classic Bluetooth features, the IW416 enables Bluetooth 5.1 capabilities including Low Energy (LE), LE long range and LE data up to 2 Mbit/s.] with [In addition to classic Bluetooth features, the IW416 enables Bluetooth capabilities including Low Energy (LE), LE long range, LE 2 Mbps, and Periodic Advertising Sync Transfer(PAST).] . Second paragraph: replaced [With the single-antenna configuration, simultaneous 5 GHz Wi-Fi and Bluetooth is supported and in the 2.4 GHz band, the single-antenna configuration allows arbitrated transmit and receive operation of Wi-Fi and Bluetooth.] with [With the single-antenna configuration, simultaneous 5 GHz Wi-Fi and Bluetooth is supported. In the 2.4 GHz band, the single-antenna configuration allows arbitrated transmit and receive operation of Wi-Fi and Bluetooth.] . Third paragraph: replaced [In addition, support for external radio co-existence (e.g. cellular) is provided through an external interface.] with [In addition, support for external radio co-existence is provided through an external interface.] • Section 1.2 "Wi-Fi key features": . Removed WEP and TKIP as these encryption methods are no longer supported. . Replaced [Interface to coexist with 802.15.4, LTE, or other radios] with [IEEE 802.15.2 PTA coexistence interface to coexist with 802.15.4, and other external radios] . Replaced [Security: WPA3, WPA2, WPA2 and WPA mixed mode] with [Security: WPA3, WPA2, WPA2-WPA mixed mode] • Section 1.5 "Operating characteristics": . Replaced [Supply voltage] with [Supply voltages] . Replaced [Operating temperature] with [Operating temperature ranges] • Section 1.6 "General features": replaced [WLCSP76 (76 terminals, 3.95 mm x 3.565 mm x 0.495 mm body)] with [WLCSP76 (76 terminals, 0.35 mm pitch, 3.95 mm x 3.565 mm x 0.495 mm body)] **Ordering information** • Table 2 "Part order codes": added [, with 0.35 mm pitch] to WLCSP76 package type (2 entries) ————*Continues*————

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Table 68. Revision history...*continued*

Document ID	Release date	Description
IW416 v.5.0	15 December 2021	————*Continued*———— **Wi-Fi subsystem** • Section 3.1 "IEEE 802.11 standards": added the note [(available through Host Supplicant)] to 802.11k, 802.11v, and 802.11r features • Section 3.2 "Wi-Fi MAC": . Replaced [Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses] with [Duplicate frame detection] . Removed [Packet drop scheme] . Removed [Multiple BSS/Station] . Removed [NXP mobile hotspot] • Section 3.4 "Wi-Fi radio": . In Wi-Fi RX path subsection: - Removed [Direct conversion architecture: no need for an external SAW filter] - Replaced [On-chip gain selectable LNA with optimized noise figure and power consumption] with [On-chip LNA with optimized noise figure and power consumption] . In Radio channel frequencies: - Renamed the caption of the first table as [Supported channels (20 MHz)] - Removed the duplicated rows (channel 128 to 165) - Added one row for channel 144 - 5845 MHz - Renamed the caption of the second table as [Supported channels (40 MHz)] - Added one row for channel pair 9-13 - 2462 MHz • Section 3.5 "Wi-Fi encryption": . Removed WEP and TKIP as these encryption methods are no longer supported. . Replaced [AES/CCMP as part of the 802.11i security standard (WPA2 and WPA mixed mode)] with [AES/CCMP as part of the 802.11i security standard (WPA3, WPA2, WPA2-WPA mixed mode)] **Bluetooth subsystem** • Section 4.1 "Bluetooth 2.4 GHz TX/RX": . Removed [Bluetooth-based indoor location with up to 16 antenna support] . Removed [Low Latency Reconnection (LLR) (future BT standard)] • Section 4.2 "Bluetooth Low Energy (LE)": . Replaced [2 Mbit/s LE] with [LE 2 Mbps] . Added [LE Long Range] , [Periodic Advertising Sync Transfer(PAST)], and [Advertising Channel Index] • Section 4.3 "Bluetooth host interfaces": . Replaced [High-Speed UART interface up to 4 Mbit/s] with [High-Speed UART interface up to 3 Mbit/s] • Section 4.4.2 "PCM interface": . Replaced [The PCM interface is used to exchange audio data between the host and the Bluetooth/ LE functional block.] with [The PCM interface is used to exchange audio data between the host and the Bluetooth functional block.] • Section *Coexistence*: . Replaced [Coexistence between internal Wi-Fi and Bluetooth radios and an external radio such as 802.15.4, LTE or 5G.] with [Coexistence between internal Wi-Fi and Bluetooth radios and an external radio such as 802.15.4.] ————*Continues*————

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Table 68. Revision history...*continued*

Document ID	Release date	Description
IW416 v.5.0	15 December 2021	————*Continued*———— **Pin information** • Section 6.5.2 "General purpose I/O (GPIO) (MFP)": rename [Host wake-up mode] as [Out-of-band mode] for GPIO[12] • Section 6.5.5 "SDIO host interface (MFP)": updated SD_CMD 1-bit mode definition • Section 6.5.7 "Audio interface": updated PCM and I2S signal descriptions **Power information** • Table 24 "Device power modes ": replaced [standby] with [standby/idle] • Section 7.6 "Reset": changed the value for PDn input pin to 0.5 V in the third bullet point **Absolute maximum ratings** • Table 27 "Limiting values": replaced [Limiting values (HVQFN68 package)] with [Limiting values] **Electrical specifications** • Section 10.3.2 "2.4 GHz Wi-Fi receive performance": updated RF frequency range maximum value to 2484 MHz • Section 10.3.4 "2.4 GHz Wi-Fi transmit performance": updated RF frequency range min and max values to 2400 MHz and 2484 MHz respectively • Section 10.3.5 "5 GHz Wi-Fi transmit performance": updated RF frequency range min and max values to 5150 MHz and 5850 MHz respectively • Section 10.4.1 "Bluetooth/Bluetooth LE receive performance": updated RF frequency range min and max values to 2400 MHz and 2483.5 MHz respectively • Section 10.4.2 "Bluetooth/Bluetooth LE transmit performance": . Updated RF frequency range min and max values to 2400 MHz and 2483.5 MHz respectively . Updated transmit output power (TRM/CA/01/C) typical value to 13 dBm (BDR), and 10 dBm (EDR) • Section 10.7.1 "VIO_SD DC characteristics": replaced [SDR50] with [DDR50] in the last table row • Section 10.6 "Current consumption" . Added the parameters and values for Wi-Fi 2.4 GHz receive idle mode . Added the parameters and values for Wi-Fi 5 GHz receive idle mode • : changed T_{BAUD} condition to [26 MHz or 40 MHz reference clock] • Section 10.9.2 "PCM interface specifications": – Figure 34 and Figure 36 : renamed T_{BCLK} as $1/F_{BCLK}$, added T_{BCLK} rise and T_{BCLK} fall – Table 51 and Table 52: added F_{BCLK} min and max values • Table 60 "PDn pin (Power Down) specifications—Power remains high at PDn assertion ": changed PDn pulse width minimum value to 50 us • Table 61 "PDn pin (Power Down) specifications—Power ramps down at PDn assertion ": changed V_{IL} maximum value to 0.5 V

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Table 68. Revision history...*continued*

Document ID	Release date	Description
IW416 v.4.0	25 June 2021	Product data sheet **Product overview** • Figure 1 "Application block diagram ": Added a reference to IW416 design guide • Section 1.5 "Operating characteristics": Removed "3.3 V (optional)" **Pin information** • Section 6.5.12 "Power supply and ground": Added a note to AVDD33 description **Electrical specifications** • Section 10.6 "Current consumption": added the values for VIO (3.3 V) • Table 43 "VIO_SD requirements": added **Package information** • Table 66 "Package information": added
IW416 v.3.0	12 March 2021	Preliminary data sheet **Product overview** • Section 1 "Product overview": updated • Section 1.2 "Wi-Fi key features": updated • Section 1.3 "Bluetooth key features": updated • Section 1.4 "Host interfaces": updated **Ordering information** • Figure 3 "Part numbering scheme": updated • Table 2 "Part order codes": updated **Wi-Fi subsystem** • Section 3.1 "IEEE 802.11 standards": updated • Section 3.3 "Wi-Fi baseband": updated • Section 3.6 "Wi-Fi host interfaces": updated **Bluetooth subsystem** • Section 4.3 "Bluetooth host interfaces": updated • Section 5 "Coexistence ": updated **Pin information** • Section 6.4 "Pin types": added A I/O • Section 6.5.1 "Pin states": updated • Section 6.5.2 "General purpose I/O (GPIO) (MFP)": updated GPIO[15], GPIO[14], GPIO[13], GPIO[12], GPIO[5] , GPIO[4], and GPIO[1] description • Section 6.5.10 "Clock interface": updated XTAL_IN and SLP_CLK_IN descriptions • Section 6.5.12 "Power supply and ground": updated VIO_SD description • Section 6.5.13 "JTAG interface": added • Section 6.6 "Configuration pins": updated the second table *Host configuration options* ————*Continues*————

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Table 68. Revision history...*continued*

Document ID	Release date	Description
IW416 v.3.0	12 March 2021	————*Continued*———— **Power information** • Section 7.1 "Power modes": added a table footnote for deep-sleep mode • Section 7.2 "Power-up sequence": updated the introduction • Section 7.3 "Power-down sequence": updated VCORE value in the figure • Section *Host power-down pin (PMIC_EN) usage*: updated VCORE value in the figure **Absolute maximum ratings** • Table 26 "Absolute maximum ratings ": updated the parameter definitions and removed the column with typical values. No change for the min. and max. values. **Electrical specifications** • Section 10.10.2 "External crystal specifications": updated the series resistance (ESR) maximum value • Section 10.3.1 "Wi-Fi radio performance measurement": added • Section 10.3.2 "2.4 GHz Wi-Fi receive performance": updated • Section 10.3.3 "5 GHz Wi-Fi receive performance": updated • Section 10.3.4 "2.4 GHz Wi-Fi transmit performance": updated • Section 10.3.4 "2.4 GHz Wi-Fi transmit performance": updated • Section 10.4.1 "Bluetooth/Bluetooth LE receive performance": updated • Section 10.4.2 "Bluetooth/Bluetooth LE transmit performance": updated • Section 10.6 "Current consumption": updated **Package information** • Section 11.1.2 "WLCSP76 thermal conditions": added • Section 11.3.1 "HVFQN68 marking": updated • Section 11.3.2 "WLCSP76 marking": added

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Table 68. Revision history...*continued*

Document ID	Release date	Description
IW416 v.2.0	31 July 2020	Preliminary data sheet **Overall document** • Changed the document title • Renamed WLAN as Wi-Fi **Product overview** • Updated the introduction • Replaced the overall block diagram with the application block diagram and the internal block diagram Section 1.6 "General features": added WLCSP76 package option ***Wi-Fi subsystem*** • Moved the content related to Wi-Fi in former Main Features section into this section ***Bluetooth subsystem*** • Moved the content related to Bluetooth in former Main Features section into this section ***Pin information*** • Updated Section 6.1 "Signal diagram" • Corrected pins 39 and 40 in Section 6.2 "Pin assignment - HVQFN68 package" and rotated the diagram to reflect the position of pin 1 on the top left side • Added Section 6.2.1 "Pin list by number - HVQFN68 package" • Added Section 6.5 "Pin description" • Added Section 6.3 "Bump locations - WLCSP76 package" **Absolute maximum ratings** • Section 8 "Absolute maximum ratings": added the table with limiting values **Recommended operating conditions** • Updated VCORE minimum value **Electrical specifications** • Section 10.10.1 "External crystal oscillator specifications": added 40 MHz reference clock • Section 10.10.2 "External crystal specifications": updated fundamental frequencies typical value **Package information** • Updated Section 11.2.1 "HVQFN68 mechanical drawing" • Added Section 11.2.2 "WLCSP76 mechanical drawing" • Added Section 11.1.2 "WLCSP76 thermal conditions" • Updated Section 11.3.1 "HVFQN68 marking" • Added Section 11.3.2 "WLCSP76 marking" **Ordering information** • Added the part numbering scheme and updated the part order codes
IW416 v.1.0	10 January 2020	Objective data sheet • Initial release

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Tables

Tab. 1. Host interface options 2
Tab. 2. Part order codes 5
Tab. 3. Supported channels (20 MHz) 8
Tab. 4. Supported channels (40 MHz) 9
Tab. 5. Wi-Fi and Bluetooth/Bluetooth LE supported TX and or RX operations - Single-antenna configuration 14
Tab. 6. Pin list by number - HVQFN68 package 19
Tab. 7. Pin by name - HVQFN68 package 21
Tab. 8. Bump names and locations on WLCSP76 top view 24
Tab. 9. Pin types 27
Tab. 10. GPIO (MFP) 28
Tab. 11. Wi-Fi/Bluetooth radio interface 30
Tab. 12. Wi-Fi RF front-end control interface 30
Tab. 13. SDIO host i (MFP) 31
Tab. 14. UART host interface (MFP) 32
Tab. 15. Audio interface pins (MFP) 32
Tab. 16. PTA coexistence interface (MFP) 33
Tab. 17. WCI-2 coexistence interface 33
Tab. 18. Clock interface 34
Tab. 19. Power down (PDn) pin 34
Tab. 20. Power and ground pins 35
Tab. 21. JTAG interface pins (MFP) 35
Tab. 22. Configuration pins 36
Tab. 23. Host configuration options 36
Tab. 24. Device power modes 37
Tab. 25. Configuration—VCORE from PMIC 38
Tab. 26. Absolute maximum ratings 42
Tab. 27. Limiting values 42
Tab. 28. Recommended operating conditions 43
Tab. 29. DC electrical characteristics—1.8V operation (VIO) 44
Tab. 30. DC electrical characteristics—3.3V operation (VIO) 44
Tab. 31. DC electrical characteristics—1.8V operation (VIO_RF) 45
Tab. 32. DC electrical characteristics—3.3V operation (VIO_RF) 45
Tab. 33. 2.4 GHz Wi-Fi receive performance 47
Tab. 34. 5 GHz Wi-Fi receive performance 49
Tab. 35. 2.4 GHz Wi-Fi transmit performance 51
Tab. 36. 5 GHz Wi-Fi transmit performance 52
Tab. 37. Local oscillator 52
Tab. 38. Bluetooth/Bluetooth LE receive performance 53
Tab. 39. Bluetooth/Bluetooth LE transmit performance 57
Tab. 40. WCI-2 interface transport settings 63
Tab. 41. PTA coexistence interface signal timing data 69
Tab. 42. Current consumption values 70
Tab. 43. VIO_SD requirements 73
Tab. 44. DC electrical characteristics—1.8V operation (VIO_SD) 73
Tab. 45. DC electrical characteristics—3.3V operation (VIO_SD) 73
Tab. 46. SDIO timing data—Default speed, high-speed modes 74
Tab. 47. SDIO timing data——SDR12, SDR25, SDR50 modes (up to 100MHz) (1.8V) 75
Tab. 48. SDIO timing data—DDR50 mode (50MHz) 77
Tab. 49. SDIO internal pull-up/pull-down specifications 77
Tab. 50. UART timing data 78
Tab. 51. PCM timing specification data—central mode 79
Tab. 52. PCM timing specification data—peripheral mode 80
Tab. 53. Clock DC specifications 81
Tab. 54. 26 MHz clock timing 81
Tab. 55. 40 MHz clock timing 81
Tab. 56. Phase noise—2.4 GHz operation 82
Tab. 57. Phase noise—5 GHz operation 82
Tab. 58. External crystal specifications 83
Tab. 59. External sleep clock specifications 83
Tab. 60. PDn pin (Power Down) specifications—Power remains high at PDn assertion 84
Tab. 61. PDn pin (Power Down) specifications—Power ramps down at PDn assertion 85
Tab. 62. Configuration pin specifications 86
Tab. 63. JTAG timing data 86
Tab. 64. Package thermal conditions—HVQFN68 87
Tab. 65. Package thermal conditions—WLCSP76 88
Tab. 66. Package information 89
Tab. 67. Abbreviations 96
Tab. 68. Revision history 99

Figures

Fig. 1. Application block diagram 1
Fig. 2. Internal block diagram 4
Fig. 3. Part numbering scheme 5
Fig. 4. PCM Short Frame Sync 13
Fig. 5. Hardware coexistence interface - WCI-2 coexistence interface 15
Fig. 6. Hardware coexistence interface - PTA external coexistence interface 16
Fig. 7. Signal diagram 17
Fig. 8. Pin assignment (package top view) - HVQFN68 18
Fig. 9. Bump locations - WLCSP76 (non-bump side view, bumps down) 23
Fig. 10. Configuration—VCORE from PMIC 38
Fig. 11. Power-up sequence 39
Fig. 12. Power-down sequence 40

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Fig. 13. RF performance measurement points 46
Fig. 14. UART waveform 60
Fig. 15. WCI-2 coexistence interface 60
Fig. 16. Type 0: Real time signaling message - external radio to IW416 61
Fig. 17. Type 7: Vendor specific message - external radio to IW416 61
Fig. 18. Type 0: Real time signaling message - IW416 to external radio 61
Fig. 19. Type 1: Transport control message time signaling message - IW416 to external radio 62
Fig. 20. MWS inactivity duration message 62
Fig. 21. Type 5: MWS scan frequency message 62
Fig. 22. WCI-2 transmit signal waveform 63
Fig. 23. PTA coexistence interface timing diagram - Example 1 64
Fig. 24. PTA coexistence interface timing diagram - Example 2 65
Fig. 25. PTA coexistence interface timing diagram - Example 3 66
Fig. 26. PTA coexistence interface timing diagram - Example 4 67
Fig. 27. PTA coexistence interface timing diagram - Example 5 68
Fig. 28. SDIO protocol timing diagram—Default speed mode 74
Fig. 29. SDIO protocol timing diagram—High-speed mode 74
Fig. 30. SDIO protocol timing diagram—SDR12, SDR25, SDR50 modes (up to 100MHz) (1.8V) 75
Fig. 31. SDIO CMD timing diagram—DDR50 mode (50MHz) 76
Fig. 32. SDIO DAT[3:0] timing diagram—DDR50 mode 76
Fig. 33. UART timing diagram 78
Fig. 34. PCM timing specification diagram for data signals—central mode 79
Fig. 35. PCM timing specification diagram for PCM_SYNC signal—central mode 79
Fig. 36. PCM timing specification diagram for data signals—peripheral mode 80
Fig. 37. PCM timing specification diagram for PCM_SYNC signal—peripheral mode 80
Fig. 38. PDn pin (Power-down) timing—Power remains high at PDn assertion 84
Fig. 39. PDn pin (Power Down) timing—Power ramps down at PDn assertion 85
Fig. 40. JTAG timing diagram 86
Fig. 41. HVQFN68 package mechanical drawing 90
Fig. 42. HVFQN68 package mechanical drawing - Detail G 91
Fig. 43. WLCSP76 package mechanical drawing 92
Fig. 44. WLCSP76 package mechanical drawing - Detail E 93
Fig. 45. Package marking and pin 1 location —HVQFN68, commercial operating temperature 94
Fig. 46. Package marking and pin 1 location—HVQFN68, industrial operating temperature ... 94
Fig. 47. Package marking and pin 1 location —WLCSP76, commercial operating temperature range 95
Fig. 48. Package marking and pin 1 location—WLCSP76, industrial operating temperature range 95

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Contents

1 Product overview 1
1.1 Applications 2
1.2 Wi-Fi key features 2
1.3 Bluetooth key features 2
1.4 Host interfaces 2
1.5 Operating characteristics 3
1.6 General features 3
1.7 Internal block diagram 4
2 Ordering information 5
3 Wi-Fi subsystem 6
3.1 IEEE 802.11 standards 6
3.2 Wi-Fi MAC 6
3.3 Wi-Fi baseband 7
3.4 Wi-Fi radio 7
3.5 Wi-Fi encryption 10
3.6 Wi-Fi host interfaces 10
4 Bluetooth subsystem 11
4.1 Bluetooth 2.4 GHz TX/RX 11
4.2 Bluetooth Low Energy (LE) 12
4.3 Bluetooth host interfaces 12
4.4 Audio interfaces 12
4.4.1 I2S interface 12
4.4.2 PCM interface 12
4.4.2.1 Protocol description 13
5 Coexistence 14
5.1 Antenna configurations 14
5.1.1 Dual-antenna configuration 14
5.1.2 Single-antenna configuration 14
5.2 Central hardware packet traffic arbiter 14
5.3 Coexistence with an external radio 15
6 Pin information 17
6.1 Signal diagram 17
6.2 Pin assignment - HVQFN68 package 18
6.2.1 Pin list by number - HVQFN68 package 19
6.2.1 Pin list by name - HVQFN68 package 21
6.3 Bump locations - WLCSP76 package 23
6.3.1 Bump positions relative to die center - WLCSP76 24
6.4 Pin types 27
6.5 Pin description 27
6.5.1 Pin states 27
6.5.2 General purpose I/O (GPIO) (MFP) 28
6.5.3 Wi-Fi/Bluetooth radio interface 30
6.5.4 Wi-Fi RF front-end control interface 30
6.5.5 SDIO host interface (MFP) 31
6.5.6 UART host interface 32
6.5.7 Audio interface 32
6.5.8 PTA coexistence interface 33
6.5.9 WCI-2 coexistence interface 33
6.5.10 Clock interface 34
6.5.11 Power down (PDn) pin 34
6.5.12 Power supply and ground 35
6.5.13 JTAG interface 35
6.6 Configuration pins 36
7 Power information 37
7.1 Power modes 37
7.2 Power-up sequence 38
7.2.1 Configuration—VCORE from PMIC 38
7.2.2 Power-up sequence timing 39
7.3 Power-down sequence 40
7.4 Leakage optimization 41
7.5 Deep sleep 41
7.6 Reset 41
8 Absolute maximum ratings 42
9 Recommended operating conditions 43
10 Electrical specifications 44
10.1 GPIO/LED interface specifications 44
10.1.1 VIO DC characteristics 44
10.1.1.1 1.8V operation 44
10.1.1.2 3.3V operation 44
10.2 RF front-end control interface specifications 45
10.2.1 VIO_RF DC characteristics 45
10.2.1.1 1.8V operation 45
10.2.1.2 3.3V operation 45
10.3 Wi-Fi radio specifications 46
10.3.1 Wi-Fi radio performance measurement 46
10.3.2 2.4 GHz Wi-Fi receive performance 47
10.3.3 5 GHz Wi-Fi receive performance 49
10.3.4 2.4 GHz Wi-Fi transmit performance 51
10.3.5 5 GHz Wi-Fi transmit performance 52
10.3.6 Local oscillator 52
10.4 Bluetooth radio specifications 53
10.4.1 Bluetooth/Bluetooth LE receive performance 53
10.4.2 Bluetooth/Bluetooth LE transmit performance 57
10.5 External coexistence interface specifications 60
10.5.1 WCI-2 coexistence interface specifications 60
10.5.1.1 WCI-2 interface 60
10.5.1.2 WCI-2 messages 61
10.5.1.3 WCI-2 signal waveform format 63
10.5.2 PTA interface coexistence specifications 64
10.6 Current consumption 70
10.7 SDIO host interface specifications 73
10.7.1 VIO_SD DC characteristics 73
10.7.1.1 1.8V operation 73
10.7.1.2 3.3V operation 73
10.7.2 Default speed, high-speed modes 74
10.7.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V) 75
10.7.4 DDR50 mode (50MHz) (1.8V) 76
10.7.5 SDIO internal pull-up/pull-down specifications 77
10.8 High-speed UART specifications 78
10.9 Audio interface specifications 78
10.9.1 I2S interface specifications 78
10.9.2 PCM interface specifications 78
10.10 Reference clock specifications 81
10.10.1 External crystal oscillator specifications 81
10.10.2 External crystal specifications 83
10.10.3 External sleep clock specifications 83

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10.11 Power down (PDn) pin specifications 84
10.11.1 PDn asserted low—All power supplies good ... 84
10.11.2 PDn asserted low—One or more power supplies ramp down 85
10.12 Configuration pin specifications 86
10.13 JTAG interface specifications 86
11 Package information 87
11.1 Package thermal conditions 87
11.1.1 HVQFN68 thermal conditions 87
11.1.2 WLCSP76 thermal conditions 88
11.2 Package mechanical drawing 89
11.2.1 HVQFN68 mechanical drawing 90
11.2.2 WLCSP76 mechanical drawing 92
11.3 Package marking 94
11.3.1 HVFQN68 marking 94
11.3.2 WLCSP76 marking 95
12 Abbreviations 96
13 Revision history 99
Legal information 106

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