IW623S

Tri-band (2.4-5-7 GHz) Wi-Fi 6/6E and Bluetooth Combo Solution

Rev. 5.0 — 30 March 2026 Product data sheet

1 Product overview

The IW623S is a highly integrated Wi-Fi 6/6E device enabling tri-band Wi-Fi and Bluetooth operation. Supporting a 2x2 MIMO configuration in the 2.4 GHz and 5-7 GHz bands, the system-on-chip (SoC) implements advanced features including MU-MIMO, OFDMA, target wake-up time (TWT), and Bluetooth LE Audio.

With integrated 2.4 GHz and 5-7 GHz TX power amplifiers (PA), RX low noise amplifiers (LNA) and TX/RX switches (T/R SW) as well as a full Bluetooth radio, the IW623S simplifies design.

The IW623S implements advanced real-time Wi-Fi and Bluetooth arbitration hardware with software algorithms to optimize coexistence performance.

NXP's Edgelock technology is integrated. The embedded Edgelock secure subsystem (ELS) supports hardware crypto accelerated secure boot, key management, firmware encryption and authentication, secure life cycle management, and anti-rollback protection. IW623S is designed from the ground up to meet SESIP security.

The IW623S integrates dedicated CPUs and memories for both the Wi-Fi and Bluetooth subsystems for real time, independent protocol processing.

The interfaces to external host processors include SDIO for Wi-Fi and UART for Bluetooth.

Figure 1 shows IW623S application diagram.

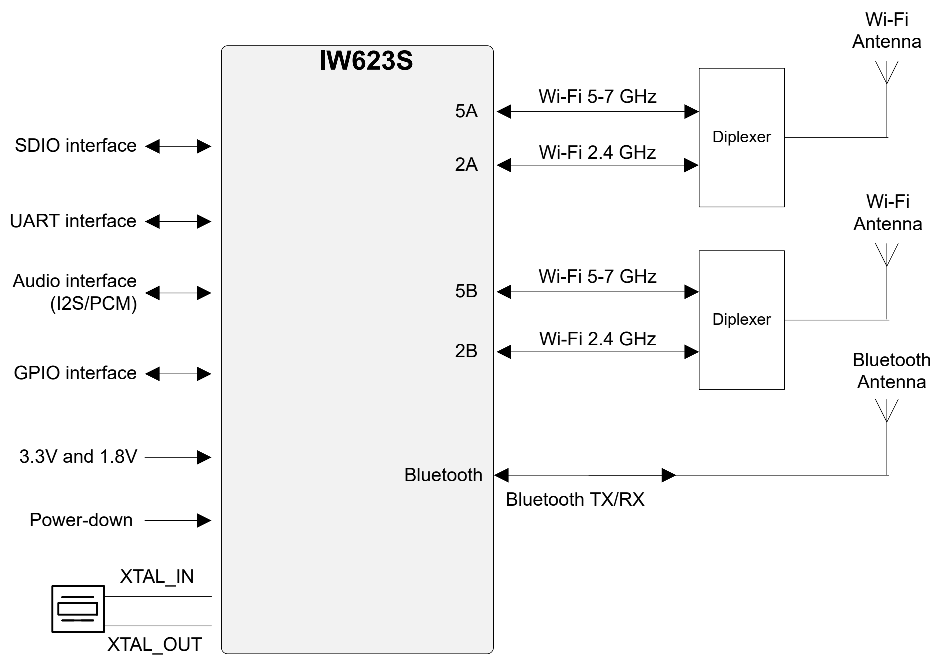


Figure 1. IW623S application diagram

1.1 Applications

- Wireless IP and security cameras
- Video-enabled smart appliances
- Wireless power over Ethernet (POE) hub
- Smart home hub
- Internet of things (IoT) gateways

1.2 Wi-Fi key features

2x2 Wi-Fi 6E (802.11ax)

- Tri-band (2.4 GHz, 5 GHz, and 6 GHz)
- 40 MHz channel for 2.4 GHz (RF paths 2A/2B)
- 1024 QAM (MCS11), up to 80 MHz channel for 5-7 GHz (RF paths 5A/5B)
- STA and mobile AP
- Wi-Fi TSF host clock sync between AP and STA
- Wi-Fi cross-chip TSF clock sync between AP and AP

1.3 Bluetooth key features

- Integrated PA (+13 dBm)/LNA/RF switch
- BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), 3 Mbps (8DPSK)
- Bluetooth LE uncoded (1 Mbps/2 Mbps) and long range (125 kbps/500 kbps) support
- Bluetooth LE advertising extensions for improved capacity
- Isochronous channels (ISOC) supporting LE Audio

1.4 Host interfaces

Wi-Fi and Bluetooth interface options

Table 1. Host interface options

Wi-Fi	Bluetooth
SDIO	UART

1.5 Operating characteristics

- Supply voltage: 1.8 V and 3.3 V
- Operating temperature: – 40 °C to 85 °C
- Storage temperature: – 55 °C to 125 °C

1.6 General features

Package options

- HVQFN148 (dual-row) 11 mm x 11 mm x 0.85 mm with 0.5 mm pitch

Coexistence

- Internal coexistence between Wi-Fi and Bluetooth
- External coexistence interface for connection to external radios such as UWB and cellular modems

Power management

- Individual low-power down for Wi-Fi and Bluetooth subsystems
- Low-power standby
- Integrated high-efficiency buck DC-DC converter
- Wake-up through GPIO, host interface, and RTC

Memory

- One Time Programmable (OTP) memory to store the MAC address and calibration data
- Addressable memory space is accessible to all CPUs

Security

- Secure boot and debug management
- Firmware authentication
- Lifecycle management
- Anti-rollback protection
- Hardware cryptography for boot acceleration
- Secure key generation and management for boot management
- Authenticated, integrity-verified, and encrypted firmware
- Voltage glitch attack resistance
- Targeting SESIP security certification

1.7 Internal block diagram

Figure 2 shows IW623S internal block diagram.

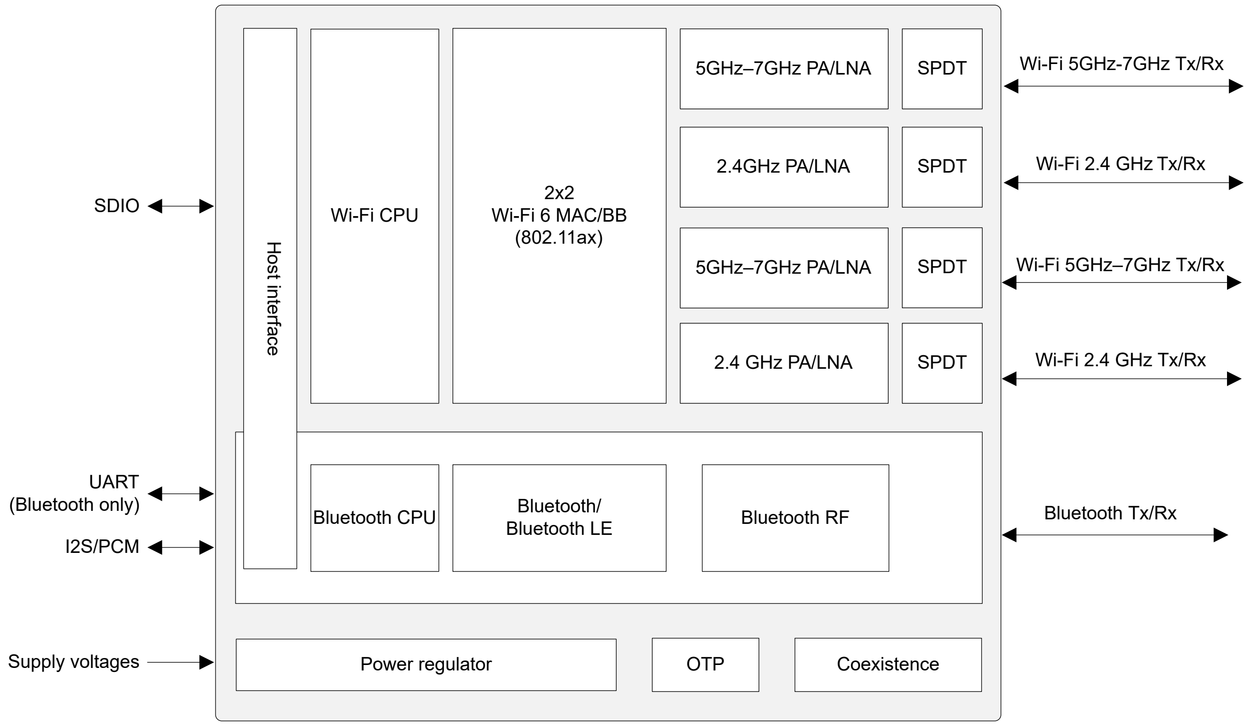


Figure 2. IW623S internal block diagram

2 Ordering information

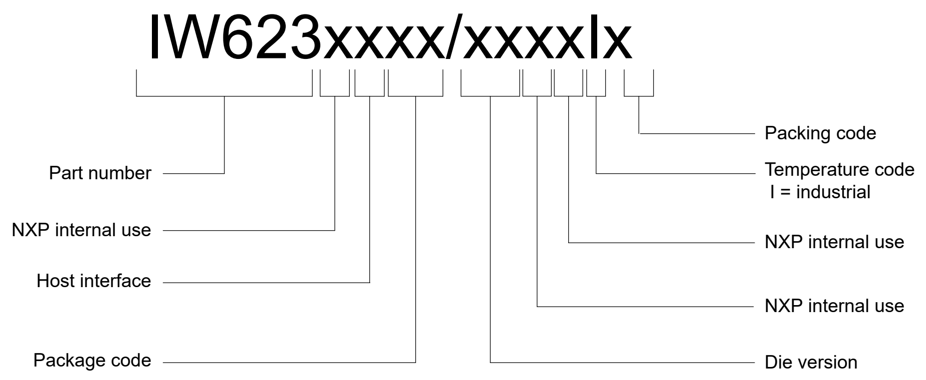


Figure 3. IW623S part numbering scheme

Table 2. Part order codes

Part order code	Package type	Operating temperature range	Packing
IW623LSHN/A1ZDIK	HVQFN148 (dual-row) 11 mm x 11 mm x 0.85 mm with 0.5 mm pitch	40°C to 85°C	Tray
IW623LSHN/A1ZDIMP	HVQFN148 (dual-row) 11 mm x 11 mm x 0.85 mm with 0.5 mm pitch	40°C to 85°C	Tape and Reel

3 Wi-Fi subsystem

3.1 IEEE 802.11 standards

- 802.11ax
  - 2x2 SU and MU-MIMO/OFDMA (MU-MIMO/OFDMA for STA mode only)
  - Target wake time (TWT)
- 802.11ac
  - Wave 1/2 backward-compatible
  - Downlink MU-MIMO for STA mode only
- 802.11n/a/g/b backward-compatible
- 802.11az accurate ranging
- 802.11d operation in other regulatory domains
- 802.11e quality of the service
- 802.11h
  - Transmit power control
  - DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11mc fine time measurement (FTM)
- 802.11r fast hand-off for AP roaming
- 802.11u Hotspot 2.0 (STA mode only)
- 802.11v TIM frame transmission/reception
- 802.11w protected management frames
- 802.11z tunneled direct-link setup
- Fully supports clients (stations) implementing IEEE Power-save mode

3.2 Wi-Fi MAC

- 802.11ax 2x2 MU-MIMO MAC
- Trigger Frame Formats
  - Basic trigger frame
  - Beamforming Report Poll (BFRP)
  - MU-BAR, MU-RTS, BSR Poll (BSRP) trigger variant
  - Trigger frame MAC padding
- Wireless Multi-stream
- HE Variants of HT Control
  - Basic format
  - UL Power Headroom
  - Receive Operation Mode control sub field
- HE MU Frame Exchange Sequences
- MU Acknowledgment (ACK)
- M-BA and C-BA Variants in BA Frames
- MU-RTS/CTS Procedures
- Target Wake Time Scheduling
- HE Dual-NAV
- UL Carrier Sensing
- Buffer Status Reports
- Operating Mode Indication (OMI)
- Multiple BSS/Station
- A-MPDU RX (de-aggregation) and TX (aggregation) (supports single-MPDU A-MPDU)
- Management information base counters
- Transmit rate adaptation
- Transmit power control
- Mobile hotspot

3.3 Wi-Fi baseband

BBU - 2x2 baseband

- 802.11ax 2x2 MU-MIMO baseband, backward-compatible with 802.11ac/n/a/g/b technology
- 6 GHz PHY data rates up 1.2 Gbit/s
- 5 GHz PHY data rates up 1.2 Gbit/s
- 2.4 GHz PHY data rates up 573.5 Mbps
- Bandwidth support
  - 20 MHz
  - 40 MHz
  - 80 MHz
- Modulation and coding schemes (MCS)
  - 802.11ax—MCS 0~11
    - Up to 2 spatial streams for 20, 40, 80 MHz
  - 802.11ac—MCS 0~9 Nsts = 1 and 2
    - Up to 2 spatial streams for 20, 40, 80 MHz
  - 802.11n—MCS 0~15 and MCS 32 (duplicate 6 Mbps)
  - Dual sub-carrier modulation (DCM)
    - MCS 0 only
  - BCC and LDPC coding
- Frame formats
  - 802.11ax HE_SU (Tx/Rx)
  - 802.11ax HE_MU (RX)
  - 802.11ax HE_ER_SU (Tx/Rx)
  - 802.11ax HE_TB (TX)
  - 802.11ac VHT
  - 802.11n HT
  - 802.11a (including dup/quad modes)
  - 802.11g (including dup mode)
  - 802.11b
- Channel state information (CSI)
- Optional 802.11ac and 802.11n MIMO features:
  - LDPC transmission and reception for both 802.11ac and 802.11n
  - 256 QAM (MCS 8, 9) modulation (optional support for 802.11ac MCS 9 in 20 MHz using LDPC)
  - Spectral intelligence
    - Spectrum monitoring
    - DFS assists to reduce false detections

BBU additional features

- Uplink MU-MIMO (STA mode only)
- Packet extension
  - Up to 8 us for highest rates
  - 0 us for all other modes
- Range extension
- Beam change
- Guard interval (GI) modes
  - 1x HE-LTF with 0.8 us GI
  - 1x HE-LTF with 1.6 us GI (for UL TB PPDU)
  - 2x HE-LTF with 0.8 us GI
  - 2x HE-LTF with 1.6 us GI
  - 4x HE-LTF with 3.2 us GI
  - 4x HE-LTF with 0.8 us GI
- Optional 802.11ac and 802.11n MIMO features:
  - 20/40/80 MHz coexistence with middle-packet detection (GI detection) for enhanced CCA
  - Short guard interval (0.4 us)
  - RIFS on receive path for 802.11n packets
  - VHT MU-PPDU (receive)
- Precise indoor location positioning (802.11mc)
- Power save features

3.4 Wi-Fi radio

RFU – 2x2 dual-band Wi-Fi RF

- 802.11ax 2x2 MU-MIMO on-chip RF radio

RFU additional features

- Integrated PA
- On-chip LNAs with optimized noise figure and power consumption
- High dynamic range RX AGC
- Optimized TX gain distribution for linearity and noise performance

3.5 Wi-Fi encryption

- Data Frame Encryption/Decryption
  - AES/CCMP
  - AES/GCMP
  - WAPI
- Management Frame Encryption/Decryption for broadcast/multicast packets
  - AES/CMAC
- Management Frame Encryption/Decryption for unicast packets
  - AES/CCMP
  - AES/GCMP

3.6 Transmit Beamforming (TxBF)

- 802.11ax/ac/n explicit beamformer
  - NDP sounding to stations capable of explicit beamformee
  - Beamforming up to two streams
- 802.11ax/ac/n explicit beamformee
  - Supports sounding feedback for up to 8x8 beamformer

3.7 RF channels

The list of channels for Wi-Fi is available in Section 14.1.

3.8 Wi-Fi host interfaces

- SDIO 3.0 device interface

4 Bluetooth subsystem

4.1 Bluetooth features

- Bluetooth 6.1 certified
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Bluetooth
- PCM and I2S interfaces for voice applications
- Baseband/radio BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), 3 Mbps (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER)
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full central and peripheral piconet support[1]
- Scatternet support
- Standard UART HCI transport layer
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power saving mechanisms (sniff modes, and sniff sub-rating)
- Enhanced Power Control (EPC)
- Channel Quality Driven Data Rate (CQDDR)
- Wideband Speech (WBS) support (two WBS links)[2]
- Encryption (AES) support
- HCI Encryption Key Size Control

1 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.
2 Two WBS over PCM where the device under test (DUT) must be central.

4.2 Bluetooth Low Energy (LE) features

- Bluetooth LE 6.1 certified
- Supports up to 16 simultaneous central/peripheral connections[3]
- Wi-Fi/Bluetooth coexistence protocol support
- Shared RF with BDR/EDR
- Encryption (AES) support
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- Bluetooth LE Long Range
- Bluetooth LE 2 Mbps
- Bluetooth LE Power Control (LEPC)
- Bluetooth LE Isochronous Channels (ISOC)[4]
- Bluetooth LE Connection Subrating[5]
- Bluetooth LE Channel Classification Enhancement[5]
- Periodic Advertising ADI support[5]

4.3 Bluetooth host interfaces

- High-Speed UART interface

3 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.
4 Bluetooth LE audio supported with external host running Low Complexity Communication Codec (LC3) through HCI interface.
5 Check the feature support in the software release notes.

4.4 Digital audio interfaces

4.4.1 I2S interface

- I2S (Inter-IC Sound) interface for audio data connection to Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)
- Central and peripheral mode for I2S, MSB, LSB audio interfaces (single Bluetooth)[6]
- Tri-state I2S interface compatibility
- I2S pins shared with PCM pins
- I2S narrow band speech (NBS) with 8 kHz sampling rate
- I2S wide band speech (WBS) with 16 kHz sampling rate

4.4.1.1 I2S interface signals

Refer to Section 6.5.8 "Digital audio interface".

4.4.1.2 I2S interface protocol

Figure 4 shows I2S interface protocol.

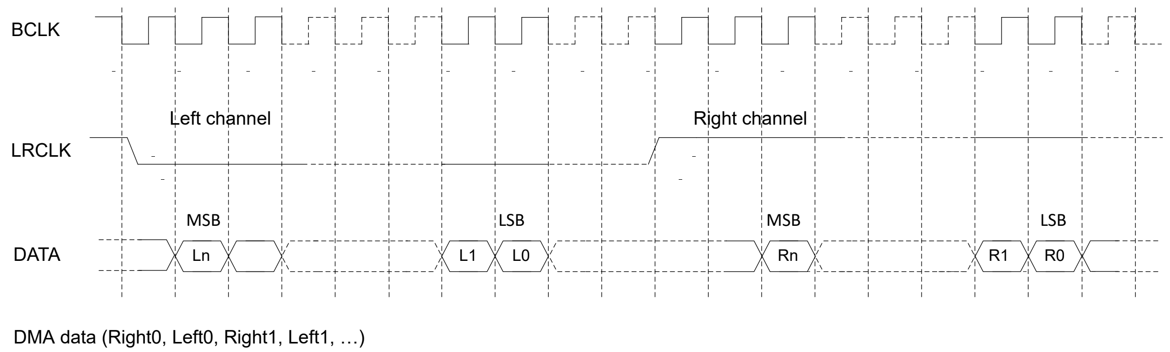


Figure 4. I2S interface protocol

6 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

IW623S supports mono and dual channel modes.

In mono-channel mode, by default the left channel is used for data.

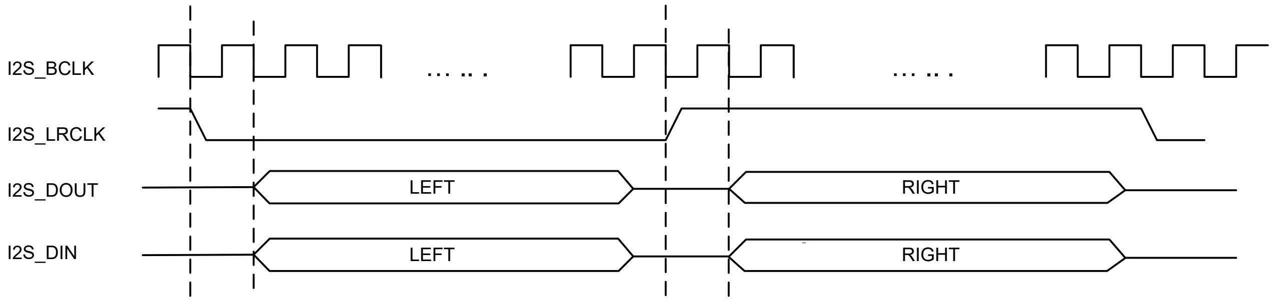


Figure 5. I2S timing specification diagram—Mono channel mode

In dual-channel mode, the two channels are supported on two time slots.

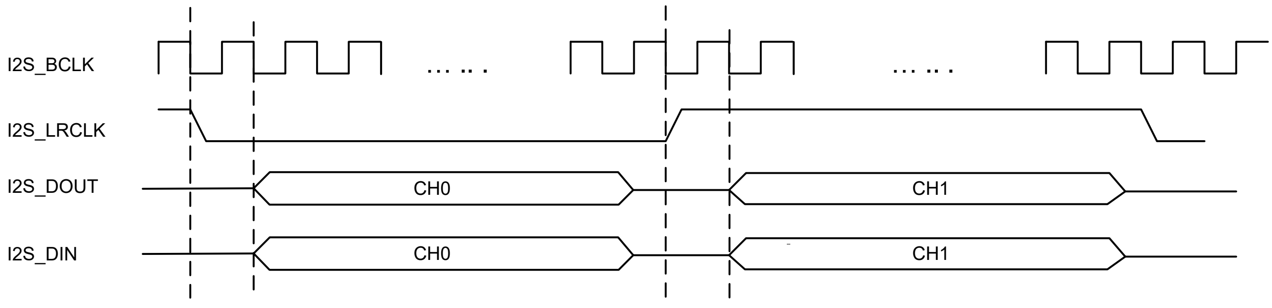


Figure 6. I2S timing specification diagram—Dual channel mode

4.4.1.3 Clock frequency and audio data resolutions

Audio data may arrive with different input data formats with different sampling rates.

In central mode, the I2S interface uses an audio input clock of 4.096 MHz or 2.048 MHz to provide the appropriate M clock (MCLK) and bit clock (I2S_BCLK) frequency to match the sampling rates of each audio data format. The sampling rates can be 8 kHz to 16 kHz.[7]

In peripheral mode, the I2S interface does not provide the bit clock (I2S_BCLK) but it can provide the M clock (MCLK).[7]

7 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

4.4.2 PCM interface

- Central or peripheral mode[8]
- PCM bit width size of 16 bits
- Up to 4 slots with configurable bit width and start positions
- Tri-state PCM interface capability
- PCM short frame synchronization
- PCM pins shared with I2S
- PCM narrow band speech (NBS) with 8 kHz sampling rate
- PCM wide band speech (WBS) with 16 kHz sampling rate[9]
- Dual Hands free profile (HFP) (WBS/NBS) PCM

4.4.2.1 PCM interface signal description

Refer to Section 6.5.8 "Digital audio interface".

4.4.2.2 PCM protocol

The PCM interface supports short frame sync. Figure 7 shows an example of a PCM interface with four signals.

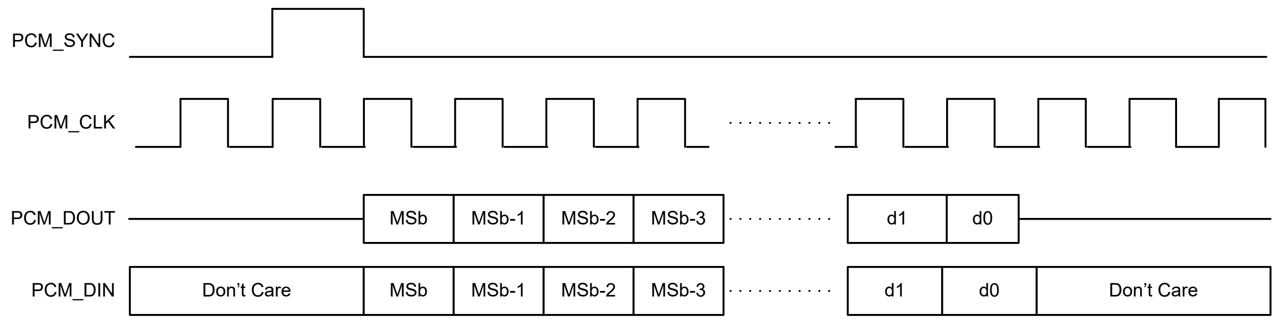


Figure 7. PCM short frame sync

8 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.
9 Two WBS over PCM where the device under test (DUT) must be Bluetooth piconet central

IW623S supports mono and dual channel modes.

Note: *Figure 8 and Figure 9 illustrate PCM mono and dual channel modes in short frame sync.*

In mono-channel mode, by default the left channel is used for data.

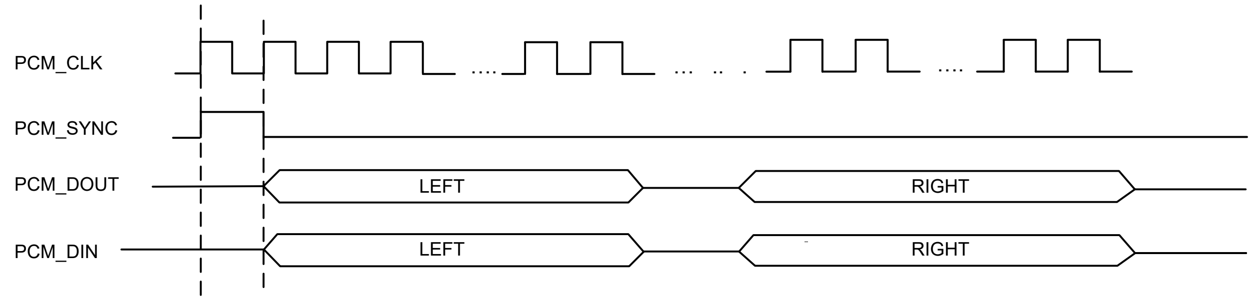


Figure 8. PCM mono channel mode (short frame sync)

In dual-channel mode, the two channels are supported on two time slots.

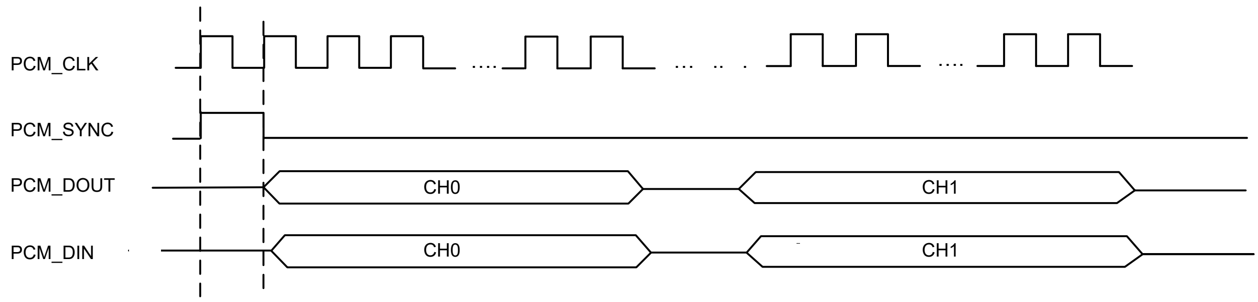


Figure 9. PCM dual channel mode (short frame sync)

4.4.2.3 PCM modes of operation

The PCM interface supports two modes of operation:

- PCM central[10]
- PCM peripheral[10]

When in PCM central mode, the interface generates a 2 MHz or a 2.048 MHz PCM_CLK and 8 kHz PCM_SYNC signal. An alternative PCM central mode is available that uses an externally generated PCM_CLK, but still generates the 8 kHz PCM_SYNC. The external PCM_CLK must have a frequency that is an integer multiple of 8 kHz. Supported frequencies are in the 512 kHz to 4 MHz range.[10]

When in PCM peripheral mode, the interface has both PCM_CLK and PCM_SYNC as inputs, thereby letting another unit on the PCM bus generate the signals.[10]

The PCM interface consists of up to four PCM slots (time divided) preceded by a PCM sync signal. Each PCM slot can be either 8 bit or 16 bit wide. The slots can be separated in time, but are not required to follow immediately after one other. The timing is relative to PCM_CLK. Figure 10 shows an example of a PCM burst with two slots.

The burst starts with a PCM_SYNC and then follows the PCM burst. In this example, the PCM burst consists of two PCM slots (the first slot is 8 bit wide, the second slot is 16 bit wide) separated with two PCM_ CLK clock cycles. The PCM slots can be configured to start at an arbitrary point in time, and the start value is given relative to the start of the PCM_SYNC. The timing of the four PCM slots must be such that slot 0 is always located before slot 1, slot 1 before slot 2, etc. It is possible to only use for example slot 1 and not slot 0.

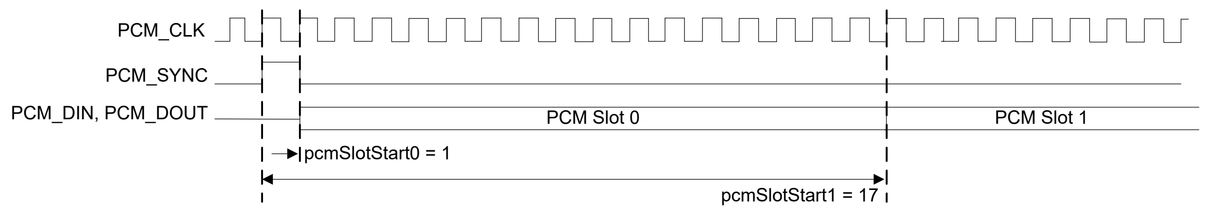


Figure 10. PCM burst with two PCM slots - PCM short frame sync

10 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

5 Coexistence

5.1 Antenna configurations

The IW623S supports two-antenna and three-antenna configurations.

5.1.1 Three-antenna configuration

The three separate antennas allow simultaneous independent operation of the Wi-Fi and Bluetooth radios, depending upon the antenna isolation.

5.2 Central hardware packet traffic arbiter

The central hardware packet traffic arbiter arbitrates the transmit and/or receive operations between the on-chip Wi-Fi and Bluetooth radios as per the supported hardware configuration. See Section 5.1.

The central hardware packet traffic arbiter has the following features:

- Supports simultaneous Wi-Fi and Bluetooth transmissions to optimize output transmit power levels and performance
- Supports simultaneous receive for all on-chip radios

In addition to the on-chip radios, the central hardware packet traffic arbiter arbitrates up to three external radios. Refer to Section 5.3.

5.3 Coexistence with external radios

The available interfaces for external coexistence are PTA, WCI-2, coex-UART, and debug-UART.

Note: *The external coexistence interfaces share the same multi-function pins (MFP). Refer to Section 6.5.2 for more details.*

WCI-2 external coexistence interface

WCI-2 is the two-wire wireless coexistence interface 2 protocol defined in the Bluetooth Core Specification (Vol 7 Part C).

Figure 11 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW623S.

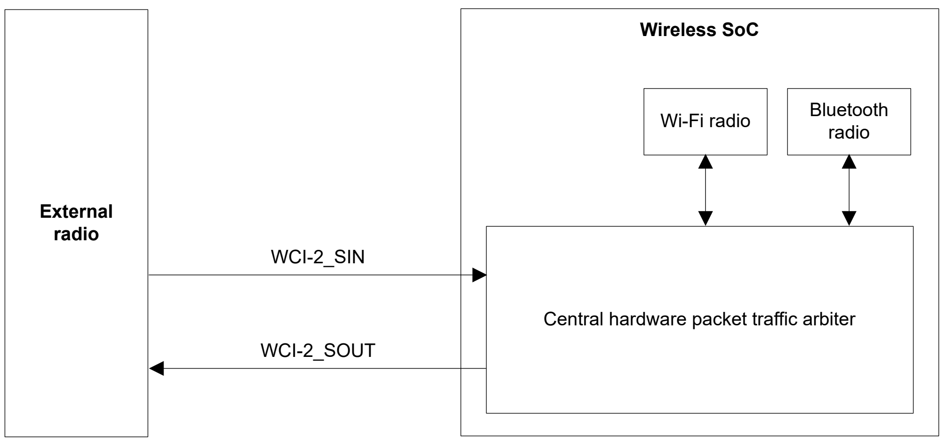


Figure 11. Hardware coexistence interface - WCI-2 coexistence interface

Note: *Refer to Section 6.5.10 for the description of WCI-2 coexistence interface signals.*

PTA external coexistence interface

Figure 12 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW623S.

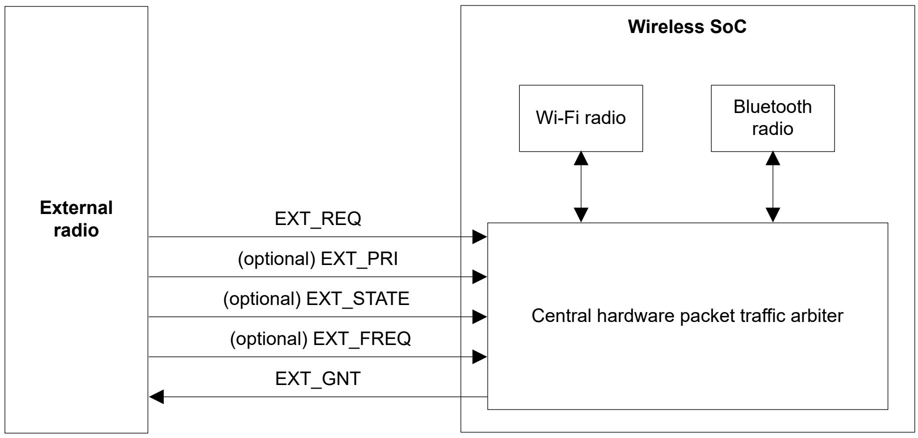


Figure 12. Hardware coexistence interface - PTA external coexistence interface

Note: *Refer to Section 6.5.9 for the description of PTA external coexistence interface signals.*

Coex-UART external coexistence interface

Figure 13 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW623S.

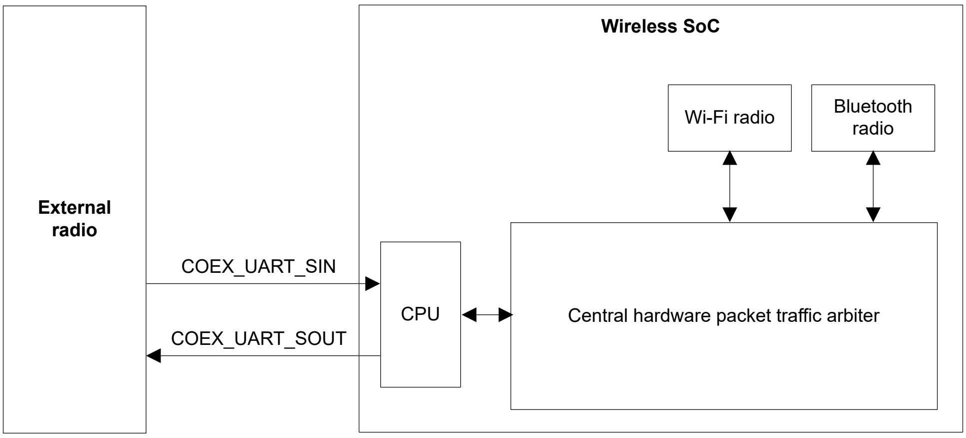


Figure 13. Hardware coexistence interface - Coex-UART external coexistence interface

Note: *Refer to Section 6.5.11 for the description of PTA external coexistence interface signals.*

The UART messages from the external radio are handled within the CPU and coordinated with the central hardware packet traffic arbiter for the arbitration with the on-chip radios.

Debug-UART external coexistence interface

Figure 14 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW623S.

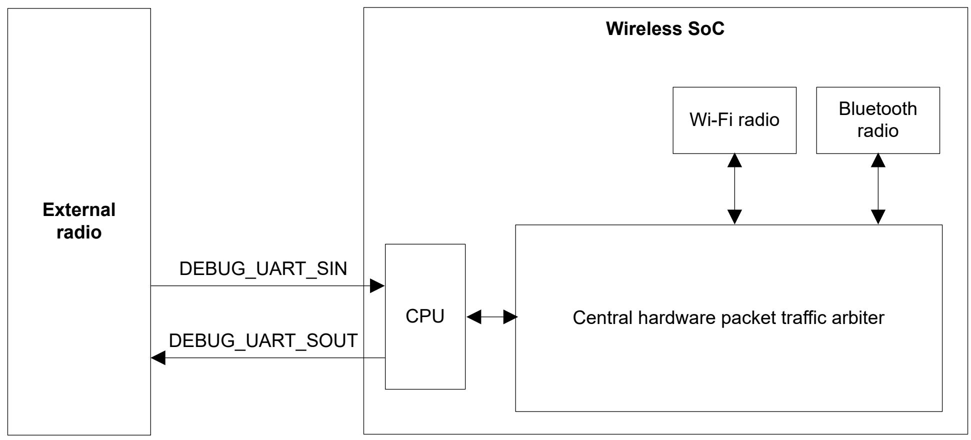


Figure 14. Hardware coexistence interface - Debug-UART external coexistence interface

Note: *Refer to Section 6.5.12 for the description of PTA external coexistence interface signals.*

The UART messages from the external radio are handled within the CPU and coordinated with the central hardware packet traffic arbiter for the arbitration with the on-chip radios.

6 Pin information

6.1 Signal diagram

Note: *Signals are muxed on dedicated pins. See Section 6.5 "Pin description" for the dedicated pin/muxed signal descriptions.*

In Figure 15, Wireless SoC is IW623S.

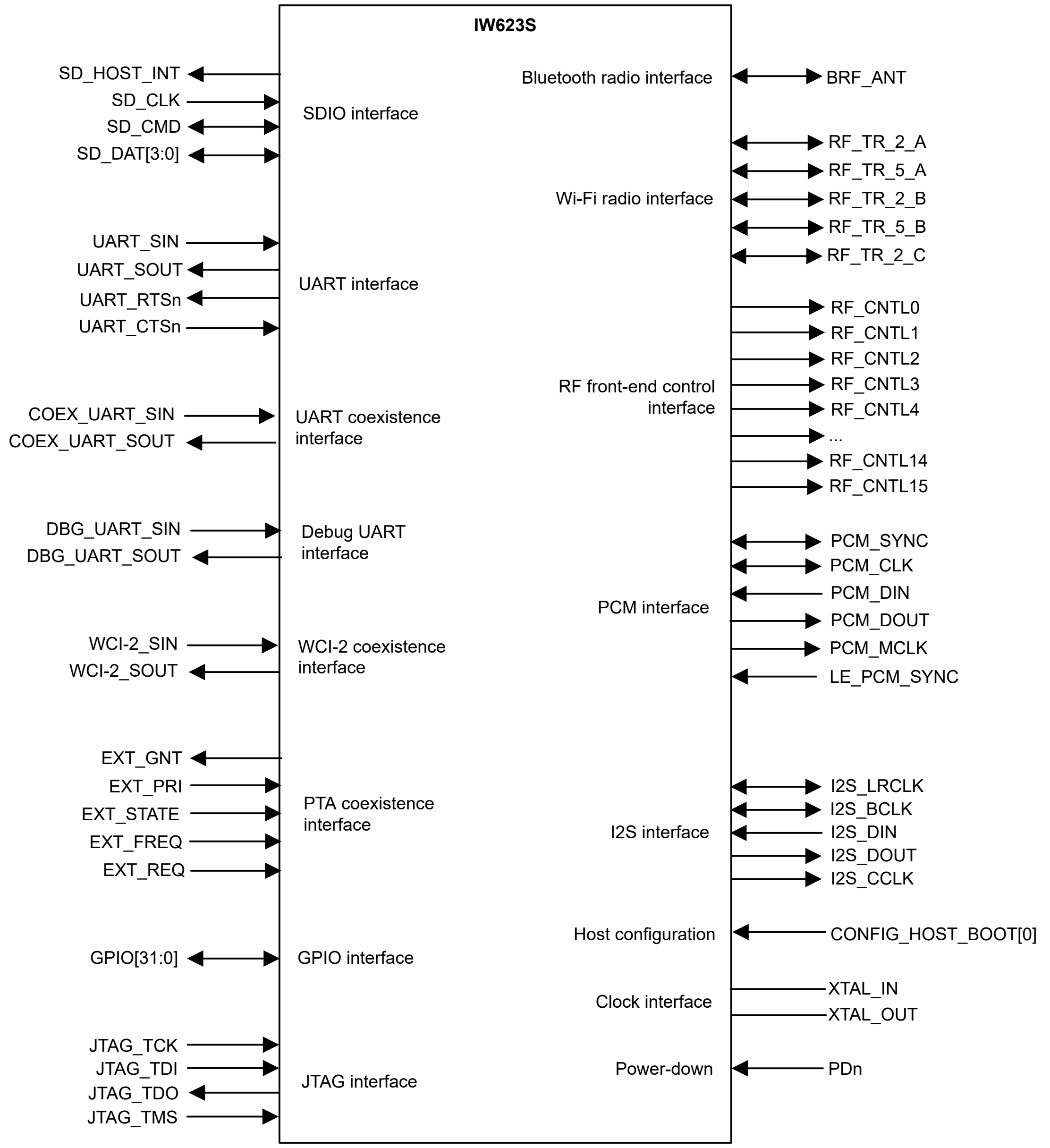


Figure 15. IW623S signal diagram

6.2 Pin assignment – HVQFN package

Figure 16 shows the pin assignment with SDIO host interface for Wi-Fi. Wireless SoC is IW623S.

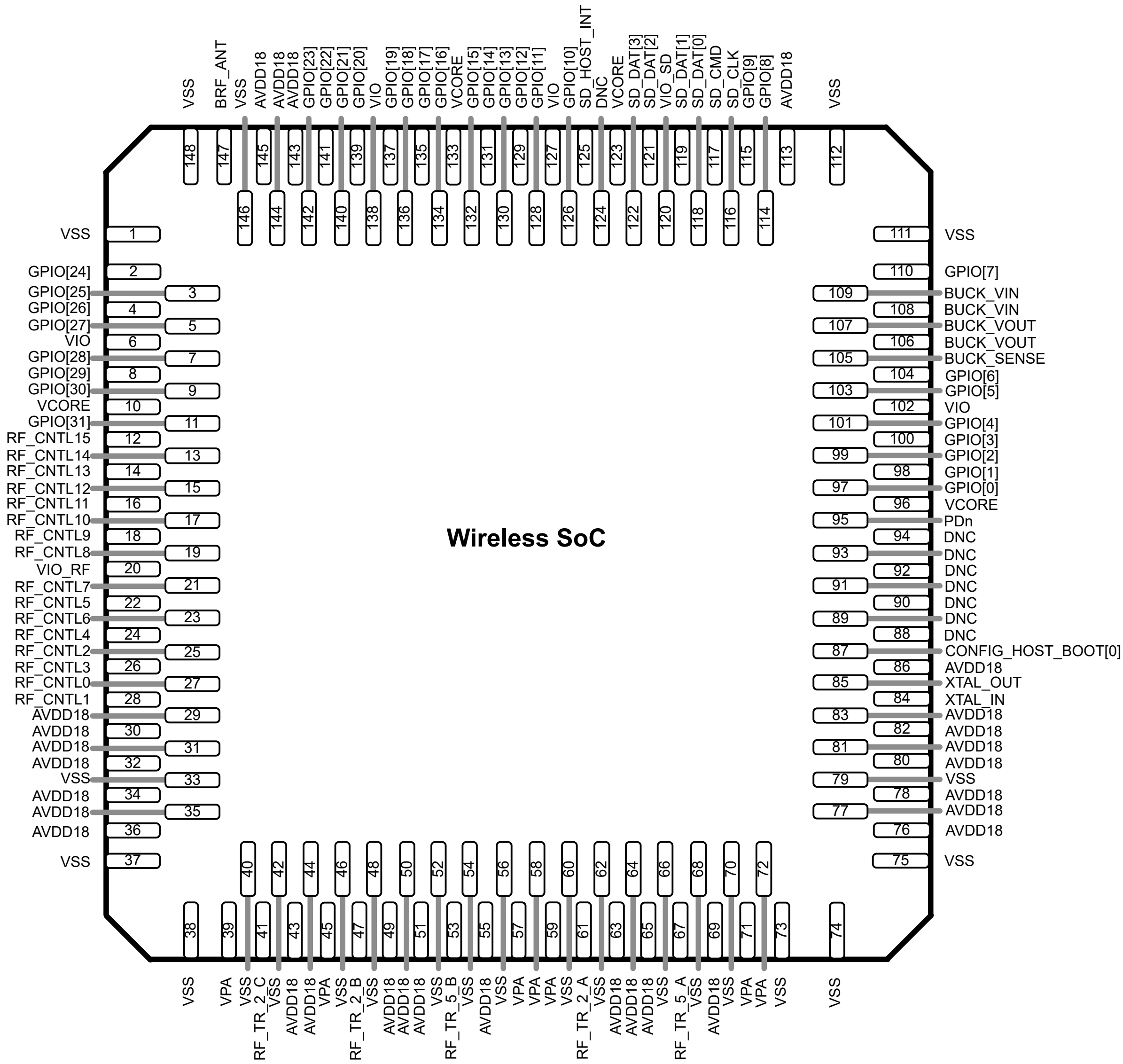


Figure 16. IW623S pin assignment (package top view) – SDIO host interface for Wi-Fi

6.3 Pin types

Table 3. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
DNC	Do not connect
Power	Power
Ground	Ground

6.4 Pin list – HVQFN package

Table 4 lists the pins for IW623S in HVQFN package, with SDIO host interface for Wi-Fi.

Table 4. Pin list by number – SDIO host interface for Wi-Fi

Pin number	Pin name	Supply	Type
1	VSS	—	Ground
2	GPIO[24]	VIO	I/O
3	GPIO[25]	VIO	I/O
4	GPIO[26]	VIO	I/O
5	GPIO[27]	VIO	I/O
6	VIO	—	Power
7	GPIO[28]	VIO	I/O
8	GPIO[29]	VIO	I/O
9	GPIO[30]	VIO	I/O
10	VCORE	—	Power
11	GPIO[31]	VIO_RF	I/O
12	RF_CNTL15	VIO_RF	O
13	RF_CNTL14	VIO_RF	O
14	RF_CNTL13	VIO_RF	O
15	RF_CNTL12	VIO_RF	O
16	RF_CNTL11	VIO_RF	O
17	RF_CNTL10	VIO_RF	O
18	RF_CNTL9	VIO_RF	O
19	RF_CNTL8	VIO_RF	O
20	VIO_RF	—	Power
21	RF_CNTL7	VIO_RF	O
22	RF_CNTL5	VIO_RF	O
23	RF_CNTL6	VIO_RF	O
24	RF_CNTL4	VIO_RF	O
25	RF_CNTL2	VIO_RF	O
26	RF_CNTL3	VIO_RF	O
27	RF_CNTL0	VIO_RF	O
28	RF_CNTL1	VIO_RF	O
29	AVDD18	—	Power
30	AVDD18	—	Power
31	AVDD18	—	Power
32	AVDD18	—	Power
33	VSS	—	Ground

Table 4. Pin list by number – SDIO host interface for Wi-Fi*...continued*

Pin number	Pin name	Supply	Type
34	AVDD18	—	Power
35	AVDD18	—	Power
36	AVDD18	—	Power
37	VSS	—	Ground
38	VSS	—	Ground
39	VPA	—	Power
40	VSS	—	Ground
41	RF_TR_2_C[1]	AVDD18	A, I/O
42	VSS	—	Ground
43	AVDD18	—	Power
44	AVDD18	—	Power
45	VPA	—	Power
46	VSS	—	Ground
47	RF_TR_2_B	AVDD18	A, I/O
48	VSS	—	Ground
49	AVDD18	—	Power
50	AVDD18	—	Power
51	AVDD18	—	Power
52	VSS	—	Ground
53	RF_TR_5_B	AVDD18	A, I/O
54	VSS	—	Ground
55	AVDD18	—	Power
56	VSS	—	Ground
57	VPA	—	Power
58	VPA	—	Power
59	VPA	—	Power
60	VSS	—	Ground
61	RF_TR_2_A	AVDD18	A, I/O
62	VSS	—	Ground
63	AVDD18	—	Power
64	AVDD18	—	Power
65	AVDD18	—	Power
66	VSS	—	Ground
67	RF_TR_5_A	AVDD18	A, I/O
68	VSS	—	Ground
69	AVDD18	—	Power

Table 4. Pin list by number – SDIO host interface for Wi-Fi...*continued*

Pin number	Pin name	Supply	Type
70	VSS	—	Ground
71	VPA	—	Power
72	VPA	—	Power
73	VSS	—	Ground
74	VSS	—	Ground
75	VSS	—	Ground
76	AVDD18	—	Power
77	AVDD18	—	Power
78	AVDD18	—	Power
79	VSS	—	Ground
80	AVDD18	—	Power
81	AVDD18	—	Power
82	AVDD18	—	Power
83	AVDD18	—	Power
84	XTAL_IN	AVDD18	A, I
85	XTAL_OUT	AVDD18	A, O
86	AVDD18	—	Power
87	CONFIG_HOST_BOOT[0]	AVDD18	I
88	DNC	—	DNC
89	DNC	—	DNC
90	DNC	—	DNC
91	DNC	—	DNC
92	DNC	—	DNC
93	DNC	—	DNC
94	DNC	—	DNC
95	PDn	AVDD18	I
96	VCORE	—	Power
97	GPIO[0]	VIO	I/O
98	GPIO[1]	VIO	I/O
99	GPIO[2]	VIO	I/O
100	GPIO[3]	VIO	I/O
101	GPIO[4]	VIO	I/O
102	VIO	—	Power
103	GPIO[5]	VIO	I/O
104	GPIO[6]	VIO	I/O
105	BUCK_SENSE	—	Power

Table 4. Pin list by number – SDIO host interface for Wi-Fi*...continued*

Pin number	Pin name	Supply	Type
106	BUCK_VOUT	—	Power
107	BUCK_VOUT	—	Power
108	BUCK_VIN	—	Power
109	BUCK_VIN	—	Power
110	GPIO[7]	VIO	I/O
111	VSS	—	Ground
112	VSS	—	Ground
113	AVDD18	—	Power
114	GPIO[8]	VIO	I/O
115	GPIO[9]	VIO	I/O
116	SD_CLK	VIO_SD	I
117	SD_CMD	VIO_SD	I
118	SD_DAT[0]	VIO_SD	I/O
119	SD_DAT[1]	VIO_SD	I/O
120	VIO_SD	—	Power
121	SD_DAT[2]	VIO_SD	I/O
122	SD_DAT[3]	VIO_SD	I/O
123	VCORE	—	Power
124	DNC	—	—
125	SD_HOST_INT	VIO_SD	O
126	GPIO[10]	VIO	I/O
127	VIO	—	Power
128	GPIO[11]	VIO	I/O
129	GPIO[12]	VIO	I/O
130	GPIO[13]	VIO	I/O
131	GPIO[14]	VIO	I/O
132	GPIO[15]	VIO	I/O
133	VCORE	—	Power
134	GPIO[16]	VIO	I/O
135	GPIO[17]	VIO	I/O
136	GPIO[18]	VIO	I/O
137	GPIO[19]	VIO	I/O
138	VIO	—	Power
139	GPIO[20]	VIO	I/O
140	GPIO[21]	VIO	I/O
141	GPIO[22]	VIO	I/O

Table 4. Pin list by number – SDIO host interface for Wi-Fi*...continued*

Pin number	Pin name	Supply	Type
142	GPIO[23]	VIO	I/O
143	AVDD18	—	Power
144	AVDD18	—	Power
145	AVDD18	—	Power
146	VSS	—	Ground
147	BRF_ANT	AVDD18	A, I/O
148	VSS	—	Ground

[1] Connect a 50 Ω to GND.

6.5 Pin description

6.5.1 Pin states

The pin states information provided in the tables includes:

- **No Pad Power State** indicates the state when there is no power
- **PwrDwn State** denotes the power-down state in the default configuration. Many pads have programmable power-down values which can be set by firmware.
- **Reset State** is the state after the power-on-reset state and before the hardware state (HW State)
- **HW State** (hardware state) is the state after the boot code finishes and before the firmware download begins (firmware may change the pin state). HW State may differ based on the pin muxing/configuration setting.
- **PwrDwn Prog** indicates if the power-down state can be programmed
- **Internal PU/PD** columns indicates the following:
  - Type of PU/PD (weak vs nominal)
  - The polarity (PU vs. PD)

  The internal pull-up or pull-down applies when the pin is in input mode
- **PU** denotes whether the pull-up can be programmed or not
- **PD** denotes whether the pull-down can be programmed or not
- Pull-up and pull-down are only effective when the pad is in input mode
- At the end of the firmware download, the pads (for example GPIO and RF control) are programmed in the functional mode corresponding to the functionality of the pins

6.5.2 General purpose I/O (GPIO)

Table 5. General purpose I/O (MFP)

Pins may be Multi-Functional Pins (MFP). See the pin descriptions for functional modes.

<table>
<tr><th>Pin name</th><th>Supply</th><th>No Pad Power State[1]</th><th>Reset state</th><th>HW state</th><th>PwrDwn state</th><th>PwrDwn prog</th><th>Internal PU/ PD</th><th>PU</th><th>PD</th></tr>
<tr><td>GPIO[31]</td><td>VIO_RF</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[31] (input/output)</td></tr>
<tr><td>GPIO[30]</td><td>VIO</td><td>tristate</td><td>output high</td><td>output high</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[30] (input/output)
JTAG mode: JTAG_TDO - JTAG test data (output) (default mode). See Section 6.5.19 "JTAG interface".</td></tr>
<tr><td>GPIO[29]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[29] (input/output)
JTAG mode: JTAG_TDI - JTAG test data (input). See Section 6.5.19 "JTAG interface".
Bluetooth PCM mode - LE_PCM_SYNC2 - PCM sync pulse signal (input). Alternate assignment of LE_PCM_SYNC1 (GPIO[2]. See Section 6.5.8 "Digital audio interface".</td></tr>
<tr><td>GPIO[28]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[28] (input/output)
JTAG mode: JTAG_TMS - JTAG test mode select (input) (default mode). See Section 6.5.19 "JTAG interface".</td></tr>
<tr><td>GPIO[27]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[27] (input/output)
JTAG mode: JTAG_TCK - JTAG clock (input). See Section 6.5.19 "JTAG interface".</td></tr>
<tr><td>GPIO[26]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[26] (input/output)
UART coexistence mode: COEX_UART_SOUT - Coexistence UART transmit serial data (output). See Section 6.5.11 "UART coexistence interface".
WCI-2 coexistence mode: WCI-2_SIN - WCI-2 receive serial data (input). See Section 6.5.10 "WCI-2 coexistence interface".</td></tr>
<tr><td>GPIO[25]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[25] (input/output)
UART coexistence mode: COEX_UART_SIN - Coexistence UART receive serial data (input) . See Section 6.5.11 "UART coexistence interface".
WCI-2 coexistence mode: WCI-2_SOUT - WCI-2 transmit serial data (output). See Section 6.5.10 "WCI-2 coexistence interface".</td></tr>
<tr><td>GPIO[24]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[24] (input/output)
TSF host clock sync mode: MCU_TSF_SYNC – TSF clock synchronization indication to MCU (input)</td></tr>
<tr><td>GPIO[23]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[23] (input/output)
Narrowband trigger mode: NB1_HOST_TRIG1 - Host_Trigger pin 1 (input/output) for the narrowband (Bluetooth) and host</td></tr>
</table>

Table 5. General purpose I/O (MFP) *...continued*

Pins may be Multi-Functional Pins (MFP). See the pin descriptions for functional modes.

<table>
<tr><th>Pin name</th><th>Supply</th><th>No Pad Power State[1]</th><th>Reset state</th><th>HW state</th><th>PwrDwn state</th><th>PwrDwn prog</th><th>Internal PU/ PD</th><th>PU</th><th>PD</th></tr>
<tr><td>GPIO[22]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[22] (input/output)
Narrowband trigger mode: NB1_HOST_TRIG0 - Host_Trigger pin 0 (input/output) for the narrowband (Bluetooth) and host</td></tr>
<tr><td>GPIO[21]</td><td>VIO</td><td>tristate</td><td>input</td><td>input/output high</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[21] (input/output)
UART interface mode: UART_SOUT - UART transmit serial data (output). See Section 6.5.7 "UART host interface".</td></tr>
<tr><td>GPIO[20]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[20] (input/output)
UART interface mode: UART_SIN - UART receive serial data (input). See Section 6.5.7 "UART host interface".</td></tr>
<tr><td>GPIO[19]</td><td>VIO</td><td>tristate</td><td>input</td><td>input/output high</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[19] (input/output)
UART interface mode: UART_RTSn - UART request-to-send (output). See Section 6.5.7 "UART host interface".</td></tr>
<tr><td>GPIO[18]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[18] (input/output)
UART interface mode: UART_CTSn - UART clear-to-send (input). See Section 6.5.7 "UART host interface".</td></tr>
<tr><td>GPIO[17]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[17] (input/output)
TSF clock sync mode: TSF clock synchronization indication to host from the Wi-Fi subsystem (output).</td></tr>
<tr><td>GPIO[16]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">Wake-up/interrupt mode: NB_WAKE_IN – Bluetooth wake-up signal (input). See Section 6.5.13 "Wake-up/interrupt interface".</td></tr>
<tr><td>GPIO[15]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[15] (input/output)
PTA coexistence mode: EXT_GNT - External radio grant signal (output). See Section 6.5.9 "PTA coexistence interface".</td></tr>
<tr><td>GPIO[14]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[14] (input/output)
PTA coexistence mode: EXT_FREQ - External radio frequency signal (input). See Section 6.5.9 "PTA coexistence interface".
Debug UART mode: DBG_UART_SIN - Debug UART signal for Wi-Fi (input). See Section 6.5.12 "Debug UART interface".</td></tr>
<tr><td>GPIO[13]</td><td>VIO</td><td>tristate</td><td>input</td><td>input</td><td>tristate</td><td>yes</td><td>weak PU</td><td>yes</td><td>yes</td></tr>
<tr><td colspan="10">GPIO mode: GPIO[13] (input/output)
PTA coexistence interface mode: EXT_STATE (input). See Section 6.5.9 "PTA coexistence interface".
Debug UART mode: DBG_UART_SOUT - Debug UART signal for Wi-Fi (output). See Section 6.5.12 "Debug UART interface".</td></tr>
</table>

Table 5. General purpose I/O (MFP) *...continued*

Pins may be Multi-Functional Pins (MFP). See the pin descriptions for functional modes.

Pin name	Supply	No Pad Power State[1]	Reset state	HW state	PwrDwn state	PwrDwn prog	Internal PU/ PD	PU	PD
GPIO[12]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[12] (input/output) **PTA coexistence interface mode**: EXT_PRI (input). See Section 6.5.9 "PTA coexistence interface". **WCI-2 coexistence mode**: WCI-2_SIN (input). See Section 6.5.10 "WCI-2 coexistence interface". **Debug UART mode**: DBG_UART_SIN - Alternate Debug UART signal for Wi-Fi (input). See Section 6.5.12 "Debug UART interface".									
GPIO[11]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[11] (input/output) **PTA coexistence interface mode**: EXT_REQ (input). See Section 6.5.9 "PTA coexistence interface". **WCI-2 coexistence mode**: WCI-2_SOUT (output). See Section 6.5.10 "WCI-2 coexistence interface". **Debug UART mode**: DBG_UART_SOUT - Alternate debug UART signal for Wi-Fi (output). See Section 6.5.12 "Debug UART interface".									
GPIO[10]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[10] (input/output) **Wake-up/interrupt mode**: NB_WAKE_OUT – Bluetooth out-of-band wake-up signal to host (output). See Section 6.5.13 "Wake-up/interrupt interface".									
GPIO[9]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[9] (input/output) **Wake-up/interrupt mode**: WLAN_WAKE_OUT – Wi-Fi out-of-band wake-up signal to host (output). See Section 6.5.13 "Wake-up/interrupt interface".									
GPIO[8]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[8] (input/output) **Wake-up/interrupt mode**: WLAN_WAKE_IN – Wi-Fi out-of-band wake-up signal (input). See Section 6.5.13 "Wake-up/interrupt interface".									
GPIO[7]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[7] (input/output) **LED mode**: LED_OUT_BT (output) - LED indication for Bluetooth activity **Reset recovery mode**: WLAN_RST - Independent software reset for Wi-Fi (input). See Section 6.5.14 "Software reset interface".									
GPIO[6]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[6] (input/output) **Bluetooth PCM mode**: PCM_DIN - PCM receive data signal (input). See Section 6.5.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_DIN - I2S receive data signal (input). See Section 6.5.8 "Digital audio interface".									
GPIO[5]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[5] (input/output) **Bluetooth PCM mode:** PCM_DOUT - PCM transmit data signal (output). See Section 6.5.8 "Digital audio interface". **Bluetooth I2S mode:** I2S_DOUT - I2S transmit data signal (output). See Section 6.5.8 "Digital audio interface".									

Table 5. General purpose I/O (MFP) *...continued*

Pins may be Multi-Functional Pins (MFP). See the pin descriptions for functional modes.

Pin name	Supply	No Pad Power State[1]	Reset state	HW state	PwrDwn state	PwrDwn prog	Internal PU/ PD	PU	PD
GPIO[4]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[4] (input/output) **Bluetooth PCM mode**: PCM_CLK - PCM data clock (output if central, input if peripheral). See Section 6.5.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_BCLK - I2S audio bit clock (output if central, input if peripheral). See Section 6.5.8 "Digital audio interface".									
GPIO[3]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[3] (input/output) **Bluetooth I2S mode**: I2S_CCLK - I2S clock output signal (optional). See Section 6.5.8 "Digital audio interface". **Bluetooth PCM mode**: PCM_MCLK - PCM clock output signal (optional). See Section 6.5.8 "Digital audio interface". **LED mode**: LED_OUT_WLAN (output) - LED indication of Wi-Fi activity									
GPIO[2]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[2] (input/output) **Bluetooth PCM mode**: PCM_SYNC - PCM frame sync (output if central, input if peripheral). See Section 6.5.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_LRCLK - I2S left/right clock (output if central, input if peripheral). See Section 6.5.8 "Digital audio interface". **Bluetooth PCM mode** - LE_PCM_SYNC1 - PCM sync pulse signal (input). Alternate assignment of LE_PCM_SYNC2 (GPIO[29] . See Section 6.5.8 "Digital audio interface".									
GPIO[1]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[1] (input/output) **Reset recovery mode**: NB_RST - Independent software reset for Bluetooth subsystem (input). See Section 6.5.14 "Software reset interface".									
GPIO[0]	VIO	tristate	output	output high	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[0] (input/output)									

[1] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).

6.5.3 RF front-end control interface

Table 6. RF front-end control interface[1]

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/ PD	PU	PD
RF_CNTL0	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control mode: RF control 0 - RF control line 0 used to control the front-end module (FEM)									
RF_CNTL1	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control mode: RF control 1 - RF control line 1 used to control the front-end module (FEM)									
RF_CNTL2	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 2 — RF control line 2									
RF_CNTL3	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 3 — RF control line 3									
RF_CNTL4	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 4 — RF control line 4									
RF_CNTL5	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 5 — RF control line 5									
RF_CNTL6	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 6 — RF control line 6									
RF_CNTL7	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 7 — RF control line 7									
RF_CNTL8	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 8— RF control line 8									
RF_CNTL9	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 9 — RF control line 9									
RF_CNTL10	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 10 — RF control line 10									
RF_CNTL11	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 11 — RF control line 11									
RF_CNTL12	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 12 — RF control line 12									
RF_CNTL13	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 13 — RF control line 13									
RF_CNTL14	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 14 — RF control line 14									
RF_CNTL15	VIO_RF	tristate	output low	output low	drive low	yes	weak PU	yes	yes
RF control 15 — RF control line 15									

[1] Maximum input voltage is 0.4V when VIO_RF has no power (or in uncertain situations).

6.5.4 Wi-Fi radio interface

Table 7. Wi-Fi radio interface

Pin name	Type	Supply	Description
RF_TR_2_A	A, I/O	AVDD18	Wi-Fi transmit/receive path A (2.4 GHz)
RF_TR_2_B	A, I/O	AVDD18	Wi-Fi transmit/receive path B (2.4 GHz)
RF_TR_5_A	A, I/O	AVDD18	Wi-Fi transmit/receive path A (5-7 GHz)
RF_TR_5_B	A, I/O	AVDD18	Wi-Fi transmit/receive path B (5-7 GHz)

6.5.5 Bluetooth radio interface

Table 8. Bluetooth radio interface

Pin name	Type	Supply	Description
BRF_ANT	A, I/O	AVDD18	Bluetooth radio transmit/receive interface

6.5.6 SDIO host interface

Table 9. SDIO host interface

Pin Name	Supply	No Pad Power State[1]	Reset state	HW state	PwrDwn state	PwrDwn prog	Internal PU/ PD	PU	PD
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Clock input									
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Command/response (input/output)									
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[3]									
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[2] or read wait (optional)									
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[1]									
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[0]									
SD_HOST_ INT	VIO_SD	tristate	input	input	tristate	yes	weak PU	yes	yes
Interrupt mode: interrupt signal to host									

[1] Maximum input voltage is 0.4V when VIO_SD has no power (or in uncertain situations).

6.5.7 UART host interface

Table 10. UART host interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
UART_SIN	I	VIO	UART serial input signal - Muxed with GPIO[20]
UART_SOUT	O	VIO	UART serial output signal - Muxed with GPIO[21]
UART_RTSn	O	VIO	UART request-to-send output signal - Active low - Muxed with GPIO[19]
UART_CTSn	I	VIO	UART clear-to-send input signal - Active low - Muxed with GPIO[18]

6.5.8 Digital audio interface

Table 11. Audio interface pins

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
PCM_DIN	I	VIO	PCM audio codec output data (for recording) - Muxed with GPIO[6]
PCM_DOUT	O	VIO	PCM audio codec input data (for playback) - Muxed with GPIO[5]
PCM_SYNC	I/O	VIO	PCM sync pulse signal - Muxed with GPIO[2] . Central mode: output . Peripheral mode: input
PCM_CLK	I/O	VIO	PCM clock signal - Muxed with GPIO[4] . Central mode: output . Peripheral mode: input
PCM_MCLK	O	VIO	PCM clock output signal (optional) - Muxed with GPIO[3] Optional clock used for some codecs. Derived from PCM_CLK.
LE_PCM_SYNC1	I	VIO	Bluetooth LE PCM sync pulse signal for Bluetooth LE audio function (input). Muxed with GPIO[2]
LE_PCM_SYNC2	I	VIO	Bluetooth LE PCM sync pulse signal for Bluetooth LE audio function (input). Alternate assignment of PCM_SYNC1. Muxed with GPIO[29]
I2S_DIN	I	VIO	I2S audio codec output data (for recording) - Muxed with GPIO[6]
I2S_DOUT	O	VIO	I2S audio codec input data (for playback) - Muxed with GPIO[5]
I2S_BCLK	I/O	VIO	I2S audio bit clock - Muxed with GPIO[4] . Central mode: output . Peripheral mode: input
I2S_LRCLK	I/O	VIO	I2S audio left/right clock - Muxed with GPIO[2] . Central mode: output . Peripheral mode: input
I2S_CCLK	O	VIO	I2S codec main clock (optional) - Muxed with GPIO[3] Optional clock used for some codecs. Derived from I2S_BCLK.

6.5.9 PTA coexistence interface

Table 12. PTA coexistence interface (MFP)

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
EXT_STATE	I	VIO	External radio state input signal (optional) - muxed with GPIO[13]. See Section 6.5.3 "RF front-end control interface". External radio traffic direction (TX/RX): • 1: TX (default) • 0: RX
EXT_GNT	O	VIO	External radio grant output signal (mandatory) - muxed with GPIO[15]
EXT_FREQ	I	VIO	External radio frequency input signal (optional) - muxed with GPIO[14]. See Section 6.5.3 "RF front-end control interface". Frequency overlap between external radio and Wi-Fi: • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
EXT_PRI	I	VIO	External radio input priority signal (optional) - muxed with GPIO[12] Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also have TX/RX info following the priority info if EXT_STATE is not used.
EXT_REQ	I	VIO	Request from the external radio (mandatory) - muxed with GPIO[11]

6.5.10 WCI-2 coexistence interface

Table 13. WCI-2 coexistence interface - Option 1

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
WCI-2_SOUT	O	VIO	WCI-2 output signal - muxed with GPIO[11]. See Section 6.5.2 "General purpose I/O (GPIO)".
WCI-2_SIN	I	VIO	WCI-2 input signal - muxed with GPIO[12]. See Section 6.5.2 "General purpose I/O (GPIO)".

Table 14. WCI-2 coexistence interface - Option 2

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
WCI-2_SOUT	O	VIO	WCI-2 output signal - muxed with GPIO[25]. See Section 6.5.2 "General purpose I/O (GPIO)".
WCI-2_SIN	I	VIO	WCI-2 input signal - muxed with GPIO[26]. See Section 6.5.2 "General purpose I/O (GPIO)".

6.5.11 UART coexistence interface

Table 15. UART coexistence interface

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
COEX_UART_SOUT	O	VIO	COEX_UART output signal - muxed with GPIO[26]. See Section 6.5.2 "General purpose I/O (GPIO)".
COEX_UART_SIN	I	VIO	COEX_UART input signal - muxed with GPIO[25]. See Section 6.5.2 "General purpose I/O (GPIO)".

6.5.12 Debug UART interface

Table 16. Debug UART coexistence interface - Option 1

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
DBG_UART_SOUT	O	VIO	DBG_UART output signal - muxed with GPIO[13]. See Section 6.5.2 "General purpose I/O (GPIO)".
DBG_UART_SIN	I	VIO	DBG_UART input signal - muxed with GPIO[14]. See Section 6.5.2 "General purpose I/O (GPIO)".

Table 17. Debug UART coexistence interface - Option 2

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
DBG_UART_SOUT	O	VIO	DBG_UART output signal - muxed with GPIO[11]. See Section 6.5.2 "General purpose I/O (GPIO)".
DBG_UART_SIN	I	VIO	DBG_UART input signal - muxed with GPIO[12]. See Section 6.5.2 "General purpose I/O (GPIO)".

6.5.13 Wake-up/interrupt interface

Table 18. Wake-up/interrupt interface

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
NB_WAKE_IN	I	VIO	Bluetooth out-of-band wake-up signal (input) - muxed with GPIO[16]. See Section 6.5.2 "General purpose I/O (GPIO)".
NB_WAKE_OUT	O	VIO	Bluetooth out-of-band wake-up signal to host (output) - muxed with GPIO[10]. See Section 6.5.2 "General purpose I/O (GPIO)".
WLAN_WAKE_IN	I	VIO	Wi-Fi out-of-band wake-up signal (input) - muxed with GPIO[8]. See Section 6.5.2 "General purpose I/O (GPIO)".
WLAN_WAKE_OUT	O	VIO	Wi-Fi out-of-band wake-up signal to host (output) - muxed with GPIO[9]. See Section 6.5.2 "General purpose I/O (GPIO)".

6.5.14 Software reset interface

Table 19. Software reset interface

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin name	Type	Supply	Description
WLAN_RST	O	VIO	Independent software reset for Wi-Fi (input) - muxed with GPIO[7]. See Section 6.5.2 "General purpose I/O (GPIO)".
NB_RST	O	VIO	Independent software reset for Bluetooth (input) - muxed with GPIO[1]. See Section 6.5.2 "General purpose I/O (GPIO)".

6.5.15 Host configuration

Table 20. Host configuration

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
CONFIG_ HOST_BOOT[0]	AVDD18	tristate	input	input	tristate	no	weak PD	yes	yes
CONFIG_HOST_BOOT[0]: see Section 6.6 "Configuration pins "									

6.5.16 Clock interface

Table 21. Clock interface

Pin Name	Supply	No Pad Power State[1]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
XTAL_IN	AVDD18	—	—	—	—	—	—	—	—
Reference clock input signal. The reference clock signal frequency must be 40 MHz from an external crystal or external crystal oscillator. To achieve lower power consumption in sleep mode, it is recommended to use an external crystal instead of an external crystal oscillator. See Section 11.8 "Reference clock specifications".									
XTAL_OUT	AVDD18	—	—	—	—	—	—	—	—
Reference clock output signal. Connect this pin to an external crystal when an external crystal is used. When an external crystal oscillator is used, connect this pin to ground with resistance less than 100 Ω.									

[1] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).

6.5.17 Power down pin

Table 22. Power down pin

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/ PD	PU	PD
PDn	AVDD18	n/a	n/a	n/a	n/a	n/a	weak PD	n/a	n/a
Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.8V to 4.5V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin. This pin has an always-on internal weak pull-down.									

6.5.18 Power supply and ground pins

Table 23. Power supply and ground pins

Pin name	Type	Description
VCORE	Power	1.05V core power supply
VIO	Power	1.8V/3.3V digital I/O power supply
VIO_SD	Power	1.8V/3.3V Digital I/O SDIO Power Supply
VIO_RF	Power	1.8V/3.3V digital I/O RF power supply
AVDD18	Power	1.8V analog power supply
VPA	Power	PA power supply See Section 9 "Recommended operating conditions"
BUCK_VIN	Power	Internal buck voltage input See Section 9 "Recommended operating conditions"
BUCK_VOUT	Power	Internal buck voltage output See Internal buck connections in Section 7.1.
BUCK_SENSE	Power	Internal buck voltage sense This pin senses the output voltage of the internal Buck. See internal buck connections in Section 7.1.
VSS	Ground	Ground
DNC	DNC	Do Not Connect Do not connect these pins. Leave these pins floating.

6.5.19 JTAG interface

Table 24. JTAG interface pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
JTAG_TDO	O	VIO	JTAG test data output signal - Muxed with GPIO[30]
JTAG_TDI	I	VIO	JTAG test data input signal - Muxed with GPIO[29]
JTAG_TMS	I	VIO	JTAG test mode select input signal - Muxed with GPIO[28]
JTAG_TCK	I	VIO	JTAG test clock input signal - Muxed with GPIO[27]

6.6 Configuration pins

Table 25 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function.

To set a configuration bit to 0, attach a 51 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

External circuitry that shares functionality with the configuration pins after a device reset must not pull the configuration pins to undesired values/states as this will change the post-reset behavior of the device.

Table 25. Configuration pins

Configuration bits	Pin name	Configuration function
CON[13]	GPIO[23]	Reserved. Do not connect.
CON[12]	GPIO[22]	Reserved. Do not connect.
CON[10]	GPIO[6]	Reserved. Do not connect.
CON[9]	GPIO[5]	Reserved. Do not connect.
CON[8]	GPIO[4]	Reserved. Do not connect.
CON[3]	GPIO[24]	Reserved. Do not connect.
CON[0]	CONFIG_HOST_ BOOT[0]	Host configuration options Selects the host interface used for Wi-Fi and Bluetooth. See Table 26.

Table 26. Host configuration options for IW623S

CONFIG_HOST_BOOT[0]	Wi-Fi	Bluetooth/ Bluetooth LE
1	SDIO	UART
0	Reserved	Reserved

7 Power information

7.1 Internal buck regulator

VCORE must be supplied by the internal buck regulator. The following figure shows the application circuit for VCORE supply using the internal Buck regulator. The power inductor in the application is chosen to maximize the internal Buck efficiency.

Note: *In Figure 17, Wireless SoC is IW623S.*

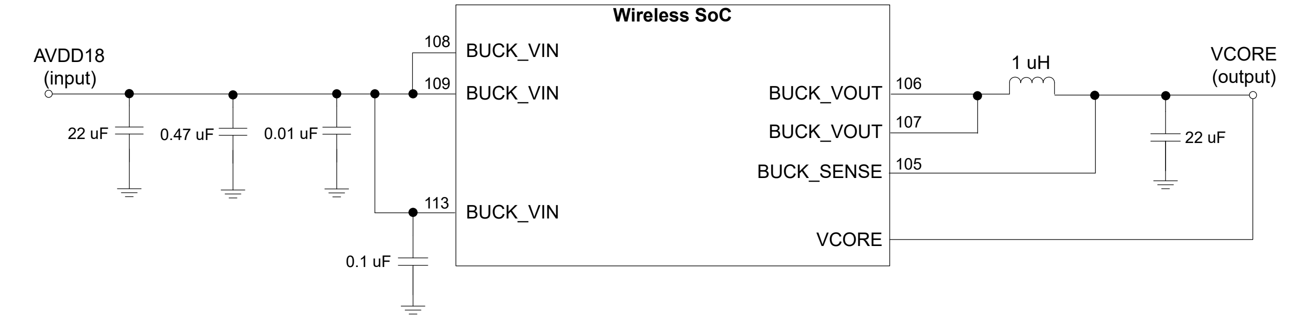


Figure 17. Internal buck connections

Deep-sleep mode

When the internal Buck is used to supply VCORE, the VCORE level can be reduced to approximately 0.8 V to reduce power consumption in deep sleep mode.

7.2 Power-up sequence

The IW623S does not have power-up sequence requirements. The power-down pin (PDn) must be held low (asserted) until all power supply rails are stable. The following figures and tables are recommendations.

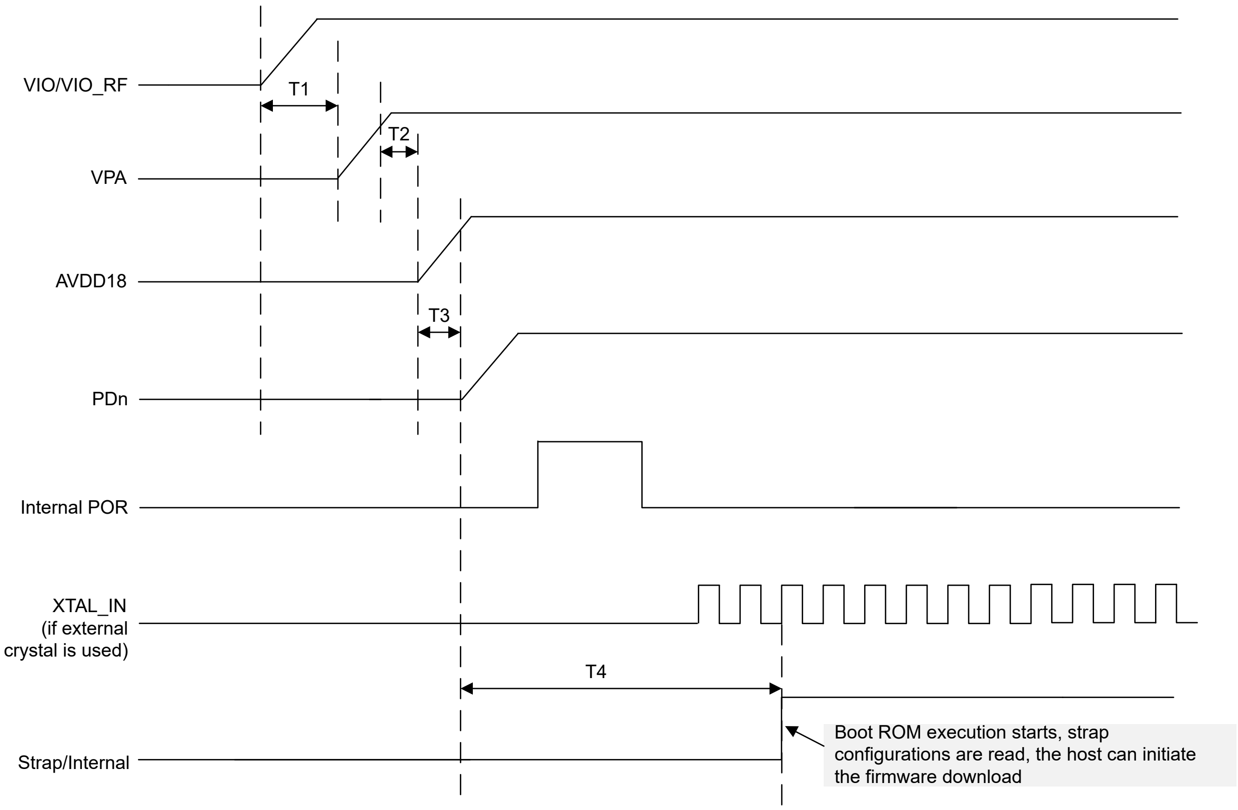


Figure 18. Power-up timing diagram – Internal PA (VPA/VIO/VIO_RF = 3.3 V)

Table 27. Power-up timing parameters – Internal PA (VPA/VIO/VIO_RF = 3.3 V)[1]

Symbol	Description	Min	Typ	Max	Unit
T1	Delay from start of VIO/VIO_RF ramp-up to start of VPA ramp-up	0	—	—	ms
T2	Delay from VPA high (at least 90%) to start of AVDD18 ramp-up	0	100	—	ms
T3	Delay from start of AVDD18 ramp-up to start of PDn ramp-up	0	—	—	ms
T4	Delay from AVDD18 high (90%) to start of Boot ROM	—	10	—	ms

[1] The ramp-up time of VIO/VIO_RF, VPA and AVDD18 must be less than 100 ms.
All supplies must be monotonic.
If using an external crystal oscillator, the reference clock must be stable before PDn ramps up.

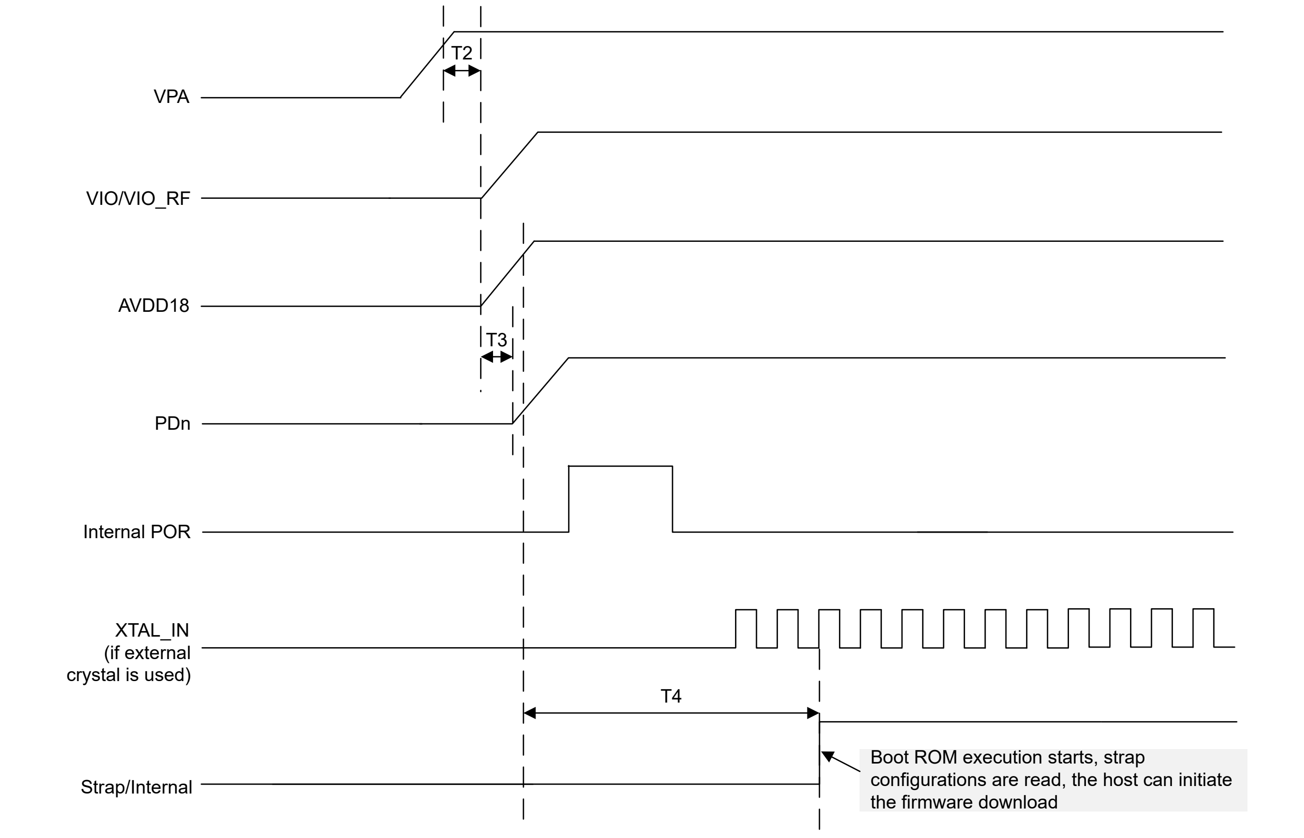


Figure 19. Power-up timing diagram – Internal PA (VIO/VIO_RF = 1.8 V, VPA = 3.3 V)

Table 28. Power-up timing parameters – Internal PA (VIO/VIO_RF = 1.8 V, VPA = 3.3 V)[1]

Symbol	Description	Min	Typ	Max	Unit
T2	Delay from VPA high (at least 90%) to start of AVDD18 ramp-up	0	100	—	ms
T3	Delay from start of AVDD18 ramp-up to start of PDn ramp-up	0	—	—	ms
T4	Delay from AVDD18 high (90%) to start of Boot ROM	—	10	—	ms

[1] The ramp-up time of VIO/VIO_RF, VPA and AVDD18 must be less than 100 ms.
All supplies must be monotonic.
If using an external crystal oscillator, the reference clock must be stable before PDn ramps up.

7.3 Power-down sequence

PDn must be discharged to less than 0.2 V before Power-On Reset (POR) is triggered again.

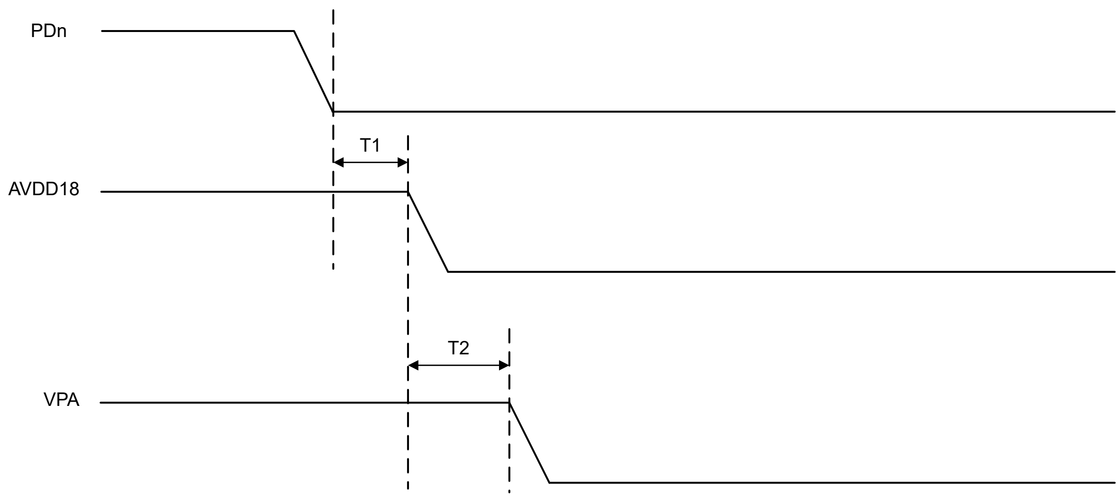


Figure 20. Power-down timing diagram when using internal PA (VPA = 3.3 V)

Table 29. Power-down timing parameters - when using internal PA

Symbol	Description	Min	Typ	Max	Units
T1	Recommended delay from PDn low (less than 0.2V) to start of AVDD18 ramp-down	0	—	—	ms
T2	Recommended delay from start of AVDD18 ramp-down to start of VPA ramp-down	0	—	—	ms

7.4 Reset

The IW623S is reset to its default operating state under any of the following conditions:

- Internal Power-On Reset (POR): POR is triggered when the device receives power and VCORE and AVDD18 supplies are good. See Section 7.2.
- Software/Firmware reset: software/firmware issues a reset.
- External PDn pin assertion: the device is reset when the PDn input pin is <0.2V and transitions from low to high.

See Section 11.9 "Power-down specifications" for the electrical specifications.

Lowest power state

The device can be put into the lowest power mode of operation to conserve energy when Wi-Fi and Bluetooth are not in use.

To put the device in the lowest power mode, assert PDn low to enter power-down mode. Once PDn is de-asserted, the power sequence must be followed. If the firmware is not downloaded, the device must be kept in power-down mode to reduce leakage.

8 Absolute maximum ratings

CAUTION: The absolute maximum ratings table defines the limitation for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 30. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCORE[1]	1.05V core power supply	—	1.21	V
VIO	1.8V/3.3V digital I/O power supply	—	2.16	V
		—	3.96	V
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	—	2.16	V
		—	3.96	V
VIO_RF	1.8V/3.3V I/O power supply	—	2.16	V
		—	3.96	V
AVDD18	1.8V analog power supply	—	2.16	V
VPA	3.3V analog power supply	—	3.96	V
BUCK_VIN	Buck input power supply	—	2.16	V
$T_{STORAGE}$	Storage temperature	-55	+125	°C

[1] VCORE must be powered from the internal buck as shown in the figure in Section 7.1.

Table 31. Limiting values

Symbol	Parameter[1]	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)	-2	+2	kV
		charged device model (CDM)– all pins except pins number 30 and 82	-500	+500	V
		charged device model (CDM) – Pin number 30 (AVDD18) and pin number 82 (AVDD18)	-400	+400	V
		charged device model (CDM) – corner pins	-750	+750	V

[1] HBM values according to AEC-Q100-002.
CDM values according to AEC-Q100-011.

9 Recommended operating conditions

Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Table 32. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCORE [1]	1.05V core power supply	—	1.025	—	1.155	V
VIO	1.8V/3.3V digital I/O power supply	—	1.71	1.8	1.89	V
			3.14	3.3	3.46	V
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	—	1.71	1.8	1.89	V
			3.14	3.3	3.46	V
VIO_RF	1.8V/3.3V I/O power supply	—	1.71	1.8	1.89	V
			3.14	3.3	3.46	V
AVDD18	1.8V analog power supply	—	1.71	1.8	1.89	V
VPA	3.3V analog power supply	—	3.14	3.3	3.46	V
BUCK_VIN	Buck input power supply	—	1.71	1.8	1.89	V
T_A	Ambient operating temperature	Industrial	-40	—	85	°C
T_J	Maximum junction temperature	—	—	—	125	°C

[1] VCORE must be powered from the internal Buck as shown in the figure in Section 7.1.

10 Radio specifications

10.1 Wi-Fi radio specifications

10.1.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port with Wi-Fi radio interface pins.

Note: *In Figure 21, Wireless SoC is IW623S.*

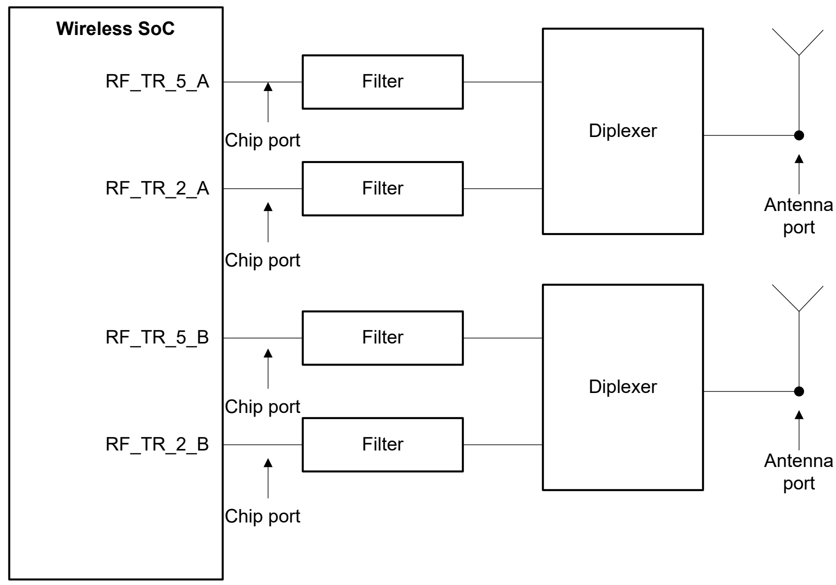


Figure 21. RF performance measurement points

10.1.2 2.4 GHz Wi-Fi receiver performance – 2A/2B RF paths

Note: *Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and at RF_TR_2_A/ RF_TR_2_B pin.*

Table 33. 2.4 GHz Wi-Fi receiver performance – 2A/2B RF paths

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	2.4 GHz	2400	—	2483	MHz
Receiver sensitivity SISO, NRx = 1, Nss = 1					
Receiver sensitivity (1 x 1)	802.11b, 20 MHz, 1 Mbps	—	-99.75	—	dBm
Receiver sensitivity (1 x 1)	802.11b, 20 MHz, 11 Mbps	—	-91.75	—	dBm
Receiver sensitivity (1 x 1)	802.11g, 20 MHz, 6 Mbps	—	-95.75	—	dBm
Receiver sensitivity (1 x 1)	802.11g, 20 MHz, 54 Mbps	—	-78.25	—	dBm
Receiver sensitivity (1 x 1)	802.11n, 20 MHz, MCS0 Nss1 BCC	—	-94.50	—	dBm
Receiver sensitivity (1 x 1)	802.11n, 20 MHz, MCS7 Nss1 BCC	—	-75.50	—	dBm
Receiver sensitivity (1 x 1)	802.11n, 40 MHz, MCS0 Nss1 BCC	—	-91.75	—	dBm
Receiver sensitivity (1 x 1)	802.11n, 40 MHz, MCS7 Nss1 BCC	—	-73.00	—	dBm
Receiver sensitivity (1 x 1)	802.11ac, 20 MHz, MCS0 Nss1 LDPC	—	-95.00	—	dBm
Receiver sensitivity (1 x 1)	802.11ac, 20 MHz, MCS7 Nss1 LDPC	—	-77.75	—	dBm
Receiver sensitivity (1 x 1)	802.11ac, 20 MHz, MCS8 Nss1 LDPC	—	-73.75	—	dBm
Receiver sensitivity (1 x 1)	802.11ac, 40 MHz, MCS0 Nss1 LDPC	—	-92.00	—	dBm
Receiver sensitivity (1 x 1)	802.11ac, 40 MHz, MCS7 Nss1 LDPC	—	-75.00	—	dBm
Receiver sensitivity (1 x 1)	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	-69.50	—	dBm
Receiver sensitivity (1 x 1)	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x + 3.2	—	-95.25	—	dBm
Receiver sensitivity (1 x 1)	802.11ax, 20 MHz, MCS11 Nss1 LDPC4x + 3.2	—	-65.75	—	dBm
Receiver sensitivity (1 x 1)	802.11ax, 40 MHz, MCS0 Nss1 LDPC4x + 3.2	—	-92.50	—	dBm
Receiver sensitivity (1 x 1)	802.11ax, 40 MHz, MCS11 Nss1 LDPC4x + 3.2	—	-63.50	—	dBm
Receiver sensitivity MIMO, NRx = 2, Nss = 1					
Receiver sensitivity (1 x 2)	802.11b, 20 MHz, 1 Mbps	—	-103.00	—	dBm
Receiver sensitivity (1 x 2)	802.11b, 20 MHz, 11 Mbps	—	-92.00	—	dBm
Receiver sensitivity (1 x 2)	802.11g, 20 MHz, 6 Mbps	—	-97.75	—	dBm
Receiver sensitivity (1 x 2)	802.11g, 20 MHz, 54 Mbps	—	-81.25	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 20 MHz, MCS0 Nss1 BCC	—	-96.50	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 20 MHz, MCS7 Nss1 BCC	—	-79.00	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 40 MHz, MCS0 Nss1 BCC	—	-94.00	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 40 MHz, MCS7 Nss1 BCC	—	-76.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 20 MHz, MCS0 Nss1 LDPC	—	-97.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 20 MHz, MCS7 Nss1 LDPC	—	-81.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 20 MHz, MCS8 Nss1 LDPC	—	-77.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 40 MHz, MCS0 Nss1 LDPC	—	-94.00	—	dBm

Table 33. 2.4 GHz Wi-Fi receiver performance – 2A/2B RF paths*...continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver sensitivity (1 x 2)	802.11ac, 40 MHz, MCS7 Nss1 LDPC	—	-78.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	-73.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x + 3.2	—	-97.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS11 Nss1 LDPC4x + 3.2	—	-69.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS0 Nss1 LDPC4x + 3.2	—	-95.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS11 Nss1 LDPC4x + 3.2	—	-67.00	—	dBm
Receiver maximum input level (MIL) - SISO, NRx = 1, Nss = 1					
Receiver maximum input level DSSS	802.11b DSSS MIL	—	-3.40	—	dBm
Receiver maximum input level CCK	802.11b CCK MIL	—	-3.40	—	dBm
Receiver maximum input level OFDM	OFDM MIL	—	-12.90	—	dBm
Receiver adjacent channel interference (ACI) - NRx = 1, Nss = 1					
Receiver ACI	802.11b, 20 MHz, 1 Mbps	—	53.00	—	dB
Receiver ACI	802.11b, 20 MHz, 11 Mbps	—	45.50	—	dB
Receiver ACI	802.11g, 20 MHz, 6 Mbps	—	31.00	—	dB
Receiver ACI	802.11g, 20 MHz, 54 Mbps	—	21.25	—	dB
Receiver ACI	802.11n, 20 MHz, MCS0 Nss1 BCC	—	38.00	—	dB
Receiver ACI	802.11n, 20 MHz, MCS7 Nss1 BCC	—	25.50	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	27.00	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS11 Nss1 LDPC4x+3.2	—	3.75	—	dB
Receiver alternative adjacent channel interference (AACI) - NRx = 1, Nss = 1					
Receiver AACI	802.11b, 20 MHz, 1 Mbps	—	53.00	—	dB
Receiver AACI	802.11b, 20 MHz, 11 Mbps	—	49.00	—	dB
Receiver AACI	802.11g, 20 MHz, 6 Mbps	—	46.25	—	dB
Receiver AACI	802.11g, 20 MHz, 54 Mbps	—	33.00	—	dB
Receiver AACI	802.11n, 20 MHz, MCS0 Nss1 BCC	—	49.00	—	dB
Receiver AACI	802.11n, 20 MHz, MCS7 Nss1 BCC	—	31.25	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	47.25	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS11 Nss1 LDPC4x+3.2	—	20.50	—	dB

10.1.3 5 GHz Wi-Fi receiver performance - 5A/5B RF paths

Note: *Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and at RF_TR_5_A/ RF_TR_5_B pin.*

Table 34. 5 GHz Wi-Fi receiver performance - 5A/5B RF paths

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	5 GHz	5180	—	5885	MHz
Receiver sensitivity SISO, NRx = 1, Nss = 1					
Receiver sensitivity (1x1)	802.11a, 20 MHz, 6 Mbps	—	-95.50	—	dBm
Receiver sensitivity (1x1)	802.11a, 20 MHz, 54 Mbps	—	-78.00	—	dBm
Receiver sensitivity (1x1)	802.11n, 20 MHz, MCS0 Nss1 BCC	—	-94.25	—	dBm
Receiver sensitivity (1x1)	802.11n, 20 MHz, MCS7 Nss1 BCC	—	-75.25	—	dBm
Receiver sensitivity (1x1)	802.11n, 40 MHz, MCS0 Nss1 BCC	—	-91.25	—	dBm
Receiver sensitivity (1x1)	802.11n, 40 MHz, MCS7 Nss1 BCC	—	-72.75	—	dBm
Receiver sensitivity (1x1)	802.11ac, 20 MHz, MCS0 Nss1 LDPC	—	-94.75	—	dBm
Receiver sensitivity (1x1)	802.11ac, 20 MHz, MCS7 Nss1 LDPC	—	-77.50	—	dBm
Receiver sensitivity (1x1)	802.11ac, 20 MHz, MCS8 Nss1 LDPC	—	-73.25	—	dBm
Receiver sensitivity (1x1)	802.11ac, 40 MHz, MCS0 Nss1 LDPC	—	-91.50	—	dBm
Receiver sensitivity (1x1)	802.11ac, 40 MHz, MCS7 Nss1 LDPC	—	-74.75	—	dBm
Receiver sensitivity (1x1)	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	-69.00	—	dBm
Receiver sensitivity (1x1)	802.11ac, 80 MHz, MCS0 Nss1 LDPC	—	-87.75	—	dBm
Receiver sensitivity (1x1)	802.11ac, 80 MHz, MCS7 Nss1 LDPC	—	-71.75	—	dBm
Receiver sensitivity (1x1)	802.11ac, 80 MHz, MCS9 Nss1 LDPC	—	-66.00	—	dBm
Receiver sensitivity (1x1)	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-94.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-71.00	—	dBm
Receiver sensitivity (1x1)	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-65.50	—	dBm
Receiver sensitivity (1x1)	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-92.00	—	dBm
Receiver sensitivity (1x1)	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-68.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-63.00	—	dBm
Receiver sensitivity (1x1)	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-88.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-65.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-59.75	—	dBm

Table 34. 5 GHz Wi-Fi receiver performance - 5A/5B RF paths...*continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver sensitivity MIMO, NRx = 2, Nss = 1					
Receiver sensitivity (1 x 2)	802.11a, 20 MHz, 6 Mbps	—	-97.25	—	dBm
Receiver sensitivity (1 x 2)	802.11a, 20 MHz, 54 Mbps	—	-80.75	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 20 MHz, MCS0 Nss1 BCC	—	-96.00	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 20 MHz, MCS7 Nss1 BCC	—	-78.25	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 40 MHz, MCS0 Nss1 BCC	—	-92.75	—	dBm
Receiver sensitivity (1 x 2)	802.11n, 40 MHz, MCS7 Nss1 BCC	—	-75.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 20 MHz, MCS0 Nss1 LDPC	—	-96.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 20 MHz, MCS7 Nss1 LDPC	—	-80.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 20 MHz, MCS8 Nss1 LDPC	—	-76.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 40 MHz, MCS0 Nss1 LDPC	—	-93.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 40 MHz, MCS7 Nss1 LDPC	—	-77.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	-72.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 80 MHz, MCS0 Nss1 LDPC	—	-89.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 80 MHz, MCS7 Nss1 LDPC	—	-74.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ac, 80 MHz, MCS9 Nss1 LDPC	—	-69.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-96.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-74.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-68.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-93.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-72.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-66.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-90.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-68.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-63.25	—	dBm
Receiver adjacent channel interference (ACI) - NRx = 1, Nss = 1					
Receiver ACI	802.11a, 20 MHz, 6 Mbps	—	23.00	—	dB
Receiver ACI	802.11a, 20 MHz, 54 Mbps	—	15.00	—	dB
Receiver ACI	802.11n, 20 MHz, MCS0 Nss1 BCC	—	26.50	—	dB
Receiver ACI	802.11n, 20 MHz, MCS7 Nss1 BCC	—	9.75	—	dB
Receiver ACI	802.11n, 40 MHz, MCS0 Nss1 BCC	—	27.50	—	dB
Receiver ACI	802.11n, 40 MHz, MCS7 Nss1 BCC	—	13.00	—	dB
Receiver ACI	802.11ac, 20 MHz, MCS0 Nss1 LDPC	—	27.00	—	dB
Receiver ACI	802.11ac, 20 MHz, MCS9 Nss1 LDPC	—	15.00	—	dB
Receiver ACI	802.11ac, 40 MHz, MCS0 Nss1 LDPC	—	26.75	—	dB
Receiver ACI	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	10.00	—	dB

Table 34. 5 GHz Wi-Fi receiver performance - 5A/5B RF paths...*continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver ACI	802.11ac, 80 MHz, MCS0 Nss1 LDPC	—	24.50	—	dB
Receiver ACI	802.11ac, 80 MHz, MCS9 Nss1 LDPC	—	13.00	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	27.50	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	12.25	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	6.50	—	dB
Receiver ACI	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	27.00	—	dB
Receiver ACI	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	13.75	—	dB
Receiver ACI	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	8.75	—	dB
Receiver ACI	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	24.50	—	dB
Receiver ACI	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	14.50	—	dB
Receiver ACI	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	8.00	—	dB
Receiver alternative adjacent channel interference (AACI) - NRx = 1, Nss = 1					
Receiver AACI	802.11a, 20 MHz, 6 Mbps	—	45.25	—	dB
Receiver AACI	802.11a, 20 MHz, 54 Mbps	—	27.00	—	dB
Receiver AACI	802.11n, 20 MHz, MCS0 Nss1 BCC	—	45.00	—	dB
Receiver AACI	802.11n, 20 MHz, MCS7 Nss1 BCC	—	30.00	—	dB
Receiver AACI	802.11n, 40 MHz, MCS0 Nss1 BCC	—	43.00	—	dB
Receiver AACI	802.11n, 40 MHz, MCS7 Nss1 BCC	—	27.50	—	dB
Receiver AACI	802.11ac, 20 MHz, MCS0 Nss1 LDPC	—	45.25	—	dB
Receiver AACI	802.11ac, 20 MHz, MCS9 Nss1 LDPC	—	26.75	—	dB
Receiver AACI	802.11ac, 40 MHz, MCS0 Nss1 LDPC	—	43.00	—	dB
Receiver AACI	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	22.25	—	dB
Receiver AACI	802.11ac, 80 MHz, MCS0 Nss1 LDPC	—	42.75	—	dB
Receiver AACI	802.11ac, 80 MHz, MCS9 Nss1 LDPC	—	21.75	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	45.00	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	25.75	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	19.25	—	dB
Receiver AACI	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	44.25	—	dB
Receiver AACI	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	23.25	—	dB
Receiver AACI	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	16.25	—	dB
Receiver AACI	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	44.50	—	dB
Receiver AACI	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	24.75	—	dB
Receiver AACI	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	17.50	—	dB

10.1.4 6 GHz Wi-Fi receiver performance – 5A/5B RF paths

Note: *Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and at RF_TR_5_A/ RF_TR_5_B pin.*

Table 35. 6 GHz Wi-Fi receiver performance – 5A/5B RF paths

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	6 GHz	5925	—	7125	MHz
Receiver sensitivity SISO, NRx = 1, Nss = 1					
Receiver sensitivity (1x1)	802.11a, 20 MHz, 6 Mbps	—	-95.00	—	dBm
Receiver sensitivity (1x1)	802.11a, 20 MHz, 54 Mbps	—	-77.25	—	dBm
Receiver sensitivity (1x1)	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-94.50	—	dBm
Receiver sensitivity (1x1)	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-70.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-65.00	—	dBm
Receiver sensitivity (1x1)	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-91.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-68.75	—	dBm
Receiver sensitivity (1x1)	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-63.00	—	dBm
Receiver sensitivity (1x1)	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-88.50	—	dBm
Receiver sensitivity (1x1)	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-65.50	—	dBm
Receiver sensitivity (1x1)	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-59.00	—	dBm
Receiver sensitivity MIMO, NRx = 2, Nss = 1					
Receiver sensitivity (1 x 2)	802.11a, 20 MHz, 6 Mbps	—	-96.75	—	dBm
Receiver sensitivity (1 x 2)	802.11a, 20 MHz, 54 Mbps	—	-80.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-96.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-74.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-68.25	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-93.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-71.75	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-66.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	-90.00	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	-68.50	—	dBm
Receiver sensitivity (1 x 2)	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	-63.00	—	dBm

Table 35. 6 GHz Wi-Fi receiver performance – 5A/5B RF paths*...continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver adjacent channel interference (ACI) - NRx = 1, Nss = 1					
Receiver ACI	802.11a, 20 MHz, 6 Mbps	—	27.00	—	dB
Receiver ACI	802.11a, 20 MHz, 54 Mbps	—	15.25	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	27.50	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	11.25	—	dB
Receiver ACI	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	6.50	—	dB
Receiver ACI	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	27.00	—	dB
Receiver ACI	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	13.75	—	dB
Receiver ACI	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	8.25	—	dB
Receiver ACI	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	23.50	—	dB
Receiver ACI	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	11.00	—	dB
Receiver ACI	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	6.50	—	dB
Receiver alternative adjacent channel interference (AACI) - NRx = 1, Nss = 1					
Receiver AACI	802.11a, 20 MHz, 6 Mbps	—	40.50	—	dB
Receiver AACI	802.11a, 20 MHz, 54 Mbps	—	26.50	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS0 Nss1 LDPC 4x+3.2	—	44.50	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS9 Nss1 LDPC 4x+3.2	—	25.00	—	dB
Receiver AACI	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	19.75	—	dB
Receiver AACI	802.11ax, 40 MHz, MCS0 Nss1 LDPC 4x+3.2	—	43.50	—	dB
Receiver AACI	802.11ax, 40 MHz, MCS9 Nss1 LDPC 4x+3.2	—	22.25	—	dB
Receiver AACI	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	16.75	—	dB
Receiver AACI	802.11ax, 80 MHz, MCS0 Nss1 LDPC 4x+3.2	—	42.50	—	dB
Receiver AACI	802.11ax, 80 MHz, MCS9 Nss1 LDPC 4x+3.2	—	23.50	—	dB
Receiver AACI	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	17.25	—	dB

10.1.5 2.4 GHz Wi-Fi transmitter performance – 2A/2B RF paths

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2_A/RF_TR_2_B pin.*

Table 36. 2.4 GHz Wi-Fi transmitter performance – 2A/2B RF paths

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	2.4 GHz	2400	—	2483	MHz
Transmit power					
Transmit power EVM and Mask Limited	802.11b, 20 MHz, 1 Mbps	—	22.00	—	dBm
Transmit power EVM and Mask Limited	802.11b, 20 MHz, 11 Mbps	—	22.00	—	dBm
Transmit power EVM and Mask Limited	802.11g, 20 MHz, 54 Mbps	—	20.30	—	dBm
Transmit power EVM and Mask Limited	802.11n, 20 MHz, MCS7 Nss1 BCC	—	20.30	—	dBm
Transmit power EVM and Mask Limited	802.11n, 40 MHz, MCS7 Nss1 BCC	—	20.30	—	dBm
Transmit power EVM and Mask Limited	802.11ac, 20 MHz, MCS8 Nss1 LDPC	—	19.30	—	dBm
Transmit power EVM and Mask Limited	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	19.30	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 20 MHz, MCS11 Nss1 LDPC4x+3.2	—	18.30	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 40 MHz, MCS11 Nss1 LDPC4x+3.2	—	18.30	—	dBm
Transmit carrier suppression					
Transmit carrier suppression	802.11ax MCS11	—	40.00	—	dBc
Transmit output power					
Transmit output power control step		—	1.00	—	dB
Transmit output power level control range		—	0 – 22	—	dBm
Transmit output power accuracy	With manufacturing time per board calibration	-1.6	—	1.6	dBm
Transmit frequency error					
Transmit frequency error	802.11ax MCS11 With manufacturing time per board calibration	—	8.00	—	ppm
Transmit harmonics and sub harmonics[1]					
Transmit general spurs, harmonics, and sub-harmonics (1 Mbps TX at 18 dBm with 100% duty cycle)	< 1GHz	—	-77.00	—	dBm/100 kHz
	1 GHz to 12 GHz	—	-49.00	—	dBm/100 kHz
	2nd Harmonic	—	-47.00	—	dBm/1 MHz
	3rd Harmonic	—	-60.00	—	dBm/1 MHz
	LO leakage (2.4 GHz, MCS11)	—	-40.00	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.1.6 5 GHz Wi-Fi transmitter performance – 5A/5B RF paths

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5_A/RF_TR_5_B pin.*

Table 37. 5 GHz Wi-Fi transmitter performance – 5A/5B RF paths

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	5 GHz	5180	—	5885	MHz
Transmit power					
Transmit power EVM and Mask Limited	802.11a, 20 MHz, 54 Mbps	—	20.70	—	dBm
Transmit power EVM and Mask Limited	802.11n, 20 MHz, MCS7 Nss1 BCC	—	19.70	—	dBm
Transmit power EVM and Mask Limited	802.11n, 40 MHz, MCS7 Nss1 BCC	—	19.70	—	dBm
Transmit power EVM and Mask Limited	802.11ac, 20 MHz, MCS8 Nss1 LDPC	—	18.70	—	dBm
Transmit power EVM and Mask Limited	802.11ac, 40 MHz, MCS9 Nss1 LDPC	—	18.20	—	dBm
Transmit power EVM and Mask Limited	802.11ac, 80 MHz, MCS9 Nss1 LDPC	—	18.20	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	16.70	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	17.20	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	16.70	—	dBm
Transmit carrier suppression					
Transmit carrier suppression	802.11ax MCS11	—	34.00	—	dBc
Transmit output power					
Transmit output power control step		—	1.00	—	dB
Transmit output power level control range		—	0 – 22	—	dBm
Transmit output power accuracy	With manufacturing time per board calibration	-1.6	—	1.6	dBm
Transmit frequency error					
Transmit frequency error	802.11ax MCS11 With manufacturing time per board calibration	—	8.00	—	ppm
Transmit harmonics and sub harmonics[1]					
Transmit general spurs, harmonics, and sub-harmonics (6 Mbps TX at 18 dBm with 100% duty cycle)	< 1GHz	—	-78.00	—	dBm/100 kHz
	1 GHz to 12 GHz	—	-62.00	—	dBm/100 kHz
	2nd Harmonic	—	-57.00	—	dBm/1 MHz
	3rd Harmonic	—	-62.00	—	dBm/1 MHz
	LO leakage (5 GHz, MCS11)	—	-34.00	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.1.7 6 GHz Wi-Fi transmitter performance – 5A/5B RF paths

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5_A/RF_TR_5_B pin.*

Table 38. 6 GHz Wi-Fi transmitter performance – 5A/5B RF paths

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	6 GHz	5925	—	7125	MHz
Transmit power					
Transmit power EVM and Mask Limited	802.11a, 20 MHz, 54 Mbps	—	20.00	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 20 MHz, MCS11 Nss1 LDPC 4x+3.2	—	17.50	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 40 MHz, MCS11 Nss1 LDPC 4x+3.2	—	17.00	—	dBm
Transmit power EVM and Mask Limited	802.11ax, 80 MHz, MCS11 Nss1 LDPC 4x+3.2	—	16.50	—	dBm
Transmit carrier suppression					
Transmit carrier suppression	802.11ax MCS11	—	36.00	—	dBc
Transmit output power					
Transmit output power control step		—	1.00	—	dB
Transmit output power level control range		—	0 – 22	—	dBm
Transmit output power accuracy	With manufacturing time per board calibration	-1.6	—	1.6	dBm
Transmit frequency error					
Transmit frequency error	802.11ax MCS11 With manufacturing time per board calibration	—	8.00	—	ppm
Transmit harmonics and sub harmonics[1]					
Transmit general spurs, harmonics, and sub-harmonics (6 Mbps TX at 18 dBm with 100% duty cycle)	< 1GHz	—	-78.00	—	dBm/100 kHz
	1 GHz to 12 GHz	—	-62.00	—	dBm/100 kHz
	2nd Harmonic	—	-54.00	—	dBm/1 MHz
	3rd Harmonic	—	-51.00	—	dBm/1 MHz
	LO leakage (6 GHz, MCS11)	—	-36.00	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.2 Bluetooth radio specifications

10.2.1 Bluetooth/Bluetooth LE receiver performance

Note: *Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and at BRF_ANT pin.*

Table 39. Bluetooth/Bluetooth LE receiver performance

Bluetooth/Bluetooth LE receiver refers to Dirty TX. That is, the transmitter has impairments as specified by the Bluetooth SIG standard.

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency range	—	2400	—	2483	MHz
RSSI accuracy					
RSSI accuracy		-3	—	3	dB
RSSI readback resolution		—	1.00	—	dB
Regulatory					
Transmit power		—	12.90	—	dBm
Receiver sensitivity					
BDR 1 Mbps	Dirty TX ON	—	-97.90	—	dBm
EDR 2 Mbps	Dirty TX ON	—	-97.00	—	dBm
EDR 3 Mbps	Dirty TX ON	—	-90.90	—	dBm
Bluetooth LE 1 Mbps	Dirty TX ON	—	-100.00	—	dBm
Bluetooth LE 2 Mbps	Dirty TX ON	—	-97.50	—	dBm
Bluetooth LR 125 Kbps	Dirty TX ON	—	-108.30	—	dBm
Bluetooth LR 500 Kbps	Dirty TX ON	—	-101.40	—	dBm
Receiver maximum input level (MIL)					
BDR 1 Mbps	Dirty TX OFF	—	-3.00	—	dBm
EDR 2 Mbps	Dirty TX OFF	—	-6.00	—	dBm
EDR 3 Mbps	Dirty TX OFF	—	-6.00	—	dBm
Bluetooth LE 1 Mbps	Dirty TX OFF	—	-3.00	—	dBm
Bluetooth LE 2 Mbps	Dirty TX OFF	—	-3.00	—	dBm
Bluetooth LR 125 Kbps	Dirty TX OFF	—	-3.00	—	dBm
Bluetooth LR 500 Kbps	Dirty TX OFF	—	-3.00	—	dBm
Receiver interference/selectivity performance[1]					
BDR 1 Mbps					
Receiver ACI @ -5 MHz (image - 1)	BDR	—	-50.50	—	dB
Receiver ACI @ -4 MHz (image)	BDR	—	-30.00	—	dB
Receiver ACI @ -3 MHz (image + 1)	BDR	—	-40.00	—	dB
Receiver ACI @ -2 MHz	BDR	—	-46.50	—	dB
Receiver ACI @ -1 MHz	BDR	—	-10.00	—	dB
Receiver CCI	BDR	—	10.00	—	dB

Table 39. Bluetooth/Bluetooth LE receiver performance *...continued*

Bluetooth/Bluetooth LE receiver refers to Dirty TX. That is, the transmitter has impairments as specified by the Bluetooth SIG standard.

Parameter	Conditions	Min	Typ.	Max	Unit
Receiver ACI @ +1 MHz	BDR	—	-10.00	—	dB
Receiver ACI @ +2 MHz	BDR	—	-46.00	—	dB
Receiver ACI @ +3 MHz	BDR	—	-50.50	—	dB
EDR 2 Mbps					
Receiver ACI @ -5 MHz (image - 1)	EDR 2 Mbps	—	-50.00	—	dB
Receiver ACI @ -4 MHz (image)	EDR 2 Mbps	—	-30.00	—	dB
Receiver ACI @ -3 MHz (image + 1)	EDR 2 Mbps	—	-39.50	—	dB
Receiver ACI @ -2 MHz	EDR 2 Mbps	—	-46.00	—	dB
Receiver ACI @ -1 MHz	EDR 2 Mbps	—	-10.00	—	dB
Receiver CCI	EDR 2 Mbps	—	10.00	—	dB
Receiver ACI @ +1 MHz	EDR 2 Mbps	—	-10.00	—	dB
Receiver ACI @ +2 MHz	EDR 2 Mbps	—	-47.00	—	dB
Receiver ACI @ +3 MHz	EDR 2 Mbps	—	-51.50	—	dB
EDR 3 Mbps					
Receiver ACI @ -5 MHz (image - 1)	EDR 3 Mbps	—	-42.50	—	dB
Receiver ACI @ -4 MHz (image)	EDR 3 Mbps	—	-24.00	—	dB
Receiver ACI @ -3 MHz (image + 1)	EDR 3 Mbps	—	-40.00	—	dB
Receiver ACI @ -2 MHz	EDR 3 Mbps	—	-40.00	—	dB
Receiver ACI @ -1 MHz	EDR 3 Mbps	—	-8.00	—	dB
Receiver CCI	EDR 3 Mbps	—	15.00	—	dB
Receiver ACI @ +1 MHz	EDR 3 Mbps	—	-8.00	—	dB
Receiver ACI @ +2 MHz	EDR 3 Mbps	—	-40.50	—	dB
Receiver ACI @ +3 MHz	EDR 3 Mbps	—	-45.50	—	dB
Bluetooth LE 1 Mbps					
Receiver ACI @ -5 MHz (image - 1)	Bluetooth LE 1 Mbps	—	-40.00	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LE 1 Mbps	—	-31.00	—	dB
Receiver ACI @ -3 MHz (image + 1)	Bluetooth LE 1 Mbps	—	-33.00	—	dB
Receiver ACI @ -2 MHz	Bluetooth LE 1 Mbps	—	-41.00	—	dB
Receiver ACI @ -1 MHz	Bluetooth LE 1 Mbps	—	-3.00	—	dB
Receiver CCI	Bluetooth LE 1 Mbps	—	9.00	—	dB
Receiver ACI @ +1 MHz	Bluetooth LE 1 Mbps	—	-7.00	—	dB
Receiver ACI @ +2 MHz	Bluetooth LE 1 Mbps	—	-42.00	—	dB
Receiver ACI @ +3 MHz	Bluetooth LE 1 Mbps	—	-50.00	—	dB

Table 39. Bluetooth/Bluetooth LE receiver performance *...continued*

Bluetooth/Bluetooth LE receiver refers to Dirty TX. That is, the transmitter has impairments as specified by the Bluetooth SIG standard.

Parameter	Conditions	Min	Typ.	Max	Unit
Bluetooth LE 2 Mbps					
Receiver ACI @ -6 MHz (image - 2)	Bluetooth LE 2 Mbps	—	-52.50	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LE 2 Mbps	—	-29.00	—	dB
Receiver ACI @ -2 MHz	Bluetooth LE 2 Mbps	—	-21.00	—	dB
Receiver CCI	Bluetooth LE 2 Mbps	—	8.00	—	dB
Receiver ACI @ +2 MHz	Bluetooth LE 2 Mbps	—	-26.00	—	dB
Receiver ACI @ +4 MHz	Bluetooth LE 2 Mbps	—	-50.00	—	dB
Receiver ACI @ +6 MHz	Bluetooth LE 2 Mbps	—	-54.00	—	dB
Bluetooth LR 125 Kbps					
Receiver ACI @ -5 MHz (image - 1)	Bluetooth LR 125 Kbps	—	-44.00	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LR 125 Kbps	—	-31.00	—	dB
Receiver ACI @ -3 MHz (image + 1)	Bluetooth LR 125 Kbps	—	-34.00	—	dB
Receiver ACI @ -2 MHz	Bluetooth LR 125 Kbps	—	-50.00	—	dB
Receiver ACI @ -1 MHz	Bluetooth LR 125 Kbps	—	-9.00	—	dB
Receiver CCI	Bluetooth LR 125 Kbps	—	3.00	—	dB
Receiver ACI @ +1 MHz	Bluetooth LR 125 Kbps	—	-10.00	—	dB
Receiver ACI @ +2 MHz	Bluetooth LR 125 Kbps	—	-51.00	—	dB
Receiver ACI @ +3 MHz	Bluetooth LR 125 Kbps	—	-59.00	—	dB
Bluetooth LR 500 Kbps					
Receiver ACI @ -5 MHz (image - 1)	Bluetooth LR 500 Kbps	—	-41.00	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LR 500 Kbps	—	-28.00	—	dB
Receiver ACI @ -3 MHz (image + 1)	Bluetooth LR 500 Kbps	—	-34.00	—	dB
Receiver ACI @ -2 MHz	Bluetooth LR 500 Kbps	—	-49.00	—	dB
Receiver ACI @ -1 MHz	Bluetooth LR 500 Kbps	—	-5.00	—	dB
Receiver CCI	Bluetooth LR 500 Kbps	—	9.00	—	dB
Receiver ACI @ +1 MHz	Bluetooth LR 500 Kbps	—	-9.00	—	dB
Receiver ACI @ +2 MHz	Bluetooth LR 500 Kbps	—	-49.00	—	dB
Receiver ACI @ +3 MHz	Bluetooth LR 500 Kbps	—	-52.00	—	dB

[1] The selectivity numbers show the C/I ratio (in dB).

10.2.2 Bluetooth/Bluetooth LE transmitter performance

Note: *Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and at BRF_ANT pin.*

Table 40. Bluetooth/Bluetooth LE transmitter performance

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency range	—	2400	—	2483	MHz
Regulatory					
Transmit power (BDR)	13 dBm (mask compliant)	—	13.00	—	dBm
Transmit power (EDR)	10 dBm (EVM and mask compliant)	—	9.90	—	dBm
Transmit power (Bluetooth LE)	13 dBm (mask compliant)	—	12.90	—	dBm
Out-of-band noise floor					
Out-of-band noise floor at different operation standard frequency range (TX at 13 dBm with 100 % duty cycle)		—	-136.00	—	dBm/Hz
Transmit frequency error					
Transmit frequency error		—	8.80	—	kHz
Transmit output power					
Transmit output power accuracy (BDR/Bluetooth LE)		0.6	—	1.00	dB
Transmit output power control step (BDR)		—	1.00	—	dB
Transmit output power level control range (BDR)		-20.2	—	12.2	dBm
Transmit output power accuracy (EDR)		-0.6	—	1.00	dB
Transmit output power control step (EDR)		—	1.00	—	dB
Transmit output power level control range (EDR)		-24.00	—	10.00	dBm

Table 40. Bluetooth/Bluetooth LE transmitter performance *...continued*

Parameter	Conditions	Min	Typ.	Max	Unit
Transmit harmonics and sub harmonics[1]					
Transmit general spurs, harmonics, and sub-harmonics (TX at 13 dBm with 100% duty cycle)	< 1 GHz	—	-70.00	—	dBm/100 kHz
Transmit general spurs, harmonics, and sub-harmonics (TX at 13 dBm with 100% duty cycle)	1 GHz to 18 GHz	—	-65.30	—	dBm/100 kHz
Transmit general spurs, harmonics, and sub-harmonics (TX at 13 dBm with 100% duty cycle)	2nd harmonic	—	-62.00	—	dBm/1 MHz
Transmit general spurs, harmonics, and sub-harmonics (TX at 13 dBm with 100% duty cycle)	3rd harmonic	—	-66.00	—	dBm/1 MHz

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.3 Current consumption

Note: *Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and typical value. The current consumption data is collected with SDIO-UART interface configuration, and using the internal Buck regulator.*

Table 41. Current consumption values

Mode	Conditions	1.8 V	3.3 V	Unit
Power down				
Power down	PDn asserted	0.01	0.02	mA
Deep sleep				
Bluetooth only in deep sleep mode	SDIO 2.0	0.43	0.23	mA
Wi-Fi only in deep sleep mode	SDIO 2.0	0.73	0.23	mA
Wi-Fi and Bluetooth both in deep sleep mode	SDIO 2.0 (VIO = 1.8 V)	0.87	0.24	mA
Wi-Fi only in deep sleep mode	SDIO 3.0 200 MHz (clock gating)	2.00	0.04	mA
Wi-Fi and Bluetooth both in deep sleep mode	SDIO 3.0 200 MHz (clock gating)	2.49	0.04	mA
Bluetooth LE only (Wi-Fi in sleep mode)				
Bluetooth LE advertise	interval = 1.28 second	0.55	0.24	mA
Bluetooth LE scan	interval = 1.28 second, window = 11.25 ms	0.85	0.24	mA
Bluetooth LE transmit	at 0 dBm, 1 Mbps	40	0.35	mA
Bluetooth LE transmit	at 4 dBm, 1 Mbps	42	0.35	mA
Bluetooth LE transmit	at 10 dBm, 1 Mbps	67	0.35	mA
Bluetooth LE receive	1 Mbps	36	0.34	mA
Bluetooth only (Wi-Fi in sleep mode)				
Bluetooth idle	—	16	0.34	mA
Bluetooth transmit	at 0 dBm, DH5	41	0.35	mA
Bluetooth transmit	at 4 dBm, DH5	43	0.35	mA
Bluetooth transmit	at 10 dBm, DH5	68	0.35	mA
Bluetooth transmit	at 13 dBm, DH5	77	0.35	mA
Bluetooth receive	DH5	32	0.35	mA
Bluetooth only (Wi-Fi in sleep mode) - 85 °C				
Bluetooth peak transmit	at 13 dBm, DH5	88	0.40	mA
Bluetooth peak receive	—	44	0.40	mA

Table 41. Current consumption values...*continued*

Mode	Conditions	1.8 V	3.3 V	Unit
IEEE Wi-Fi power save mode (Bluetooth in sleep mode)				
2.4 GHz Wi-Fi				
DTIM-1 (2.4 GHz, 20 MHz)	SDIO 3.0 (clock gating), channel-1, beacon interval 102.4 ms, beacon length 1000 μs, 2.4 GHz basic rate for beacon transmit: 1 Mbps	4.54	0.04	mA
DTIM-3 (2.4 GHz, 20 MHz)		3.42	0.04	mA
DTIM-5 (2.4 GHz, 20 MHz)		3.18	0.04	mA
DTIM-10 (2.4 GHz, 20 MHz)		2.95	0.04	mA
5 GHz Wi-Fi				
DTIM-1 (5 GHz, 20 MHz)	SDIO 3.0 (clock gating), channel-36, beacon interval 102.4 ms, beacon length 300 μs, 5 GHz basic rate for beacon transmit: 6 Mbps	4.48	0.04	mA
DTIM-3 (5 GHz, 20 MHz)		3.31	0.04	mA
DTIM-5 (5 GHz, 20 MHz)		2.99	0.04	mA
DTIM-10 (5 GHz, 20 MHz)		2.80	0.04	mA
Wi-Fi TWT mode				
2.4 GHz Wi-Fi				
TWT interval 1 min	SDIO 3.0 clock gating	2.85	0.23	mA
TWT interval 5 min		2.74	0.23	mA
TWT interval 10 min		2.71	0.23	mA
TWT interval 30 min		2.69	0.23	mA
5 GHz Wi-Fi				
TWT interval 1 min	SDIO 3.0 clock gating	2.85	0.23	mA
TWT interval 5 min		2.76	0.23	mA
TWT interval 10 min		2.72	0.23	mA
TWT interval 30 min		2.71	0.23	mA
Wi-Fi idle mode				
2.4 GHz 1x1 receive idle mode (MAC1)	2.4GHz, RX, 802.11b, 20 MHz, channel-1, listening	163	0.31	mA
	2.4 GHz, RX, 802.11g, 20 MHz, channel-1, listening	162	0.31	mA
	2.4 GHz, RX, 802.11n, 20 MHz, channel-1, listening	162	0.31	mA
	2.4 GHz, RX, 802.11n, 40 MHz, channel-1, listening	175	0.31	mA
	2.4 GHz, RX, 802.11ax, 20 MHz, channel-1, listening	162	0.31	mA
	2.4 GHz, RX, 802.11ax, 40 MHz, channel-1, listening	177	0.31	mA
5 GHz 1x1 receive idle mode	5 GHz, RX, 802.11a, 20 MHz, channel-36, listening	207	0.31	mA
	5 GHz, RX, 802.11n, 20 MHz, channel-36, listening	209	0.31	mA

Table 41. Current consumption values *...continued*

Mode	Conditions	1.8 V	3.3 V	Unit
	5 GHz, RX, 802.11n, 40 MHz, channel-36, listening	222	0.31	mA
	5 GHz, RX, 802.11ac, 20 MHz, channel-36, listening	208	0.31	mA
	5 GHz, RX, 802.11ac, 40 MHz, channel-36, listening	220	0.31	mA
	5 GHz, RX, 802.11ac, 80 MHz, channel-36, listening	260	0.31	mA
	5 GHz, RX, 802.11ax, 20 MHz, channel-36, listening	208	0.31	mA
	5 GHz, RX, 802.11ax, 40 MHz, channel-36, listening	221	0.31	mA
	5 GHz, RX, 802.11ax, 80 MHz, channel-36, listening	260	0.31	mA
6 GHz 1x1 receive idle mode	6 GHz, RX, 802.11ax, 20 MHz, channel-33, listening	217	0.31	mA
	6 GHz, RX, 802.11ax, 40 MHz, channel-33, listening	228	0.31	mA
	6 GHz, RX, 802.11ax, 80 MHz, channel-33, listening	272	0.31	mA
2.4 GHz 2x2 receive idle mode	2.4 GHz, RX, 802.11b, 20 MHz, channel-1, listening	199	0.31	mA
	2.4 GHz, RX, 802.11g, 20 MHz, channel-1, listening	199	0.31	mA
	2.4 GHz, RX, 802.11n, 20 MHz, channel-1, listening	198	0.31	mA
	2.4 GHz, RX, 802.11n, 40 MHz, channel-1, listening	222	0.31	mA
	2.4 GHz, RX, 802.11ax, 20 MHz, channel-1, listening	199	0.31	mA
	2.4 GHz, RX, 802.11ax, 40 MHz, channel-1, listening	220	0.31	mA
5 GHz 2x2 receive idle mode	5 GHz, RX, 802.11a, 20 MHz, channel-36, listening	243	0.31	mA
	5 GHz, RX, 802.11n, 20 MHz, channel-36, listening	249	0.31	mA
	5 GHz, RX, 802.11n, 40 MHz, channel-36, listening	280	0.31	mA
	5 GHz, RX, 802.11ac, 20 MHz, channel-36, listening	241	0.31	mA
	5 GHz, RX, 802.11ac, 40 MHz, channel-36, listening	280	0.31	mA
	5 GHz, RX, 802.11ac, 80 MHz, channel-36, listening	344	0.31	mA

Table 41. Current consumption values *...continued*

Mode	Conditions	1.8 V	3.3 V	Unit
	5 GHz, RX, 802.11ax, 20 MHz, channel-36, listening	241	0.31	mA
	5 GHz, RX, 802.11ax, 40 MHz, channel-36, listening	278	0.31	mA
	5 GHz, RX, 802.11ax, 80 MHz, channel-36, listening	345	0.31	mA
6 GHz 2x2 receive idle mode	6 GHz, RX, 802.11ax, 20 MHz, channel-33, listening	260	0.31	mA
	6 GHz, RX, 802.11ax, 40 MHz, channel-33, listening	296	0.31	mA
	6 GHz, RX, 802.11ax, 80 MHz, channel-33, listening	355	0.31	mA
Wi-Fi active receive mode				
2.4 GHz 1x1 receive mode	2.4 GHz, 802.11b, 20 MHz, 11 Mbps, channel-1	157	0.31	mA
	2.4 GHz, 802.11g, 20 MHz, 54 Mbps, channel-1	181	0.31	mA
	2.4 GHz, 802.11n, 20 MHz, MCS7, channel-1	199	0.31	mA
	2.4 GHz, 802.11n, 40 MHz, MCS7, channel-1	225	0.31	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS11, channel-1	209	0.31	mA
	2.4 GHz, 802.11ax, 40 MHz, MCS11, channel-1	228	0.31	mA
5 GHz 1x1 receive mode	5 GHz, 802.11a, 20 MHz, 54 Mbps, channel-36	226	0.31	mA
	5 GHz, 802.11n, 20 MHz, MCS7, channel-36	243	0.31	mA
	5GHz, 802.11n, 40 MHz, MCS7, channel-36	275	0.31	mA
	5 GHz, 802.11ac, 20 MHz, MCS8, channel-36	242	0.31	mA
	5 GHz, 802.11ac, 40 MHz, MCS9, channel-36	270	0.31	mA
	5 GHz, 802.11ac, 80 MHz, MCS9, channel-36	322	0.31	mA
	5 GHz, 802.11ax, 20 MHz, MCS11, channel-36	259	0.31	mA
	5 GHz, 802.11ax, 40 MHz, MCS11, channel-36	266	0.31	mA
	5 GHz, 802.11ax, 80 MHz, MCS11, channel-36	340	0.31	mA
6 GHz 1x1 receive mode	5 GHz, 802.11ax, 20 MHz, MCS11, channel-33	270	0.31	mA
	6 GHz, 802.11ax, 40 MHz, MCS11, channel-33	303	0.31	mA
	6 GHz, 802.11ax, 80 MHz, MCS11, channel-33	360	0.31	mA
2.4 GHz 2x2 receive mode	2.4 GHz, 802.11b, 20 MHz, 11 Mbps, channel-1	195	0.31	mA
	2.4 GHz, 802.11g, 20 MHz, 54 Mbps, channel-1	223	0.31	mA
	2.4 GHz, 802.11n, 20 MHz, MCS15, channel-1	264	0.31	mA
	2.4 GHz, 802.11n, 40 MHz, MCS15, channel-1	301	0.31	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS11, channel-1	271	0.31	mA
	2.4 GHz, 802.11ax, 40 MHz, MCS11, channel-1	313	0.31	mA
5 GHz 2x2 receive mode	5 GHz, 802.11a, 20 MHz, 54 Mbps, channel-36	282	0.31	mA

Table 41. Current consumption values*...continued*

Mode	Conditions	1.8 V	3.3 V	Unit
	5 GHz, 802.11n, 20 MHz, MCS15, channel-36	304	0.31	mA
	5 GHz, 802.11n, 40 MHz, MCS15, channel-36	345	0.31	mA
	5 GHz, 802.11ac, 20 MHz, MCS8, channel-36	304	0.31	mA
	5 GHz, 802.11ac, 40 MHz, MCS9, channel-36	343	0.31	mA
	5 GHz, 802.11ac, 80 MHz, MCS9, channel-36	433	0.31	mA
	5 GHz, 802.11ax, 20 MHz, MCS11, channel-36	304	0.31	mA
	5 GHz, 802.11ax, 40 MHz, MCS11, channel-36	347	0.31	mA
	5 GHz, 802.11ax, 80 MHz, MCS11, channel-36	433	0.31	mA
6 GHz 2x2 receive mode	6 GHz, 802.11ax, 20 MHz, MCS11, channel-33	316	0.31	mA
	6 GHz, 802.11ax, 40 MHz, MCS11, channel-33	373	0.31	mA
	6 GHz, 802.11ax, 80 MHz, MCS11, channel-33	463	0.31	mA
Wi-Fi active transmit mode (transmit power referred to chip pin)				
2.4 GHz 1x1 transmit mode	2.4 GHz, 802.11b, 20 MHz, 11 Mbps at 20 dBm, channel-1	225	154	mA
	2.4 GHz, 802.11g, 20 MHz, 54 Mbps at 20 dBm, channel-1	238	156	mA
	2.4 GHz, 802.11n, 20 MHz, MCS7 at 20 dBm, channel-1	244	156	mA
	2.4 GHz, 802.11n, 40 MHz, MCS7 at 20 dBm, channel-1	247	159	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS11 at 20 dBm, channel-1	239	156	mA
	2.4 GHz, 802.11ax, 40 MHz, MCS11 at 20 dBm, channel-1	242	155	mA
5 GHz 1x1 transmit mode	5 GHz, 802.11a, 20 MHz, 54 Mbps at 19 dBm, channel-36	356	247	mA
	5 GHz, 802.11n, 20 MHz, MCS7 at 19 dBm, channel-36	339	245	mA
	5 GHz, 802.11n, 40 MHz, MCS7 at 17 dBm, channel-36	340	213	mA
	5 GHz, 802.11ac, 20 MHz, MCS8 at 19 dBm, channel-36	346	247	mA
	5 GHz, 802.11ac, 40 MHz, MCS9 at 17 dBm, channel-36	346	216	mA
	5 GHz, 802.11ac, 80 MHz, MCS9 at 15 dBm, channel-36	373	196	mA
	5 GHz, 802.11ax, 20 MHz, MCS11 at 19 dBm, channel-36	343	249	mA
	5 GHz, 802.11ax, 40 MHz, MCS11 at 17 dBm, channel-36	343	216	mA

Table 41. Current consumption values*...continued*

Mode	Conditions	1.8 V	3.3 V	Unit
	5 GHz, 802.11ax, 80 MHz, MCS11 at 15 dBm, channel-36	376	193	mA
6 GHz 1x1 transmit mode	6 GHz, 802.11ax, 20 MHz, MCS11 at 19 dBm, channel-33	352	253	mA
	6 GHz, 802.11ax, 40 MHz, MCS11 at 17 dBm, channel-33	362	226	mA
	6 GHz, 802.11ax, 80 MHz, MCS11 at 15 dBm, channel-33	379	196	mA
2.4GHz 2x2 transmit mode	2.4 GHz, 802.11b, 20 MHz, 11 Mbps at 20 dBm, channel-1	335	319	mA
	2.4 GHz, 802.11g, 20 MHz, 54 Mbps at 20 dBm, channel-1	343	348	mA
	2.4 GHz, 802.11n, 20 MHz, MCS15 at 20 dBm, channel-1	357	327	mA
	2.4 GHz, 802.11n, 40 MHz, MCS15 at 20 dBm, channel-1	388	342	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS11 at 20 dBm, channel-1	355	343	mA
	2.4 GHz, 802.11ax, 40 MHz, MCS11 at 20 dBm, channel-1	400	338	mA
5 GHz 2x2 transmit mode	5 GHz, 802.11a, 20 MHz, 54 Mbps at 19 dBm, channel-36	536	537	mA
	5 GHz, 802.11n, 20 MHz, MCS15 at 19 dBm, channel-36	550	531	mA
	5 GHz, 802.11n, 40 MHz, MCS15 at 17 dBm, channel-36	556	471	mA
	5 GHz, 802.11ac, 20 MHz, MCS8 at 19 dBm, channel-36	544	535	mA
	5 GHz, 802.11ac, 40 MHz, MCS9 at 17 dBm, channel-36	563	475	mA
	5 GHz, 802.11ac, 80 MHz, MCS9 at 15 dBm, channel-36	610	423	mA
	5 GHz, 802.11ax, 20 MHz, MCS11 at 19 dBm, channel-36	532	534	mA
	5 GHz, 802.11ax, 40 MHz, MCS11 at 17 dBm, channel-36	566	476	mA
	5 GHz, 802.11ax, 80 MHz, MCS11 at 15 dBm, channel-36	641	424	mA
6 GHz 2x2 transmit mode	6 GHz, 802.11ax, 20 MHz, MCS11 at 19 dBm, channel-33	546	525	mA
	6 GHz, 802.11ax, 40 MHz, MCS11 at 17 dBm, channel-33	546	465	mA

Table 41. Current consumption values...*continued*

Mode	Conditions	1.8 V	3.3 V	Unit
	6 GHz, 802.11ax, 80 MHz, MCS11 at 15 dBm, channel-33	641	408	mA
Wi-Fi, BT concurrent mode				
6 GHz 2x2 transmit + BT transmit mode	Wi-Fi 6 GHz, 802.11ax, 80 MHz, 2x2, MCS11 at 15 dBm, channel-33 and BT DH5 at 13 dBm (at 25 °C)	718	408	mA
6 GHz 2x2 receive + BT receive mode	Wi-Fi 6 GHz, 802.11ax, 80 MHz, 2x2, MCS11, channel-33 and BT DH5 (at 5 °C)	495	0.32	mA
6 GHz 2x2 transmit + BT transmit mode	Wi-Fi 6 GHz, 802.11ax, 80 MHz, 2x2, MCS11 at 15 dBm, channel-33 and BT DH5 at 13 dBm (at 85 °C)	888	430	mA
6 GHz 2x2 receive + BT receive mode	Wi-Fi 6 GHz, 802.11ax, 80 MHz, 2x2, MCS11, channel-33 and BT DH5 (at 85 °C)	620	0.31	mA
Peak current				
Peak current drawn with the maximum supported radio configuration	Measured at 25 °C	718	520	mA
Peak current drawn with the maximum supported radio configuration	Measured at 85 °C	888	550	mA

11 Electrical specifications

11.1 GPIO/LED interface specifications

For the list of GPIOs, see Section 6.5.2.

11.1.1 VIO DC characteristics

11.1.1.1 VIO 1.8 V operation

Table 42. DC electrical specifications—1.8V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIO	I/O pad supply voltage	—	1.71	1.8	1.89	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.1.1.2 VIO 3.3 V operation

Table 43. DC electrical specifications—3.3V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIO	I/O pad supply voltage	—	3.14	3.3	3.46	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.1.2 LED mode

Table 44. LED mode data

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Typ	Unit
I_{OH}	Output high current	Tristate on pad (requires pull-up on board)	0	mA
I_{OL}	Output low current	@ 0.4V	10	mA

11.2 RF front-end control interface specifications

11.2.1 VIO_RF DC characteristics

11.2.1.1 VIO_RF 1.8 V operation

Table 45. DC electrical specifications—1.8V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	—	0.7*VIO_RF	—	VIO_RF+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_RF-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.2.1.2 VIO_RF 3.3 V operation

Table 46. DC electrical specifications—3.3V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	—	0.7*VIO_RF	—	VIO_RF+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_RF-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3 SDIO host interface specifications

The SDIO host interface pins are powered by VIO_SD voltage supply.

11.3.1 VIO_SD DC characteristics

11.3.1.1 VIO_SD 1.8 V operation

Table 47. DC electrical characteristics—1.8 V operation (VIO_SD)
Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	—	0.7*VIO_SD	—	VIO_SD+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_SD-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3.1.2 VIO_SD 3.3 V operation

Table 48. DC electrical characteristics—3.3 V operation (VIO_SD)
Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	—	0.7*VIO_SD	—	VIO_SD+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_SD-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3.2 Default speed, high-speed modes

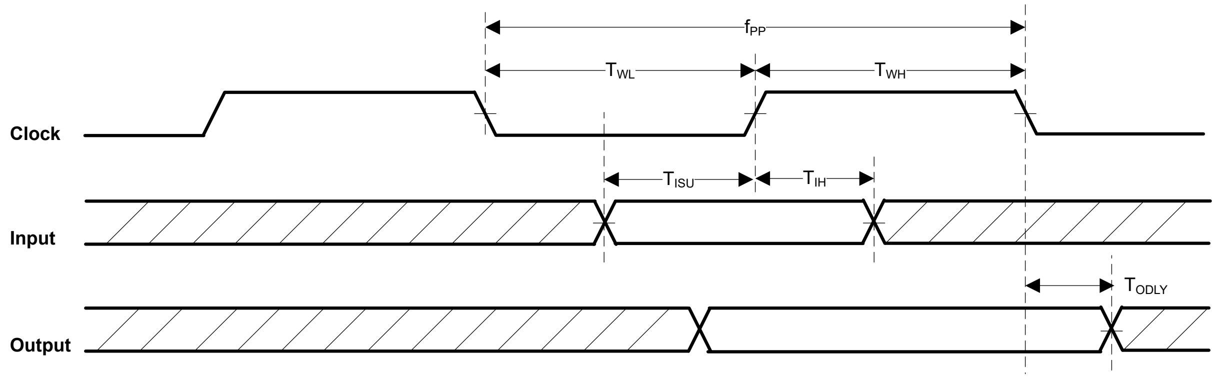


Figure 22. SDIO protocol timing diagram—Default speed mode

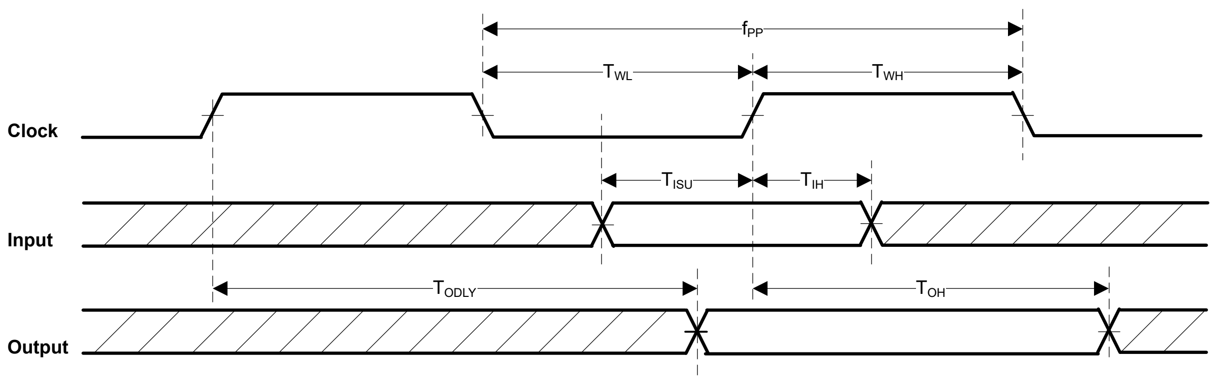


Figure 23. SDIO protocol timing diagram—High-speed mode

Table 49. SDIO timing data—Default speed, High-speed Modes

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	—	25	MHz
		High-speed	0	—	50	MHz
T_{WL}	Clock low time	Normal	10	—	—	ns
		High-speed	7	—	—	ns
T_{WH}	Clock high time	Normal	10	—	—	ns
		High-speed	7	—	—	ns
T_{ISU}	Input setup time	Normal	5	—	—	ns
		High-speed	6	—	—	ns
T_{IH}	Input hold time	Normal	5	—	—	ns
		High-speed	2	—	—	ns
T_{ODLY}	Output delay time	Normal	—	—	14	ns
	CL ≤ 40 pF (1 card)	High-speed	—	—	14	ns
T_{OH}	Output hold time	High-speed	2.5	—	—	ns

11.3.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

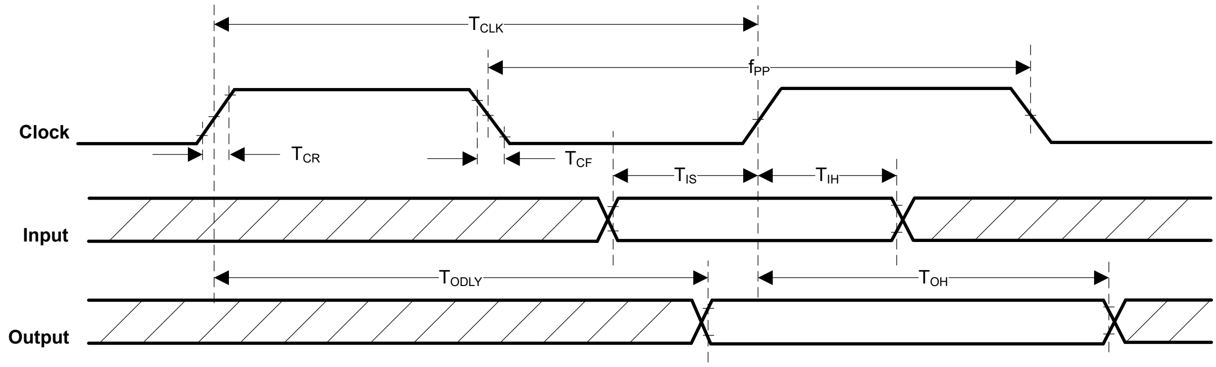


Figure 24. SDIO protocol timing diagram—SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Table 50. SDIO timing data——SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR12	—	—	25	MHz
		SDR25	—	—	50	MHz
		SDR50	—	—	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	—	—	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	—	—	ns
T_{CLK}	Clock time	SDR12	40	—	—	ns
		SDR25	20	—	—	ns
		SDR50	10	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	—	—	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25/50	—	—	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	—	—	ns

11.3.4 SDR104 mode (208 MHz) (1.8V)

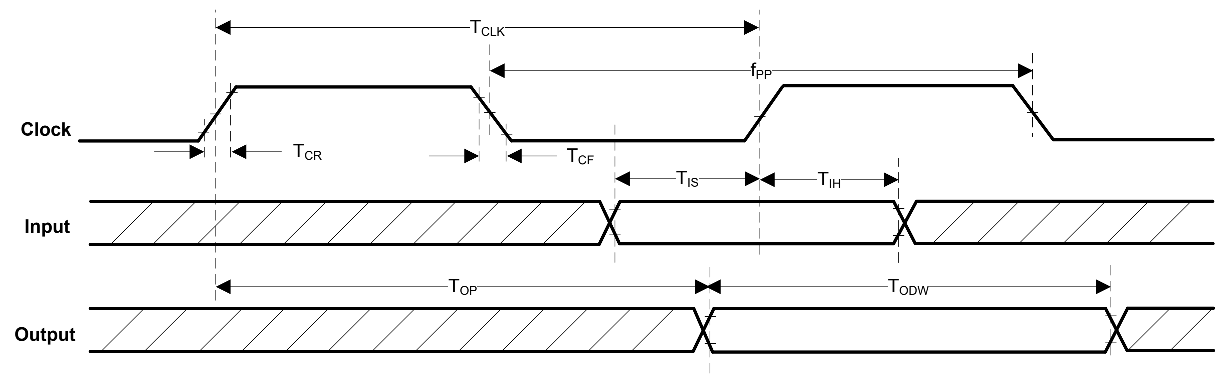


Figure 25. SDIO protocol timing diagram—SDR104 mode (208 MHz)

Table 51. SDIO timing data—SDR104 mode (208 MHz)

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	—	208	MHz
T_{IS}	Input setup time	SDR104	1.4	—	—	ns
T_{IH}	Input hold time	SDR104	0.8	—	—	ns
T_{CLK}	Clock time	SDR104	4.8	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	—	—	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	—	2	T_{CLK}
T_{ODW}	Output timing of variable data window	SDR104	2.88	—	—	ns

11.3.5 DDR50 mode (50 MHz) (1.8V)

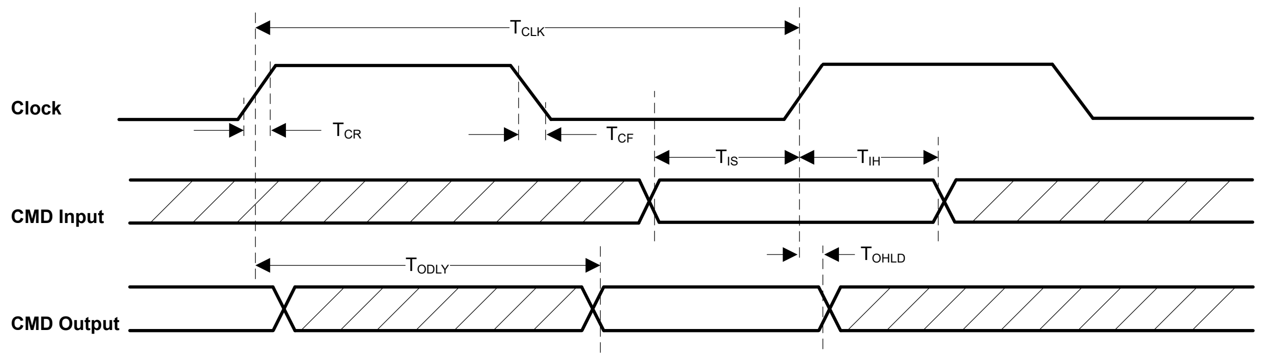


Figure 26. SDIO CMD timing diagram—DDR50 mode (50 MHz)

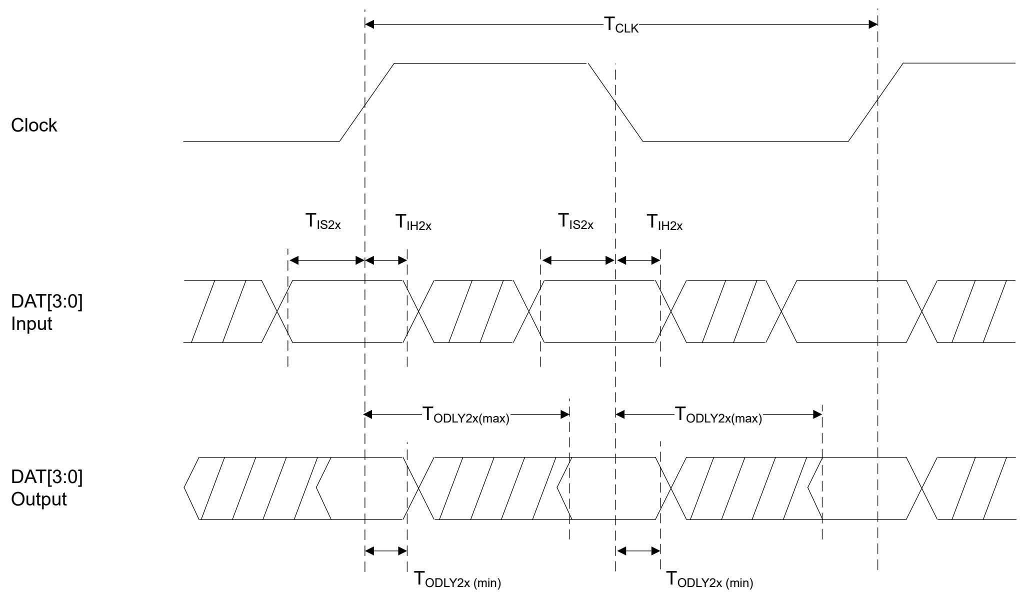


Figure 27. SDIO DAT[3:0] timing diagram—DDR50 mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Table 52. SDIO timing data—DDR50 mode (50 MHz)

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	—	—	0.2*T_{CLK}	ns
Clock Duty	—	DDR50	45	—	55	%
CMD input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	—	—	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	—	—	ns
CMD output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	—	—	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	—	—	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	—	—	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	—	—	ns
DAT[3:0] output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	—	—	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	—	—	ns

11.3.6 SDIO internal pull-up/pull-down specifications

Table 53. SDIO internal pull-up/pull-down specifications

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance	—	70	100	140	kΩ

11.4 UART interface specifications

The UART Tx and Rx pins are powered from the VIO voltage supply.

See Section 11.1.1 "VIO DC characteristics" for DC specifications.

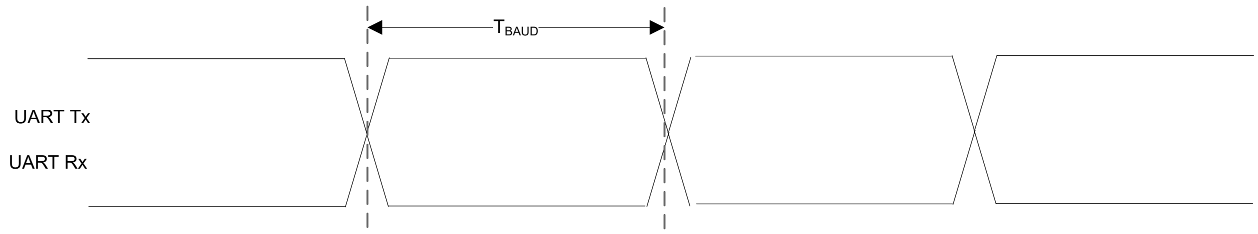


Figure 28. UART timing diagram

Table 54. UART timing data[1] [2]

Over full range of values specified in Section 9 "Recommended operating conditions" unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{BAUD}	Baud time	40 MHz input clock	250	--	--	ns

[1] The acceptable deviation from the UART Rx target baud rate is ±3%.
[2] UART TX baud rate deviation is determined by the external crystal accuracy. See Section 11.8.1.

11.5 Audio interface specifications

11.5.1 I2S interface specifications

The I2S pins are powered by VIO voltage supply. See Section 11.1.1 "VIO DC characteristics" for specifications.

Central mode

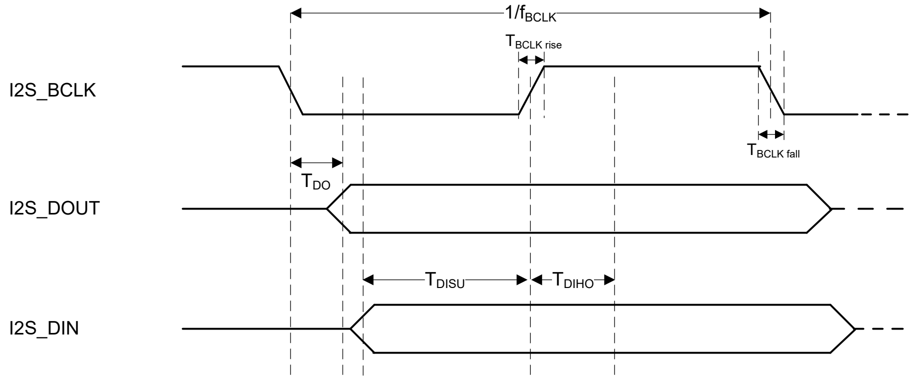


Figure 29. I2S timing specification diagram for data signals—Central mode

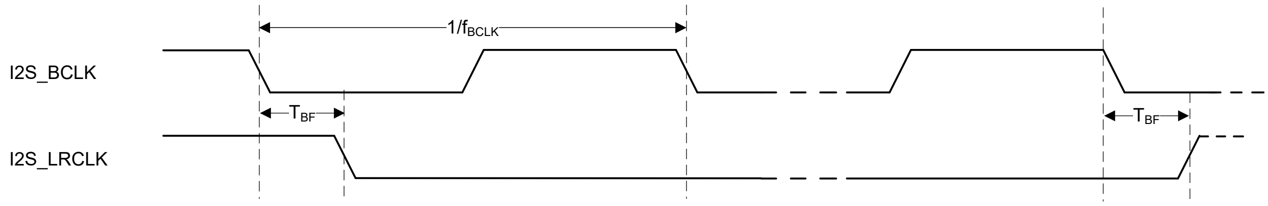


Figure 30. I2S timing specification diagram for clock signals—Central mode

Table 55. I2S timing specification data—Centra mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	—	1.024	2/2.048	4.096	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	—	45	50	55	%
$T_{BCLK\ rise/fall}$	I2S_BCLK rise/fall time	—	—	3	—	ns
T_{DO}	Delay from I2S_BCLK falling edge to I2S_DOUT rising edge	—	—	—	40	ns
T_{DISU}	Setup time for I2S_DIN before I2S_BCLK rising edge	—	10	—	—	ns
T_{DIHO}	Hold time for I2S_DIN after I2S_BCLK rising edge	—	0	—	—	ns
T_{BF}	Delay from I2S_BCLK falling edge to I2S_LRCLK falling edge	—	—	—	40	ns

Peripheral mode

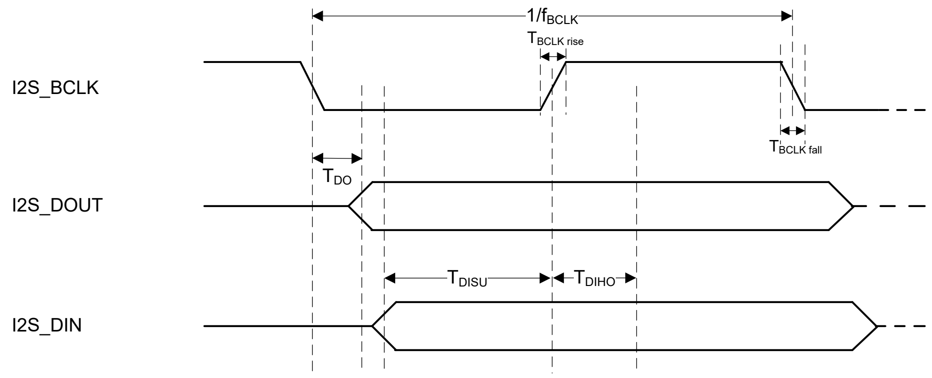


Figure 31. I2S timing specification diagram for data signals—Peripheral mode

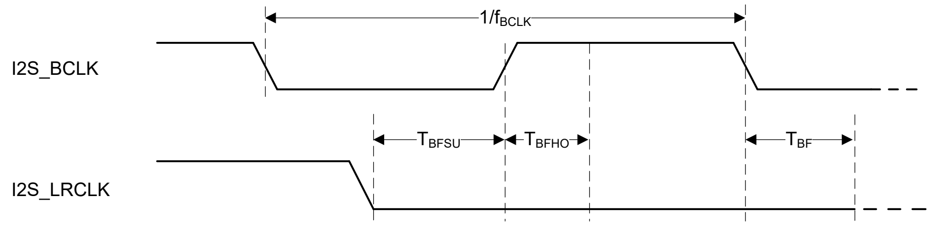


Figure 32. I2S timing specification diagram for clock signal—Peripheral mode

Table 56. I2S timing specification data—Peripheral mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	—	1.024	2/2.048	4.096	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	—	45	50	55	%
$T_{BCLK\ rise/fall}$	I2S_CLK rise/fall time	—	—	3	—	ns
T_{DO}	Delay from I2S_BCLK falling edge to I2S_DOUT rising edge	—	—	—	40	ns
T_{DISU}	Setup time for I2S_DIN before I2S_BCLK rising edge	—	10	—	—	ns
T_{DIHO}	Hold time for I2S_DIN after I2S_BCLK rising edge	—	0	—	—	ns
T_{BFSU}	Setup time for I2S_LRCLK before I2S_BCLK rising edge	—	40	—	—	ns
T_{BFHO}	Hold time for I2S_LRCLK after I2S_BCLK rising edge	—	0	—	—	ns

11.5.2 PCM interface specifications

The PCM pins are powered by VIO voltage supply. See Section 11.1.1 "VIO DC characteristics" for specifications.

Central mode

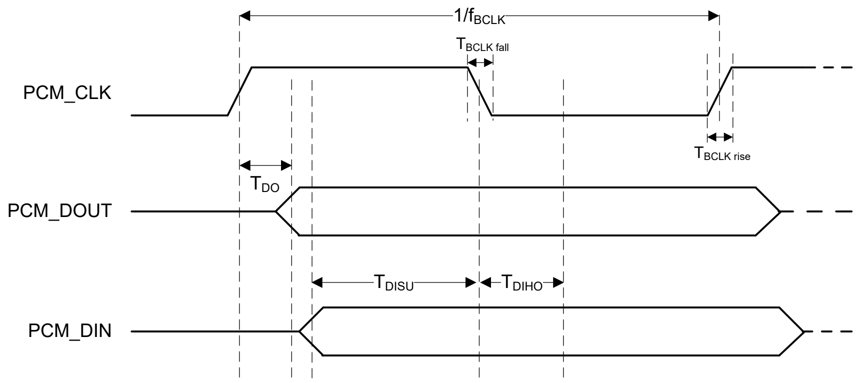


Figure 33. PCM timing specification diagram for data signals—Central mode

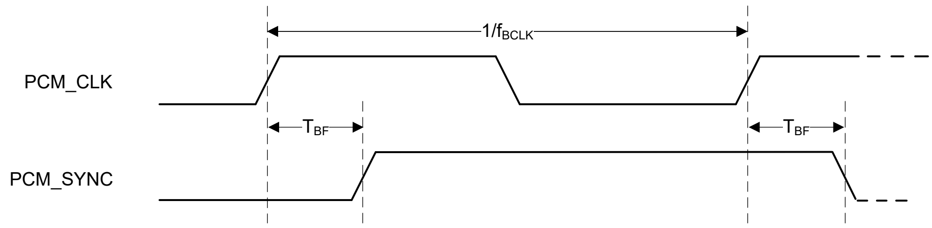


Figure 34. PCM timing specification diagram for PCM_SYNC signal—Central mode

Table 57. PCM timing specification data—Central mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	--	2	2/2.048	2.048	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

Peripheral mode

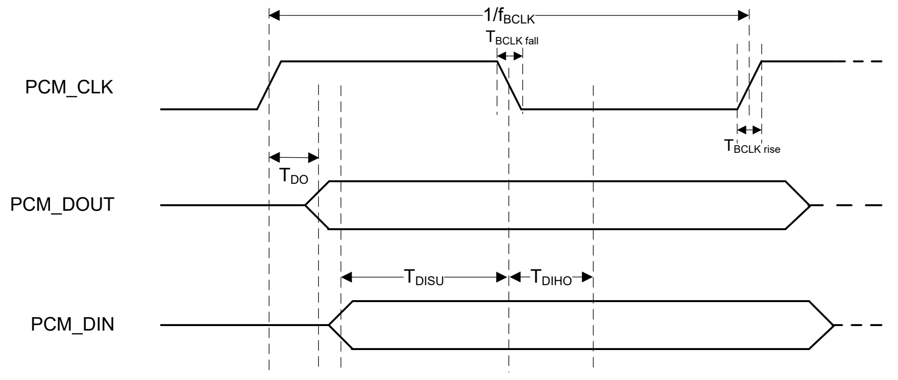


Figure 35. PCM timing specification diagram for data signals—Peripheral mode

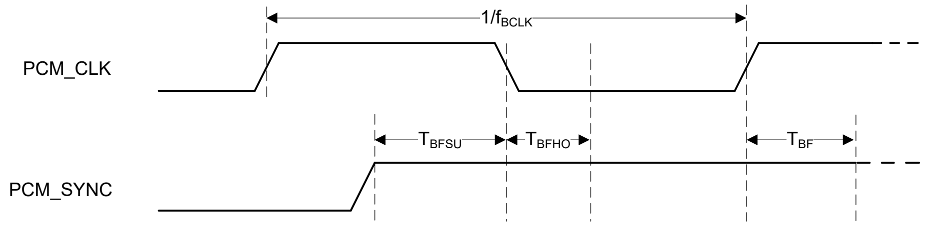


Figure 36. PCM timing specification diagram for PCM_SYNC signal—Peripheral mode

Table 58. PCM timing specification data—Peripheral mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	--	0.512[1]	2/2.048	4	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

[1] For applications that support dual-WBS (Wide Band Speech) capabilities over Bluetooth, a minimum PCM clock rate of 1.024 MHz is required due to bandwidth considerations. A single–WBS link or dual-NBS link configuration can be supported using a 0.512 MHz PCM clock rate.

11.6 External radio coexistence interface specifications

11.6.1 WCI-2 coexistence interface specifications

11.6.1.1 WCI-2 interface

WCI-2 is a simplified 2-wire UART interface defined in Bluetooth Core Spec Vol 7 Part C.

Figure 37 shows UART waveform.

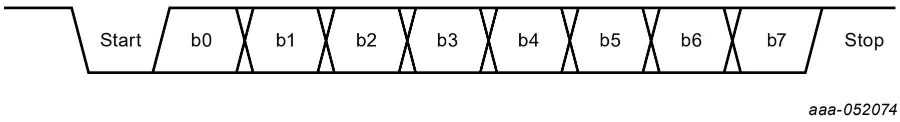


Figure 37. UART waveform

Figure 38 illustrates WCI-2 hardware coexistence interface between IW623S (Wireless SoC) and the external radio.

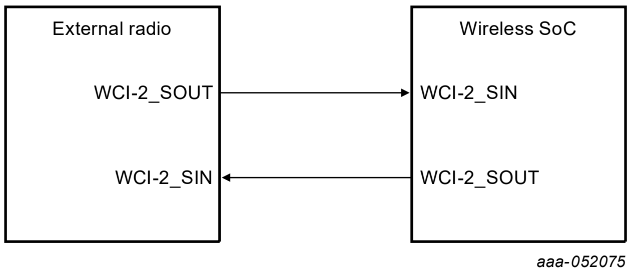


Figure 38. WCI-2 coexistence interface

11.6.1.2 WCI-2 messages

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for request and grant, where:

- The real time message from the external radio to IW623S indicates the request to operate (Figure 39)
  - MWS_Rx=1 indicates an external radio request to Rx
  - MWS_Tx=1 indicates an external radio request to Tx

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	FRAME_SYNC	MWS_RX	MWS_TX	MWS_PATTERN[0]	MWS_PATTERN[1]

aaa-052076

Figure 39. Type 0: Real time signaling message - external radio to IW623S

- The external radio can send an optional second message following the real time message to indicate the traffic priority using the vendor specific message (Figure 40). Otherwise, the priority is set via a BCA register.

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	1	1	0	MWS_TX_PRI[0]	MWS_TX_PRI[1]	MWS_RX_PRI[0]	MWS_RX_PRI[1]

aaa-052077

Figure 40. Type 7: Vendor specific message - external radio to IW623S

- The real time message from IW623S to the external radio indicates the arbitration results (Figure 41):
  - BT_Rx_Pri = 1: the Bluetooth radio Rx wins the arbitration and is in operation
  - BT_Tx_On = 1: the Bluetooth radio Tx wins the arbitration and is in operation
  - 802_Rx_Pri = 1: Wi-Fi Rx wins the arbitration and is in operation
  - 802_Tx_On = 1: Wi-Fi Tx wins the arbitration and is in operation
  - Otherwise, the external radio is granted

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	NB_RX_PRI	NB_TX_ON	802_RX_PRI	802_TX_ON	RFU

aaa-052078

Figure 41. Type 0: Real time signaling message - IW623S to external radio

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for other purposes, such as:

- Transport control message from IW623S to the external radio to request real time message upon wake up (Figure 42)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	1	Resend_real_time	RFU	RFU	RFU	RFU

aaa-052079

Figure 42. Type 1: Transport control message time signaling message - IW623S to external radio

- MWS inactivity duration message from the external radio to IW623S indicates the inactivity duration to IW623S before going to sleep (Figure 43)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	1	1	Duration[0]	Duration[1]	Duration[2]	Duration[3]	Duration[4]

aaa-052081

Figure 43. MWS inactivity duration message

- MWS scan frequency message from the external radio to IW623S indicates the external radio scan frequency to IW623S (Figure 44)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	0	0	Freq[0]	Freq[1]	Freq[2]	Freq[3]	Freq[4]

aaa-052080

Figure 44. Type 5: MWS scan frequency message

11.6.1.3 WCI-2 signal waveform format

The messaging is based on a standard UART format.

Figure 45 shows the waveform for the transmit signal (UART_SOUT to UART_SIN).

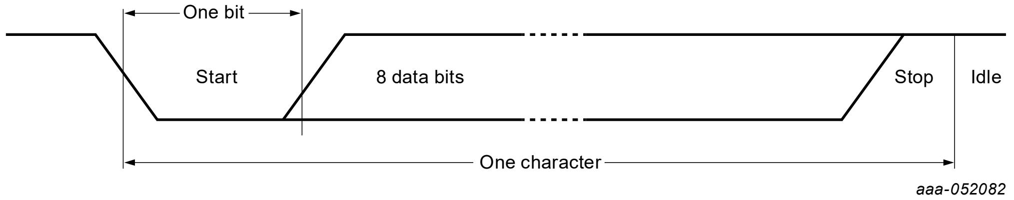


Figure 45. WCI-2 transmit signal waveform

Table 59. WCI-2 interface transport settings

Parameter	Range	Note
Baud rate	921600 ~ 4000000	Baud
Data bits	8	LSB first
Parity bits	0	No parity
Stop bit	1	One stop bit
Flow control	No	No flow control

11.6.2 PTA interface coexistence specifications

This section illustrates how the central hardware packet traffic arbiter samples the interface signals. The sampling is based on which interface signals are being used.

Figure 46 shows PTA coexistence interface signal timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority ready at Request signal assertion
- Output: grant

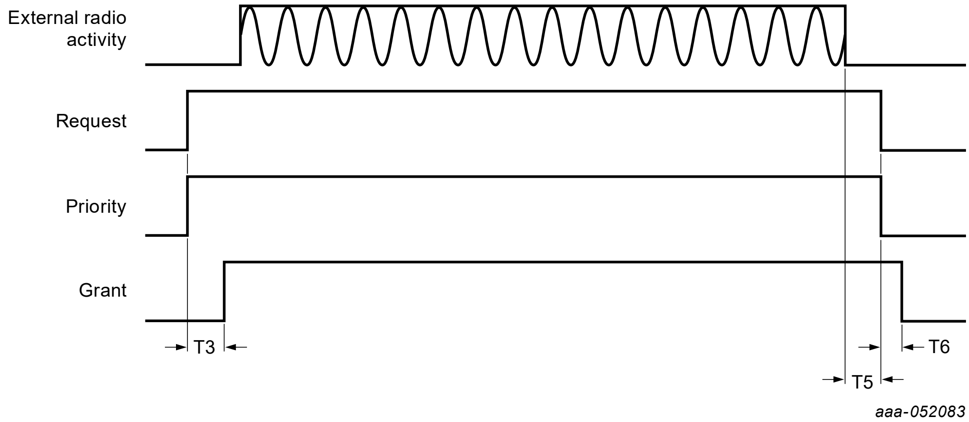


Figure 46. PTA coexistence interface timing diagram - Example 1

Figure 47 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, state
  - Priority signal and State signal are ready at Request signal assertion
- Output: grant

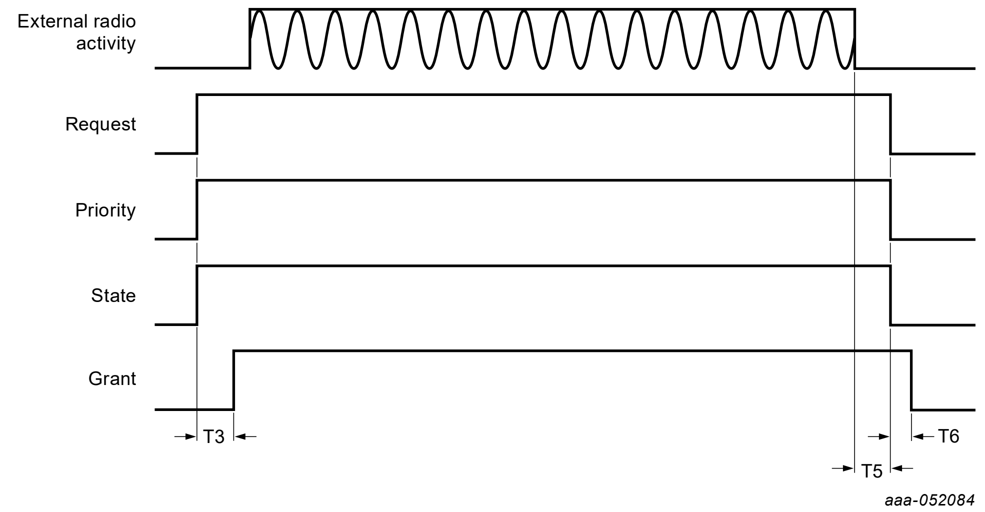


Figure 47. PTA coexistence interface timing diagram - Example 2

Figure 48 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, frequency, state
  - Priority, State, and Frequency ready at Request assertion
- Output: grant

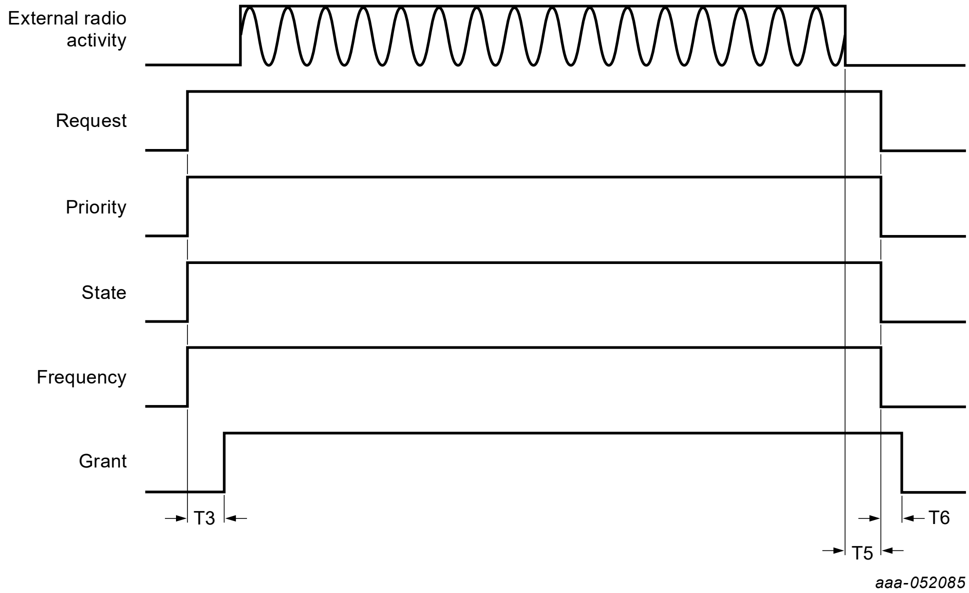


Figure 48. PTA coexistence interface timing diagram - Example 3

Figure 49 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority signal is ready at Request signal assertion
- Output: grant
  - Grant signal is de-asserted before Request signal de-assertion due to a traffic abort caused by other traffic with higher priority

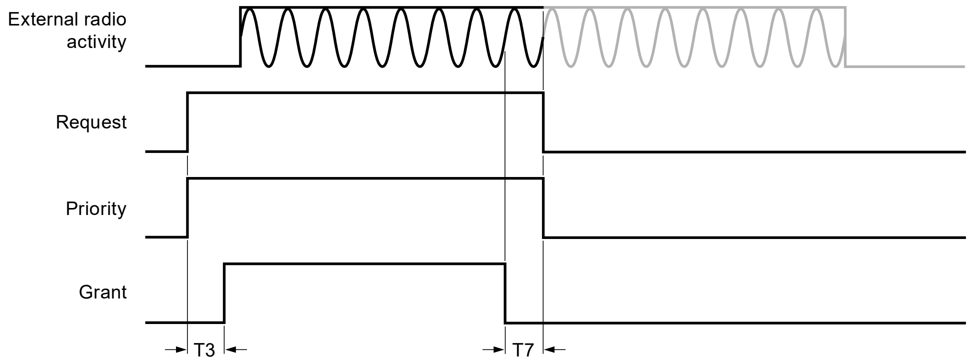


Figure 49. PTA coexistence interface timing diagram - Example 4

Figure 50 shows PTA coexistence interface timing diagram for the example where:

- Input: request and priority
  - Priority pin is sampled three times to obtain two priority bits and Tx/Rx info. No input from State pin.
- Output: grant

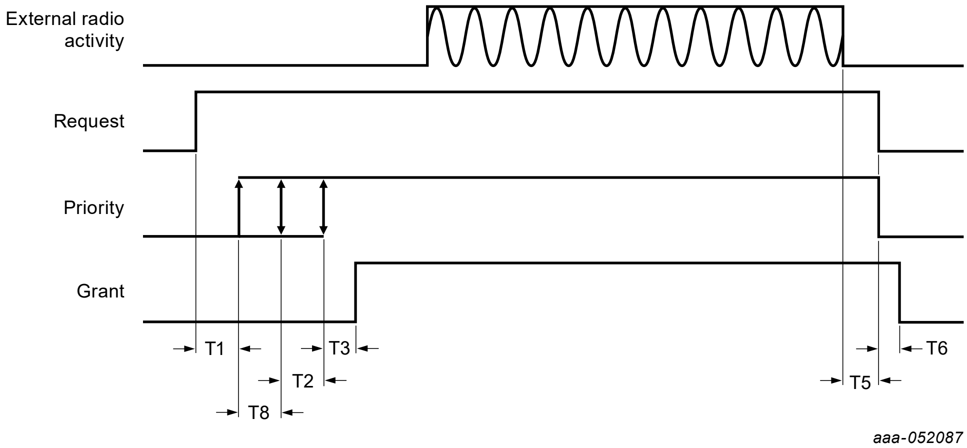


Figure 50. PTA coexistence interface timing diagram - Example 5

Table 60 provides the timing specifications for PTA coexistence interface signals.

Table 60. PTA coexistence interface signal timing data

Parameter[1]	Conditions	Min	Typ.	Max	Unit
T1	Priority[0] is sampled on Priority pin at T1 from Request assertion.	0	—	100	μs
T8	Optional: priority[1], if present on Priority pin, is sampled at T1+T8 from Request assertion.	0.025	—	100	μs
T2	Optional: Tx/Rx Info, if present on Priority pin, is sampled at T1+T2 (one priority bit on Priority pin) or T1+T8+T2 (two priority bits on Priority pin) from Request assertion.	0.025	—	100	μs
T3	Time from all information available to BCA to grant decision ready	0.1	—	0.4	μs
T5	The Request signal de-asserts T5 after the last symbol is done	—	—	—	μs
T6	The Grant signal de-asserts T6 after the Request de-assertion	0.1	—	0.3	μs
T7	The Request signal de-asserts T7 after the grant de-assertion due to a traffic abort.	—	—	—	μs

[1] T1, T2, and T8 are valid for serially sampled Priority pin.
T3, T5, T6, and T7 are valid for all implementations.

11.7 Host configuration specifications

For a list of configuration pins, see Section 6.5.15 "Host configuration".

Table 61. Configuration pin specifications[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal weak pull-up resistance	Around 1 ms following any reset	–	800	–	kΩ
Internal weak pull-down resistance	Around 1 ms following any reset	–	700	–	kΩ
Internal nominal pull-up resistance	Around 1 ms following any reset	–	100	–	kΩ
Internal nominal pull-down resistance	Around 1 ms following any reset	–	90	–	kΩ

[1] After approximately 1 ms, the configuration pins become functional pins.

11.8 Reference clock specifications

11.8.1 External crystal specifications

Table 62. External crystal specifications

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fundamental frequencies	—	—	40	—	MHz
Resonance mode	—	—	A1, Fundamental	—	—
Equivalent differential load capacitance	—	7	8	9	pF
Shunt capacitance	—	—	2	—	pF
Frequency tolerance	Over process at 25ºC	-10	—	+10	ppm
Frequency stability	Over operating temperature	-10	—	+10	ppm
Aging	—	-2	—	+2	ppm/ 5 years
Series resistance (ESR)	40 MHz	—	—	40	Ω
Insulation resistance	at DC 100V	500	—	—	MΩ
Maximum drive level	—	120	—	—	µW

11.8.2 External crystal oscillator specifications

The reference clock from external crystal oscillator requires CMOS input signal or a clipped sinusoidal signal.

Table 63. Clock DC specifications[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Single-ended high-level voltage	—	—	—	1.8	V
Single-ended low-level voltage	—	0	—	—	V
Clock amplitude (pk-pk)[2]	—	0.5	—	1.8	V
Mid-point slope	—	125	—	—	MV/s

[1] AC-coupling capacitor is integrated into IW623S.
[2] Minimum 0.8V for clipped sinusoidal signal.

Table 64. 40 MHz clock timing

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO40 period	—	25.00 - 20 ppm	25.00	25.00 + 20 ppm	ns
XO40 rise time	—	—	2.00	—	ns
XO40 fall time	—	—	2.00	—	ns
XO40 duty cycle	—	47	50	53	%

Table 65. Phase noise

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 40 MHz	Offset = 1 kHz	—	—	-130	dBc/Hz
	Offset = 10 kHz	—	—	-145	dBc/Hz
	Offset = 100 kHz	—	—	-155	dBc/Hz
	Offset > 1 MHz	—	—	-162	dBc/Hz

11.9 Power-down specifications

11.9.1 PDn asserted low—Power supplies remain high

Figure 51 and Table 66 show the specifications for PDn signal when it is asserted (low) while all power supplies to the device are high.

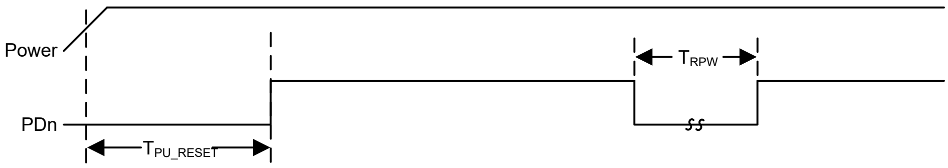


Figure 51. PDn pin (power-down) timing—Power remains high at PDn assertion

Table 66. PDn pin (power-down) specifications—Power remains high at PDn assertion

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	—	0	—	—	ms
T_{RPW}	PDn pulse width	—	1 [1]	—	—	µs
V_{IH}	Input high voltage	—	1.4	—	4.5	V
V_{IL}	Input low voltage	—	-0.4	—	0.5	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

11.9.2 PDn asserted low—1 or more power supplies ramp down

The following table and figure show the specifications for the PDn signal when it is asserted (low) while one or more of the power supplies (including VCORE) ramps down. When PDn is asserted, the integrated Buck regulator used to supply power to VCORE ramps down as specified below.

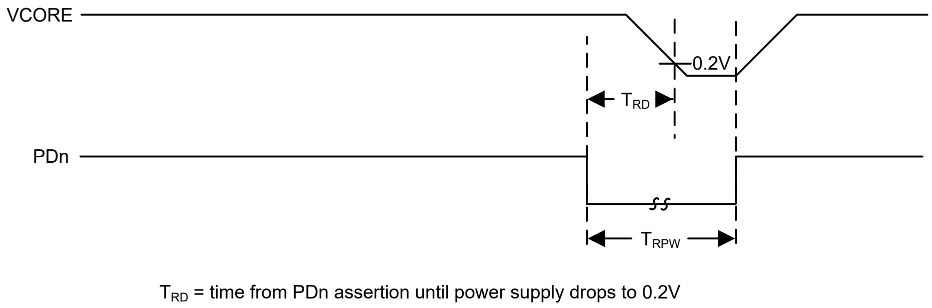


Figure 52. Power down (PDn) pin timing—Power ramps down at PDn assertion

Table 67. PDn pin specifications—Power ramps down at PDn assertion

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	--	0	--	--	ms
T_{RPW}	PDn pulse width	--	T_{RD}[1]	--	--	µs
V_{IH}	Input high voltage	--	1.4	--	4.5	V
V_{IL}	Input low voltage	--	-0.4	--	0.2	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

11.10 JTAG interface specifications

The test interface pins are powered by VIO voltage supply.

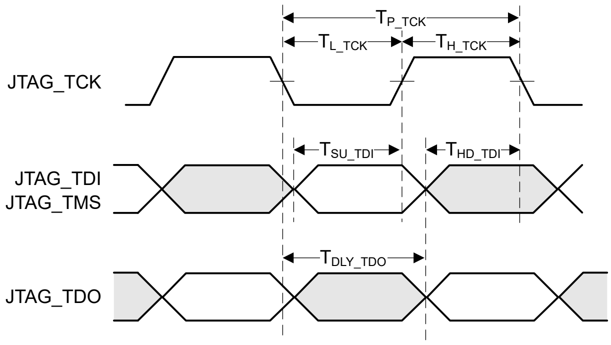


Figure 53. JTAG timing diagram

Table 68. JTAG timing data[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_TCK}	TCK period	—	40	—	—	ns
T_{H_TCK}	TCK high	—	12	—	—	ns
T_{L_TCK}	TCK low	—	12	—	—	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	—	10	—	—	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	—	10	—	—	ns
T_{DLY_TDO}	TCK to TDO delay	—	0	—	15	ns

[1] Does not apply to JTAG enabled by the JTAG_TMS pin.

12 Package information

12.1 Package thermal conditions

12.1.1 HVQFN thermal conditions

Table 69. Package thermal conditions—HVQFN148

Symbol	Rating	Board type[1]	Value	Unit
Rthj-a/θja	Junction to ambient thermal resistance [2]	JESD51-9, 2s2p board	25	°C/W
Psij-top/Ψj-top	Junction to top of package thermal characterization parameter[2]	JESD51-9, 2s2p board	3.4	°C/W

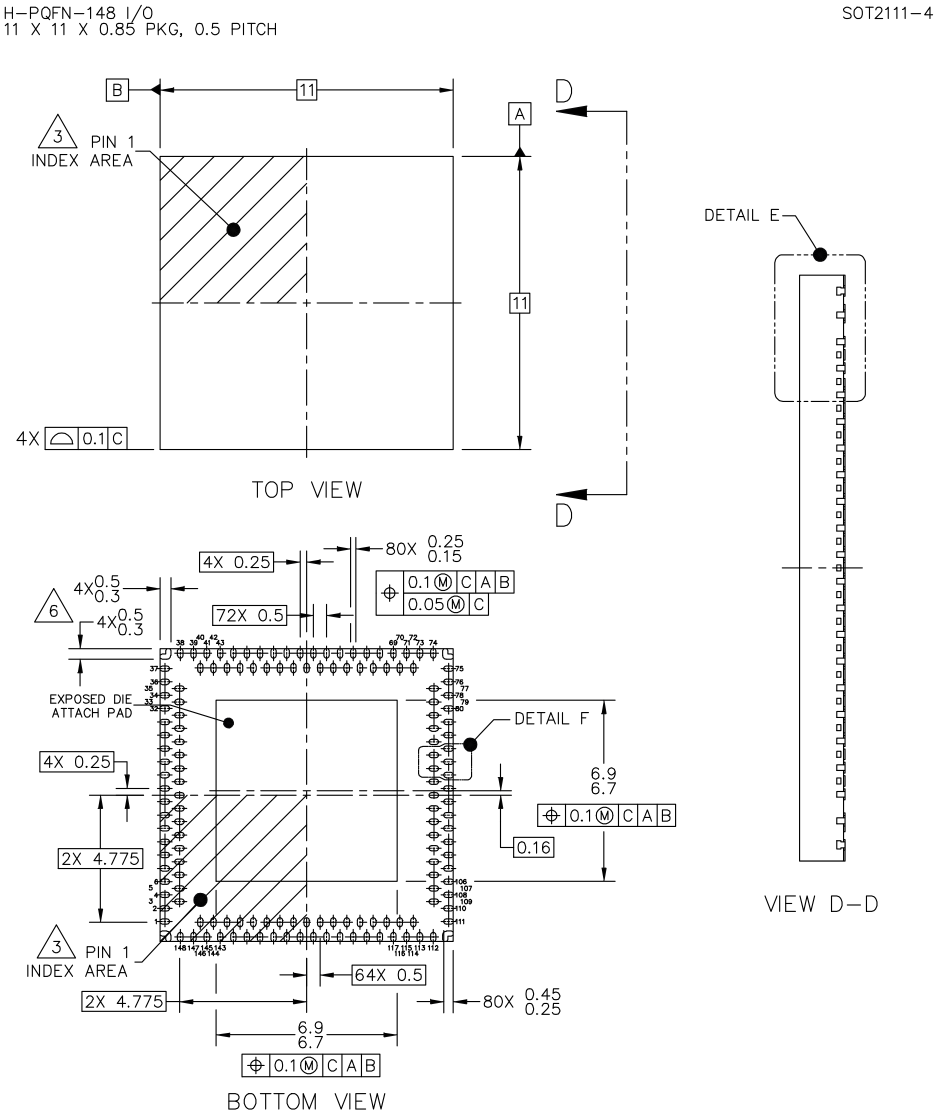
[1] The thermal test board meets JEDEC specification for this package (JESD51-9).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

12.2 Package mechanical drawings

Table 70. Package information

Package name	Link to package information on NXP website
HVQFN148	SOT-2111-4

12.2.1 HVQFN mechanical drawing



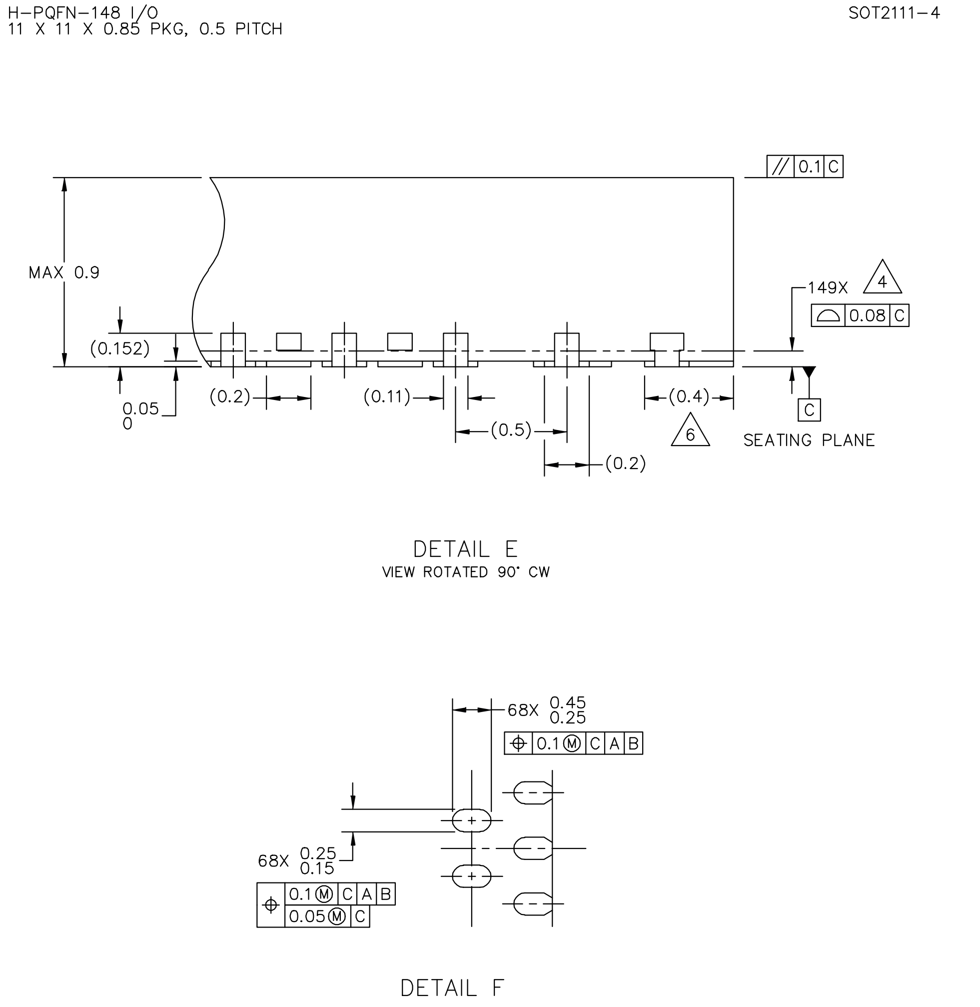
 DATE: 16 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02005D	REVISION: O	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.

Figure 54. HVQFN148 package mechanical drawing



DATE: 16 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02005D	REVISION: 0	

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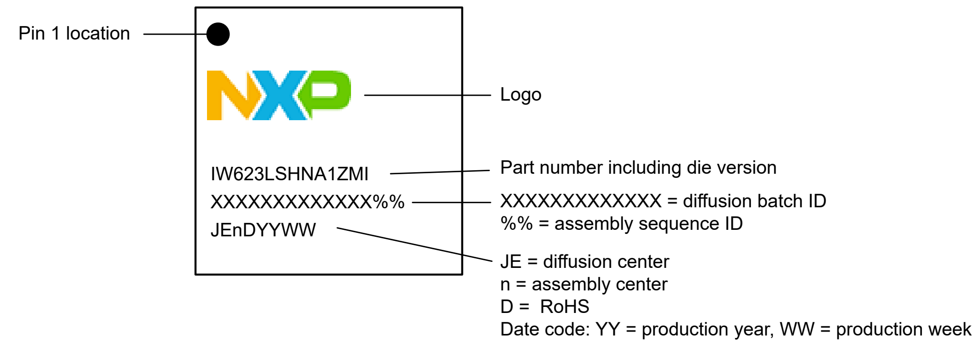
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.

Figure 55. Details E and F of HVQFN148 package mechanical drawing

12.3 Package marking

12.3.1 HVQFN marking

IW623S marking for HVQFN package and SDIO host interface for Wi-Fi.



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 56. IW623S marking for HVQFN package – SDIO host interface for Wi-Fi

13 Abbreviations

Table 71. Abbreviations

Abbreviation	Definition
A2DP	Advanced audio distribution profiles
ACK	Acknowledgment
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AFH	Adaptive frequency hopping
AGC	Automatic gain control
AP	Access point
Arm	Advanced RISC machine
BDR	Basic data rate
BOM	Bill of materials
BRF	Bluetooth RF unit
BSS	Basic service set
BTM	BSS transition management
CBC	Cipher block chaining
CCA	Clear channel assessment
CCK	Complementary code keying
CCMP	Counter mode CBC-MAC protocol
CMD	Command
CRC	Cyclic redundancy check
CTS	Clear to send
DAC	Digital-to-analog converter
DCF	Distributed coordination function
DFS	Dynamic frequency selection
DMA	Direct memory access
DPD	Digital pre distortion
DQPSK	Differential quadrature phase shift keying
DTIM	Delivery traffic indication message
EAP	Extensible authentication protocol
ED	Energy detect
EDCA	Enhanced distributed channel access
FIFO	First in first out
GATT	Generic attribute profile
GCMP	Galois/counter mode protocol
GI	Guard interval

Table 71. Abbreviations*...continued*

Abbreviation	Definition
GPIO	General purpose input/output
HID	Human interface device
HT	High throughput
HVQFN	Thermal enhanced very thin quad flat package
HW	Hardware
I/F	Interface
I/Q	In-phase/quadrature
IEEE	Institute of electrical and electronics engineers
JEDEC	Joint electronic device engineering council
JTAG	Joint test action group
LC3	Low complexity communication codec
LDPC	Low density parity check
LE	Low energy
LED	Light emitting diode
LNA	Low noise amplifier
LSB	Least significant byte
LTE	Long term evolution
MAC	Media/medium access controller
MCS	Modulation and coding scheme
MFP	Multi functional pin
MIMO	Multiple input multiple output
MPDU	MAC protocol data unit
MSb	Most significant bit
MSB	Most significant byte
MU-MIMO	Multi user MIMO
MU-PPDU	Multi user PPDU
MWS	Mobile wireless system Multimedia wireless system
NAV	Network allocation vector
NBS	Narrow band speech
NDP	Null data packet
Nsts	Number of space time streams
OFDM	Orthogonal frequency division multiplexing
OFDMA	Orthogonal frequency division multiple access
OTP	One time programmable
OTT	Over-the-top (device)

Table 71. Abbreviations*...continued*

Abbreviation	Definition
PA	Power amplifier
PCI	Peripheral component interconnect
PCM	Pulse code modulation
PDn	Power down
PHY	Physical layer
POS	Point of sale
PPDU	PHY protocol data unit
PSK	Pre shared keys
PTA	Packet traffic arbitration
QAM	Quadrature amplitude modulation
QFN	Quad flat non-leaded package
RF	Radio frequency
RIFS	Reduced inter frame space
RISC	Reduced instruction set computer
RSSI	Receiver signal strength indication
RTC	Real time clock
RTS	Request to send
SISO	Single input single output
SoC	System-on-chip
SPDT	Single pole double throw
SPI	Serial peripheral interface
STA	Station
TA	Transmitter address
TCP/IP	Transmission control protocol/internet protocol
TKIP	Temporal key integrity protocol
TWT	Target wake time
UART	Universal asynchronous receiver/transmitter
UDP	User datagram protocol
VHT	Very high throughput
WAP	Wireless application protocol
WBS	Wide band speech
WCI-2	Wireless coexistence interface 2
WEP	Wired equivalent privacy
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless local area network
WLCSP	Wafer level chip scale package

Table 71. Abbreviations*...continued*

Abbreviation	Definition
WPA	Wi-Fi protected access
WPA2	Wi-Fi protected access 2
WPA2-PSK	Wi-Fi protected access 2 - pre shared key
WPA3	Wi-Fi protected access 3
WPA-PSK	Wi-Fi protected access - pre shared key

14 Appendix

14.1 Wi-Fi channel list

Table 72 "List of supported Wi-Fi channels" lists the channels for 2.4 GHz, 5 GHz, and 6 GHz Wi-Fi.

Table 72. List of supported Wi-Fi channels

Channel number	Frequency	Channel number	Frequency	Channel number	Frequency
2.4 GHz channel					
1	2412 MHz	2	2417 MHz	3	2422 MHz
4	2427 MHz	5	2432 MHz	6	2437 MHz
7	2442 MHz	8	2447 MHz	9	2452 MHz
10	2457 MHz	11	2462 MHz	12	2467 MHz
13	2472 MHz	—	—	—	—
5 GHz channel					
36	5180 MHz	40	5200 MHz	44	5220 MHz
48	5240 MHz	52	5260 MHz	56	5280 MHz
60	5300 MHz	64	5320 MHz	100	5500 MHz
104	5520 MHz	108	5540 MHz	112	5560 MHz
116	5580 MHz	120	5600 MHz	124	5620 MHz
128	5640 MHz	132	5660 MHz	136	5680 MHz
140	5700 MHz	144	5720 MHz	149	5745 MHz
153	5765 MHz	157	5785 MHz	161	5805 MHz
165	5825 MHz	169	5845 MHz	173	5865 MHz
177	5885 MHz	—	—	—	—
6 GHz channel					
1	5955 MHz	5	5975 MHz	9	5995 MHz
13	6015 MHz	17	6035 MHz	21	6055 MHz
25	6075 MHz	29	6095 MHz	33	6115 MHz
37	6135 MHz	41	6155 MHz	45	6175 MHz
49	6195 MHz	53	6215 MHz	57	6235 MHz
61	6255 MHz	65	6275 MHz	69	6295 MHz
73	6315 MHz	77	6335 MHz	81	6355 MHz
85	6375 MHz	89	6395 MHz	93	6415 MHz
97	6435 MHz	101	6455 MHz	105	6475 MHz
109	6495 MHz	113	6515 MHz	117	6535 MHz
121	6555 MHz	125	6575 MHz	129	6595 MHz
133	6615 MHz	137	6635 MHz	141	6655 MHz
145	6675 MHz	149	6695 MHz	153	6715 MHz

Table 72. List of supported Wi-Fi channels*...continued*

Channel number	Frequency	Channel number	Frequency	Channel number	Frequency
157	6735 MHz	161	6755 MHz	165	6775 MHz
169	6795 MHz	173	6815 MHz	177	6835 MHz
181	6855 MHz	185	6875 MHz	189	6895 MHz
193	6915 MHz	197	6935 MHz	201	6955 MHz
205	6975 MHz	209	6995 MHz	213	7015 MHz
217	7035 MHz	221	7055 MHz	225	7075 MHz
229	7095 MHz	233	7115 MHz	—	—

15 Revision history

Table 73. Revision history

Document ID	Release date	Description
IW623S v.5.0	30 March 2026	Product data sheet • Changed the access to public. • No changes in the content.
IW623S v.4.0	17 November 2025	Objective data sheet **Electrical specifications** • Section 10.1.2 "2.4 GHz Wi-Fi receiver performance – 2A/2B RF paths": Table 33 updated. • Section 10.1.3 "5 GHz Wi-Fi receiver performance - 5A/5B RF paths": Table 34 updated. • Section 10.1.4 "6 GHz Wi-Fi receiver performance – 5A/5B RF paths": Table 35 updated. • Section 10.2.1 "Bluetooth/Bluetooth LE receiver performance": Table 39 updated. • Section 10.2.2 "Bluetooth/Bluetooth LE transmitter performance": Table 40 updated. • Section 10.3 "Current consumption": Table 41 updated.
IW623 v.3.0	13 August 2025	Objective data sheet **Ordering information** • Section 2 "Ordering information": added footnotes about the host interface configurations for QFN package. **Pin information** • Section 6.5.2 "General purpose I/O (GPIO)": removed oscillator enable mode for GPIO[0]. • Section 6.5.16 "Clock interface": removed XOSC_EN. • Section 6.6 "Configuration pins ": updated. **Electrical specifications** • Section 10.3 "Current consumption": updated the description of peak current mode.
IW623 v.2.0	14 July 2025	Objective data sheet **Pin information** • Section 6.2 "Pin assignment – HVQFN package": updated. • Section 6.4 "Pin list – HVQFN package": corrected pin numbers 124 and 125. **Electrical specifications** • Section 11.7 "Host configuration specifications": added the values for power-down resistance. • Section 11.8.2 "External crystal oscillator specifications ": updated the phase noise value for Offset = 100 kHz.
IW623 v.1.0	2 May 2025	Objective data sheet • Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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