MC9S08GW64 Series
Covers: MC9S08GW64 and MC9S08GW32

8-Bit HCS08 Central Processor Unit (CPU)

- New version of S08 core with same performance as traditional S08 and lower power
- Up to 20 MHz CPU at 3.6 V to 2.15 V and up to 10 MHz CPU at 3.6 V to 1.8 V, across temperature range of –40 °C to 85 °C
- HC08 instruction set with added BGND instruction
- Support for up to 48 interrupt/reset sources

On-Chip Memory

- Flash read/program/erase over full operating voltage and temperature
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and flash contents

Power-Saving Modes

- Two low power stop modes and reduced power wait mode
- Low power run and wait modes allow peripherals to run while voltage regulator is in standby
- Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
- Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
- 6 µs typical wakeup time from stop3 mode

Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; Crystal or ceramic resonator of 32.768 kHz; Clock source for iRTC or ICS
- Oscillator (XOSC2) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz; optional clock source for ICS
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference (XOSC1, XOSC2); precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting CPU/bus frequencies from 1 MHz to 20 MHz

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
- Low-voltage warning with interrupt
- Low-voltage detection with reset or interrupt
- Illegal opcode and illegal address detection with reset
- Flash block protection

Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus 3 more breakpoints in breakpoint unit)
- Breakpoint (BKPT) debug module containing three comparators (A, B, and C) with ability to match addresses in 64 KB space. Each

Peripherals

- LCD — up to 4×40 or 8×36 LCD driver with internal charge pump and option to provide an internally regulated LCD reference that can be trimmed for contrast control
- ADC6 — two analog-to-digital converters; 16-bit resolution; one dedicated differential per ADC; up to 16-ch; up to 2.5 µs conversion time for 12-bit mode; automatic compare function; hardware averaging; calibration registers; temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
- PRACMP — three rail to rail programmable reference analog comparator; up to 8 inputs; on-chip programmable reference generator output; selectable interrupt on rising, falling, or either edge of comparator output; operation in stop3
- SCI — four full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge; SC10 designed for AMR operation; TxD of SCI1 and SCI2 can be modulated with timers and RxD can received through PRACMP
- SPI — three full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting; SPI0 designed for AMR operation
- IIC — up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supporting broadcast mode and 10-bit addressing; supporting SM BUS functionality; can wake from stop3
- FTM — 2-channel flextimer module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- IRTC — independent real-time clock, independent power domain, 32 bytes RAM, 32.768 kHz input clock optional output to ICS, hardware calendar, hardware compensation due to crystal or temperature characteristics, tamper detection and indicator
- PCRC — 16/32 bit programmable cyclic redundancy check for high-speed CRC calculation
- MTIM — two 8-bit and one 16-bit timers; configurable clock inputs and interrupt generation on overflow
- PDB — programmable delay block; optimized for scheduling ADC conversions
- PCNT — position counter; working in stop3 mode without waking CPU; can be used to generate waveforms like timer

Input/Output

- 57 GPIOs including one output-only pin
- Eight KBI interrupts with selectable polarity
- Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins.

Package Options

- 80-pin LQFP, 64-pin LQFP

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

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<td>Completed all the TBDs. Updated the voltage output data in the Table 20. Changed the classification marking of</td>
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Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual  (MC9S08GW64RM)
Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.
# Devices in the MC9S08GW64 Series

Table 1 summarizes the feature set available in the MC9S08GW64 series of MCUs.

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<th>MC9S08GW32</th>
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The block diagram in Figure 1 shows the structure of the MC9S08GW64 series MCUs.
Figure 1. MC9S08GW64 Series Block Diagram
2 Pin Assignments

This section shows the pin assignments for the MC9S08GW64 series devices.

Figure 2. MC9S08GW64 Series in 80-Pin LQFP Package
Figure 3. MC9S08GW64 Series in 64-Pin LQFP Package

Table 2. Pin Availability by Package Pin-Count

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3  3  PTF0    PTF0         LCD26
4  4  PTF1    PTF1         LCD27
5  5  PTF2    PTF2         LCD28
6  6  PTF3    PTF3         LCD29
### Table 2. Pin Availability by Package Pin-Count (continued)

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Table 2. Pin Availability by Package Pin-Count (continued)

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</table>
3 Electrical Characteristics

3.1 Introduction
This section contains electrical and timing specifications for the MC9S08GW64 series of microcontrollers available at the time of publication.

3.2 Parameter Classification
The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

<table>
<thead>
<tr>
<th>P</th>
<th>Those parameters are guaranteed during production testing on each individual device.</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.</td>
</tr>
<tr>
<td>T</td>
<td>Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.</td>
</tr>
<tr>
<td>D</td>
<td>Those parameters are derived mainly from simulations.</td>
</tr>
</tbody>
</table>

NOTE
The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings
Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this device.
high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either $V_{SS}$ or $V_{DD}$) or the programmable pull-up resistor associated with the pin is enabled.

### Table 4. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td>$-0.3$ to $+3.8$</td>
<td>V</td>
</tr>
<tr>
<td>Maximum current into $V_{DD}$</td>
<td>$I_{DD}$</td>
<td>120</td>
<td>mA</td>
</tr>
<tr>
<td>Digital input voltage</td>
<td>$V_{in}$</td>
<td>$-0.3$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Instantaneous maximum current</td>
<td>$I_{D}$</td>
<td>$\pm 25$</td>
<td>mA</td>
</tr>
<tr>
<td>Single pin limit (applies to port pins except PTA5 and PTB1)</td>
<td>$I_{D}$</td>
<td>$\pm 50$</td>
<td>mA</td>
</tr>
<tr>
<td>Instantaneous maximum current</td>
<td>$I_{D}$</td>
<td>$\pm 50$</td>
<td>mA</td>
</tr>
<tr>
<td>Single pin limit (applies to PTA5 and PTB1)</td>
<td>$T_{stg}$</td>
<td>$-55$ to $150$</td>
<td>°C</td>
</tr>
</tbody>
</table>

1. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ($V_{DD}$) and negative ($V_{SS}$) clamp voltages, then use the larger of the two resistance values.

2. All functional non-supply pins are internally clamped to $V_{SS}$ and $V_{DD}$.

3. Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

### 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ will be very small.

### Table 5. Thermal Characteristics

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature range (packaged)</td>
<td>$T_A$</td>
<td>$T_I$ to $T_H$</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum junction temperature</td>
<td>$T_J$</td>
<td>95</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal resistance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single-layer board</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80-pin LQFP</td>
<td>$\theta_{JA}$</td>
<td>61</td>
<td>°C/W</td>
</tr>
<tr>
<td>64-pin LQFP</td>
<td></td>
<td>70</td>
<td>°C/W</td>
</tr>
<tr>
<td>Four-layer board</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80-pin LQFP</td>
<td>$\theta_{JA}$</td>
<td>48</td>
<td>°C/W</td>
</tr>
<tr>
<td>64-pin LQFP</td>
<td></td>
<td>52</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
Electrical Characteristics

The average chip-junction temperature \( T_J \) in °C can be obtained from:

\[
T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}
\]

where:

- \( T_A \) = Ambient temperature, °C
- \( \theta_{JA} \) = Package thermal resistance, junction-to-ambient, °C/W
- \( P_D = P_{\text{int}} + P_{I/O} \)
- \( P_{\text{int}} = I_{DD} \times V_{DD} \) - chip internal power
- \( P_{I/O} = \) Power dissipation on input and output pins — user determined

For most applications, \( P_{I/O} \ll P_{\text{int}} \) and can be neglected. An approximate relationship between \( P_D \) and \( T_J \) (if \( P_{I/O} \) is neglected) is:

\[
P_D = K \div (T_J + 273^\circ C) \quad \text{Eqn. 2}
\]

Solving 
\[
\text{Equation 1 and Equation 2 for } K \text{ gives:}
\]

\[
K = P_D \times (T_A + 273^\circ C) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}
\]

where \( K \) is a constant pertaining to the particular part. \( K \) can be determined from equation 3 by measuring \( P_D \) (at equilibrium) for a known \( T_A \). Using this value of \( K \), the values of \( P_D \) and \( T_J \) can be obtained by solving 
Equation 1 and Equation 2 iteratively for any value of \( T_A \).

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Human Body Model</td>
<td>Series resistance</td>
<td>R1</td>
<td>1500</td>
<td>Ω</td>
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<td></td>
<td>Storage capacitance</td>
<td>C</td>
<td>100</td>
<td>pF</td>
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<tr>
<td></td>
<td>Number of pulses per pin</td>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Charge Device Model</td>
<td>Series resistance</td>
<td>R1</td>
<td>0</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Storage capacitance</td>
<td>C</td>
<td>200</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>Number of pulses per pin</td>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Latch-up</td>
<td>Minimum input voltage limit</td>
<td></td>
<td>−2.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Maximum input voltage limit</td>
<td></td>
<td>7.5</td>
<td>V</td>
</tr>
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</table>
### 3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

#### Table 7. ESD and Latch-Up Protection Characteristics

<table>
<thead>
<tr>
<th>No.</th>
<th>Rating¹</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Human body model (HBM)</td>
<td>( V_{HBM} )</td>
<td>±2000</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>2</td>
<td>Machine Model (MM)</td>
<td>( V_{MM} )</td>
<td>±200</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>3</td>
<td>Charge device model (CDM)</td>
<td>( V_{CDM} )</td>
<td>±500</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>4</td>
<td>Latch-up current at ( T_A = 85°C ) (applies to all pins except pin 31EXTL1 and pin 30 XTAL1 in 80-pin package, applies to all pins except pin 23 EXTL1 and pin 24 XTAL1 in 64-pin package)</td>
<td>( I_{LAT} )</td>
<td>±100²</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Latch-up current at ( T_A = 85°C ) (applies to pin 31EXTL1 and pin 30 XTAL1 in 80-pin package, applies to pin 23 EXTL1 and pin 24 XTAL1 in 64-pin package)</td>
<td>( I_{LAT} )</td>
<td>±62³</td>
<td>—</td>
<td>mA</td>
</tr>
</tbody>
</table>

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

² These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100mA.

³ This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±62mA.

#### Table 8. DC Characteristics

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ¹</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Operating Voltage</td>
<td>( V_{DD} )</td>
<td>( V_{DD} &gt; 1.8 )</td>
<td>1.8</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>C</td>
<td>Output high voltage</td>
<td>( V_{OH} )</td>
<td>( V_{DD} &gt; 1.8 ) ( I_{Load} = -0.6 ) mA</td>
<td>( V_{DD} - 0.5 )</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All non-LCD pins low-drive strength</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>P</td>
<td></td>
<td></td>
<td>( V_{DD} &gt; 2.7 ) ( I_{Load} = -10 ) mA</td>
<td>( V_{DD} - 0.5 )</td>
<td>—</td>
<td>—</td>
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<td></td>
<td>All non-LCD pins high-drive strength</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td></td>
<td></td>
<td>( V_{DD} &gt; 1.8 ) ( I_{Load} = -3 ) mA</td>
<td>( V_{DD} - 0.5 )</td>
<td>—</td>
<td>—</td>
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</tr>
<tr>
<td>3</td>
<td>C</td>
<td>Output high voltage</td>
<td>( V_{OH} )</td>
<td>( V_{DD} &gt; 1.8 ) ( I_{Load} = -0.5 ) mA</td>
<td>( V_{DD} - 0.5 )</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All LCD/GPIO pins low-drive strength</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>P</td>
<td></td>
<td></td>
<td>( V_{DD} &gt; 2.7 ) ( I_{Load} = -2.5 ) mA</td>
<td>( V_{DD} - 0.5 )</td>
<td>—</td>
<td>—</td>
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<tr>
<td></td>
<td></td>
<td>All LCD/GPIO pins high-drive strength</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td></td>
<td></td>
<td>( V_{DD} &gt; 1.8 ) ( I_{Load} = -1 ) mA</td>
<td>( V_{DD} - 0.5 )</td>
<td>—</td>
<td>—</td>
<td></td>
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<tr>
<td>4</td>
<td>D</td>
<td>Output high current Max total ( I_{OH} ) for all ports</td>
<td>( I_{OHT} )</td>
<td></td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mA</td>
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### Electrical Characteristics

#### Table 8. DC Characteristics (continued)

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<tr>
<th>Num</th>
<th>C</th>
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<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>5 C</td>
<td>All non-LCD pins low-drive strength</td>
<td>$V_{OL}$</td>
<td>$V_{DD} &gt; 1.8 \ V$, $I_{Load} = 0.6 \ mA$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>5 P</td>
<td>All non-LCD pins high-drive strength</td>
<td>$V_{OL}$</td>
<td>$V_{DD} &gt; 2.7 \ V$, $I_{Load} = 10 \ mA$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
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<tr>
<td>5 C</td>
<td></td>
<td>$V_{OL}$</td>
<td>$V_{DD} &gt; 1.8 \ V$, $I_{Load} = 3 \ mA$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
<td></td>
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<tr>
<td>6 C</td>
<td>All LCD/GPIO pins low-drive strength</td>
<td>$V_{OL}$</td>
<td>$V_{DD} &gt; 1.8 \ V$, $I_{Load} = 0.5 \ mA$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6 P</td>
<td>All LCD/GPIO pins high-drive strength</td>
<td>$V_{OL}$</td>
<td>$V_{DD} &gt; 2.7 \ V$, $I_{Load} = 3 \ mA$</td>
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<td>—</td>
<td>0.5</td>
<td>V</td>
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<td>6 C</td>
<td></td>
<td>$V_{OL}$</td>
<td>$V_{DD} &gt; 1.8 \ V$, $I_{Load} = 1 \ mA$</td>
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<td>—</td>
<td>0.5</td>
<td>V</td>
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<td>7 D</td>
<td>Max total $I_{OL}$ for all ports</td>
<td>$I_{OLT}$</td>
<td></td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mA</td>
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<tr>
<td>8 P</td>
<td>all digital inputs</td>
<td>$V_{IH}$</td>
<td>$V_{DD} &gt; 2.7 \ V$, $0.70 \times V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
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<tr>
<td>8 C</td>
<td></td>
<td>$V_{IH}$</td>
<td>$V_{DD} &gt; 1.8 \ V$, $0.85 \times V_{DD}$</td>
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<td>—</td>
<td>—</td>
<td>V</td>
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<tr>
<td>9 P</td>
<td>all digital inputs</td>
<td>$V_{IL}$</td>
<td>$V_{DD} &gt; 2.7 \ V$, $0.35 \times V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>9 C</td>
<td></td>
<td>$V_{IL}$</td>
<td>$V_{DD} &gt; 1.8 \ V$, $0.30 \times V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
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<td>10 C</td>
<td>all digital inputs</td>
<td>$V_{hys}$</td>
<td>$0.06 \times V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>mV</td>
<td></td>
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<tr>
<td>11 P</td>
<td>all input only pins (per pin)</td>
<td>$</td>
<td>I_{In}</td>
<td>$</td>
<td>$V_{In} = V_{DD}$ or $V_{SS}$</td>
<td>—</td>
<td>0.025</td>
<td>1</td>
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<tr>
<td>12 P</td>
<td>all input/output (per pin)</td>
<td>$</td>
<td>I_{OZ}</td>
<td>$</td>
<td>$V_{In} = V_{DD}$ or $V_{SS}$</td>
<td>—</td>
<td>0.025</td>
<td>1</td>
</tr>
<tr>
<td>13 C</td>
<td>Total leakage current</td>
<td>$I_{Int}$</td>
<td>$V_{In} = V_{DD}$ or $V_{SS}$</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>14 P</td>
<td>all digital inputs, when enabled</td>
<td>$R_{PU}$, $R_{PD}$</td>
<td></td>
<td>17.5</td>
<td>—</td>
<td>52.5</td>
<td>kΩ</td>
<td></td>
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<tr>
<td>15 P</td>
<td>all digital inputs, when enabled</td>
<td>$R_{PU}$, $R_{PD}$</td>
<td></td>
<td>17.5</td>
<td>—</td>
<td>52.5</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>16 D</td>
<td>Single pin limit</td>
<td>$I_{IC}$</td>
<td>$V_{IN} &lt; V_{SS}$, $V_{IN} &gt; V_{DD}$</td>
<td>−0.2</td>
<td>—</td>
<td>0.2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>16 C</td>
<td>Total MCU limit, includes sum of all stressed pins</td>
<td>$I_{IC}$</td>
<td>$V_{IN} &lt; V_{SS}$, $V_{IN} &gt; V_{DD}$</td>
<td>−5</td>
<td>—</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>17 C</td>
<td>all pins</td>
<td>$C_{In}$</td>
<td></td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>pF</td>
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<tr>
<td>18 C</td>
<td>$V_{RAM}$</td>
<td></td>
<td></td>
<td>6.0</td>
<td>1.0</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>19 C</td>
<td>$V_{IRAM}$</td>
<td></td>
<td></td>
<td>1.05</td>
<td>—</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>20 C</td>
<td>$V_{POR}$</td>
<td></td>
<td></td>
<td>0.9</td>
<td>1.4</td>
<td>2.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>21 D</td>
<td>$I_{POR}$</td>
<td></td>
<td></td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>μs</td>
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Table 8. DC Characteristics (continued)

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>22</td>
<td>C</td>
<td>Low-voltage detection threshold</td>
<td>$V_{LVDH}$</td>
<td>High range — $V_{DD}$ falling</td>
<td>2.11</td>
<td>2.16</td>
<td>2.22</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>High range — $V_{DD}$ rising</td>
<td>2.16</td>
<td>2.23</td>
<td>2.27</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>C</td>
<td>Low-voltage detection threshold</td>
<td>$V_{LVDL}$</td>
<td>Low range — $V_{DD}$ falling</td>
<td>1.80</td>
<td>1.85</td>
<td>1.91</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low range — $V_{DD}$ rising</td>
<td>1.86</td>
<td>1.92</td>
<td>1.99</td>
<td></td>
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<tr>
<td>24</td>
<td>C</td>
<td>Low-voltage warning threshold</td>
<td>$V_{LVWH}$</td>
<td>$V_{DD}$ falling, LVWV = 1</td>
<td>2.36</td>
<td>2.46</td>
<td>2.56</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{DD}$ rising, LVWV = 1</td>
<td>2.52</td>
<td>2.49</td>
<td>2.71</td>
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<td>25</td>
<td>C</td>
<td>Low-voltage warning</td>
<td>$V_{LVWL}$</td>
<td>$V_{DD}$ falling, LVWV = 0</td>
<td>2.10</td>
<td>2.16</td>
<td>2.23</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{DD}$ rising, LVWV = 0</td>
<td>2.15</td>
<td>2.23</td>
<td>2.26</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>C</td>
<td>Low-voltage inhibit reset/recover hysteresis</td>
<td>$V_{fys}$</td>
<td>—</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td>27</td>
<td>P</td>
<td>Bandgap Voltage Reference</td>
<td>$V_{BG}$</td>
<td>1.15</td>
<td>1.17</td>
<td>1.19</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

1 Typical values are measured at 25°C. Characterized, not tested

2 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250nA.

3 All functional non-supply pins, except for PTB2 are internally clamped to VSS and $V_{DD}$.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 POR will occur below the minimum voltage.

7 Factory trimmed at $V_{DD} = 3.0$ V, Temp $= 25$°C

Figure 4. Non LCD pins I/O Pullup Typical Resistor Values
Electrical Characteristics

Figure 5. Non LCD pins I/O Pulldown Typical Resistor Values

Figure 6. Typical Low-Side Driver (Sink) Characteristics (Non LCD pins) — Low Drive (PTxDSn = 0)
Figure 7. Typical Low-Side Driver (Sink) Characteristics (Non LCD pins) — High Drive (PTxDSn = 1)
Figure 8. Typical High-Side (Source) Characteristics (Non LCD pins)—Low Drive (PTxDSn = 0)
Figure 9. Typical High-Side (Source) Characteristics (Non LCD pins) — High Drive (PTxDSn = 1)
Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO pins) — Low Drive (PTxDSn = 0)
Figure 11. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO pins) — High Drive (PTxDSn = 1)
Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO pins)—Low Drive (PTxDSn = 0)
### 3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

#### Table 9. Supply Current Characteristics

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Bus Freq</th>
<th>( V_{DD} )</th>
<th>( \text{Typ} )</th>
<th>Max</th>
<th>Unit</th>
<th>Temp (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C</td>
<td>Run supply current FEI mode, all modules on, running from Flash</td>
<td>( R_{ID} )</td>
<td>20 MHz</td>
<td>3</td>
<td>17.4</td>
<td>20.5</td>
<td>mA</td>
<td>-40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td></td>
<td></td>
<td>2 MHz</td>
<td></td>
<td>2.6</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2</td>
<td>C</td>
<td>Run supply current FEI mode, all modules off, running from Flash</td>
<td>( R_{ID} )</td>
<td>20 MHz</td>
<td>3</td>
<td>10.5</td>
<td>—</td>
<td>mA</td>
<td>-40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td></td>
<td></td>
<td>2 MHz</td>
<td></td>
<td>1.6</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>3</td>
<td>T</td>
<td>Run supply current LPRS=0, all modules off, running from Flash</td>
<td>( R_{ID} )</td>
<td>16 kHz FBILP</td>
<td>3</td>
<td>158</td>
<td>—</td>
<td>μA</td>
<td>-40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>T</td>
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<td>16 kHz FBELP</td>
<td></td>
<td>148</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>4</td>
<td>T</td>
<td>Run supply current LPRS=1, all modules off; running from Flash</td>
<td>( R_{ID} )</td>
<td>16 kHz FBILP</td>
<td>3</td>
<td>160</td>
<td>—</td>
<td>μA</td>
<td>-40 to 85°C</td>
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<td></td>
<td>T</td>
<td></td>
<td></td>
<td>16 kHz FBELP</td>
<td></td>
<td>23</td>
<td>—</td>
<td>—</td>
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### Electrical Characteristics

#### Table 9. Supply Current Characteristics

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Bus Freq</th>
<th>$V_{DD}$ (V)</th>
<th>Typ¹</th>
<th>Max</th>
<th>Unit</th>
<th>Temp (°C)</th>
</tr>
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<tr>
<td>5</td>
<td>T</td>
<td>Run supply current, LPRS=1, all modules off; running from RAM</td>
<td>$R_{DD}$</td>
<td>16 kHz</td>
<td>3</td>
<td>137</td>
<td>—</td>
<td>μA</td>
<td>−40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td></td>
<td></td>
<td>16 kHz</td>
<td>8</td>
<td>—</td>
<td></td>
<td></td>
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<tr>
<td>6</td>
<td>C</td>
<td>Wait mode supply current, all modules off</td>
<td>$W_{DD}$</td>
<td>20 MHz</td>
<td>3</td>
<td>5.4</td>
<td>7.5</td>
<td>mA</td>
<td>−40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td></td>
<td></td>
<td>2 MHz</td>
<td></td>
<td>1.1</td>
<td>—</td>
<td></td>
<td></td>
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<tr>
<td>7</td>
<td>T</td>
<td>Wait mode supply current, LPRS = 0, all modules off</td>
<td>$W_{DD}$</td>
<td>16 kHz</td>
<td>3</td>
<td>131</td>
<td>—</td>
<td>μA</td>
<td>−40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td></td>
<td></td>
<td>16 kHz</td>
<td>123</td>
<td>—</td>
<td>μA</td>
<td>−40 to 85°C</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>T</td>
<td>Wait mode supply current, LPRS = 1, all modules off</td>
<td>$W_{DD}$</td>
<td>16 kHz</td>
<td>3</td>
<td>159</td>
<td>—</td>
<td>μA</td>
<td>−40 to 85°C</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td></td>
<td></td>
<td>16 kHz</td>
<td>5.6</td>
<td>—</td>
<td>μA</td>
<td>−40 to 85°C</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>C</td>
<td>Stop2 mode supply current</td>
<td>$S_{2DD}$</td>
<td>N/A</td>
<td>3</td>
<td>330</td>
<td>1000</td>
<td>nA</td>
<td>−40 to 25°C</td>
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<td>C</td>
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<td>1622</td>
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<td></td>
<td>70°C</td>
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<td></td>
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<td></td>
<td></td>
<td>6000</td>
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<td></td>
<td>85°C</td>
</tr>
<tr>
<td>10</td>
<td>C</td>
<td>Stop3 mode supply current, No clocks active</td>
<td>$S_{3DD}$</td>
<td>N/A</td>
<td>3</td>
<td>474</td>
<td>1100</td>
<td>nA</td>
<td>−40 to 25°C</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2608</td>
<td>—</td>
<td></td>
<td>70°C</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>9000</td>
<td>—</td>
<td></td>
<td>85°C</td>
</tr>
</tbody>
</table>

¹ Typical values are measured at 25°C. Characterized, not tested.

#### Table 10. Stop Mode Adders (V$_{DD}$=3V, V$_{DDA}$=V$_{DD}$)

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Parameter</th>
<th>Condition</th>
<th>Temperature (°C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40</td>
<td>25</td>
</tr>
<tr>
<td>1</td>
<td>C</td>
<td>LPO</td>
<td>RANGE = HGO = 0</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>C</td>
<td>ERREFSTEN</td>
<td>RANGE = HGO = 0</td>
<td>600</td>
<td>737</td>
</tr>
<tr>
<td>3</td>
<td>C</td>
<td>IREFSTEN¹</td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>4</td>
<td>C</td>
<td>LVD¹</td>
<td>LVDSE = 1</td>
<td>110</td>
<td>112</td>
</tr>
<tr>
<td>5</td>
<td>C</td>
<td>PRACMP¹</td>
<td>Not using the bandgap (BGBE = 0), PRG enabled</td>
<td>30</td>
<td>35</td>
</tr>
</tbody>
</table>

¹ Typical values are measured at 25°C. Characterized, not tested.
Table 10. Stop Mode Adders (continued)(V<sub>DD</sub>=3V, V<sub>DDA</sub>=V<sub>DD</sub>)

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Parameter</th>
<th>Condition</th>
<th>Temperature (°C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40</td>
<td>25</td>
</tr>
<tr>
<td>6</td>
<td>C</td>
<td>VREFO</td>
<td>Not using the bandgap (BGBE = 0), in tight regulation mode</td>
<td>264</td>
<td>286</td>
</tr>
<tr>
<td>7</td>
<td>C</td>
<td>IRTC</td>
<td></td>
<td>1.4</td>
<td>1.65</td>
</tr>
<tr>
<td>8</td>
<td>C</td>
<td>ADC&lt;sup&gt;1&lt;/sup&gt;</td>
<td>ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0), single conversion</td>
<td>78.1</td>
<td>88.5</td>
</tr>
<tr>
<td>9</td>
<td>C</td>
<td>LCD</td>
<td>VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 Segments, 32Hz frame rate, No LCD glass connected.</td>
<td>0.67</td>
<td>0.88</td>
</tr>
<tr>
<td>10</td>
<td>C</td>
<td>PCNT&lt;sup&gt;1&lt;/sup&gt;</td>
<td>32KHz clock, without PWM output</td>
<td>33</td>
<td>47</td>
</tr>
<tr>
<td>11</td>
<td>C</td>
<td>PCNT&lt;sup&gt;1&lt;/sup&gt;</td>
<td>32KHz clock, with PWM output</td>
<td>40</td>
<td>50</td>
</tr>
</tbody>
</table>

<sup>1</sup> Not available in stop2 mode.
3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C</td>
<td>Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range (RANGE = 0)</td>
<td>f_i0</td>
<td>32</td>
<td>—</td>
<td>38.4</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High range (RANGE = 1), high gain (HGO = 1)</td>
<td>f_hi</td>
<td>1</td>
<td>—</td>
<td>16</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High range (RANGE = 1), low power (HGO = 0)</td>
<td>f_hl</td>
<td>1</td>
<td>—</td>
<td>8</td>
<td>MHz</td>
</tr>
<tr>
<td>2</td>
<td>D</td>
<td>Load capacitors</td>
<td>C_1, C_2</td>
<td>See Note 2</td>
<td>See Note 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range (RANGE=0), low power (HGO=0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other oscillator settings</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D</td>
<td>Feedback resistor</td>
<td>R_F</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range, low power (RANGE=0, HGO=0)²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range, high gain (RANGE=0, HGO=1)</td>
<td></td>
<td>10</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High range (RANGE=1, HGO=X)</td>
<td></td>
<td>1</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D</td>
<td>Series resistor — —</td>
<td>R_S</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range, low power (RANGE = 0, HGO = 0)²</td>
<td></td>
<td>—</td>
<td>100</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range, high gain (RANGE = 0, HGO = 1)</td>
<td></td>
<td>—</td>
<td>0</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High range, low power (RANGE = 1, HGO = 0)</td>
<td></td>
<td>—</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High range, high gain (RANGE = 1, HGO = 1)</td>
<td></td>
<td>—</td>
<td>0</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>≥ 8 MHz</td>
<td></td>
<td>—</td>
<td>0</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 MHz</td>
<td></td>
<td>—</td>
<td>0</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz</td>
<td></td>
<td>—</td>
<td>0</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>C</td>
<td>Crystal start-up time ⁴</td>
<td>t_CSTL</td>
<td>—</td>
<td>600</td>
<td>—</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range, low power</td>
<td></td>
<td>—</td>
<td>400</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low range, high gain</td>
<td></td>
<td>—</td>
<td>5</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High range, low power</td>
<td></td>
<td>—</td>
<td>15</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>D</td>
<td>Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)</td>
<td>f_extal</td>
<td>0.03125</td>
<td>0</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FEE mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FBE or FBELP mode</td>
<td></td>
<td></td>
<td>20</td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.
2 Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.
3 See crystal or resonator manufacturer’s recommendation.
4 Proper PC board layout procedures must be followed to achieve specifications.
3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ¹</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P</td>
<td>Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 ºC</td>
<td>f_{int,ft}</td>
<td>—</td>
<td>32.768</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
<td>Average internal reference frequency - trimmed</td>
<td>f_{int,t}</td>
<td>31.25</td>
<td>—</td>
<td>39.063</td>
<td>kHz</td>
</tr>
<tr>
<td>3</td>
<td>T</td>
<td>Internal reference start-up time</td>
<td>t_{IRST}</td>
<td>—</td>
<td>—</td>
<td>6</td>
<td>μs</td>
</tr>
<tr>
<td>4</td>
<td>P</td>
<td>DCO output frequency range - untrimmed</td>
<td>f_{dco,ut}</td>
<td>12.8</td>
<td>16.8</td>
<td>21.33</td>
<td>MHz</td>
</tr>
<tr>
<td>5</td>
<td>P</td>
<td>DCO output frequency range - trimmed</td>
<td>f_{dco,t}</td>
<td>16</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>6</td>
<td>C</td>
<td>Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)</td>
<td>Δf_{dco,res,t}</td>
<td>—</td>
<td>± 0.1</td>
<td>± 0.2</td>
<td>%f_{dco}</td>
</tr>
<tr>
<td>7</td>
<td>C</td>
<td>Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)</td>
<td>Δf_{dco,res,t}</td>
<td>—</td>
<td>± 0.2</td>
<td>± 0.4</td>
<td>%f_{dco}</td>
</tr>
<tr>
<td>8</td>
<td>C</td>
<td>Total deviation from trimmed DCO output frequency over voltage and temperature</td>
<td>Δf_{dco}</td>
<td>—</td>
<td>+ 0.5</td>
<td>-1.0</td>
<td>± 2</td>
</tr>
</tbody>
</table>
Electrical Characteristics

### Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

<table>
<thead>
<tr>
<th>Num</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70°C</td>
<td>$\Delta f_{dco,t}$</td>
<td>—</td>
<td>± 0.5</td>
<td>± 1</td>
<td>%$f_{dco}$</td>
</tr>
<tr>
<td>10</td>
<td>FLL acquisition time $^2$</td>
<td>$t_{Acquire}$</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>ms</td>
</tr>
<tr>
<td>11</td>
<td>Long term jitter of DCO output clock (averaged over 2-ms interval) $^3$</td>
<td>$C_{Jitter}$</td>
<td>—</td>
<td>0.02</td>
<td>0.2</td>
<td>%$f_{dco}$</td>
</tr>
</tbody>
</table>

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{Bus}$.

Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via $V_{DD}$ and $V_{SS}$ and variation in the crystal oscillator frequency increase the $C_{Jitter}$ percentage for a given interval.

![Deviation of DCO Output from Trimmed Frequency](image)

Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

### 3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.
### 3.10.1 Control Timing

#### Table 13. Control Timing

<table>
<thead>
<tr>
<th>Num</th>
<th>C</th>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D</td>
<td>Bus frequency (t(<em>{\text{cy}}) = 1/f(</em>{\text{Bus}}))</td>
<td>(t_{\text{FBus}})</td>
<td>dc</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>2</td>
<td>D</td>
<td>Internal low power oscillator period</td>
<td>(t_{\text{LPO}})</td>
<td>700</td>
<td>—</td>
<td>1300</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>3</td>
<td>D</td>
<td>External reset pulse width(^2)</td>
<td>(t_{\text{extrst}})</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>4</td>
<td>D</td>
<td>Reset low drive</td>
<td>(t_{\text{rstdrv}})</td>
<td>34 x (t_{\text{cy}})</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>5</td>
<td>D</td>
<td>BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes</td>
<td>(t_{\text{MSSU}})</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>6</td>
<td>D</td>
<td>BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes(^3)</td>
<td>(t_{\text{MSH}})</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>7</td>
<td>D</td>
<td>IRQ pulse width</td>
<td>(t_{\text{ILIH}}, t_{\text{IHIL}})</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>8</td>
<td>D</td>
<td>Keyboard interrupt pulse width</td>
<td>(t_{\text{ILIH}}, t_{\text{IHIL}})</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>9</td>
<td>C</td>
<td>Port rise and fall time — Non-LCD Pins</td>
<td>(t_{\text{Rise}}, t_{\text{Fall}})</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low output drive (PTxDS = 0) (load = 50 pF)(^5,6)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slew rate control disabled (PTxSE = 0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slew rate control enabled (PTxSE = 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>C</td>
<td>Voltage Regulator Recovery time</td>
<td>(t_{\text{VRR}})</td>
<td>—</td>
<td>6</td>
<td>10</td>
<td>us</td>
</tr>
</tbody>
</table>

1. Typical values are based on characterization data at \(V_{DD} = 3.0\) V, 25°C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of \(t_{\text{MSH}}\) after \(V_{DD}\) rises above \(V_{LVD}\).
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% \(V_{DD}\) and 80% \(V_{DD}\) levels. Temperature range –40°C to 85°C.
6. Except for LCD pins in Open Drain mode.
3.10.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

<table>
<thead>
<tr>
<th>No.</th>
<th>C</th>
<th>Function</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D</td>
<td>External clock frequency</td>
<td>fTCLK</td>
<td>0</td>
<td>fBus/4</td>
<td>Hz</td>
</tr>
<tr>
<td>2</td>
<td>D</td>
<td>External clock period</td>
<td>tTCLK</td>
<td>4</td>
<td>—</td>
<td>t Cyc</td>
</tr>
<tr>
<td>3</td>
<td>D</td>
<td>External clock high time</td>
<td>tclkh</td>
<td>1.5</td>
<td>—</td>
<td>t Cyc</td>
</tr>
<tr>
<td>4</td>
<td>D</td>
<td>External clock low time</td>
<td>tclkl</td>
<td>1.5</td>
<td>—</td>
<td>t Cyc</td>
</tr>
<tr>
<td>5</td>
<td>D</td>
<td>Input capture pulse width</td>
<td>tICPW</td>
<td>1.5</td>
<td>—</td>
<td>t Cyc</td>
</tr>
</tbody>
</table>
3.10.3 SPI Timing

Table 15 and Figure 20 through Figure 23 describe the timing requirements for the SPI system\(^1\).\(^2\).

**Table 15. SPI Timing**

<table>
<thead>
<tr>
<th>No.</th>
<th>C</th>
<th>Function</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>D</td>
<td>Operating frequency</td>
<td>(f_{\text{op}})</td>
<td>(f_{\text{Bus}}/2048)</td>
<td>(f_{\text{Bus}}/2)</td>
<td>Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>D</td>
<td>SPSCK period</td>
<td>(t_{\text{SPSCK}})</td>
<td>2</td>
<td>2048</td>
<td>(t_{\text{cyc}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>D</td>
<td>Enable lead time</td>
<td>(t_{\text{Lead}})</td>
<td>1/2</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D</td>
<td>Enable lag time</td>
<td>(t_{\text{Lag}})</td>
<td>1/2</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
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<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D</td>
<td>Clock (SPSCK) high or low time</td>
<td>(t_{\text{WPSCK}})</td>
<td>(t_{\text{cyc}}) – 30</td>
<td>1024 (t_{\text{cyc}})</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D</td>
<td>Data setup time (inputs)</td>
<td>(t_{\text{SU}})</td>
<td>30</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>D</td>
<td>Data hold time (inputs)</td>
<td>(t_{\text{HI}})</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>D</td>
<td>Slave access time</td>
<td>(t_{\text{a}})</td>
<td>—</td>
<td>1</td>
<td>(t_{\text{cyc}})</td>
</tr>
<tr>
<td>8</td>
<td>D</td>
<td>Slave MISO disable time</td>
<td>(t_{\text{dis}})</td>
<td>—</td>
<td>1</td>
<td>(t_{\text{cyc}})</td>
</tr>
<tr>
<td>9</td>
<td>D</td>
<td>Data valid (after SPSCK edge)</td>
<td>(t_{v})</td>
<td>—</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>D</td>
<td>Data hold time (outputs)</td>
<td>(t_{\text{HO}})</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Master</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>D</td>
<td>Rise time</td>
<td>(t_{\text{RI}})</td>
<td>—</td>
<td>(t_{\text{cyc}}) – 25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>D</td>
<td>Fall time</td>
<td>(t_{\text{FI}})</td>
<td>—</td>
<td>(t_{\text{cyc}}) – 25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. There is 20 pF load on the SPI ports.
2. There are three types of SPI ports in MC9S08GW64 Series. They are ports for AMR, ports shared with LCD pads and normal ports. This timing is for normal ports condition.
Figure 20. SPI Master Timing (CPHA = 0)

Figure 21. SPI Master Timing (CPHA = 1)

NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.
Figure 22. SPI Slave Timing (CPHA = 0)

NOTE:
1. Not defined but normally MSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 1)

NOTE:
1. Not defined but normally LSB of character just received.
### 3.11 Analog Comparator (PRACMP) Electricals

#### Table 16. PRACMP Electrical Specifications

<table>
<thead>
<tr>
<th>N</th>
<th>C</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D</td>
<td>Supply voltage</td>
<td>$V_{PWR}$</td>
<td>1.8</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>C</td>
<td>Supply current (active) (PRG enabled)</td>
<td>$I_{DDACT1}$</td>
<td>—</td>
<td>—</td>
<td>60</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>C</td>
<td>Supply current (active) (PRG disabled)</td>
<td>$I_{DDACT2}$</td>
<td>—</td>
<td>—</td>
<td>40</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>C</td>
<td>Supply current (ACMP and PRG all disabled)</td>
<td>$I_{DDDIS}$</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D</td>
<td>Analog input voltage</td>
<td>$V_{AIN}$</td>
<td>$V_{SS} - 0.3$</td>
<td>—</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>C</td>
<td>Analog input offset voltage</td>
<td>$V_{AIO}$</td>
<td>—</td>
<td>5</td>
<td>40</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>C</td>
<td>Analog comparator hysteresis</td>
<td>$V_{H}$</td>
<td>3.0</td>
<td>—</td>
<td>20.0</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>P</td>
<td>Analog input leakage current</td>
<td>$I_{ALKG}$</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>C</td>
<td>Analog comparator initialization delay</td>
<td>$t_{AINIT}$</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>$\mu s$</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>C</td>
<td>Programmable reference generator inputs</td>
<td>$V_{In1(V_{DD})}$</td>
<td>1.8</td>
<td>—</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>C</td>
<td>Programmable reference generator inputs</td>
<td>$V_{In2(V_{DD})}$</td>
<td>1.8</td>
<td>—</td>
<td>2.75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>C</td>
<td>Programmable reference generator setup delay</td>
<td>$t_{PRGST}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>C</td>
<td>Programmable reference generator step size</td>
<td>$V_{step}$</td>
<td>$-0.25$</td>
<td>1</td>
<td>0.25</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>C</td>
<td>Programmable reference generator voltage range</td>
<td>$V_{prgout}$</td>
<td>$V_{in}/32$</td>
<td>—</td>
<td>$V_{in}$</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### 3.12 ADC Characteristics

These specs all assume separate $V_{DDAD}$ supply for ADC and isolated pad segment for ADC supplies and differential inputs. Spec’s should be de-rated for $V_{REFH} = V_{bg}$ condition.

#### Table 17. 16-bit ADC Operating Conditions

<table>
<thead>
<tr>
<th>Num</th>
<th>Characteristic</th>
<th>Conditions</th>
<th>Symb</th>
<th>Min</th>
<th>Typ$^1$</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Supply voltage</td>
<td>Absolute</td>
<td>$V_{DDA}$</td>
<td>1.8</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Delta to $V_{DD} (V_{DD}−V_{DDA})^2$</td>
<td>$\Delta V_{DDA}$</td>
<td>$-100$</td>
<td>0</td>
<td>100</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Delta to $V_{SS} (V_{SS}−V_{SSA})^2$</td>
<td>$\Delta V_{SSA}$</td>
<td>$-100$</td>
<td>0</td>
<td>100</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Ref Voltage High</td>
<td>$V_{REFH}$</td>
<td>1.15</td>
<td>$V_{DDA}$</td>
<td>$V_{DDA}$</td>
<td>V</td>
<td></td>
<td></td>
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</tbody>
</table>
### Table 17. 16-bit ADC Operating Conditions

<table>
<thead>
<tr>
<th>Num</th>
<th>Characteristic</th>
<th>Conditions</th>
<th>Symb</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Ref Voltage Low</td>
<td></td>
<td>VREFL</td>
<td>VSSA</td>
<td>VSSA</td>
<td>VSSA</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Input Voltage</td>
<td></td>
<td>VADIN</td>
<td>VREFL</td>
<td></td>
<td>VREFH</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Input Capacitance</td>
<td>16-bit modes 8/10/12-bit modes</td>
<td>CADIN</td>
<td>8</td>
<td>4</td>
<td>10</td>
<td>5 pF</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Input Resistance</td>
<td></td>
<td>RADIN</td>
<td>2</td>
<td>5</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>16 bit modes</td>
<td></td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>f_{ADCK} &gt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4MHz &lt; f_{ADCK} &lt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td></td>
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<tr>
<td>10</td>
<td>Analog Source Resistance</td>
<td>13/12 bit modes</td>
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<td></td>
<td>1</td>
<td></td>
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<tr>
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<td></td>
<td>f_{ADCK} &gt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4MHz &lt; f_{ADCK} &lt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td></td>
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<tr>
<td>11</td>
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<td>11/10 bit modes</td>
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<td></td>
<td>2</td>
<td></td>
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<td>f_{ADCK} &gt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4MHz &lt; f_{ADCK} &lt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>9/8 bit modes</td>
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<td></td>
<td></td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>f_{ADCK} &gt; 8MHz</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>ADC Conversion Clock Freq.</td>
<td>ADLPC = 0, ADHSC = 1</td>
<td></td>
<td></td>
<td>1.0</td>
<td>10</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
<td>ADLPC = 0, ADHSC = 0</td>
<td></td>
<td></td>
<td>1.0</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>ADLPC = 1, ADHSC = 0</td>
<td></td>
<td></td>
<td>1.0</td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.
Electrical Characteristics

Figure 24. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range\(V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}, f_{ADCK} \leq 10\text{MHz}\)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions(^1)</th>
<th>C</th>
<th>Symb</th>
<th>Min</th>
<th>Typ(^2)</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td>ADLPC = 1, ADHSC = 0</td>
<td>T</td>
<td>(I_{DDA})</td>
<td>215</td>
<td>215</td>
<td>—</td>
<td>(\mu)A</td>
<td>ADLSMP = 0 ADCO = 1</td>
</tr>
<tr>
<td>Supply Current</td>
<td>ADLPC = 0, ADHSC = 0</td>
<td>T</td>
<td>(I_{DDA})</td>
<td>540</td>
<td>540</td>
<td>—</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>ADLPC = 0, ADHSC = 1</td>
<td>T</td>
<td>(I_{DDA})</td>
<td>610</td>
<td>610</td>
<td>—</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td>Supply Current, Stop, Reset, Module Off</td>
<td>Stop, Reset, Module Off</td>
<td>C</td>
<td>(I_{DDA})</td>
<td>0.072</td>
<td>0.072</td>
<td>—</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td>ADC Asynchronous Clock Source</td>
<td>ADLPC = 1, ADHSC = 0</td>
<td>P</td>
<td>(f_{ADACK})</td>
<td>2.4</td>
<td>2.4</td>
<td>—</td>
<td>(MHz)</td>
<td></td>
</tr>
<tr>
<td>ADC Asynchronous Clock Source</td>
<td>ADLPC = 0, ADHSC = 0</td>
<td>P</td>
<td>(f_{ADACK})</td>
<td>5.2</td>
<td>5.2</td>
<td>—</td>
<td>(MHz)</td>
<td></td>
</tr>
<tr>
<td>ADC Asynchronous Clock Source</td>
<td>ADLPC = 0, ADHSC = 1</td>
<td>P</td>
<td>(f_{ADACK})</td>
<td>6.2</td>
<td>6.2</td>
<td>—</td>
<td>(MHz)</td>
<td>(f_{ADACK} = 1/f_{ADACK})</td>
</tr>
</tbody>
</table>

\(^1\) All accuracy numbers assume the ADC is calibrated with \(V_{REFH} = V_{DDAD}\)

\(^2\) Typical values assume \(V_{DDAD} = 3.0\text{V}, \text{Temp} = 25^\circ\text{C}, f_{ADACK} = 2.0\text{ MHz}\) unless otherwise stated. Typical values are for reference only and are not tested in production.
### Table 19. 16-bit ADC Characteristics \((V_{REFH} = V_{\text{DDAD}} \geq 2.7 \text{V}, V_{REFL} = V_{\text{SSAD}}, F_{\text{ADCK}} \leq 4 \text{MHz}, \text{ADHSC} = 1)\)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions(^1)</th>
<th>C</th>
<th>Symb</th>
<th>Min</th>
<th>Typ(^2)</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Unadjusted Error</td>
<td>16-bit differential mode</td>
<td>T</td>
<td>TUE</td>
<td>—</td>
<td>±16</td>
<td>+24/-24</td>
<td>LSB(^3) 32x Hardware Averaging (AVGE = %1 AVGS = %11)</td>
<td></td>
</tr>
<tr>
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<td>±1.5</td>
<td>±2.0</td>
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<td>—</td>
<td>±1.75</td>
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<td>±1.0</td>
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<td>±2.5</td>
<td>±3</td>
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<td>±0.75</td>
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<td>±0.75</td>
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<td>±16.0</td>
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<td>±1.0</td>
<td>±2.0</td>
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<td>±1.0</td>
<td>±2.0</td>
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<td>±1.0</td>
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<td>—</td>
<td>±0.5</td>
<td>±1.0</td>
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<td>9-bit differential mode</td>
<td>T</td>
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<td>±0.3</td>
<td>±0.5</td>
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<td>±0.3</td>
<td>±0.5</td>
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<tr>
<td>Zero-Scale Error</td>
<td>16-bit differential mode</td>
<td>T</td>
<td>E(_{\text{ZS}})</td>
<td>—</td>
<td>±4.0</td>
<td>+16/0</td>
<td>LSB(^2)</td>
<td>(V_{\text{ADIN}} = V_{\text{SSAD}})</td>
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<tr>
<td></td>
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<td></td>
<td></td>
<td>—</td>
<td>±4.0</td>
<td>+16/38</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>13-bit differential mode</td>
<td>T</td>
<td></td>
<td>—</td>
<td>±0.7</td>
<td>±2.0</td>
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<tr>
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<td>12-bit single-ended mode</td>
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<td>—</td>
<td>±0.7</td>
<td>±2.0</td>
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<tr>
<td></td>
<td>11-bit differential mode</td>
<td>T</td>
<td></td>
<td>—</td>
<td>±0.4</td>
<td>±1.0</td>
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<td></td>
<td>—</td>
<td>±0.4</td>
<td>±1.0</td>
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<tr>
<td></td>
<td>9-bit differential mode</td>
<td>T</td>
<td></td>
<td>—</td>
<td>±0.2</td>
<td>±0.5</td>
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<td></td>
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<tr>
<td></td>
<td>8-bit single-ended mode</td>
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<td></td>
<td>—</td>
<td>±0.2</td>
<td>±0.5</td>
<td></td>
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</table>
### Electrical Characteristics

#### Table 19. 16-bit ADC Characteristics (V\textsubscript{REFH} = V\textsubscript{DDAD} \geq 2.7V, V\textsubscript{REFL} = V\textsubscript{SSAD}, F\textsubscript{ADCK} \leq 4MHz, ADHSC=1)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions(^1)</th>
<th>C</th>
<th>Symb</th>
<th>Min</th>
<th>Typ(^2)</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-Scale Error</td>
<td>16-bit differential mode 16-bit single-ended mode</td>
<td>T</td>
<td>E\textsubscript{FS}</td>
<td>—</td>
<td>+8/0</td>
<td>+24/0</td>
<td>LSB(^2)</td>
<td>V\textsubscript{ADIN} = V\textsubscript{DDAD}</td>
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<tr>
<td></td>
<td>13-bit differential mode 12-bit single-ended mode</td>
<td>T</td>
<td>—</td>
<td>—</td>
<td>±0.7</td>
<td>±2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11-bit differential mode 10-bit single-ended mode</td>
<td>T</td>
<td>—</td>
<td>—</td>
<td>±0.4</td>
<td>±1.0</td>
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</tr>
<tr>
<td></td>
<td>9-bit differential mode 8-bit single-ended mode</td>
<td>T</td>
<td>—</td>
<td>—</td>
<td>±0.2</td>
<td>±0.5</td>
<td></td>
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<tr>
<td>Quantization Error</td>
<td>16 bit modes</td>
<td>D</td>
<td>E\textsubscript{Q}</td>
<td>—</td>
<td>-1 to 0</td>
<td>—</td>
<td>LSB(^2)</td>
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<td></td>
<td>≤13 bit modes</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±0.5</td>
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<tr>
<td>Effective Number of Bits</td>
<td>16 bit differential mode</td>
<td>C</td>
<td>ENOB</td>
<td>—</td>
<td>13.5</td>
<td>—</td>
<td>Bits</td>
<td>For ADC_DIV=1, ADC_CLK=10 MHz.</td>
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<td>Avg = 32</td>
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<td></td>
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<tr>
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<td>Avg = 16</td>
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<td>Avg = 8</td>
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<td>Avg = 4</td>
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<td>Avg = 1</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>16 bit single-ended mode</td>
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<td></td>
<td></td>
<td>12.39</td>
<td>—</td>
<td></td>
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<td></td>
<td>Avg = 32</td>
<td></td>
<td></td>
<td></td>
<td>12.34</td>
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<td>Avg = 16</td>
<td></td>
<td></td>
<td></td>
<td>12.13</td>
<td>—</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Avg = 8</td>
<td></td>
<td></td>
<td></td>
<td>11.94</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Avg = 1</td>
<td></td>
<td></td>
<td></td>
<td>11.4</td>
<td>—</td>
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<tr>
<td>Signal to Noise plus Distortion</td>
<td>See ENOB</td>
<td></td>
<td>SINAD</td>
<td>SIN(\textsubscript{AD} = 6.02 \cdot ENOB + 1.76) dB</td>
<td></td>
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<tr>
<td>Total Harmonic Distortion</td>
<td>16-bit differential mode</td>
<td>C</td>
<td>THD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Avg = 32</td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>16-bit single-ended mode</td>
<td>D</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
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<tr>
<td>Spurious Free Dynamic Range</td>
<td>16-bit differential mode</td>
<td>C</td>
<td>SFDR</td>
<td>91.0</td>
<td>96.5</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Avg = 32</td>
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<td></td>
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<tr>
<td></td>
<td>16-bit single-ended mode</td>
<td>D</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<tr>
<td>Input Leakage Error</td>
<td>all modes</td>
<td>D</td>
<td>E\textsubscript{IL}</td>
<td>I\textsubscript{IN} \cdot R\textsubscript{AS}</td>
<td>—</td>
<td>mV</td>
<td>I\textsubscript{IN} = leakage current (refer to DC characteristics)</td>
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<tr>
<td>Temp Sensor Slope</td>
<td>–40°C–25°C</td>
<td>D</td>
<td>m</td>
<td>—</td>
<td>1.646</td>
<td>—</td>
<td>mV/°C</td>
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<tr>
<td></td>
<td>25°C–125°C</td>
<td>—</td>
<td>1.769</td>
<td>—</td>
<td></td>
<td>—</td>
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<tr>
<td>Temp Sensor Voltage</td>
<td>25°C</td>
<td>D</td>
<td>V\text{TEMP25}</td>
<td>—</td>
<td>966</td>
<td>—</td>
<td>mV</td>
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3.13 VREF Characteristics

Table 20. Electrical specifications

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<th>Num</th>
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<th>Symbol</th>
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<tbody>
<tr>
<td>1</td>
<td>P</td>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td>1.80</td>
<td>3.60</td>
<td>V</td>
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<tr>
<td>2</td>
<td>P</td>
<td>Operating temperature range</td>
<td>$T_{op}$</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
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<tr>
<td>3</td>
<td>C</td>
<td>Maximum Load</td>
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<td>mA</td>
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Operation across Temperature

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<th>Max</th>
<th>Unit</th>
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<tr>
<td>4</td>
<td>P</td>
<td>Voltage output room temperature Untrimmed</td>
<td></td>
<td>1.070–1.3</td>
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<td>V</td>
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<tr>
<td>5</td>
<td>P</td>
<td>Voltage output room temperature Factory trimmed</td>
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<td>1.180–1.22</td>
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<td>V</td>
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<tr>
<td>6</td>
<td>C</td>
<td>−40 °C Factory trimmed</td>
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<td>1.19–1.200</td>
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<td>V</td>
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<tr>
<td>7</td>
<td>C</td>
<td>85 °C Factory trimmed</td>
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<td>1.185–1.200</td>
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<td>V</td>
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Load Bandwidth

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<th>Num</th>
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<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>C</td>
<td>Load Regulation Mode = 10 at 1mA load</td>
<td>Mode = 10</td>
<td>20</td>
<td>100</td>
<td>μV/mA</td>
</tr>
<tr>
<td>9</td>
<td>C</td>
<td>Line Regulation (Power Supply Rejection)</td>
<td>DC</td>
<td>±0.1 from room temp voltage</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>AC</td>
<td>−60</td>
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Power Consumption

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<th>Num</th>
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<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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<tr>
<td>10</td>
<td>C</td>
<td>Powered down Current (Stop Mode, VREFEN = 0, VRSTEN = 0)</td>
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<td></td>
<td>100</td>
<td>μA</td>
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<td>11</td>
<td>C</td>
<td>Bandgap only (Mode[1:0] 00)</td>
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<td>75</td>
<td></td>
<td>μA</td>
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<tr>
<td>12</td>
<td>C</td>
<td>Low Power buffer (Mode[1:0] 01)</td>
<td>I</td>
<td>125</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>13</td>
<td>C</td>
<td>Tight Regulation buffer (Mode[1:0] 10)</td>
<td>I</td>
<td>1.1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>14</td>
<td>C</td>
<td>Low Power and Tight Regulation (Mode[1:0] 11)</td>
<td>I</td>
<td>1.15</td>
<td></td>
<td>mA</td>
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1 Factory trim is performed at the room temperature.
3.14 LCD Specifications

Table 21. LCD Electricals, 3-V Glass

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tr>
<td>D LCD Frame Frequency</td>
<td>f_frame</td>
<td>28</td>
<td>30</td>
<td>58</td>
<td>Hz</td>
</tr>
<tr>
<td>D LCD Charge Pump Capacitance</td>
<td>C_LCD</td>
<td>100</td>
<td>100</td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>D LCD Bypass Capacitance</td>
<td>C_BYLCD</td>
<td>100</td>
<td>100</td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>D LCD Glass Capacitance</td>
<td>C_glass</td>
<td>2000</td>
<td>8000</td>
<td>pF</td>
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</tr>
<tr>
<td>D V_{IREG} HRefSel = 0</td>
<td>V_{IREG}</td>
<td>.89</td>
<td>1.00</td>
<td>1.15</td>
<td>V</td>
</tr>
<tr>
<td>D V_{IREG} HRefSel = 1</td>
<td>V_{IREG}</td>
<td>1.49</td>
<td>1.67</td>
<td>1.85</td>
<td>V</td>
</tr>
<tr>
<td>D V_{IREG} TRIM Resolution</td>
<td>ΔRTRIM</td>
<td>1.5</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>D V_{IREG} Ripple HRefSel = 0</td>
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<td>.1</td>
<td>.15</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>D V_{IREG} Ripple HRefSel = 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

V_{IREG} Max can not exceed V_{DD} -0.15 V

3.15 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 22. FLASH Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>D Supply voltage for program/erase</td>
<td>V_{prog/erase}</td>
<td>1.8</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>D Supply voltage for read operation</td>
<td>V_{Read}</td>
<td>1.8</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>D Internal FCLK frequency</td>
<td>f_{FCLK}</td>
<td>150</td>
<td>200</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>D Internal FCLK period (1/FCLK)</td>
<td>t_{FcyC}</td>
<td>5</td>
<td>6.67</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P Byte program time (random location)</td>
<td>t_{prog}</td>
<td>9</td>
<td></td>
<td>t_{FcyC}</td>
<td></td>
</tr>
<tr>
<td>P Byte program time (burst mode)</td>
<td>t_{Burst}</td>
<td>4</td>
<td></td>
<td>t_{FcyC}</td>
<td></td>
</tr>
<tr>
<td>P Page erase time</td>
<td>t_{Page}</td>
<td>4000</td>
<td></td>
<td>t_{FcyC}</td>
<td></td>
</tr>
<tr>
<td>P Mass erase time</td>
<td>t_{Mass}</td>
<td>20,000</td>
<td></td>
<td>t_{FcyC}</td>
<td></td>
</tr>
<tr>
<td>D Byte program current</td>
<td>R_{IDDDBP}</td>
<td>—</td>
<td>4</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>D Page erase current</td>
<td>R_{IDDPE}</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>C Program/erase endurance</td>
<td></td>
<td>10,000</td>
<td></td>
<td>100,000</td>
<td>cycles</td>
</tr>
<tr>
<td>C Data retention</td>
<td>t_{D_ret}</td>
<td>15</td>
<td>100</td>
<td>—</td>
<td>years</td>
</tr>
</tbody>
</table>

1 The frequency of this clock is controlled by a software setting.
4 Ordering Information
This section contains the ordering information and the device numbering system for the MC9S08GW64 Series.

4.1 Device Numbering System
Example of the device numbering system:

```
<table>
<thead>
<tr>
<th>Status</th>
<th>Memory</th>
<th>Core</th>
<th>Family</th>
<th>Package Designator</th>
<th>Temperature Range</th>
<th>Approximate Flash Size in KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC = Fully Qualified (MC)</td>
<td>9 = FLASH-based (9)</td>
<td>Core</td>
<td>9S08</td>
<td>GW 64</td>
<td>C XX</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>
```

5 Package Information and Mechanical Drawings

Table 23 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08GW64 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:
- Click on the appropriate link in Table 23, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 23) in the "Enter Keyword" search box at the top of the page.

<table>
<thead>
<tr>
<th>Pin Count</th>
<th>Package Type</th>
<th>Abbreviation</th>
<th>Designator</th>
<th>Case No.</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>Low Quad Flat Package</td>
<td>LQFP</td>
<td>LK</td>
<td>917A</td>
<td>98ASS23237W</td>
</tr>
<tr>
<td>64</td>
<td>Low Quad Flat Package</td>
<td>LQFP</td>
<td>LH</td>
<td>840F</td>
<td>98ASS23234W</td>
</tr>
</tbody>
</table>