4M Late Write HSTL

The MCM69L736C/818C is a 4M-bit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L818C (organized as 256K words by 18 bits) and the MCM69L736C (organized as 128K words by 36 bits) are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential clock (CK) inputs control the timing of read/write operations of the RAM. At the rising edge of CK, all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of CK, a cycle after address and control signals. Read data is available at the falling edge of CK.

The RAM uses HSTL inputs and outputs. The adjustable input trip-point ($V_{\text{ref}}$) and output voltage ($V_{\text{DDQ}}$) gives the system designer greater flexibility in optimizing system performance.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

The impedance of the output buffers is programmable, allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

- Byte Write Control
- Single 3.3 V $\pm 10\%$, $-5\%$ Operation
- HSTL — I/O (JEDEC Standard JESD8–6 Class I Compatible)
- HSTL — User Selectable Input Trip–Point
- HSTL — Compatible Programmable Impedance Output Drivers
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x18 or x36 Organization
- MCM69L736C/818C–5.5 = 5.5 ns
  MCM69L736C/818C–6.5 = 6.5 ns
  MCM69L736C/818C–7.5 = 7.5 ns
  MCM69L736C/818C–8.5 = 8.5 ns
- Sleep Mode Operation (ZZ Pin)
- 119–Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package
### MCM69L736C Pin Descriptions

<table>
<thead>
<tr>
<th>PBGA Pin Locations</th>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4K</td>
<td>CK</td>
<td>Input</td>
<td>Address, data in, and control input register clock. Active high.</td>
</tr>
<tr>
<td>4L</td>
<td>CR</td>
<td>Input</td>
<td>Address, data in, and control input register clock. Active low.</td>
</tr>
<tr>
<td>(a) 6K, 7K, 6L, 7L, 6M, 6N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P</td>
<td>DQx</td>
<td>I/O</td>
<td>Synchronous Data I/O.</td>
</tr>
<tr>
<td>4F</td>
<td>G</td>
<td>Input</td>
<td>Output Enable: Asynchronous pin, active low.</td>
</tr>
<tr>
<td>2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T</td>
<td>SA</td>
<td>Input</td>
<td>Synchronous Address Inputs: Registered on the rising clock edge.</td>
</tr>
<tr>
<td>5L, 5G, 3G, 3L (a), (b), (c), (d)</td>
<td>SBx</td>
<td>Input</td>
<td>Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the SW input. Has no effect on read cycles, active low.</td>
</tr>
<tr>
<td>4E</td>
<td>SS</td>
<td>Input</td>
<td>Synchronous Chip Enable: Registered on the rising clock edge, active low.</td>
</tr>
<tr>
<td>4M</td>
<td>SW</td>
<td>Input</td>
<td>Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.</td>
</tr>
<tr>
<td>4U</td>
<td>TCK</td>
<td>Input</td>
<td>Test Clock (JTAG).</td>
</tr>
<tr>
<td>3U</td>
<td>TDI</td>
<td>Input</td>
<td>Test Data In (JTAG).</td>
</tr>
<tr>
<td>5U</td>
<td>TDO</td>
<td>Output</td>
<td>Test Data Out (JTAG).</td>
</tr>
<tr>
<td>2U</td>
<td>TMS</td>
<td>Input</td>
<td>Test Mode Select (JTAG).</td>
</tr>
<tr>
<td>4D</td>
<td>ZQ</td>
<td>Input</td>
<td>Programmable Output Impedance: Programming pin.</td>
</tr>
<tr>
<td>7T</td>
<td>ZZ</td>
<td>Input</td>
<td>Enables sleep mode, active high.</td>
</tr>
<tr>
<td>4C, 2J, 4J, 6J, 4R, 3R</td>
<td>VDD</td>
<td>Supply</td>
<td>Core Power Supply.</td>
</tr>
<tr>
<td>1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U</td>
<td>VDDQ</td>
<td>Supply</td>
<td>Output Power Supply: Provides operating power for output buffers.</td>
</tr>
<tr>
<td>3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R</td>
<td>VSS</td>
<td>Supply</td>
<td>Ground.</td>
</tr>
<tr>
<td>4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4C, 4H, 1R, 7R, 1T, 2T, 6T, 6U</td>
<td>NC</td>
<td>—</td>
<td>No Connection; There is no connection to the chip.</td>
</tr>
</tbody>
</table>
## MCM69L818C Pin Descriptions

<table>
<thead>
<tr>
<th>PBGA Pin Locations</th>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4K</td>
<td>CK</td>
<td>Input</td>
<td>Address, data in, and control input register clock. Active high.</td>
</tr>
<tr>
<td>4L</td>
<td>CK</td>
<td>Input</td>
<td>Address, data in, and control input register clock. Active low.</td>
</tr>
<tr>
<td>(a) 6D, 7E, 6F, 6G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 1P</td>
<td>DQx</td>
<td>I/O</td>
<td>Synchronous Data I/O.</td>
</tr>
<tr>
<td>4F</td>
<td>G</td>
<td>Input</td>
<td>Output Enable: Asynchronous pin, active low.</td>
</tr>
<tr>
<td>2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T</td>
<td>SA</td>
<td>Input</td>
<td>Synchronous Address Inputs: Registered on the rising clock edge.</td>
</tr>
<tr>
<td>5L, 3G (a), (b)</td>
<td>SBx</td>
<td>Input</td>
<td>Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the SW input. Has no effect on read cycles, active low.</td>
</tr>
<tr>
<td>4E</td>
<td>SS</td>
<td>Input</td>
<td>Synchronous Chip Enable: Registered on the rising clock edge, active low.</td>
</tr>
<tr>
<td>4M</td>
<td>SW</td>
<td>Input</td>
<td>Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes.</td>
</tr>
<tr>
<td>4U</td>
<td>TCK</td>
<td>Input</td>
<td>Test Clock (JTAG).</td>
</tr>
<tr>
<td>3U</td>
<td>TDI</td>
<td>Input</td>
<td>Test Data In (JTAG).</td>
</tr>
<tr>
<td>5U</td>
<td>TDO</td>
<td>Output</td>
<td>Test Data Out (JTAG).</td>
</tr>
<tr>
<td>2U</td>
<td>TMS</td>
<td>Input</td>
<td>Test Mode Select (JTAG).</td>
</tr>
<tr>
<td>4D</td>
<td>ZQ</td>
<td>Input</td>
<td>Programmable Output Impedance: Programming pin.</td>
</tr>
<tr>
<td>7T</td>
<td>ZZ</td>
<td>Input</td>
<td>Enables sleep mode, active high.</td>
</tr>
<tr>
<td>4C, 2J, 4J, 6J, 4R, 3R</td>
<td>VDD</td>
<td>Supply</td>
<td>Core Power Supply.</td>
</tr>
<tr>
<td>1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U</td>
<td>VDDQ</td>
<td>Supply</td>
<td>Output Power Supply: Provides operating power for output buffers.</td>
</tr>
<tr>
<td>4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 2D, 7D, 1E, 6E, 2F, 1G, 4G, 6G, 2H, 4H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U</td>
<td>NC</td>
<td>—</td>
<td>No Connection: There is no connection to the chip.</td>
</tr>
</tbody>
</table>
**ABSOLUTE MAXIMUM RATINGS** (Voltages Referenced to VSS; See Note)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Supply Voltage</td>
<td>VDD</td>
<td>–0.5 to 4.6</td>
<td>V</td>
</tr>
<tr>
<td>Output Supply Voltage</td>
<td>VDDQ</td>
<td>–0.5 to VDD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>Voltage On Any Pin</td>
<td>VIn</td>
<td>–0.5 to VDD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>Input Current (per I/O)</td>
<td>IIN</td>
<td>±50</td>
<td>mA</td>
</tr>
<tr>
<td>Output Current (per I/O)</td>
<td>IOUT</td>
<td>±70</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>TA</td>
<td>0 to 70</td>
<td>°C</td>
</tr>
<tr>
<td>Temperature Under Bias</td>
<td>Tbias</td>
<td>–10 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>–55 to 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**PBGA PACKAGE THERMAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Ambient (Still Air)</td>
<td>RθJA</td>
<td>53</td>
<td>°C/W</td>
<td>1, 2</td>
</tr>
<tr>
<td>Junction to Ambient (@200 ft/min)</td>
<td>RθJA</td>
<td>38</td>
<td>°C/W</td>
<td>1, 2</td>
</tr>
<tr>
<td>Junction to Ambient (@200 ft/min)</td>
<td>RθJA</td>
<td>22</td>
<td>°C/W</td>
<td>1, 2</td>
</tr>
<tr>
<td>Junction to Board (Bottom)</td>
<td>RθJB</td>
<td>14</td>
<td>°C/W</td>
<td>3</td>
</tr>
<tr>
<td>Junction to Case (Top)</td>
<td>RθJC</td>
<td>5</td>
<td>°C/W</td>
<td>4</td>
</tr>
</tbody>
</table>

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

**CLOCK TRUTH TABLE**

<table>
<thead>
<tr>
<th>K, CLK</th>
<th>ZZ</th>
<th>SS</th>
<th>SW</th>
<th>SBa</th>
<th>SBb</th>
<th>SBc</th>
<th>SBd</th>
<th>DQ (n)</th>
<th>DQ (n + 1)</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>L – H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DOUT 0 – 35</td>
<td>X</td>
<td>Read Cycle All Bytes</td>
</tr>
<tr>
<td>L – H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>DIn 0 – 8</td>
<td>DIn 9 – 17</td>
<td>Write Cycle 1st Byte</td>
</tr>
<tr>
<td>L – H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>DIn 18 – 26</td>
<td>DIn 27 – 35</td>
<td>Write Cycle 2nd Byte</td>
</tr>
<tr>
<td>L – H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>DIn 0 – 35</td>
<td>DIn 0 – 35</td>
<td>Write Cycle 3rd Byte</td>
</tr>
<tr>
<td>L – H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>DIn 0 – 35</td>
<td>DIn 0 – 35</td>
<td>Write Cycle 4th Byte</td>
</tr>
<tr>
<td>L – H</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High–Z</td>
<td>High–Z</td>
<td>Abort Write Cycle</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High–Z</td>
<td>High–Z</td>
<td>Deselect Cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Sleep Mode</td>
</tr>
</tbody>
</table>

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. This device contains circuitry that will ensure the output devices are in High–Z at power up.
## DC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T<sub>A</sub> ≤ 70°C, Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS

(See Notes 1 through 4)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Max</th>
<th>Max</th>
<th>Max</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Power Supply Voltage</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>3.135</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Driver Supply Voltage</td>
<td>V&lt;sub&gt;DDQ&lt;/sub&gt;</td>
<td>1.4</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Active Power Supply Current (Device Selected,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>All Outputs Open, Freq = Max, V&lt;sub&gt;DD&lt;/sub&gt; = Max,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DDQ&lt;/sub&gt; = Max). Includes Supply Currents</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>for V&lt;sub&gt;DD&lt;/sub&gt;.</td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Active Standby Power Supply Current</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Device Deselected, Freq = Max, V&lt;sub&gt;DD&lt;/sub&gt; = Max,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DDQ&lt;/sub&gt; = Max)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMOS Standby Supply Current (Device Deselected,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Freq = 0, V&lt;sub&gt;DD&lt;/sub&gt; = Max, V&lt;sub&gt;DDQ&lt;/sub&gt; = Max)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep Mode Current (ZZ = V&lt;sub&gt;IH&lt;/sub&gt;, Freq = Max,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = Max, V&lt;sub&gt;DDQ&lt;/sub&gt; = Max)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Reference DC Voltage</td>
<td>V&lt;sub&gt;ref (dc)&lt;/sub&gt;</td>
<td>0.6</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1.1</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:

1. All data sheet parameters specified to full range of V<sub>DD</sub> unless otherwise noted. All voltages are referenced to voltage applied to V<sub>SS</sub> bumps.
2. Supply voltage applied to V<sub>DD</sub> connections.
3. Supply voltage applied to V<sub>DDQ</sub> connections.
4. All power supply currents measured with outputs open or deselected.
5. All inputs are zero.
6. CMOS levels for I/Os are V<sub>IC</sub> ≤ V<sub>SS</sub> + 0.2 V or ≥ V<sub>DDQ</sub> − 0.2 V. CMOS levels for other inputs are V<sub>in</sub> ≤ V<sub>SS</sub> + 0.2 V or ≥ V<sub>DD</sub> − 0.2 V.
7. Device deselected as defined by the Clock Truth Table.
8. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V<sub>ref</sub> is supported, the peak–to–peak ac component superimposed on V<sub>ref</sub> may not exceed 5% of the dc component of V<sub>ref</sub>.

### DC INPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Input Logic High</td>
<td>V&lt;sub&gt;IH (dc)&lt;/sub&gt;</td>
<td>V&lt;sub&gt;ref + 0.1&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD + 0.3&lt;/sub&gt;</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DC Input Logic Low</td>
<td>V&lt;sub&gt;IL (dc)&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>I&lt;sub&gt;Ikg(1)&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>±5</td>
<td>μA</td>
</tr>
<tr>
<td>Clock Input Signal Voltage</td>
<td>V&lt;sub&gt;in&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;DD + 0.3&lt;/sub&gt;</td>
<td>V</td>
</tr>
<tr>
<td>Clock Input Differential Voltage (See Figure 3)</td>
<td>V&lt;sub&gt;DIF (dc)&lt;/sub&gt;</td>
<td>0.1</td>
<td>V&lt;sub&gt;DD + 0.6&lt;/sub&gt;</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Clock Input Common Mode Voltage Range (See Figure 3)</td>
<td>V&lt;sub&gt;CM (dc)&lt;/sub&gt;</td>
<td>0.6</td>
<td>1.1</td>
<td>V</td>
<td>3</td>
</tr>
</tbody>
</table>

### NOTES:

1. 0 V ≤ V<sub>in</sub> ≤ V<sub>DD</sub> for all pins.
2. Minimum instantaneous differential input voltage required for differential input clock operation.
3. Maximum rejectable common mode input voltage variation.
### DC OUTPUT BUFFER CHARACTERISTICS — PROGRAMMABLE IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

\((V_{DD} = 3.3 \text{ V}, V_{DDQ} = 1.5 \text{ V}, T_A = 70^\circ \text{C}, \text{See Notes 1 and 2})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Logic Low</td>
<td>(I_{OL})</td>
<td>((V_{DDQ}/2) / \left(\left(RQ/5\right) + 30%))</td>
<td>((V_{DDQ}/2) / \left(\left(RQ/5\right) – 15%))</td>
<td>A</td>
<td>3</td>
</tr>
<tr>
<td>Output Logic High</td>
<td>(I_{OH})</td>
<td>((V_{DDQ}/2) / \left(\left(RQ/5\right) + 30%))</td>
<td>((V_{DDQ}/2) / \left(\left(RQ/5\right) – 15%))</td>
<td>A</td>
<td>4</td>
</tr>
<tr>
<td>Light Load Output Logic Low</td>
<td>(V_{OL1})</td>
<td>(V_{SS})</td>
<td>0.2</td>
<td>V</td>
<td>5</td>
</tr>
<tr>
<td>Light Load Output Logic High</td>
<td>(V_{OH1})</td>
<td>(V_{DDQ} – 0.2)</td>
<td>(V_{DDQ})</td>
<td>V</td>
<td>6</td>
</tr>
</tbody>
</table>

**NOTES:**
1. The impedance controlled mode is expected to be used in point–to–point applications, driving high–impedance inputs.
2. The ZQ pin is connected through RQ to \(V_{SS}\) for the controlled impedance mode.
3. \(V_{OL} = V_{DDQ}/2\).
4. \(V_{OH} = V_{DDQ}/2\).
5. \(I_{OL} \leq 100 \mu\text{A}\).
6. \(| I_{OH} | \leq 100 \mu\text{A}\).

### DC OUTPUT BUFFER CHARACTERISTICS — MINIMUM IMPEDANCE PUSH–PULL OUTPUT BUFFER MODE

\((0^\circ \text{C} \leq T_A \leq 70^\circ \text{C}, \text{ZQ} = V_{DD}, \text{See Notes 1 and 2})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Logic Low</td>
<td>(V_{OL2})</td>
<td>(V_{SS})</td>
<td>0.4</td>
<td>V</td>
<td>3</td>
</tr>
<tr>
<td>Output Logic High</td>
<td>(V_{OH2})</td>
<td>(V_{DDQ} – 0.4)</td>
<td>(V_{DDQ})</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>Light Load Output Logic Low</td>
<td>(V_{OL3})</td>
<td>(V_{SS})</td>
<td>0.2</td>
<td>V</td>
<td>5</td>
</tr>
<tr>
<td>Light Load Output Logic High</td>
<td>(V_{OH3})</td>
<td>(V_{DDQ} – 0.2)</td>
<td>(V_{DDQ})</td>
<td>V</td>
<td>6</td>
</tr>
</tbody>
</table>

**NOTES:**
1. The push–pull output mode is expected to be used in bussed applications and may be series or parallel terminated. Conforms to the JEDEC Standard JESD8–6 Class I.
2. The ZQ pin is connected to \(V_{DD}\) to enable the minimum impedance mode.
3. \(I_{OL} \geq \left| – 8 \text{ mA}\right|\).
4. \(I_{OH} \geq 8 \text{ mA}\).
5. \(I_{OL} \geq 100 \mu\text{A}\).
6. \(| I_{OH} | \geq 100 \mu\text{A}\).

### CAPACITANCE

\((f = 1.0 \text{ MHz, } dV = 3.0 \text{ V, } 0^\circ \text{C} \leq T_A \leq 70^\circ \text{C}, \text{Periodically Sampled Rather Than 100\% Tested})\)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance</td>
<td>(C_{in})</td>
<td>4</td>
<td>5</td>
<td>pF</td>
</tr>
<tr>
<td>Input/Output Capacitance</td>
<td>(C_{I/O})</td>
<td>7</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>CK, CK Capacitance</td>
<td>(C_{CK})</td>
<td>4</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>
AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ........................................ 0.25 to 1.25 V
Input Rise/Fall Time ...................................... 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level ............... 0.75 V
Output Timing Reference Level ........................... 0.75 V

Clock Input Timing Reference Level ..................... Differential Cross–Point ZO for 50 Ω Impedance .............................. 250 Ω
R_{θAJA} Device ........................................ TDB

READ/WRITE CYCLE TIMING

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>69L736C–5.5</th>
<th>69L736C–6.5</th>
<th>69L736C–7.5</th>
<th>69L736C–8.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle Time</td>
<td>t_KKH</td>
<td>5.5—6</td>
<td>6—7</td>
<td>7—8</td>
<td>8—ns</td>
</tr>
<tr>
<td>Clock High Pulse Width</td>
<td>t_KKHL</td>
<td>2.2—2.4</td>
<td>2.8—3.2</td>
<td>3.2—ns</td>
<td></td>
</tr>
<tr>
<td>Clock Low Pulse Width</td>
<td>t_KLKH</td>
<td>2.2—2.4</td>
<td>2.8—3.2</td>
<td>3.2—ns</td>
<td></td>
</tr>
<tr>
<td>Clock High to Output Valid</td>
<td>t_KHQV</td>
<td>—5.5—6.5</td>
<td>7.5—8.5</td>
<td>8.5—ns</td>
<td></td>
</tr>
<tr>
<td>Clock Low to Output Valid</td>
<td>t_KLOV</td>
<td>—2.5—2.5</td>
<td>—3—3.5</td>
<td></td>
<td>1.0–ns</td>
</tr>
<tr>
<td>Clock Low to Output Hold</td>
<td>t_KLOX</td>
<td>0.7—0.7</td>
<td>0.7—0.7</td>
<td>0.7—ns</td>
<td>1.0–ns</td>
</tr>
<tr>
<td>Clock Low to Output Low–Z</td>
<td>t_KLQX1</td>
<td>0.7—1</td>
<td>1—1</td>
<td>1—ns</td>
<td>1.0–ns, 2.0–ns</td>
</tr>
<tr>
<td>Clock High to Output High–Z</td>
<td>t_KHOZ</td>
<td>0.7—2.5</td>
<td>1—3</td>
<td>1.3—3.5</td>
<td>1.0–ns, 2.0–ns</td>
</tr>
<tr>
<td>Output Enable Low to Output Low–Z</td>
<td>t_GLOX</td>
<td>0.5—0.5</td>
<td>0.5—0.5</td>
<td>0.5–ns</td>
<td></td>
</tr>
<tr>
<td>Output Enable Low to Output Valid</td>
<td>t_GLOV</td>
<td>—2.3—2.5</td>
<td>—3—3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Enable to Output Hold</td>
<td>t_GHQX</td>
<td>0.5—0.5</td>
<td>0.5—0.5</td>
<td>0.5–ns</td>
<td></td>
</tr>
<tr>
<td>Output Enable High to Output High–Z</td>
<td>t_GHQZ</td>
<td>—2.3—2.5</td>
<td>—3—2.3</td>
<td></td>
<td>1.0–ns, 2.0–ns</td>
</tr>
<tr>
<td>ZZ High to Sleep Mode</td>
<td>t_ZZE</td>
<td>—50—50</td>
<td>—50—50</td>
<td>—50—50</td>
<td>—50–ns</td>
</tr>
<tr>
<td>ZZ Low to Recovery</td>
<td>t_ZZR</td>
<td>200—200</td>
<td>200—200</td>
<td>200—200</td>
<td>200–ns</td>
</tr>
</tbody>
</table>

NOTES:
1. This parameter is sampled and not 100% tested.
2. Measured at ±200 mV from steady state.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load
AC INPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Input Logic High (See Figure 4)</td>
<td>V_{IH} (ac)</td>
<td>V_{ref} + 200 mV</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>AC Input Logic Low (See Figures 2 and 4)</td>
<td>V_{IL} (ac)</td>
<td>—</td>
<td>V_{ref} – 200 mV</td>
<td>2</td>
</tr>
<tr>
<td>Input Reference Peak–to–Peak AC Voltage</td>
<td>V_{ref} (ac)</td>
<td>—</td>
<td>5% V_{ref} (dc)</td>
<td>3</td>
</tr>
<tr>
<td>Clock Input Differential Voltage</td>
<td>V_{dif} (ac)</td>
<td>400 mV</td>
<td>V_{DDQ} + 600 mV</td>
<td>4</td>
</tr>
</tbody>
</table>

NOTES:
1. Inputs may overshoot to V_{DD} – 1 V for 30% t_{KH/K}H and V_{DD} + 1.5 V peak overshoot.
2. Inputs may undershoot to V_{SS} – 1 V for 30% t_{KH/K}H and V_{SS} – 1.5 V peak undershoot.
3. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak–to–peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
4. Minimum instantaneous differential input voltage required for differential input clock operation.

Figure 2. Undershoot Voltage

Figure 3. Differential Inputs/Common Mode Input Voltage

*V_{CM}, the Common Mode Input Voltage, equals V_{TR} – [(V_{TR} – V_{CP})/2].

Figure 4. AC Input Conditions
SLEEP MODE TIMING

NORMAL OPERATION

NO READS OR WRITES ALLOWED

IN SLEEP MODE

NO NEW READS OR WRITES ALLOWED

NORMAL OPERATION

SLEEP MODE TIMING

CK
ADDR
MS
IZ
DQ
IZZ
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FUNCTIONAL OPERATION

READ AND WRITE OPERATIONS

All control signals except G are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at tKLQV or tKHQV, whichever is later. tKHQV is the internal latency of the device. During this same cycle, a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as tKHQZ and tDVKH are met. Read cycles may follow write cycles immediately.

G, SS, and SW control output drive. Chip deselect via a high on SS at the rising edge of the CK clock has its effect on the output drivers immediately. SW low deselects the output drivers immediately (on the same cycle). Output selecting via a low on SS and high on SW at a rising CK clock has its effect on the output drivers at tKLQX. Output drive is also controlled directly by output enable (G). G is an asynchronous input. No clock edges are required to enable or disable the output with G.

Output data will be valid at tGLQV, tKHQV, or tKLQV, which is even later. Outputs will begin driving at tKLQX. Outputs will hold previous data until tKLQX or tGHQX, or tKHQZ in the case of a write following a read.

WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term “byte” refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input (SW) apply to each of the byte write enable inputs (SBa, SBB, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte write enable inputs to active low (VSS). Reads of all bytes proceed normally and write cycles, activated via a low on SW and the rising edge of CK, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input (SW). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM can not simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active, is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

LATE WRITE

The write address is sampled on the first rising edge of clock, and write data is sampled on the following rising edge. The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to ensure coherent operation. This occurs in all cases, whether there is a byte write or a full word is written.

PROGRAMMABLE IMPEDANCE OPERATION

The designer can program the RAM’s output buffer impedance by terminating the ZQ pin to VSS through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, a 250 Ω resistor will give an output impedance of 50 Ω.

Impedance updates occur continuously and the frequency of the update is based on the subdivided CK clock. Note that if the K clock stops, so does the impedance update.

The actual change in the impedance occurs in small increments and is monotonic. There are no significant disturbances that occur on the output because of this smooth update method.

The impedance update is not related to any particular type of cycle because the impedance is updated continuously and is based on the CK clock. Updates occur regardless of whether the device is performing a read, write, or a deselect cycle and does not depend on the state of G.

At power up or recovery from sleep mode, the output impedance defaults to approximately 50 Ω. It will take 4,000 to 16,000 cycles for the impedance to be completely updated if the programmed impedance is much higher or lower than 50 Ω.

The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to VDD.

POWER UP AND INITIALIZATION

The following supply voltage application sequence is recommended: VSS, VDD, then VDDQ. Please note, per the Absolute Maximum Ratings table, VDDQ is not to exceed VDD + 0.5 V, whatever the instantaneous value of VDD. Once supplies have reached specification levels, a minimum dwell of 1.0 ms with CK clock inputs cycling is required before beginning normal operations. At power up the output impedance will be set at approximately 50 Ω as stated above.
SLEEP MODE

This device is equipped with an optional sleep or low power mode. The sleep mode pin is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the chip will enter sleep mode where the device will meet the lowest possible power conditions. The Sleep Mode Timing diagram shows the following modes of operation: Normal Operation, No Read/Write Allowed, and Sleep Mode.

Normal Operation

All inputs must meet setup and hold times prior to sleep and tZZR nanoseconds after recovering from sleep. Clock (CK) must also meet cycle high and low times during these periods. Two cycles prior to sleep, initiation of either a read or write operation is not allowed.

No Read/Write Allowed

During the period of time just prior to sleep and during recovery from sleep, the assertion of any write or read signal is not allowed. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM can not be guaranteed immediately after ZZ is asserted (prior to being in sleep). During sleep mode recovery, the output impedance must be given additional time above and beyond tZZR in order to match desired impedance (see explanation in Output Impedance Circuitry paragraph).

Sleep Mode

The RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (IZZ). All outputs will remain in a High–Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected, and perform any reads or writes.

SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. The TAP controller is the state machine that controls the TAP operation and can be expected to function in a manner that does not conflict with the operation of devices with IEEE 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B low voltage (3.3 V) TTL/CMOS logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to VSS to preclude mid–level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

(0°C ≤ TA ≤ 70°C, Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Input Logic High</td>
<td>VIL1</td>
<td>−0.3</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Input Logic Low</td>
<td>VIL1</td>
<td>−0.3</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Input Leakage Current</td>
<td>ILkg</td>
<td>—</td>
<td>±5</td>
<td>µA</td>
<td>1</td>
</tr>
<tr>
<td>CMOS Output Logic Low</td>
<td>VQL1</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>CMOS Output Logic High</td>
<td>VOH1</td>
<td>VDD</td>
<td>VDD − 0.2</td>
<td>V</td>
<td>3</td>
</tr>
<tr>
<td>TTL Output Logic Low</td>
<td>VQL2</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>TTL Output Logic High</td>
<td>VOH2</td>
<td>2.4</td>
<td></td>
<td>V</td>
<td>5</td>
</tr>
</tbody>
</table>

NOTES:
1. 0 V ≤ VIN ≤ VDDQ for all logic input pins.
2. |IOL1| ≤ 100 µA @ VQL = 0.2 V. Sampled, not 100% tested.
3. |IOH1| ≤ 100 µA @ VDDQ − 0.2 V. Sampled, not 100% tested.
4. IOL2 ≤ 8 mA @ VQL = 0.4 V.
5. |IOH2| ≤ 8 mA @ VOH = 2.4 V.
TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels ............................. 0 to 3.0 V
Input Rise/Fall Time ................. 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level .......... 1.5 V
Output Timing Reference Level ................. 1.5 V
Output Test Load ........ 50 Ω Parallel Terminated T-Line with 20 pF
Receiver Input Capacitance
Test Load Termination Supply Voltage (V_T) ............. 1.5 V

TAP CONTROLLER TIMING

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle Time</td>
<td>tTHTH</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Clock High Time</td>
<td>tTHTL</td>
<td>40</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Clock Low Time</td>
<td>tTLTH</td>
<td>40</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TMS Setup</td>
<td>tMVTH</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TMS Hold</td>
<td>tTHMX</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDI Valid to TCK High</td>
<td>tDVTH</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCK High to TDI Don't Care</td>
<td>tTHDX</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
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<tr>
<td>Capture Setup</td>
<td>tCS</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>Capture Hold</td>
<td>tCH</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>TCK Low to TDO Unknown</td>
<td>tTLQX</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCK Low to TDO Valid</td>
<td>tTLQV</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
1. tCS + tCH defines the minimum pause in RAM I/O pad transitions to ensure accurate pad data capture.

AC TEST LOAD

TAP CONTROLLER TIMING DIAGRAM
TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic 1 input level.

TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (see Figure 6). An undriven TDI pin will produce the same result as a logic 1 input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (see Figure 6). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST — TAP RESET

This device does not have a TRST pin. TRST is optional in IEEE 1149.1. The test–logic–reset state is entered while TMS is held high for five rising edges of TCK. Power–on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of 1s and 0s input to the TMS pin as the TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the subsequent falling edge of TCK. When a register is selected, it is “placed” between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run or idle state. The instructions are 3 bits long. The register can be loaded when it is placed between TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAM I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bump’s position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1–1990)

Reserved For Future Use

Device Width

Device Depth

Revision Number

Figure 5. ID Register Bit Meanings
### MCM69L736C Bump/Bit Scan Order

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Signal Name</th>
<th>Bump ID</th>
<th>Bit No.</th>
<th>Signal Name</th>
<th>Bump ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>M2</td>
<td>5R</td>
<td>16</td>
<td>SBa</td>
<td>5L</td>
</tr>
<tr>
<td>2</td>
<td>SA</td>
<td>4P</td>
<td>17</td>
<td>CK</td>
<td>4L</td>
</tr>
<tr>
<td>3</td>
<td>SA</td>
<td>4T</td>
<td>18</td>
<td>CK</td>
<td>4K</td>
</tr>
<tr>
<td>4</td>
<td>SA</td>
<td>6R</td>
<td>19</td>
<td>G</td>
<td>4F</td>
</tr>
<tr>
<td>5</td>
<td>SA</td>
<td>5T</td>
<td>20</td>
<td>DQb</td>
<td>5G</td>
</tr>
<tr>
<td>6</td>
<td>ZZ</td>
<td>7T</td>
<td>21</td>
<td>DQb</td>
<td>7H</td>
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<td>7</td>
<td>DQa</td>
<td>6P</td>
<td>22</td>
<td>DQb</td>
<td>6H</td>
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<tr>
<td>8</td>
<td>DQa</td>
<td>7P</td>
<td>23</td>
<td>DQb</td>
<td>6G</td>
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<tr>
<td>9</td>
<td>DQa</td>
<td>6N</td>
<td>24</td>
<td>DQb</td>
<td>6F</td>
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<tr>
<td>10</td>
<td>DQa</td>
<td>7N</td>
<td>25</td>
<td>DQb</td>
<td>7E</td>
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<tr>
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<td>DQa</td>
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<td>DQb</td>
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<td>DQa</td>
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<td>7E</td>
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<td>DQa</td>
<td>7L</td>
<td>28</td>
<td>DQb</td>
<td>6D</td>
</tr>
<tr>
<td>14</td>
<td>DQa</td>
<td>6K</td>
<td>29</td>
<td>SA</td>
<td>6D</td>
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<td>31</td>
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<td>CK</td>
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<td>SA</td>
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<td>19</td>
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<td>SBb</td>
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<td>35</td>
<td>SA</td>
<td>5B</td>
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</table>

### MCM69L818C Bump/Bit Scan Order

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Signal Name</th>
<th>Bump ID</th>
<th>Bit No.</th>
<th>Signal Name</th>
<th>Bump ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>M2</td>
<td>5R</td>
<td>16</td>
<td>SBb</td>
<td>5L</td>
</tr>
<tr>
<td>2</td>
<td>SA</td>
<td>6T</td>
<td>17</td>
<td>CK</td>
<td>4L</td>
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<tr>
<td>3</td>
<td>SA</td>
<td>4P</td>
<td>18</td>
<td>CK</td>
<td>4K</td>
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<tr>
<td>4</td>
<td>SA</td>
<td>6R</td>
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<td>G</td>
<td>4F</td>
</tr>
<tr>
<td>5</td>
<td>SA</td>
<td>5T</td>
<td>20</td>
<td>DQb</td>
<td>5G</td>
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<tr>
<td>6</td>
<td>ZZ</td>
<td>7T</td>
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<td>DQb</td>
<td>7H</td>
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<tr>
<td>7</td>
<td>DQa</td>
<td>6P</td>
<td>22</td>
<td>DQb</td>
<td>6H</td>
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<tr>
<td>8</td>
<td>DQa</td>
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<td>DQb</td>
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<td>9</td>
<td>DQa</td>
<td>6N</td>
<td>24</td>
<td>DQb</td>
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<td>DQa</td>
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<td>25</td>
<td>DQb</td>
<td>7E</td>
</tr>
<tr>
<td>11</td>
<td>DQa</td>
<td>6M</td>
<td>26</td>
<td>DQb</td>
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<tr>
<td>12</td>
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<td>6L</td>
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<td>DQb</td>
<td>7E</td>
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<tr>
<td>13</td>
<td>DQa</td>
<td>7L</td>
<td>28</td>
<td>DQb</td>
<td>6D</td>
</tr>
<tr>
<td>14</td>
<td>DQa</td>
<td>6K</td>
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<td>SA</td>
<td>6D</td>
</tr>
<tr>
<td>15</td>
<td>DQa</td>
<td>7K</td>
<td>30</td>
<td>SA</td>
<td>6A</td>
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<tr>
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<td>SBa</td>
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<td>17</td>
<td>CK</td>
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<td>SA</td>
<td>5C</td>
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<tr>
<td>18</td>
<td>CK</td>
<td>4K</td>
<td>33</td>
<td>SA</td>
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<td>SBb</td>
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<td>NC</td>
<td>6B</td>
</tr>
<tr>
<td>20</td>
<td>DQb</td>
<td>6E</td>
<td>35</td>
<td>SA</td>
<td>5B</td>
</tr>
</tbody>
</table>

### NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "place holder" bit that is forced to logic one. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. In scan mode, differential inputs CK and CK are referenced to each other and must be at opposite logic levels for reliable operation.
3. ZQ, M1, and M2 are not ordinary inputs and may not respond to standard I/O logic levels. ZQ, M1, and M2 must be driven to within 100 mV of a VDD or VSS supply rail to ensure consistent results.
4. ZZ must remain at VIL during boundary scan to ensure consistent results.
TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in IEEE Standard 1149.1–1990, the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (tCS plus tCH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore, this device is not IEEE 1149.1 compliant. Nevertheless, this RAM TAP does respond to an all 0s instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register, the RAM responds just as it does in response to the SAMPLE/PRELOAD instruction described above, except the DQ pins are forced to High–Z any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all DQ pins are forced to an inactive drive state (High–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NO OP

Do not use these instructions; they are reserved for future use.
STANDARD (PUBLIC) INSTRUCTION CODES

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST</td>
<td>000</td>
<td>Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all DQ pins to High–Z state. <strong>NOT IEEE 1149.1 COMPLIANT.</strong></td>
</tr>
<tr>
<td>IDCODE</td>
<td>001**</td>
<td>Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.</td>
</tr>
<tr>
<td>SAMPLE/PRELOAD</td>
<td>100</td>
<td>Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 PRELOAD function. <strong>NOT IEEE 1149.1 COMPLIANT.</strong></td>
</tr>
<tr>
<td>BYPASS</td>
<td>111</td>
<td>Places bypass register between TDI and TDO. Does not affect RAM operation.</td>
</tr>
<tr>
<td>SAMPLE–Z</td>
<td>010</td>
<td>Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all DQ pins to High–Z state.</td>
</tr>
</tbody>
</table>

* Instruction codes expressed in binary; MSB on left, LSB on right.
** Default instruction automatically loaded at power up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO OP</td>
<td>011</td>
<td>Do not use these instructions; they are reserved for future use.</td>
</tr>
<tr>
<td>NO OP</td>
<td>101</td>
<td>Do not use these instructions; they are reserved for future use.</td>
</tr>
<tr>
<td>NO OP</td>
<td>110</td>
<td>Do not use these instructions; they are reserved for future use.</td>
</tr>
</tbody>
</table>

* Instruction codes expressed in binary, MSB on left, LSB on right.

NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram
ORDERING INFORMATION
(Order by Full Part Number)

Motorola Memory Prefix MCM
Part Number

Full Part Numbers — MCM69L736CZP5.5 MCM69L736CZP6.5 MCM69L736CZP7.5 MCM69L736CZP8.5
MCM69L818CZP5.5 MCM69L818CZP6.5 MCM69L818CZP7.5 MCM69L818CZP8.5
MCM69L736CZP5.5R MCM69L736CZP6.5R MCM69L736CZP7.5R MCM69L736CZP8.5R
MCM69L818CZP5.5R MCM69L818CZP6.5R MCM69L818CZP7.5R MCM69L818CZP8.5R

PACKAGE DIMENSIONS
ZP PACKAGE
7 X 17 BUMP PBGA
CASE 999–02

NOTES:
2. ALL DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MILLIMETERS</th>
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<th>MAX</th>
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<tr>
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<tr>
<td>A3</td>
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<tr>
<td>D2</td>
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</tbody>
</table>

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How to reach us:
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Mfax™: RFMFAX@email.sps.mot.com – TOUCHTONE 1-602-244-5609
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JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center,
3–20–1, Minami–Azabu, Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569
ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2 Dai King Street, Tai Po Industrial Estate, Tao Po, N.T., Hong Kong.
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