Advance Information
MMC2080/2075 Integrated Processor with Roaming FLEX™ Decoder

Part 1 Introduction

The MMC2080/2075 is designed to provide the messaging and paging marketplace with a powerful and flexible solution to carry communications design into the next millennium. The MMC2080 integrates two of Motorola’s most successful product families, M•CORE™ and the Roaming FLEX™ alphanumeric decoders, a combination that will set a new standard in the communications industry. Except for the FLEX decoder, the MMC2075 offers all features of the MMC2080.

Both the MMC2080/2075 are members of the low-power, high-performance M•CORE family of 32-bit microcontroller units (MCUs). The M•CORE is a streamlined execution engine that provides many of the performance enhancements found in mainstream reduced instruction set computers (RISCs). Combining performance, speed, and cost efficiency in a compact, low-power design, the M•CORE microRISC architecture is a natural solution for applications where battery life and systems cost are critical design goals.

Given that a total system’s components and processor core determine its power consumption, the instruction set architecture (ISA) for the M•CORE is designed to optimize the trade-off between performance and total power consumption. The result is system-wide reduction of total energy consumption with maintenance of acceptable performance levels. Memory power consumption (both on-chip and external) is a major factor in system energy consumption. By adopting 16-bit instruction encoding, and thus significantly decreasing the memory bandwidth needed for a high rate of instruction execution, the MMC2080/2075 minimizes the overhead of memory system energy consumption.

The MMC2080/2075 also reduces power consumption by coupling a fully static design with dynamic power management and low-voltage operation. Versatile power management is achieved through automatic power downs of any internal functional blocks not needed on a clock-by-clock basis. Power conservation modes are also provided for absolute power conservation.

A table of contents for this document appears on the following page. Figure 1 on page 3 and Figure 2 on page 4 provide simplified block diagrams of the MMC2080/2075.
Figure 1. MMC2080/2075 144 Block Diagram (144-Pin Package)
Figure 2. MMC2080/2075 DVL Block Diagram (208-Pin Package)
1.1 Conventions and Terminology

This document uses the following conventions:

- **OVERBAR** is used to indicate a signal that is active when pulled low: for example, RESET.
- **Logic level one** is a voltage that corresponds to Boolean true (1) state.
- **Logic level zero** is a voltage that corresponds to Boolean false (0) state.
- **To set** a bit or bits means to establish logic level one.
- **To clear** a bit or bits means to establish logic level zero.
- A **signal** is an electronic construct whose state or changes in state convey information.
- A **pin** is an external physical connection. The same pin can be used to connect a number of signals.
- **Asserted** means that a discrete signal is in active logic state.
  - **Active low** signals change from logic level one to logic level zero.
  - **Active high** signals change from logic level zero to logic level one.
- **Deasserted** means that an asserted discrete signal changes logic state.
  - **Active low** signals change from logic level zero to logic level one.
  - **Active high** signals change from logic level one to logic level zero.
- **LSB** means least significant bit or bits. **MSB** means most significant bit or bits. References to low and high bytes or words are spelled out.

Please refer to the examples in Table 1.

### Table 1. Data Conventions

<table>
<thead>
<tr>
<th>Signal/Symbol</th>
<th>Logic State</th>
<th>Signal State</th>
<th>Voltage</th>
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<tbody>
<tr>
<td>PIN</td>
<td>True</td>
<td>Asserted</td>
<td>$V_{IL}/V_{OL}$</td>
</tr>
<tr>
<td>PIN</td>
<td>False</td>
<td>Deasserted</td>
<td>$V_{IH}/V_{OH}$</td>
</tr>
<tr>
<td>PIN</td>
<td>True</td>
<td>Asserted</td>
<td>$V_{IH}/V_{OH}$</td>
</tr>
<tr>
<td>PIN</td>
<td>False</td>
<td>Deasserted</td>
<td>$V_{IL}/V_{OL}$</td>
</tr>
</tbody>
</table>
1.2 Features

The MMC2080/2075 offers the following suite of features.

- **M•CORE™ RISC Processor**
  - 32-bit load/store M•CORE RISC architecture
  - Fixed 16-bit instruction length
  - 16-entry 32-bit general-purpose register file
  - 32-bit internal address and data buses
  - Efficient, four-stage, fully interlocked execution pipeline
  - Single-cycle execution for most instructions; two cycles for branches and memory accesses
  - Special branch, byte, and bit manipulation instructions
  - Support for byte, halfword, and word memory accesses
  - Fast interrupt support via vectoring/auto-vectoring and a 16-entry dedicated alternate register file

- **Integrated Roaming FLEX alphanumeric decoder (MMC2080 only)**
  - FLEX paging protocol signal processor
  - 1600, 3200, and 6400 bits per second (bps) decoding
  - Highly programmable receiver control
  - FLEX message fragmentation and group messaging support
  - SSID and NID roaming support
  - Internal demodulator and data slicer
  - Improved battery savings via partial address correlation and intermittent receiver clock
  - Full support for revision G1.9 of the FLEX protocol
  - External CAP code access through parallel or serial FLASH/PROM

- **On-chip memory**
  - 24 K x 32 CPU ROM (96 K)
  - 1.5 K x 32 CPU RAM (6 K)

- **On-chip peripherals**
  - Asynchronous serial communications interface (SCI) with IrDA capability
  - Synchronous serial peripheral interface (SPI)
  - Frequency synthesizer controller (FSC)
  - Melody generator
  - 4 x 4 keypad interface
  - Multipurpose I/O ports (MPIO)
  - Two 16-bit general purpose timers
  - Time-of-day (TOD) timer
  - Watchdog timer
  - Vectored interrupt controller with 16 programmable priority levels
— Oscillator and PLL with software selectable speeds
— AMBA peripheral bridge depipelines system bus for simpler peripheral bus
— 8/16-bit external system bus with 22-bit address bus

• Operating features
  — Processor operation to 10 MHz over full operating range
  — Low-power modes
  — OnCE™ (On-Chip Emulation) debug module
  — Voltage range 1.8 V to 3.6 V; temperature range -20 °C to 85 °C
  — Chip-select outputs for four external devices (4 Mbyte per chip select, 16 Mbyte directly addressable)
  — Programmable wait states for external accesses
  — External boot option
  — External bus interface that accepts internal, half-word, and byte transfers
  — External device that may become system bus master

• Development tools
  — Development option (different package) that adds select to bypass internal ROM
  — Development option (different package) that extends external bus to 32 bits
  — External bus that can display internal transfers
1.3 Integrated Roaming FLEX Protocol and the MMC2080

The MMC2080 integrates several field-proven technologies, providing a versatile Roaming FLEX solution. The MMC2080 operates the integrated FLEX decoder in an efficient power-consumption mode, allowing the CPU to operate in a low-power mode when monitoring for message information. The Roaming FLEX protocol is a multichannel, high-performance protocol that leading service providers worldwide have adopted as a de facto standard for roaming paging. Roaming FLEX protocol gives service providers increased capacity, added reliability, enhanced pager battery performance, and the ability to control a PLL-synthesized receiver and to receive paging messages from a list of paging channels. Finally, the MMC2080 gives the service provider an upward migration path that is completely transparent to the end user.

1.4 Target Applications

The MMC2080/2075 is intended for use in wireless and paging applications. The MMC2080 is designed for applications needing an M•CORE CPU coupled with a roaming FLEX Decoder. The MMC2075 is intended for applications requiring the processing power and flexibility of the M•CORE CPU.

1.5 Product Documentation

The three documents listed in Table 2 are required for a complete description of the MMC2080/2075 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola Semiconductor Products Sector sales office, a Motorola Literature Distribution Center, or the World Wide Web. See the last page of this document for contact information.

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Description of Contents</th>
<th>Order Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>M•CORE Reference Manual</td>
<td>Detailed description of the M•CORE MCU and instruction set</td>
<td>MCorERm/AD</td>
</tr>
<tr>
<td>MMC2080/2075 User’s Manual</td>
<td>Detailed description of the MMC2080/2075 memory, peripherals, and interfaces</td>
<td>Mmc2080/2075UM/D</td>
</tr>
<tr>
<td>MMC2080/2075 Technical Data</td>
<td>MMC2080/2075 pin and package descriptions; electrical and timing specifications</td>
<td>Mmc2080/2075/D</td>
</tr>
</tbody>
</table>

1.6 Ordering Information

Table 3 lists the information you need to supply when placing an order. Consult a Motorola Semiconductor Products Sector sales office or authorized distributor to determine availability and to order parts.

<table>
<thead>
<tr>
<th>Part</th>
<th>Supply Voltage</th>
<th>Package Type</th>
<th>Pin Count</th>
<th>Order Number</th>
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<tbody>
<tr>
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<td>3 V</td>
<td>12 mm x 12 mm MAP BGA</td>
<td>144</td>
<td>MMC2080VF001</td>
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<tr>
<td>MMC2075</td>
<td>3 V</td>
<td>12 mm x 12 mm MAP BGA</td>
<td>144</td>
<td>MMC2075VF001</td>
</tr>
<tr>
<td>MMC2080</td>
<td>3 V</td>
<td>43 mm x 43 mm Ceramic PGA</td>
<td>208</td>
<td>Contact Factory Development Use Only</td>
</tr>
<tr>
<td>MMC2075</td>
<td>3 V</td>
<td>43 mm x 43 mm Ceramic PGA</td>
<td>208</td>
<td>Contact Factory Development Use Only</td>
</tr>
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</table>
Part 2 Signal and Connection Descriptions

The pins and signals of the MMC2080/2075 are described in the following sections. Figure 3 on page 10 and Figure 4 on page 11 are top and bottom views, respectively, of the 12 mm x 12 mm MAP Ball Grid Array (BGA) package, and Figure 5 on page 12 and Figure 6 on page 13 are top and bottom views, respectively, of the 43 mm x 43 mm ceramic Pin Grid Array (PGA) package, showing the pin-outs. Table 4 on page 14 and Table 5 on page 17 list the pins by number and signal name.

Figure 7 on page 21 is a representational pin-out of the chip, grouping the signals by their function. Table 6 on page 20 identifies the number of signals for each group and refers to Table 8 on page 23 through Table 20 on page 27, which are organized according to signal type and give a brief description of each signal pin.

2.1 MMC2080/2075 Pin Descriptions

The following section provides information about the available packages for this product, including diagrams of the package pin-outs and tables describing how the signals of the MMC2080/2075 are allocated. There are two packages for each part:

- The 144-pin I/O, STD small ball (SMBALL) mold array process (MAP) ball grid array (BGA), 12 mm x 12 mm package. Table 4 on page 14 identifies the signal associated with each pin.
- The 208-pin I/O, PGA, 43 mm x 43 mm ceramic package. Table 5 on page 17 identifies the signal associated with each pin.
Figure 3. MMC2080/2075 BGA (144-Pin) Top View
Figure 4. MMC2080/2075 BGA (144-Pin) Bottom View

* Signal available only in 2080
Figure 5. MMC2080/2075 PGA (208-Pin) Top View
Figure 6. MMC2080/2075 PGA (208-Pin) Bottom View

* Signal available only in 2080
### Table 4. MMC2080/2075 BGA (144-Pin) Signal ID by Pin Number (Sheet 1 of 3)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal Name</th>
<th>Pin Number</th>
<th>Signal Name</th>
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<tbody>
<tr>
<td>A1</td>
<td>Vss I/O</td>
<td>G10</td>
<td>A20</td>
</tr>
<tr>
<td>A2</td>
<td>MPB5/ROW1</td>
<td>G11</td>
<td>A19</td>
</tr>
<tr>
<td>A3</td>
<td>BW8</td>
<td>G12</td>
<td>A18</td>
</tr>
<tr>
<td>A4</td>
<td>MPB2/COL2</td>
<td>G13</td>
<td>Vss Core</td>
</tr>
<tr>
<td>A5</td>
<td>MPB0/COL0</td>
<td>H1</td>
<td>Vss I/O</td>
</tr>
<tr>
<td>A6</td>
<td>Vdd I/O</td>
<td>H2</td>
<td>D8</td>
</tr>
<tr>
<td>A7</td>
<td>SELT</td>
<td>H3</td>
<td>D9</td>
</tr>
<tr>
<td>A8</td>
<td>Vss I/O</td>
<td>H4</td>
<td>Vdd I/O</td>
</tr>
<tr>
<td>A9</td>
<td>Vss Core</td>
<td>H10</td>
<td>A16</td>
</tr>
<tr>
<td>A10</td>
<td>S2 (2080 Only)</td>
<td>H11</td>
<td>A17</td>
</tr>
<tr>
<td>A11</td>
<td>LOBAT (2080 Only)</td>
<td>H12</td>
<td>Vdd I/O</td>
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<tr>
<td>A12</td>
<td>CLKOUT (2080 Only)</td>
<td>H13</td>
<td>BREQ</td>
</tr>
<tr>
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<td>Vdd I/O</td>
<td>J1</td>
<td>Vss Core</td>
</tr>
<tr>
<td>B1</td>
<td>MPB7/ROW3</td>
<td>J2</td>
<td>D5</td>
</tr>
<tr>
<td>B2</td>
<td>MPB6/ROW2</td>
<td>J3</td>
<td>D10</td>
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<tr>
<td>B3</td>
<td>BW8</td>
<td>J4</td>
<td>BGNT</td>
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<td>B4</td>
<td>ABORT</td>
<td>J10</td>
<td>MPE1/ŚŚ</td>
</tr>
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<td>B5</td>
<td>EB0</td>
<td>J11</td>
<td>MPE2/MISO</td>
</tr>
<tr>
<td>B6</td>
<td>Vdd Core</td>
<td>J12</td>
<td>Vss I/O</td>
</tr>
<tr>
<td>B7</td>
<td>SEL0</td>
<td>J13</td>
<td>A15</td>
</tr>
<tr>
<td>B8</td>
<td>S7 (2080 Only)</td>
<td>K1</td>
<td>D11</td>
</tr>
<tr>
<td>B9</td>
<td>S4 (2080 Only)</td>
<td>K2</td>
<td>D12</td>
</tr>
<tr>
<td>B10</td>
<td>S1 (2080 Only)</td>
<td>K3</td>
<td>Vdd Core</td>
</tr>
<tr>
<td>B11</td>
<td>Vss I/O</td>
<td>K4</td>
<td>TDI</td>
</tr>
<tr>
<td>B12</td>
<td>MLDY</td>
<td>K5</td>
<td>A1</td>
</tr>
<tr>
<td>B13</td>
<td>EXTS1 (2080 Only)</td>
<td>K6</td>
<td>MPC0/TOC0</td>
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<tr>
<td>C1</td>
<td>IRQ</td>
<td>K7</td>
<td>MPC5/UCTS</td>
</tr>
<tr>
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<td>MPA0</td>
<td>K8</td>
<td>Vdd Core</td>
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### Table 4. MMC2080/2075 BGA (144-Pin) Signal ID by Pin Number (Sheet 2 of 3)

<table>
<thead>
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<th>Pin Number</th>
<th>Signal Name</th>
<th>Pin Number</th>
<th>Signal Name</th>
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<tbody>
<tr>
<td>C3</td>
<td>MPB4/ROW0</td>
<td>K9</td>
<td>A8</td>
</tr>
<tr>
<td>C4</td>
<td>MPB3/COL3</td>
<td>K10</td>
<td>A12</td>
</tr>
<tr>
<td>C5</td>
<td>MPB1/COL1</td>
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<td>MPE0/SCLK</td>
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<tr>
<td>C6</td>
<td>TA</td>
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<td>A13</td>
</tr>
<tr>
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<td>SEL2</td>
<td>K13</td>
<td>A14</td>
</tr>
<tr>
<td>C8</td>
<td>S6 (2080 Only)</td>
<td>L1</td>
<td>D6</td>
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<tr>
<td>C9</td>
<td>S3 (2080 Only)</td>
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<tr>
<td>C10</td>
<td>SYMCLK (2080 Only)</td>
<td>L3</td>
<td>D13</td>
</tr>
<tr>
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<td>EXTS0 (2080 Only)</td>
<td>L4</td>
<td>TDO</td>
</tr>
<tr>
<td>C12</td>
<td>Vdd I/O</td>
<td>L5</td>
<td>Vss Core</td>
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<td>Vss I/O</td>
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<td>MPC3/TIC1</td>
</tr>
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<td>Vdd Core</td>
<td>L7</td>
<td>A5</td>
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<td>D0</td>
<td>L8</td>
<td>MPC6/UTXD</td>
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<td>MPA1</td>
<td>L9</td>
<td>Vdd I/O</td>
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<td>Vss CORE</td>
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<td>A10</td>
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<tr>
<td>D5</td>
<td>OE</td>
<td>L11</td>
<td>Vss I/O</td>
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<td>WE</td>
<td>L12</td>
<td>Vdd I/O</td>
</tr>
<tr>
<td>D7</td>
<td>SEL3</td>
<td>L13</td>
<td>A11</td>
</tr>
<tr>
<td>D8</td>
<td>S5 (2080 Only)</td>
<td>M1</td>
<td>D14</td>
</tr>
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<td>D9</td>
<td>XBOOT</td>
<td>M2</td>
<td>D15</td>
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<tr>
<td>D10</td>
<td>S0/IFIN (2080 only)</td>
<td>M3</td>
<td>Vss I/O</td>
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<tr>
<td>D11</td>
<td>MPE4/LOCK</td>
<td>M4</td>
<td>TRST</td>
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<td>Vdd Core</td>
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<td>A2</td>
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<td>MPE3/MOSI</td>
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<td>MPC2/TOC1</td>
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<td>Vss I/O</td>
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<td>MPC7/URXD</td>
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<td>E3</td>
<td>D2</td>
<td>M9</td>
<td>A7</td>
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<tr>
<td>E4</td>
<td>D1</td>
<td>M10</td>
<td>TEST</td>
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### MMC2080/2075 Pin Descriptions

**Table 4. MMC2080/2075 BGA (144-Pin) Signal ID by Pin Number (Sheet 3 of 3)**

<table>
<thead>
<tr>
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<th>Signal Name</th>
<th>Pin Number</th>
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<tbody>
<tr>
<td>E10</td>
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<td>RSTOUT</td>
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<td>E11</td>
<td>EXTAL</td>
<td>M12</td>
<td>Vdd I/O</td>
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<td>XTAL</td>
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<td>UCLK</td>
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<td>E13</td>
<td>Vss OSC</td>
<td>N1</td>
<td>Vdd I/O</td>
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<td>F1</td>
<td>Vdd I/O</td>
<td>N2</td>
<td>TCK</td>
</tr>
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<td>MPA3</td>
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<td>MPA2</td>
<td>N4</td>
<td>A0</td>
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<tr>
<td>F4</td>
<td>Vdd I/O</td>
<td>N5</td>
<td>MPC1/TIC0</td>
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<td>F10</td>
<td>Vdd PLL</td>
<td>N6</td>
<td>Vss I/O</td>
</tr>
<tr>
<td>F11</td>
<td>CXFC</td>
<td>N7</td>
<td>A4</td>
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<td>F12</td>
<td>Vss PLL</td>
<td>N8</td>
<td>MPC4/URTS</td>
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<td>A21</td>
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<td>A6</td>
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<td>MPA5</td>
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<td>D4</td>
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Table 5. MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 1 of 4)

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<th>Signal Name</th>
<th>Pin Number</th>
<th>Signal Name</th>
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<tr>
<td>A1</td>
<td>MPB6/ROW2</td>
<td>J4</td>
<td>D3</td>
</tr>
<tr>
<td>A2</td>
<td>MPB4/ROW0</td>
<td>J14</td>
<td>A21</td>
</tr>
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<td>A3</td>
<td>BW8</td>
<td>J15</td>
<td>A20</td>
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<tr>
<td>A4</td>
<td>MPB2/COL2</td>
<td>J16</td>
<td>Vss Core</td>
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<td>A5</td>
<td>MPB0/COL0</td>
<td>J17</td>
<td>Vss PLL</td>
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<td>A6</td>
<td>TA</td>
<td>K1</td>
<td>D8</td>
</tr>
<tr>
<td>A7</td>
<td>DVLEBT</td>
<td>K2</td>
<td>Vss I/O</td>
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<td>A8</td>
<td>SEL3</td>
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<td>D9</td>
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<td>SEL1</td>
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<td>D21</td>
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<td>A10</td>
<td>Vss I/O</td>
<td>K14</td>
<td>A17</td>
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<td>DVLEB0</td>
<td>K15</td>
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<td>Vss Core</td>
<td>K16</td>
<td>BREQ</td>
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<td>S2 (2080 Only)</td>
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<td>S0/IFIN’(2080 only)</td>
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<td>Vdd I/O</td>
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<td>DVLMX</td>
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<td>MPB5/ROW1</td>
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<td>BGNT</td>
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<td>PULL_EN</td>
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<td>MPE2/MIS0</td>
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<td>MPB1/COL1</td>
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<td>A18</td>
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<td>WE</td>
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<td>A19</td>
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<td>D23</td>
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<td>M14</td>
<td>A11</td>
</tr>
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<td>B13</td>
<td>DVL1</td>
<td>M15</td>
<td>MPE0/SCLK</td>
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<td>B14</td>
<td>LOBAT (2080 Only)</td>
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### MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 2 of 4)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal Name</th>
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<th>Signal Name</th>
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<tbody>
<tr>
<td>B17</td>
<td>EXTS0 (2080 Only)</td>
<td>M17</td>
<td>Vdd I/O</td>
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<tr>
<td>C1</td>
<td>IRQ</td>
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<td>D5</td>
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<td>C5</td>
<td>D16</td>
<td>N2</td>
<td>D24</td>
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<td>C6</td>
<td>ABORT</td>
<td>N3</td>
<td>D6</td>
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<tr>
<td>C7</td>
<td>EB0</td>
<td>N14</td>
<td>UCLK</td>
</tr>
<tr>
<td>C8</td>
<td>Vdd I/O</td>
<td>N15</td>
<td>Vdd I/O</td>
</tr>
<tr>
<td>C9</td>
<td>TEA</td>
<td>N16</td>
<td>MPE1/SS</td>
</tr>
<tr>
<td>C10</td>
<td>XBOOT</td>
<td>N17</td>
<td>Vss I/O</td>
</tr>
<tr>
<td>C11</td>
<td>S1 (2080 Only)</td>
<td>P1</td>
<td>D11</td>
</tr>
<tr>
<td>C12</td>
<td>DVLO</td>
<td>P2</td>
<td>D7</td>
</tr>
<tr>
<td>C13</td>
<td>Vss I/O</td>
<td>P3</td>
<td>TCK</td>
</tr>
<tr>
<td>C14</td>
<td>Vdd I/O</td>
<td>P4</td>
<td>TC0</td>
</tr>
<tr>
<td>C16</td>
<td>EXTS1 (2080 Only)</td>
<td>P5</td>
<td>TCK</td>
</tr>
<tr>
<td>C17</td>
<td>DSTAT4</td>
<td>P6</td>
<td>TC0</td>
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<td>D1</td>
<td>Vdd Core</td>
<td>P7</td>
<td>D26</td>
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<td>D2</td>
<td>MPA1</td>
<td>P8</td>
<td>VssCore</td>
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<td>D3</td>
<td>Vss I/O</td>
<td>P9</td>
<td>A3</td>
</tr>
<tr>
<td>D4</td>
<td>EB1</td>
<td>P10</td>
<td>MPC6/UTXD</td>
</tr>
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<td>D5</td>
<td>OE</td>
<td>P11</td>
<td>A8</td>
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<tr>
<td>D6</td>
<td>Vdd Core</td>
<td>P12</td>
<td>DE</td>
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<td>D7</td>
<td>OE</td>
<td>P15</td>
<td>Vss I/O</td>
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<td>D8</td>
<td>VddCORE</td>
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<td>A12</td>
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<td>D9</td>
<td>SEL0</td>
<td>P17</td>
<td>A13</td>
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<td>D10</td>
<td>S4 (2080 Only)</td>
<td>R1</td>
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<td>SYMCLK (2080 Only)</td>
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</tr>
<tr>
<td>D12</td>
<td>DVLSEL</td>
<td>R4</td>
<td>Vdd I/O</td>
</tr>
<tr>
<td>D13</td>
<td>CLKOUT (2080 Only)</td>
<td>R5</td>
<td>Vss I/O</td>
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<td>D16</td>
<td>DSTAT5</td>
<td>R6</td>
<td>HIGHZ</td>
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### Table 5. MMC2080/2075 PGA (208-Pin) Signal ID by Pin Number (Sheet 3 of 4)

<table>
<thead>
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<th>Pin Number</th>
<th>Signal Name</th>
<th>Pin Number</th>
<th>Signal Name</th>
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<tr>
<td>D17</td>
<td>DSTAT1</td>
<td>R7</td>
<td>D27</td>
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<tr>
<td>E1</td>
<td>BUSCLK</td>
<td>R8</td>
<td>A0</td>
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<tr>
<td>E2</td>
<td>D2</td>
<td>R9</td>
<td>MPC2/TOC1</td>
</tr>
<tr>
<td>E3</td>
<td>MPA0</td>
<td>R10</td>
<td>MPC4/URTS</td>
</tr>
<tr>
<td>E4</td>
<td>MPB7/ROW3</td>
<td>R11</td>
<td>A7</td>
</tr>
<tr>
<td>E15</td>
<td>Vdd I/O</td>
<td>R12</td>
<td>TEST</td>
</tr>
<tr>
<td>E16</td>
<td>Vss I/O</td>
<td>R13</td>
<td>RSTOUT</td>
</tr>
<tr>
<td>E17</td>
<td>MPE3/MOSI</td>
<td>T1</td>
<td>D13</td>
</tr>
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<td>F1</td>
<td>D17</td>
<td>T4</td>
<td>TMS</td>
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<td>MPA2</td>
<td>T5</td>
<td>TDO</td>
</tr>
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<td>D0</td>
<td>T6</td>
<td>A1</td>
</tr>
<tr>
<td>F4</td>
<td>Vss CORE</td>
<td>T7</td>
<td>MPC1/TIC0</td>
</tr>
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<td>DSTAT3</td>
<td>T8</td>
<td>D28</td>
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<td>F15</td>
<td>DSTAT2</td>
<td>T9</td>
<td>MPC0/TOC0</td>
</tr>
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<td>F16</td>
<td>DSTAT0</td>
<td>T10</td>
<td>A5</td>
</tr>
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<td>F17</td>
<td>Vdd OSC</td>
<td>T11</td>
<td>Vdd Core</td>
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<tr>
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<td>MPA4</td>
<td>T12</td>
<td>Vdd I/O</td>
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<td>Vdd I/O</td>
<td>T13</td>
<td>A10</td>
</tr>
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<td>Vss I/O</td>
<td>T14</td>
<td>D31</td>
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<td>G4</td>
<td>D1</td>
<td>T15</td>
<td>RESET</td>
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<td>MPE4/LOCK</td>
<td>T16</td>
<td>SHS</td>
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<td>Vdd Core</td>
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<td>D15</td>
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<td>TDI</td>
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<td>XTAL</td>
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<td>TRST</td>
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<td>MPA5</td>
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<td>A2</td>
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<td>D18</td>
<td>U7</td>
<td>MPC3/TIC1</td>
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<td>Vdd I/O</td>
<td>U8</td>
<td>Vss I/O</td>
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<td>MPA3</td>
<td>U9</td>
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2.2 Tables of Signals

The MMC2080 input and output signals are organized into functional groups in Table 6 and in Figure 7 on page 21. Table 7 on page 22 displays data relating to I/O cell names, including descriptions and the availability of Hi-Z impedance, pull-up resistors, and high drive-current capability. Table 8 on page 23 through Table 20 on page 27 are organized according to signal type and give a brief description of each signal pin. Package type is indicated as “N” for the 144-pin normal-function package. All pins are available in the 208-pin development extensions package.

Table 6. MMC2080 Signal Functional Group Organization

<table>
<thead>
<tr>
<th>Functional Group</th>
<th>Number of Signals</th>
<th>Detailed Description</th>
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</thead>
<tbody>
<tr>
<td>Arbitration signals</td>
<td>2</td>
<td>Table 20 on page 27</td>
</tr>
<tr>
<td>External system bus signals</td>
<td>52</td>
<td>Table 8 on page 23</td>
</tr>
<tr>
<td>Development extensions (208-pin package only)</td>
<td>34</td>
<td>Table 9 on page 24</td>
</tr>
<tr>
<td>FLEX signals</td>
<td>13</td>
<td>Table 10 on page 25</td>
</tr>
<tr>
<td>FSC/SPI signals</td>
<td>5</td>
<td>Table 11 on page 25</td>
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<tr>
<td>SCI signals</td>
<td>5</td>
<td>Table 12 on page 25</td>
</tr>
<tr>
<td>Timer signals</td>
<td>4</td>
<td>Table 13 on page 26</td>
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<tr>
<td>Melody generator signals</td>
<td>1</td>
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<tr>
<td>Keypad signals</td>
<td>8</td>
<td>Table 15 on page 26</td>
</tr>
<tr>
<td>Dedicated MPIO signals</td>
<td>6</td>
<td>Table 16 on page 26</td>
</tr>
<tr>
<td>SIM signals</td>
<td>2</td>
<td>Table 17 on page 26</td>
</tr>
<tr>
<td>JTAG/OnCE signals</td>
<td>6</td>
<td>Table 18 on page 27</td>
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<tr>
<td>Clock and power</td>
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<td>Table 19 on page 27</td>
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### Figure 7. MMC2080 Signal Group Organization

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<th>MMC2080</th>
<th>SCI Signals</th>
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<tr>
<td>BREQ</td>
<td>Arbitration Request</td>
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<td>BGNT</td>
<td>Arbitration Grant</td>
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<tr>
<td>MPD[7:0]/D[15:8]</td>
<td>High-Order Data Bus</td>
</tr>
<tr>
<td>MPD[7:0]</td>
<td>Low-Order Data Bus</td>
</tr>
<tr>
<td>A[21:0]</td>
<td>Address</td>
</tr>
<tr>
<td>EBE-1</td>
<td>Byte Enable</td>
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<tr>
<td>BW8</td>
<td>Bus Width (8-Bit)</td>
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<tr>
<td>WE</td>
<td>Data Direction</td>
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<td>OE</td>
<td>Output Enable</td>
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<td>TA</td>
<td>Transfer Acknowledge</td>
</tr>
<tr>
<td>ABORT</td>
<td>Data Transfer Abort</td>
</tr>
<tr>
<td>BUSCLK</td>
<td>External Bus Clock</td>
</tr>
<tr>
<td>SEL0-3</td>
<td>External Device Select</td>
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<tr>
<td>XB00T</td>
<td>External Boot</td>
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<tr>
<td>IRQ</td>
<td>Interrupt Request</td>
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<td>D[31:16]</td>
<td>Extension</td>
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<td>DVLB0-1</td>
<td>Byte Enable</td>
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<td>DVL0-1</td>
<td>Development Mode</td>
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<td>DVLSEL</td>
<td>Development Select</td>
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<td>DSTAT0-5</td>
<td>Development Status</td>
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<td>TC0-2</td>
<td>Transfer Code</td>
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<tr>
<td>TEA</td>
<td>Transfer Error Acknowledge</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>Tri-State Disable</td>
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<td>PULL_EN</td>
<td>Pull-up Enable</td>
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<td>SHS</td>
<td>Show Cycle Strobe</td>
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<td>Low Battery</td>
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<td>Extension Symbol</td>
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<td>Clock Output</td>
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<td>SYMCLK</td>
<td>Symbol Clock</td>
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<td>S1-7</td>
<td>Serial Port</td>
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<td>S0/IFIN</td>
<td>Serial Port</td>
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<td>MPE4/LOCK</td>
<td>Synthesizer Lock</td>
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<tr>
<td>MPE3/MOSI</td>
<td>Master in/Slave Out</td>
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<tr>
<td>MPE2/MISO</td>
<td>Master Out/Slave In</td>
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<tr>
<td>MPE1/SS</td>
<td>Slave Select</td>
</tr>
<tr>
<td>MPE0/SCLK</td>
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Freescale Semiconductor, Inc.
Table 7. I/O Cell Description

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<tr>
<th>I/O Cell Name</th>
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<th>Hi-Z</th>
<th>Pull-up</th>
<th>High Drive Capable</th>
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<tr>
<td>OTP</td>
<td>Tri-state output with selectable drive strength; always enabled with strong drive except during JTAG Hi-Z command or unless otherwise stated</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>INHP</td>
<td>Input with hysteresis</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>INHPP</td>
<td>INHP with selectable pull-up enable</td>
<td>N</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>IOHP</td>
<td>INHP and OTP</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>IOHPPH</td>
<td>INHPP and OTP</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>SWIOP</td>
<td>High-current IOHPPH</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>AIN/AOT</td>
<td>Analog input/output (same cell)</td>
<td>N</td>
<td>N</td>
<td>N</td>
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### Table 8. External System Bus Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPD[7:0]/D[15:8]</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>High-Order Data Bus—May be used as general I/O when the data bus is configured as an 8-bit bus. Output drivers are disabled and pull-up resistors are enabled during reset.</td>
</tr>
<tr>
<td>D[7:0]</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Low-Order Data Bus—Output drivers are disabled and pull-up resistors are enabled during reset.</td>
</tr>
<tr>
<td>A[21:0]</td>
<td>I/O</td>
<td>Y</td>
<td>IOHP</td>
<td>Address—Input when BGNT is low; otherwise output. Twenty-two bits is a 4 Mbyte address space.</td>
</tr>
<tr>
<td>EB[1:0]</td>
<td>I/O</td>
<td>Y</td>
<td>IOHP</td>
<td>Byte Enable (active low)—Input when BGNT is low; otherwise output. EB0 enables D[15:8] and EB1 enables D[7:0]. When the data bus is configured as an 8-bit bus, EB0 is always released (high) and EB1 is always asserted (low).</td>
</tr>
<tr>
<td>BW8</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Bus Width 8 (open-drain, active low)—If this pin is driven low either externally or internally, the external bus functions as an 8-bit bus.</td>
</tr>
<tr>
<td>WE</td>
<td>I/O</td>
<td>Y</td>
<td>IOHP</td>
<td>Write Enable (active low)—Input when BGNT is low. When WE is low, data is driven by an external device and received by the MMC2080. Output when BGNT is high. When WE is low, data is driven by the MMC2080 and received by an external device.</td>
</tr>
<tr>
<td>OE</td>
<td>I/O</td>
<td>Y</td>
<td>IOHP</td>
<td>Output Enable (active low)—Input when BGNT is low: when OE is high, D[7:0] (and D[15:8] when in 16-bit mode) external data drivers are disabled. Output when BGNT is high; when OE is high, drivers are disabled.</td>
</tr>
<tr>
<td>TA</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Transfer Acknowledge (active low)—An external transaction continues when this pin is high. When low, the external data transfer cycle will complete. When MONITOR mode is set. TA also indicates the end of internal transactions.</td>
</tr>
<tr>
<td>ABORT</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Data Transfer Abort (active low)—When a transaction is aborted, this pin is driven low.</td>
</tr>
<tr>
<td>BUSCLK</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>External Bus Clock.</td>
</tr>
<tr>
<td>SEL[3:0]</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>External Device Select—SEL0 is always active low; SEL[3:1] may be individually programmed as active low or active high. After reset, SEL3 is active high. SEL1 and SEL2 are active low after restart.</td>
</tr>
<tr>
<td>XBOOT</td>
<td>I</td>
<td>Y</td>
<td>INHPP</td>
<td>External Boot (active low)—If this pin is low after a reset, the external boot portion of the system memory map is enabled; otherwise the internal boot map is enabled.</td>
</tr>
<tr>
<td>IRQ</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Interrupt Request—This is driven high when either a normal interrupt or a fast interrupt is generated by the interrupt controller.</td>
</tr>
</tbody>
</table>
Table 9. Development Extensions (208-Pin Package)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D[31:16]</td>
<td>I/O</td>
<td>N</td>
<td>IOHPPH</td>
<td>Extension to provide a 32-bit external bus. The bus is enabled when either ( DVL0 ) or ( \overline{DVL0} ) is asserted.</td>
</tr>
<tr>
<td>DVLEB[1:0]</td>
<td>I/O</td>
<td>N</td>
<td>IOHPPH</td>
<td><strong>Byte Enable</strong> (active low)—Input when ( BGNT ) is low; otherwise output. DVLEB0 enables D[31:24] and DVLEB1 enables D[23:16].</td>
</tr>
<tr>
<td>DVL[1:0]</td>
<td>I</td>
<td>N</td>
<td>INHPP</td>
<td><strong>Development Mode</strong>—When DVL1 is low, the internal ROM is bypassed. If the ROM space is addressed when DVL1 is low and XBOOT is high, the 32-bit extension is enabled and DVLSEL is asserted to select an external memory. When DVL0 is low, the 32-bit bus extension is enabled for external bus masters (BGNT is low) and for debug monitor modes.</td>
</tr>
<tr>
<td>DVLSEL</td>
<td>O</td>
<td>N</td>
<td>OTP</td>
<td><strong>Development Select</strong> (active low)—When DVL1 is low and XBOOT is high, this output is asserted when the internal ROM locations are addressed.</td>
</tr>
<tr>
<td>DVLMX</td>
<td>I</td>
<td>N</td>
<td>INHPP</td>
<td>Selects the output of DSTAT[5:0].</td>
</tr>
<tr>
<td>DSTAT[5:0]</td>
<td>O</td>
<td>N</td>
<td>OTP</td>
<td>When DVLMX is high, DSTAT is the low-order 6 bits of the interrupt vector. When DVLMX is low, DSTAT[3:0] is the M-CORE pipeline status, PSTAT[3:0], and DSTAT[5:4] is the transfer size in M-CORE format.</td>
</tr>
<tr>
<td>TEA</td>
<td>I</td>
<td>N</td>
<td>INHPP</td>
<td><strong>Transfer Error Acknowledge</strong> (active low).</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>I</td>
<td>N</td>
<td>INHPP</td>
<td><strong>Tri-State Disable</strong> (active low)—When asserted (low), all tri-state outputs are disabled (high-Z). This performs the same function as the JTAG HIGHZ command.</td>
</tr>
<tr>
<td>PULL_EN</td>
<td>I</td>
<td>N</td>
<td>INHPP</td>
<td><strong>Enable Pull-up Resistors</strong>—When low, all pull-up resistors (except the pull-up resistor on this I/O cell) are disabled.</td>
</tr>
<tr>
<td>SHS</td>
<td>O</td>
<td>N</td>
<td>OTP</td>
<td><strong>Show Cycle Strobe (active low)</strong>—Strobes low when data is valid.</td>
</tr>
</tbody>
</table>
Table 10. FLEX Signals (MMC2080 Only)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOBAT</td>
<td>In</td>
<td>Y</td>
<td>INHP</td>
<td>Low Battery—LOBAT is an input signal to indicate to the MMC2080 when external battery power is going low. (An external voltage sensing circuit is required.) Polarity is programmable.</td>
</tr>
<tr>
<td>EXTS[1:0]</td>
<td>In</td>
<td>Y</td>
<td>IOHP</td>
<td>External Symbol—EXTS 1 is the MSB of the current FLEX symbol. EXTS0 is the LSB of the current FLEX symbol. These pins are used when demodulation is being performed externally.</td>
</tr>
<tr>
<td>CLKOUT*</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Clock Output—CLKOUT is programmable as a 38.4 or 40 kHz clock output (derived from oscillator).</td>
</tr>
<tr>
<td>SYMCLK</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Recovered Symbol Clock—Data is synchronized to the internal clock, and this recovered clock output enhances lock-on capability by reducing jitter from cable-induced noise.</td>
</tr>
<tr>
<td>S[7:1]</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Control Lines 1–7—These signals are the seven additional receiver control lines. Selectable polarity.</td>
</tr>
<tr>
<td>S0/IFIN</td>
<td>I/O</td>
<td>Y</td>
<td>IOHP</td>
<td>S0—This signal is a receiver control output line when the IDE bit is clear (that is, the internal demodulator is disabled). IFIN—This signal is a limited IF input when the IDE bit is set (that is, the internal demodulator is enabled).</td>
</tr>
</tbody>
</table>

Table 11. FSC/SPI1 Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPE4/LOCK</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>External Synthesizer Lock Input—PIO when SPI1 is disabled</td>
</tr>
<tr>
<td>MPE3/MOSI</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Master-out / Slave-in—PIO when SPI1 is disabled</td>
</tr>
<tr>
<td>MPE2/MISO</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Master-in / Slave-out—PIO when SPI1 is disabled</td>
</tr>
<tr>
<td>MPE1/SS</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Slave Select (selectable polarity)—PIO when SPI1 is disabled</td>
</tr>
<tr>
<td>MPE0/SCLK</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Serial Clock—PIO when SPI1 is disabled</td>
</tr>
</tbody>
</table>

Table 12. SCI Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPC7/URXD</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Receive Data—An input when used as URXD; otherwise a PIO</td>
</tr>
<tr>
<td>MPC6/UTXD</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Transmit Data—An output when used as UTXD; otherwise a PIO</td>
</tr>
<tr>
<td>MPC5/UCTS</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Clear-to-Send (active low)—An input when used as UCTS; otherwise a PIO</td>
</tr>
<tr>
<td>MPC4/URTS</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Request-to-Send (active low)—An output when used as URTS; otherwise a PIO</td>
</tr>
<tr>
<td>UCLK</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>UART Clock</td>
</tr>
</tbody>
</table>
### Table 13. Timer Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPC3/TIC1</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Timer1 Input Capture—An input when used as TIC1; otherwise a PIO</td>
</tr>
<tr>
<td>MPC2/TOC1</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Timer1 Output Capture—An output when used as TOC1; otherwise a PIO</td>
</tr>
<tr>
<td>MPC1/TIC0</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Timer0 Input Capture—An input when used as TIC0; otherwise a PIO</td>
</tr>
<tr>
<td>MPC0/TOC0</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Timer0 Output Capture—An output when used as TOC0; otherwise a PIO</td>
</tr>
</tbody>
</table>

### Table 14. Melody Generator Signal

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MLDY</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Melody Generator Waveform</td>
</tr>
</tbody>
</table>

### Table 15. Keypad Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPB[7:4]/ROW[3:0]</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Row Detect—Inputs when used as row detect; otherwise a PIO</td>
</tr>
<tr>
<td>MPB[3:0]/COL[3:0]</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Column Select—Open-drain outputs when used as column select; otherwise a PIO</td>
</tr>
</tbody>
</table>

### Table 16. MPIO Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPA[5:0]</td>
<td>I/O</td>
<td>Y</td>
<td>SWIOP</td>
<td>These bits can be individually programmed as input (with selectable pull-up resistor), output (with selectable drive strength), or external interrupt (with selectable assertion level). Each GPIO input pin is latched at the beginning of a read cycle.</td>
</tr>
<tr>
<td>Other pins when configured as PIO</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>These bits can be individually programmed as input (with selectable pull-up resistor) or output (with selectable drive strength). Each MPIO input pin is latched at the beginning of a read cycle.</td>
</tr>
</tbody>
</table>

### Table 17. SIM Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>I</td>
<td>Y</td>
<td>INHP</td>
<td>External Reset (active low)</td>
</tr>
<tr>
<td>RSTOUT</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Reset Output (active low)</td>
</tr>
</tbody>
</table>
### Table 18. JTAG/OnCE™ Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMS</td>
<td>I</td>
<td>Y</td>
<td>INHPP</td>
<td>Test Mode Select—Pull-up resistor always enabled</td>
</tr>
<tr>
<td>TCK</td>
<td>I</td>
<td>Y</td>
<td>INHPP</td>
<td>Test Clock—Pull-up resistor always enabled</td>
</tr>
<tr>
<td>TDI</td>
<td>I</td>
<td>Y</td>
<td>INHPP</td>
<td>Test Data In—Pull-up resistor always enabled</td>
</tr>
<tr>
<td>TDO</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Test Data Out</td>
</tr>
<tr>
<td>TRST</td>
<td>I</td>
<td>Y</td>
<td>INHP</td>
<td>TAP Reset (active low)</td>
</tr>
<tr>
<td>DE</td>
<td>I/O</td>
<td>Y</td>
<td>IOHPPH</td>
<td>Debug Enable (open drain, active low)</td>
</tr>
</tbody>
</table>

### Table 19. Clock and Power

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTAL</td>
<td>Y</td>
<td>AIN</td>
<td>Oscillator circuit input—external 76.8 kHz crystal</td>
</tr>
<tr>
<td>XTAL</td>
<td>Y</td>
<td>AOT</td>
<td>Oscillator circuit output</td>
</tr>
<tr>
<td>CXFC</td>
<td>Y</td>
<td>AIN</td>
<td>PLL filter capacitor</td>
</tr>
<tr>
<td>$V_{dd}$Core(5)</td>
<td>Y</td>
<td>Power</td>
<td>Core power</td>
</tr>
<tr>
<td>$V_{ss}$Core(5)</td>
<td>Y</td>
<td>Power</td>
<td>Core ground</td>
</tr>
<tr>
<td>$V_{dd}$I/O (11)</td>
<td>Y</td>
<td>Power</td>
<td>I/O pad power</td>
</tr>
<tr>
<td>$V_{ss}$I/O (11)</td>
<td>Y</td>
<td>Power</td>
<td>I/O pad ground</td>
</tr>
<tr>
<td>$V_{dd}$OSC</td>
<td>Y</td>
<td>Power</td>
<td>Oscillator power</td>
</tr>
<tr>
<td>$V_{ss}$OSC</td>
<td>Y</td>
<td>Power</td>
<td>Oscillator ground</td>
</tr>
<tr>
<td>$V_{dd}$PLL</td>
<td>Y</td>
<td>Power</td>
<td>PLL power</td>
</tr>
<tr>
<td>$V_{ss}$PLL</td>
<td>Y</td>
<td>Power</td>
<td>PLL ground</td>
</tr>
</tbody>
</table>

### Table 20. Arbitration Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>N</th>
<th>I/O Cell</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BREQ</td>
<td>I</td>
<td>Y</td>
<td>INHPP</td>
<td>Arbitration Request (active low)—Request mastership of the internal system bus; pull-up resistor always enabled</td>
</tr>
<tr>
<td>BGNT</td>
<td>O</td>
<td>Y</td>
<td>OTP</td>
<td>Arbitration Grant (active low)—Indicates system bus is granted to external master</td>
</tr>
</tbody>
</table>
Part 3 Specifications

3.1 General Characteristics
The MMC2080/2075 specifications are preliminary, from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published upon the completion of full characterization and device qualifications.

3.2 Maximum Ratings

WARNING:
This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either Vss or Vdd).

NOTE:
In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst-case variation of process parameter values in one direction. The minimum specification is calculated using the worst-case variation for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 21. DC Absolute Maximum Operating Conditions

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (All)</td>
<td>Vdd</td>
<td>1.8</td>
<td>3.0</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>V_I</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Clamp Current</td>
<td>I_i</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(V&lt;0 or V&gt;QVDDH)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Clamp Current</td>
<td>I_O</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(V&lt;0 or V&gt;QVDDH)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

Remaining specification information to be provided.
Part 4 Pin-out and Package Information

This section provides information about the available packages for this product. The MMC2080/2075 is available in a 144-pin Ball Grid Array (BGA) package. A 208-pin Pin Grid Array (PGA) is produced for engineering use only. Contact the factory for availability.

4.1 BGA Details

The MMC2080/2075 is offered in the JEDEC-standard, Mold Array Process (MAP), 12 mm x 12 mm BGA with 0.8 mm ball pitch (0.4 mm small solder balls). Refer to Figure 8 for the package drawings and dimensions.

4.1.1 BGA Package Mechanical Drawings

The mechanical drawings for the 144-pin Ball Grid Array package are shown in Figure 8.

![Figure 8. MMC2080/2075 BGA Mechanical Drawings](image-url)
4.2 PGA Details

The MMC2080/2075 is also offered in a ceramic, 43 mm x 43 mm PGA for engineering use only. Contact the factory for availability. Refer to Figure 9 for the package drawings and dimensions.

4.2.1 PGA Package Mechanical Drawings

The mechanical drawings for the 208-pin Ball Grid PGA package are shown in Figure 9.

![Figure 9. MMC2080/2075 PGA Mechanical Drawings](image-url)
4.3 Ordering Drawings

Complete mechanical information regarding MMC2080/2075 packaging is available by facsimile through Motorola's MFAX™ system. Call the following number to obtain information by facsimile:

(602) 244-6591

The MFAX automated system requests the following information:

- The receiving facsimile telephone number, including area code or country code
- The caller’s personal identification number (PIN)

**NOTE:**
For first-time callers, the system provides instructions for setting up a PIN, which requires the entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific-part technical information or datasheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The MMC2080/2075 144-pin BGA package mechanical drawing is referenced as Case 1248A-01 Rev. 0.

The MMC2080/2075 208-pin BGA package mechanical drawing is referenced as Case 1297-01 Rev. 0.
Part 5  Design Considerations

5.1  Heat Dissipation

An estimate of the MMC2080/2075 chip junction temperature, $T_J$, in °C can be obtained from the following equation.

$$ T_J = T_A + (P_D \times R_{θJA}) $$

Where:

- $T_A$ = ambient temperature °C
- $R_{θJA}$ = package junction-to-ambient thermal resistance °C/W
- $P_D$ = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance, as follows:

$$ R_{θJA} = R_{θJC} + R_{θCA} $$

Where:

- $R_{θJA}$ = package junction-to-ambient thermal resistance °C/W
- $R_{θJC}$ = package junction-to-case thermal resistance °C/W
- $R_{θCA}$ = package case-to-ambient thermal resistance °C/W

$R_{θJC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{θCA}$. For example, the user can change the air flow around the device, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; ninety percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device’s thermal performance may need the additional modeling capability of a system-level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{θJA}$ do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case ($T_τ$) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_τ)/P_D$.

As noted previously, the junction-to-case thermal resistances quoted in this document are determined using the first definition. From a practical standpoint, this value is also suitable for determining the junction
temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than the actual temperature. Hence, the new thermal metric, thermal characterization parameter or \( \Psi_{JT} \), has been defined to be \( (T_J - T_T)/P_D \). This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

**NOTE:**
Section 3, “Specifications,” on page 28 of this document contains the package thermal values for this chip.

### 5.2 Electrical Design Considerations

**WARNING:**
This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either Vss or Vdd).

Use the following list of recommendations to assure correct operation:

- Provide a low-impedance path from the board power supply to each Vdd pin on the MMC2080/2075 and from the board ground to each Vss pin.
- Use at least four 0.1 \( \mu \)F bypass capacitors positioned as close as possible to the four sides of the package to connect the Vdd power source to Vss.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip Vdd and Vss pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer printed circuit board (PCB) with two inner layers for Vdd and Vss.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the Vdd and Vss circuits.
- All inputs must be terminated (that is, not allowed to float) using CMOS levels.

Take special care to minimize noise levels on the PLL supply pins (both Vdd and Vss).
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