



Figure Number	LIST OF FIGURES	Page Number
1-1	MC68F375 Block Diagram .....	1-7
1-2	MC68F375 Address Map .....	1-10
2-1	MC68F375 Pad Map .....	2-8
2-2	MC68F375 Ball Map .....	2-9
3-1	CPU32 Block Diagram .....	3-2
3-2	User Programming Model .....	3-3
3-3	Supervisor Programming Model Supplement .....	3-4
3-4	Data Organization in Data Registers .....	3-5
3-5	Address Organization in Address Registers .....	3-6
3-6	Memory Operand Addressing .....	3-8
3-7	Loop Mode Instruction Sequence .....	3-16
3-8	Common In-Circuit Emulator Diagram .....	3-20
3-9	Bus State Analyzer Configuration .....	3-20
3-10	Debug Serial I/O Block Diagram .....	3-25
3-11	BDM Serial Data Word .....	3-26
3-12	BDM Connector Pinout .....	3-26
4-1	SCIM2E Block Diagram .....	4-2
4-2	Slow Reference Mode .....	4-9
4-3	Fast Reference Mode .....	4-12
4-4	External Clock Mode .....	4-14
4-5	Crystal Oscillator and External Capacitor Configuration .....	4-17
4-6	LPSTOP Flowchart .....	4-22
4-7	System Protection .....	4-24
4-8	Periodic Interrupt Timer and Software Watchdog Timer .....	4-28
4-9	MCU Basic System .....	4-33
4-10	Operand Byte Order .....	4-37
4-11	Word Read Cycle Flowchart .....	4-40
4-12	Write Cycle Flowchart .....	4-41
4-13	CPU Space Address Encoding .....	4-43
4-14	Breakpoint Operation Flowchart .....	4-45
4-15	LPSTOP Interrupt Mask Encoding on DATA[15:0] .....	4-46
4-16	Bus Arbitration Flowchart for Single Request .....	4-51
4-17	SCIM2 Reset Control Flow .....	4-54
4-18	Power-On Reset .....	4-58
4-19	Preferred Circuit for Data Bus Mode Select Conditioning .....	4-63
4-20	Alternate Circuit for Data Bus Mode Select Conditioning .....	4-64
4-21	Basic MCU System .....	4-74
4-22	Chip-Select Circuit Block Diagram .....	4-75
4-23	CPU Space Encoding for Interrupt Acknowledge .....	4-85
4-24	Port F Block Diagram .....	4-91

## Figure Number

## Page Number



5-1	QADC64 Block Diagram .....	5-1
5-2	QADC64 Input and Output Signals .....	5-3
5-3	Example of Full External Multiplexing .....	5-10
5-4	QADC64 Module Block Diagram .....	5-12
5-5	Conversion Timing .....	5-13
5-6	Bypass Mode Conversion Timing .....	5-13
5-7	QADC64 Queue Operation with Pause .....	5-16
5-8	QADC64 Clock Subsystem Functions .....	5-26
5-9	QADC64 Clock Programmability Examples .....	5-28
5-10	QADC64 Interrupt Flow Diagram .....	5-30
5-11	QADC64 Interrupt Vector Format .....	5-33
5-12	QADC64 Conversion Queue Operation .....	5-46
5-13	AMUX/QADC64 Configured for Mixed Multiplexing .....	5-55
5-14	Analog Multiplexer Submodule Charging Current Illustration .....	5-57
6-1	QSMCM Block Diagram .....	6-2
6-2	QSPI Block Diagram .....	6-14
6-3	QSPI RAM .....	6-22
6-4	Flowchart of QSPI Initialization Operation .....	6-27
6-5	Flowchart of QSPI Master Operation (Part 1) .....	6-28
6-6	Flowchart of QSPI Master Operation (Part 2) .....	6-29
6-7	Flowchart of QSPI Master Operation (Part 3) .....	6-30
6-8	Flowchart of QSPI Slave Operation (Part 1) .....	6-31
6-9	Flowchart of QSPI Slave Operation (Part 2) .....	6-32
6-10	SCI Transmitter Block Diagram .....	6-42
6-11	SCI Receiver Block Diagram .....	6-43
6-12	Queue Transmitter Block Enhancements .....	6-60
6-13	Queue Transmit Flow .....	6-62
6-14	Queue Transmit Software Flow .....	6-63
6-15	Queue Transmit Example for 17 Data Bytes .....	6-64
6-16	Queue Transmit Example for 25 Data Frames .....	6-65
6-17	Queue Receiver Block Enhancements .....	6-66
6-18	Queue Receive Flow .....	6-69
6-19	Queue Receive Software Flow .....	6-70
6-20	Queue Receive Example for 17 Data Bytes .....	6-71
7-1	TouCAN Block Diagram .....	7-1
7-2	Typical CAN Network .....	7-3
7-3	Extended ID Message Buffer Structure .....	7-4
7-4	Standard ID Message Buffer Structure .....	7-4
7-5	TouCAN Interrupt Vector Generation .....	7-19
7-6	TouCAN Message Buffer Memory Map .....	7-23
8-1	TPU3 Block Diagram .....	8-1
8-2	TCR1 Prescaler Control .....	8-7
8-3	TCR2 Prescaler Control .....	8-8

**Figure  
Number**

**Page  
Number**



9-1	DPTRAM Configuration .....	9-2
10-1	Block Diagram for a CMFI EEPROM in the 256-Kbyte Configuration. ....	10-2
10-3	Shadow Information .....	10-12
10-2		10-12
10-4	Pulse Status Timing .....	10-19
10-5	Master Reset Configuration Timing .....	10-24
10-6	Program State Diagram .....	10-28
10-7	Erase State Diagram .....	10-33
11-1	SRAM Module Configuration .....	11-2
13-1	Configurable Timer Module, CTM9 Block Diagram .....	13-2
13-2	FCSM Block Diagram .....	13-5
13-3	MCSM Block Diagram .....	13-9
13-4	SASM Block Diagram .....	13-15
13-5	SASM Block Diagram (Channel A) .....	13-16
13-6	DASM Block Diagram .....	13-24
13-7	Input Pulse Width Measurement Example .....	13-27
13-8	Input Period Measurement Example .....	13-28
13-9	DASM Input Capture Example .....	13-29
13-10	Single Shot Output Pulse Example .....	13-31
13-11	Single Shot Output Transition Example .....	13-31
13-12	DASM Output Pulse Width Modulation Example .....	13-33
13-13	Pulse Width Modulation Submodule Block Diagram .....	13-39
13-14	CPSM Block Diagram .....	13-53
13-15	CTM9 Example — Single Edge Input Capture .....	13-56
13-16	CTM9 Example — Double Capture Pulse Width Measurement .....	13-57
13-17	CTM9 Example — Double Capture Period Measurement .....	13-58
13-18	CTM9 Example — Single Edge Output Compare .....	13-59
13-19	CTM9 Example — Double Edge Output Compare .....	13-60
13-20	CTM9 Example — Pulse Width Modulation Output .....	13-61
D-1	TPU3 Memory Map .....	D-1
D-2	PTA Parameters .....	D-4
D-3	QOM Parameters .....	D-6
D-4	TSM Parameters — Master Mode .....	D-8
D-5	TSM Parameters — Slave Mode .....	D-9
D-6	FQM Parameters .....	D-11
D-7	UART Transmitter Parameters .....	D-13
D-8	UART Receiver Parameters .....	D-14
D-9	NITC Parameters .....	D-16
D-10	COMM Parameters, Part 1 of 2 .....	D-18
D-11	COMM Parameters, Part 2 of 2 .....	D-19
D-12	HALLD Parameters .....	D-20
D-13	MCPWM Parameters — Master Mode .....	D-22

## Figure Number

## Page Number



D-14	MCPWM Parameters — Slave Edge-Aligned Mode .....	D-23
D-15	MCPWM Parameters — Slave Ch A Non-Inverted Center-Aligned Mode ...	D-24
D-16	MCPWM Parameters — Slave Ch B Non-Inverted Center-Aligned Mode ...	D-25
D-17	MCPWM Parameters — Slave Ch A Inverted Center-Aligned Mode .....	D-26
D-18	MCPWM Parameters — Slave Ch B Inverted Center-Aligned Mode .....	D-27
D-19	FQD Parameters — Primary Channel .....	D-29
D-20	FQD Parameters — Secondary Channel .....	D-30
D-21	PPWA Parameters .....	D-32
D-22	OC Parameters .....	D-34
D-23	PWM Parameters .....	D-36
D-24	DIO Parameters .....	D-38
D-25	SPWM Parameters, Part 1 of 2 .....	D-40
D-26	SPWM Parameters, Part 2 of 2 .....	D-41
D-27	Two Possible SIOP Configurations .....	D-42
D-28	SIOP Parameters .....	D-43
D-29	SIOP Function Data Transition Example .....	D-47
E-1	CLKOUT Output Timing Diagram .....	E-9
E-2	External Clock Input Timing Diagram .....	E-9
E-3	ECLK Output Timing Diagram .....	E-9
E-4	Read Cycle Timing Diagram .....	E-10
E-5	Write Cycle Timing Diagram .....	E-11
E-6	Fast Termination Read Cycle Timing Diagram .....	E-12
E-7	Fast Termination Write Cycle Timing Diagram .....	E-13
E-8	Bus Arbitration Timing Diagram — Active Bus Case .....	E-14
E-9	Bus Arbitration Timing Diagram — Idle Bus Case .....	E-15
E-10	Show Cycle Timing Diagram .....	E-15
E-11	Chip-Select Timing Diagram .....	E-16
E-12	Reset and Mode Select Timing Diagram .....	E-16
E-13	Background Debugging Mode Timing — Serial Communication .....	E-17
E-14	Background Debugging Mode Timing — Freeze Assertion .....	E-17
E-15	ECLK Timing Diagram .....	E-19
E-16	QSPI Timing — Master, CPHA = 0 .....	E-21
E-17	QSPI Timing — Master, CPHA = 1 .....	E-21
E-18	QSPI Timing — Slave, CPHA = 0 .....	E-22
E-19	QSPI Timing — Slave, CPHA = 1 .....	E-22
E-20	TPU Timing Diagram .....	E-23
E-21	EPEB0 Pin Timing .....	E-34
E-22	V <sub>PP</sub> and V <sub>DD</sub> Power Sequencing .....	E-35
E-23	A Recommended External V <sub>PP</sub> Pin Conditioning Circuit .....	E-36