# SECTION 8
# STANDBY RAM WITH TPU EMULATION

The standby RAM module with TPU emulation capability (TPURAM) consists of a control register block and a 2-Kbyte array of fast (two system clock) static RAM, which is especially useful for system stacks and variable storage. The TPURAM responds to both program and data space accesses. The TPURAM can also be used to emulate TPU microcode ROM.

## 8.1 General

The TPURAM can be mapped to any 2-Kbyte boundary in the address map, but must not overlap the module control registers as overlap makes the registers inaccessible. Data can be read or written in bytes, words or long words. The TPURAM is powered by $V_{DD}$ in normal operation. During power-down, TPURAM contents can be maintained by power from the $V_{STBY}$ input. Power switching between sources is automatic.

## 8.2 TPURAM Register Block

There are three TPURAM control registers: the TPURAM module configuration register (TRAMMCR), the TPURAM test register (TRAMTST), and the TPURAM base address and status register (TRAMBAR). To protect these registers from accidental modification, they are always mapped to supervisor data space.

The TPURAM control register block begins at address $7FFB00 or $FFFB00, depending on the value of the module mapping (MM) bit in the SIM configuration register (SIMCR). Refer to **5.2.1 Module Mapping** for more information on how the state of MM affects the system.

The TPURAM control register block occupies eight bytes of address space. Unimplemented register addresses are read as zeros, and writes have no effect. Refer to **APPENDIX D REGISTER SUMMARY** for register block address map and register bit/field definitions.

## 8.3 TPURAM Array Address Mapping

The base address and status register TRAMBAR specifies the TPURAM array base address in the MCU memory map. TRAMBAR[15:4] specify the 12 high-order bits of the base address. The TPU bus interface unit compares these bits to address lines ADDR[23:12]. If the two match, then the low order address lines and the SIZ[1:0] signals are used to access the RAM location in the array.

The RAM disable (RAMDS) bit, the LSB of TRAMBAR, indicates whether the TPURAM array is active (RAMDS = 0) or disabled (RAMDS = 1). The array is disabled coming out of reset and remains disabled if the base address field is programmed with an address that overlaps the address of the module control register block. Writing a valid base address to TRAMBAR[15:4] clears RAMDS and enables the array.

TRAMBAR can be written only once after a reset. This prevents runaway software from accidentally re-mapping the array. Because the locking mechanism is activated by the first write after a reset, the base address field should be written in a single word operation. Writing only one-half of the register prevents the other half from being written.

## 8.4 TPURAM Privilege Level

The RASP field in TRAMMCR specifies whether access to the TPURAM can be made from supervisor mode only, or from either user or supervisor mode. If supervisor-only access is specified, an access from user mode is ignored by the TPURAM control logic and can be decoded externally. Refer to **4.7 Privilege Levels** and **5.5.1.7 Function Codes** for more information concerning privilege levels.

## 8.5 Normal Operation

During normal operation, the TPURAM control registers and array can be accessed by the CPU32, by byte, word, or long word. A byte or aligned word access takes one bus cycle (two system clock cycles). A long word access requires two bus cycles. Misaligned accesses are not permitted by the CPU32 and will result in an address error exception. Refer to **5.6 Bus Operation** for more information concerning access times. The TPU cannot access the array and has no effect on the operation of the TPURAM during normal operation.

## 8.6 Standby Operation

Standby mode maintains the RAM array when the MCU main power supply is turned off.

Relative voltage levels of the $V_{DD}$ and $V_{STBY}$ pins determine whether the TPURAM is in standby mode. TPURAM circuitry switches to the standby power source when specified limits are exceeded. The TPURAM is essentially powered by the power supply pin with the greatest voltage (for example, $V_{DD}$ or $V_{STBY}$). If specified standby supply voltage levels are maintained during the transition, there is no loss of memory when switching occurs. The RAM array cannot be accessed while the TPURAM is powered from $V_{STBY}$. If standby operation is not desired, connect the $V_{STBY}$ pin to the $V_{SS}$ pin.

$I_{SB}$ (SRAM standby current) may exceed specified maximum standby current during the time $V_{DD}$ makes the transition from normal operating level to the level specified for standby operation. This occurs within the voltage range $V_{SB} - 0.5\ V \leq V_{DD} \leq V_{SS} + 0.5\ V$. Typically, $I_{SB}$ peaks when $V_{DD} \approx V_{SB} - 1.5\ V$, and averages 1.0 mA over the transition period.

Refer to **APPENDIX A ELECTRICAL CHARACTERISTICS** for standby switching and power consumption specifications.

## 8.7 Low-Power Stop Operation

Setting the STOP bit in TRAMMCR places the TPURAM in low-power stop mode. In low-power stop mode, the array retains its contents, but cannot be read or written by the CPU32. STOP can be written only when the processor is operating in supervisor mode. STOP is set during resets. Low-power stop mode is exited by clearing STOP.

The TPURAM module will switch to standby mode while it is in low-power mode, provided the operating constraints discussed above are met.

## 8.8 Reset

Reset places the TPURAM in low-power stop mode, enables supervisor mode access only, clears the base address register, and disables the array. These actions make it possible to write a new base address into the base address register.

When a synchronous reset occurs while a byte or word TPURAM access is in progress, the access is completed. If reset occurs during the first word access of a long-word operation, only the first word access is completed. If reset occurs during the second word access of a long-word operation, the entire access is completed. Data being read from or written to the TPURAM may be corrupted by asynchronous reset. Refer to **5.7 Reset** for more information concerning resets.

## 8.9 TPU Microcode Emulation

The TPURAM array can emulate the microcode ROM in the TPU module. This provides a means for developing custom TPU code. The TPU selects TPU emulation mode.

The TPU is connected to the TPURAM via a dedicated bus. While the TPURAM array is in TPU emulation mode, the access timing of the TPURAM module matches the timing of the TPU microcode ROM to ensure accurate emulation. Normal accesses through the IMB are inhibited and the control registers have no effect, allowing external RAM to emulate the TPURAM at the same addresses. Refer to **SECTION 7 TIME PROCESSOR UNIT** and to the ***TPU Reference Manual*** (TPURM/AD) for more information.