SECTION 2
SIGNAL DESCRIPTIONS

This section describes the MPC509 signals and pins. For a more detailed discussion of a particular signal, refer to the section of the manual that discusses the function involved.

2.1 Pin List

Table 2-1 MPC509 Pin List

Primary Function(s)	Port Function
Address Bus, Data Bus, Chip Selects	
ADDR[0:11]/$\overline{\text{CS}}$[0:11]	PA[0:7], PB[0:3]
ADDR[12:15]	PB[4:7]
ADDR[16:29]	—
DATA[0:31]	—
$\overline{\text{CSBOOT}}$	—
Bus Control, Clock, Development Support	
$\overline{\text{BURST}}$, $\overline{\text{TEA}}$, $\overline{\text{AACK}}$, $\overline{\text{TA}}$, $\overline{\text{BE}}$[0:1], $\overline{\text{BE2}}$/ADDR30, $\overline{\text{BE3}}$	PI[0:7]
AT[0:1], $\overline{\text{TS}}$, CT[0:3]	PJ[1:7]
$\overline{\text{BDIP}}$, $\overline{\text{WR}}$, PLLL/DSDO, VF[0:2], VFLS[0:1]	PK[0:7]
$\overline{\text{WP}}$[0:5]	PL[2:7]
$\overline{\text{BI}}$, $\overline{\text{BR}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{ARETRY}}$	PM[3:7]
$\overline{\text{CR}}$/$\overline{\text{DS}}$	—
DSCK, DSDI	—
XTAL, EXTAL, XFCN, XFCP, CLKOUT, ECROUT, PDWU, MODCLK	—
Reset, Interrupts	
$\overline{\text{RESET}}$, $\overline{\text{RESETOUT}}$	—
$\overline{\text{IRQ}}$[0:6]	PQ[0:6]
Test	
TDI, TDO, TCK, TMS, TRST	—
Power	

Table 2-1 MPC509 Pin List (Continued)

Primary Function(s)	Port Function
V_{DDSN}, V_{SSSN}	—
V_{DDI}, V_{SSI}	—
V_{DDE}, V_{SSE}	—
VDDKAP1, VDDKAP2	—

2.2 Pin Characteristics

Table 2-2 shows the characteristics of the MPC509 pins. Assume the model for output only and three-state I/O buffers shown in **Figure 2-1**.

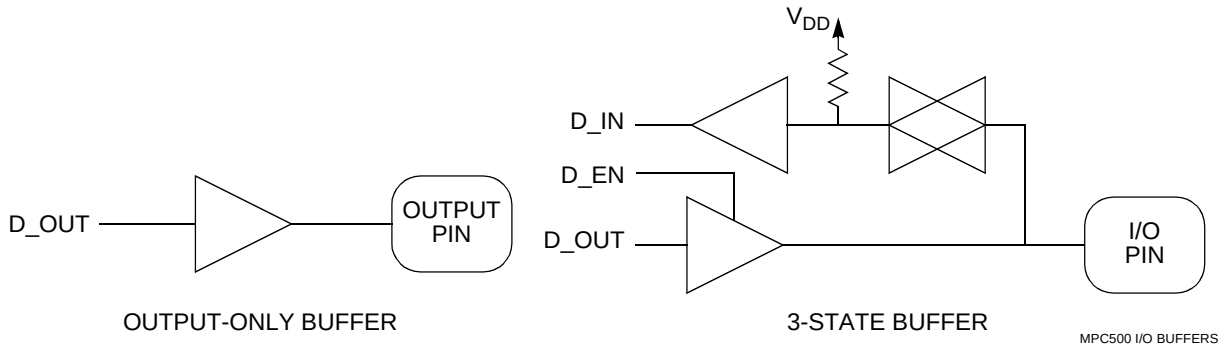

Figure 2-1 Output-Only and Three-State I/O Buffers

Table 2-2 EBI Pin Definitions

Mnemonic	Buffer Type	Weak Pull-Up[1]	When Bus is Granted	When Bus Is Not Granted	During Reset
Address and Data Bus					
$\overline{CS}$[0:11]/ ADDR[0:11]	Output only	No	Driven	Driven high	Initially high, changes five clock cycles after reset source is negated
ADDR[12:29]	3-state	No	Driven unless config-ured as input port	Float unless config-ured as output port	Float
DATA[0:31]	3-state	No	Driven if write, float if read	Float unless config-ured as output port	Float
Transfer Attributes					

Table 2-2 EBI Pin Definitions (Continued)

Mnemonic	Buffer Type	Weak Pull-Up[1]	When Bus is Granted	When Bus Is Not Granted	During Reset
$\overline{WR}$	3-state	No	Output unless configured as input ports	Float unless configured as output port	Float
$\overline{BURST}$	3-state	No			
$\overline{BE[0:3]}$	3-state	No			
AT[0:1]	3-state	No			
CT[0:3]	3-state	No			
Transfer Handshakes					
$\overline{TS}$	3-state	No	Output unless configured as input port	Float unless configured as output port	Input port; output three-stated
$\overline{AACK}$	3-state	Yes	Input unless configured as an output port	Float unless configured as output port	Input port; output three-stated
$\overline{BDIP}/\overline{LAST}$	3-state	No	Output unless configured as input port	Float unless configured as output port	Input port. After reset, driven by CPU
$\overline{BI}$	3-state	Yes	Input unless configured as output port		Float
$\overline{TA}$	3-state	Yes	Input unless configured as an output port	Float (listen only); only driven if configured as output port	Input port; output three-stated
$\overline{TEA}$	3-state	Yes	Input unless configured as an output port	Float (listen only); only driven if configured as output port	Input port; output three-stated
$\overline{ARETRY}$	3-state	Yes	Input unless configured as output port	Input; driven if configured as output port	Input port; output three-stated
Arbitration					
$\overline{BR}$	3-state	No	Output unless configured as input port. Not affected by $\overline{BG}$.		Float
$\overline{BG}$	3-state	Weak pulldown	Input unless configured as output port	Output only if configured as output port	Float
$\overline{BB}$	3-state	Yes	Output unless configured as input port	If relinquishing drive high then float unless configured as output port	Float
Miscellaneous					
$\overline{CR}/\overline{DS}$	3-state	Yes	Not affected by $\overline{BG}$. Input unless configured for secondary function		Float
$\overline{RESETOUT}$	Output	No	Not affected by $\overline{BG}$		—
$\overline{RESET}$	Input	No	Not affected by $\overline{BG}$		—
CLKOUT	Output	No	Not affected by $\overline{BG}$		Not affected

NOTES:
1. Weak pull-ups can maintain an internal logic level one but may not maintain a logic level one on external pins.

2.3 Power Connections

Table 2-3 shows the MPC509 power connections.

Table 2-3 MPC509 Power Connections

Pin	Description
V_{DDE}, V_{SSE}	External periphery power
V_{DDI}, V_{SSI}	Internal module power
V_{DDSN}, V_{SSSN}	Clock synthesizer power
VDDKAP1	Keep-alive power for the internal oscillator, time base, and decrementer
VDDKAP2	Keep-alive power for the SRAM array

CAUTION

The keep-alive power pins (VDDKAP1 and VDDKAP2) must be powered up before or at the same time as V_{DD} (V_{DDI}, V_{DDE}, and V_{DDSN}). Otherwise, an excessive draw may result.

2.4 Pins with Internal Pull-Ups and Pulldowns

Table 2-4 lists MPC509 pins with internal pull-ups or pulldowns.

Table 2-4 Pins with Internal Pull-Ups/Pulldowns

Pin	Pull-up/Pull-down
$\overline{TA}$	Pull-up
$\overline{TEA}$	
$\overline{AACK}$	
$\overline{ARETRY}$	
$\overline{CR}$	
$\overline{BI}$	
$\overline{BB}$	
$\overline{IRQ[0:6]}$	
TMS	
$\overline{TRST}$	
TDI	

Table 2-4 Pins with Internal Pull-Ups/Pulldowns

Pin	Pull-up/Pull-down
$\overline{BG}$	Pull-down
DSCK	
DSDI	
TCK	

2.5 Signal Descriptions

MPC509 signals are summarized in **Table 2-5** and described in the following subsections. Since pins often have more than one function, more than one description may apply to a pin.

Table 2-5 Signal Descriptions

Mnemonic	Module	Direction	Description
ADDR[0:29]	EBI	Output	32-bit address bus. Driven by the bus master to index the bus slave. Low-order bit (ADDR31) not pinned out — use byte enables instead. BE2 functions as ADDR30 during accesses to 16-bit ports.
$\overline{AACK}$	EBI	Input	Address acknowledge. When asserted, indicates the slave has received the address from the bus master.
$\overline{ARETRY}$	EBI	Input	When asserted, indicates the master needs to retry its address phase.
AT[0:1]	EBI	Output	Address types. Define addressed space as user or supervisor, data or instruction.
$\overline{BB}$	EBI	Input/Output	Bus busy. Asserted by current bus master to indicate the bus is currently in use. Prospective new master should wait until the current master negates this signal.
$\overline{BDIP}$	EBI	Output	Burst data in progress. Asserted at the beginning of a burst cycle and negated prior to the last beat. This signal can be negated prior to the end of a burst to terminate the burst data phase early.
$\overline{BE[0:3]}$	EBI	Output	Byte enables. One byte enable per byte lane of the data bus.
$\overline{BG}$	EBI	Input	Bus grant. When asserted by bus arbiter, the bus is granted to the bus master. Each master has its own bus grant signal.
$\overline{BI}$	EBI	Input	Burst inhibit. When asserted, indicates the slave does not support burst mode.
$\overline{BR}$	EBI	Output	Bus request. When asserted, indicates the potential bus master is requesting the bus. Each master has its own bus request signal.
$\overline{BURST}$	EBI	Output	If asserted, indicates cycle is a burst cycle.
CLKOUT	EBI	Output	Continuously-running clock. All signals driven on the E-bus must be synchronized to the rising edge of this clock.
$\overline{CR}$	EBI	Input	Cancel reservation. Each RCPU has its own $\overline{CR}$ signal. When asserted, instructs the bus master to clear its reservation.

Table 2-5 Signal Descriptions (Continued)

Mnemonic	Module	Direction	Description
$\overline{\text{CSBOOT}}$	Chip Selects	Output	Chip select of system boot memory.
$\overline{\text{CS[0:11]}}$	Chip Selects	Output	Chip-select signals for external memory devices.
CT[0:3]	EBI	Output	Cycle type signals. Indicate what type of bus cycle the bus master is initiating.
DATA[0:31]	EBI	Input/Output	32-bit data bus.
$\overline{\text{DS}}$	EBI	Output	Data strobe. Asserted by EBI at the end of a chip-select-controlled bus cycle after the chip-select unit asserts the internal $\overline{\text{TA}}$ signal or the bus monitor timer asserts the internal $\overline{\text{TEA}}$ signal. Also asserted at the end of a show cycle. Used primarily by development tools.
DSCK	Dev. Support	Input	Development serial clock. Used to clock data shifted into or out of development serial port.
DSDI	Dev. Support	Input	Development serial data in. Used to shift development serial data into the development port shift register.
DSDO	Dev. Support	Output	Development serial data out. Used to shift development serial data out of the development port shift register.
ECROUT	Clocks	Output	Provides a clock reference output with a frequency equal to the crystal oscillator frequency, taken from the PLL feedback signal.
EXTAL	Clocks	Input	Connection for external crystal to the internal oscillator circuit, or clock input.
$\overline{\text{IRQ[0:6]}}$	PCU	Input	Interrupt request inputs.
MODCLK	Clocks	Input	Clock mode. The state of this signal and that of V_{DDSN} during reset determine the source of the system clock (normal operation, 1:1 mode, PLL bypass mode, or special test mode). Refer to **Table 5-32** in **SECTION 5 SYSTEM INTERFACE UNIT** for details.
PA[0:7]	Ports	Output	Port A discrete output signals.
PB[0:7]	Ports	Output	Port B discrete output signals.
PDWU	Clocks	Output	Power-down wakeup to external power-on reset circuit.
PI[0:7]	Ports	Input/Output	Port I discrete input/output signals.
PJ[0:7]	Ports	Input/Output	Port J discrete input/output signals.
PK[0:7]	Ports	Input/Output	Port K discrete input/output signals.
PL[2:7]	Ports	Input/Output	Port L discrete input/output signals.
PM[3:7]	Ports	Input/Output	Port M discrete input/output signals.
PQ[0:6]	PCU	Input/Output	Port Q discrete input/output signals.
PLLL	Clock	Output	Indicates whether phase-locked loop is locked.
$\overline{\text{RESET}}$	EBI	Input	Hard reset. When asserted, devices on the bus must reset.

Table 2-5 Signal Descriptions (Continued)

Mnemonic	Module	Direction	Description
$\overline{\text{RESETOUT}}$	EBI	Output	Reset output signal. Asserted by MCU during reset. When asserted, instructs all devices monitoring this signal to reset all parts within themselves that can be reset by software.
$\overline{\text{TA}}$	EBI	Input	Transfer acknowledge. When asserted, indicates the slave has received the data during a write cycle or returned the data during a read cycle.
TCK	JTAG	Input	Test clock input with a pull-down resistor to synchronize the test logic.
TDI	JTAG	Input	Test data input with a pull-up resistor sampled on the rising edge of TCK.
TDO	JTAG	Output	Three-statable test data output that changes on the falling edge of TCK.
$\overline{\text{TEA}}$	EBI	Input	Transfer error acknowledge. Asserted by an external device to signal a bus error condition.
TMS	JTAG	Input	Test mode select input with a pull-up resistor. Sampled on the rising edge of TCK to sequence the test controller's state machine.
$\overline{\text{TRST}}$	JTAG	Input	Asynchronous active-low test reset with a pull-up resistor that provides initialization of the TAP controller and other logic as required by the standard.
$\overline{\text{TS}}$	EBI	Output	Transfer start. When asserted, indicates the start of a bus cycle.
V_{DDSN}	Clocks	Input	Power supply input to the VCO. In addition, the state of this signal and that of MODCLK during reset determine the source of the system clock (normal operation, 1:1 mode, PLL bypass mode, or special test mode). Referto **Table 5-32** in **SECTION 5 SYSTEM INTERFACE UNIT** for details.
VF[0:2]	Dev. Support	Output	Denotes the last fetched instruction or how many instructions were flushed from the instruction queue.
VFLS[0:1]	Dev. Support	Output	Denotes how many instructions are flushed from the history buffer during the current clock cycle. Also indicates freeze state.
V_{SSSN}	Clocks	Input	Power ground input to the VCO.
WP[0:5]	Dev. Support	Output	Output signals for I-bus watchpoints (WP[0:3]) and L-bus watchpoints (WP[4:5]).
XTAL	Clocks	Output	Connection for external crystal to the internal oscillator circuit.
$\overline{\text{WR}}$	EBI	Output	Asserted (low): write cycle. Negated (high): read cycle.
XFCN, XFCP	Clocks	Input	Used to add an external capacitor to the filter circuit of the phase-locked loop.

2.5.1 Bus Arbitration and Reservation Support Signals

The bus arbitration signals request the bus, recognize when the request is granted, and indicate to other devices when mastership is granted. There are no separate arbitration phases for the address and data buses. For a detailed description of how these signals interact, see **5.4.5.1 Arbitration Phase**.

The cancel reservation ($\overline{CR}$) signal is used to indicate that the processor should not perform any **stwcx.** cycle to external memory. This signal is sampled at the same time the MCU samples the arbitration pins for a qualified bus grant.

2.5.1.1 Bus Request ($\overline{BR}$)

Output only
Module: EBI

State Meaning

Asserted — Indicates the potential bus master is requesting the bus. Each master has its own bus request signal. The SIU asserts $\overline{BR}$ to request bus mastership if its bus grant ($\overline{BG}$) pin is not already asserted and the bus busy ($\overline{BB}$) has not been negated by the current bus master.

The SIU assumes mastership of the external bus only after receiving a qualified bus grant. This occurs when the bus arbiter asserts $\overline{BG}$ to the SIU and the $\overline{BB}$ pin has also been negated by the previous bus master. The SIU cannot start a cycle on the external bus if the current master is holding the $\overline{BB}$ pin asserted, even if the SIU has received a bus grant ($\overline{BG}$ asserted) from the bus arbiter.

Negated — Indicates the MCU is not requesting the address bus. The MCU may have no bus operation pending, it may be parked, or the MCU may be in the process of releasing the bus in response to $\overline{ARETRY}$.

Timing Comments

Assertion — Occurs when the MCU is not parked and a bus transaction is needed.

Negation — Occurs as soon as the SIU starts a bus cycle after receiving a qualified bus grant.

2.5.1.2 Bus Grant ($\overline{BG}$)

Input only
Module: EBI

State Meaning

Asserted — (By bus arbiter) indicates the bus is granted to the requesting device. The signal can be kept asserted to allow the current master to park the bus. Single-master systems can tie this signal low permanently.

Negated — Indicates the requesting device is not granted bus mastership.

Timing Comments

Assertion — May occur at any time to indicate the MCU is free to use the address bus. After the MCU assumes bus mastership, it does not check for a qualified bus grant again until the cycle during which the address bus tenure is com-

pleted (assuming it has another transaction to run). The MCU does not accept a $\overline{BG}$ in the cycles between the assertion of any $\overline{TS}$ and $\overline{AACK}$.

Negation — May occur at any time to indicate the MCU cannot use the bus. The MCU may still assume bus mastership on the clock cycle of the negation of $\overline{BG}$ because during the previous cycle $\overline{BG}$ indicated to the MCU that it was free to take mastership (if qualified).

2.5.1.3 Bus Busy ($\overline{BB}$)

Input/Output
Module: EBI

State Meaning

Asserted — The current bus master asserts this signal to indicate the bus is currently in use. The prospective new master must wait until the current master negates this signal.

Negated — Indicates that the bus is not owned by another bus master and that the bus is available to the MCU when accompanied by a qualified bus grant.

Timing Comments

Assertion — $\overline{BB}$ is asserted during the address phase of each external bus cycle, if it was previously negated. It remains asserted between internal atomic cycles (any non-burst word accesses to an external 16-bit port).

Negation — Occurs during the clock cycle following termination of the data phase of an external bus cycle. The signal is negated for half a clock cycle and then placed in a high-impedance state.

2.5.1.4 Cancel Reservation ($\overline{CR}$)

Input only
Module: EBI

State Meaning

Asserted — (By an external bus arbiter or reservation snooping logic) indicates that there is no outstanding reservation on the external bus. Each RCPU has its own $\overline{CR}$ signal. Assertion indicates that the processor should not perform any **stwcx.** cycle to external memory.

Negated — Indicates there is an outstanding reservation on the external bus.

Timing Comments

Assertion — Can occur at any rising edge of the bus clock. This signal is sampled at the same time the MCU samples the arbitration pins for a qualified bus grant prior to starting a bus cycle.

2.5.2 Address Phase Signals

The address phase is the period of time from the assertion of transfer start ($\overline{TS}$) until the address phase is terminated by one of the following signals: address acknowledge ($\overline{AACK}$), address retry ($\overline{ARETRY}$), or transfer error acknowledge ($\overline{TEA}$). $\overline{TS}$ is valid for one clock cycle at the start of the address phase. The address bus and the address attributes described below are valid for the duration of the address phase. Refer to **5.4.5.2 Address Phase** for additional information on address phase signals.

2.5.2.1 Address Bus (ADDR[0:29])

Output only
Module: EBI

State Meaning — Asserted/Negated — Represents the physical address of the data to be transferred. Driven by the bus master to index the bus slave. Low-order bit (ADDR31) is not pinned out; byte enable signals (BE[0:3]) are used instead (see **Table 2-6**). During accesses to 16-bit ports, $\overline{BE2}$ pin provides ADDR30 signal.

Timing Comments — Assertion/Negation — Occurs one clock cycle after a qualified bus grant. Coincides with assertion of $\overline{BB}$ and $\overline{TS}$.

High impedance — Coincides with negation of $\overline{BB}$, provided no qualified bus grant exists.

2.5.2.2 Write/Read ($\overline{WR}$)

Output only
Module: EBI

State Meaning — Asserted/Negated — This signal is driven high for a read cycle and low for a write cycle.

Timing Comments — Assertion/Negation — $\overline{WR}$ is an address attribute; it is updated at the start of the address phase and maintained until the start of the next address phase. Note that for pipelined accesses, it is not valid during the data phase.

High impedance — Coincides with negation of $\overline{BB}$, provided no qualified bus grant exists.

2.5.2.3 Burst Indicator ($\overline{BURST}$)

Output only
Module: EBI

State Meaning — Asserted — indicates a burst cycle. If a burst access is burst-inhibited by the slave, $\overline{BURST}$ is driven during each single-beat (decomposed) cycle.

Negated — Indicates current cycle is not a burst cycle.

Timing Comments

Assertion/Negation — $\overline{\text{BURST}}$ is an address attribute; it is updated at the start of the address phase and maintained until the start of the next address phase.

High impedance — Coincides with negation of $\overline{\text{BB}}$, provided no qualified bus grant exists.

2.5.2.4 Byte Enables ($\overline{\text{BE[0:3]}}$)

Output only
Module: EBI

State Meaning

$\overline{\text{BE[0:3]}}$ indicate which byte within a word is being accessed. External memory chips can use these signals to determine which byte location is enabled. **Table 2-6** explains the encodings during accesses to 32-bit and 16-bit ports.

Table 2-6 Byte Enable Encodings

Byte Enable	Use During 32-Bit Port Access	Use During 16-Bit Port Access
$\overline{\text{BE0}}$	Byte enable for DATA[0:7]	Byte enable for DATA[0:7]
$\overline{\text{BE1}}$	Byte enable for DATA[8:15]	Byte enable for DATA[8:15]
$\overline{\text{BE2}}$	Byte enable for DATA[16:23]	ADDR30
$\overline{\text{BE3}}$	Byte enable for DATA[24:31]	0 = Operand size is word 1 = Operand size is byte or half-word

Timing Comments

Assertion/Negation — The $\overline{\text{BE[0:3]}}$ signals are address attributes; they are updated at the start of the address phase and maintained until the start of the next address phase.

High impedance — Coincides with negation of $\overline{\text{BB}}$, provided no qualified bus grant exists.

2.5.2.5 Transfer Start ($\overline{\text{TS}}$)

Output only
Module: EBI

State Meaning

Asserted — Indicates the start of a bus cycle.

Timing Comments

Assertion — Coincides with the assertion of $\overline{\text{BB}}$.

Negation — Occurs one clock cycle after $\overline{\text{TS}}$ is asserted.

High impedance — Coincides with negation of $\overline{\text{BB}}$, provided no qualified bus grant exists.

2.5.2.6 Address Acknowledge ($\overline{\text{AACK}}$)

Input only
Module: EBI

State Meaning

Asserted — Indicates that the address phase of a transaction is complete.

If the external access is to a chip-select region for which the chip select is programmed to return $\overline{\text{AACK}}$ and $\overline{\text{TA}}$, then the external bus interface uses the logical OR of the external $\overline{\text{AACK}}$ pin and the $\overline{\text{AACK}}$ signal returned by the chip select. If the chip select returns $\overline{\text{AACK}}$, it is not visible on the external pins.

Negated — (While the MCU is driving $\overline{\text{BB}}$) indicates that the address bus and the transfer attributes must remain driven.

Timing Comments

Assertion — May occur as early as the clock cycle after $\overline{\text{TS}}$ is asserted; assertion can be delayed to allow adequate address access time for slow devices. $\overline{\text{AACK}}$ should be asserted at the same time as or prior to the assertion of $\overline{\text{TA}}$. If $\overline{\text{AACK}}$ is returned prior to the assertion of $\overline{\text{TA}}$, the SIU can initiate another cycle while the previous cycle is still in progress; that is, returning $\overline{\text{AACK}}$ early allows pipelining of bus cycles.

Negation — Must occur one clock cycle after the assertion of $\overline{\text{AACK}}$.

High impedance — Coincides with negation of $\overline{\text{BB}}$, provided no qualified bus grant exists.

2.5.2.7 Burst Inhibit ($\overline{\text{BI}}$)

Input only
Module: EBI

State Meaning

Asserted — Indicates the addressed device does not have burst capability. When this signal is asserted, the SIU decomposes the transfer into multiple cycles, incrementing the address for each cycle.

For systems that do not use burst mode at all, this signal can be tied low permanently.

Negated — Indicates the device supports burst mode, or that the $\overline{\text{BI}}$ signal is being sent by the chip-select unit. For systems that use SIU chip selects with all external memory, the $\overline{\text{BI}}$ pin can remain negated; the chip-select unit can be programmed to assert $\overline{\text{BI}}$ to prevent bursts.

Timing Comments

Assertion/Negation — Sampled when $\overline{\text{AACK}}$ is asserted. A burst transfer can only be burst-inhibited before the first $\overline{\text{TA}}$ assertion.

Simple, asynchronous memory devices should keep $\overline{\text{AACK}}$ negated to keep the address valid. They can assert $\overline{\text{BI}}$ at the same time as or before $\overline{\text{AACK}}$ and at the same time as the first $\overline{\text{TA}}$ assertion.

Synchronous, pipelineable memory devices that do not support bursting should return $\overline{\text{BI}}$ with $\overline{\text{AACK}}$ as soon as they are ready to receive the next address.

Burstable memory devices should negate $\overline{\text{BI}}$ at the same time as or before they assert $\overline{\text{AACK}}$.

2.5.2.8 Address Retry ($\overline{\text{ARETRY}}$)

Input only
Module: EBI

State Meaning

Asserted — If the MCU is the bus master, $\overline{\text{ARETRY}}$ indicates that the MCU must retry the preceding address phase. The MCU will not begin a bus cycle for the clock cycle following assertion of $\overline{\text{ARETRY}}$. Note that the subsequent address retried may not be the same one associated with the assertion of the $\overline{\text{ARETRY}}$ signal. Assertion of $\overline{\text{ARETRY}}$ overrides the assertion of $\overline{\text{AACK}}$.

Negated/High Impedance — Indicates that the MCU does not need to retry the last address phase.

Timing Comments

Assertion — Must occur at least one clock cycle following the assertion of $\overline{\text{TS}}$ if a retry is required. $\overline{\text{TA}}$ or $\overline{\text{TEA}}$ must not be asserted during a cycle in which $\overline{\text{ARETRY}}$ is asserted. If $\overline{\text{TA}}$ is asserted for any part of a burst cycle, $\overline{\text{ARETRY}}$ must not be asserted at any time during the cycle; if $\overline{\text{ARETRY}}$ is asserted during a burst cycle, it must be asserted before the first beat is terminated with $\overline{\text{TA}}$.

Note that $\overline{\text{BB}}$ is not negated until the second clock cycle after $\overline{\text{ARETRY}}$ assertion.

Negation — Must occur one clock cycle after assertion of $\overline{\text{ARETRY}}$.

2.5.2.9 Address Type (AT[0:1])

Output only
Module: EBI

State Meaning

Asserted/Negated — AT[0:1] define the addressed space as user or supervisor and as data or instruction, as shown

in **Table 2-7**.

Table 2-7 Address Type Definitions

AT[0:1]	Address Space Definition
0b00	User, data
0b01	User, instruction
0b10	Supervisor, data
0b11	Supervisor, instruction

Timing Comments Assertion/Negation — The AT[0:1] signals are address attributes; they are updated at the start of the address phase and maintained until the start of the next address phase.

High impedance — Coincides with negation of $\overline{BB}$, provided no qualified bus grant exists.

2.5.2.10 Cycle Types (CT[0:3])

Output only
Module: EBI

State Meaning Asserted/Negated — Cycle type signals. Indicate what type of bus cycle the bus master is initiating. Refer to **Table 5-14** in **SECTION 5 SYSTEM INTERFACE UNIT** for cycle type encodings.

Timing Comments Assertion/Negation — The CT[0:3] signals are address attributes; they are updated at the start of the address phase and maintained until the start of the next address phase.

High impedance — Coincides with negation of $\overline{BB}$, provided no qualified bus grant exists.

2.5.3 Data Phase Signals

Depending on the state of the pipeline, the data phase starts either one clock cycle after the address phase starts, or as soon as the previous data phase completes. The data phase completes when it is terminated by transfer acknowledge ($\overline{TA}$) or transfer error acknowledge ($\overline{TEA}$). If the cycle is a burst cycle, then multiple $\overline{TA}$ assertions are required to terminate the data phase. Refer to **5.4.5.3 Data Phase** for additional information on data phase signals.

2.5.3.1 Data Bus (DATA[0:31])

Input/output
Module: EBI

State Meaning Asserted/Negated — Represents the state of data during a

read or write. 16-bit devices must reside on DATA[0:15]. 32-bit devices reside on DATA[0:31].

Timing Comments

Assertion/negation — On write cycles, the SIU drives data one clock after driving $\overline{TS}$. The data is available until the slave asserts $\overline{TA}$.

During reads, the data must be available from the slave with $\overline{TA}$. The data bus is driven once for non-burst transactions and four times for burst transactions.

High impedance — The pins are placed in a high-impedance state during reads, or while the bus is idle, or when the bus is arbitrated away. For write cycles, the high-impedance state occurs on the clock cycle after the final assertion of $\overline{TA}$.

2.5.3.2 Burst Data in Progress ($\overline{BDIP}$)

Output only
Module: EBI

State Meaning

Asserted — Indicates the data beat in front of the current one is needed by the master. This signal is asserted at the beginning of a burst data phase.

Negated — Indicates the final beat of a burst. This signal can be negated prior to the end of a burst to terminate the burst data phase early.

Timing Comments

Assertion/Negation — When the LST bit in the SIUMCR is set, $\overline{BDIP}$ uses the timing for the $\overline{LAST}$ signal. When LST is cleared, $\overline{BDIP}$ uses the timing for the $\overline{BDIP}$ signal. Refer to **5.5.16.6 Synchronous Burst Interface** for more information.

High impedance — Coincides with negation of $\overline{BB}$, provided no qualified bus grant exists.

2.5.3.3 Transfer Acknowledge ($\overline{TA}$)

Input only
Module: EBI

State Meaning

Asserted — Indicates the slave has received the data during a write cycle or returned the data during a read cycle. Note that $\overline{TA}$ must be asserted for each data beat in a burst transaction.

If the external access is to a chip-select region for which the chip-select circuit is programmed to return $\overline{AACK}$ and $\overline{TA}$, the EBI uses the logical OR of the external $\overline{TA}$ pin and the internal $\overline{TA}$ signal returned by the chip-select unit.

Negated — (While $\overline{BB}$ is asserted) indicates that, until $\overline{TA}$ is asserted, the MCU must continue to drive the data for the current write or must wait to sample the data for reads.

Timing Comments

Assertion — Must not occur before $\overline{AACK}$ is asserted for the current transaction. $\overline{TA}$ must not be asserted on cycles terminated by $\overline{ARETRY}$ and must not be asserted after the cycle has been terminated. The system can withhold assertion of $\overline{TA}$ to indicate that the MCU should insert wait states to extend the duration of the data beat.

Negation — Must occur after the clock cycle of the final (or only) data beat of the transfer. For a burst transfer that is not under chip-select control, the system can assert $\overline{TA}$ for one clock cycle and then negate it to advance the burst transfer to the next beat and insert wait states during the next beat.

2.5.3.4 Transfer Error Acknowledge ($\overline{TEA}$)

Input only
Module: EBI

State Meaning

Asserted — (By an external device) signals a bus error condition. $\overline{TEA}$ assertion terminates the data phase of the current bus cycle and overrides the assertion of $\overline{TA}$. If $\overline{AACK}$ has not been asserted for the current bus cycle, $\overline{TEA}$ terminates both the address phase and the data phase.

This signal is intended for the cases of a write to a read-only address space or an access to a non-existent address. The signal can be output by a bus monitor timer or some system address protection mechanism, such as the chip-select logic.

Negated — Indicates that no external device has signaled a bus error.

Timing Comments

Assertion — May occur at any time during the address phase or data phase of a bus cycle.

Negation — Must occur one clock cycle after assertion of $\overline{TEA}$.

2.5.3.5 Data Strobe ($\overline{DS}$)

Output only
Module: EBI

State Meaning

Asserted — (By EBI) indicates the termination of a cycle from an internal source ($\overline{TA}$ or $\overline{TEA}$ assertion from the chip select unit, $\overline{TEA}$ assertion from the bus monitor, or a show

cycle). DS can be used to latch data for a bus analyzer. It can also aid in following the external bus pipeline.

Timing Comments Assertion — Occurs after the chip-select unit asserts the internal TA signal or the bus monitor timer asserts the internal TEA signal. DS is also asserted at the end of a show cycle.

2.5.4 Development Support Signals

2.5.4.1 Development Port Serial Data Out (DSDO)

Output only
Module: Development support

State Meaning Asserted/Negated — Indicates the logic level of data being shifted out of the development port shift register.

Timing Comments Transitions are relative to CLKOUT in self-clocked mode and relative to DSCK in clocked mode. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for more information.

2.5.4.2 Development Port Serial Data In (DSDI)

Input only
Module: Development support

State Meaning Asserted/Negated — Indicates the logic level of data being shifted into the development port shift register.

Reset Operation During reset, this pin functions as a reset configuration mode pin. If the pin is pulled high while the MCU asserts RESETOUT, the data bus pins are used to configure the system when the reset state is exited. If the pin is low at the positive edge of RESETOUT, then the system is configured by the internal default mode. Refer to **5.8.3 Configuration During Reset** for more information on reset operation.

Timing Comments Transitions are relative to CLKOUT in self-clocked mode and relative to DSCK in clocked mode. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for more information.

2.5.4.3 Development Port Serial Clock Input (DSCK)

Input only
Module: Development support

State Meaning Asserted/Negated — Provides a clock signal for shifting data into or out of development serial port.

Reset Operation During reset, this pin functions as a debug mode enable pin. If the pin is pulled high while the MCU asserts RE-

$\overline{\text{SETOUT}}$, debug mode is enabled when the reset state is exited. For normal operation, this pin should be pulled to ground through a resistor. Refer to **5.8.3 Configuration During Reset** for more information.

Timing Comments Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for detailed timing information.

2.5.4.4 Instruction Fetch Visibility Signals (VF[0:2])

Output only
Module: Development support

State Meaning Asserted/Negated — Denote the last fetched instruction or the number of instructions that were flushed from the instruction queue. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for details.

Timing Comments Assertion/Negation — Transitions may occur every clock cycle. This signal is not synchronous with bus cycles. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for more information on these signals.

2.5.4.5 Instruction Flush Count (VFLS[0:1])

Output only
Module: Development support

State Meaning Asserted/Negated — Denote the number of instructions that are flushed from the history buffer during the current clock cycle. These signals also provide the freeze indication. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for details.

Timing Comments Assertion/Negation — Transitions may occur every clock cycle. This signal is not synchronous with bus cycles. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for more information on these signals.

2.5.4.6 Watchpoints (WP[0:5])

Output only
Module: Development support

State Meaning Asserted — Indicate that a watchpoint event has occurred on the I-bus (WP[0:3]) or L-bus (WP[4:5]).

Negated — Indicate that no watchpoint event has occurred.

Timing Comments Assertion/Negation — Transitions may occur every clock cycle. This signal is not synchronous with bus cycles. Refer to the ***RCPU Reference Manual*** (RCPURM/AD) for more

information on these signals.

2.5.5 Chip-Select Signals

2.5.5.1 Chip Select for System Boot Memory ($\overline{\text{CSBOOT}}$)

Input only
Module: Chip selects

State Meaning Asserted — Indicates the boot memory device is being selected. In systems that have no external boot device, this pin can be configured as a write enable or output enable of an external memory device. At power up, this pin defaults as a chip enable of the boot device.

Negated — Indicates the boot device is not being selected.

Timing Comments Assertion/Negation — This is an address phase signal when used as chip enable of the boot device, or a data phase signal when used as output enable or write enable of an external memory device. When this signal is a chip enable, assertion may be delayed from the assertion of $\overline{\text{TS}}$.

2.5.5.2 Chip Selects for External Memory ($\overline{\text{CS[0:11]}}$)

Output only
Module: Chip selects

State Meaning Asserted — Indicates that the memory region for which the chip select is programmed is being accessed. $\overline{\text{CS}}$[1:5] can be programmed as chip enables, output enables, or write enables. $\overline{\text{CS0}}$ and $\overline{\text{CS}}$[6:11] can be programmed as output enables or write enables.

Negated — Indicates that the memory region for which the chip select is programmed is not being accessed.

Timing Comments Assertion/Negation — These are address phase signals when used as chip enables ($\overline{\text{CS}}$[1:5] only), or data phase signals when used as output enables or write enables. When these signals are chip enables, assertion may be delayed from the assertion of $\overline{\text{TS}}$.

2.5.6 Clock Signals

2.5.6.1 Clock Output (CLKOUT)

Output only
Module: Clocks

State Meaning Asserted/Negated — Provides a clock which runs continuously. All signals driven on the E-bus must be synchronized

to the rising edge of this clock.

2.5.6.2 Engineering Clock Output (ECROUT)

Output only
Module: Clocks

State Meaning Asserted/Negated — Provides a buffered clock reference output with a frequency equal to the crystal oscillator frequency, taken from the PLL feedback signal.

2.5.6.3 Crystal Oscillator Connections (EXTAL, XTAL)

Input, Output
Module: EBI

State Meaning Connections for the external crystal to the internal oscillator circuit. An external oscillator should serve as input to the EXTAL pin, when used.

2.5.6.4 External Filter Capacitor Pins (XFCP, XFCN)

Input only
Module: EBI

State Meaning Used to add an external capacitor to the filter circuit of the phase-locked loop.

2.5.6.5 Clock Mode (MODCLK)

Input only
Module: EBI

Reset Operation During reset, this signal and V_{DDSN} select the source of the system clock. Refer to **5.8.3 Configuration During Reset** for details.

2.5.6.6 Phase-Locked Loop Lock Signal (PLLL)

Output only
Module: Clocks

State Meaning Asserted — Indicates that the phase-locked loop is locked.

Negated — Indicates that the phase-locked loop is not locked.

2.5.6.7 Power-Down Wake-Up (PDWU)

Output only
Module: EBI

State Meaning Asserted — Can be used as power-down wakeup to external power-on reset circuit, or assertion can signal other events depending on system requirements. PDWU is as-

serted when bit 0 of the decrementer register changes from zero to one and can also be asserted by software. See the ***RCPU Reference Manual*** (RCPURM/AD) for details on decrementer exceptions.

Negated — (By software) indicates the event causing assertion of PDWU is not or is no longer occurring.

Timing Comments Negation — Does not occur until at least one decrementer clock following assertion.

2.5.7 Reset Signals

The $\overline{\text{RESET}}$ and $\overline{\text{RESETOUT}}$ signals are used while the part is being placed into or coming out of reset. Refer to **5.8 Reset Operation** for more details on these pins.

2.5.7.1 Reset ($\overline{\text{RESET}}$)

Input only
Module: Reset

State Meaning Asserted — Indicates that devices on the bus must reset.

Negated — Indicates normal operation.

Timing Comments For timing information, refer to **5.8 Reset Operation**.

2.5.7.2 Reset Output ($\overline{\text{RESETOUT}}$)

Output only
Module: Reset

State Meaning Asserted — (During reset) instructs all devices monitoring this signal to reset all parts within themselves that can be reset by software. Assertion indicates that the MCU is in reset.

Negated — Indicates normal operation.

Timing Comments For timing information, refer to **5.8 Reset Operation**.

2.5.8 SIU General-Purpose Input/Output Signals

Many of the pins associated with the SIU can be used for more than one function. The primary function of these pins is to provide an external bus interface. When not used for their primary function, many of these pins can be used for digital I/O. Refer to **5.9 General-Purpose I/O** for more information on these signals.

2.5.8.1 Ports A and B (PA[0:7], PB[0:7])

Output only
Module: Ports

State Meaning Asserted/Negated — Indicates the logic level of the data being transmitted. Port A and port B share a data register

(PORTA/PORTB) and pin assignment register (PAPAR/PBPAR).

Timing Comments Assertion/Negation — Accesses to these ports require three clock cycles, the same as for external accesses to port replacement logic if a port replacement unit (PRU) is used.

2.5.8.2 Ports I, J, K, and L (PI[0:7], PJ[0:7], PK[0:7], PL[2:7]

Input/Output
Module: Ports

State Meaning Asserted/Negated — Indicates the logic level of the data being transmitted. Ports I, J, K, and L share a data register (PORTI, PORTJ, PORTK, PORTL), data direction register (DDRI, DDRJ, DDRK, DDRL), and pin assignment register (PIPAR, PJPAR, PKPAR, PLPAR).

Timing Comments Assertion/Negation — Accesses to these ports require three clock cycles, the same as for external accesses to port replacement logic if a port replacement unit (PRU) is used.

2.5.8.3 Port M (PM[3:7])

Input/Output
Module: EBI

State Meaning Asserted/Negated — Indicates the logic level of the data being transmitted.

Timing Comments Assertion/Negation — Accesses to port M require two clock cycles.

2.5.9 Interrupts and Port Q Signals

The MPC509 contains seven external interrupt pins. These pins are grouped into a general-purpose port (port Q). When not used as interrupt inputs, any of these pins can be used for digital input or output. Refer to **SECTION 6 PERIPHERAL CONTROL UNIT** for more information on these pins.

2.5.9.1 Interrupt Requests ($\overline{\text{IRQ[0:6]}}$)

Input only
Module: EBI

State Meaning Asserted — Indicates an external interrupt is being requested with a request level corresponding to the $\overline{\text{IRQ}}$ number of the pin.

Negated — Indicates no external interrupt when the indicat-

ed level is being requested.

2.5.9.2 Port Q (PQ[0:6])

Input/Output
Module: PCU

State Meaning	Asserted/Negated — Indicates the logic level of the data being transmitted.
Timing Comments	Assertion/Negation — Accesses to port Q require two clock cycles.

2.5.10 JTAG Interface Signals

Refer to **SECTION 9 IEEE 1149.1-COMPLIANT INTERFACE** for more information on these pins.

2.5.10.1 Test Data Input (TDI)

Input only
Module: JTAG

State Meaning	Asserted/Negated — Represents the value of the test data input.
Timing Comments	Sampled on the rising edge of TCK.

2.5.10.2 Test Data Output (TDO)

Output only
Module: JTAG

State Meaning	Asserted/Negated — Represents the value of the test data output.
Timing Comments	Changes on the falling edge of TCK.

2.5.10.3 Test Mode Select (TMS)

Input only
Module: JTAG

State Meaning	Asserted/Negated — Sequences the test controller’s state machine.
Timing Comments	Sampled on the rising edge of TCK.

2.5.10.4 Test Clock (TCK)

Input only
Module: JTAG

State Meaning	Test clock input to synchronize the test logic.

2.5.10.5 Test Reset ($\overline{\text{TRST}}$)

Input only
Module: JTAG

State Meaning	Asserted — Signals TAP controller to reset itself.
Timing Comments	Asynchronous.