



APPENDIX B REGISTER GENERAL INDEX

–A–

Associated registers 10-4

–B–

BAR (breakpoint address register) 22-45
BBCMCR BBC module configuration register 4-25
BR0 (BR3 - memory controller base registers 0 - 3) 10-29
Breakpoint address register (BAR) 22-45
Breakpoint counter A value and control register (COUNTA) 22-50
Breakpoint counter B value and control register (COUNTB) 22-51

–C–

CALRAM_OTR CALRAM ownership trace register 21-21
CANCTRL0 (control register 0) 16-25
CANCTRL1 (control register 1) 16-26
CANCTRL2 (control register 2) 16-28
CANICR (TouCAN interrupt configuration register) 16-24
CANMCR (TouCAN module configuration register) 16-22
CFSR0 (TPU3 channel function select register 0) 18-17
CFSR1 (TPU3 channel function select register 1) 18-17
CFSR2 (TPU3 channel function select register 2) 18-17
CFSR3 (TPU3 channel function select register 3) 18-17
CIER (TPU3 channel interrupt enable register) 18-16
CISR (TPU3 channel interrupt status register) 18-20
CMPA-CMPD (comparator A-D value register) 22-44
CMPE-CMPF (comparator E-F value registers) 22-45
CMPG-CMPH (comparator G-H value registers) 22-45
COLIR
 change of lock interrupt register 8-36
COLIR (change of lock register) 8-36
Comparator A-D value registers (CMPA-CMPD) 22-44
Comparator E-F value registers (CMPE-CMPF) 22-45
Comparator G-H value registers (CMPG-CMPH) 22-45
control register (QACR1) 13-18
COUNTA (breakpoint counter A value and control register) 22-50
COUNTB (breakpoint counter B value and control register) 22-51
CPR0 (TPU3 channel priority register 0) 18-19
CPR1 (TPU3 channel priority register 1) 18-20
CR (condition register) 3-16
CRAM_RBAX CALRAM region base address register 21-18, 21-19
CRAMMCR CALRAM module configuration register 6-36, 8-30, 21-15, 21-16
CRAMOV L CALRAM overlay configuration register 21-20
CTR (count register) 3-19

–D–

DAR (data address register) 3-22
DCCR0-DCCR15 decompressor class configuration registers 4-32
DDRQS (PORTQS data direction register) 14-14



Debug enable register (DER) 22-53
DEC (decrementer register) 3-24, 6-39
Decrementer register (DEC) 6-39
DER (debug enable register) 22-53
Development port data register (DPDR) 22-55
DLCMD2 command register (CMD) 15-35, 15-36
DLCMD2 interrupt level register (ILR) 15-31, 15-32
DLCMD2 interrupt pending register (IPR) 15-30
DLCMD2 interrupt vector register (IVR) 15-32
DLCMD2 module configuration register (MCR) 15-27
DLCMD2 receive data register (RDATA) 15-34, 15-44
DLCMD2 status register (STAT) 15-41
DLCMD2 symbol timing control and pre-scaler register (SCTL) 15-32
DLCMD2 test configuration register (TCR) 15-58
DLCMD2 transmit data register (TDATA) 15-40
DMBR (dual mapping base register) 10-33
DMOR (dual mapping option register) 10-34
DPTMCR (DPTRAM module configuration register) 19-4
DPTRAM
 module configuration register (DPTMCR) 19-4
 ram base address register (RAMBAR) 19-5
 test register 19-5
DSCR (TPU3 development support control register) 18-13
DSISR (dae/source instruction service register) 3-22
DSSR (TPU3 development support status register) 18-15
Dual mapping base register (DMBR) 10-33
Dual mapping option register 10-34

–E–

ECR (exception cause register) 22-52
EIBADR external interrupt relocation table base address register 4-31
EMCR (external master control register) 6-29
ESTAT (error and status register) 16-30
Exception cause register (ECR) 22-51
External master control register (EMCR) 6-29

–F–

FASRAM module test register (FTEST) 17-42
FPRs - (floating-point registers) 3-12
FPSCR (floating-point status and control register) 3-13

–G–

General-Purpose I/O registers 6-45
GPRs (general-purpose registers) 3-12

–H–

HSQR0 (TPU3 host sequence register 0) 18-18
HSQR1 (TPU3 host sequence register 1) 18-18
HSSR0 (TPU3 host service request register 0) 18-19
HSSR1 (TPU3 host service request register 1) 18-19

–I–

I-Bus support control register (ICTRL) 22-46
ICTRL (i-bus support control register) 22-46
IFLAG (interrupt flag register) 16-33
IMASK (interrupt mask register) 16-32
IMMR (internal memory mapping register) 6-28

Internal memory map register 6-28

–K–

Keep alive power registers lock mechanism 8-24

–L–

L2U

- global region attribute register (L2U_GRA) 11-16
- module configuration register (L2U_MCR) 11-13
- region attribute registers (L2U_RAx) 11-15
- region base address registers (L2U_RBAX) 11-14
- L2U_GRA (L2U global region attribute register) 11-16
- L2U_MCR (L2U module configuration register) 11-14
- L2U_RAx (L2U region X attribute register) 11-15
- L2U_RBAX (L2U region x base address register) 11-14
- L-Bus support control register 1 (LCTRL1) 22-48
- L-Bus support control register 2 (LCTRL2) 22-49
- LCTRL1 (l-bus support control register 1) 22-48
- LCTRL2 (l-bus support control register 2) 22-49
- LR (link register) 3-19

–M–

- MCPSMCR MCPSM status/control register 17-36
- MDASMAR MDASM DataA register 17-60
- MDASMBR MDASM DataB register 17-61
- MDASMSCR MDASM status/control register 17-62
- Memory controller base registers (BR0 - BR3) 10-29
- Memory controller option registers (OR0 - OR3) 10-31
- Memory controller status registers (MSTAT) 10-29
- MI_GRA Global region attribute register 4-29
- MI_GRA Global region attribute register 4-29
- MIOS14ER0 interrupt enable register 17-27
- MIOS14ER1 interrupt enable register 17-29
- MIOS14LVL0 interrupt register 17-30
- MIOS14LVL1 register 17-30
- MIOS14MCR module configuration register 17-33, 17-34
- MIOS14RPR0 request pending register 17-28
- MIOS14RPR1 request pending register 17-29
- MIOS14SR0 interrupt status register 17-27, 23-8
- MIOS14SR1 interrupt status register 17-28
- MIOS14TPCR test and pin control register 17-32
- MIOS14VECT vector register 17-33
- MIOS14VNR module-version number register 17-33
- MISCNT (MISC counter) 19-6, 20-7, 20-10, 20-13
- MISRH (multiple input signature register high) 19-6
- MISRL (multiple input signature register low) 19-6
- MMCSMCNT MMCSM up-counter register 17-42
- MMCSMMLL MMCSM modulus latch register 17-42
- MMCSMSCR MMCSM status/control register 17-43
- MPIOSMDDR MPIO SM data direction register 17-82
- MPIOSMDR MPIO SM data register 17-82
- MPWMCNTR MPWMSM counter register 17-76
- MPWMPERR MPWMSM period register 17-74, 17-75
- MPWMPULR MPWMSM pulse width register 17-75
- MPWMSCR MPWMSM status/control register 17-76, 17-77
- MRTCPMR MRTCSM prescaler counter buffer register 17-93
- MRTCSMFRCH MRTCSM 32-bit counter high buffer register 17-92
- MRTCSMFRCL MRTCSM 32-bit counter low buffer register 17-93



MRTCSMSCR MRTCSM status/control register 17-93
MSR (machine state register) 3-20
MSTAT (memory controller status register) 10-29



–O–

OR0 (OR3 - memory controller option registers 0 - 3) 10-31

–P–

PDMCR pads module configuration register 2-3, 2-4
PDMCR2 pads module configuration register 2-5
Periodic interrupt status and control register (PISCR) 6-43
Periodic interrupt timer count register (PITC) 6-43
Periodic interrupt timer register (PITR) 6-44
PISCR (periodic interrupt status and control register) 6-43
PITC (periodic interrupt timer count) 6-43
PITR (periodic interrupt timer register) 6-44
PLL,
 low power, and reset control register (PLPRCR) 8-33
PLPRCR (PLL, low power, and reset control register) 8-34
port data direction registers 13-15
port data registers 13-15
PORTQS (port QS data register) 14-12
PQSPAR (PORTQS pin assignment register) 14-13
PRESDIV (prescaler divide register) 16-27
PVR (processor version register) 3-26

–Q–

QADC64E control register 0 (QACR0) 13-16
QADC64E control register 1 (QACR1) 13-18
QADC64E control register 2 (QACR2) 13-20
QADC64E conversion command word table (CCW) 13-33
QADC64E left justified, signed result format (LJSRR) 13-37
QADC64E left justified, unsigned result format (LJURR) 13-37
QADC64E port A data direction registers (DDRQA) 13-16
QADC64E port A data register (PORTQA) 13-15
QADC64E port B data direction register (DDRQB) 13-16
QADC64E port B data registers (PORTQB) 13-15
QADC64E right justified, unsigned result format (RJURR) 13-37
QADC64E status register 0 (QASR0) 13-23
QADC64E status register 1 (QASR1) 13-29
QADCINT-QADC64E interrupt register (with IACK(C)/with ILBS(D) QADCINT 13-13, 13-14
QDSCI_IL (QSM2 dual SCI interrupt level register) 14-9
QSCI1CR (QSCI1 control register) 14-60
QSCI1SR (QSCI1 status register) 14-62
QSMCM
 configuration register (QMCMMCR) 14-9
 interrupt level registers (QDSCI_IL, QSPI_IL) 14-9
 port QS data register (PORTQS) 14-11
 PORTQS data direction register (DDRQS) 14-13
 PORTQS pin assignment register (PQSPAR) 14-12
 QSCI1 control register (QSCI1CR) 14-60
 QSCI1 status register (QSCI1SR) 14-62
 QSPI command RAM (CRx) 14-23
 QSPI control register 0 (SPCR0) 14-17
 QSPI control register 1 (SPCR1) 14-19
 QSPI control register 2 (SPCR2) 14-20
 QSPI control register 3 (SPCR3) 14-20
 QSPI registers 14-16



QSPI status register (SPSR) 14-21
queued SCI1 status and control registers 14-60
SCI control register 0 (SCCxR0) 14-46
SCI control register 1 (SCCxR1) 14-46
SCI data register (SCxDR) 14-50
SCI registers 14-45
SCI status register (SCxSR) 14-48
test register (QTEST) 14-9
QSMCMCR (QSMCM module configuration register) 14-9
QSPI_IL (QSPI interrupt level register) 14-10

–R–

RAMBAR (ram array base address register) 19-5

RCPU

additional implementation-specific registers 3-27
condition register (CR) 3-15
condition register CR0 field definition 3-16
condition register CR1 field definition 3-16
condition register crn field - compare instruction 3-17
count register (CTR) 3-19
dae/source instruction service register (DSISR) 3-22
data address register (DAR) 3-22
decrementer register (DEC) 3-23
EIE, EID, and NRI special-purpose registers 3-26
floating-point exception cause register (FPECR) 3-26
floating-point registers (FPRs) 3-12
floating-point status and control register (FPSCR) 3-12
general special-purpose registers (SPRG0-SPRG3) 3-25
general-purpose registers (GPRs) 3-12
implementation-specific special-purpose registers 3-26
integer exception register (XER) 3-17
link register (LR) 3-18
machine state register (MSR) 3-20
machine status save/restore register 0 (SRR0) 3-24
machine status save/restore register 1 (SRR1) 3-24
powerpc OEA register set 3-20
powerpc UISA register set 3-11
powerpc VEA register set - time base 3-19
processor version register (PVR) 3-25
READI data trace attributes 1 and 2 register 23-16
READI development control register 23-10
READI device ID register 23-9
READI DID 23-9, 23-10
READI DTA 1 and 2 23-16
READI read/write access register 23-13
READI RWA 23-13
READI UBA 23-11, 23-12, 23-15
READI user base access register 23-11, 23-12, 23-15
READI user base address register 23-11, 23-12, 23-15
READI_OTR READI ownership trace register 23-8
Real-Time clock alarm register (RTCAL) 6-42
Real-Time clock register (RTC) 6-42
Real-Time clock status and control register (RTCSC) 6-41
Region attribute registers (0 - 3) 4-27
Region base address registers (0 - 3) 4-27
Register descriptions
SIUMCR SIU module configuration register 6-25
Reset status register (RSR) 7-5
RSR (reset status register) 7-5
RTC (real time clock alarm register) 6-42



RTC (real time clock register) 6-42
RTCS (real time clock status and control register) 6-41
RXECTR (receive error counter) 16-33
RXGMSKHI (receive global mask register high) 16-29

–S–

SCCxR0 (QSMCM SCI control register 0) 14-46
SCCxR1 (QSMCM SCI control register 1) 14-47
SCDR (QSMCM SCI data register) 14-50
SCxSR (QSMCM SCIx status register) 14-48
SGPIO
 control register (SGPIOCR) 6-46
 data register 1 (SGPIODT1) 6-45
 data register 2 (SGPIODT2) 6-45
SGPIOCR (SGPIO control register) 6-46
SGPIODT1 (SGPIO data register 1) 6-45
SGPIODT2 (SGPIO data register 2) 6-45
SIEL (SIU interrupt edge level register) 6-34
SIMASK (SIU interrupt mask register) 6-32, 6-33
SIPEND (SIU interrupt pending register) 6-31, 6-32
SIU
 interrupt edge level register (SIEL) 6-33
 interrupt mask register (SIMASK) 6-32
 interrupt registers 6-30
 interrupt vector register (SIVEC) 6-34
SIUMCR SIU module configuration register 6-25
SIVEC (SIU interrupt vector) 6-34
Software service register (SWSR) 6-37
SPCR0 (QSPI control register 0) 14-18
SPCR1 (QSPI control register 1) 14-19
SPCR2 (QSPI control register 2) 14-20
SPCR3 (QSPI control register) 14-21
SPRG0-SPRG3 (general special-purpose registers 0-3) 3-25
SPSR (QSPI status register) 14-21
SRR0 (machine status save/restore register 0) 3-24
SRR1 (machine status save/restore register 1) 3-25
status register (QASR) 13-23
SWSR (software service register) 6-38
SYPCR (system protection control register) 6-37
System clock control register (SCCR) 8-29
System configuration and protection registers 6-24
System configuration registers 6-25
System protection control register (SYPCR) 6-36
System protection registers 6-36
System timer registers 6-39

–T–

TB (time base) 3-19, 3-23, 6-40
TBREF0 (time base reference register 0) 6-40
TBREF1 (time base reference register 1) 6-40
TBSCR (time base control and status register) 6-41
TESR (transfer error status register) 6-38
TICR (TPU3 interrupt configuration register) 18-15
Time base control and status register (TBSCR) 6-40
Time base reference registers (TBREF0) 6-40
TIMER (free running timer register) 16-29
TouCAN
 control register 0 (CANCTRL0) 16-25
 control register 1 (CANCTRL1) 16-26



control register 2 (CANCTRL2) 16-28
error and status register (ESTAT) 16-30
interrupt configuration register (CANICR) 16-24
interrupt flag register (IFLAG) 16-33
interrupt mask register (IMASK) 16-32
module configuration register (CANMCR) 16-22
prescaler divide register (PRESDIV) 16-27
receive buffer 14 mask registers 16-30
receive buffer 15 mask registers 16-30
receive global mask registers (RXGMSKHI) 16-29
receive mask registers 16-7
test configuration register 16-24

TPU3

channel function select registers (CFSRx) 18-16
channel interrupt enable register (CIER) 18-16
channel interrupt status register (CISR) 18-20
channel priority registers (CPRx) 18-19
decoded channel number register (DCNR) 18-21
development support control register (DSCR) 18-13
development support status register (DSSR) 18-15
host sequence registers (HSQRx) 18-18
host service request registers (HSSRx) 18-18
interrupt configuration register (TICR) 18-15
link register (LR) 18-21
module configuration register (TPUMCR) 18-11
module configuration register 2 (TPUMCR2) 18-21
module configuration register 3 (TPUMCR3) 18-23
service grant latch register (SGLR) 18-21
test configuration register (TCR) 18-13
test registers (ISDR, ISCR) 18-23

TPUMCR (TPU3 module configuration register) 18-11

TPUMCR2 (TPU3 module configuration register 2) 18-21

TPUMCR3 (TPU3 module configuration register 3) 18-23

Transfer error status register (TESR) 6-38

–U–

UC3FCFIG (hard reset configuration word) 20-18, 20-19

UIMB

module configuration register (UMCR) 12-7
pending interrupt request register (UIPEND) 12-8
test control register (UTSTCREG) 12-8

UIPEND (UIMB pending interrupt request register) 12-8

UMCR (UIMB module configuration register) 12-7

–V–

VDDSRM

sensor register (VSRMSR) 8-36

VSRMSR (VDDSRM control register) 8-37

–X–

XER (integer exception register) 3-18

