APPENDIX E
ELECTRICAL AND AC CHARACTERISTICS

E.1 Absolute Maximum Ratings

Table E-1 Maximum Ratings (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
3.3-V Supply Voltage	V_{DDI}, V_{DD3}, $V_{DDDPTRAM}$, V_{STBY}	-0.3 to + 4.0	V
Clock Sythesizer Voltage	V_{DDSYN}	-0.3 to 4.0	V
QADC Supply Voltage	V_{DDA}	-0.3 to 6.0	V
5-V Supply Voltage	V_{DD5}	-0.3 to 6.0	V
DC Input Voltage[10]	V_{IN}	-0.3 to 5.5	V
Operating Temperature Range (Packaged)	T_A	-40 to +125	°C
Operating Temperature Range (Die Form)	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
Maximum Input Current per Pin[7,8]	I_{MAX}	1.0	mA

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
4. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except XTAL and EXTAL are internally clamped to V_{DD}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.
7. This parameter is periodically sampled rather than 100% tested
8. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.
10. All 3-V input pins are 5-V tolerant except XTAL and EXTAL.

Table E-2 Thermal Characteristics

Rating	Symbol	Value	Unit
Thermal Resistance Plastic 272-Pin Ball Grid Array	Θ_{JA}	TBD	°C/W

NOTES:

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

where

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table E-3 General DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
3V Input High Voltage [1] Except EXTAL and XTAL	V_{IH3}	2.0	V_{DD5}	V
5v Input High Voltage[2] All input pins except TPU and CTM9 TPU and CTM9 input pins	V_{IH5}	0.7 (V_{DD5}) 3.3	V_{DD5} + 0.3 V_{DD5} + 0.3	V V
3-V Input Low Voltage	V_{IL3}	V_{SS} - 0.3	0.8	V
5-V Input Low Voltage All input pins except TPU and CTM9 TPU and CTM9 input pins	V_{IL5}	V_{SS} – 0.3 V_{SS} – 0.3	0.35 (V_{DD5}) 2.3	V V
Input Hysteresis[11] All pins except TPU and CTM9 TPU and CTM9 input pins	V_{HYS}	0.5 0.3	-	V V
Mode Select Pullup/Pulldown Current	I_{ACT}	20	130	µA
Input Leakage Current[3] Pull-up/down inactive	I_{INACT}	-1.0	1.0	µA
3-V Output High Voltage (I_{OH3} = -2 mA)	V_{OH3}	2.4	-	V
5-V Output High Voltage (I_{OH5} = -2 mA)	V_{OH5}	V_{DD5} - 0.7	-	V
3-V Output Low Voltage (I_{OL3} = 3.2 mA)	V_{OL3}	-	0.5	V
5-V Output Low Voltage (I_{OL5} = 2 mA)	V_{OL5}	-	0.5	V
Clock Output Low Current CLKOUT or BCLK @ V_{OL3} = 0.5 V	I_{OL}	2.0	-	mA

Table E-3 General DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
Load for BIM 3-V Bus Output Pins, 25 MHZ[9] Partial Drive Full Drive	C_{LBIM25}	-	 40 80	pF
Load for BIM 3-V Bus Output Pins, 33 MHZ[9] Partial Drive Full Drive	C_{LBIM33}	-	 25 50	pF
Load for Visibility Bus 3-V Output Pins[9] Load for QSM 5V Output Pins[9] Primary Functions Digital Output	C_{LVB} C_{LQSM}	-	25 200 50	pF
Capacitance for Input, Output, and Bidirectional[9] V_{in} = 0V, f = 1MHz (except QADC)	C_{IN}	-	15	pF
Supply Current 25 MHZ[6,11,12] RUN LPSTOP, 10 MHz crystal, VCO Off LPSTOP (External clock input frequency = max f_{sys})	 I_{DD3} I_{DD5} I_{DDXTAL} $I_{DDEXTCK}$		 215 20 **TBD** **TBD**	mA
Supply Current 33 MHZ[6,11,12] RUN LPSTOP, 10 MHz crystal, VCO Off LPSTOP (External clock input frequency = max f_{sys})	 I_{DD3} I_{DD5} I_{DDXTAL} $I_{DDEXTCK}$		 **TBD** **TBD** **TBD** **TBD**	mA
PLL Supply Current (V_{DDSYN})[6,12] 10 MHz crystal, VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, 10 MHz crystal, VCO off (STBIM = 0) LPSTOP, 10 MHz crystal, VCO on (STBIM = 1) LPSTOP, 10 MHz crystal, VCO off (STCLKS = 1)	 I_{DDSYN} EXI_{DDSYN} SI_{DDSYNB} SI_{DDSYNV} $SI_{DDSYNST}$		 10.0 **TBD** **TBD** **TBD** **TBD**	 mA mA mA mA µA
FASRAM Standby Voltage (VSTBY)[7] Run Standby mode, $V_{DD} = V_{SS}$	V_{SB}	3.14 2.5	3.45 3.45	V
FASRAM Standby Current [6,7,10,11] Normal RAM operation$V_{DD} > V_{SB} - 0.5$ V Transient condition$V_{SB} - 0.5$ V >=V_{DD} >=V_{SS} + 0.5 V Standby operation$V_{DD} < V_{SS} + 0.5$ V	 I_{SB}	 **TBD**	 **TBD** **TBD** **TBD**	 µA mA µA
DC Injection Current per Pin, 3V/5V[3,9]	I_{IC}	-1.0	1.0	mA

NOTES:

1. This spec is for 3V outputs with 5-V tolerent input pins.
2. This spec is for 5V outputs with 5-V tolerent input pins.
3 After characterization this value may be improved.
6. Power dissipation measured at 32 Mhz or 25 Mhz system clock frequency, all modules active. Power dissipation can be calculated using the following expression: P_D = Maximum V_{DD5} (I_{DD5} + I_{DDA}) + Maximum V_{DD3} (I_{DD3} + I_{DDSYN} + I_{SB})
7. The RAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 Volt. The RAM array cannot be accessed while the module is in standby mode. V_{SB} must be applied to the RAM during normal operation.

8. Power dissipation measured at 32 Mhz or 25 Mhz system clock frequency, all modules active.
9. This parameter is periodically sampled rather than 100% tested.
10. When V_{DD} is transitioning during power-up or power down sequence, and V_{SB} is applied, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the V_{DD} and V_{STBY} pins can contribute to this condition.
11. These values are design targets, Motorola makes no commitment to achieve this level of electrical performance.
12. I_{DD3} and I_{DD5} are estimates based on average current calculations.

E.2 AC Specifications

Each timing diagram contains parameters abstracted from the timing specification tables. Pertinent notes have been included in the timing tables.

In some cases a timing parameter has been augmented based on different signal options. The user must select the appropriate parameter.

EXAMPLE

Timing parameter 9 has been augmented to include specific timing for: (9) Clock low to CS Valid (CS set to DS timing), (9A) Clock low to AS/DS Valid, and (9B) Clock low to CS Valid (CS set to CE timing).

AC timing is measured under the following conditions:

- Timing is measured between 20% V_{DD} and 70% V_{DD}.
- Temperature: T_A in normal operating range.
- Voltage: V_{DD3}, V_{DDi}, V_{STBY}, V_{DDSYN} = 3.3 V ± 5%; V_{DD5}, V_{DDA} = 5.0 V ± 5%.

Characterization of device emissions are performed per *SAE J1752/3* Issued March 1995.

E.2.1 PLL AC Timing

Table E-4 PLL Timing

(10 MHz Reference)

Num	Characteristic	Symbol	Min	Max	Unit
C1	PLL Reference Frequency Range Crystal reference External reference[10]	 $f_{ref\_crystal}$ f_{ref_ext}	 2 10	 10 32	MHz
C2	System Frequency On-Chip PLL Frequency	f_{sys}	dc 0.032	32 32	MHz
C3	Loss of Reference Frequency[2,8]	f_{lor}	1.5	3.0	% fsys
C4	Self Clocked Mode Clock Frequency[2,9]	f_{scm}	.5	32	MHz
C5	Crystal Start-up Time[2,4]	t_{cst}		20	ms
C6	PLL Lock Time[2,3,4,5]	t_{lpll}		200	µs
C7	Power-To-Lock Time[2,3,4,6] With Crystal Reference Without Crystal Reference	t_{lplk}		 21 200	 ms µs
C8	CLKOUT Period Jitter[2,3,4,5,7] Peak-to-peak Jitter Short Term Jitter (3 system clock cycles interval) Long Term Jitter (2 msec interval)	Cjitter		 3 1 .01	 % % %
C9	Duty Cycle of reference[2]	tdc	40	60	%
C10	1:1 Clock Skew (between CLKOUT and EXTAL)[10]	tskew	-2	2	ns

NOTES:

2. This parameter is periodically sampled rather than 100% tested.
3. Presently, the filter capacitor is implemented on chip, but any future application without an internal filter assumes that low-leakage external filter capacitors are attached to the XFCN and XFCP pins. Total external resistance from either of the XFCN or XFCP pins due to external leakage sources to either V_{DD} or V_{SS} must be greater than 10 MΩ to guarantee this specification.
4. Proper layout procedures must be followed to achieve specifications.
5. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR), and to the period required for the PLL to relock on exiting LP-STOP.
6. Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RESET}}$ release. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN}, V_{SS}, and variations in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.
8. Loss of reference frequency is the reference frequency detected internally which transitions the PLL into self clocked mode. Loss of reference frequency is specified as a percentage of the operating frequency, fsys.
9. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{lor} with default MFD/RFD settings.
10. PLL is operating in 1:1 PLL mode.

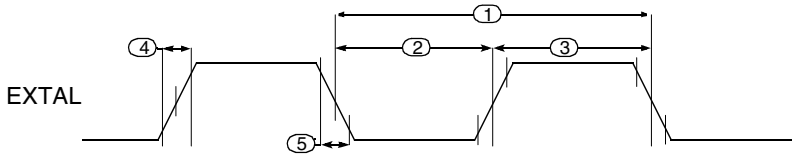


Figure E-1 External / 1:1 PLL CLOCK Input Timing

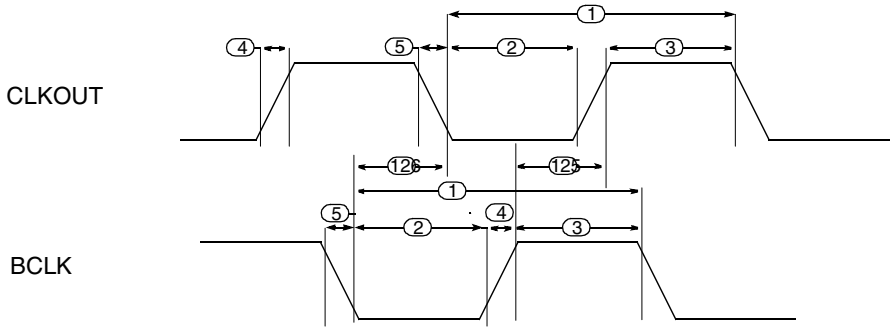


Figure E-2 CLKOUT and BCLK Output Timing

E.2.2 BIM AC Timing

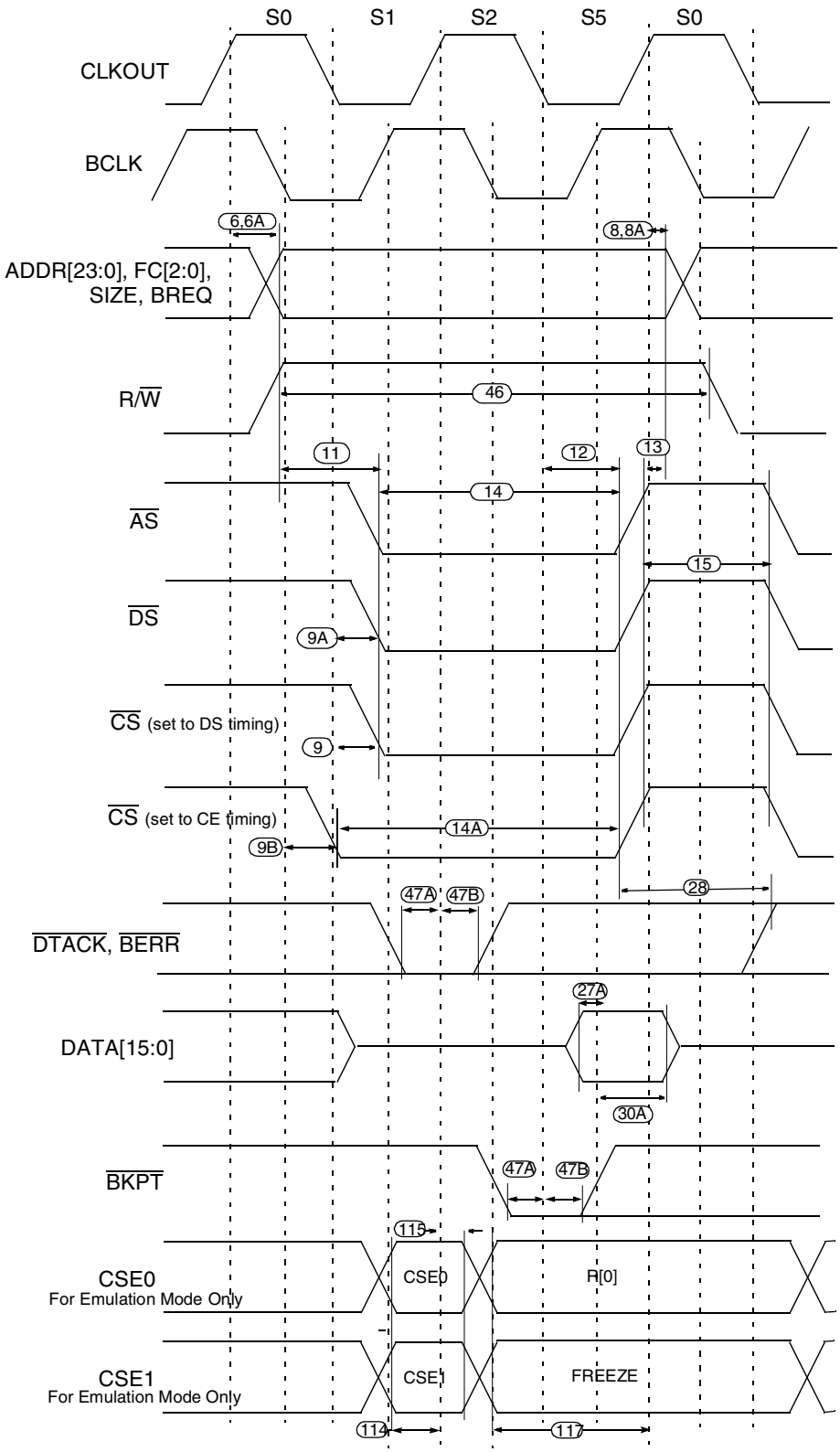
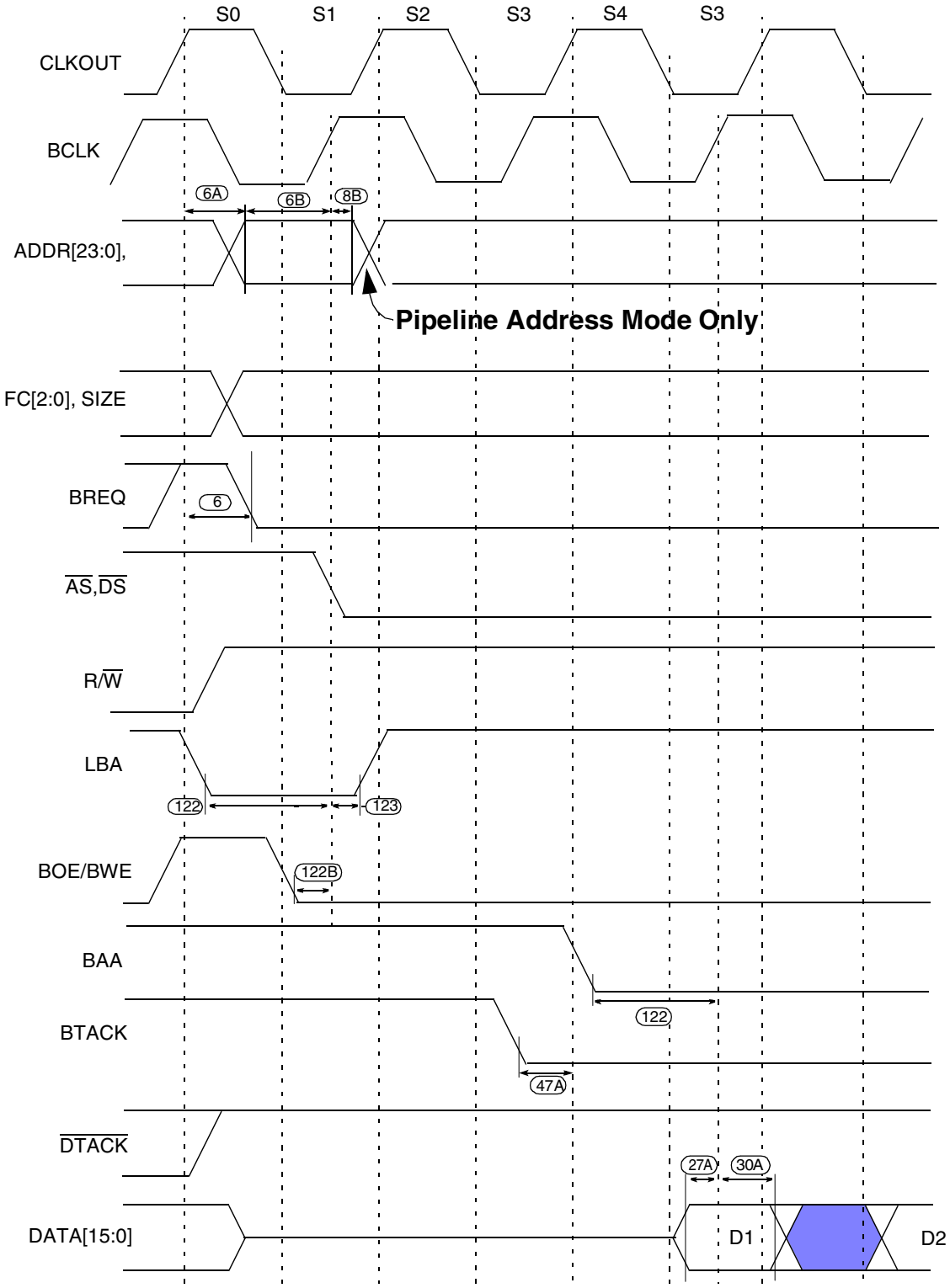


Figure E-3 Read Cycle



Note: Bus cycle is shown with HPCE asserted - LBA asserts in S0.

Figure E-4 Burst Read Cycle — Initiation

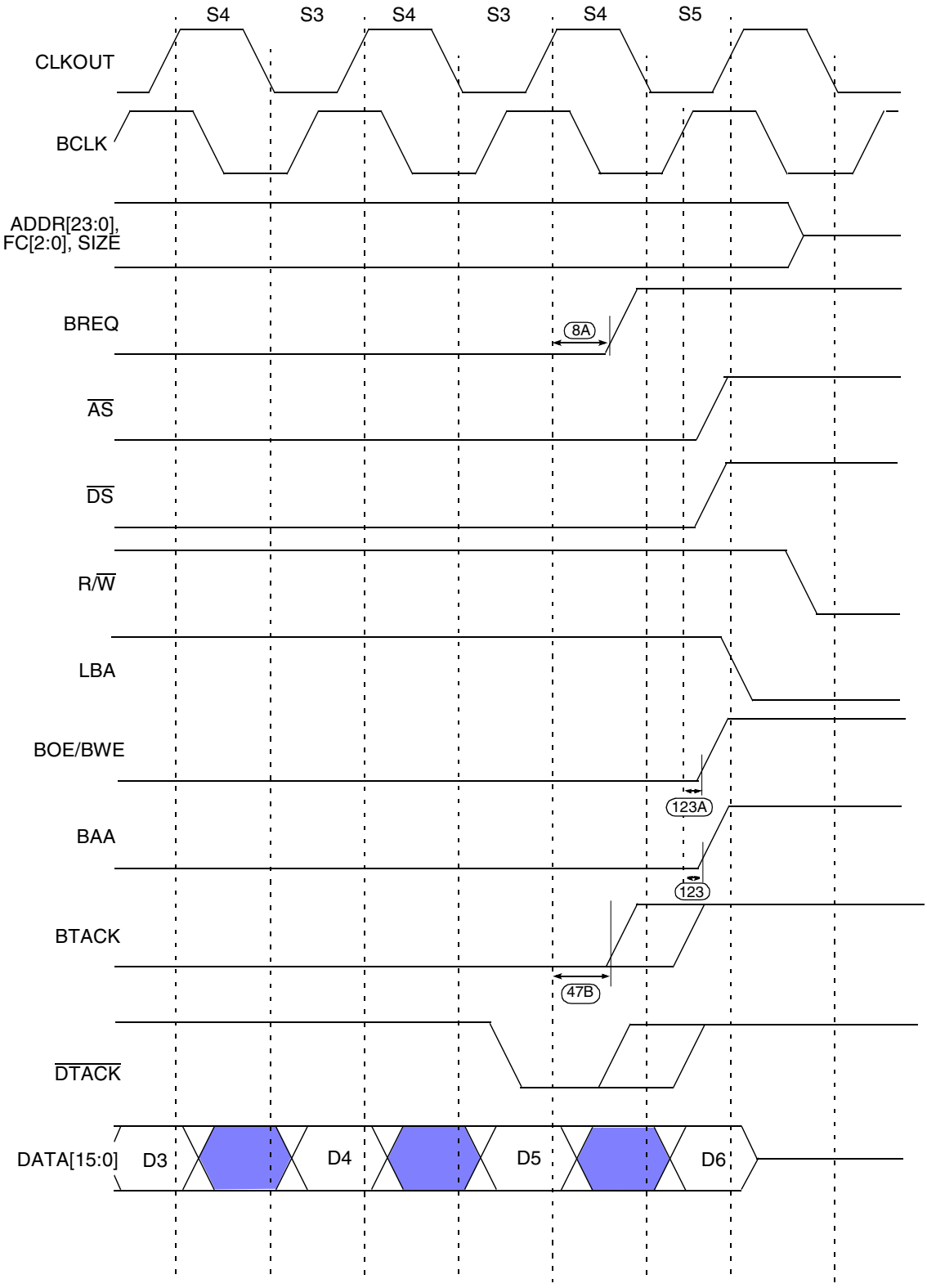


Figure E-5 Burst Read Cycle — Completion

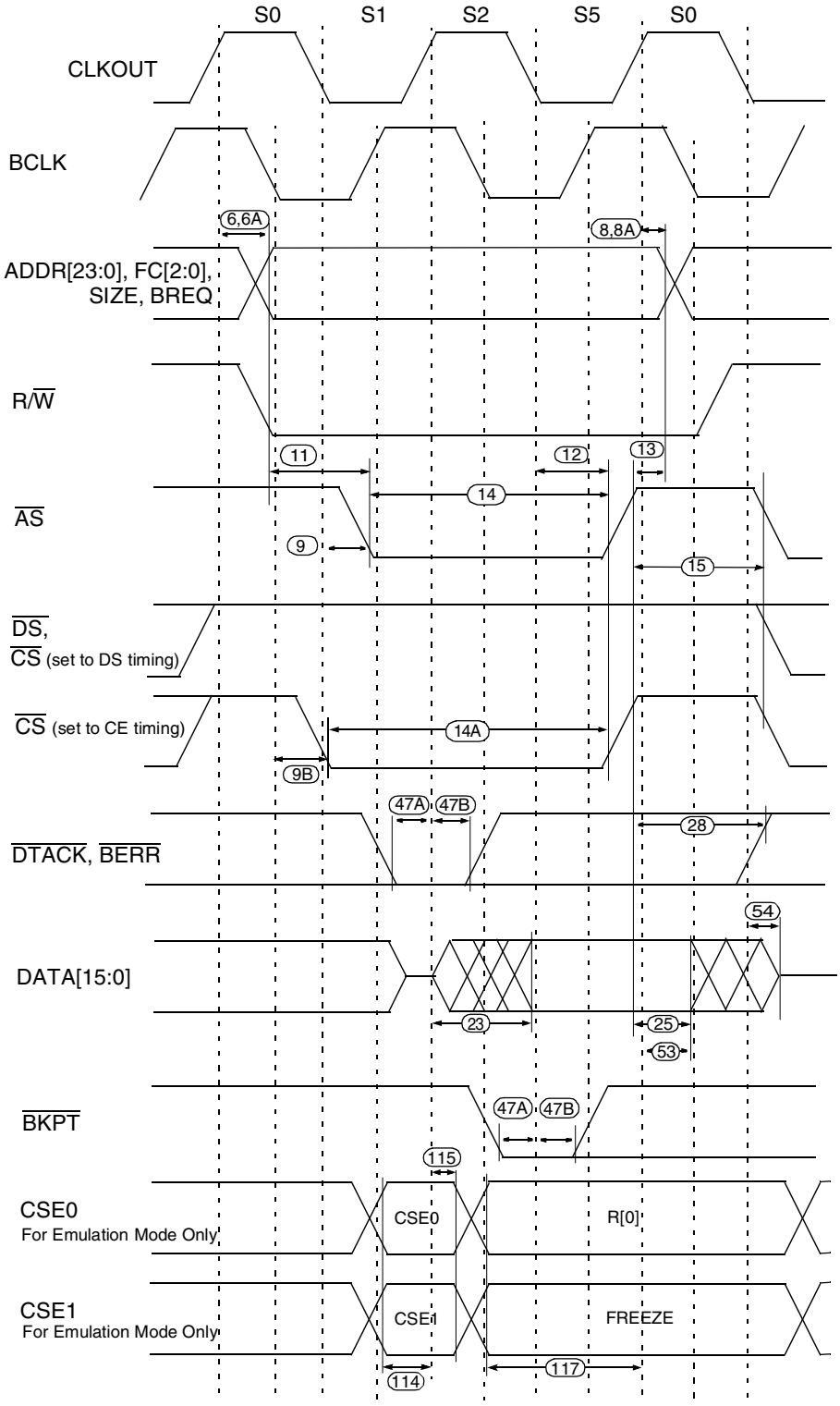


Figure E-6 Write Cycle

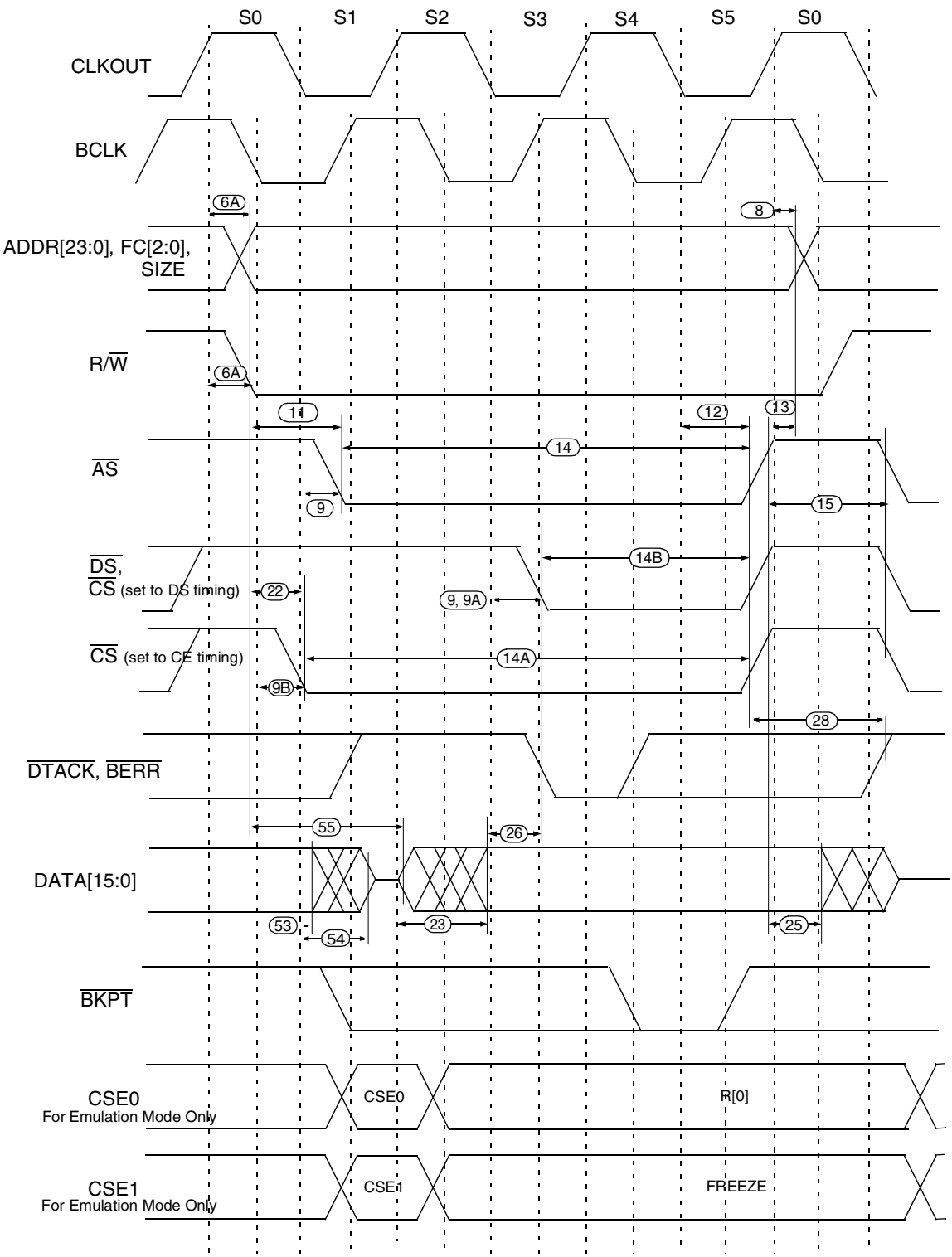
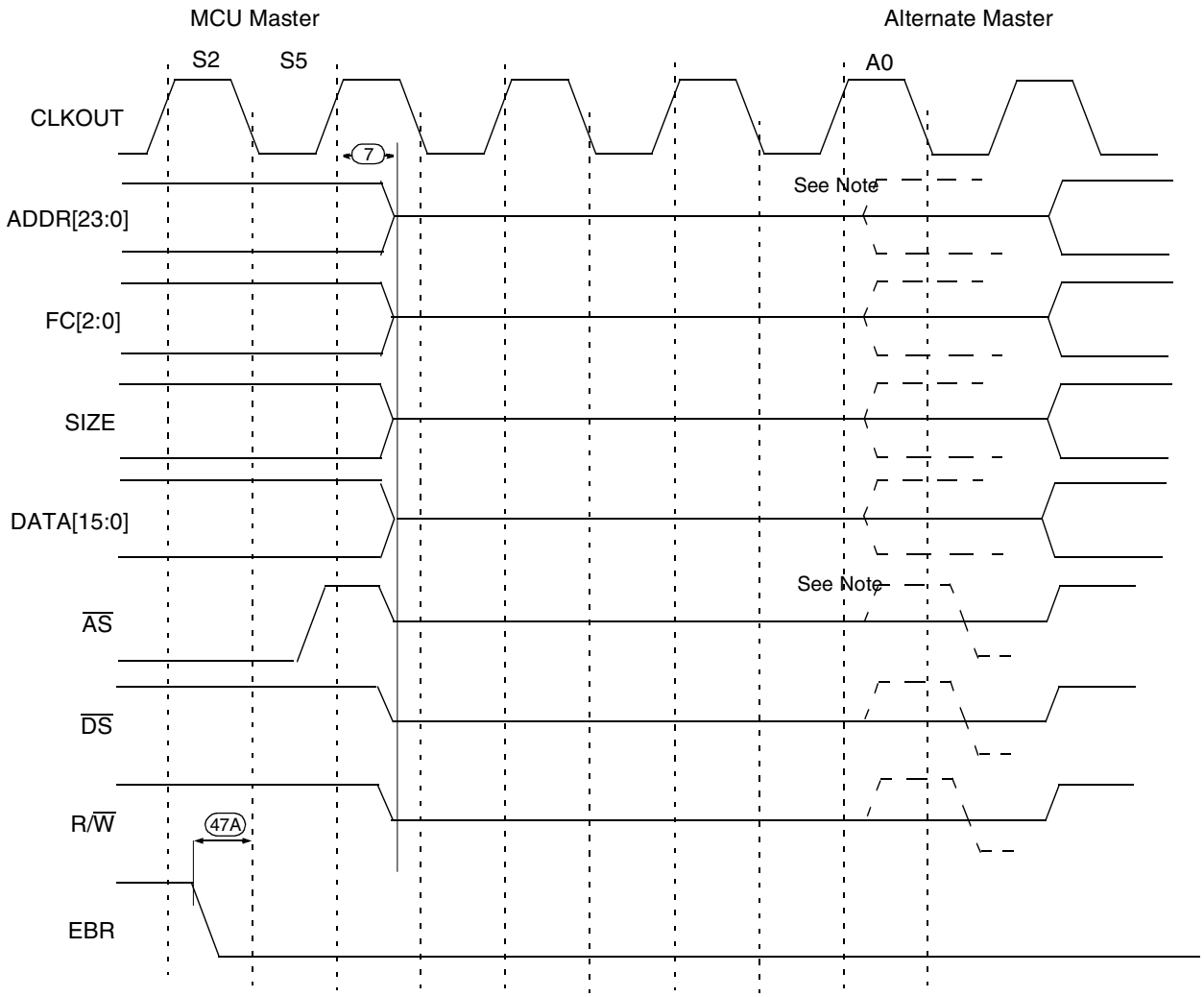


Figure E-7 Write Cycle With One Wait State



Note: The EBI may run one or more bus cycles after EBR is asserted. An external master may not start a bus cycle until the AS and DS pins have been negated for three clocks.

Figure E-8 Alternate Bus Mastership

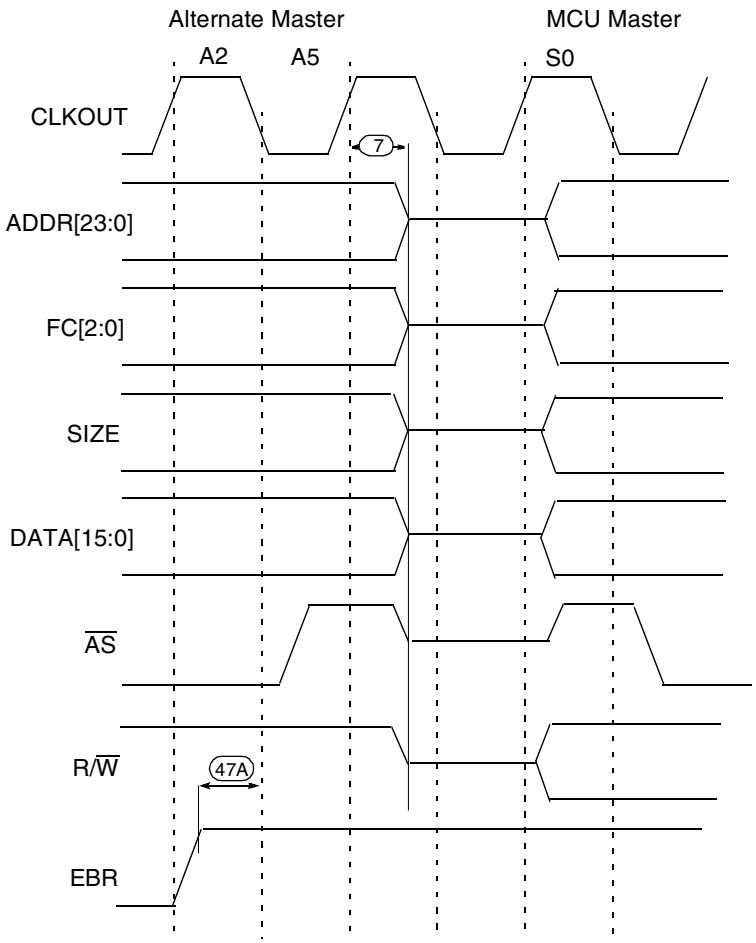
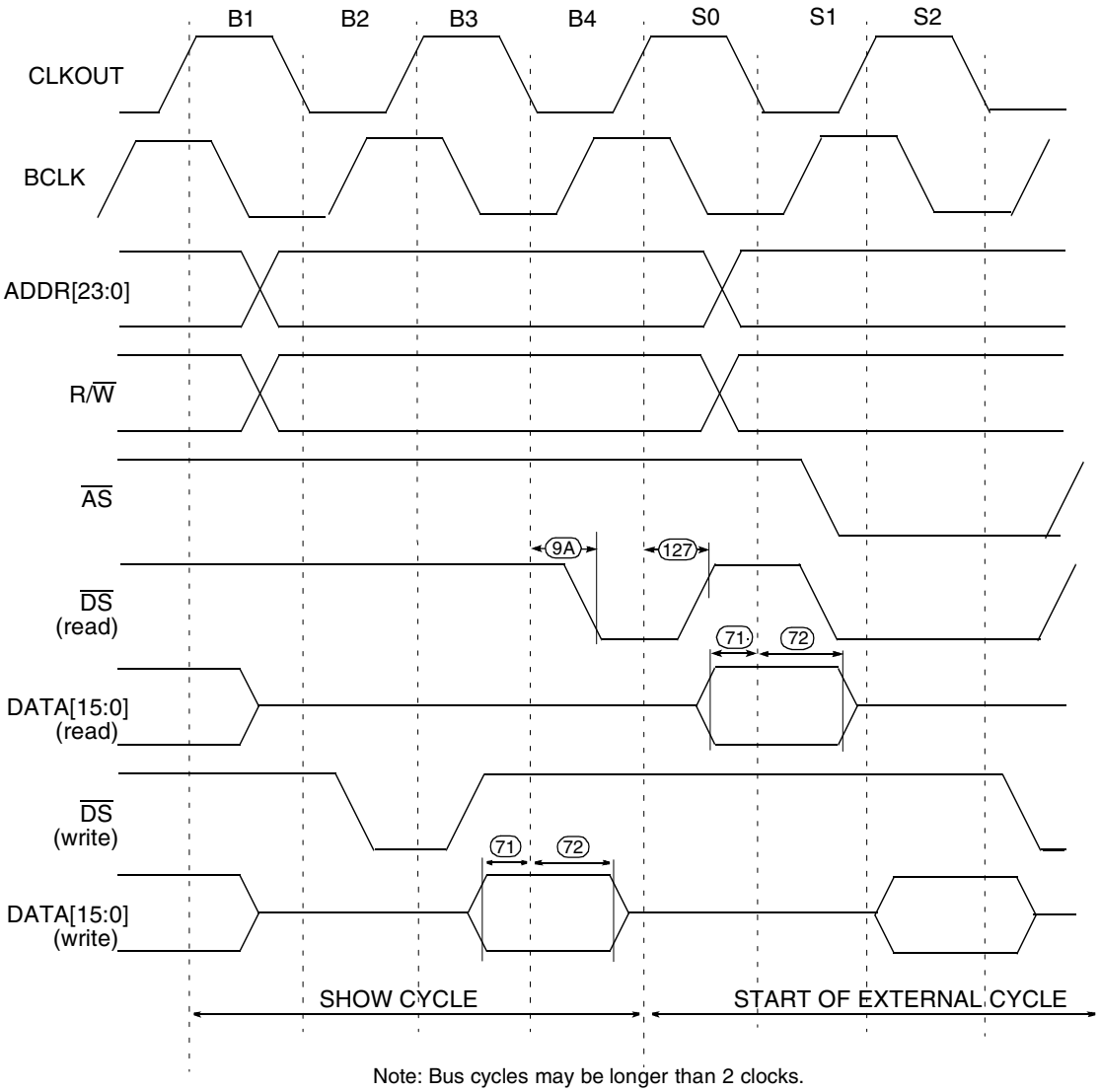


Figure E-9 EBR — Alternate Master Bus Release



Note: Bus cycles may be longer than 2 clocks.

Figure E-10 Non-Burst Show Cycle Timing

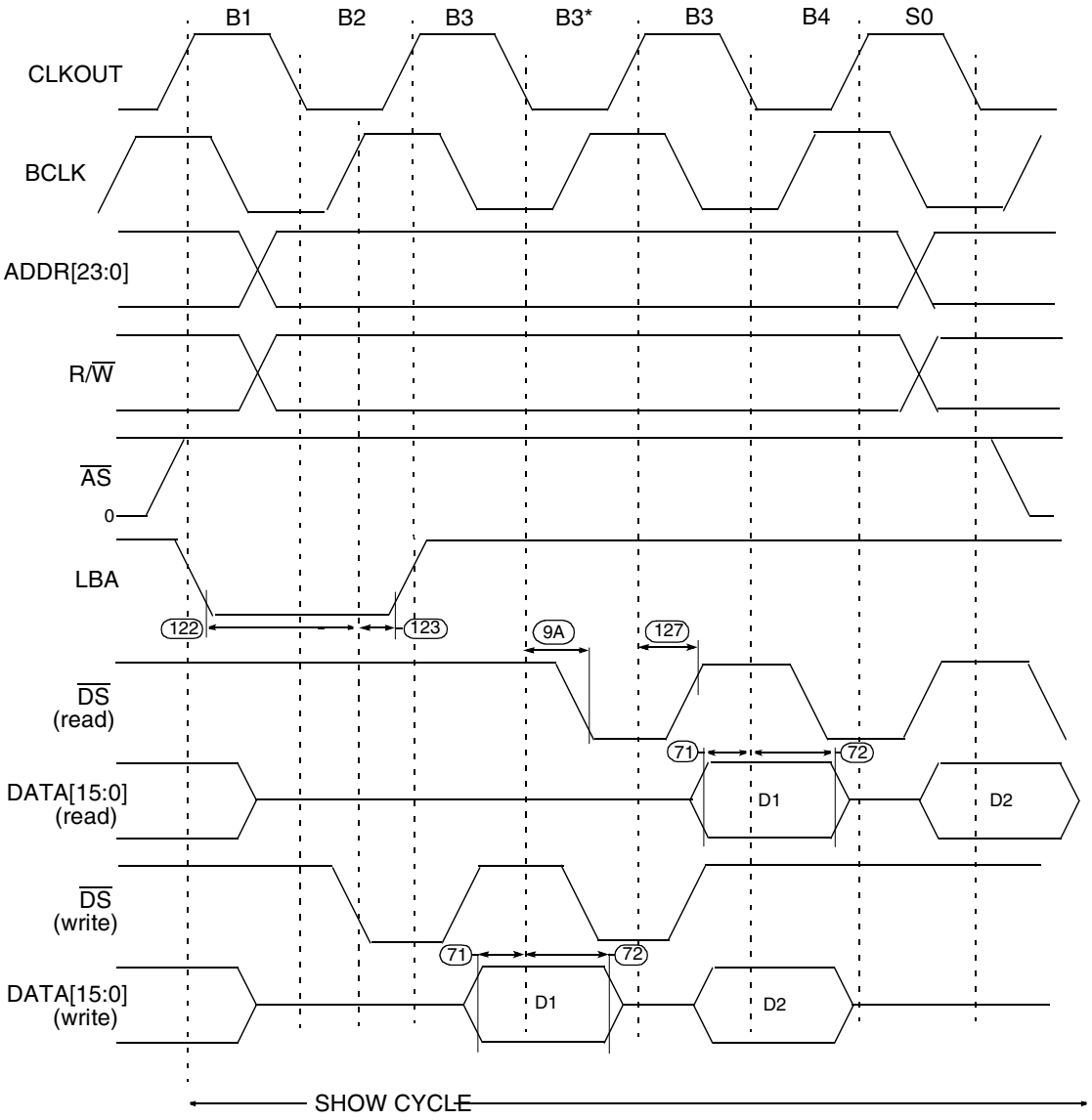


Figure E-11 Burst Show Cycle Timing

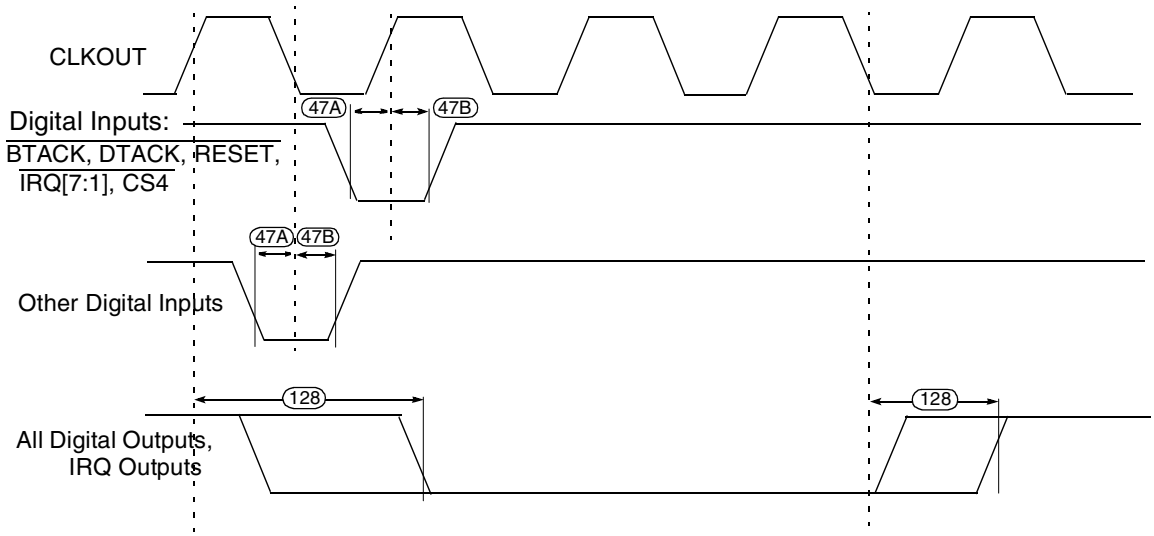


Figure E-12 Digital Input/Output and IRQ Output

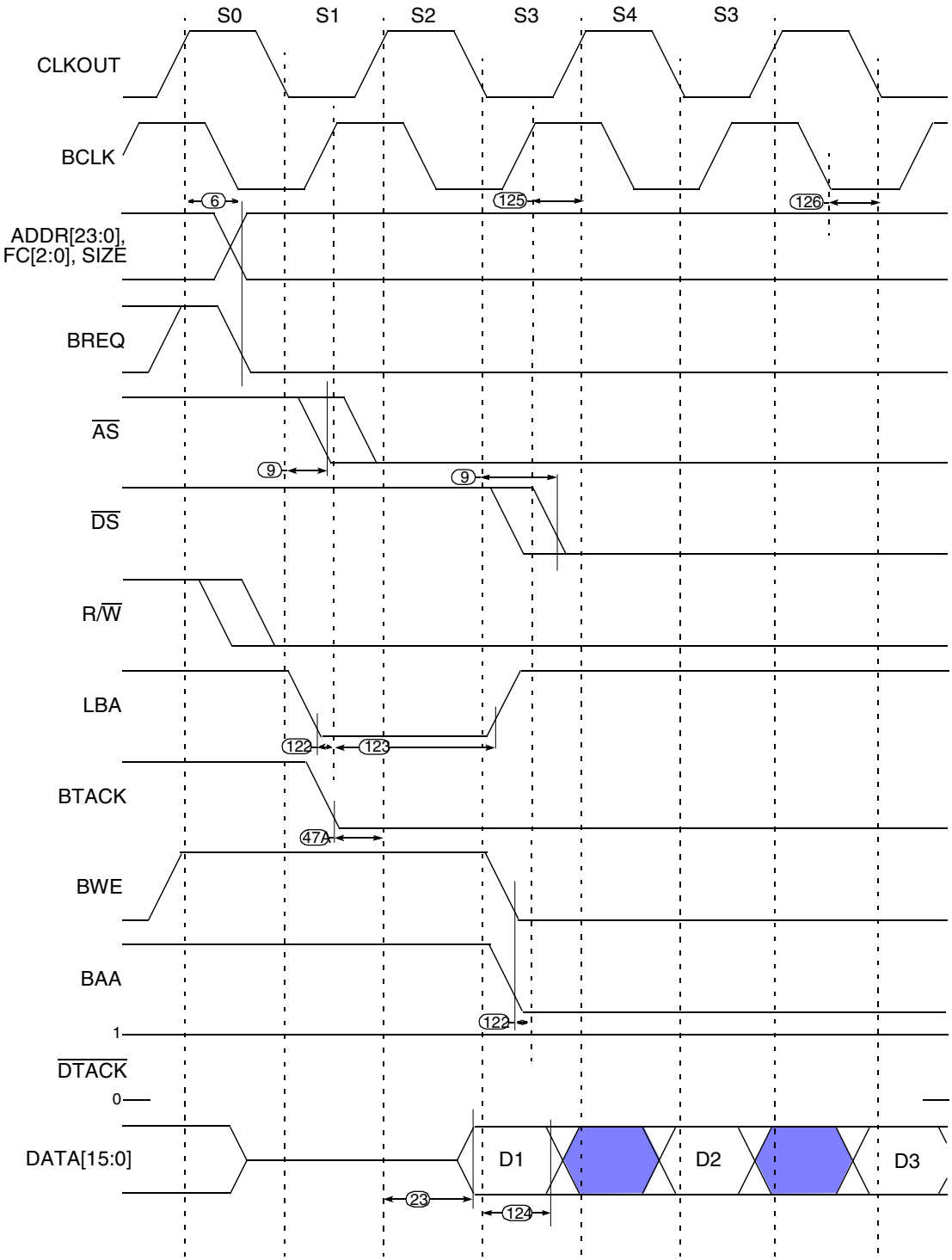


Figure E-13 Reset and Mode Select

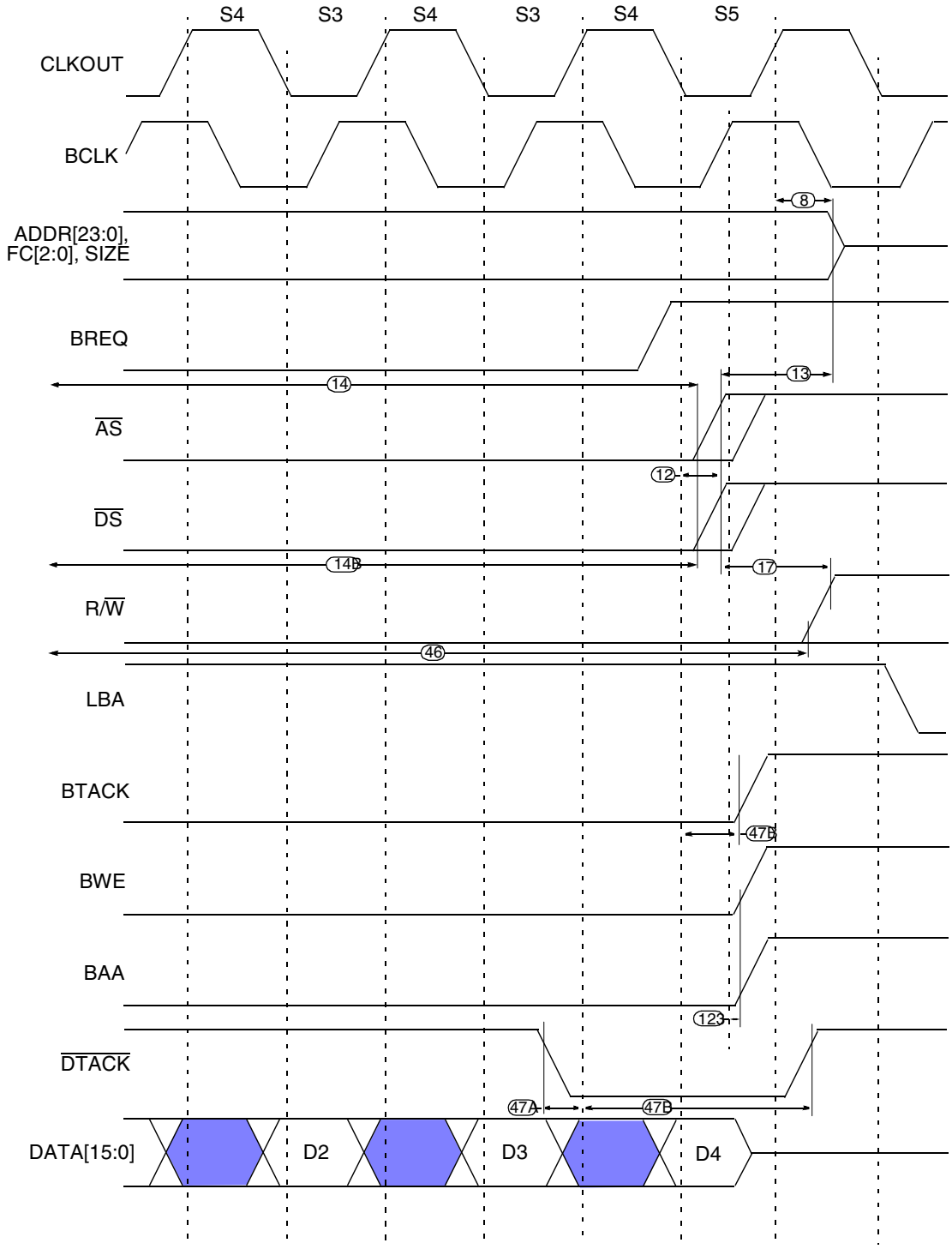
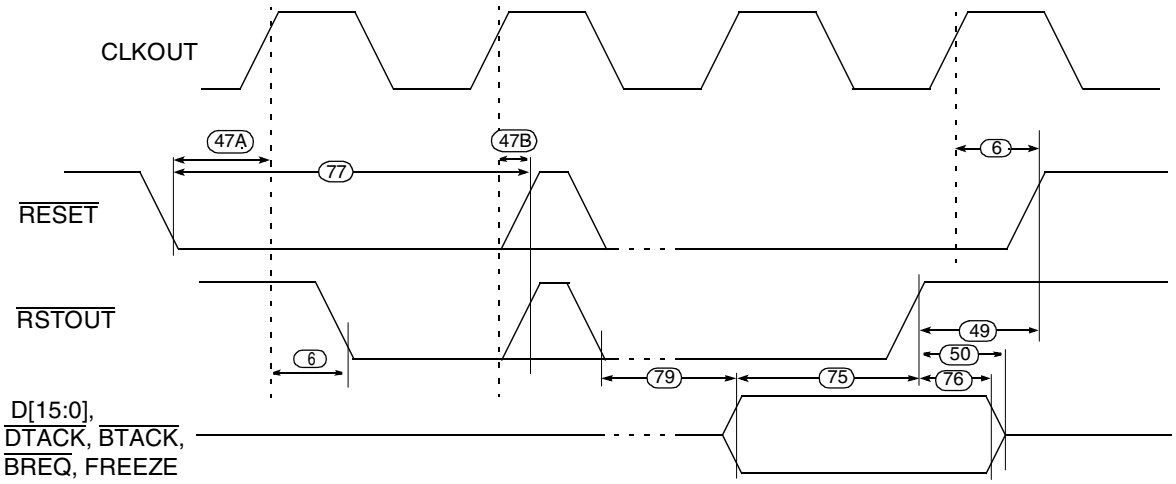


Figure E-14 Burst Write Cycle Timing — Initiation



Note: External data is sampled on the rising edge of CLOCKOUT
RESET and RSTOUT are driven on the rising edge of CLOCKOUT

Figure E-15 Burst Write Cycle Timing — Completion

Table E-5 BIM 25 MHz AC Timing

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation, Fast Reference (5.44 MHz crystal)[1]	f_{FST}	(0.032)TBD	25	MHz
1	Clock Period	t_{CYC}	40	—	ns
1B	External Clock Input Period	t_{XCYC}	40	—	ns
2, 3	Clock Pulse Width	t_{CW}	0.5 t_{cyc-2}	—	ns
4, 5	EXTAL input Rise and Fall Time	t_{Crf}	—	2	ns
4A, 5A	Other Signal Rise and Fall Time	t_{Crf}	—	3	ns
6	Clock High to BREQ, RESET, RSTOUT Valid	t_{CHAV}	—	16	ns
6A	Clock High to Address, FC, SIZE, R/$\overline{W}$, Valid	t_{CHAVA}	—	8	ns
6B	Address Valid to BCLK High (Including Pipeline Mode)	—	20	—	ns
7	Clock High to Address, Data, AS, DS, FC, SIZE, R/W, BREQ High Impedance	t_{CHAZx}	—	1.0	t_{cyc}
8	Clock High to Address, FC, SIZE, R/W Invalid	t_{CHAZn}	2	—	ns
8A	Clock High to BREQ Invalid	t_{CHAB}	2	20	ns
8B	BCLK High to Address Invalid (Pipeline Mode Only)	—	2	—	ns
9[2]	Clock Low to CS Valid (CS set to DS timing)	t_{CLSA}	2	16	ns
9A	Clock Low to AS, DS Valid	t_{STSA}	2	14	ns
9B	BCLK Low to CS Asserted (CS set to CE timing)	t_{STSB}	2	16	ns
11	Address, FC, SIZE, BREQ, R/W Valid to AS, DS, CS (CS set to DS timing) Valid	t_{AVSA}	7	—	ns
12	Clock Low to AS, DS, CS Invalid	t_{CLSN}	10	20	ns

Table E-5 BIM 25 MHz AC Timing (Continued)

Num	Characteristic	Symbol	Min	Max	Unit
13	AS, DS, CS Negated to Address, FC, SIZE Invalid (Address/ control Hold)	t_{SNAI}	7	—	t_{cyc}
14	AS Width Asserted, Read or Write Cycle[3] DS Width Asserted, Read Cycle	t_{SWA}	0.75 + ws	—	t_{cyc}
14A	CS Width Asserted, Read (CS set to CE timing)[3]	tSWAW	1 + ws	—	t_{cyc}
14B	DS, CS Width Asserted, Write (CS set to DS timing)[3]	tSWDW	ws - 0.25	—	t_{cyc}
15	AS, DS, CS Width Negated	t_{SN}	12	—	ns
17	AS, DS, CS Negated to R/W Invalid	t_{SNRN}	7	—	ns
22	R/W Low to CS Valid (CS set to CE timing)	t_{RASA}	7	—	ns
23	Clock High to Data-Out Valid, Write	t_{CHDO}	—	16	ns
25	DS, CS Negated to Data-Out Invalid (Data-Out Hold)	t_{SNDOI}	1	—	ns
26	Data-Out Valid to DS, CS Valid (Write)[4]	t_{DVSA}	7	—	ns
27A	Data-In Valid to BCLK High (Data Setup)	tCDSUA	7	—	ns
28	AS, DS Invalid to DTACK Invalid	t_{SNDN}	0	0.75	t_{cyc}
29	DS, CS Invalid to Data-In valid/High Impedance (Data-In Hold)[5]	t_{SNDI}	3	—	ns
30A	BCLK High to Data-In Invalid/High Impedance (Data-In Hold)	t_{CLDIA}	3	—	ns
46	R/$\overline{W}$ Width Asserted (Write or Read Cycle)[3]	t_{RWA}	1.5 + ws	—	t_{cyc}
47A	Asynchronous Input Setup Time $\overline{EBR}$, $\overline{DTACK}$, $\overline{BERR}$, $\overline{BTACK}$, $\overline{BKPT}$, $\overline{RESET}$	t_{AIST}	8	—	ns
47B	Asynchronous Input Hold Time $\overline{DTACK}$, $\overline{BERR}$, $\overline{BTACK}$, $\overline{BKPT}$, $\overline{RESET}$	t_{AIHT}	4	—	ns
49	$\overline{RSTOUT}$ High to $\overline{RESET}$ High	t_{IHRH}	12	—	ns
50	$\overline{RSTOUT}$ High to Mode Select Invalid/High Impedance	—	—	14	t_{cyc}
51	$\overline{RESET}$ High to $\overline{RSTOUT}$ Valid	t_{IHMZ}	—	0.5	t_{cyc}
53	Data-Out Hold from Clock Low	t_{DOCH}	0	—	ns
54	Clock Low to Data-Out High Impedance	t_{CHDH}	—	0.5	t_{cyc}
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	0.5	—	t_{cyc}
56	$\overline{RSTOUT}$ Pulse Width (Reset Instruction)	t_{RPWI}		256	t_{cyc}
56A	$\overline{RSTOUT}$ Pulse Width (Reset Pin)	t_{RPWP}	512	—	t_{cyc}
71	Data Valid to Clock Low (Show data setup)	t_{SCLDS}	5	—	ns
72	Clock Low to Data Invalid (Show data hold)	t_{SCLDH}	5	—	ns
75	Mode Select Setup Time	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time	t_{MSH}	0	—	ns
77	$\overline{RESET}$ (Input) Assertion Time[6]	t_{RSTA}	4	—	t_{cyc}
79	$\overline{RESET}$ Low and $\overline{RSTOUT}$ Low to Mode Select Drive	t_{RILM}	0	1	t_{cyc}
114	CSE0, CSE1 Valid to Clock High (Emulation, Setup)	t_{CECH}	5	—	ns
115	Clock High to CSE0, CSE1, FREEZE Invalid (Emulation, Hold)	t_{CHCEI}	5	—	ns
117	FREEZE Valid to Clock High (Emulation, Setup)	t_{FCH}	15	—	ns
122	LBA, BAA Valid to BCLK High	tBSU	24	—	ns
122A	HPCE Valid to BCLK High (LBA or BAA set to HPCE function)	tHPCE	30	—	ns
122B	BOE, BWE Valid to BCLK High (Burst, Setup)	tBSUB	0	—	ns
123	BCLK High to LBA, BAA, Invalid (Burst, Hold)	t_{BH}	2	16	ns
123A	BCLK High to BOE, BWE Invalid (Burst, Hold)	t_{BHA}	2	10	t_{cyc}

Table E-5 BIM 25 MHz AC Timing (Continued)

Num	Characteristic	Symbol	Min	Max	Unit
125	Clock High to BCLK High	tBCH	$0.25t_{cyc}$-1	$0.25t_{cyc}$+1	ns
126	Clock Low to BCLK Low	tBCL	$0.25t_{cyc}$-1	$0.25t_{cyc}$+1	ns
127	Clock High to $\overline{DS}$ Invalid(Show)	t_{CHDN}	2	16	ns
128	Clock High to Digital Output Valid	t_{CDIO}	90	600	ns

NOTES:

1. Minimum system clock frequency is crystal frequency divided by 128, subject to specified limits.
2. DS and CS do not assert on a zero wait state write cycle.
3. Number of wait states = ws. In a 2-clock bus cycle, ws =0. For 3-clock bus cycle, ws = 1.
4. Specification 26 is valid only for 3-clock or more bus cycles. Specification 26 does not apply to 2-clock bus cycles. Data-Out to CS asserted apply only when CS is configured as DS timing (STRB=1)
5. These hold times are specified with respect to DS or CS on asynchronous reads or CLKOUT. The user is free to choose either hold time.

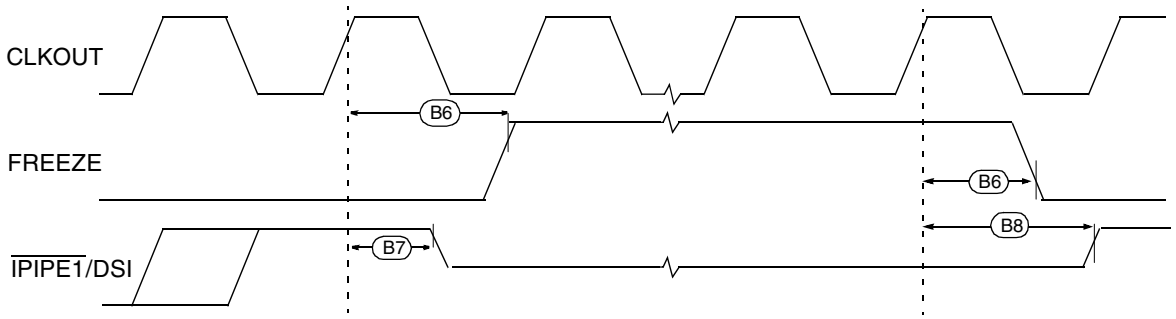


Figure E-16 Background Debug Mode (Freeze Assertion)

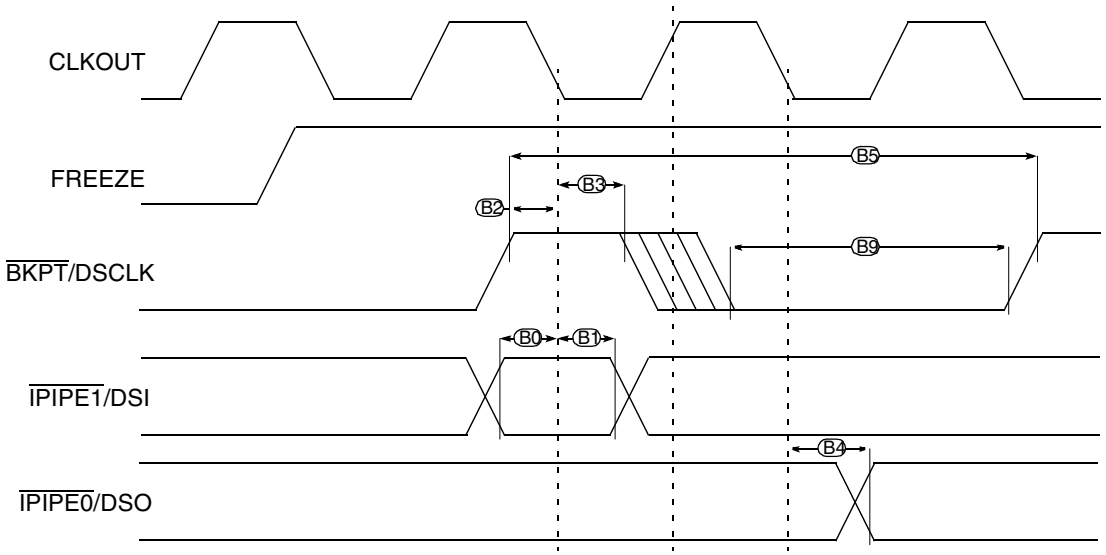


Figure E-17 Background Mode (Serial Communication)

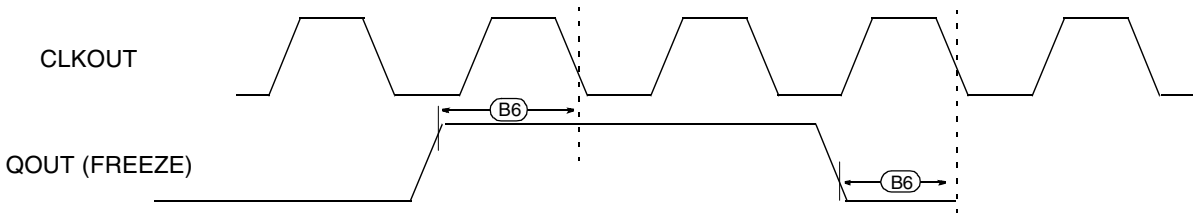


Figure E-18 QOUT Assertion

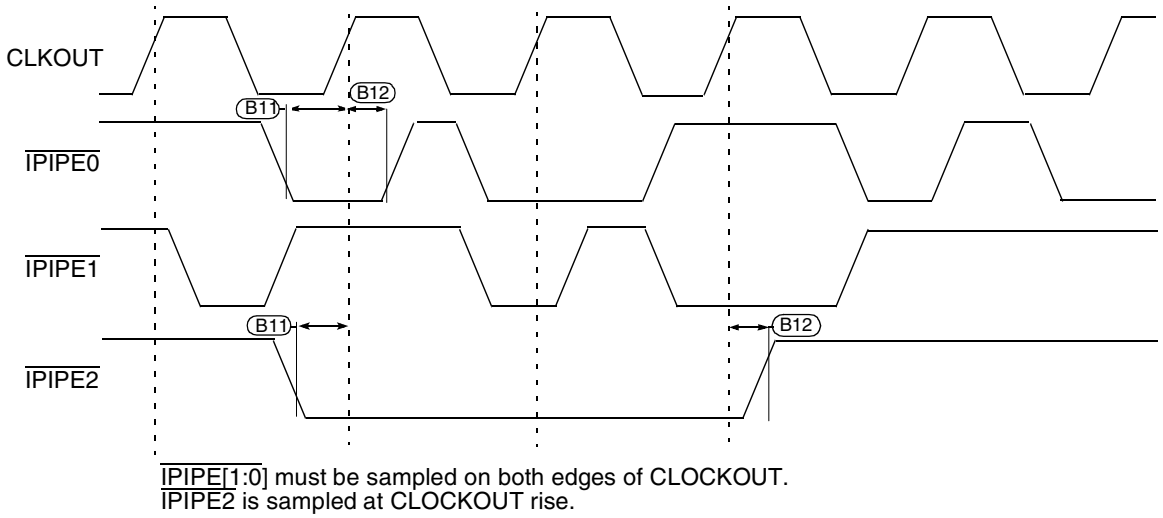


Figure E-19 Pipe Tracking Pin

Table E-6 Background Debug Mode Timing

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	0.25	—	t_{cyc}
B1	DSI Input Hold Time	t_{DSIH}	0.25	—	t_{cyc}
B2	DSCLK Setup Time	t_{DSCSU}	0.25	—	t_{cyc}
B3	DSCLK Hold Time	t_{DSCH}	0.25	—	t_{cyc}
B4	DSO Delay Time	t_{DSOD}	—	0.5	t_{cyc}
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	t_{FRZAN}	—	1	t_{cyc}
B6B	QOUT(FREEZE) Asserted/Negated to CLKOUT Low	t_{FRZAL}	4	t_{cyc}- 2	ns
B7	CLKOUT High to IPIPE1 High Impedance	t_{IFZ}	—	1	t_{cyc}
B8	CLKOUT High to IPIPE1 Valid	t_{IF}	—	1	t_{cyc}
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}
B11	IPIPE Valid to CLKOUT High or Low	tISU	2.5		ns
B12	CLKOUT High or Low to IPIPE Invalid	tIH	2		ns

E.2.3 FASRAM AC Timings

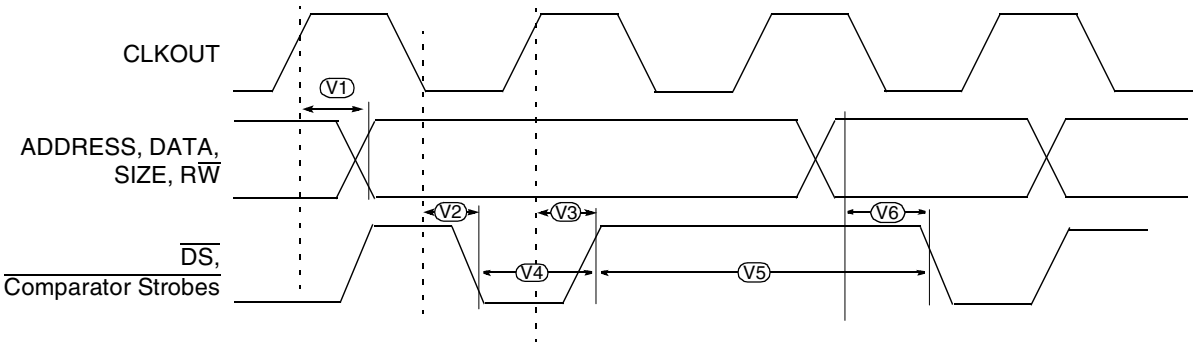


Figure E-20 Visibility Bus

Table E-7 Visibility Bus Timing

Num	Characteristic	Symbol	Min	Max	Unit
V1	CLKOUT High to Address, Data, Size, RW Valid	t_{VSU}	2	13	ns
V2	CLKOUT Low to STROBEs Asserted	t_{VH}	2	11.5	ns
V3	CLKOUT High to STROBEs Negated	t_{VSSU}	2	11.5	ns
V4	Strobe Width Asserted	t_{VSWA}	0.25	0.5	t_{cyc}
V5	Strobe Width Negated	t_{VSWN}	0.25	0.5	t_{cyc}
V6	Address, Data, R/W, SIZE Valid to Strobe Asserted	t_{VSH}	0.25	—	t_{cyc}

E.2.4 QADC64 Electrical and AC Characteristics

Table E-8 QADC64 Maximum Ratings

Num	Characteristic	Symbol	Min	Max	Unit
1	Analog Supply, with reference to V_{SSA}	V_{DDA}	-0.3	6.5	V
2	Internal Digital Supply, with reference to V_{SSI}	V_{DDI}	-0.3	6.5	V
3	Reference Supply, with reference to V_{RL}	V_{RH}	-0.3	6.5	V
4	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	-0.1	0.1	V
5	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	-6.5	6.5	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	-6.5	6.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	-6.5	6.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	-6.5	6.5	V
9	Disruptive Input Current[1, 2, 3, 4, 5, 6] $V_{NEGCLMAP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DDA} + 2$	I_{NA}	-500	500	µA
10	Adjacent Pin Attenuation[1, 5, 6, 7]	—	500	—	—
11	Maximum Input Current [3, 4, 6] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DDA} + 2$	I_{MA}	-25	25	mA

NOTES:

1. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
2. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also affect the conversion accuracy of other channels.
3. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using positive and negative clamp values, then use the larger of the calculated values.
5. This parameter is periodically sampled rather than 100% tested.
6. Condition applies to one pin at a time only.
7. The attenuation factor reflects current induced on pins adjacent pins to the pin under negative stress conditions. A voltage drop may occur across the external source impedances of the adjacent pins impacting conversions on these pins.

Table E-9 QADC64 Electrical Characteristics (Operating)

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Internal Digital Supply[1]	V_{DDL}	3.0	3.6	V
3	V_{SS} Differential Voltage	$V_{SS} - V_{SSA}$	-100	100	mV
4	Reference Voltage Low[2]	V_{RL}	V_{SSA}	V_{SSA} + 0.1	V
5	Reference Voltage High[2]	V_{RH}	V_{DDA} - 0.1	V_{DDA}	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	4.5	5.5	V
7	Input Voltage	V_{INDC}	V_{SSA} - 0.3	V_{DDA} + 0.3	V
8	Input High Voltage, PQA and PQB	V_{IH}	0.7 (V_{DDA})	V_{DDA} + 0.3	V
9	Input Low Voltage, PQA and PQB	V_{IL}	V_{SSA} - 0.3	0.4 (V_{DDA})	V
10	Input Hysteresis, PQA, PQB[3]	V_{HYS}	0.5	—	V
11	Output Voltage, PQA[4] I_{OL} = 3.2 mA I_{OH}= -2.0 mA	 V_{OL} V_{OH}	 — 3.8	 0.45 —	 V V
12	Analog Supply Current Normal Operation[5] Low-Power Stop	 I_{DDA}	 — —	 5.0 10.0	 mA µA
13	Reference Supply Current, DC Reference Supply Current, Transient	I_{REF} i_{REF}	— —	250 2.0	µA mA
14	Load Capacitance, PQA output	C_L	—	50	pF
15	Input Current, Channel Off[6] PQA, PQB	I_{OFF}	-200	200	nA
16	Total Input Capacitance[7] PQA, PQB, Not Sampling Incremental Cap added during Sampling	C_{IN}	— —	15 5	pF
17	Disruptive Input Injection Current[8]	I_{INJ}	-3	3	mA

NOTES:

1. Refers to operation over full temperature and frequency range. Here V_{DDL}= 3.3 V typical.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Parameter applies to the following pins:
   Port A: PQA[7:0]/AN[59:58]/ETRIG[2:1]
   Port B: PQB[7:0]/AN[3:0]/AN[51:48]/AN[Z:W]
4. Full driver (push-pull).
5. Current measured at maximum system clock frequency with QADC active.
6. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C.
7. This parameter is periodically sampled rather than 100% tested.
8. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \le V_{DDA}$ and $V_{RL} \ge V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

E.2.5 QADC64 AC TIMINGS

Table E-10 QADC64 Conversion Characteristics (Operating)

Num	Parameter	Symbol	Min	Typ	Max	Unit
1	QADC Clock (QCLK) Frequency[1]	F_{QCLK}	0.5	—	2.1	MHz
2	Conversion Cycles[2]	CC	14	—	28	QCLK cycles
3	Conversion Time [2,3] F_{QCLK} = 2.0MHz[1,4] Min = CCW/IST =%00 Max = CCW/IST =%11	T_{CONV}	7.0	—	14.0	µs
4	Stop Mode Recovery Time	T_{SR}	—	—	10	µs
5	Resolution[5]	—	—	5	—	mV
7	Disruptive Input Injection Current[7, 6, 7, 8, 9]	I_{INJ}	-3		3	mA
8	Coupling Ratio [7 ,10,11, 12] PQA, PQB	K	—	—	10^{-4}	V/V or A/A
9	Incremental Error due to injection current All channels have same 10 KΩ < Rs < 100 KΩ[15] Channel under test has Rs = 10 KΩ, I_{INJ} = ± 3 mA[13,14]				±1.0 ±1.0	Counts Counts
10	Source impedance at input[13]	R_S	—	10	100	KΩ
11	Incremental Capacitance during Sampling[14]	C_{SAMP}	—	—	5	pF

NOTES:

1. Conversion characteristics may vary with F_{QCLK} rate, possibly causing reduced conversion accuracy at max F_{QCLK} rate.
2. This specification depends on the value of “BYP” and “IST” control bits in the active CCW.
3. Assumes that f_{SYS} = 40 MHz.
4. Assumes F_{QCLK} = 2.00 MHz, with clock prescaler values of:
   QACR0: PSH =%01011, PSA =%0, PSL =111)
   CCW: BYP =%0
5. At $V_{RH} - V_{RL}$ = 5.12 V, one count = 5 mV.
6. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \le V_{DDA}$ and $V_{RL} \ge V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
7. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
8. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP}$ = VDDA + 0.3 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.
9. Condition applies to two pins, adjacent to channel being converted.
10. Coupling Ratio, K, is defined as the ratio of the output current, I_{out}, measured on the pin under test to the injection current, I_{inj}, when both adjacent pins are overstressed with the specified injection current. $K = I_{out} / I_{inj}$ The input voltage error on the channel under test is calculated as $Verr = I_{inj} * K * R_S$
11. Total Injection current is determined by the number of channels injecting (e.g. 15), external injection voltage ($V_{INJ} - V_{POSCLAMP}$, or $V_{INJ} - V_{NEGCLAMP}$) , and the external source impedance, Rs, wherein all input channels have the same values. To determine the error voltage on the converted channel, only the two adjacent channels are expected to contribute to the error voltage:
    $$V_{errj} = (V_{INJ} - V_{CLAMP}) * K*2$$
12. Performance expected with production silicon.

13. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.
Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{errj}):

$$V_{errj} = R_S * I_{OFF}$$

where I_{OFF} is a function of operating temperature. (See **Table E-9**, note 6).
Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the filtering capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance.
14. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * C_{SAMP}$. The value of C_{SAMP} in the new design may be reduced, or increased slightly.

E.2.6 QSM Electrical Characteristics

Table E-11 QSM DC Electrical Specifications

Characteristic	Symbol	Rise/Fall Time (ns)	Max Load (pf)
Load Capacitance for QSM Output Pins	$QSMC_L$	41	200
		31	150
		21	100

E.2.7 QSM AC Timings

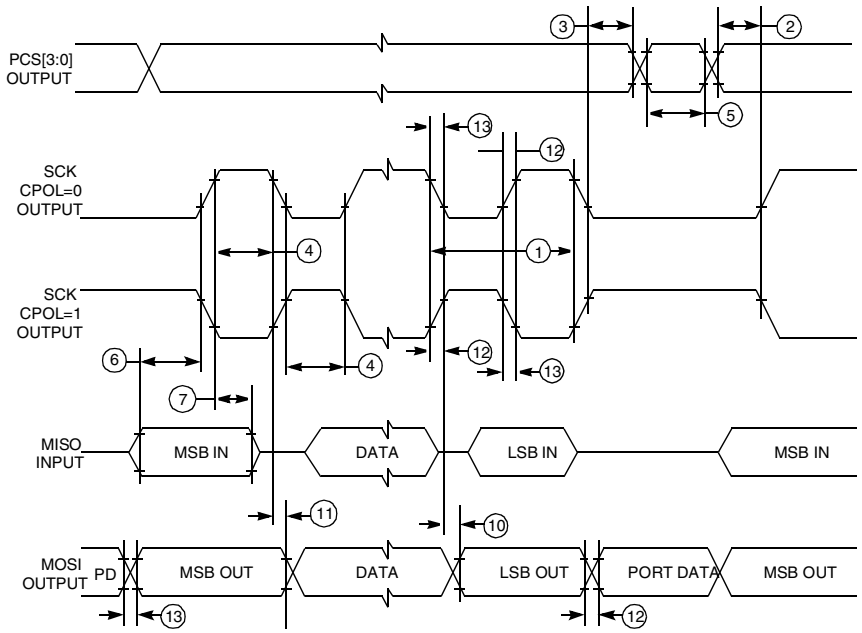


Figure E-21 QSPI Timing — Master, CPHA = 0

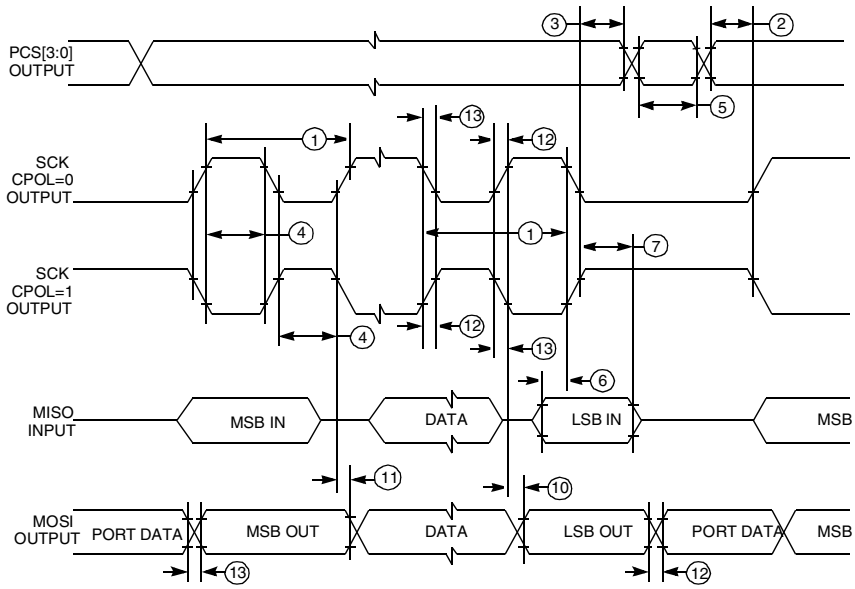


Figure E-22 QSPI Timing — Master, CPHA = 1

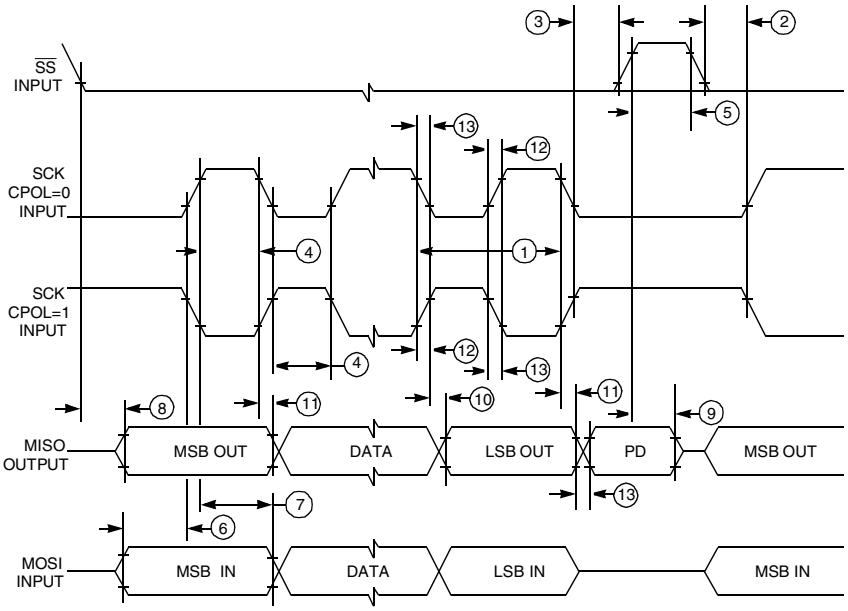


Figure E-23 QSPI Timing — Slave, CPHA = 0

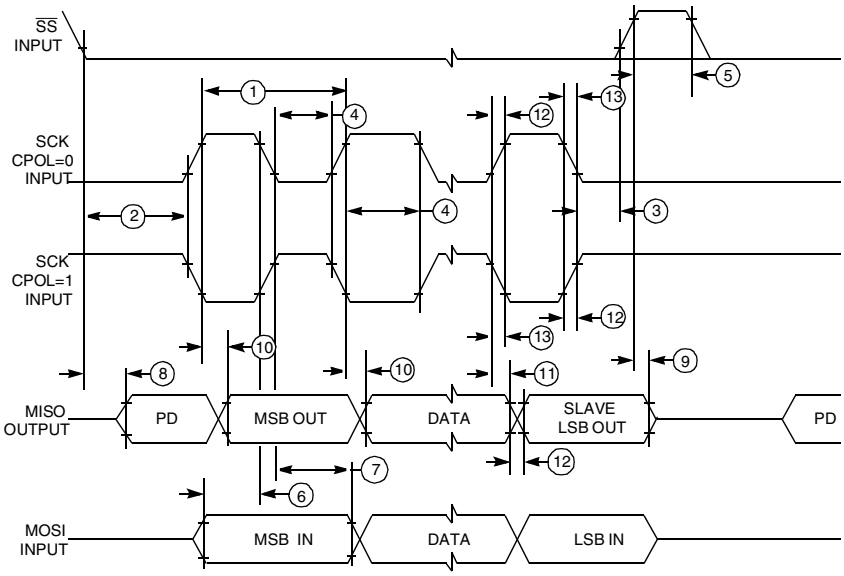


Figure E-24 QSPI TIming — Slave, CPHA = 1

Table E-12 QSPI Timing

Num	Function	Symbol	Min	Max	Unit
0	Operating Frequency Master Slave	f_{op}	DC DC	1/4 1/4	f_{sys} f_{sys}
1	Cycle Time Master Slave	t_{qcyc}	4 4	510 —	t_{cyc} t_{cyc}
2	Enable Lead Time Master Slave	t_{lead}	2 2	128 —	t_{cyc} t_{cyc}
3	Enable Lag Time Master Slave	t_{lag}	2 —	1/2 —	SCK t_{cyc}
4	Clock (SCK) High or Low Time Master Slave[1]	t_{sw}	2 tcyc – 60 2 tcyc – n	255 tcyc —	ns ns
5	Sequential Transfer Delay Master Slave (Does Not Require Dese-lect)	t_{td}	17 13	8192 —	t_{cyc} t_{cyc}
6	Data Setup Time (Inputs) Master Slave	t_{su}	30 20	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	t_{hi}	0 20	— —	ns ns
8	Slave Access Time	t_a	—	1	t_{cyc}

Table E-12 QSPI Timing (Continued)

Num	Function	Symbol	Min	Max	Unit
9	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
10	Data Valid (after SCK Edge) Master Slave	t_v	— —	50 50	ns ns
11	Data Hold Time (Outputs) Master Slave	t_{ho}	0 0	— —	ns ns
12	Rise Time Input Output	t_{ri} t_{ro}	— —	2 See Note 2	µs ns
13	Fall Time Input Output	t_{fi} t_{fo}	— —	2 See Note 2	µs ns

NOTES:
1. For high time, n = external SCK rise time; for low time, n = external SCK fall time.
2. The output rise time and fall time vary for different MCUs depending on the I/O pad used.

E.2.8 CTM9 AC Timing

Table E-13 MCSM Timing

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin frequency[1]	f_{PCNTR}	0	$f_{sys}/4$	MHz
2	Input pin low time	t_{PINL}	$2.0/f_{sys}$	—	µs
3	Input pin high time	t_{PINH}	$2.0/f_{sys}$	—	µs
4	Clock pin to counter increment	t_{PINC}	$4.5/f_{sys}$	$6.5/f_{sys}$	µs
5	Clock pin to new TBB value	t_{PTBB}	$5.0/f_{sys}$	$7.0/f_{sys}$	µs
6	Clock pin to COF set ($FFFF)	t_{PCOF}	$4.5/f_{sys}$	$6.5/f_{sys}$	µs
7	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
8	Flag to IMB interrupt request	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs
9	Counter resolution[2]	t_{CRES}	—	$2.0/f_{sys}$	µs

NOTES:
1. Value applies when using external clock
2. Value applies when using internal clock. Minimum counter resolution depends on prescaler divide ratio selection

Table E-14 PWMSM Timing

Num	Parameter	Symbol	Min	Max	Unit
1	PWMSM output resolution[1]	t_{PWMR}	—	—	µs
2	PWMSM output pulse[2]	t_{PWMO}	$2.0/f_{sys}$	—	µs
3	PWMSM output pulse[3]	t_{PWMO}	$2.0/f_{sys}$	$2.0/f_{sys}$	µs
4	CPSM enable to output set PWMSM enabled before CPSM, DIV23 = 0 PWMSM enabled before CPSM, DIV23 = 1	t_{PWMP}	 $3.5/f_{sys}$ $6.5/f_{sys}$	—	µs
5	PWM enable to output set PWMSM enabled before CPSM, DIV23 = 0 PWMSM enabled before CPSM, DIV23 = 1	t_{PWME}	 $3.5/f_{sys}$ $5.5/f_{sys}$	 $4.5/f_{sys}$ $6.5/f_{sys}$	µs
6	FLAG to IMB interrupt request	t_{FIRQ}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs

NOTES:
1. Minimum output resolution depends on counter and prescaler divide ratio selection.
2. Excluding the case where the output is always zero.
3. Excluding the case where the output is always zero.

Table E-15 SASM Timing

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	t_{PINL}	$2.0/f_{sys}$	—	µs
2	Input pin high time	t_{PINH}	$2.0/f_{sys}$	—	µs
3	Input capture resolution[1]	t_{RESCA}	—	$2.0/f_{sys}$	µs
4	Pin to input capture delay	t_{PCAPT}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
5	Pin to FLAG set	t_{PFLAG}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
6	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
7	OCT output pulse	t_{OCT}	$2.0/f_{sys}$	—	µs
8	Compare resolution[1]	t_{RESCM}	—	$2.0/f_{sys}$	µs
9	TBB change to FLAG set	t_{CFLAG}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
10	TBB change to pin change[2]	t_{CPIN}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
11	Flag to IMB interrupt request[2]	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs

NOTES:
1. Minimum resolution depends on counter and prescaler divide ratio selection.
2. Time given from when new value is stable on time base bus.

Table E-16 DASM Timing

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	t_{PINL}	$2.0/f_{sys}$	—	µs
2	Input pin high time	t_{PINH}	$2.0/f_{sys}$	—	µs
3	Input capture resolution[1]	t_{RESCA}	—	$2.0/f_{sys}$	µs
4	Pin to input capture delay	t_{PCAPT}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
5	Pin to FLAG set	t_{PFLAG}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
6	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
7	OCT output pulse	t_{OCT}	$2.0/f_{sys}$	—	µs
8	Compare resolution[1]	t_{RESCM}	—	$2.0/f_{sys}$	µs
9	TBB change to FLAG set	t_{CFLAG}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
10	TBB change to pin change[2]	t_{CPIN}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
11	Flag to IMB interrupt request[2]	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs

NOTES:
1. Minimum resolution depends on counter and prescaler divide ratio selection.
2. Time given from when new value is stable on time base bus.

Table E-17 PWMSM Timing

Num	Parameter	Symbol	Min	Max	Unit
1	PWMSM output resolution[1]	t_{PWMR}	—	—	µs
2	PWMSM output pulse[2]	t_{PWMO}	$2.0/f_{sys}$	—	µs
3	PWMSM output pulse[2]	t_{PWMO}	$2.0/f_{sys}$	$2.0/f_{sys}$	µs
4	CPSM enable to output set PWMSM enabled before CPSM, DIV23 = 0 PWMSM enabled before CPSM, DIV23 = 1	t_{PWMP}	 $3.5/f_{sys}$ $6.5/f_{sys}$	—	µs
5	PWM enable to output set PWMSM enabled before CPSM, DIV23 = 0 PWMSM enabled before CPSM, DIV23 = 1	t_{PWME}	 $3.5/f_{sys}$ $5.5/f_{sys}$	 $4.5/f_{sys}$ $6.5/f_{sys}$	µs
6	FLAG to IMB interrupt request	t_{FIRQ}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs

NOTES:
1. Minimum output resolution depends on counter and prescaler divide ratio selection.
2. Excluding the case where the output is always zero.

E.2.9 TPU AC Characteristics

Table E-18 Time Processor Unit Timing (TPU)

Num	Rating	Symbol	Min	Max	Unit
1	CLKOUT High to TPU2 Output Channel Valid	t_{CHTOV}	2	23	ns
2	CLKOUT High to TPU2 Output Channel Hold	t_{CHTOH}	0	20	ns
3	TPU2 Input Channel Pulse Width	t_{TIPW}	4	—	t_{cyc}

E.2.10 TouCAN AC Characteristics

Table E-19 TouCAN AC Characteristics

Num	Parameter	Symbol	Value	Unit
1	CNTX0 – Delay from ICLOCK	—	19	ns
2	CNRX0 – Set-up to rise ICLOCK	—	0	ns
3	TOUCAN serial (Tx, Rx pins) max frequency	—	1	MHz

E.2.11 DLCMD3 AC Characteristics

Table E-20 DLCMD2 Requirements

Operating Temperature	IC Package	Clock Speed[1]	Quiescent Current Draw
–40 to +125 °C	NA	2.00 Mhz (Min) to 128.00 MHz (Max)	50 µA LPSTOP, 200 µA idle

NOTE:

1. No additional clock part needed for the DLCMD2. The DLCMD2 will adapt to the CPU (IMB3) clocking using software programmable prescaler. DLCMD2 must correctly operate over any clock jitter present within the integrated device.