



SECTION 2 NOMENCLATURE

The following nomenclature is used throughout the manual. Nomenclature used only in certain sections, such as register bit mnemonics, is defined in those sections.

2.1 Symbols and Operators

| | | |
|-------------------------|---|--|
| + | — | Addition |
| − | — | Subtraction or negation (two's complement) |
| * | — | Multiplication |
| / | — | Division |
| > | — | Greater |
| < | — | Less |
| = | — | Equal |
| ≥ | — | Equal or greater |
| ≤ | — | Equal or less |
| ≠ | — | Not equal |
| • | — | AND |
| + | — | Inclusive OR (OR) |
| ⊕ | — | Exclusive OR (EOR) |
| $\overline{\text{NOT}}$ | — | Complementation |
| : | — | Concatenation |
| ⇒ | — | Transferred |
| ⇔ | — | Exchanged |
| ± | — | Sign bit; also used to show tolerance |
| « | — | Sign extension |
| % | — | Binary value |
| \$ | — | Hexadecimal value |

2.2 CPU32 Registers



A6–A0 — Address registers (index registers)
A7 (SSP) — Supervisor stack pointer
A7 (USP) — User stack pointer
CCR — Condition code register (user portion of SR)
D7–D0 — Data registers (index registers)
DFC — Alternate function code register
PC — Program counter
SFC — Alternate function code register
SR — Status register
VBR — Vector base register
X — Extend indicator
N — Negative indicator
Z — Zero indicator
V — Two's complement overflow indicator
C — Carry/borrow indicator

2.3 Pin and Signal Mnemonics

ADDR[23:0] — Address Bus
AN[59:48]/[3:0] — QADC Analog Input
AN[w, x, y, z] — QADC Analog Input
 \overline{AS} — Address Strobe
 \overline{AVEC} — Autovector
 \overline{BERR} — Bus Error
 \overline{BG} — Bus Grant
 \overline{BGACK} — Bus Grant Acknowledge
 \overline{BKPT} — Breakpoint
 \overline{BR} — Bus Request
CANRX0 — TouCAN Receive Data
CANTX0 — TouCAN Transmit Data
CLKOUT — System Clock
 $\overline{CS}[10:0]$ — Chip Selects
 \overline{CSBOOT} — Boot ROM Chip Select
CPWM[8:5] — CTM Pulse Width Modulation Channel
CTD[10:9]/[4:3] — CTM Double Action Channel
CTM2C — CTM Modulus Clock



| | |
|-----------------------|--|
| DATA[15:0] | — Data Bus |
| \overline{DS} | — Data Strobe |
| DSACK[1:0] | — Data and Size Acknowledge |
| DSCLK | — Development Serial Clock |
| DSI | — Development Serial Input |
| DSO | — Development Serial Output |
| ECLK | — MC6800 Devices and Peripherals Bus Clock |
| ETRIG[2:1] | — QADC External Trigger |
| EXTAL | — Crystal Oscillator Input |
| FC[2:0] | — Function Codes |
| FREEZE | — Freeze |
| \overline{HALT} | — Halt |
| \overline{IFETCH} | — Instruction Fetch |
| \overline{IPIPE} | — Instruction Pipeline |
| $\overline{IRQ}[7:1]$ | — Interrupt Request |
| MA[2:0] | — QADC Multiplexed Address |
| MISO | — QSM Master In Slave Out |
| MODCLK | — Clock Mode Select |
| MOSI | — QSM Master Out Slave In |
| PCS[3:0] | — QSM Peripheral Chip-Selects |
| PQA[7:0] | — QADC Port A |
| PQB[7:0] | — QADC Port B |
| PC[6:0] | — SIM Port C |
| PE[7:0] | — SIM Port E |
| PF[7:0] | — SIM Port F |
| QUOT | — Quotient Out |
| R/\overline{W} | — Read/Write |
| \overline{RESET} | — Reset |
| \overline{RMC} | — Read-Modify-Write Cycle |
| RXD | — SCI Receive Data |
| SCK | — QSPI Serial Clock |
| SIZ[1:0] | — Size |
| \overline{SS} | — Slave Select |
| T2CLK | — TPU Clock In |
| TPUCH[15:0] | — TPU Channel Signals |
| TSC | — Three-State Control |
| \overline{TSTME} | — Test Mode Enable |



V_{RH} — QADC High Reference Voltage
 V_{RL} — QADC Low Reference Voltage
XFC — External Filter Capacitor
XTAL — Crystal Oscillator Output

2.4 Register Mnemonics

BIUMCR — CTM4 BIUSM Module Configuration
BIUTEST — CTM4 BIUSM Test Register
BIUTBR — CTM4 BIUSM Time Base Register
CANCTRL[0:2] — TouCAN Control Register [0:2]
CANICR — TouCAN Interrupt Configuration Register
IFLAG — TouCAN Interrupt Flags Register
IMASK — TouCAN Interrupt Masks Register
CANMCR — TouCAN Module Configuration Register
CANTCR — TouCAN Test Configuration Register
CCW[0:27] — QADC Command Conversion Words [0:27]
CFSR[0:3] — TPU Channel Function Select Registers [0:3]
CIER — TPU Channel Interrupt Enable Register
CISR — TPU Channel Interrupt Status Register
CPCR — CTM4 CPSM Control Register
CPR[0:1] — TPU Channel Priority Registers [0:1]
CPTR — CTM4 CPSM Test Register
CR[0:F] — QSM Command RAM
CREG — SIM Test Control Register C
CSBARBT — SIM Chip-Select Base Address Register Boot ROM
CSBAR[0:10] — SIM Chip-Select Base Address Registers [0:10]
CSORBT — SIM Chip-Select Option Register Boot ROM
CSOR[0:10] — SIM Chip-Select Option Registers [0:10]
CSPAR[0:1] — SIM Chip-Select Pin Assignment Registers [0:1]
DASM[3:4]/[9:10]A — CTM4 DASM A Registers [3:4]/[9:10]
DASM[3:4]/[9:10]B — CTM4 DASM B Registers [3:4]/[9:10]
DASM[3:4]/[9:10]SIC — CTM4 DASM Status/Interrupt/Control Registers [3:4]/[9:10]
DCNR — Decoded Channel Number Register
DDRE — SIM Port E Data Direction Register
DDRF — SIM Port F Data Direction Register
DDRQA — QADC Port A Data Direction Register



| | | |
|-----------------|---|---|
| DDRQS | — | QSM Port QS Data Direction Register |
| DREG | — | SIM Test Module Distributed Register |
| DSCR | — | TPU Development Support Control Register |
| DSSR | — | TPU Development Support Status Register |
| ESTAT | — | TouCAN Error and Status Register |
| FCSM12CNT | — | CTM4 FCSM12 Counter Register |
| FCSM12SIC | — | CTM4 FCSM12 Status/Interrupt/Control Register |
| HSQR[0:1] | — | TPU Host Sequence Registers [0:1] |
| HSRR[0:1] | — | TPU Host Service Request Registers [0:1] |
| LJSRR[0:27] | — | QADC Left-Justified Signed Result Registers [0:27] |
| LJURR[0:27] | — | QADC Left-Justified Unsigned Result Registers [0:27] |
| LR | — | Link Register |
| MCSM[2]/[11]CNT | — | CTM4 MCSM Counter Registers [2]/[11] |
| MCSM[2]/[11]ML | — | CTM4 MCSM Modulus Latch Registers [2]/[11] |
| MCSM[2]/[11]SIC | — | CTM4 MCSM Status/Interrupt/Control Registers [2]/[11] |
| MRMCR | — | Masked ROM Module Configuration Register |
| PEPAR | — | SIM Port E Pin Assignment Register |
| PFPAR | — | SIM Port F Pin Assignment Register |
| PICR | — | SIM Periodic Interrupt Control Register |
| PITR | — | SIM Periodic Interrupt Timer Register |
| PORTC | — | SIM Port C Data Register |
| PORTE | — | SIM Port E Data Register |
| PORTF | — | SIM Port F Data Register |
| PORTQA | — | QADC Port A Data Register |
| PORTQB | — | QADC Port B Data Register |
| PORTQS | — | QSM Port QS Data Register |
| PQSPAR | — | QSM Port QS Pin Assignment Register |
| PRES DIV | — | TouCAN Prescaler Divide Register |
| PWM[5:8]C | — | CTM4 PWMSM Counter Registers [5:8] |
| PWM[5:8]A | — | CTM4 PWMSM Period Registers [5:8] |
| PWM[5:8]B | — | CTM4 PWMSM Pulse Width Registers [5:8] |
| PWM[5:8]SIC | — | CTM4 PWMSM Status/Interrupt/Control Registers [5:8] |
| QACR[0:1] | — | QADC Control Registers [0:2] |
| QADCINT | — | QADC Interrupt Register |
| QADCMCR | — | QADC Module Configuration Register |
| QADCTEST | — | QADC Test Register |
| QASR | — | QADC Status Register |



| | | |
|----------------|---|---|
| QILR | — | QSM Interrupt Level Register |
| QIVR | — | QSM Interrupt Vector Register |
| QSMCR | — | QSM Module Configuration Register |
| QTEST | — | QSM Test Register |
| RAMBAH | — | RAM Base Address High Register |
| RAMBAL | — | RAM Base Address Low Register |
| RAMMCR | — | RAM Module Configuration Register |
| RAMTST | — | RAM Test Register |
| ROMBAH | — | ROM Base Address High Register |
| ROMBAL | — | ROM Base Address Low Register |
| RR[0:F] | — | QSM Receive RAM |
| RSIGHI | — | ROM Signature High Register |
| RSIGLO | — | ROM Signature Low Register |
| ROMBS[0:3] | — | ROM Bootstrap Words [0:3] |
| RXGMSKHI | — | TouCAN Receive Global Mask High Register |
| RXGMSKLO | — | TouCAN Receive Global Mask Low Register |
| RX[14:15]MSKHI | — | TouCAN Receive Buffer [14:15] Mask High Registers |
| RX[14:15]MSKLO | — | TouCAN Receive Buffer [14:15] Mask Low Registers |
| RJURR[0:27] | — | QADC Right-Justified Unsigned Result Registers |
| RSR | — | SIM Reset Status Register |
| RXECTR | — | TouCAN Receive Error Counter Register |
| SCCR[0:1] | — | QSM SCI Control Registers [0:1] |
| SCDR | — | QSM SCI Data Register |
| SCSR | — | QSM SCI Status Register |
| SGLR | — | Service Grant Latch Register |
| SIMCR | — | SIM Module Configuration Register |
| SIMTR | — | SIM System Integration Test Register |
| SIMTRE | — | SIM System Integration Test Register (ECLK) |
| SPCR[0:3] | — | QSM QSPI Control Registers [0:3] |
| SPSR | — | QSM QSPI Status Register |
| SWSR | — | SIM Software Watchdog Service Register |
| SYNCR | — | SIM Clock Synthesizer Control Register |
| SYPCR | — | SIM System Protection Control Register |
| TICR | — | TPU Interrupt Configuration Register |
| TIMER | — | TouCAN Free Running Timer Register |
| TPUMCR | — | TPU Module Configuration Register |
| TR[0:F] | — | QSM Transmit RAM |



TRAMBAR — TPURAM Base Address Register
TRAMMCR — TPURAM Module Configuration Register
TRAMTST — TPURAM Test Register
TSTMSRA — SIM Test Module Master Shift Register A
TSTMSRB — SIM Test Module Master Shift Register B
TSTRC — SIM Test Module Repetition Counter Register
TSTSC — SIM Test Module Shift Count Register
TTR — TouCAN Test Register
TXECTR — TouCAN Transmit Error Counter Register

2.5 Conventions

Logic level one is the voltage that corresponds to a Boolean true (1) state.

Logic level zero is the voltage that corresponds to a Boolean false (0) state.

Set refers specifically to establishing logic level one on a bit or bits.

Clear refers specifically to establishing logic level zero on a bit or bits.

Asserted means that a signal is in active logic state. An active low signal changes from logic level one to logic level zero when asserted. An active high signal changes from logic level zero to logic level one.

Negated means that an asserted signal changes logic state. An active low signal changes from logic level zero to logic level one when negated. An active high signal changes from logic level one to logic level zero.

A specific mnemonic within a range is referred to by mnemonic and number. A15 is bit 15 of accumulator A; ADDR7 is line 7 of the address bus; CSOR0 is chip-select option register 0. **A range of mnemonics** is referred to by mnemonic and the numbers that define the range. VBR[4:0] are bits four to zero of the vector base register; CSOR[0:5] are the first six option registers.

Parentheses are used to indicate the content of a register or memory location rather than the register or memory location itself. (A) is the content of accumulator A. (M : M + 1) is the content of the word at address M.

LSB means least significant bit. **MSB** means most significant bit. References to low and high bytes are spelled out.

LSW means least significant word. **MSW** means most significant word.

ADDR is the address bus. ADDR[7:0] are the eight LSBs of the address bus.

DATA is the data bus. DATA[15:8] are the eight MSBs of the data bus.

