SECTION 21
CALRAM OPERATION

21.1 Definitions and Acronyms

- CALRAM — The module name for the calibration RAM
- L2U — The module name for the L-bus to U-bus interface unit
- USIU / SIU — Unified system integration unit / system integration unit
- READI — The module name for real-time embedded application development interface (READI)
- BIU — Bus interface unit
- Array — Array indicates the RAM array; this is sometimes used to distinguish from CALRAM internal registers.
- Reserved — Memory locations and register bit fields that are unimplemented. This term is used interchangeably with unimplemented register bit fields.
- Bus access — Synonymous with bus cycle and bus transaction. Refers to the sequence of events on a bus and are defined by a bus protocol.
- RCPU — RISC CPU
- MSR — Machine status register is a register which defines the state of the processor. This register resides in the RCPU core.
- PPC register — PowerPC^{TM} special purpose register (SPR) defined by the PowerPC^{TM} architecture
- Byte — Eight bits of data form a byte
- Half-word — 16 bits of data form a half-word
- Word —32 bits of data form a word
- Calibration — Calibration tuning in engine control is a means of optimization of parameters in real time. The parameters reside in the flash.
- RAM overlay — During calibration mode, it is necessary to change the data within the calibration data region. The calibration data resides in the flash, which makes it very difficult to change this data in normal operation. The concept of RAM overlay is that the portion(s) of CALRAM map to calibration data regions of the flash address space. Hence, when overlay is enabled, data for these regions are driven by the CALRAM rather than by the flash.
- One-cycle — Equivalent to one clock period (1/system clock frequency)
- Two-cycle — Equivalent to two clock periods (2/system clock frequency)
- Freeze mode — Special mode used during debug
- Supervisor/user — L-bus signal indicating whether an access is a supervisor (privileged access) or user access
- Data/instruction — L-bus signal indicating whether data read or instruction fetch
- Machine check/data storage interrupt — Type of exceptions that can be generated due to an access causing an error. See the ***RCPU Reference Manual (RCPURM/AD)*** for details.
- Hex address — Addresses in hexadecimal numbers unless otherwise stated

21.1.1 Key Feature List

Standard RAM features are listed below:

- One-clock accesses
- Byte, half-word (16-bits), or word (32-bit) read/write accesses
- Each 8-Kbyte block has individual protection control bits.
- Two-cycle access for power savings
- Low power standby operation for data retention

Special overlay features are:

- Eight overlay regions; each can be programmed to be four, 16, 32, 64, 128, 256, or 512 bytes long
- Each overlay region size can be forced to be of 4 bytes long
- Data driven from the CALRAM module for overly access has the same timing as the data that would have come from the U-bus flash
- Overlay is for data read from the U-bus flash space and does not affect instruction fetches from the flash
- Overlay block is naturally aligned
  — For example, 128-byte block is 128-byte aligned
- Normal access to overlaid portion of CALRAM array can be made to generate an error (machine check) if so configured

21.2 CALRAM Introduction

The calibration static random access memory (CALRAM) module provides the micro-controller unit (MCU) with a general purpose memory which may be read from or written to as either bytes, half-words, or words. In addition to this, a portion of the CAL-RAM called the overlay region can be used for calibration. Calibration in this context is defined as overlaying portions of the U-bus flash with a portion of the CALRAM array. During normal flash access, the PowerPC core reads data from U-bus flash (through L-bus and L2U), as shown in **Figure 21-1**. During calibration access, instead of flash providing the data, the overlay regions of CALRAM provide the data to the PowerPC core.

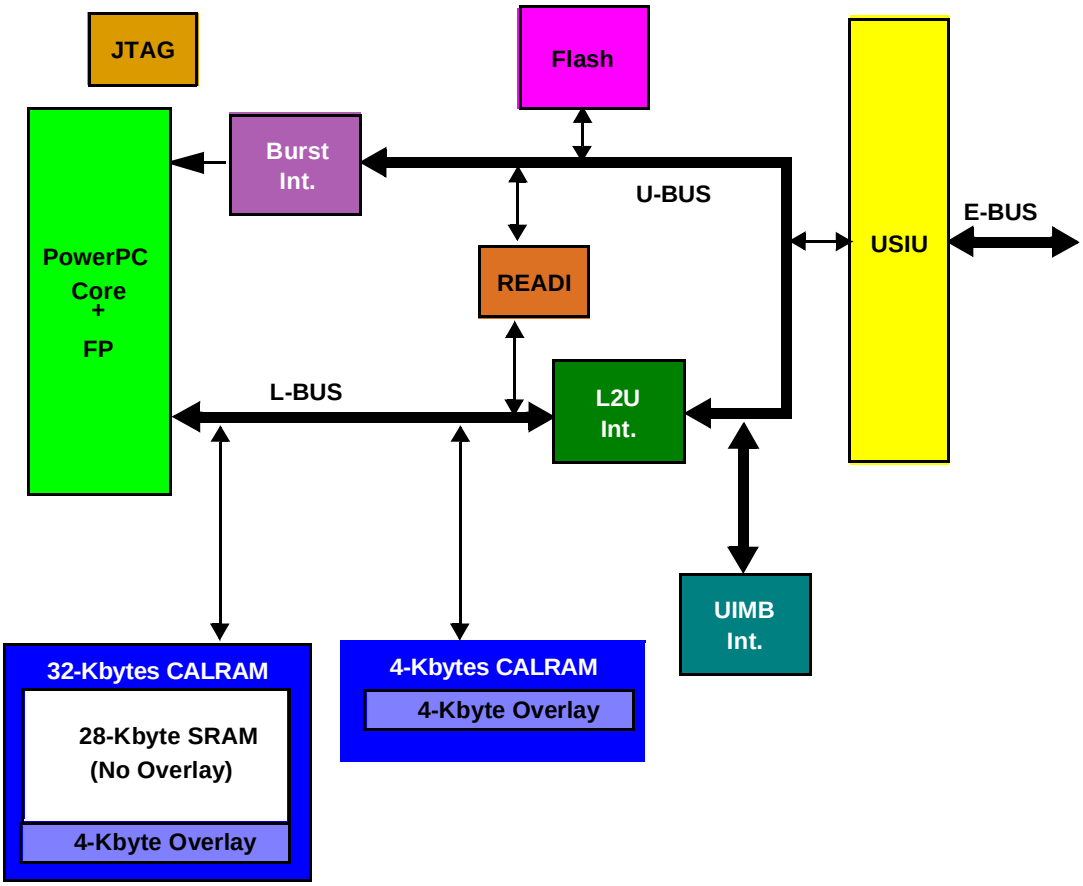

Figure 21-1 System Block Diagram

The MPC565 / MPC566 chip internal memory map is shown in **Figure 21-2**.

The internal memory block can reside in one of eight possible 4-Mbyte memory spaces. This 32-Mbyte (8 x 4-Mbyte) memory blocks starts at address 0x0000 0000. There is a user-programmable register (internal memory space (ISB) bits in internal memory map register (IMMR)) to configure the internal memory map to one of the eight possible locations. All addresses shown in this chapter are the default 4-Mbyte address from 0x00 0000 to 0x3F FFFF.

The CALRAM module is divided into two sections.

- Control section:
  — Includes all the registers in the CALRAM module
- Array sub-region:
  — Contains memory arrays

The MPC565 / MPC566 contains two CALRAM modules — one is a 32-Kbyte memory (at address 0x3F 8000 – 0x3F FFFF) and another is a 4-Kbyte memory (at address 0x3F 7000 – 0x3F 7FFF) as shown in **Figure 21-1** in and at address spaces shown in

Figure 21-2. In addition, each module is assigned 16 32-bit register address spaces — 12 registers are implemented and four registers are unimplemented. The 12 registers are-- one module configuration register (CRAMMCR), one register reserved for factory test, eight region base address (CRAM_RBAx) registers, one overlay configuration register (CRAMOVLCR), and one ownership trace register (CALRAM_OTR) to support a separate module called READI. Refer to **SECTION 23 READI MODULE**.

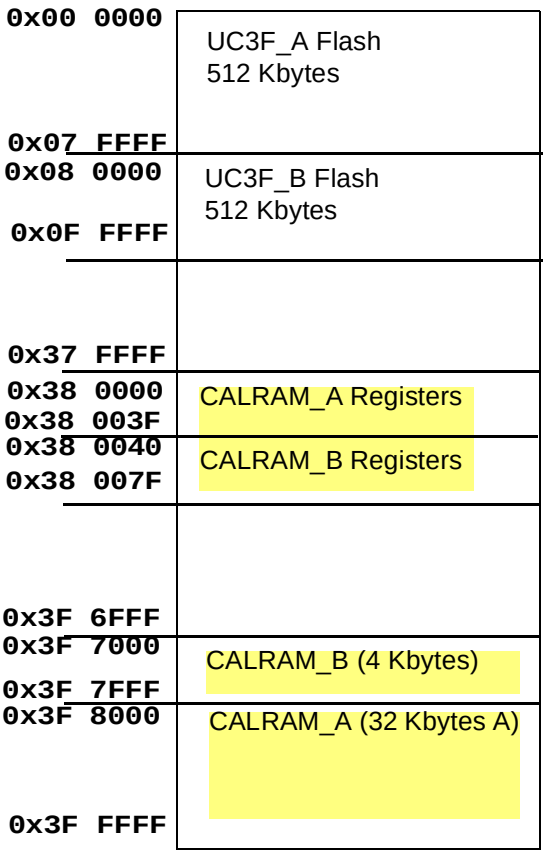

Figure 21-2 MPC565 / MPC566 Memory Map with CALRAM Address Ranges

When the normal chip power (VDD) is off, portions of the CALRAM array can be powered by separate power supply sources (VDDSRAM1/VDDSRAM2) as shown in **Figure 21-3**, thus allowing the data to be retained.

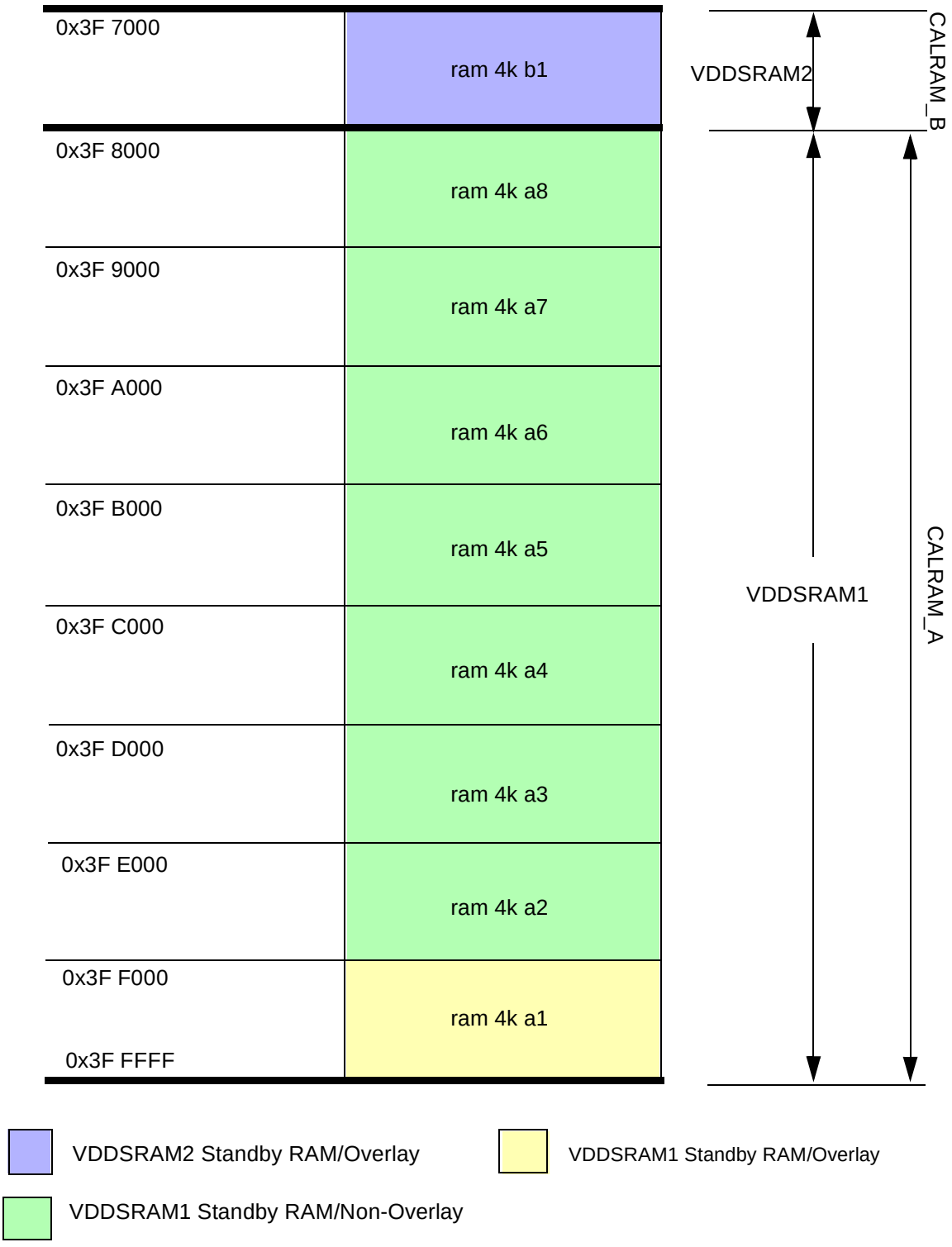

Figure 21-3 Standby Power Supply Configuration for CALRAM Array

21.3 Modes of Operation

The CALRAM module has the following modes of operation:

- Reset
- One-cycle
- Two-cycle
- Standby
- Stop
- Overlay

21.3.1 Reset

Reset configures the CALRAM module and resets some of the bits in the CALRAM registers to their default reset state. Some register bits are unaffected by reset. See section **21.4 Register Definitions**.

21.3.2 One-Cycle Mode

The CALRAM registers and array may be accessed for reads or writes as byte, (aligned) half-word, or word. This mode is the default mode of operation and, as the name suggests, the access time to the array and the internal registers for reads and writes is one cycle. Thus the one-cycle mode is used for high performance although it consumes more power than the two cycle mode.

21.3.2.1 CALRAM Access/Privilege Violations

Each 8-Kbyte CALRAM array can be assigned read-only, data-only, or supervisor-only privilege if data relocate (DR) bit in MSR is set. All CALRAM registers are assigned supervisor-only and data-only privilege. A privilege violation causes an error. See section **21.4.1 CALRAM Module Configuration Register (CRAMMCR)**.

Each CALRAM module can have up to 32 Kbytes of array. If less than 32 Kbytes of array are implemented in a CALRAM module, an attempt to access unimplemented portion of array causes an error. For example, if only four Kbytes of CALRAM_B implemented in MPC565 / MPC566, access to the remaining 28-Kbyte region of CALRAM_B causes an error; that is, any accesses to the array from 0x3F 0000 to 0x3F 6FFF end in an error. Each CALRAM module is allocated 16 register spaces among which only twelve registers are implemented. An attempt to access any of the four unimplemented reserved registers causes an error and returns 0’s on the data bus for a read access.

If an error condition occurs due to privilege violation or due to an attempt to access unimplemented portion of array or register space then the type of the error generated depends on whether the access generating the error was initiated by the RCPU core or by a non-RCPU bus master. If the error causing access was initiated by the RCPU core, a data storage interrupt (DSI) is generated. If the access was initiated by a non-RCPU bus master, a machine check exception is generated. Also, a write access that generates an error does not corrupt the data in an array or a register. Similarly, a read access that generates an error does not drive the data on the L-bus from the array or the register, instead it drives 0’s. Also, aborted accesses maintains data integrity —

aborted writes do not corrupt data in register/array, aborted reads do not drive the requested data on L-bus.

21.3.3 Two-Cycle Mode

In this mode, the CALRAM module takes two cycles to complete an access and the consumes less power than in one-cycle mode. It follows the normal one-cycle mode operation except that the accesses are completed one cycle later. This mode is selected by setting the 2CY bit in the CRAMMCR register.

21.3.4 Standby Operation / Keep-Alive Power

The registers and control logic for the CALRAM module is powered by VDD. The memory array(s) is also supplied by VDD during normal operation but when the VDD is off portions of CALRAM array is backed up by switched sources (VDDSRAM1/ VDDSRAM2) which are also known as standby power.

In the MPC565 / MPC566, when the VDD is off, the CALRAM arrays from 0x3F 8000 to 0x3F FFFF (32 Kbytes of CALRAM module A) and from 0x3F 7000 to 0x3F 7FFF (all four Kbytes of CALRAM module B) are powered by VDDSRAM1 and VDDSRAM2 respectively as shown in **Figure 21-3**.

21.3.5 Stop Operation

The low power stop mode for this module is entered by setting the disable bit (DIS) in the CRAMMCR register. Reads from and writes to the array during this mode will generate an error.

When the disable bit (DIS) is cleared, the module returns to normal function.

21.3.6 Overlay Mode Operation

For a microcontroller used as a controller for an engine (or other electromechanical device), various parameters stored in the flash memory may need to be changed in order to properly tune (calibrate) the engine. Since flash memory may not be readily programmed during normal operation of an embedded controller, this problem is solved by overlaying portions of CALRAM array onto the flash memory residing in U-bus. By allowing CALRAM module to overlay portions of flash memory, parameters normally stored in the flash may be tweaked and changed by development tool during normal operation and prior to programming a final version of the flash memory with more precise parameters.

The overlay is to read only data and does not affect instruction fetches from the flash. The data for any L-bus address which falls in the overlay region of the U-bus flash will be driven by the CALRAM on the L-bus. The CALRAM also indicates to the L2U to block the data from the flash to be driven on the L-bus. As far as the RCPU core is concerned, the timing of data coming from the CALRAM appears to be the same as that from the flash.

21.3.6.1 Overlay Mode Configuration

Each CALRAM module contains eight overlay regions, each of which is 512 bytes long as shown in **Figure 21-4**. All overlay regions of a module are contiguous **Figure 21-4** and each starts at the least significant address of the region and can increment all the way up to 512 bytes as shown in **Figure 21-5**. As described in section **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)**, CRAM_RBAx registers allow the programming of the base addresses RBA[11:29] of the U-bus flash regions and the RGN_SIZE[0:4] to be overlaid. Note that each region can also be individually disabled by writing 0000 to RGN_SIZE[0:3]. If the programmed base address is not naturally aligned with respect to the RGN_SIZE field, the least significant bits of the base address fields can be considered 0's in order to make the starting address naturally aligned. In an RBA register, RGN_SIZE[0:3] ={0101} select the size to be 128 bytes, and even if CRAM_RBAx [25:29] are not all 0's, they will be considered as 0's so that the address becomes 128-byte naturally aligned.

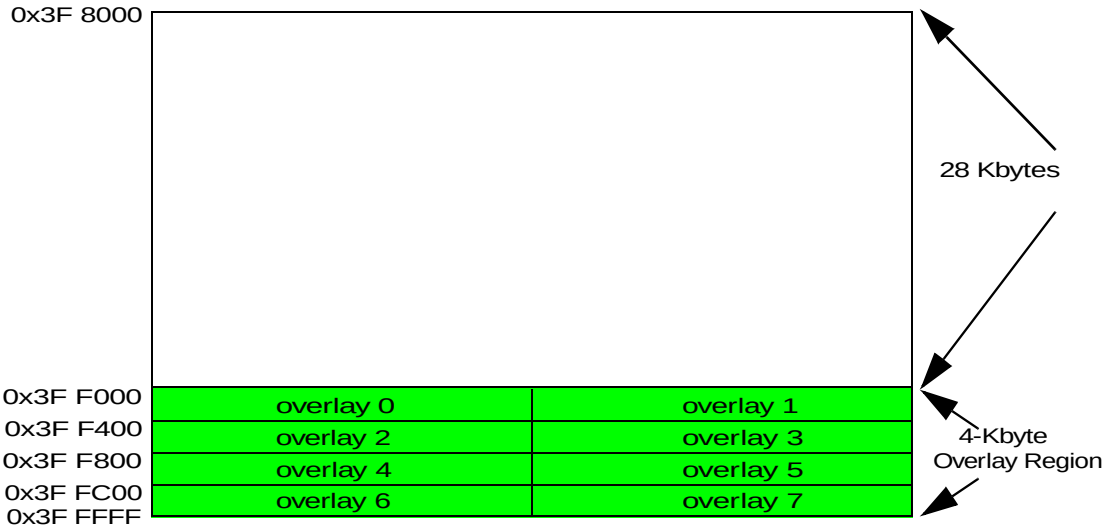

Figure 21-4 CALRAM_A array

When programming the CRAM_RBAx registers, the CALRAM can be put in overlay mode by setting the OVL bit in the CALRAM overlay configuration register (CRAMOVL) as described in section **21.4.3 CALRAM Overlay Configuration Register (CRAMOVLCR)**. For example, **Figure 21-5** shows that overlay regions 0, 4, and 5 have their entire region of 512 bytes mapped to regions in the flash as specified by CRAM_RBA0, CRAM_RBA4, and CRAM_RBA5. Overlay region 1 is partially mapped to a region in flash as specified by the CRAM_RBA1. For example, if the region size of 256 bytes is selected for overlay region 1, then the enabled portion of the overlay region 1 occupies array from 0x3F F200 to 0x3F F2FF. The rest of overlay region 1 from 0x3F F300 to 0x3F F3FF is available for normal (non-overlay) array access. Overlay regions 2, 3, 6, and 7 are disabled for overlay and hence can be used, in their entirety, for normal (non-overlay) array accesses.

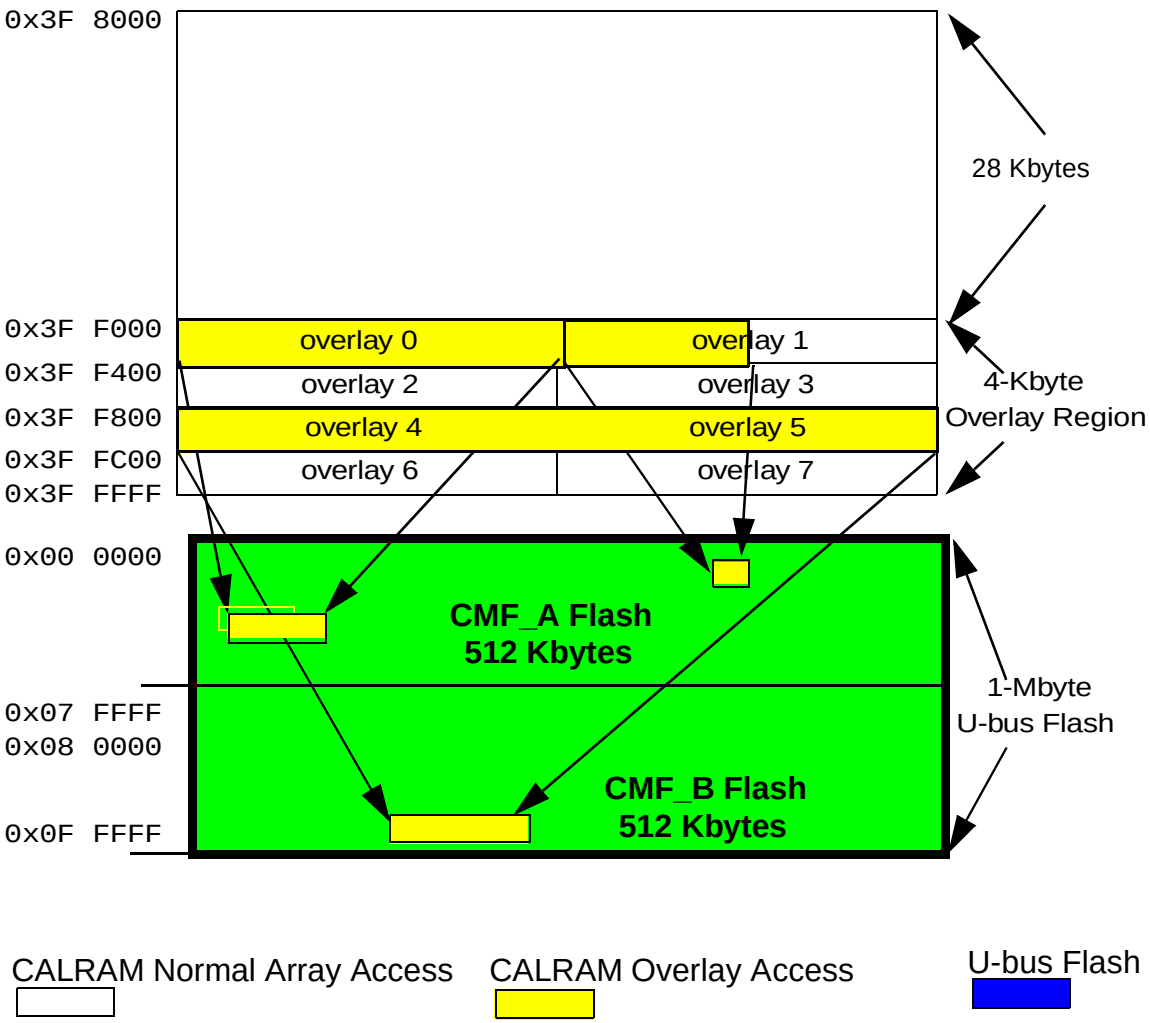

Figure 21-5 CALRAM_A Module Overlay Map of Flash (CLPS = 0)

Figure 21-6, illustrates the address spaces occupied by the two CALRAM modules available in MPC565 / MPC566.

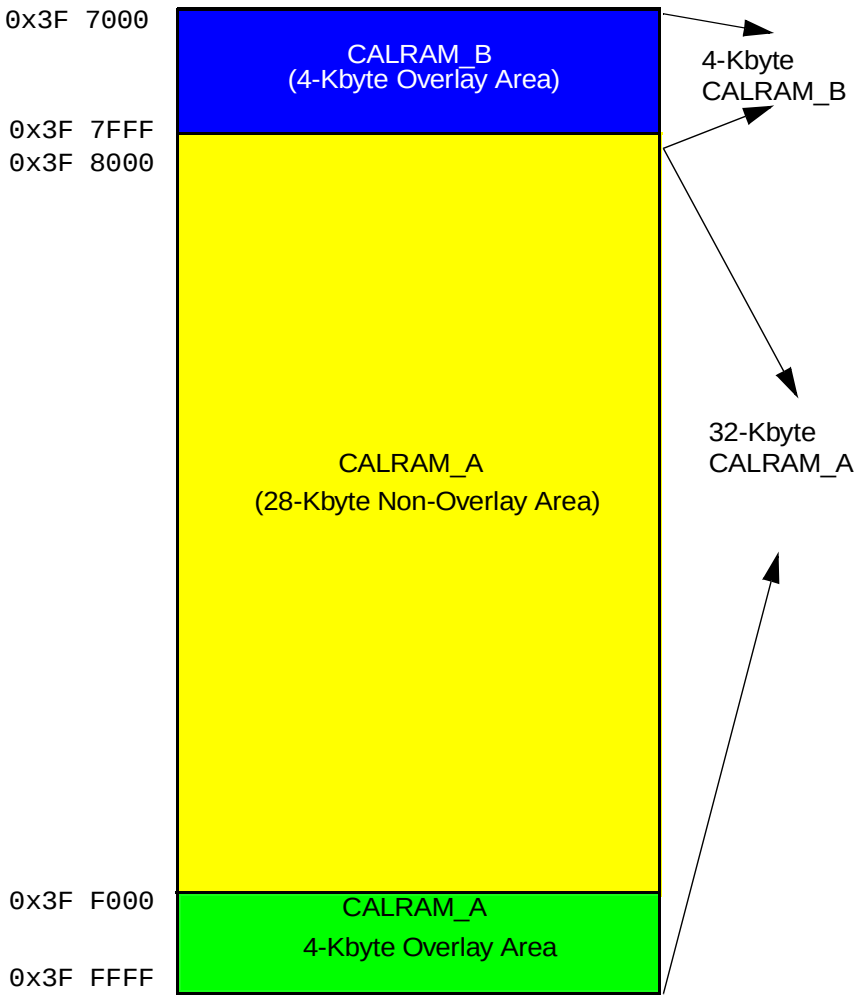

Figure 21-6 CALRAM_B and CALRAM_A Address Map (When CLPS = 0)

If the CLPS bit in OVLCR register is set, then each of the eight region size is forced to be 4 bytes long as shown in **Figure 21-7**,regardless of the value programmed in the RGN_SIZE field. These 32 bytes occupy contiguous address space in CALRAM_A, for example, from 0x3F FFE0 to 0x3F FFFF. The remainder (4 Kbytes – 32 bytes) is not only available for normal array access but also contiguous with a 28-Kbyte non-overlay array.

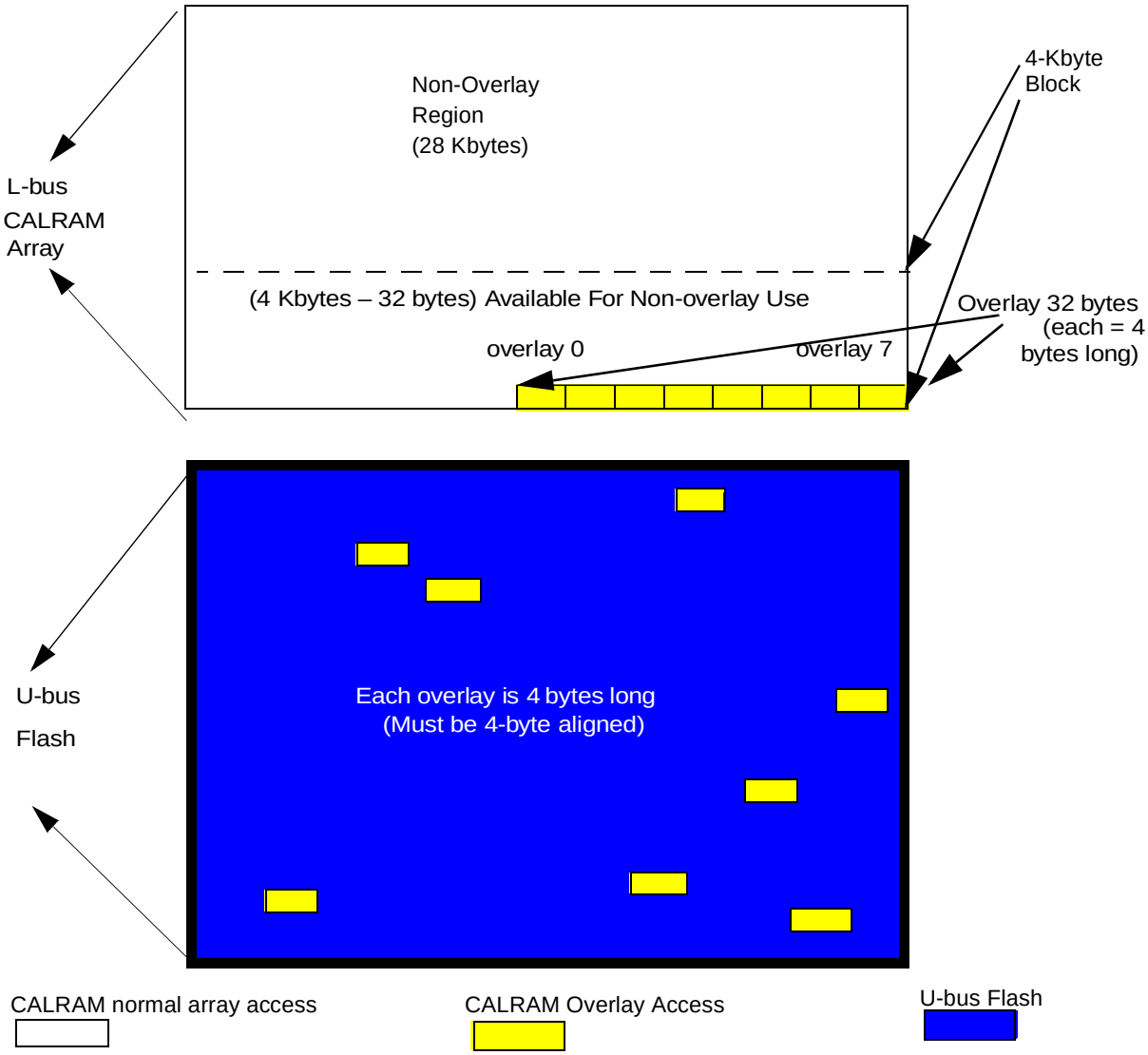

Figure 21-7 CALRAM Module Overlay Map of FLASH (CLPS = 1)

Figure 21-8 shows the overlay regions when the CLPS bit is set for both CALRAM_A and CALRAM_B in MPC565 / MPC566.

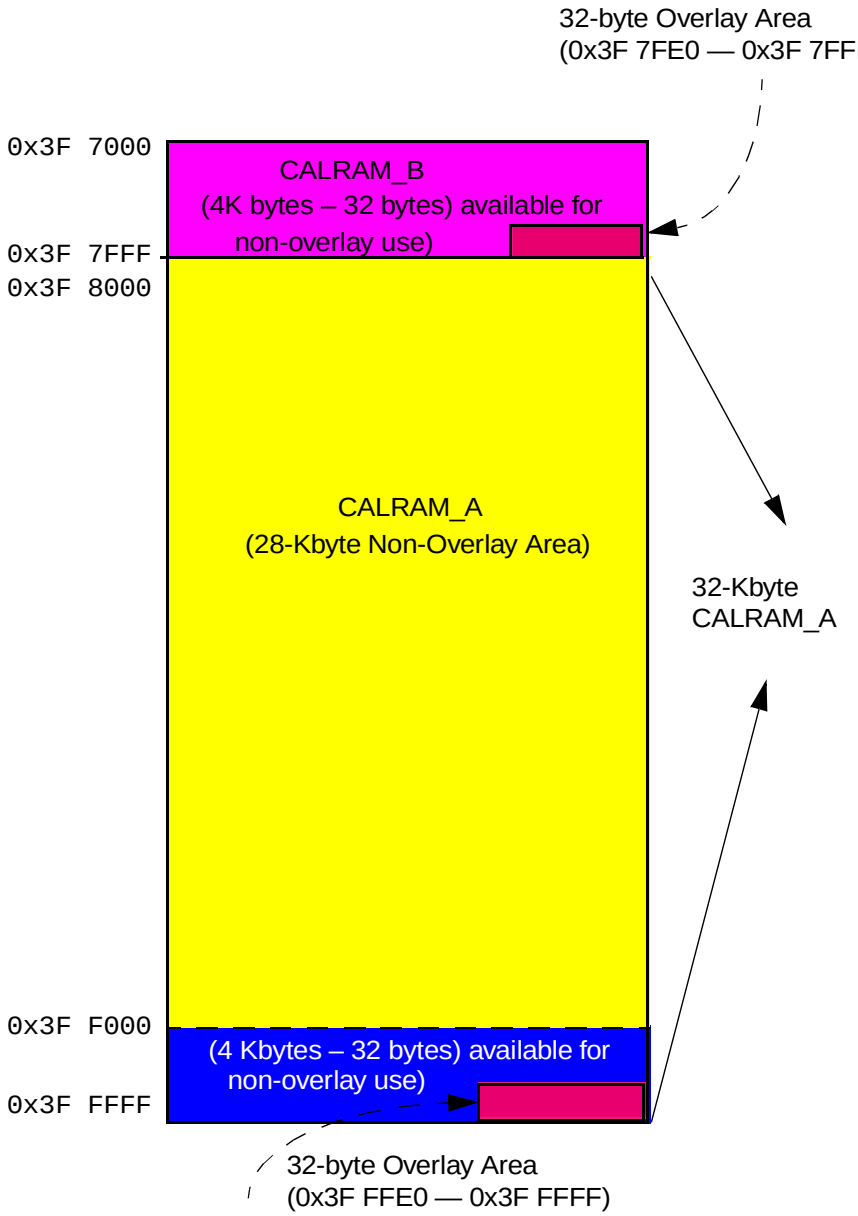

Figure 21-8 CALRAM_B and CALRAM_A Address Map (When CLPS = 1 for Both CALRAM_A and CALRAM_B)

NOTE

The values programmed in the RBAx registers are unaffected by reset. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for details. On reset, the it is not necessary to have to reprogram RABx registers. In such cases, the calibration mode can be re-entered simply by setting the OVL bit.

21.3.6.2 Priority of Overlay Regions

When the address matches to more than one enabled portion of the overlay region, the effective region is the region with the highest priority. Priority is determined by the region number; the highest priority assigned to the lowest region number. In an MCU with multiple CALRAM modules, the highest priority is assigned to the one in lowest address space (highest address).

EXAMPLE

In MPC565 / MPC566, region 0 of CALRAM_A has the higher priority and region 7 of CALRAM_B has the lowest priority as shown in **Table 21-1**. Also, region 7 of CALRAM_A has higher priority than region 0 of CALRAM_B.

The benefit from this priority feature is that by storing the parameters in eight overlay regions, it overlays all eight regions onto the same 512-byte flash region, and enables the overlay feature. Upon observing system performance with a set of parameters, the next set of parameters can be selected by simply disabling the highest priority region. This “observing and disabling the highest priority region” loop can continue until all regions are disabled. This allows moving from one set of parameters to another with minimal amount of reprograming efforts. If there are two CALRAM modules in a chip like in MPC565 / MPC566, then 16 sets of parameters can be run using this technique.

Table 21-1 Priorities of Overlay Regions

Module/Region Number	Priority
CALRAM_A/region 0	highest
CALRAM_A/region 1	.
CALRAM_A/region 2	.
CALRAM_A/region 3	.
CALRAM_A/region 4	.
CALRAM_A/region 5	.
CALRAM_A/region 6	.
CALRAM_A/region 7	.
CALRAM_B/region 0	.
CALRAM_B/region 1	.
CALRAM_B/region 2	.
CALRAM_B/region 3	.
CALRAM_B/region 4	.
CALRAM_B/region 5	.
CALRAM_B/region 6	.
CALRAM_B/region 7	lowest

21.3.6.3 Normal (Non-Overlay) Access to Overlay Regions

If overlay is enabled then any normal L-bus array access which falls within any of the eight enabled overlay regions, a machine check exception is generated if the option bit DERR is set in CRAMOVLCR register; otherwise, the access terminates normally

without asserting data error. The L-bus write accesses cause the data to be written regardless of whether DERR bit is set or not.

EXAMPLE

If overlay region 1 is programmed such that it is enabled and its region size is 256 bytes, then any L-bus access to address in the range of 0x3F F200 – 0x3F F2FF generates machine check exception if the DERR bit is set in CRAMOVLCR register. The other portion of region 1 from 0x3F F300 to 0x3F F3FF can be used as normal (non-overlay) array.

21.3.6.4 Calibration Write Cycle Flow

Write accesses to the overlaid U-bus flash regions are ignored completely by the CALRAM module.

21.4 Register Definitions

The following section describes the CALRAM programmer's model. The CALRAM has one register for configuring the CALRAM array and one register dedicated to factory test. In addition, there are eight 32-bit region base address registers for calibration purposes and a 32-bit overlay configuration register. The region base address registers hold the base address for the flash region and region size that need to be overlaid by the CALRAM. The overlay configuration register provides three bits (OVL, DERR, and CLSP) that are needed for overlay configuration. The CALRAM ownership trace register (CRAM_OTR) is provided to support a separate module called a READI module. Access to all CALRAM registers requires the bus master to be in supervisor data mode. On a privilege violation, the register is not accessed and the access generates an error.

Table 21-2 shows the register address map for MPC565 / MPC566.

Table 21-2 CALRAM A and B Control Registers

Address	Register
CALRAM_A	
0x38 0000	CRAMMCR_A
0x38 0004	for factory test
0x38 0008	CRAM_RBA0_A
0x38 000C	CRAM_RBA1_A
0x38 0010	CRAM_RBA2_A
0x38 0014	CRAM_RBA3_A
0x38 0018	CRAM_RBA4_A
0x38 001C	CRAM_RBA5_A
0x38 0020	CRAM_RBA6_A
0x38 0024	CRAM_RBA7_A
0x38 0028	CRAMOVLCR_A
0x38 002C	CRAMOTR_A
0x38 0030	Reserved
0x38 0034	Reserved
0x38 0038	Reserved
0x38 003C	Reserved
CALRAM_B	
0x38 0040	CRAMMCR_B
0x38 0044	for factory test
0x38 0048	CRAM_RBA0_B
0x38 004C	CRAM_RBA1_B
0x38 0050	CRAM_RBA2_B
0x38 0054	CRAM_RBA3_B
0x38 0058	CRAM_RBA4_B
0x38 005C	CRAM_RBA5_B
0x38 0060	CRAM_RBA6_B
0x38 0064	CRAM_RBA7_B
0x38 0068	CRAMOVLCR_B
0x38 006C	CRAMOTR_B
0x38 0070	Reserved
0x38 0074	Reserved
0x38 0078	Reserved
0x38 007C	Reserved

Any unimplemented bits in CALRAM registers return 0’s on a read and writes to these bits are ignored.

21.4.1 CALRAM Module Configuration Register (CRAMMCR)

The module configuration register (CRAMMCR) contains bits that allow the CALRAM to be configured for normal RAM accesses.

CRAMMCR — CALRAM Module Configuration Register

0x38 8040
0x38 8000

LSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MSB 15
LCK	DIS	2CY	Reserved												
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LSB 16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	MSB 31
Reserved				R0	D0	S0	R1	D1	S1	R2	D2	S2	R3	D3	S3
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A brief description of each bit is provided in **Table 21-3**:

Table 21-3 CRAMMCR Bit Descriptions

Bit(s)	Name	Description
0	LCK	Write protection — This bit is designed to lock out writes to the CRAMMCR. While LCK = 0 the register can be written repeatedly without restriction. If LCK = 1, the register does not accept writes (i.e., the value of the register remains unchanged, but the cycle terminates normally.) In normal mode, this bit can only be set once and can only be cleared by reset 0 = writes to the CRAMMCR are unrestricted 1 = writes to the CRAMMCR are ignored In freeze mode, only the LCK bit may be written to zero if it was previously set.
1	DIS	Array disable — When set, this bit disables the CALRAM array. In this mode, all reads and writes to the CALRAM array are ignored and a bus error is generated. The CALRAM responds to register access while DIS = 1. This is a low power mode for the module, since all internal functions will be disabled. The module can be re-enabled by writing the DIS bit back to a zeroReset will also re-enable the module. 0 = CALRAM module array access is enabled 1 = CALRAM module array access is disabled
2	2CY	Two cycle mode — When set, this bit puts the CALRAM into a two cycle access mode operation for CALRAM register accesses as well as array accesses. This mode provides power savings by using the first cycle to decode any L-bus access for an address match to where the array resides. 0 = CALRAM module in one-cycle operation 1 = CALRAM module in two-cycle operation
3:19	—	Reserved

Table 21-3 CRAMMCR Bit Descriptions (Continued)

Bit(s)	Name	Description
20	R0	Read-only/read-write privilege — If the data relocate (DR) bit is set in Machine Status Register (MSR in RCPU) and R0 is also set, then write accesses are terminated with an error. If DR bit is 0, both reads and writes to the array block is allowed regardless of the value programmed in R0. This bit controls the highest 8-Kbyte block (lowest address) of CALRAM in the associated array. Likewise, R1, R2, and R3 control three other 8-Kbyte blocks in the same manner. See **Table 21-4** for control bit address ranges. R0 = 0 and DR = 0 readable and writable (array 8-Kbyte block) R0 = 0 and DR = 1 readable and writable (array 8-Kbyte block) R0 = 0 and DR = 0 readable and writable (array 8-Kbyte block) R0 = 1 and DR = 1 read only (array 8-Kbyte block)
21	D0	Data-only/data-instruction privilege (Data type assignment) — If the data relocate (DR) bit is set in Machine Status Register (MSR) and D0 is also set, then any access attempting to fetch an instruction from the array block generates an error. If DR bit is 0, both data read and instruction fetch from the array block is allowed, regardless of the value programmed in D0. This bit controls the highest 8-Kbyte block (lowest address) of CALRAM in the associated array. Likewise, D1, D2, and D3 control three other 8-Kbyte blocks in the same manner. See **Table 21-4** for control bit address ranges. D0 = 0 and DR = 0 data and/or Instruction (array 8-Kbyte block) D0 = 0 and DR = 1 data and/or Instruction (array 8-Kbyte block) D0 = 0 and DR = 0 data and/or Instruction (array 8-Kbyte block) D0 = 1 and DR = 1 data only (array 8-Kbyte block)
22	S0	Supervisor-only/supervisor-user privilege (Space assignment) — If the data relocate (DR) bit is set in Machine Status Register (MSR) and S0 is also set, then any access to the array block by a user program generates an error. If DR bit is 0, both user and supervisor program can access the array block, regardless of the value programmed in S0. The CALRAM array may be placed in supervisor or unrestricted space. This bit controls the highest 8-Kbyte block (lowest address) of CALRAM in the associated array. Likewise, S1, S2, and S3 control other three blocks in the same manner. See **Table 21-4** for control bit address ranges. S0 = 0 and DR = 0 both user and supervisor access allowed (array 8-Kbyte block) S0 = 0 and DR = 1 both user and supervisor access allowed (array 8-Kbyte block) S0 = 0 and DR = 0 both user and supervisor access allowed (array 8-Kbyte block) S0 = 1 and DR = 1 only supervisor access allowed (array 8-Kbyte block)
23	R1	Same as R0 except for address ranges shown on **Table 21-4**.
24	D1	Same as D0 except for address ranges shown on **Table 21-4**.
25	S1	Same as S0 except for address ranges shown on **Table 21-4**.
26	R2	Same as R0 except for address ranges shown on **Table 21-4**.
27	D2	Same as D0 except for address ranges shown on **Table 21-4**.
28	S2	Same as S0 except for address ranges shown on **Table 21-4**.
29	R3	Same as R0 except for address ranges shown on **Table 21-4**.
30	D3	Same as D0 except for address ranges shown on **Table 21-4**.
31	S3	Same as S0 except for address ranges shown on **Table 21-4**.

Table 21-4 CRAMMCR Privilege Bit Assignment for 8-Kbyte Array Blocks

Bit Selection	Address Block (Relative)
R0, D0, and S0	0xXXXX 0000 – 0xXXXX 1FFF
R1, D1, and S1	0xXXXX 2000 – 0xXXXX 3FFF
R2, D2, and S2	0xXXXX 4000 – 0xXXXX 5FFF
R3, D3, and S3	0xXXXX 6000 – 0xXXXX 7FFF

Since only a 4-Kbyte array is implemented in CALRAM_B module in MPC565 / MPC566, note that R3, D3, and S3 provide the privilege bits for the array from 0x3F 7000 to 0x3F 7FFF.

21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)

The region base address register defines the base address of a region on the U-bus flash memory space that will be overlaid by a portion of the CALRAM memory space and the region size. Since eight such regions in the flash can be overlaid by the CAL-RAM, eight such registers (x = 0, 1, 2, ., 7) are provided.

The CRAM_RBAx[11:29] provides the base address (starting address) of the of the U-bus flash region to be overlaid and the CRAM_RBAx[0:3] provides size corresponding to the region. See **Table 21-6** for details. The RGN_SIZE[0] is reserved and should never be programmed to a one. Since MPC565 / MPC566 has only one Mbyte of flash, CRAM_RBAx[11] should never be programmed to a one. Also, note that if CLPS bit in CRAMOVLCR is set, each of the eight sizes are forced to be four bytes, regardless of the value programmed in RGN_SIZE[0:3] field. See **21.4.3 CALRAM Overlay Configuration Register (CRAMOVLCR)** for details.

The implemented bits of CRAM_RBAx bits are, indeed, unaffected by reset (hard reset). The diagram below shows one such registers, CRAM_RBA0 which provides the base address of overlay region 0.

CRAM_RBA0-7 — CALRAM Region Base Address Register **0x38 0048 — 0x38 0064**
0x38 0008 — 0x38 0024

LSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MSB 15
RGN_SIZE				RESERVED							RBA				
HARD RESET:															
X[1]	X	X	X	0	0	0	0	0	0	0	X	X	X	X	X

LSB 16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	MSB 31
RBA														RESERVED	
HARD RESET:															
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0

NOTES:
1. Reset (hard reset) does not affect the values of these bits.

Table 21-5 CRAMMCR Bit Descriptions

Bit(s)	Name	Description
0:3	RGN_ SIZE	These bits define the size of the overlay region. See **Table 21-5** for sizes.
4:10	—	Reserved
11:29	RBA	The Region Base Address defines the starting address of the memory to be overlayed.
30:31	—	Reserved

Table 21-6 RGN_SIZE Encoding

RGN_SIZE	Number of Overlay Bytes
0000	Overlay block disabled
0001	Overlay block is 4 bytes
0010	Overlay block is 16 bytes
0011	Overlay block is 32 bytes
0100	Overlay block is 64 bytes
0101	Overlay block is 128 bytes
0110	Overlay block is 256 bytes
0111	Overlay block is 512 bytes
1000	Reserved
1001	Reserved
1010	Reserved
1011	Reserved

Table 21-6 RGN_SIZE Encoding

RGN_SIZE	Number of Overlay Bytes
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

NOTE

The overlay size of eight bytes cannot be selected.

21.4.3 CALRAM Overlay Configuration Register (CRAMOVLCR)

CRAMOVLCR — CALRAM Overlay Configuration Register **0x38 0068**
0x38 0028

LSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MSB 15
OVL	DERR	CLPS	Reserved												
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LSB 16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	MSB 31
Reserved															
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21-7 CRAMOVLCR Bit Descriptions

Bit(s)	Name	Description
0	OVL	Overlay enable — When set, the CALRAM overlay mode operation is enabled. In this mode CALRAM allows eight programmable sections (four to 512 bytes) of the on-chip U-bus flash memory module to be overlaid by sections of the CALRAM. 0 = CALRAM module overlay is disabled 1 = CALRAM module overlay is enabled
1	DERR	Data error 0 = CALRAM module will not generate machine check exception due to normal L-bus array access to the enabled portion overlay region even if overlay is enabled 1 = CALRAM module will generate machine check exception due to normal L-bus array access to the enabled portion of overlay region even if overlay is enabled
2	CLPS	Collapse the total overlay region from 4 Kbytes to 32 bytes; that is, the size is forced to be four bytes for each for the eight regions regardless of the values programmed in CRAM_RBAx[0:3]; these bits are also referred to as RGN_SIZE[0:3]. 0 = Overlay region of four Kbytes; region size as specified by CRAM_RBAx[0:3]. 1 = Overlay region of 32 bytes; each region size is four bytes long regardless of the valuesin CRAM_RBAx[0:3].
3:31	—	Reserved

21.4.4 CALRAM Ownership Trace Register (CRAMOTR)

This register is provided to support a separate module called READI. Refer to **SECTION 23 READI MODULE**.

The reads from this register will return 0's.

NOTE

CRAMOTR_A is also defined as READI_OTR. See **23.2.1.1 User Mapped Register**. CRAMOTR_B is not used on the MPC565 / MPC566.

CRAMOTR — CALRAM Ownership Trace Register **READI_OTR 0x38 006C**
CRAMOTR_B 0x38 002C

LSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MSB 15
Ownership Trace Register															
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LSB 16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	MSB 31
Ownership Trace Register															
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0