SECTION 1
OVERVIEW

The purpose of this section is to give an overview of the MPC565 / MPC566 part, including the features, module mix, pins, address map, package, and electrical characteristics. The module mix of the part is shown in the block diagram and the text.

The remaining sections of the document describe the modules which are used on the chip. The MPC565 / MPC566 has duplicates of several modules, including TPU3, TouCAN, QSMCM, QADC64, CALRAM, UC3F, DPTRAM.

1.1 Introduction

The MPC565 / MPC566 is a member in the Motorola MPC500 PowerPC™ RISC Microcontroller family. As shown in **Figure 1-1**, it is composed of:

— A PowerPC core with FPU and BBC
— 36 Kbytes of static RAM (two CALRAM modules)
  • Eight Kbytes of normal access or overlay access (sixteen 512-byte regions)
    — (four Kbytes in CALRAM_A, four Kbytes in CALRAM_B)
— One Mbyte of flash memory (UC3F)
— Unified system integration unit (USIU), a flexible memory controller, an improved interrupt controller
— Three time processor units (TPU3)
  • TPU3_A and TPU3_B are connected to DPTRAM_AB (six Kbytes)
  • TPU3_C is connected to DPTRAM_C (four Kbytes)
— A 22-timer channel modular I/O system (MIOS14)
  • Same as MIOS1 plus a real-time clock sub-module (MRTCSM), four counter sub-modules (MCSM), and four PWM sub-modules (MPWMSM)
— Three TouCAN modules (TOUCAN_A, TOUCAN_B, TOUCAN_C)
— Two enhanced queued analog system (QADC64E_A, QADC64E_B) with analog multiplexors (AMUX) for 40 total analog channels. These modules are configured so each module can access all 40 of the analog inputs to the part.
— Two queued serial multi-channel module (QSMCM_A, QSMCM_B), each of which contains a queued serial peripheral interface (QSPI) and two serial controller interfaces (SCI/UART)
— A J1850 (DLCMD2) communications module
— A NEXUS debug port (class 3) – IEEE-ISTO 5001-1999
— JTAG and background debug mode (BDM)

1.2 Block Diagram

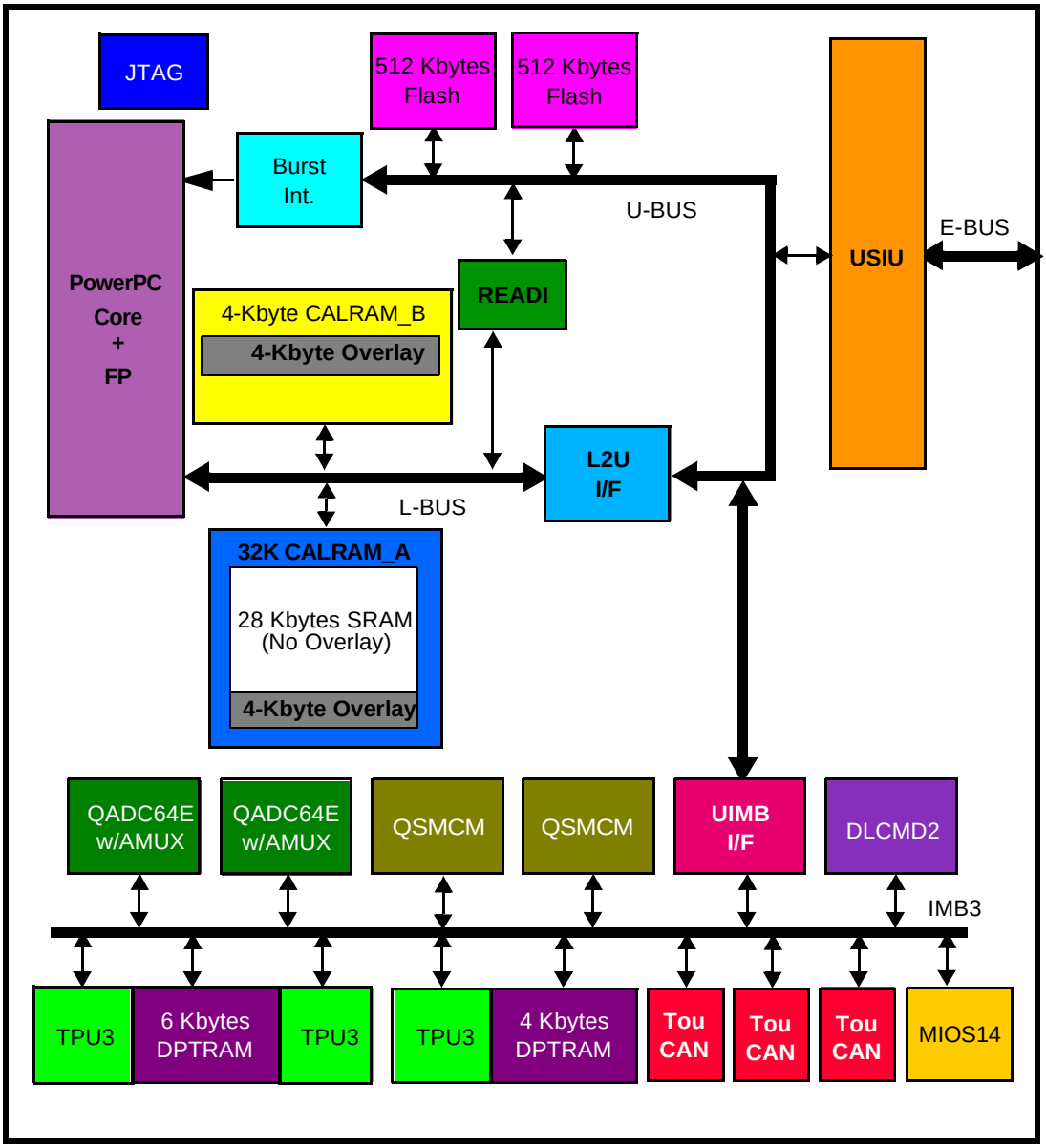

Figure 1-1 MPC565 / MPC566 Block Diagram

1.2.1 Detailed Feature List

The MPC565 / MPC566 key features are as follows. The information inside boxes are optional features.

- 40 MHz / 56 MHz operation
- 56 MHz operation is available as an option.
  - — -40° – 125° C ambient temperature

- 2.6 V ± 0.1 V external bus
  - External bus is compatible with external memory devices operating from 2.5 V to 3.4 V.
  - Extended voltage range (2.7 – 3.4 V) degrades data drive timing by 1.1 ns on date writes.
- 2.6 ± 0.1 V internal logic
- 5-V I/O (5.0 ± 0.25 V)

• High performance CPU system

- High performance core
  - PowerPC single issue integer core
  - Precise exception model
  - Floating point
  - Code compression supported on the MPC566
    - Compression reduces usage of internal or external flash memory
    - Compression optimized for automotive (non-cached) applications
    - New compression scheme increases compression performance to 40% – 50% compression
    - 4-Kbyte static DECRAM can be used as memory if Compression is not used.
  - Extensive system development support
    - On-chip watchpoints and breakpoints
    - Program flow tracking
    - Background debug mode (BDM)
- MPC500 PowerPC system interface (USIU, BBC, L2U)
  - Periodic interrupt timer, bus monitor, clocks, decrementer and time base
  - Clock synthesizer, power management, reset controller
  - External bus tolerates 5-V inputs, provides 3.3-V outputs
  - Enhanced interrupt controller supports a separate interrupt vector for up to eight external and 40 Internal interrupts
  - IEEE 1149.1 JTAG test access port
  - Bus supports multiple master designs
  - Flexible memory protection units in BBC (IMPU) and L2U (DMPU)
  - Flexible chip selects via memory controller
    - 24-bit address and 32-bit data buses
    - Four- to 16-Mbyte (data) or 4-Gbyte (instruction) region size support
    - Four-beat transfer bursts, two-clock minimum bus transactions
    - Use with SRAM, EPROM, flash and other peripherals
    - Byte selects or write enables
    - 32-bit address decodes with bit masks
    - Four instruction regions
    - Four data regions
  - Default attributes available in one global entry
  - Attribute support for speculative accesses
  - Exception vector table relocation features allow exception table to be relocated to following locations:
    - 0x0000 0100 (normal PowerPC exception table location)
    - 0x0001 0000 (0 + 64 Kbytes; second page of internal flash)

- — Second internal flash module
- — Internal SRAM
- — 0x0FFF_0100 (external memory space; normal PowerPC exception table location)
  - USIU supports dual-mapping of flash to move part of internal flash memory to external bus for development

— Fully static design

— Four major power saving modes
- On, doze, nap and sleep

— One Mbyte flash
- Two UC3F modules, 512 Kbytes each
- Page mode read
- Block (64-Kbyte) erasable
- External 4.75- to 5.25-V V_{PP} program and erase power supply

— 36-Kbyte static RAM (CALRAM)
- Composed of four- and 32-Kbyte CALRAM modules
- Fast access: one clock
- Keep-alive power
- Soft defect detection (SDD)
- 4-Kbyte calibration (overlay) RAM per module (eight Kbytes total)
- Eight 512-byte overlay regions per module (16 regions total)

— NEXUS/GEPDIS/IEEE – ISTO 5001-1999 debug port (Class 3)
- Nine- or 16-pin interface

— General purpose I/O support
- Address (24) and data (32) pins can be used as GPIO in single chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 5-V outputs with slew rate control

• Integrated I/O System

— True 5-V I/O

— Three time processing units (TPU3)
- 16 channels each
- Each TPU3 is a microcoded timer subsystem
- One 6-Kbyte and one 4-Kbyte dual port TPU RAM (DPTRAM), one (6-Kbyte) shared by two TPU3 modules for TPU microcode and the 4-Kbyte dedicated to the third TPU3 for microcode.

— 22-channel MIOS timer (MIOS14)
- Six modulus counter sub-module (MCSM)
  - — Four additional MCSM submodules compared to MIOS1
- 10 double action sub-module (DASM).
- 12 dedicated PWM sub-modules (PWMSM)
  - — Four additional PWM submodules compared to MIOS1 (shared with MIOS GPIO pins)
- Real-time clock sub-module (MRTCSM) provides low power clock/counter
  - — Requires external 32-KHz crystal
  - — Uses four pins: two for 32-KHz crystal, two for power/ground.

— Two queued analog-to-digital converter modules (QADC64E_A, QADC64E_B) with AMUXes providing a total of 40 analog channels.
  - 40 total input channels on the two modules with internal multiplexing (AMUXes)
  - Each QADC64E can see all 40 input channels
  - 10 bit A/D converter with internal sample/hold
  - Typical conversion time is 4 µs (250-Kbyte samples/sec)
  - Two conversion command queues of variable length
  - Automated queue modes initiated by:
    - — External edge trigger/level gate
    - — Software command
    - — Periodic/interval timer, assignable to both queue 1 and 2
  - 64 result registers in each QADC64E module
  - Synchronized clock mode allows both QADC64Es to see the same conversion clock. This allows the two modules to look like one large QADC with four queues.
  - Conversions alternate reference (ALTREF) pin. This pin can be connected to a different reference voltage
  - Output data is right or left justified, signed or unsigned

— Message data link controller (DLCMD2) module
  - Two pins muxed with QSMCMB pins. Muxing controlled by QSMCMB PCS3 pin assignment register
  - SAE J1850 Class B data communications network interface compatible and ISO compatible for low-speed (≥125 Kbps) serial data communications in automotive applications
  - 10.4 Kbps variable pulse width (VPW) bit format
  - Digital noise filter, collision detection
  - Hardware cyclical redundancy check (CRC) generation and checking
  - Block mode receive and transmit supported
  - 4X receive mode supported (41.6 Kbps)
  - Digital loopback mode
  - In-frame response (IFR) types 0, 1, 2, and 3 supported
  - Dedicated register for symbol timing adjustments
  - Inter-module bus 3 (IMB3) slave interface
  - Power-saving IMB3 stop mode with automatic wakeup on network activity
  - Power-saving IMB3 CLOCKDIS mode
  - Debug mode available through IMB3 FREEZE signal or user controllable SOFT_FRZ bit
  - Polling and IMB3 interrupt generation with vector lookup available

— Three TouCAN™ modules (TOUCAN_A, TOUCAN_B, TOUCAN_C)
  - 16 message buffers each, programmable I/O modes
  - Maskable interrupts
  - Programmable loop-back for self test operation
  - Independent of the transmission medium (external transceiver is assumed)
  - Open network architecture, multimaster concept
  - High immunity to EMI
  - Short latency time for high-priority messages

- Low power sleep mode, with programmable wake up on bus activity
- TOUCAN_C pins shared with MIOS14 GPIO pins

— Two queued serial modules with one queued-SPI and two SCI each (QSMCM_A, QSMCM_B)
- QSMCM_A matches full MPC555/MPC556 QSMCM functionality
- QSMCM_B has pins muxed with DLCMD2 module
  - — Two pins are muxed with DLCMD2 (J1850) transmit and receive pins (B_PCS3_J1850_TX and B_RXD2_J1850_RX)
  - — QSMCM_B vs J1850 mux control provided by QPAPCS3 bit in QSMCM pin assignment register (PQSPAR)
- Queued-SPI
  - — Provides full-duplex communication port for peripheral expansion or inter-processor communication
  - — Up to 32 preprogrammed transfers, reducing overhead
  - — Synchronous serial interface with baud rate of up to system clock / 4
  - — Four programmable peripheral-selects pins support up to 16 devices
  - — Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
  - — UART mode provides NRZ format and half- or full-duplex interface
  - — 16 register receive buffer and 16 register transmit buffer on one SCI
  - — Advanced error detection, and optional parity generation and detection
  - — word length programmable as eight or nine bits
  - — Separate transmitter and receiver enable bits, and double buffering of data
  - — Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received
  - — External source clock for baud generation

- Available in package or bumped die

— Plastic ball grid array (PBGA) packaging
  - — 352/388 ball PBGA
  - — 27 mm x 27 mm body size
  - — 1.0 mm ball pitch

1.2.1.1 MPC565 / MPC566 Optional Features

The following features of the MPC565 / MPC566 are optional features and may not appear in certain configurations:

- 56-MHz operation (40-MHz is default)
- MPC566 supports code compression

1.2.1.2 Supporting Documentation List

This list contains references to currently available and planned documentation.

- RCPU

— ***RCPU Reference Manual*** (RCPURM/AD)
- NEXUS Standard Specification Rev 1.0 (IEEE-ISTO 5001-1999)

— NEXUS Web Site: ***http://www.ieee-isto.org/Nexus5001/***

- JTAG

— IEEE 1149.1 Specification

1.2.2 Module or Mode Descriptions

1.2.2.1 Comparison of MPC565 / MPC566 and MPC555 / MPC556

The MPC565 / MPC566 is a derivative of the MPC555 / MPC556. Most functional features of the MPC555 / MPC556 are unchanged on the MPC565 / MPC566. **Table 1-1** shows the high level differences.

Table 1-1 Differences Between MPC555 / MPC556 and MPC565 / MPC566

MODULE	MPC555 / MPC556	MPC565 / MPC566
CPU Core	Identical	
BBC	BBC	BBC w/Improved Code Compression[1]
L2U	Identical	
SRAM	26 Kbytes	36-Kbyte CALRAM with Overlay features
Flash	448-Kbyte CMF	1-Mbyte UC3F (New Programming, etc.)
USIU	USIU	USIU w/Enhanced Interrupt Controller
JTAG	Identical	
READI	None	New Module
UIMB	Identical	
QADC64	2 QADC64 (16 channels on each QADC for 32 total channels)	2 QADC64E w/AMUXes (40 channels accessible from either QADC64E)
QSMCM	(1) Identical (2)	
DLCMD2 (J1850)	None	1
MIOS	MIOS1	MIOS14: MIOS1 with Real-Time Clock (MRTCSM), 4 more PWMSMs and 4 more MCSMs
TouCAN	(2) Identical (3)	
TPU3	(2) Identical (3)	
DPTRAM	(6 Kbytes) Identical (6 Kbytes, 4 Kbytes)	
Power Supplies		
—	40 MHz with two power supplies: nominal 3.3-V to 5.0-V power supplies	56 MHz with two power supplies: 5.0-V I/O, 2.6-V internal logic

NOTES:
1. Available on some options.

1.2.2.2 Additional MPC565 / MPC566 Differences

The following are detailed differences between the MPC565 / MPC566 and the MPC555 / MPC556.

- SPI (MISO, MOSI and SCK) pin drive.
  - — MPC565 / MPC566 provides 21-ns rise/fall with 200-pf load using CMOS (20%/70%) levels
- GPIO on MODCK1 pin outputs only 2.6 V
  - — MODCK1 pin is in keep-alive power section with no 5-V rail available
  - — 5.0-V compatibility modes
    - Input is 5-V friendly
    - 2.6-V output has less slew rate control
    - 2.6-V bus VOH = 2.3 V
- Power supplies for external bus pins
  - — QVDDL is quiet supply to hold non-switching outputs quiet even when noisy supply (NVDDL) sags
  - — QVDDL supplies pre-drive and other pad logic
  - — NVDDL only supplies final PMOS driver stage
  - — QVDDL and NVDDL shorted on customer board after filtering
- Pull-up and pull-down changes during $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$
  - — All 2.6-V/5-V pads (ext. bus: addr/data/control) pull down at reset
  - — All 5-V pads pull up at reset
  - — Additional control granularity in the PDMCR register
- No pull-ups on QSMCM SCI receive pads
- A_RXD1_QGPI1, A_RXD2_QGPI2, B_RXD1_QGPI1 pins do not have weak pull-up during reset or any other time
- CLKOUT has 3 drive strength options
  - — Better matches drive to requirements to reduce EMI
  - — 25, 50, 100 pf instead of 45 and 90 pf
- Change reset value of ENGCLK to maximum divide (crystal/128)
  - — For a 4-MHz crystal, this is 31.25 kHz
    - ENGCLK is selectable between 2.6 V and 5 V
- A daisy chain between UC3F modules allows either module to provide the reset configuration word (RCW)
- Censorship operation:
  - — An RCW bit controls whether or not the entire C3F can be erased while censorship is violated
- BBC SPRs (PPC regs) access in two clocks instead of one clock
- CALRAM internal protection block size is eight Kbytes
  - — Instead of four Kbytes on MPC555/MPC556 LRAM
- CALRAM causes machine check exception instead of data storage interrupt (DSI) exception in certain cases
  - — For non-overlay CPU core accesses, a DSI exception is taken
  - — For overlay accesses and any non-core access (slave mode), a machine check exception is taken
- CALRAM causes DSI exception only if the data relocation (DR) bit in the core ma-

chine state register, MSR[DR], is set. Refer to **Table 3-12**.

— L2U on MPC555/MPC556 already followed this protocol. but the LRAM did not. Now all L-bus peripherals follow this protocol.

— The MSR[DR] bit is described in the ***MPC555/MPC556 User's Manual (MPC555/MPC556UM/AD)***. Refer to **3.9.1 Machine State Register (MSR)** for more information.

- Four additional PRDS control bits were added to the USIU to allow more granularity of PRDS control on a part
- BBC includes a 4-Kbyte DECRAM that can be used if compression is not used or is not available.

1.2.2.3 SRAM Keep-Alive Power Behavior

The SRAM has three keep-alive power pins ($V_{DDSRAM1}$, $V_{DDSRAM2}$, and $V_{DDSRAM3}$). These pins provide keep-alive power to the SRAM arrays in the CALRAM modules and the DPTRAM modules.

The $V_{DDSRAM1}$ pin powers the 32-Kbyte CALRAM_A during keep-alive while power is off to the MPC565 / MPC566 (except for the keep-alive power supplies). CALRAM_A keeps all of its 32 Kbytes powered during power down.

The $V_{DDSRAM2}$ pin powers the 4-Kbyte CALRAM_B module. The $V_{DDSRAM3}$ pin powers the DPTRAM modules during keep-alive as well as during normal operation. The CALRAM modules only power their arrays from the V_{DDSRAM} pins during keep-alive. During normal operation, they are powered by the normal internal V_{DD} of the part.

The DPTRAM modules (six Kbytes and four Kbytes) and the four-Kbyte DECRAM in the BBC module power their arrays via the VDDSRAM3 pin during during keep-alive and are supplied by VDD during normal operation.

1.3 MPC565 / MPC566 Address Map

The internal memory map is organized as a single 4-Mbyte block. This is shown in **Figure 1-3**. This block can be moved to one of eight different locations. The internal memory space is divided into the following sections:

- Flash memory (one Mbyte) — U-bus memory
- Static RAM memory (26 Kbytes CALRAM) — L-bus memory
- Control registers and IMB3 modules (64 Kbytes), which is partitioned as

  — USIU and flash control registers
  — UIMB interface and IMB3 modules
  — CALRAM and READI control registers (L-bus control register space)

The internal memory block can reside in one of eight possible 4-Mbyte memory spaces. These eight locations are the first eight 4-Mbyte memory blocks starting with address 0x0000 0000, as shown in **Figure 1-2**. There is a user programmable register in the USIU to configure the internal memory map to one of the eight possible locations. Programmability of internal memory map location allows multiple chip system.

The IMB3 address space block in **Figure 1-4** shows memory allocation for IMB3 modules. It does not show the actual memory space required for individual modules. All these modules are mapped to the low address, numerically, of the memory allocated for that module in the IMB3 address space.

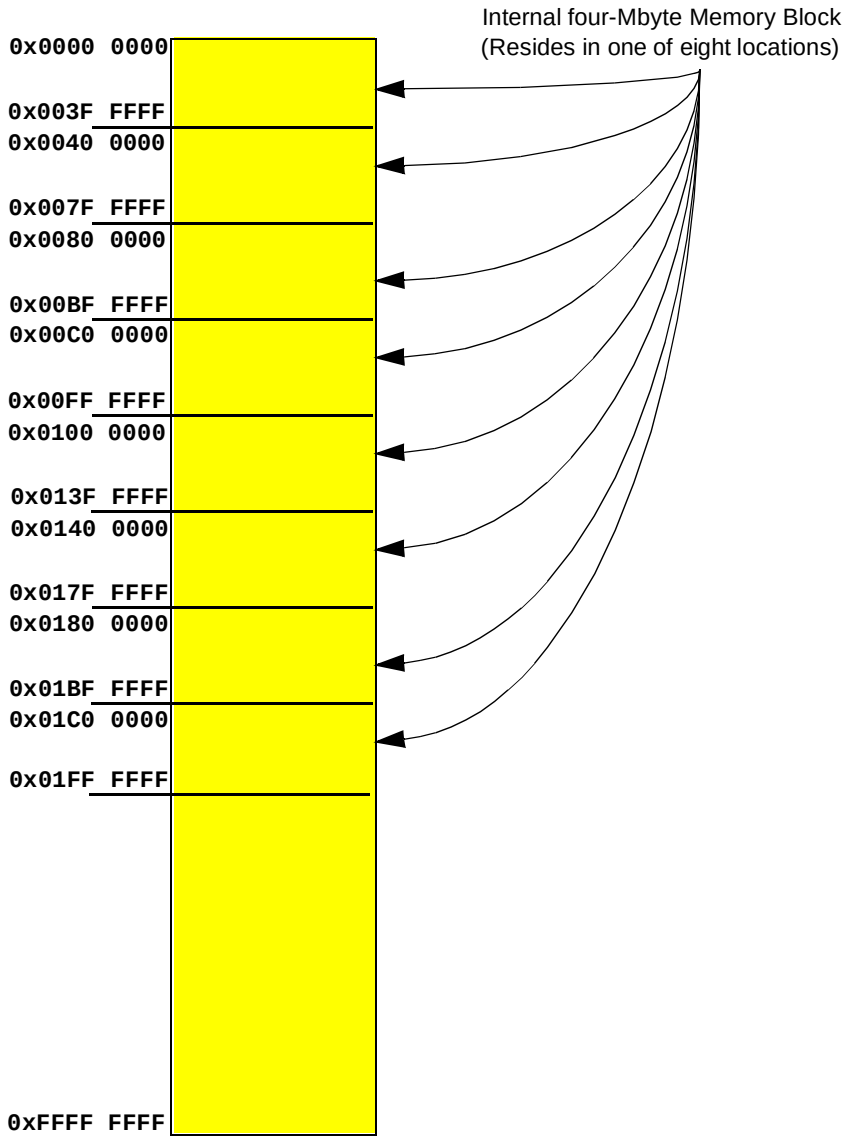

Figure 1-2 MPC565 / MPC566 Memory Map

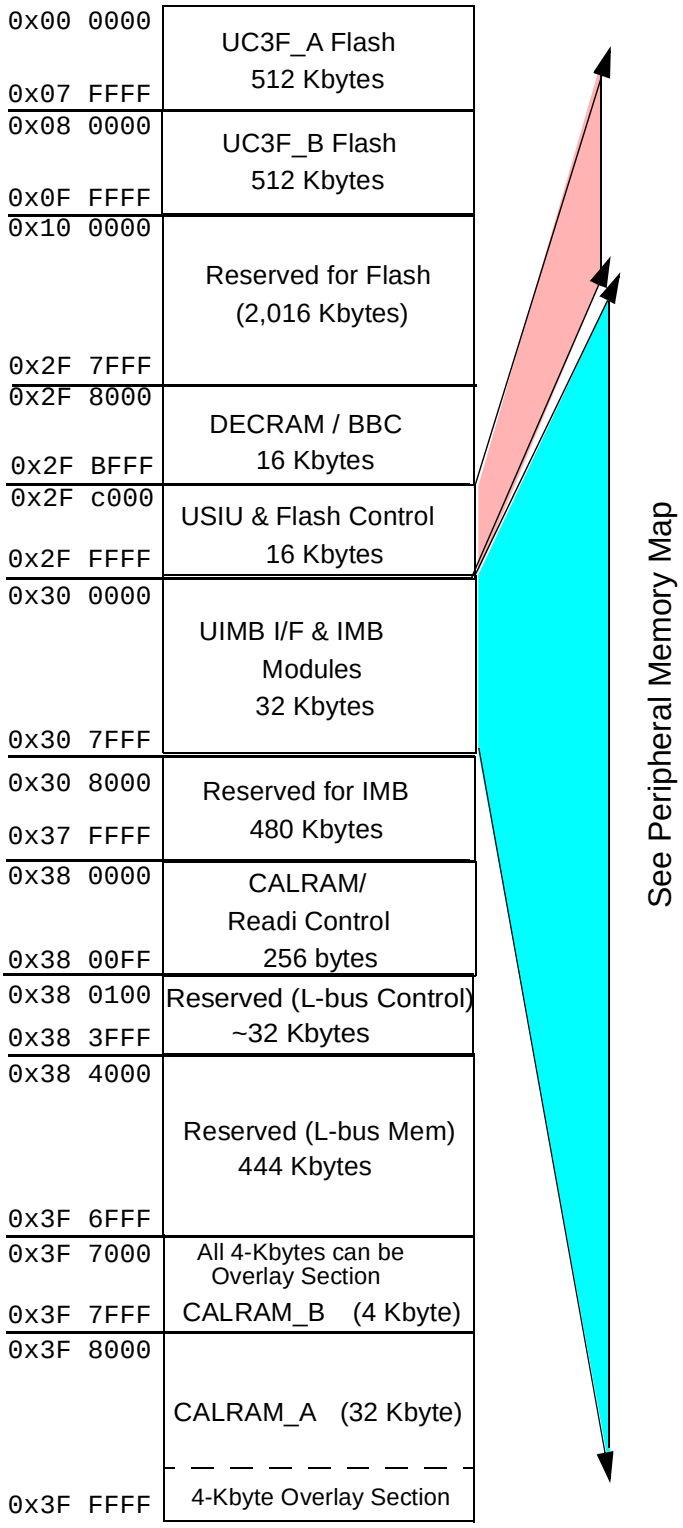

Figure 1-3 MPC565 / MPC566 Internal Memory Block

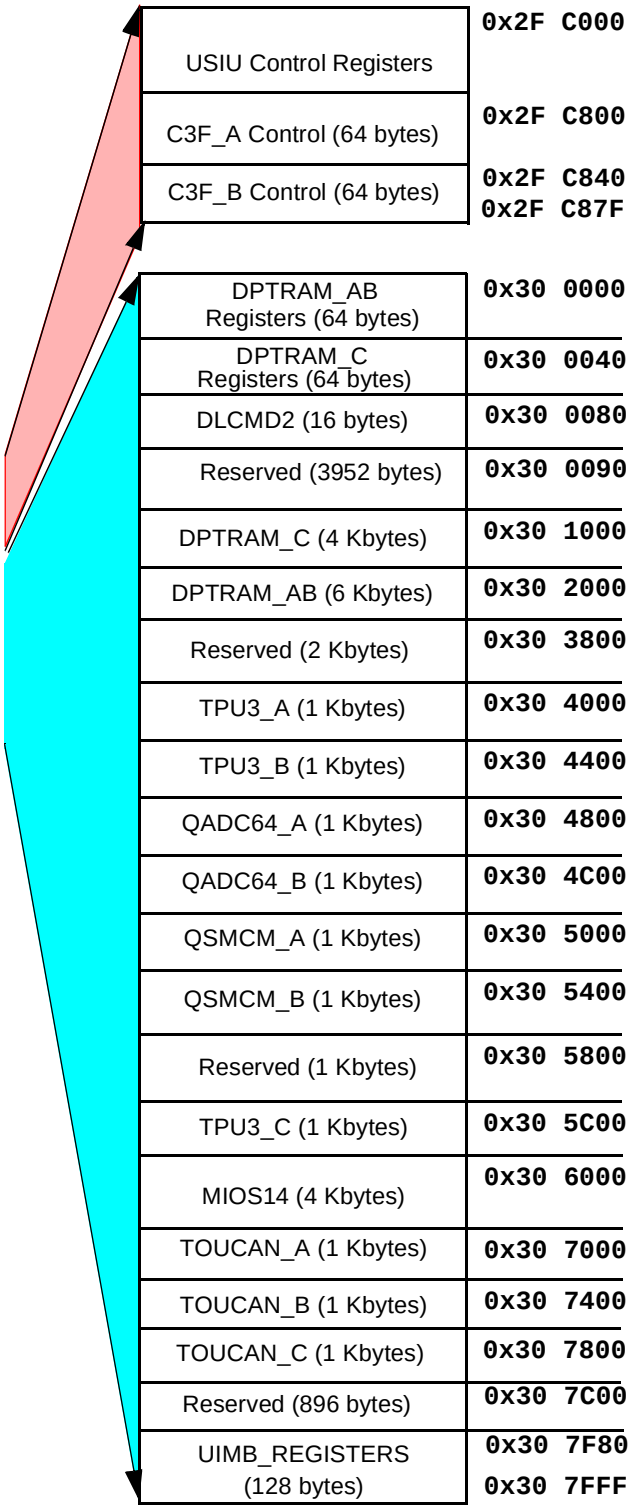

Figure 1-4 MPC565 / MPC566 Peripheral Memory Map

About
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News & Events
Membership
Members Only
Contact
IEEE-ISTO
Home

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