MOTOROLA
SEMICONDUCTOR
ERRATA SHEET

Part: MPC565.0A
Mask Set: 01K85H

# Customer Errata and Information Sheet Transportation Systems Group

Part: MPC565.0A Mask Set: 01K85H. Report generated 14 June 2000

**TRANSPORTATION SYSTEMS GROUP**
**CUSTOMER ERRATA AND INFORMATION SHEET**
**Part: MPC565.0A Mask Set: 01K85H**
**General Business Use**
**Report Generated: Wed Jun 14, 2000, 11:54:18**


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## DETAILED ERRATA DESCRIPTIONS

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CDR_AR_769 Customer Erratum MPC565.0A

MPC565.0 PADS: TA,TEA,BI,RETRY Outputs have a max freq of 30 MHz

**DESCRIPTION:**
In MPC565.0, TA_B, TEA_B, BI_B, and RETRY_B output signals are not generated correctly by the MPC565 at frequencies above 30 MHz. These pins could potentially be used by a logic analyzer or other debug equipment.

**WORKAROUND:**
For MPC565.0, do not use external logic requiring assertion of ta, tea, bi, or retry pins by the MPC565 while operating the system at frequencies higher than 30 MHz. External memory accesses should be controlled by the MPC565 memory controller.

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CDR_AR_765 Customer Erratum MPC565.0A

EPEE and B0EPEE of the FLASH are always enabled.

**DESCRIPTION:**
EPEE (External Program/Erase Enable) and B0EPEE (Block 0 External Program/Erase Enable) are always enabled such that the external pins EPEE and B0EPEE of the chip cannot disable programming or erasing of the Flash.

**WORKAROUND:**
Even with EPEE and B0EPEE always enabled, a series of writes to the High Voltage Control Register(C3FCTL) are required in order to perform a program or erase. This required series of accesses provides a level of protection to prevent the user from performing unwanted programs or erases.

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CDR_AR_761 Customer Erratum MPC565.0A

BBC DECRAM Powered by KAPWR instead of VDDSRAM3

**DESCRIPTION:**
The KAPWR pin supplies power to the BBC DECRAM which should be on the separate backup supply VDDSRAM3. The DECRAM should be powered by the VDDSRAM3 pin, which also powers the DPTRAM_4K and the DPTRAM_6K.

**WORKAROUND:**
In order to maintain the DECRAM array contents when VDD is turned off, then KAPWR must remain powered.

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**CDR_AR_764** **Customer Erratum** **MPC565.0A**

**MPC565.0 PADS: Multimaster Modes Non-Functional**

**DESCRIPTION:**
The active negate pads (TA_B, TEA_B, BI_B, RETRY_B) do not properly three-state after negation when operating as outputs. This prevents multi-master operation as well as assertion of the TA_B or TEA_B pin by external logic.

**WORKAROUND:**
Use the memory controller for external memory access. Do not use multiple masters on the MPC565.0 external bus.

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**CDR_AR_782** **Customer Erratum** **MPC565.0A**

**SIU Powerdown Counter Modes Don’t Operate Correctly**

**DESCRIPTION:**
When VDD is turned off, the powerdown counter modes of the SIU lose their state. This affects the PPC RTC, the Decrementer (DEC), the Time Base (TB), and the PIT.

**WORKAROUND:**
Use the MIOS14 Real-Time Clock submodule and an external 32 KHz crystal for powerdown counting.

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**CDR_AR_793** **Customer Erratum** **BBC2.CDR3UBUS_01_0**

**BBC2 Compression: No Compressed code in ETR Space**

**DESCRIPTION:**
IMPU translates addresses in compression mode regardless of address form. Note that this bug has a very minor impact, and will cause problems ONLY if the compressed address space covers the Exception/External Int Table Relocation address space (0xFFF0_xxxx).

**WORKAROUND:**
Do not put compressed code in the address space reserved for Exception Table relocation.

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**CDR_AR_794** **Customer Erratum** **BBC2.CDR3UBUS_01_0**

**BBC2 Compression: BTB Non-functional**

**DESCRIPTION:**
The BTB (Branch Target Buffer) operates incorrectly.

**WORKAROUND:**
Do not activate BTB.

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**CDR_AR_795** **Customer Erratum** **BBC2.CDR3UBUS_01_0**

**BBC2 Compression: Speed Paths Limit Compression to 40MHz Room.**

**DESCRIPTION:**
Speed Paths in the compression logic of the BBC2 limit frequency of operation to 40 MHz at Room temperature.

**WORKAROUND:**
Limit compression mode usage to 40 MHz, Room temperature.

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**CDR_AR_748** **Customer Erratum** **C3FBIU.CDR3UBUS_01_0**

**On-page Fetches to Flash are Disabled Resulting in 2-Clock Fetches Only**

**DESCRIPTION:**
Flash read pages (2 per Flash module) contain 8 words each. Fetches to instructions loaded into either read page take 1 clock and fetches to instructions in the Flash array take 2 clocks. The 1-clock on-page access feature is disabled and all fetches are considered off-page and take 2 clocks. Likewise all data accesses will take 4 clocks (no 3-clock on-page accesses).

**WORKAROUND:**
None

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**CDR_AR_707** **Customer Erratum** **C3FBIU.CDR3UBUS_01_0**

**Do not program Reset Configuration Word in Flash**

**DESCRIPTION:**
If Reset Configuration Word is programmed in Flash, device configuration during reset will be indeterminant.

**WORKAROUND:**
Use External Reset Configuration or the Default Internal Reset Configuration Word (0x00000000) for providing the Reset Configuration Word.

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**CDR_AR_747** **Customer Erratum** **C3F_ARRAYS.A**

**Excessive Access Abort Latency Results in Lower Flash Operating Frequency**

**DESCRIPTION:**
Fetch aborts, due to misprediction of branch outcome, which are intended for an off-page address in the Flash will require more latency than initially anticipated. Thus the operating frequency will need to be limited to accomodate for this case, if fetches are performed from the Flash.

**WORKAROUND:**
Limit frequency to 40 Mhz at room and cold temperatures and to 35 Mhz at hot temperatures.

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**CDR_AR_718** Customer Erratum **C3F_ARRAYS.A**

**Flash Censorship is Not Operational**

**DESCRIPTION:**
Programming and erasing the Censorship Bits should not be performed. The device operates as it would in uncensored mode (no security enabled).

**WORKAROUND:**
No workaround for emulating censored mode.

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**CDR_AR_719** Customer Erratum **C3F_ARRAYS.A**

**Flash Suspend Feature is not Operational**

**DESCRIPTION:**
The Suspend feature should not be used.

**WORKAROUND:**
Do not use Suspend feature.

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**CDR_AR_786** Customer Erratum **C3F_ARRAYS.A**

**Flash: Set of EHV for Program or Erase**

**DESCRIPTION:**
EHV may not be protected by the interlock, causing C3F to respond either with an inadvertent program verify (PE=0) or an inadverent erase (PE=1).

**WORKAROUND:**
Follow Program or Erase sequence as stated in the MPC565 Reference Manual. Also note that interlock protection of EHV will work properly as long as a successful Program or Erase is completed prior to this event.

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**CDR_AR_788** Customer Erratum **C3F_ARRAYS.A**

**Flash: Don’t Terminate Pgm/Erase, Censor Clear, or FEM**

**DESCRIPTION:**
If Program, Erase, or Clear Censor are terminated early by negating EHV, "hot switching" in the array may occur on any C3F access (array or register access).

**WORKAROUND:**
Do not terminate embedded program or erase by setting EHV=0 prior to HVS=0. If this does occur, delay C3F accesses (array or register) for <400 nanoseconds.

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**CDR_AR_789** Customer Erratum **C3F_ARRAYS.A**

**Flash: Shadow Row Program/Erase Select and Protect**

**DESCRIPTION:**
Shadow Row contents may be programmed or erased while BLOCK[0], SBBLOCK[0], PROTECT[0], or SBPROTECT[0] are set.

**WORKAROUND:**
Do not rely on PROTECT[0] or SBPROTECT[0] to protect the shadow row contents against unintentional program or erase.

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**CDR_AR_755** **Customer Erratum** **DLCMD2.CDR3IMB3_03_0**

**DLCMD2 switching into 1x-4x mode**

**DESCRIPTION:**
If 4x mode is entered before the symbol counter value reaches the normal mode TIFS value but after the counter has passed the 4x mode TIFS value, the module will hang.Before a transmitter can send an SOF (which resets the symbol counter) it must wait for either of the two following conditions. One, TIFS must have been reached. Two, REOF and a rising edge from another module must have been detected. The second condition means that if another module tries to access the bus before TIFS and after REOF then we can also contend and try and gain access to the bus. If no other module is trying to access the bus then condition two won't occur.The symbol counter does not reset when the mode is changed. This means that if the module is put into 4x mode before the normal mode TIFSvalue has been detected (which would signal an SOF and reset the counter) the module will keep counting until it reaches its max value and holds. Since the counter is stuck at its max value the module cannever detect any symbols on the bus so it will hang until reset.

**WORKAROUND:**
Software work-around: Wait for TIFS before changing to/from 4x mode. To wait for TIFS the difference between the normal mode REOF and TIFS values must be found. Once that value is determined, wait for bus_idle (REOF), which can be polled for, and wait (TIFS - REOF) amount of time.

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**CDR_AR_758** **Customer Erratum** **DLCMD2.CDR3IMB3_03_0**

**DLCMD2 Temporary Interrupt Deassertions**

**DESCRIPTION:**
Writes to the CMD/TDATA register or reads of the STAT/RDATA register during a pending DLCMD2 interrupt cause a temporary deassertion of the interrupt signal. One of two things can happen at this point. One, the CPU will generate a level zero IACK cycle because the interrupt line is currently deasserted.Two, the deassertion could occur after the CPU latches the DLCMD2 interrupt request. Since the interrupt line is deasserted the DLCMD2 will not respond to the CPU's IACK cycle and a spurious interupt will occur.

**WORKAROUND:**
If interrupts are disabled before the register accesses are performed and then enabled after the accesses the interrupt deassertions can not occur. However, it may be necessary on parts that use a CPU32X/FASRAM combination to insert a NOP instructions after the last register access and before the interrupt enabling. This is due to the fact that the FASRAM has a dedicated bus to the CPU32X which allows much faster accesses between it and the CPU32X then the CPU32X has between itself and another IMB module such as the DLCMD2. If the Program stack is being kept in the FASRAM it is possible that the CPU32X's instruction to enable interrupts, which would only require a stack access to check the status register, will occur before its access of the DLCMD2's register. Since interrupts will no longer be disabled, the register access could cause an interrupt deassertion.

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**CDR_AR_759** **Customer Erratum** **DLCMD2.CDR3IMB3_03_0**

**DLCMD2 LCK bit is write once not set only.**

**DESCRIPTION:**
**The LCK bit in the SCTL is implemented incorrectly. The spec states that once the LCK bit is set all writes to the SCLT register are disabled and only a reset can clear the bit (unless in test mode). The DLCMD2 operates as follows. The first time the LCK bit is written, whether it is a one or zero, the bit cannot be changed unless the part is in test mode, freeze mode, or a reset occurs. This means that in master mode, if a zero is first written to the LCK bit, the SCTl register can never be locked and full access to it will be permitted until a reset occurs.**

**WORKAROUND:**
**The SOFT_FRZ bit in the MCR (bit 10) should be kept at 1 (its initial state) until the SDATA registers have been initialized and the LCK bit set. This will keep the module in debug mode which allows writes to the LCK bit.**

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**CDR_AR_772** **Customer Erratum** **DLCMD2.CDR3IMB3_03_0**

**DLCMD2 Equating Parameter Values**

**DESCRIPTION:**
**If certain symbols are assigned the same counter value, one of the symbols might never be recognized. Instead the other symbol with the same value would be detected. For excample, if RMIN=TSHA than an active RMIN will always be recongnized. In the hardware implementation the parameter values are checked with a priority scheme. Once a parameter matches, no furthur checking is done until the next clock cycle when the counter value has changed. For an active pulse the following parameters are checked in order: TSOF, TSHA,TLNA, TBRK, RMIN, RSH, RLN, and REOF. In order for each parameter to be detectable they must all have unique values. Similarly, during a passive pulse the following parameters are checked in order: TSHP, TLNP, TIFR, TIFS, RMIN, RSH, RLN, REOF. Again, this set of passive parameters must be distinct.Keeping these parameters distinct is almost guranteed due to the timing requirements of the J1850 specifications. Certain round trip delays in the transceiver may suggest that some parameters should be equated. In this case either parameter should be adjusted to make them unique. The real risk of equation parameters occurs in test mode when parameters are set as small as possible to accelerate testing.Ideally the hardware should be changed so that all parameters are checked every time in parallel. As a result, any parameter could be set as calculated without concern for uniqueness.**

**WORKAROUND:**
**Parameters in the active set must all be distinct and parameters in the passive set must all be distinct.**

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**CDR_AR_785** **Customer Erratum** **DLCMD2.CDR3IMB3_03_0**

**DLCMD2 RFIFO Polling**

**DESCRIPTION:**
Reads from the staus/rdata word result in valid data being popped from the RFIFO. If the FIFO is empty no pop occurs. This behavior is implemented as follows. First, the status and data at the head of the FIFO is returned. If the FIFO is currently empty, the status register will indicate this and the FIFO data returned will be invalid. After the read has completed, the FIFO will be popped if not empty. The problem occurs if data has been pushed since the status register read indicated an empty FIFO. In this case, when the pop is requested, the FIFO contains valid data which is then popped and lost.

**WORKAROUND:**
When polling for data, access the status register with a byte read access. Upon finding valid data present in the FIFO, access both the status and data with a word read access.

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**CDR_AR_771** **Customer Erratum** **DLCMD2.CDR3IMB3_03_0**

**DLCMD2 SEL bit is not lockable.**

**DESCRIPTION:**
The spec states that if LCK=1 writes to the SEL bit are disabled. This is not the case. The SEL bit can still be written when LCK=1. This allows the user to read both the 1x SDATA parameters and the 4x SDATA parameters. If writes to the SEL bit were not allowed, after the LCK bit was set it would only be possible to view one set of SDATA parameters depending on the state of the SEL bit wen the LCK bit was set.

**WORKAROUND:**
This is the desired operation of the DLCMD2 and a spec change is recommended.

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**CDR_AR_776** **Customer Erratum** **DPTRAM.4K_CDR3IMB3_04_0**

**DPTRAM_4K array not accessible in correct Spanish Oak memory map.**

**DESCRIPTION:**
The DPTRAM_4K array is not accessible when the Base Address register is set to the proper value for the Spanish Oak (0xff90). It functions correctly when the array is in the correct location for the DPTRAM_6Karray. On the Spanish Oak, both the DPTRAM_4K and the DPTRAM_6K can be used as TPU microcode RAM, or one DPTRAM can be used for TPU microcode and the other as normal RAM. It is not possible to use both RAMs as normal RAMs at the same time.

**WORKAROUND:**
In order to use the DPTRAM_4K as a TPU microcode RAM, the DPTRAM4K_RBAR (Base Address Register) should be programmed with 0xffa0 to place it in the DPTRAM_6K location. This must be done before the DPTRAM6K_RBAR is programmed. The 4K array can then be addressed starting at the expected location for the DPTRAM_6K array. After writing the TPU3 microcode into the RAM array, the DPTRAM_4K is placed in TPU emulation mode. This removes it from the memory map. Now the DPTRAM_6K can be intialized and used in its normal location.

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**CDR_AR_727** Customer Erratum **PADRING.565_CDR3_01_0**

**MPC565.0 PADS: IRQ4_B_AT2_SGPIOC4 GPIO Output Non-functional**

**DESCRIPTION:**
The GPIO output function on the IRQ4_B_AT2_SGPIOC4 pin does not function correctly. The data output is the sgpioc1 data register bit instead of the correct value.

**WORKAROUND:**
Do not use the SGPIOC4 output function.

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**CDR_AR_731** Customer Erratum **PADRING.565_CDR3_01_0**

**MPC565.0 PADS: GPIO Input on ADDR_SGPIOA[14] Not Functional**

**DESCRIPTION:**
GPIO Input on ADDR_SGPIOA[14] Not Functional

**WORKAROUND:**
Do not use the GPIO input function on ADDR_SGPIOA[14].

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**CDR_AR_732** Customer Erratum **PADRING.565_CDR3_01_0**

**MPC565.0 PADS: GPIO Output Function on DATA_SGPIOD[15] Does Not Work**

**DESCRIPTION:**
MPC565.0 PADS: GPIO output function on DATA_SGPIOD[15] does not work. The value output is not the value which should appear, but the value programmed for GPIO data output on the DATA_SGPIOD[16] pin.

**WORKAROUND:**
Do not use the DATA_SGPIOD[15] pin as GPIO data output.

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**CDR_AR_739** Customer Erratum **PADRING.565_CDR3_01_0**

**READI: RSTI_B pad should have weak pull-down; has pull-up instead**

**DESCRIPTION:**
The internal weak pull on the RSTI_B pin should be a pull-down. Instead it is a pull-up.

**WORKAROUND:**
Provide an external pull-down on the RSTI_B pin (<6 Kohms).

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**CDR_AR_790** Customer Erratum **PADRING.565_CDR3_01_0**

**MPC565.0 PADS: DSCK Pin Needs Weak Pulldown**

**DESCRIPTION:**
The DSCK pin needs a weak pull-down at reset instead of a weak pull-up, which it currently has. A pull-up at reset will enable debug mode out of reset.

**WORKAROUND:**
Put an external pull-up on the DSCK pin ( <6 K Ohms).

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**CDR_AR_791** **Customer Erratum** **PADRING.565_CDR3_01_0**

**MPC565.0 PADS: HRESET_B & SRESET_B not 5V Compatible**

**DESCRIPTION:**
**The HRESET_B and SRESET_B pads cannot be pulled to 5V externally without long-term reliability problems.**

**WORKAROUND:**
**Use an external device to reset parts which require a 5V reset.**

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**CDR_AR_749** **Customer Information** **PADRING.565_CDR3_01_0**

**Long-Term Reliability Prohibits Full 5V Compatibility for 2.6V Outputs**

**DESCRIPTION:**
**CDR3 device constraints for the 2.6V pad drivers indicate a gate stress limitation of 3.1V to either the drain or source. If 5V is driven onto any pin with a 2.6V driver (such as the external data bus) before the MPC565 drives out with 2.6V, the 3.1V stress limit will be exceeded and can cause long term reliability problems to that pin. An external RAM or ASIC on the data bus can operate at up to 3.6V VDD assuming a maximum long-term duty cycle of writes occuring up to 0.1% of the total bus clocks.**

**WORKAROUND:**
**Limit voltage on external data bus to 3.6V. Don’t pull any pin above 3.1V if it has a 2.6V output which will turn on. Ensuring that 5V inputs are current limited to <2mA allows the 2.6V output to pull the pin voltage quickly to a legal range, so that erroneously turning on the 2.6V output won’t damage the pad unless the erroneous condition persists for a long time (years?).**

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**CDR_AR_440** **Customer Information** **RCPU.CDR3LBUSIBUS_15_0**

**Execute any IMUL/DIV instruction prior to entering low power modes.**

**DESCRIPTION:**
**There is a possibility of higher than desired currents during low power modes. This is caused by a possible contention in the IMULDIV control area. This contention may only exist prior to the execution of any IMULDIV instruction.**

**WORKAROUND:**
**Execute a mullw instruction prior to entering into any low power mode (anytime after reset, and prior to entering the low power mode).**

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**CDR_AR_214** **Customer Information** **RCPU.CDR3LBUSIBUS_15_0**

**Only negate interrupts while the EE bit (MSR) disables interrupts**

**DESCRIPTION:**
An IRQ to the core, which is negated before the core services it, may cause the core to stop fetching until reset.

**WORKAROUND:**
Interrupt request to the core should only be negated while interrupts are disabled by the EE bit in the MSR. Software should disable interrupts in the CPU core prior to masking or disabling any interrupt which might be currently pending at the CPU core. For external interrupts, it is recommended to use the edge triggered interrupt scheme. After disabling an interrupt, sufficient time should be allowed for the negated signal to propagate to the CPU core, prior to re-enabling interrupts. For an interrupt generated from an IMB module, 6 clocks is sufficient (for IMBCLK in 1:1 mode).

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**CDR_AR_754** **Customer Erratum** **QADC64E.CDR3IMB3_01_0**

**QADC64:Do not use queue1 in external gated mode with queue2 in continuous mode.**

**DESCRIPTION:**
When the gate for queue1 opens when queue2 is converting the last word in its queue, queue1 completion flag will immediately set and no conversions will occur. Queue1 will remain in a hung state for the duration of the gate (no conversions will occur regardless of how long the gate is open). This failure will only occur when the QADC64 is configured with queue1 in external gated mode (continuous or single scan) and queue2 is in continuous mode. The failure mode can be detected if it is known that the gate for queue 1 is shorter than the length of the queue, and the completion flag becomes set. The failure can also be detected as follows: software writes invalid results to the result register (3ff when it is known the input will never go to full scale); after the gate has closed if the invalid result is still in result space 0, then the failure has occured.

**WORKAROUND:**
There are 2 workarounds: 1) Do not use queue 2 if queue1 is set for external gated mode. Or, 2) If queue2 is used and queue1 is in external gated mode, set queue2 to single scan mode (for silicon with CDR_AR_421 use only use ch63 EOQ for queue2 EOQ condition)

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**CDR_AR_734** **Customer Erratum** **READI.CDR3LBUSUBUS_01_0**

**READI Module cannot be enabled without Nexus input clock (MCKI).**

**DESCRIPTION:**
A free-running input clock (MCKI) must be supplied to enable and configure the READI module.

**WORKAROUND:**
Instead of using MCKO to generate MCKI, use another clock (max frequency = CLKOUT/2).

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**CDR_AR_783** Customer Erratum **READI.CDR3LBUSUBUS_01_0**

**READI input messages must be 4 MCKI apart.**

**DESCRIPTION:**
**READI input messages must be spaced by at least 4 MCKI input clocks.**

**WORKAROUND:**
**Wait for an output message response before sending in another input message.**

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**CDR_AR_698** Customer Information **READI.CDR3LBUSUBUS_01_0**

**READI Input message requires 2 MCKI idle after READI Enabled.**

**DESCRIPTION:**
**If an input message is sent to the READI immediately after deassertion of RSTI_B (enabling READI) the READI may not recognize the start of the message and will ignore it. This behavior could cause the tool to get out of sync with the READI.**

**WORKAROUND:**
**Do not send in an input message until at least 2 MCKI after READI is enabled, or better, until the DID message is received from the READI.**

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**CDR_AR_627** Customer Information **TPU3.CDR3IMB3_03_0**

**TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase**

**DESCRIPTION:**
**Wrong generation of 50% duty cycle caused when we have the command combination "write_mer, end." If the write_mer is the last instruction together with the end, this may create an additional match using the old content of the match register (which is in the past now and therefore handled as an immediate match)**

**WORKAROUND:**
**Add neg_mrl together with the last write_mer and with end-of-phase. The negation of the flag overrides the false match which is enabled by write_mer and postpones the match effect by only u-instruction. In the following u-instruction the NEW MER value is already compared to the selected TCR and no false match is generated. The neg_mrl command has priority over the match event recognition, separating the write_mer and the end command. This gives enough time for the new MER to update before the channel transition re-enables match events.**

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**CDR_AR_757** Customer Erratum **USIU.CDR3UBUS_07_0**

**USIU: PULL_DIS & SPULL_DIS bits affect masked by PRDS and SPRDS bit state.**

**DESCRIPTION:**
**The effect of the PULL_DIS bits is masked by the PRDS bit and the effect of the SPULL_DIS bits is masked by the SPRDS bit. The PULL_DIS and SPULL_DIS bits only function properly if PRDS and SPRDS, respectively, are set. It is not possible to disable weak pulls on pads controlled by a PULL_DIS bit if PRDS=0. Similarly for SPRDS and SPULL_DIS. It is possible to disable the weak pulls controlled by PRDS and leave the PULL_DIS weak pulls active.**

**WORKAROUND:**
**None.**

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**Little Endian modes are not supported**

**DESCRIPTION:**
The little Endian modes are not functional.

**WORKAROUND:**
Do not activate little endian modes.