SECTION 17
MODULAR I/O SYSTEM (MIOS14)

The intent of the following section is to describe in detail the configuration of the MIOS14. The MIOS14 is a MIOS derivative.

The modular I/O subsystem (MIOS) is an integral module of Motorola's CISC and RISC modular embedded controller families.

Members of these families are generally composed of a processor and slave modules that are connected together through a bus that is referred to, throughout this document, as the "peripheral bus".

A generic block diagram of such a configuration is shown on **Figure 17-1**.

17.1 Overview

The MIOS is, in itself, modular and is composed of submodules, making it easily configurable for different kinds of applications. It offers an expandable library of simple-to-use yet flexible I/O and timer functions such as:

- I/O ports
- Counters
- Input captures, output compares
- Pulse and period measurements
- Pulse width modulation
- Real-time clock

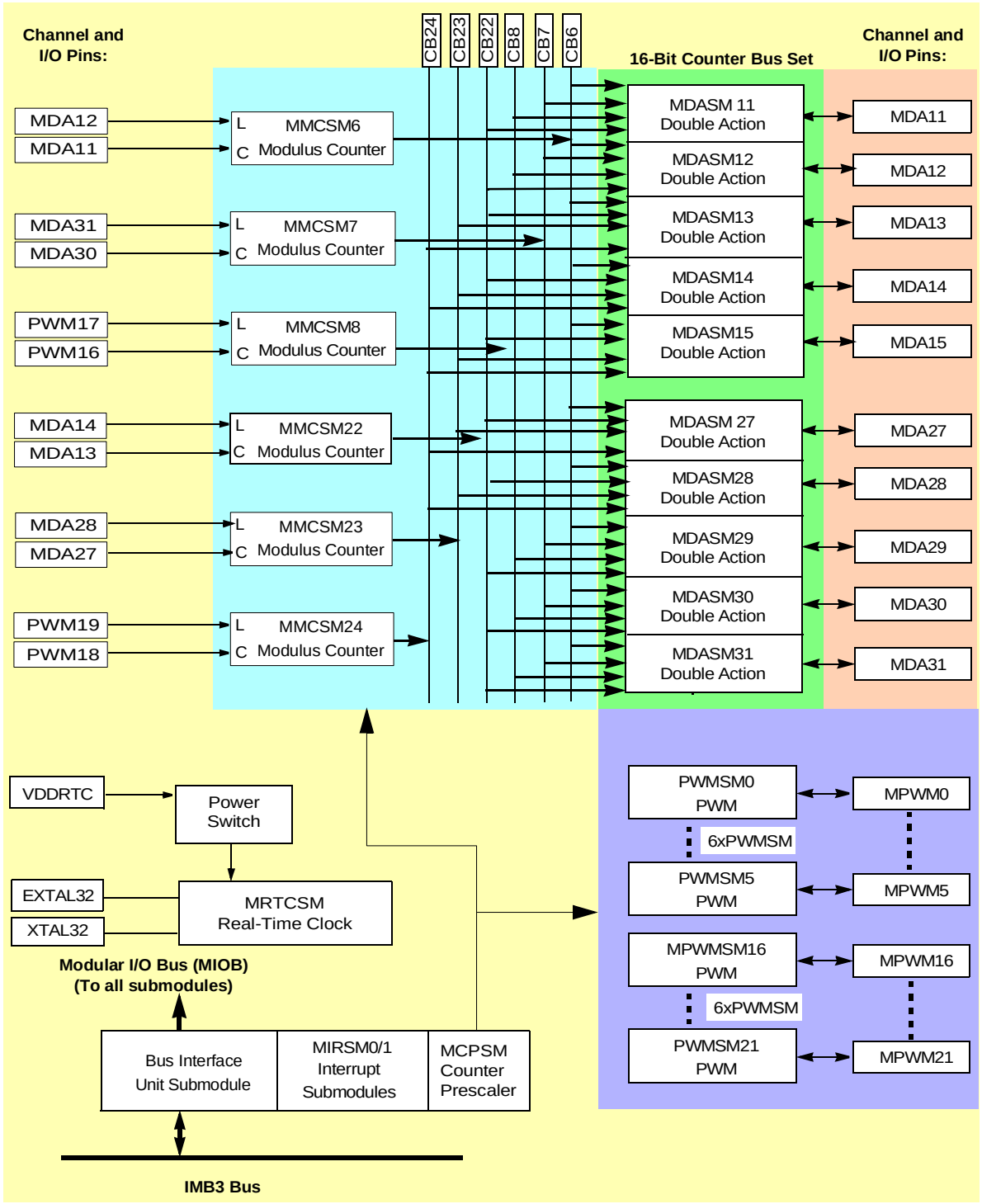


Figure 17-1 MPC565 / MPC566 MIOS14 Block Diagram

17.1.1 Documentation Conventions

The following conventions are applied throughout this document.

17.1.1.1 Terminology Definitions:

Peripheral Bus — A bus that is used to connect together the different modules, the CPU and the integration module of a given chip. This bus can be for example the IMB3.

Bus Cycle — A single transfer of data across the bus using the established protocols and timing. For any MIOS, a bus cycle consists of a single byte or a 16-bit transfer.

Master — The module that initiates a bus request and controls the bus cycle with the slave module.

Slave — The module that responds to a master's bus transaction.

Transaction — The transfer of data between two modules (a master and a slave) utilizing the internal auxiliary bus and its established protocol. A single transaction may require multiple bus cycles (for example a 32-bit transfer).

Asserted — A signal is driven to its active or true state, irrespective of that state being represented by a high or low voltage level.

Negated — A signal is driven to its inactive or false state, irrespective of that state being represented by a high or low voltage level.

Tic — A clock tic is defined as the single high or low state of a clock signal. For a 40-MHz clock, a tic has a duration of 12.5 ns.

Clock — Two tics: a full period. For a 40-MHz clock, a clock has a duration of 25 ns.

BIU — Bus interface unit: a submodule responsible for interfacing between the peripheral bus and the module.

Block — A group of four 16-bit registers.

$\mathbf{f_{SYS}}$ — Frequency of the chip clock used by the MIOS.

17.1.2 Bit and Byte Ordering

Throughout this document:

- The least significant bit of a register (LSB) is called bit-0
- The least significant byte of an MIOS14 register is at an odd address

17.1.2.1 Supported Data Sizes

The following data sizes are supported within the MIOS14:

- 32-bit words
- 16-bit words
- bytes (8 bits)

17.1.2.2 MIOS14 Port Size:

The MIOS14 port size is 16 bits.

17.1.3 Submodule Numbering Convention

By definition, a block is a group of four 16-bit registers. Each of the blocks within the MIOS14 addressing range is assigned a block number. The first block is located at the base address of the MIOS14. The blocks are numbered sequentially starting from zero.

Every submodule instantiation is also assigned a number. The number of a given submodule is the block number of the first block of this submodule.

This does not apply to the MBISM, the MCPSM and the RQSMs:

- The MBISM and the MCPSM are unique in the MIOS14 and does not need a number
- The RQSMs are numbered incrementally starting from zero

17.1.4 MIOS14 Module/Submodule Addressing

17.1.4.1 MIOS14 Base Address

The MIOS14 base address is 0x306000, and is referred to as “MIOS14 base address” in this document. The MIOS14 addressable range is 4 Kbytes.

17.1.4.2 Submodule Base Addresses

The base address of a given implemented submodule within the MIOS14 is the sum of the base address of the MIOS14 and the submodule number multiplied by eight. (This does not apply to the MBISM nor to the MCPSM and RQSMs).

17.1.4.3 Bus Error Support

A bus error signal has to be generated when accessing unimplemented/reserved 16-bit registers and privilege violations.

The MIOS14 should return a bus error under the following conditions:

- Access to unimplemented 16-bit registers within the decoded register block boundary (no bits in register)
- User access to supervisor registers
- Access to test registers when not in test mode (TSTMOD negated)
- Writes to read-only registers

17.1.4.4 Wait States

The MIOS14 does not generate any wait states.

17.1.4.5 Unimplemented Locations

All MIOS14 unimplemented locations, within the addressable range, will return a logic 0 when accessed, and will generate a BERR signal.

17.1.4.6 Unimplemented Bits

All MIOS14 registers unused bits should return a 0 when accessed.

17.2 MIOS14 Naming Convention

17.2.1 Submodule Naming Convention

An instantiated submodule is assigned a name made of its acronym followed by its submodule number.

EXAMPLE

If submodule number 18 was an MPWMSM it would be named MPWMSM18.

17.2.2 MIOS14 Pin Naming Convention

The MIOS14 input and output pin names are composed of five fields according to the following convention:

– “M”

– <submodule short_prefix>

– <submodule number>

– <pin attribute suffix> (optional)

– <bit number> (optional)

The pin prefix and suffix for the different MIOS14 submodules are as follows:

- MMCSM:
  submodule short_prefix: “MC”
  pin attribute suffix: C for the clock pin
  pin attribute suffix: L for the load pin
  For example an MMCSM placed as submodule number n would have its corresponding input clock pin named MMCnC and its input load pin named MMCnL.

- MDASM:
  submodule short_prefix: “DA”
  pin attribute suffix: none
  For example a MDASM placed as submodule number n would have its corresponding channel I/O pin named MDAn

- MPWMSM:
  submodule short_prefix: “PWM”
  pin attribute suffix: none
  For example a MPWMSM placed as submodule number n would have its corresponding channel I/O pin named MPWMn

- MPIOSM:
  submodule short_prefix: “PIO”
  pin attribute suffix: B
  For example a MPIOSM placed as submodule number n would have its corresponding I/O pins named MPIOnB0 to MPIOnB15 for bit 0 to bit 15, respectively.

In the MIOS14, some pins are multiplexed between submodules. This is shown in **Table 17-1** with using the same pin names for the inputs or outputs which are connected together.

Table 17-1 MIOS14 Configuration Description

Sub-Module Type	Block Number	Connected to:				RQSM Number	RQSM Bit Position	Base Address Offset	Pin Function	Input Pin Name	Output Pin Name	Alternate Pin Function
		CBA	CBB	CBC	CBD							
		BSL0=0 BSL1=0	BSL0=1 BSL1=0	BSL0=0 BSL1=1	BSL0=1 BSL1=1							
PWMSM	0					0	0	0x30 6000	PWM, I/O	MPWM0	MPWM0	
PWMSM	1					0	1	0x30 6008	PWM, I/O	MPWM1	MPWM1	
PWMSM	2					0	2	0x30 6010	PWM, I/O	MPWM2	MPWM2	
PWMSM	3					0	3	0x30 6018	PWM, I/O	MPWM3	MPWM3	
PWMSM	4					0	4	0x30 6020	PWM, I/O	MPWM4	MPWM4	
PWMSM	5					0	5	0x30 6028	PWM, I/O	MPWM5	MPWM5	
MMCSM	6	CB6				0	6	0x30 6030	Clock In	MDA11		
									Load In	MDA12		
MMCSM	7			CB7		0	7	0x30 6038	Clock In	MDA30		
									Load In	MDA31		
MMCSM	8				CB8	0	8	0x30 6040	Clock In	MPWM16		
									Load In	MPWM17		
Reserved	9-9											
RTCSM	10					0	10	0x30 6050	Osc. Input	EXTAL32		
									Osc. Output	XTAL32		
									Power Supply	VRTC		
MDASM	11	CB6	CB22	CB7	CB8	0	11	0x30 6058	Channel I/O	MDA11	MDA11	
MDASM	12	CB6	CB22	CB7	CB8	0	12	0x30 6060	Channel I/O	MDA12	MDA12	
MDASM	13	CB6	CB22	CB23	CB24	0	13	0x30 6068	Channel I/O	MDA13	MDA13	
MDASM	14	CB6	CB22	CB23	CB24	0	14	0x30 6070	Channel I/O	MDA14	MDA14	
MDASM	15	CB6	CB22	CB23	CB24	0	15	0x30 6078	Channel I/O	MDA15	MDA15	
PWMSM	16					1	0	0x30 6080	PWM, I/O	MPWM16	MPWM16	
PWMSM	17					1	1	0x30 6088	PWM, I/O	MPWM17	MPWM17	
PWMSM	18					1	2	0x30 6090	PWM, I/O	MPWM18	MPWM18	
PWMSM	19					1	3	0x30 6098	PWM, I/O	MPWM19	MPWM19	
PWMSM	20					1	4	0x30 60A0	PWM, I/O	MPWM20	MPWM20	

Table 17-1 MIOS14 Configuration Description (Continued)

Sub-Module Type	Block Number	Connected to: CBA BSL0=0 BSL1=0	CBB BSL0=1 BSL1=0	CBC BSL0=0 BSL1=1	CBD BSL0=1 BSL1=1	RQSM Number	RQSM Bit Position	Base Address Offset	Pin Function	Input Pin Name	Output Pin Name	Alternate Pin Function
PWMSM	21					1	5	0x30 60A8	PWM, I/O	MPWM21	MPWM21	
MMCSM	22		CB22			1	6	0x30 60B0	Clock In	MDA13		
									Load In	MDA14		
MMCSM	23			CB23		1	7	0x30 60B8	Clock In	MDA27		
									Load In	MDA28		
MMCSM	24				CB24	1	8	0x30 60C0	Clock In	MPWM18		
									Load In	MPWM19		
Reserved	25-26											
MDASM	27	CB6	CB22	CB23	CB24	1	11	0x30 60D8	Channel I/O	MDA27	MDA27	
MDASM	28	CB6	CB22	CB23	CB24	1	12	0x30 60E0	Channel I/O	MDA28	MDA28	
MDASM	29	CB6	CB22	CB7	CB8	1	13	0x30 60E8	Channel I/O	MDA29	MDA29	
MDASM	30	CB6	CB22	CB7	CB8	1	14	0x30 60F0	Channel I/O	MDA30	MDA30	
MDASM	31	CB6	CB22	CB7	CB8	1	15	0x30 60F8	Channel I/O	MDA31	MDA31	
PIOSM	32							0x30 6100	GPIO	MPIO32B0	MPIO32B0	VF[0]
									GPIO	MPIO32B1	MPIO32B1	VF[1]
									GPIO	MPIO32B2	MPIO32B2	VF[2]
									GPIO	MPIO32B3	MPIO32B3	VFLS[0]
									GPIO	MPIO32B4	MPIO32B4	VFLS[1]
									GPIO	MPIO32B5	MPIO32B5	MPWM4
									GPIO	MPIO32B6	MPIO32B6	MPWM5
									GPIO	MPIO32B7	MPIO32B7	MDO[7]
									GPIO	MPIO32B8	MPIO32B8	MDO[6]
									GPIO	MPIO32B9	MPIO32B9	MDO[5]
									GPIO	MPIO32B10	MPIO32B10	MDO[4]
									GPIO	MPIO32B11	MPIO32B11	MPWM20
									GPIO	MPIO32B12	MPIO32B12	MPWM21
									GPIO	MPIO32B13	MPIO32B13	C_CNTX0
									GPIO	MPIO32B14	MPIO32B14	C_CNRX0
									GPIO	MPIO32B15	MPIO32B15	32KCLKOUT
Reserved	33-255											
MBISM	256							0x30 6800				
Reserved	257-257											
MCPSM	258							0x30 6810				
Reserved	259-383											
MIRSM0	384-391							0x30 6C00				
MIRSM1	392-399							0x30 6C40				
Reserved	400-511											

17.3 MIOS14 Functional Overview

This section gives an overview of the MIOS14, a description of the timing function concepts, an overview description of the MIOS14 submodules and examples of how to implement functions with the MIOS14.

17.3.1 MIOS14 Configuration

The MIOS14 is composed of the following submodules:

- One MIOS bus interface submodule (MBISM)
- One MIOS counter prescaler submodule (MCPSM)
- Six MIOS modulus counter submodules (MMCSM)
- 10 MIOS double action submodules (MDASM)
- 12 MIOS pulse-width modulation submodules (MPWMSM)
- One MIOS 16-bit parallel port I/O submodule (MPIOSM)
- Two request submodules (RQSM)
- One MIOS real time clock submodule (MRTCSM)

Figure 17-1 shows the block diagram of the MIOS14 configuration.

17.4 MIOS14 Feature List

The basic features of the MIOS14 are as follows:

- Modular architecture at the silicon implementation level
- Disable capability in each submodule to allow power saving when its function is not needed
- Six 16-bit counter bus to allow action submodules to use counter data
- When not used for timing functions, every channel pin can be used as a port pin: I/O, output only or input only, depending on the channel function.
- Submodules' pin status bits reflect the status of the pin
- MIOS counter prescaler submodule (MCPSM):
  - Centralized counter clock generator
  - Programmable 4-bit modulus down-counter
  - Wide range of possible division ratios: 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16
  - Count inhibit under software control
- MIOS modulus counter submodule (MMCSM):
  - Programmable 16-bit modulus up-counter with built-in programmable 8-bit prescaler clocked by MCPSM output.

  - Maximum increment frequency of the counter:
    - Clocked by the internal MCPSM output: f_{SYS} / 2
    - Clocked by the external pin: f_{SYS} / 4
  - Flag setting and possible interrupt generation on overflow of the up-counter
  - Time counter on internal clock with interrupt capability after a pre-determined time
  - Optional pin usable as an external event counter (pulse accumulator) with overflow and interrupt capability after a pre-determined number of external events.
  - Usable as a regular free-running up-counter
  - Capable of driving a dedicated 16-bit counter bus to provide timing information to action submodules (the value driven is the contents of the 16-bit up-counter register)
  - Optional pin to externally force a load to the counter with modulus value
- MIOS double action submodule (MDASM):
  - Versatile 16-bit dual action unit allowing two events to occur before software intervention is required
  - Six software selectable modes allowing the MDASM to perform pulse width and period measurements, PWM generation, single input capture and output compare operations as well as port functions
  - Software selection of one of the six possible 16-bit counter buses used for timing operations
  - Flag setting and possible interrupt generation after MDASM action completion
  - Software selection of output pulse polarity
  - Software selection of totem-pole or open-drain output
  - Software readable output pin status
  - Possible use of pin as I/O port when MDASM function is not needed
- MIOS pulse width modulation submodule (MPWMSM):
  - Output pulse width modulated (PWM) signal generation with no software involvement
  - Built-in 8-bit programmable prescaler clocked by the MCPSM

- PWM period and pulse width values provided by software:
  - Double-buffered for glitch-free period and pulse width changes
  - Two-cycle minimum output period/pulse-width increment (50 ns @ 40 MHz)
  - 50% duty-cycle output maximum frequency: 10 MHz
  - Up to 16 bits output pulse width resolution
  - Wide range of periods:
    - 16 bits of resolution: period range from 3.27 ms (with 50-ns steps) to 6.71 s (with 102.4 µs steps)
    - Eight bits of resolution: period range from 12.8 µs (with 50 ns steps) to 26.2 ms (with 102.4-µs steps)
  - Wide range of frequencies:
    - Maximum output frequency at f_{SYS} = 40 MHz with 16 bits of resolution and divide-by-2 prescaler selection: 305 Hz (3.27 ms)
    - Minimum output frequency at f_{SYS} = 40 MHz with 16 bits of resolution and divide-by-4096 prescaler selection: 0.15 Hz (6.7 s)
    - Maximum output frequency at f_{SYS} = 40 MHz with eight bits of resolution and divide-by-2 prescaler selection: 78125 Hz (12.8 µs)
    - Minimum output frequency at f_{SYS} = 40 MHz with 8 bits of resolution and divide-by-4096 prescaler selection: 38.14 Hz (8.2 ms)
  - Programmable duty cycle from 0% to 100%
  - Possible interrupt generation after every period
  - Software selectable output pulse polarity
  - Software readable output pin status
  - Possible use of pin as I/O port when PWM function is not needed
- MIOS 16-bit parallel port I/O submodule (MPIOSM):
  - Up to 16 parallel I/O pins per MPIOSM
  - Uses four 16-bit registers in the address space, one for data and one for direction and two reserved

- Simple data direction register (DDR) concept for selection of pin direction

- MIOS real time clock submodule (MRTCSM):
  - Programmable 47-bit free-running ripple counter for minimum power consumption split into a 15-bit prescaler and a 32-bit second counter
  - Buffering of the 47-bit free-running counter to guaranty 32-bit and 47-bit coherent accesses on the 16-bit MIOB bus
  - Possibility of suppressing 15-bit prescaler update
  - Software shutdown of the dedicated low power oscillator to maintain battery shelf life
  - Flag setting and possible interrupt generation according to eight software selectable rates
  - Automatic hardware power supply selection through dedicated power switch
  - Customized to use low cost standard 32.768-KHz crystal for internal clocking of the 32-bit counter at 1Hz
  - Software accessible precision of 2^{-15} second and unique time indication in seconds over a span of 136 years (2^{32} seconds)
  - Eliminates risk of time inaccuracy due to interrupt overruns appearing in systems with software accumulated time

17.5 MIOS14 Pin Count

The MIOS14 requires 40 pins. The usage of these pins is shown in **Figure 17-2**.

NOTE

Three “non-I/O” pins are dedicated to the real-time clock standby power supply and oscillator.

17.6 Submodule Overview

17.6.1 MIOS Bus Interface Submodule (MBISM)

The MIOS bus interface submodule (MBISM) allows all the MIOS14 submodules to communicate to the peripheral bus master via the modular I/O bus (MIOB).

17.6.2 MIOS Modulus Counter Submodule (MMCSM)

The MIOS modulus counter submodule (MMCSM) contains a programmable 8-bit prescaler, a 16-bit up counter associated with a modulus latch that gives the flexibility of recycling the counter at a count other than 64-Kbyte clock cycles, a clock source

selector, software writable control registers and software readable status bits. When the 16-bit up counter overflows an interrupt flag is generated.

The state of the modulus latch is transferred to the counter under the following three conditions:

1. When an overflow occurs
2. When an appropriate transition occurs on the external load pin
3. When the program writes to the counter register. In this case, the value is first written into the modulus latch and immediately transferred to the counter.

Software can also write a value to the modulus latch for later loading into the counter with one of the two first criteria.

The current state of the 16-bit counter is the primary output of the MIOS modulus counter submodule. The 16-bit counter always drives a value onto a dedicated 16-bit counter bus.

A software control register selects whether the clock input to the counter is one of the prescaler output or the corresponding input pin. The polarity of the external input pin is also programmable. Clocking of the counter may also be inhibited under software control.

17.6.3 MIOS Double Action Submodule (MDASM)

The MIOS double action submodule (MDASM) provides two consecutive 16-bit input captures or two consecutive 16-bit output compare functions that can occur automatically without software involvement. The input edge detector is programmable to cause the capture function to occur on the desired edges. The output flip-flop is set by one of the output compare and is reset by the other one. In either the input capture modes or the output compare modes, an optional interrupt is available to the software. Software selection is provided to select which of the incoming 16-bit counter buses is used for the input capture or the output compare

The MDASM has six different software selectable modes:

- Disable mode
- Pulse width measurement
- Period measurement
- Input capture mode
- Single pulse generation
- Continuous pulse width generation

The MDASM has three data registers that are accessible to the software from the various modes. For some of the modes, two of the registers are cascaded together to provide double buffering. The value in one register is transferred to another register

automatically at the correct time so that the minimum pulse (measurement or generation) is just one 16-bit counter bus count.

17.6.4 MIOS Pulse Width Modulation Submodule (MPWMSM)

The purpose of the MIOS pulse width modulation submodule (MPWMSM) is to create a variable pulse width output signal at a wide range of frequencies, independent of other MIOS14 output signals. The MPWMSM includes its own 8-bit prescaler and counter, and thus does not use the MIOS14 16-bit counter buses.

The MPWMSM pulse width can vary from 0.0%t to 100.0%, with up to 16 bits of resolution. The finest output resolution is the MCU system clock time divided by two (for a f_{SYS} of 40.0 MHz, the finest output pulse width resolution is 50 ns). With the full 16 bits of resolution and the overall prescaler divide ratio varying from divide-by-2 to divide-by-4096, the period of the MPWMSM output can range from 3.2 8ms to 6. 7s (assuming a f_{SYS} of 40 MHz). By reducing the counting value, the output signal period can be reduced. The period can be as fast as 205 µs (4.882 KHz) with 12 bits of resolution, as fast as 12.8 µs (78.125 KHz) with eight bits of resolution, and as fast as 3.2 µs (312.500 KHz) with 6 bits of resolution (still assuming a f_{SYS} of 40 MHz and a first stage prescaler divide-by-2 clock selection).

17.6.5 MIOS 16-bit Parallel Port I/O Submodule (MPIOSM)

An MIOS 16-bit parallel port I/O submodule can handle up to 16 input/output pins. It contains two 16-bit registers: the data register (DR) and the data direction register (DDR). Each pin of the MPIOSM may be programmed as an input or an output under software control. The direction of the pins is determined by the state of the corresponding bits in the DDR.

17.6.6 MIOS Real-Time Clock Submodule (MRTCSM)

The purpose of the MRTCSM is to provide a real-time clock function independent of other MIOS14 submodules. This time counter is driven by a dedicated low frequency oscillator (32.768 KHz) for low power consumption. The MRTCSM contains a 15-bit prescaler and a 32-bit free-running counter, from which seconds, minutes, hours and days can be determined. The MRTCSM also has internal interrupt generation capability.

The MRTCSM may be sustained on a separate power supply, VDDRTC, for battery backup. The power switch, associated with the VDDRTC power pin, controls which supply (V_{DD} or VDDRTC) powers the MRTCSM.

17.6.7 Timing Function Examples

The versatility of the MIOS timer architecture is based on multiple counters and capture/compare channel units interconnected on 16-bit counter buses. Rather than present block diagrams of each submodule, this section includes some typical application examples to show how the submodules can be interconnected to form timing functions. The diagrams used to illustrate these examples show only the blocks utilized for that function.

To illustrate the timing range of the MIOS in different applications, many of the following paragraphs include time intervals quoted in microseconds and seconds. The assumptions used are that f_{SYS} is at 40 MHz with minimum prescaling (50-ns cycle) and with the maximum prescaling (102-µs cycle). For other f_{SYS} clock cycle rates and prescaler choices, the times mentioned in these paragraphs scale appropriately.

17.6.7.1 Single-Edge Input Capture

The MIOS single action submodule (MSASM) has an input capture register to latch the current state of a 16-bit counter bus when an external input edge is detected. The MSASM is software programmable to latch on the rising or falling edge of the input signal. The software also selects one of the 16-bit counter buses, each originating at a counter submodule. The software can also enable an interrupt to occur when the input edge is detected to notify the software that new edge capture information is available.

Figure 17-2 shows an example of an MIOS modulus counter submodule (MMCSM) for an MIOS single action submodule (MSASM) configured for input capturing. To measure the period of an incoming signal, the software reads and saves the latched value in register A for one edge, then when the next edge arrives, the software subtracts the new captured value in register A from the previously saved value to obtain the period interval. The maximum period that can be measured is the worst case software response time to a newly captured value.

The software measures the width of a pulse in a very similar way, the only difference is that after each edge, the edge detector is reprogrammed to trigger on the next opposite edge.

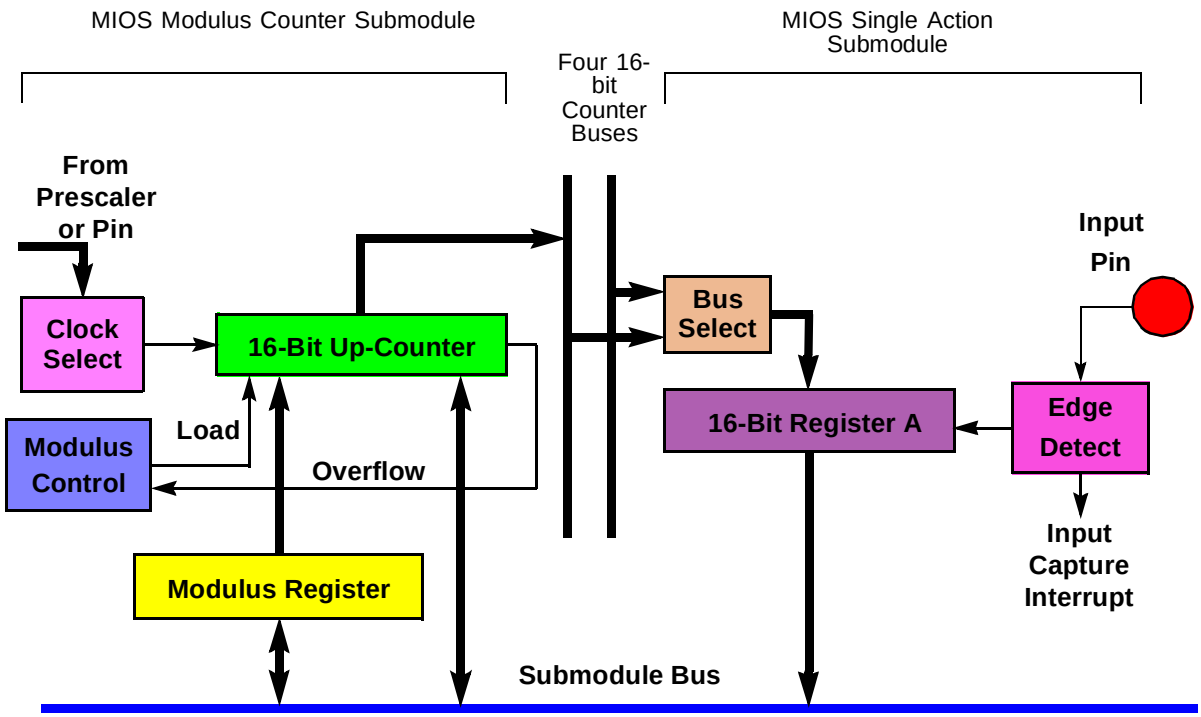


Figure 17-2 Example: Single-Edge Input Capture

17.6.7.2 Input Double-Edge Pulse Width Measurement

To measure the width of an input pulse, the MIOS double action submodule (MDASM) has two capture registers so that only one interrupt is needed after the second edge. The software can read both edge samples and subtract them to get the pulse width. The leading edge sample is double latched so that the software has the time of one full period of the input signal to read the samples to be sure that nothing is lost. Depending on the prescaler divide ratio, pulses width from 50 ns to 6.71 s can be measured.

NOTE

A software option is provided to also generate an interrupt after the first edge.

In the example shown in **Figure 17-2**, a counter submodule is used as the time-base for a MDASM configured in the input pulse width measurement mode. When the leading edge (programmed for being either rising or falling) of the input signal occurs, the state of the 16-bit counter bus is saved in register B1. When the trailing edge occurs, the 16-bit counter bus is latched into register A, and the content of register B1 is transferred to register B2. This operation leaves register B1 free for the next leading edge to occur, as soon as on the next clock cycle. When enabled, an interrupt is provided after the trailing edge, to notify the software that pulse width measurement data is available for a new pulse. After the trailing edge, the software has one cycle time of the input signal to obtain the values for each edge. When software attention is not needed for every pulse, the interrupt can be disabled — the software can at any time read registers A and B2 coherently (using a 32-bit read instruction) to get the latest edge measurements. Since the measurement resolution is 16 bits, signals with pulse duty cycles from 0.0015% to 99.9985% can be measured. The software work is less than half that needed with a timer that requires the software to read one edge and save the value, and then wait for the second edge.

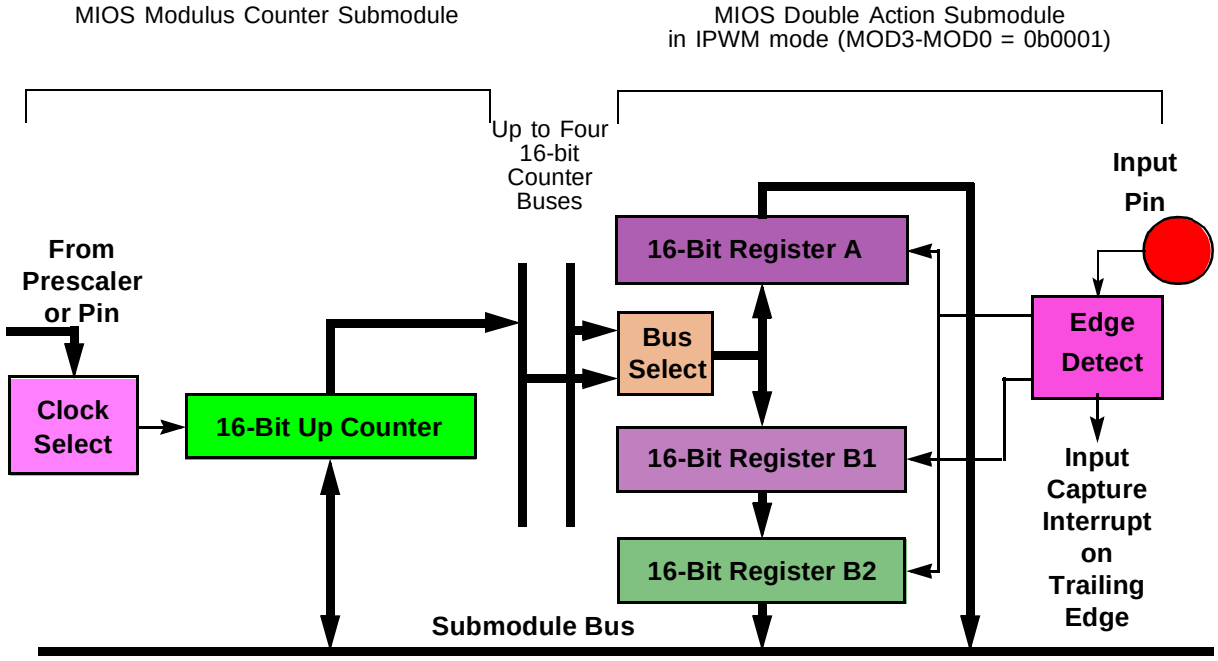


Figure 17-3 Example: Double-Edge Pulse Width Measurement

17.6.7.3 Input Double-Edge Period Measurement

Two samples are also available to the software from a MIOS double action submodule for period measurement. The software can read the previous and the current edge samples and subtract them. As with pulse width measurement, the software can be sure of not missing samples by insuring that the interrupt response time is faster than the fastest input period. Alternately, when the software is just interested in the latest period measurement, one 32-bit coherent read instruction can get both the current and the previous samples. Depending on the prescaler divide ratio, period times can be measured from 50 ns to 6.71 s.

Figure 17-3 shows an MMCSM and an MDASM combination as an example of period measurement. The software designates whether the rising or falling edge of the input signal is to be used for the measurements. When the edge is detected, the state of the 16-bit counter bus is stored in register A, and the content of register B1 is transferred into register B2. After register B2 is safely latched, the content of register A is transferred to register B1. This procedure gives the software coherent current and previous samples in registers A and B2 at all times. An interrupt is available for the cases where the software needs to be aware of each new sample.

NOTE

A software option is provided to also generate an interrupt after the first edge.

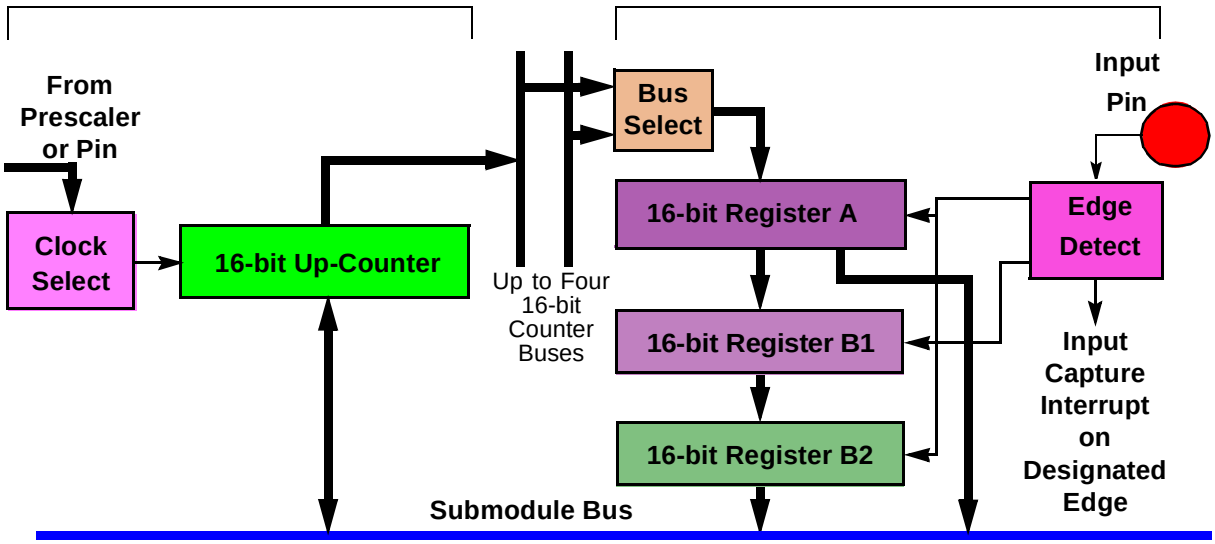


Figure 17-4 Example: Double-Edge Period Measurement

17.6.7.4 Single-Edge Output Compare

To create one output edge, the software can use an MSASM channel. The software provides a compare value in a register and the MSASM compares that value to the incrementing value seen on one of the 16-bit counter buses. When a comparison is detected, the state of the output pin is changed.

The example shown in **Figure 17-4** uses a counter submodule with one channel of an MSASM to create an output signal. The software can read the current state of the counter submodule. That, or some other criteria, is used to determine the time-base value when the output is to change. The software thus writes the compare value into register A. In the MSASM control register, the software establishes whether the output flip-flop is to toggle to the opposite state, or is to go to a high or a low level. The output compare interrupt is typically used to notify the software that the previous compare is complete and the MSASM is available for a new compare value in register A.

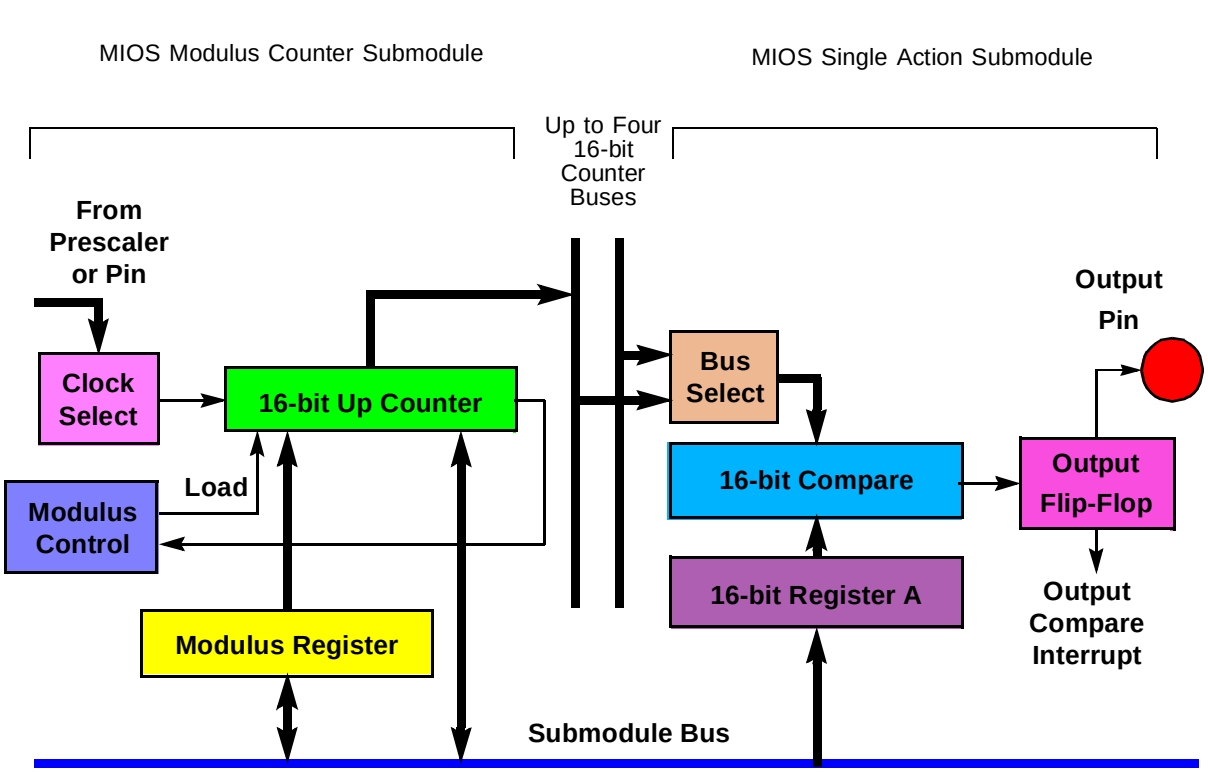


Figure 17-5 MIOS Example: Single-Edge Output Compare

17.6.7.5 Double-Edge Single Output Pulse Generation

Software can initialize the MIOS to generate both the rising and the falling edge of an output pulse. With a MDASM, pulses as narrow as 50 ns can be generated since software action is not needed between the edges. Pulses as long as 6.71 s can be generated. When an interrupt is desired, it can be selected to occur on every edge or only after the second edge.

Figure 17-5 shows how a counter submodule and a MDASM can be used to generate both edges of a single output pulse. The software puts the compare value for one edge in register A and the other one in register B2. The MDASM automatically creates both edges, and the pulse can be selected by software to be a high-going or a low-going. After the trailing edge, the MDASM stops to await further commands from the software.

NOTE

A single-edge output can be generated by writing to only one register.

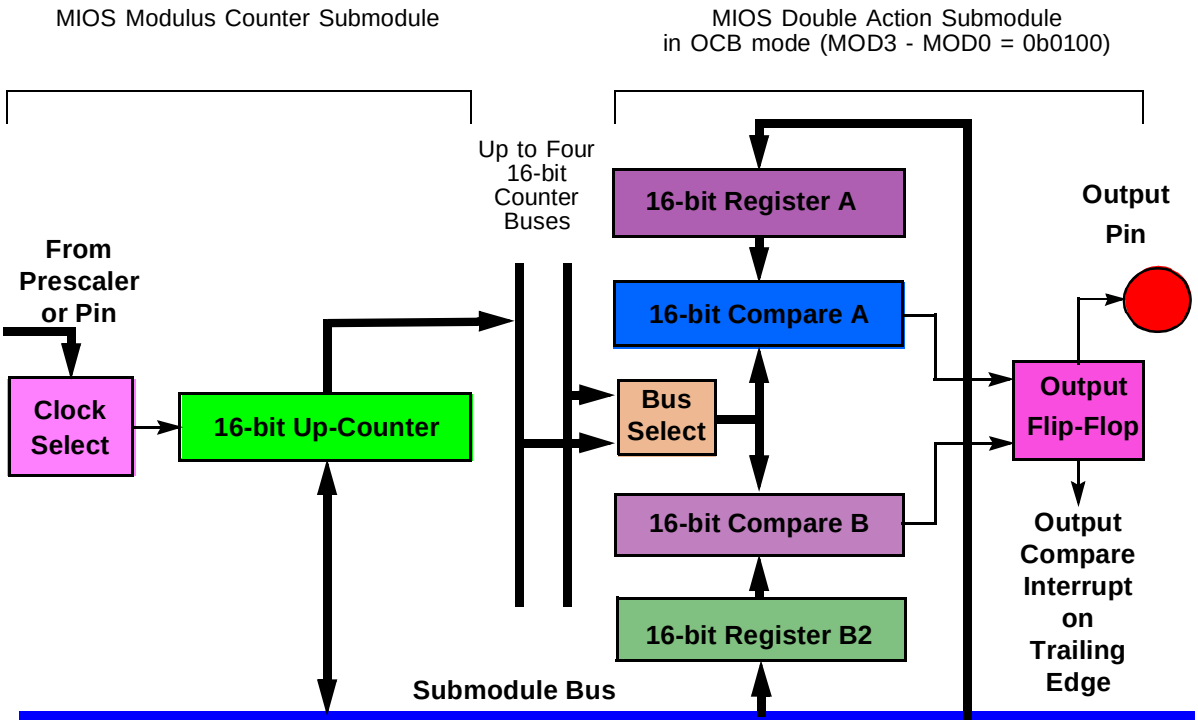


Figure 17-6 MIOS Example: Double-Edge Output Compare

17.6.7.6 Output Pulse Width Modulation With MDASM

Output waveforms can be generated with any duty cycle without software involvement. The software sets up a MDASM with the compare times for the rising and falling edges, and they are automatically repeated. The software does not need to respond to interrupts to generate continuous pulses. The period may be selected as the period of a MIOS modulus counter submodule used in free-running mode time-base, times a binary multiplier selected in the MDASM. Multiple PWM outputs can be created from multiple MDASMs and share one counter submodule, provided that the periods of all of the output signals are a binary multiple of the time-base, and that the counter sub-module is operating in a free-running mode. Each MDASM has a software selectable “don’t care” on high-order bits of the time-base comparison so that the period of one output can be a binary multiple of another signal. Masking the time-base serves to multiply the period of the time-base by a binary number to form the period of the output waveform. The duty cycle can vary from one cycle to 64-Kbyte cycles. The frequency can range from 0.6 Hz to 156 KHz, though the resolution decreases at the higher frequencies to as low as seven bits. The generation of output square wave signals is of course the special case where the high and low time are equal.

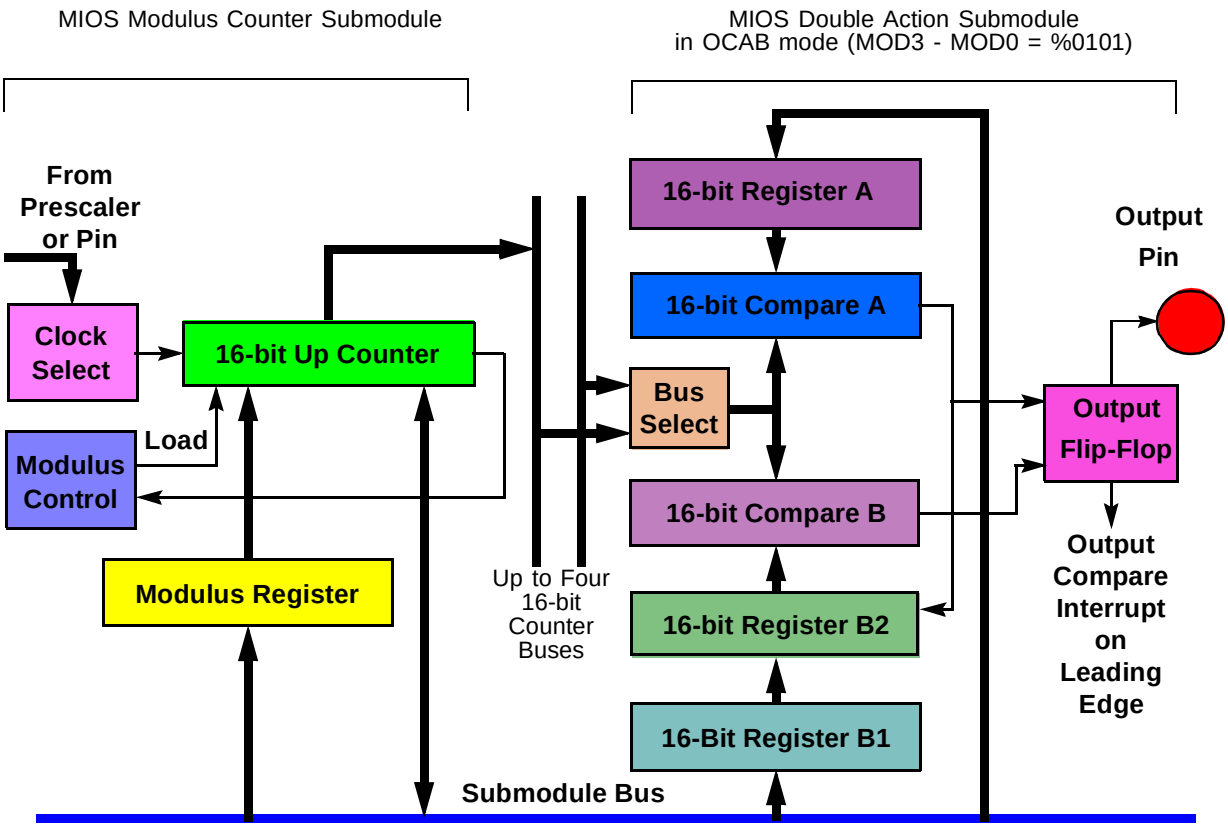


Figure 17-7 MIOS Example: Pulse Width Modulation Output

When an MMCSM is used to drive the time-base, the modulus value is the period of the output PWM signal. **Figure 17-7** shows such an example. The polarity of the leading edge of an output waveform is programmable for a rising or a falling edge. The software selects the period of the output signal by programming the MMCSM with a modulus value. The leading edge compare value is written into register A by software, and the trailing edge time is written into register B1. When the leading edge value is reached, the content of register B1 is transferred to register B2, to form the next trailing edge value. Subsequent changes to the output pulse width are made by writing a new time into register B1. Updates to the pulse width are always synchronized to the leading edge of the waveform.

It is typical to use the pulse width modulation mode of the MDASM without interrupts, though an interrupt can be enabled to occur on the leading edge. When the output is an unchanging repetitive waveform, the MDASM continuously generates the signal without any software intervention. When the software needs to change the pulse width, a new trailing edge time is written to the MDASM. The output is changed on the next full pulse. When the software needs to change the output at a regular rate, such as an acceleration curve, the leading edge interrupt gives the software one period time to update the new trailing edge time.

17.6.7.7 Input Pulse Accumulation

Counting the number of pulses on an input signal is another capability of the MIOS14. Pulse accumulation uses an MMCSM. Since the counters in the counter submodules are software accessible, pulse accumulation does not require the use of an action submodule. The pulse accumulation can operate continuously, interrupting only on binary overflow of the 16-bit counter. When an MMCSM is used, an interrupt can instead be created when the pulse accumulation reaches a preprogrammed value. To do that, the complement of the value is put in the modulus register and the interrupt occurs when the counter overflows.

17.7 MIOS14 I/O Ports

Each pin of each submodule can be used as an input, output or I/O port:

Submodule:	Number:	Type:
MPIOSM	16	I/O
MMCSM	2	Input
MDASM	1	I/O
MPWMSM	1	I/O

17.7.1 Using and Clearing Flag Bits

To clear any flag bit in the MIOS14, the software must first read the concerned flag as a one, then write a zero to it. These two steps do not have to be done on consecutive instructions. Writing a one to a flag bit has no effect.

NOTE

The flag clearing mechanism works only when no flag setting event occurs between the read and write operations. When a flag setting event occurs between the read and write operations, the flag bit is not cleared.

17.8 MIOS14 Bus System Description

In addition to its connection to the peripheral bus, there is an internal bus system within the MIOS14, called the modular I/O bus (MIOB). The MIOB is a bus that makes communications possible between any submodule and the peripheral bus master through the MBISM.

This MIOB is described in the following sections.

17.8.1 Modular I/O Bus Description

The MIOB is divided into three dedicated buses:

- The read/write and control bus
- The request bus
- The counter bus set

17.8.2 Read/Write and Control Bus Description

The read/write and control bus (RWCB) allows read and write data transfers to and from any I/O submodule through the MBISM. It includes signals for data and addresses as well as control signals. The control signals allow 16-bit simple synchronous single master accesses, and supports fast or slow masters accesses.

17.8.3 Request Bus Description

The request bus (RQB) provides interrupt requests signals along with I/O submodule identification and priority information to the MBISM.

NOTE

That some submodules do not generate interrupts and are therefore independent of the RQB.

17.8.4 Counter Bus Set Description

The counter bus set (CBS) is a set of six 16-bit counter buses. The CBS makes it possible to transfer information between submodules. Typically, counter submodules drive the CBS, while action submodules process the data on these buses.

NOTE

Some submodules are self contained and therefore independent of the counter bus set.

17.9 MIOS14 Address Map

The address space of the MIOS14 consist of 4Kbytes starting at the base address of the module (0x306000). The overall address map organization is shown in **Figure 17-1**.

The basic memory map in shown on **Figure 17-8**.

NOTE

If a supervisor privilege address space is accessed in user mode, the module will return a bus error.

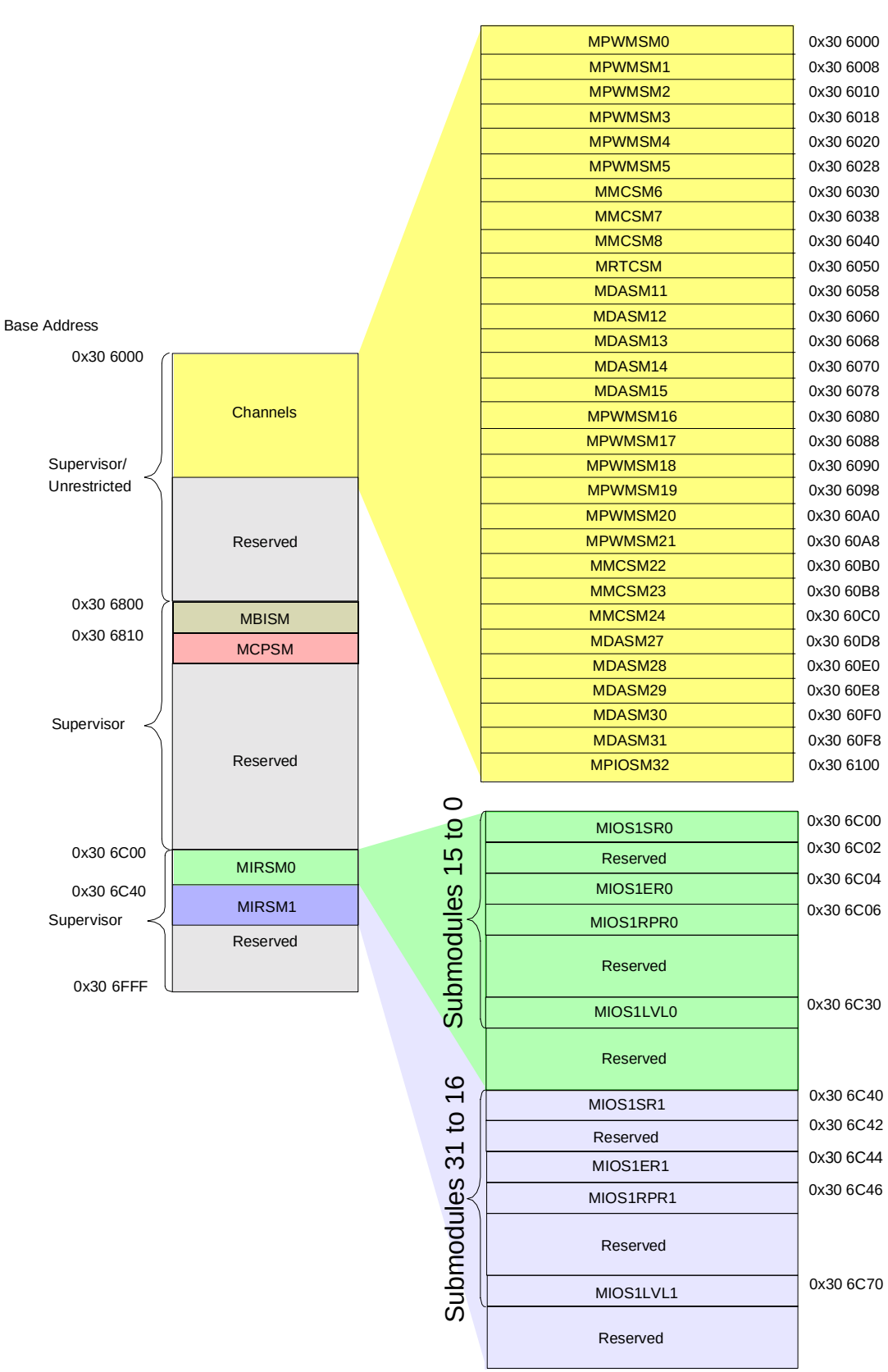


Figure 17-8 MIOS14 Memory Map

17.9.1 Interrupts

This section describes the interrupt functions of the MIOS14 and its submodules and how these interrupts are passed to the CPU via the Peripheral bus. Interrupt requests from the MIOS14 are treated as exceptions by the CPU and are dealt with by the CPU's exception processing routines. For a more detailed description of exception processing in the relevant microprocessors, please refer **SECTION 3 CENTRAL PROCESSING UNIT** and to the ***RCPU Reference Manual*** **(RCPURM/AD)**

17.9.2 MIOS14 Interrupt Structure

The MIOS14 and its submodules are capable of generating interrupts on different levels to be transmitted to the CPU via the peripheral bus. Inside the MIOS14, all the information required for requesting and servicing the interrupts are treated in two different sections:

- The interrupt control section (ICS)
- The request submodules (RQSM)

The request submodule gathers in service request flags from each group of up-to 16 submodules and transfers those requests to the MIOS14 interrupt control section (ICS). **Figure 17-9** shows a block diagram of the whole interrupt architecture.

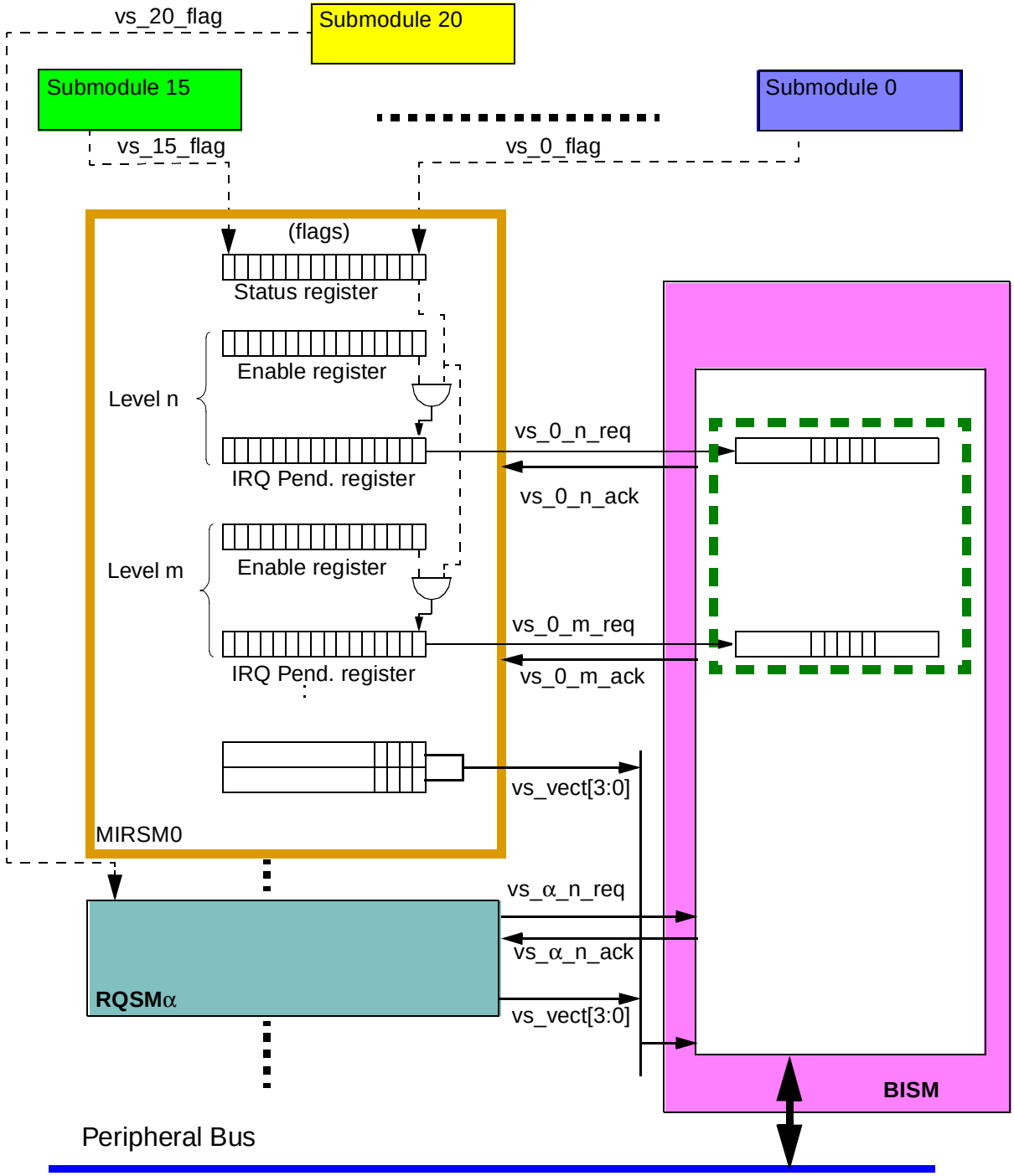


Figure 17-9 MIOS Interrupt Structure

17.9.3 Request Submodule (RQSM)

Each submodule that is capable of generating an interrupt can assert a flag line when an event occurs. In the maximum MIOS configuration, there could be up to 128 flag lines. Each RQSM serves up to 16 submodules. A particular MIOS configuration includes as many RQSM as are needed (maximum of eight).

Each RQSM includes:

- One 16-bit status register (for the flags)
- One 16-bit enable register for each implemented level
- One 16-bit IRQ pending register for each implemented level

One bit position in each of the above registers is associated with one submodule.

NOTE

If a submodule in a group of 16 cannot generate interrupts, then its corresponding flag bit in the status register is inactive and is read as zero.

When an event occurs in a submodule that activates a flag line, the corresponding flag bit in the status register is set. The status register is read/write, but a flag bit can be reset only if it has previously been read as a one. Writing a “one” to a flag bit has no effect. When the software intends to clear only one flag bit within a status register, the software must write an all-ones 16-bit value except for the bit position to be cleared which is a zero.

The enable register is initialized by the software to indicate whether each interrupt request is enabled for the levels defined in the ICS.

NOTE

In the case of multiple requests levels implementation in the same MIOS, it is possible to enable interrupts at more than one different levels for the same submodule. It is the responsibility of the software to manage this.

Each bit in the IRQ pending register is the result of a logical “AND” between the corresponding bits in the status and in the enable registers. If a flag bit is set and the level enable bit is also set, then the IRQ pending bit is set, and the information is transferred to the interrupt control section that is in charge of sending the corresponding level to the CPU. The IRQ pending register is read only.

NOTE

When the enable bit is not set for a particular submodule, the corresponding status register bit is still set when the corresponding flag is set. This allows the traditional software approach of polling the flag bits to see which ones are set. The status register makes flag polling easy, since up to 16 flag bits are contained in one register.

The submodule number of an interrupting source defines the corresponding RQSM number and the bit position in the status registers. To find the RQSM number and bit position of an interrupting source, proceed as follow:

1. Divide the interrupting submodule number by 16
2. The integer result of the division gives the RQSM number

3. The reminder of the division gives the bit position

17.9.4 MIRSM0 Registers

17.9.4.1 MIOS14SR0 Interrupt Status Register

MIOS14SR0 — Interrupt Status Register **0x30 6C00**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
FLG15	FLG14	FLG13	FLG12	FLG11	FLG10	RSVD	FLG8	FLG7	FLG6	FLG5	FLG4	FLG3	FLG2	FLG1	FLG0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-2 MIOS14SR0 Bit Descriptions

Bit(s)	Name	Description
15:11	FLG15:11	Flag Bits — MDASM flag bits [15:11]
10	FLG10	Flag Bit — RTCSM flag bit [10]
9	—	Reserved
8:6	FLG8:6	Flag Bits — MMCSM flag bits [8:6]
5:0	FLG5:0	Flag Bits — PWMSM flag bits [5:0]

This register contains the flag bits that are raised when the submodules generate an interrupt. Each bit corresponds to a given submodule.

17.9.4.2 MIOS14ER0 Interrupt Enable Registers

MIOS14ER0 — Interrupt Enable Register **0x30 6C04**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
EN15	EN14	EN13	EN12	EN11	EN10	RSVD	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
SRESET:															
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O

Table 17-3 MIOS14ER0 Bit Descriptions

Bit(s)	Name	Description
0:4	EN15:11	Flag Bits — MDASM flag bits [15:11]
5	EN10	Flag Bit — RTCSM flag bit [10]
6	—	Reserved
8:6	EN8:6	Flag Bits — MMCSM flag bits [8:6]
5:0	EN5:0	Flag Bits — PWMSM flag bits [5:0]

This register contains the interrupt enable bits for the submodules. Each bit corresponds to a given submodule.

17.9.4.3 MIOS14RPR0 Request Pending Register

MIOS14RPR0 — Request Pending Register **0x30 6C06**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
IRP15	IRP14	IRP13	IRP12	IRP11	IRP10	RSVD	IRP8	IRP7	IRP6	IRP5	IRP4	IRP3	IRP2	IRP1	IRP0
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-4 MIOS14PR0 Bit Descriptions

Bit(s)	Name	Description
0:4	IRP15:11	Flag Bits — MDASM flag bits [15:11]
5	IRP10	Flag Bit — RTCSM flag bit [10]
6	—	Reserved
7:9	IRP8:6	Flag Bits — MMCSM flag bits [8:6]
10:15	IRP5:0	Flag Bits — PWMSM flag bits [5:0]

This register is a read only register that contains the interrupt pending bits for the sub-modules. Each bit corresponds to a given submodule. When one of these bits is set, it means that a submodule raised its flag and the corresponding enable was set.

As this register is read only, a write to this register has no other effect than generating a bus error if the bus error option is selected.

17.9.5 MIRSM1 Registers

17.9.5.1 MIOS14SR1 Interrupt Status Register

MIOS14SR1 — Interrupt Status Register **0x30 6C40**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
FLG31	FLG30	FLG29	FLG28	FLG27	RESERVED		FLG24	FLG23	FLG22	FLG21	FLG20	FLG19	FLG18	FLG17	FLG16
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-5 MIOS14SR1 Bit Descriptions

Bit(s)	Name	Description
0:4	FLG31:27	Flag Bits — MDASM flag bits [31:27]
5:6	—	Reserved
7:10	FLGL24:22	Flag Bit — MMCSM flag bit [24:22]
11:15	FLG21:16	Flag Bits — PWMSM flag bits [5:0]

This register contains the flag bits that are raised when the submodules generate an interrupt. Each bit corresponds to a given submodule.

17.9.5.2 MIOS14ER1 Interrupt Enable Registers

MIOS14ER1 — Interrupt Enable Register **0x30 6C44**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
EN31	EN30	EN29	EN28	EN27	RESERVED		EN24	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-6 MIOS14ER1 Bit Descriptions

Bit(s)	Name	Description
15:11	EN31:27	Flag Bits — MDASM flag bits [15:11]
10:9	—	Reserved
8:6	EN24:22	Flag Bits — MMCSM flag bits [8:6]
5:0	EN21:16	Flag Bits — PWMSM flag bits [5:0]

This register contains the interrupt enable bits for the submodules. Each bit corresponds to a given submodule.

17.9.5.3 MIOS14RPR1 Request Pending Register

MIOS14RPR1 — Request Pending Register **0x30 6C46**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
IRP31	IRP30	IRP29	IRP28	IRP27	RESERVED		IRP24	IRP23	IRP22	IRP21	IRP20	IRP19	IRP18	IRP17	IRP16
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-7 MIOS14PR1 Bit Descriptions

Bit(s)	Name	Description
15:11	IRP31:27	Flag Bits — MDASM flag bits [15:11]
10:9	—	Reserved
8:6	IRP24:22	Flag Bits — MMCSM flag bits [8:6]
5:0	IRP21:16	Flag Bits — PWMSM flag bits [5:0]

This register is a read only register that contains the interrupt pending bits for the submodules. Each bit corresponds to a given submodule. When one of these bits is set, it means that a submodule raised its flag and the corresponding enable was set.

As this register is read only, a write to this register has no other effect than generating a bus error if the bus error option is selected.

17.9.6 MBISM Interrupt Registers

17.9.6.1 MIOS14LVL0 Register

MIOS14LVL0 — Interrupt Level 0 Register **0x30 6C30**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED					LVL2	LVL1	LVL0	TM1	TM0	RESERVED					
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-8 MIOS14LVL0 Bit Descriptions

Bit(s)	Name	Description
15:11	—	Reserved
10:8	LVL2 — LVL1	Interrupt Level 2-1 — Represent one of eight possible levels.
7:6	TMM1 — TM0	Only used in the case of non-vectored interrupt to determine the mulitplexed time slot. Read/write unused bits in the case of vectored interrupt.
5:0	—	Reserved

This register contains the interrupt level that apply to the submodules number 15 to 0.

17.9.6.2 MIOS14LVL1 Register

MIOS14LVL1 — Interrupt Level 1 Register **0x30 6C70**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED					LVL2	LVL1	LVL0	TM1	TM0	RESERVED					
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-9 MIOS14LVL1 Bit Descriptions

Bit(s)	Name	Description
15:11	—	Reserved
10:8	LVL2 — LVL1	Interrupt Level 2-1 — Represent one of eight possible levels.
7:6	TMM1 — TM0	Only used in the case of non-vectored interrupt to determine the mulitplexed time slot. Read/write unused bits in the case of vectored interrupt.
5:0	—	Reserved

This register contains the interrupt level that apply to the submodules number 31 to 16.

17.9.7 Interrupt Control Section (ICS)

The function of the interrupt control section is to deliver the level and the vector, if the vectored interrupt is concerned, to the CPU. An interrupt control section adapts the

characteristics of the MIOB request bus to the characteristics of the interrupt structure of the peripheral bus.

17.9.7.1 Non-Vectored Interrupt

This ICS mode is used when the MIOS is connected to a processor that does not run an IACK cycle.

When at least one of the bits is set in an IRQ pending register, the ICS receives a signal. This signal is the result of a logical “OR” between all the bits of the IRQ pending register.

Each signal received from the IRQ pending register is associated with an interrupt level register within the ICS. This level is coded on five bits in this register: three bits represent one of eight levels and the two other ones represent the four time multiplex slots. According to this level, the ICS sets the correct IRQ[7:0] lines with the correct ILBS[1:0] time multiplex lines on the peripheral bus. The CPU is then informed of which of the 32 interrupt levels is requested.

Based on the interrupt level requested, the software must determine which submodule requested the interrupt. The software may use a find-first-one type of instruction to determine, in the concerned RQSM, which bit is set. The CPU can then serve the requested interrupt.

17.10 Bus Interface Submodule (MBISM)

17.10.1 MBISM Overview Description

The MIOS bus interface submodule (MBISM) is used as an interface between the MIOB (modular I/O bus) and the peripheral bus. It allows the CPU to communicate with the MIOS14 submodules.

17.10.2 MBISM Registers

All MBISM registers are supervisor access only.

17.10.2.1 MBISM Registers Organization

Table 17-10 MBISM Registers

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0x30 6800	MIOS14 Test and Pin Control Register (MIOS14TPCR)															
0x03 6802	MIOS14 Vector Register (MIOS14VECT)															
0x03 6804	MIOS14 Module-Version Number Register (MIOS14VNR)															
0x03 6806	MIOS14 Module Control Register (MIOS14MCR)															
0x03 6808	Reserved															
0x03 680A	Reserved															
0x03 680C	Reserved															
0x03 680E	Reserved															

17.10.2.2 MIOS14 Test and Pin Control Register (MIOS14TPCR)

MIOS14TPCR — Test and Pin Control Register **0x30 6800**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
TEST	RESERVED							VMUX[7:5]			PWM	RESERVED	CCAN	VF	VFLS
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-11 MIOS14TPCR Bit Descriptions

Bit(s)	Name	Description
15	—	Test — This bit is used for MIOS14 factory testing and should always be programmed to a 0.
14:8	—	Reserved
7:5	VMUX7 — VMUX5	Pin Multiplex — These bits are unused on MPC565 / MPC566.
4	PWM	PWM Pin Multiplex — This bit controls the function of the following pins: mpwm20_mpio32b11, mpwm21_mpio32b12, mpwm4_mpio32b5, mpwm5_mpio32b6. 1 = PWM function is selected (mpwm4, mpwm5, mpwm20, mpwm21) 0 = MIOS General Purpose I/O is selected (mpio32b5, mpio32b6, mpio32b11, mpio32b12)
3	—	This bit should be set to 0.
2	CCAN	TOUCAN_C Pin Multiplex — This bit controls the function of the following pins: c_cntx0_mpio32b13 c_cnrx0_mpio32b14 1 = TOUCAN_C function is selected (c_cntx0, c_cnrx0) 0 = MIOS General Purpose I/O is selected (mpio32b13, mpio32b14)
1	VF	VF Pin Multiplex — This bit controls the function of the VF pins (vf0_mpio32b0, vf1_mpio32b1, vf2_mpio32b2) 1 = VF function is selected (vf[0:2]) 0 = MIOS General Purpose I/O is selected (mpio32b0, mpio32b1, mpio32b2)
0	VFLS	VFLS Pin Multiplex — This bit controls the function of the VFLS pins (vfls0_mpio32b3, vfls1_mpio32b4) 1 = VFLS function is selected (vfls[0:1]) 0 = MIOS General Purpose I/O is selected (mpio32b0, mpio32b1, mpio32b2)

This register is used for MIOS14 factory testing and to specify the pin usage. Note that this register does not control the pin multiplexing of the MIOS GPIO pins which are shared with the READI MDO function (mdo_4_mpio32b10, mdo_5_mpio32b9, mdo_6_mpio32b8, mdo_7_mpio32b7). These pins are controlled by the READI module.

17.10.2.3 MIOS14 Vector Register (MIOS14VECT)

MIOS14VECT— Vector Register **0x30 6802**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED								VECT	VECT	VECT	VECT	RESERVED			
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-12 MIOS14VECT Bit Descriptions

Bit(s)	Name	Description
15:8	—	Reserved
7:4	VECT7 — VECT5	Interrupt Vectors MSBs — These bits are not used on the MPC565 / MPC566.
3:0	—	Reserved

17.10.2.4 MIOS14 Module-Version Number Register (MIOS14VNR)

This register is read only, and contains the hard-coded values of the version and module number. These values are different for each implementation and allow a tracking of module numbers and versionning.

MIOS14VNR — Module-Version Number Register **0x30 6804**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
MN7	MN6	MN5	MN4	MN3	MN2	MN1	MN0	VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0
SRESET:															
0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0

Table 17-13 MIOS14VNR Bit Descriptions

Bit(s)	Name	Description
15:8	MN7 — MN0	Module Number — These bits represent the module number. In the MPC565 / MPC566 the module number is 0xE.
7:0	VN7 — VN0	Version Number — These bits represent the version number of the described module.This has a value of 0x01 in the K85H mask set of the MPC565 / MPC566 and may be incremented in the future.

17.10.2.5 MIOS14 Module Configuration Register (MIOS14MCR)

The MIOS14MCR register is a collection of read/write stop, freeze, reset and supervisor bits, as well as interrupt arbitration number bits. These bits are detailed in **Table 17-14**.

MIOS14MCR— Module Configuration Register **0x30 6806**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
STOP	RSVD	FRZ	RST	RESERVED				SUPV	RESERVED						
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-14 MIOS14MCR Bit Descriptions

Bit(s)	Name	Description
15	STOP	Stop enable — The STOP bit, while asserted, activates the MIOB freeze signal regardless of the state of the IMB3 FREEZE signal. The MIOB freeze signal is further validated in some submodules with internal freeze enable bits in order for the submodule to be stopped. The MBISM continues to operate to allow the CPU access to the submodule's registers. The MIOB freeze signal remains active until reset or until the STOP bit is written to zero by the CPU (via the IMB3). The STOP bit is cleared by reset. 0 = Allows MIOS14 operation. 1 = Selectively stops MIOS14 operation.
14	—	Reserved
13	FRZ	Freeze enable — The FRZ bit, while asserted, activates the MIOB freeze signal only when the IMB3 FREEZE signal is active. The MIOB freeze signal is further validated in some submodules with internal freeze enable bits in order for the submodule to be frozen. The MBISM continues to operate to allow the CPU access to the submodule's registers. The MIOB freeze signal remains active until the FRZ bit is written to zero or the IMB3 FREEZE signal is negated. The FRZ bit is cleared by reset. 0 = Ignores the FREEZE signal on the IMB3, allows MIOS14 operation. 1 = Selectively stops MIOS14 operation when the FREEZE signal appears on the IMB3.
12	RST	Module reset — The RST bit is always read as 0 and can be written to 1. When the RST bit is written to 1, the MBISM activates the vs_rst signal on the MIOB. This completely stops the operation of the MIOS14 and reset all the values in the submodules registers that are affected by reset. This bit provides a way of resetting the complete MIOS14 module regardless of the reset state of the CPU. The RST bit is cleared by reset. 0 = Writing a 0 to RST has no effect. 1 = Reset the MIOS14 submodules.
11:8	—	Reserved
7	SUPV	Supervisor data space selector — The SUPV bit tells if the address space from (0x30 6000) to (0x30 67FF) in the MIOS14 is accessed at the supervisor privilege level (See the address map on **Figure 17-1**). When cleared, these addresses are accessed at the unrestricted privilege level. 0 = Unrestricted Data Space. 1 = Supervisor Data Space. The SUPV bit is cleared by reset.
6:0	—	Reserved. These bits are used for the IARB (interrupt arbitration ID) field in TPU3 implementations that use hardware interrupt arbitration.

17.11 Counter Prescaler Submodule (MCPSM)

17.11.1 MCPSM Overview Description

The MIOS counter prescaler submodule (MCPSM) divides the MIOS14 clock (f_{SYS}) to generate the counter clock. It is designed to provide all the submodules with the same division of the main MIOS14 clock (division of f_{SYS}). It uses a 4-bit modulus counter. The clock signal is prescaled by loading the value of the clock prescaler register into

the prescaler counter every time it overflows. This allows all prescaling factors between two and 16. Counting is enabled by asserting the PREN bit in the control register. The counter can be stopped at any time by negating this bit, thereby stopping all submodules using the output of the MCPSM (counter clock). A block diagram of the MCPSM is given in **Figure 17-10**.

The following sections describe the MCPSM in detail.

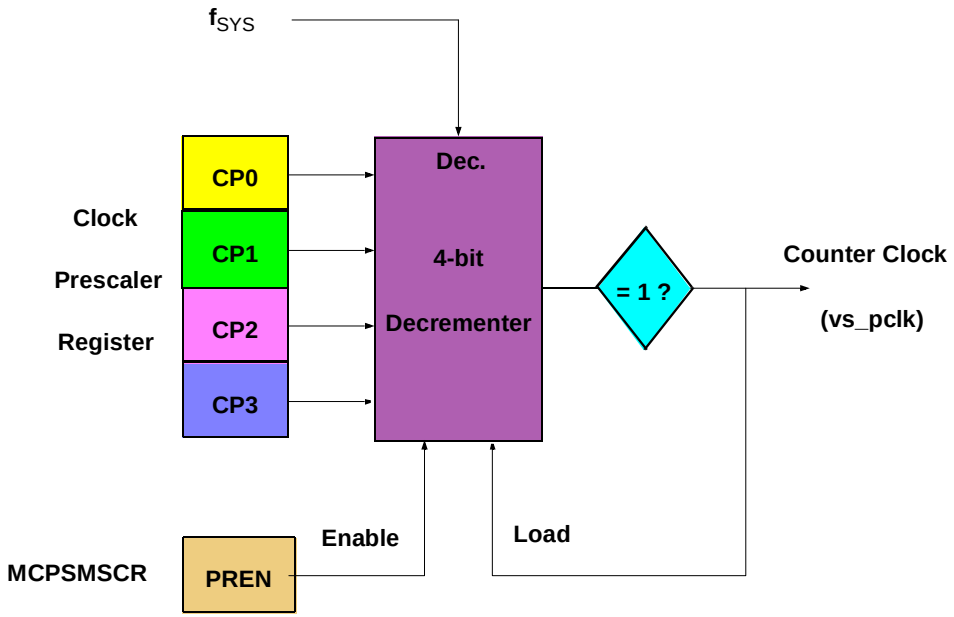


Figure 17-10 MCPSM Block Diagram

17.11.1.1 MCPSM features

- Centralized counter clock generator
- Programmable 4-bit modulus down-counter
- Wide range of possible division ratios:
  2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 or 16
- Count inhibit under software control

17.11.1.2 MCPSM Pin Functions

The MCPSM has no associated external pins.

17.11.1.3 Modular I/O Bus (MIOB) Interface

- The MCPSM is connected to all the signals in the read/write and control bus, to allow data transfer from and to the MCPSM registers, and to control the MCPSM in the different possible situations.
- The MIOS counter prescaler submodule does not use any 16-bit counter bus.

• The MIOS counter prescaler submodule does not use the request bus.

17.11.2 Effect of RESET on MCPSM

When the RESET signal is asserted, all the bits in the MCPSM status and control register are cleared.

NOTE

The MCPSM is still disabled after the RESET signal is negated and counting must be explicitly enabled by asserting the PREN bit.

17.11.3 MCPSM Registers

The privilege level to access to the MCPSM registers is supervisor only.

17.11.3.1 MCPSM Registers Organization

MCPSM— Register Organization

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
0x30 6810	Reserved														
0x30 6812	Reserved														
0x30 6814	Reserved														
0x30 6816	MCPSM Status/Control Register (MCPSMSCR)														

17.11.3.2 MCPSMSCR — MCPSM Status/Control Register

MCPSMSCR — MCPSM Status/Control Register **0x30 6816**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PREN	FREN	RESERVED										PSL3	PSL2	PSL1	PSL0
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-15 MCPSMSCR Bit Descriptions

Bit(s)	Name	Description
0	PREN	Prescaler enable bit — This active high read/write control bit enables the MCPSM counter. The PREN bit is cleared by reset. 1 = MCPSM counter enabled. 0 = MCPSM counter disabled.
1	FREN	Freeze bit — This active high read/write control bit when set make possible a freeze of the MCPSM counter if the MIOB freeze line is activated: note that this line is active when the MIOS14MCR STOP bit is set or when the MIOS14MCR FREN bit and the IMB3 FREEZE line are set. When the MCPSM is frozen, its stops counting. Then when the FREN bit is reset or when the freeze condition on the MIOB is negated, the counter restart from where it was before to freeze. The FREN bit is cleared by reset. 1 = MCPSM counter frozen if MIOB freeze active. 0 = MCPSM counter not frozen.

Table 17-15 MCPSMSCR Bit Descriptions (Continued)

Bit(s)	Name	Description
2:11	—	Reserved
12:15	PSL3 — PSL0	Clock prescaler — This 4-bit read/write data register stores the modulus value for loading into the clock prescaler. The new value is loaded into the counter on the next time the counter equals one or when disabled (PREN bit at “0”).

Table 17-16 Clock Prescaler Setting

PSL3-PSL0 Value	Divide ratio
0x0	16
0x1	No counter clock output (vs_pclk signal is set to 0)
0x2	2
0x3	3
...	...
0xE	14
0xF	15

Note that if the binary value %0001 is entered in PSL3 — PSL0, the output signal is stuck at zero, no clock is output.

17.12 Modulus Counter Submodule (MMCSM)

In this section the values taken by the bits in the registers are given according to the following rule:

- 0 -> reset (negated)
- 1 -> set (asserted)
- u -> undefined
- - -> unaffected

17.12.1 MMCSM Overview Description

The MMCSM is a versatile counter submodule capable of performing complex counting and timing functions, including modulus counting, in a wide range of applications. The MMCSM may also be configured as an event counter, allowing the overflow flag to be set after a predefined number of events (internal clocks or external events), or as a time source for other submodules.

NOTE

The MMCSM can also operate as a free running counter by loading the modulus value of zero.

The main components of the MMCSM are an 8-bit prescaler counter, an 8-bit prescaler register, a 16-bit up-counter register, a 16-bit modulus latch register, counter loading and interrupt flag generation logic.

The contents of the modulus latch register is transferred to the counter under the following three conditions:

1. When an overflow occurs
2. When an appropriate transition occurs on the external load pin
3. When the program writes to the counter register. In this case, the value is first written into the modulus register and immediately transferred to the counter.

Software can also write a value to the modulus register for later loading into the counter with one of the two first criteria.

A software control register selects whether the clock input to the counter is one of the prescaler outputs or the corresponding input pin. The polarity of the external input pin is also programmable.

The following sections describe the MMCSM in detail. A block diagram of the MMCSM is shown in **Figure 17-11**.

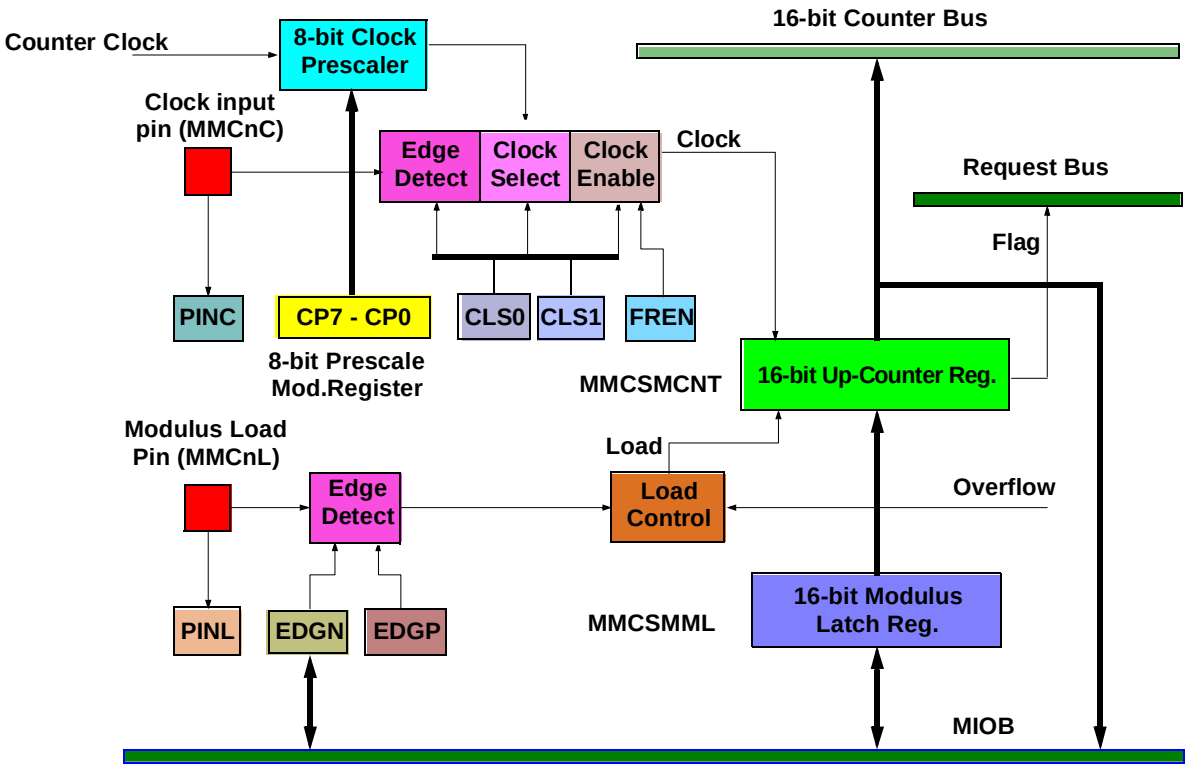


Figure 17-11 MMCSM Block Diagram

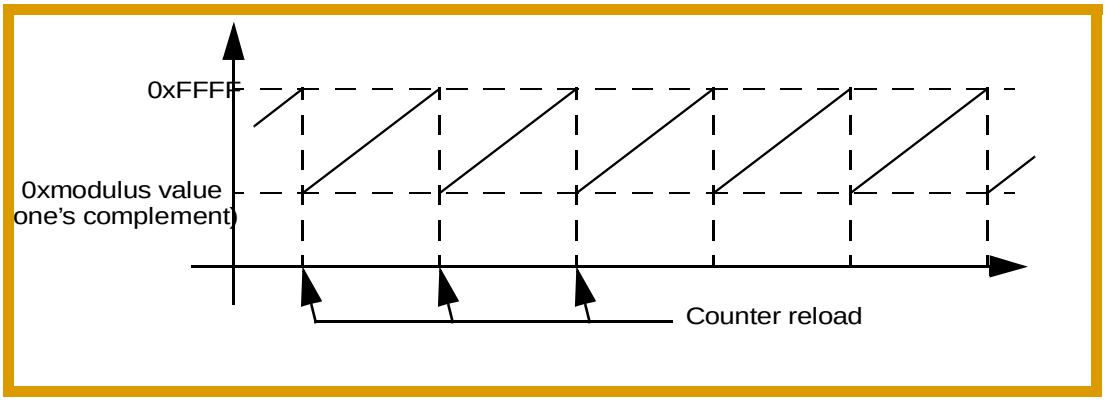


Figure 17-12 MMCSM Modulus Up-Counter

17.12.2 MMCSM features

- Programmable 16-bit modulus up-counter with a built-in programmable 8-bit prescaler clocked by MCPSM
- Maximum increment frequency of the counter:
  - clocked by the internal MCPSM output: f_{SYS} / 2
  - clocked by the external pin: f_{SYS} / 4
- Flag setting and possible interrupt generation on overflow of the up-counter register
- Time counter on internal clock with interrupt capability after a pre-determined time
- External event counter (pulse accumulator) with overflow and interrupt capability after a pre-determined number of external events
- Usable as a regular free-running up-counter
- Capable of driving a dedicated 16-bit counter bus to provide timing information to action submodules (the value driven is the contents of the 16-bit up-counter register)
- Optional pin for counting external events
- Optional pin to externally force a load of the modulus counter

17.12.2.1 MMCSM Pin Functions

The MMCSM has two dedicated external pins.

An external modulus load pin (MMCnL) allows the modulus value stored in the modulus latch register (MMCSMML) to be loaded into the up-counter register (MMCSMCNT) at any time. Both rising and falling edges of the load signal may be used, according to the EDGEP and EDGEN bit settings in the MMCSMSCR.

An external event clock pin (MMCnC) can be selected as the clock source for the up-counter register (MMCSMCNT) by setting the appropriate bits (CLS0 and CLS1) in the status/control register (MMCSMSCR). Either rising or falling edge may be used according to the setting of these bits.

When the external clock source is selected, the MMCSM is in the event counter mode. The counter can simply counts the number of events occurring on the input pin. Alternatively, the MMCSM can be programmed to generate an interrupt when a predefined number of events have been counted; this is done by presetting the counter with the *complement value of the desired number of events*.

17.12.3 MMCSM Prescaler

The built-in prescaler consists of a 8-bit modulus counter, clocked by the MCPSM output. It is loaded with an 8-bit value every time the counter overflows or whenever the prescaler output is selected as the clock source. This 8-bit value is stored in the MMCSMSCR bits CP7 — CP0. The prescaler overflow signal is used to clock the MMCSM up-counter. This allows the MMCSMCNT to be incremented at the MCPSM output frequency divided by a value between one and 256.

17.12.4 Modular I/O Bus (MIOB) Interface

- The MMCSM is connected to all the signals in the read/write and control bus, to allow data transfer from and to the MMCSM registers, and to control the MMCSM in the different possible situations.
- The MMCSM drives a dedicated 16-bit counter bus with the value currently in the up-counter register
- The MMCSM uses the request bus to transmit the FLAG line to the request submodule (RQSM). A flag is set when an overflow has occurred in the up-counter register.

17.12.5 Effect of RESET on MMCSM

When the RESET signal is asserted, only the FREN, EDGP, EDGN, CLS1 and CLS0 bits in the MMCSMSCR are cleared. The clock prescaler (CP7-CP0), PINC and PINL bits in the same register are not cleared.

- The PINC and PINL bits in the MMCSMSCR always reflect the state of the appropriate external pins.
- The MMCSM is disabled after reset and must be explicitly enabled by selecting a clock source using the CLS1-CLS0 bits.

The MMCSMCNT and the MMCSMML, together with the clock prescaler register bits, must be initialized by software, since they are undefined after a hardware reset. A modulus value must be written to the MMCSMCNT (which also writes into the MMCSMML) before the MMCSMSCR is written to. The latter access initializes the clock prescaler.

17.12.6 MMCSM Registers

The privilege level to access to the MMCSM registers depends on the MIOS14MCR SUPV bit. The privilege level is unrestricted after reset and can be change to supervisor by software.

17.12.7 MMCSM Register Organization

Table 17-17 MMCSM Address Map

Address	Register
MMCSM6	
0x30 6030	MMCSM6 Up-Counter Register (MMCSMCNT) See **Table 17-17** for bit descriptions.
0x30 6032	MMCSM6 Modulus Latch Register (MMCSMML) See **Table 17-19** for bit descriptions.
0x30 6034	MMCSM6 Status/Control Register Duplicated (MMCSMSCRD) See **17.12.8.3 MMCSM Status/Control Register (MMCSMSCR)** for bit descriptions.
0x30 6036	MMCSM6 Status/Control Register (MMCSMSCR). See **Table 17-20** for bit descriptions.
MMCSM7	
0x30 6038	MMCSM7 Up-Counter Register (MMCSMCNT)
0x30 603A	MMCSM7 Modulus Latch Register (MMCSMML)
0x30 603C	MMCSM7 Status/Control Register Duplicated (MMCSMSCRD)
0x30 603E	MMCSM7 Status/Control Register (MMCSMSCR)
MMCSM8	
0x30 6040	MMCSM8 Up-Counter Register (MMCSMCNT)
0x30 6042	MMCSM8 Modulus Latch Register (MMCSMML)
0x30 6044	MMCSM8 Status/Control Register Duplicated (MMCSMSCRD)
0x30 6046	MMCSM8 Status/Control Register (MMCSMSCR)
MMCSM22	
0x30 60B0	MMCSM22 Up-Counter Register (MMCSMCNT)
0x30 60B2	MMCSM22 Modulus Latch Register (MMCSMML)
0x30 60B4	MMCSM22 Status/Control Register Duplicated (MMCSMSCRD)
0x30 60B6	MMCSM22 Status/Control Register (MMCSMSCR)
MMCSM23	
0x30 60B8	MMCSM23 Up-Counter Register (MMCSMCNT)
0x30 60BA	MMCSM23 Modulus Latch Register (MMCSMML)
0x30 60BC	MMCSM23 Status/Control Register Duplicated (MMCSMSCRD)
0x30 60BE	MMCSM23 Status/Control Register (MMCSMSCR)

Table 17-17 MMCSM Address Map (Continued)

Address	Register
MMCSM24	
0x30 60C0	MMCSM24 Up-Counter Register (MMCSMCNT)
0x30 60C2	MMCSM24 Modulus Latch Register (MMCSMML)
0x30 60C4	MMCSM24 Status/Control Register Duplicated (MMCSMSCRD)
0x30 60C6	MMCSM24 Status/Control Register (MMCSMSCR)

17.12.8 MMCSM Up-Counter Register (MMCSMCNT)

MMCSMCNT — MMCSM Up-Counter Register

0x30 6030
0x30 6038
0x30 6040
0x30 60B0
0x30 60B8
0x30 60C0

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-18 MMCSMCNT Bit Descriptions

Bit(s)	Name	Description
0:15	CNT15 — CNT0	Counter value — These bits are read/write data bits representing the 16-bit value of the up-counter. It contains the value that is driven onto the 16-bit counter bus. **NOTE:** Writing to MMCSMCNT simultaneously writes to MMCSMML.

17.12.8.1 MMCSM Modulus Latch Register (MMCSMML)

MMCSMML — MMCSM Modulus Latch Register

0x30 6032
0x30 603A
0x30 6042
0x30 60B2
0x30 60BA
0x30 60C2

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
ML15	ML14	ML13	ML12	ML11	ML10	ML9	ML8	ML7	ML6	ML5	ML4	ML3	ML2	ML1	ML0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-19 MMCSMML Bit Descriptions

Bit(s)	Name	Description
0:15	ML15 — ML0	Modulus latches — These bits are read/write data bits containing the 16-bit modulus value to be loaded into the up-counter. The value loaded in this register must be the one's complement of the desired modulus count. The up-counter increments from this one's complement value up to 0xFFFF to get the correct number of steps before an overflow is generated to reload the modulus value into the up-counter.

17.12.8.2 MMCSMSCRD — MMCSM Status/Control Register (Duplicated)

The MMCSMSCRD and the MMCSMSCR are the same registers accessed at two different addresses.

Reading or writing to one of these two addresses has exactly the same effect.

The duplication of the SCR register allows coherent 32-bit accesses when using a RCPU.

WARNING

The user should not write directly to the address of the MMCSMSCRD. This register's address may be reserved for future use and should not be accessed by the software to ensure future software compatibility.

17.12.8.3 MMCSM Status/Control Register (MMCSMSCR)

The status/control register (SCR) is a collection of read-only pin status bits, read/write control bits and an 8-bit read/write data register, as detailed below.

MMCSMSCR — MMCSM Status/Control Register

0x30 6036
0x30 603E
0x30 6046
0x30 60B6
0x30 60BE
0x30 60C6

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PINC	PINL	FREN	EDGN	EDGP	CLS1	CLS0	RSVD	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-20 MMCSMSCR Bit Descriptions

Bit(s)	Name	Description
0	PINC	Clock input pin status bit — This read-only status bit reflects the logic state of the clock input pin MMCnC.
1	PINL	Modulus load input pin status bit — This read-only status bit reflects the logic state of the modulus load pin MMCnL.

Table 17-20 MMCSMSCR Bit Descriptions (Continued)

Bit(s)	Name	Description
2	FREN	Freeze enable — This active high read/write control bit enables the MMCSM to recognize the MIOB freeze signal.
3	EDGN	Modulus load falling-edge sensitivity — This active high read/write control bit sets falling-edge sensitivity for the MMCnL pin, such that a high-to-low transition causes a load of the MMCSMCNT.
4	EDGP	Modulus load rising-edge sensitivity This active high read/write control bit sets rising-edge sensitivity for the MMCnL pin, such that a low-to-high transition causes a load of the MMCSMCNT. See **Table 17-21** for details about edge sensitivity.
5:6	CLS1 — CLS0	Clock select — These read/write control bits select the clock source for the modulus counter. Either the rising edge or falling edge of the clock signal on the MMCnC pin may be selected, as well as, the internal MMCSM prescaler output or disable mode (no clock source). See **Table 17-22** for details about the clock selection.
7	—	Reserved
8:15	CP7 — CP0	Clock prescaler — This 8-bit read/write data register stores the modulus value for loading into the built-in 8-bit clock prescaler. The new value is loaded into the prescaler counter on the next counter overflow, or upon setting the CLS1 — CLS0 bits for selecting the clock prescaler as the clock source. **Table 17-23** gives the clock divide ratio according to the CP7..CP0 values:

Table 17-21 MMCSMCNT Edge Sensitivity

EDGN	EDGP	Edge Sensitivity
1	1	MMCSMCNT load on rising and falling edges
1	0	MMCSMCNT load on falling edges
0	1	MMCSMCNT load on rising edges
0	0	None (disabled)

Table 17-22 MMCSMCNT Clock Signal

CLS1	CLS0	Clocking Selected
1	1	MMCSM clock prescaler
1	0	Clock pin rising-edge
0	1	Clock pin falling-edge
0	0	None (disable)

Table 17-23 Prescaler Values

Prescaler Value (CP7..CP0 in Hex)	MIOS14 Prescaler Clock Divided By:
FF	1
FE	2
FD	3
FC	4

Table 17-23 Prescaler Values

Prescaler Value (CP7..CP0 in Hex)	MIOS14 Prescaler Clock Divided By:
FB	5
FA	6
F9	7
F8	8
.....	.....
02	254 (2^8 -2)
01	255 (2^8 -1)
00	256 (2^8)

17.12.9 Double Action Submodule (MDASM)

In this section the values taken by the bits in the registers are given according to the following rule:

- 0 -> reset (negated))
- 1 -> set (asserted)
- u -> undefined
- - -> unaffected

17.12.10 MDASM Overview Description

The MIOS double action submodule (MDASM) is a function included in the MIOS library. It is a versatile 16-bit dual action submodule capable of performing two event operations before software intervention is required. It can perform two event operations such as PWM generation and measurement, input capture, output compare, etc.

The MDASM is composed of two timing channels (A and B), an output flip-flop, an input edge detector and some control logic. All control and status bits are contained in the MDASM status and control register.

The following sections describe the MDASM in detail. A block diagram of the MDASM is shown in **Figure 17-13**.

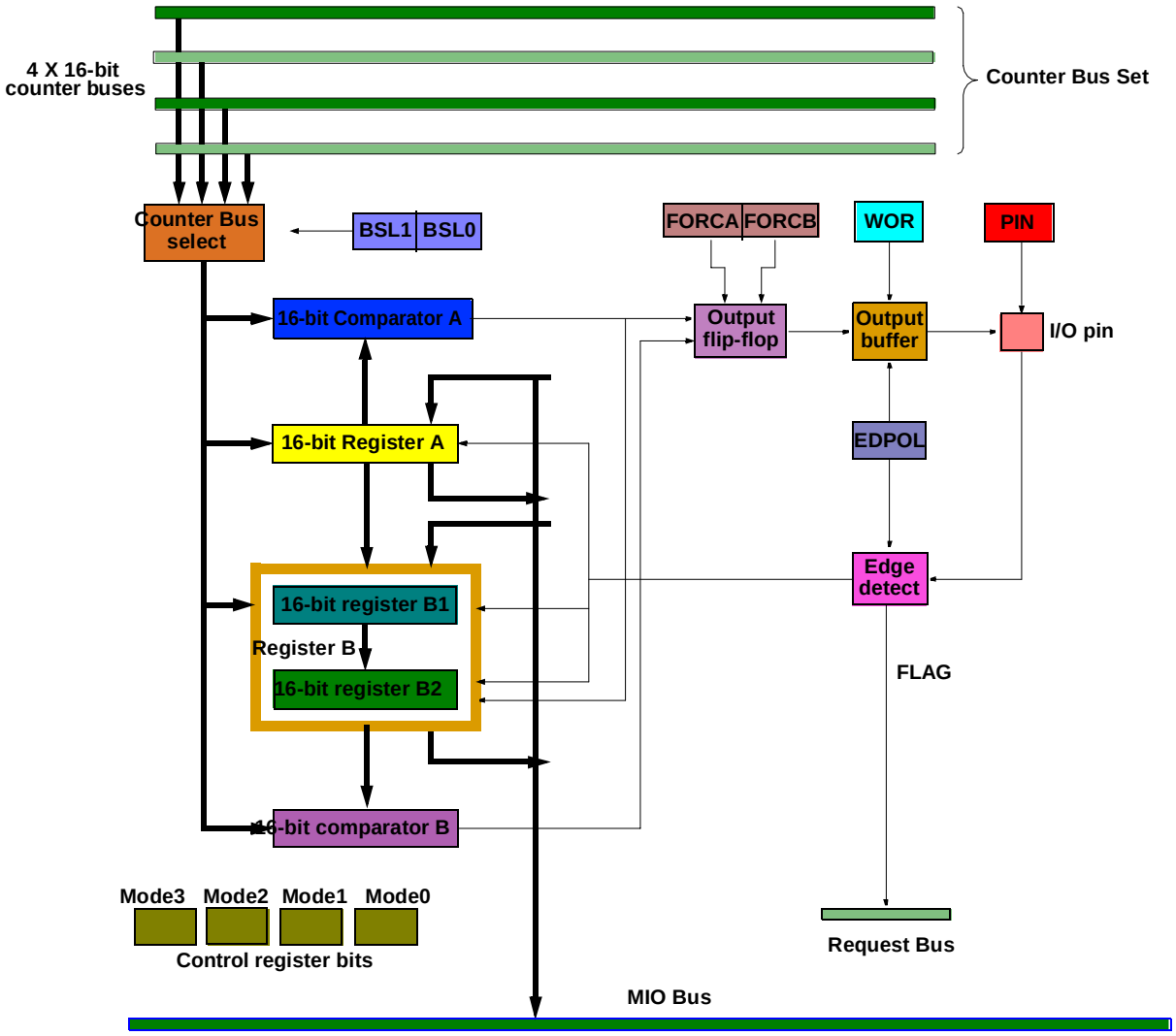


Figure 17-13 MDASM Block Diagram

17.12.11 MDASM Features

- Versatile 16-bit dual action unit allowing up to two events to occur before software intervention is required
- Six software selectable modes allowing the MDASM to perform pulse width and period measurements, PWM generation, single input capture and output compare operations as well as port functions
- Software selection of one of the four possible 16-bit counter buses used for timing operations
- Flag setting and possible interrupt generation after MDASM action completion
- Software selection of output pulse polarity
- Software selection of totem-pole or open-drain output
- Software readable output pin status

17.12.11.1 MDASM Pin Functions

The MDASM has one dedicated external pin. This pin is used in input or in output depending on the selected mode. When in input, it allows the MDASM to perform input capture, input pulse width measurement and input period measurement. When in output, it allows output compare, single shot output pulse, single output compare and output port bit operations as well as output pulse width modulation.

NOTE

In disable mode, the pin becomes a high impedance input and the input level on this pin is reflected by the state of the PIN bit in the MDASMSCR register.

17.12.12 MDASM Description

The MDASM contains two timing channels A and B associated with the same input/output pin. The dual action submodule is so called because its timing channel configuration allows two events (input capture or output compare) to occur before software intervention is required.

Six operating modes allow the software to use the MDASM's input capture and output compare functions to perform pulse width measurement, period measurement, single pulse generation and continuous pulse width generation, as well as standard input capture and output compare. The MDASM can also work as a single I/O pin. See **Table 17-24** for details.

Channel A comprises one 16-bit data register and one 16-bit comparator. Channel B also consists of one 16-bit data register and one 16-bit comparator, however, internally, channel B has two data registers B1 and B2, and the operating mode determines which register is accessed by the software:

- In the input modes (IPWM, IPM and IC), registers A and B2 are used to hold the captured values; in these modes, the B1 register is used as a temporary latch for channel B.
- In the output compare modes (OCB and OCAB), registers A and B2 are used to define the output pulse; register B1 is not used in these modes.
- In the output pulse width modulation mode (OPWM), registers A and B1 are used as primary registers and hidden register B2 is used as a double buffer for channel B.

Register contents are always transferred automatically at the correct time so that the minimum pulse (measurement or generation) is just one 16-bit counter bus count. The A and B data registers are always read/write registers, accessible via the MIOB.

In the input modes, the edge detect circuitry triggers a capture whenever a rising or falling edge (as defined by the EDPOL bit) is applied to the input pin. The signal on the input pin is Schmitt triggered and synchronized with the MIOS CLOCK.

In the disable mode (DIS) and in the input modes, the PIN bit reflects the state present on the input pin (after being Schmitt triggered and synchronized). In the output modes the PIN bit reflects the value present on the output flip-flop.

The output flip-flop is used in output modes to hold the logic level applied to the output pin.

The 16-bit counter bus selector is common to all input and output functions; it connects the MDASM to one of the four 16-bit counter buses available to that submodule instance and is controlled in software by the 16-bit counter bus selector bits BSL0 and BSL1 in the MDASMSCR register.

17.12.13 MDASM Modes of Operation

The mode of operation of the MDASM is determined by the mode select bits MODE[3:0] in the MDASMSCR register (see **Table 17-24**).

Table 17-24 MDASM Modes Of Operation

MODE[3:0]	Mode	Description of Mode
0000	DIS	Disabled — Input pin is high impedance; PIN gives state of the input pin.
0001	IPWM	Input pulse width measurement — Capture on the leading edge and the trailing edge of an input pulse.
0010	IPM	Input period measurement — Capture two consecutive rising/falling edges.
0011	IC	Input capture — Capture when the designated edge is detected.
0100	OCB	Output compare, flag line activated on B compare — Generate leading and trailing edges of an output pulse.
0101	OCAB	Output compare, flag line activated on A and B compare — Generate leading and trailing edges of an output pulse.
1xxx	OPWM	Output pulse width modulation — Generate continuous PWM output with 7, 9, 11, 12, 13, 14, 15 or 16 bits of resolution.

To avoid spurious interrupts, and to make sure that the FLAG line is activated according to the newly selected mode, the following sequence of operations should be adopted when changing mode:

1. Disable MDASM interrupts (by resetting the enable bit in the relevant RQSM)
2. Change mode (via disable mode)
3. Reset the corresponding FLAG bit in the relevant RQSM
4. Re-enable MDASM interrupts (if desired)

NOTE

When changing between output modes, it is not necessary to follow this procedure, as in these modes the FLAG bit merely indicates to the software that the compare value can be updated. However

changing modes without passing via the disable mode does not guarantee the subsequent functionality.

17.12.13.1 Disable (DIS) Mode

The disable mode is selected by setting MODE[3:0] to 0000.

In this mode, all input capture and output compare functions of the MDASM are disabled and the FLAG line is maintained inactive, but the input port pin function remains available. The associated pin becomes a high impedance input and the input level on this pin is reflected by the state of the PIN bit in the MDASMSCR register. All control bits remain accessible, allowing the software to prepare for future mode selection. Data registers A and B are accessible at consecutive addresses. Writing to data register B stores the same value in registers B1 and B2.

WARNING

When changing modes, it is imperative to go through the DIS mode in order to reset the MDASM's internal functions properly. Failure to do this could lead to invalid and unexpected output compare or input capture results, and to flags being set incorrectly.

17.12.13.2 Input Pulse Width Measurement (IPWM) Mode

IPWM mode is selected by setting MODE[3:0] to 0001.

This mode allows the width of a positive or negative pulse to be determined by capturing the leading edge of the pulse on channel B and the trailing edge of the pulse on channel A; successive captures are done on consecutive edges of opposite polarity. The edge sensitivity is selected by the EDPOL bit in the MDASMSCR register.

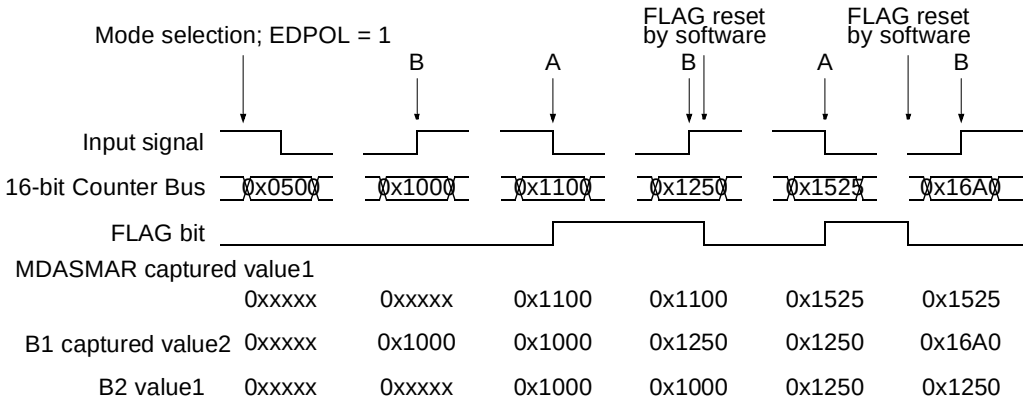
This mode also allows the software to determine the logic level on the input pin at any time by reading the PIN bit in the MDASMSCR register.

The channel A input capture function remains disabled until the first leading edge triggers the first input capture on channel B. When this leading edge is detected, the count value of the 16-bit counter bus selected by the BSL[1:0] bits is latched in the 16-bit data register B1; the FLAG line is not activated. When the next trailing edge is detected, the count value of the 16-bit counter bus is latched into the 16-bit data register A and, at the same time, the FLAG line is activated and the contents of register B1 are transferred to register B2. Reading data register B returns the value in register B2. If subsequent input capture events occur while the FLAG bit is set in the corresponding RQSM, data registers A and B will be updated with the latest captured values and the FLAG line will remain active.

If a 32-bit coherent operation is in progress when the trailing edge is detected, the transfer from B1 to B2 is deferred until the coherent operation is completed. Operation of the MDASM then continues on channels B and A as previously described.

The input pulse width is calculated by subtracting the value in data register B from the value in data register A.

Figure 17-14 provides an example of how the MDASM can be used for input pulse width measurement.



Notes: 1. These values are accessible to the software.
2. These values are internal and are not accessible.

Figure 17-14 Input Pulse Width Measurement Example

17.12.14 Input Period Measurement (IPM) Mode

IPM mode is selected by setting MODE[3:0] to 0010.

This mode allows the period of an input signal to be determined by capturing two consecutive rising edges or two consecutive falling edges; successive input captures are done on consecutive edges of the same polarity. The edge polarity is defined by the EDPOL bit in the MDASMSCR register.

This mode also allows the software to determine the logic level on the input pin at any time by reading the PIN bit in the MDASMSCR register.

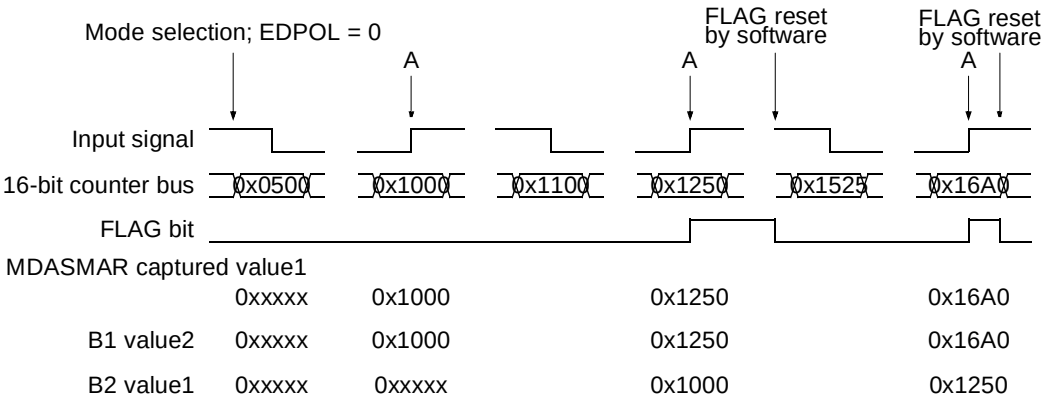
When the first edge having the selected polarity is detected, the 16-bit counter bus value is latched into the 16-bit data register A, the data in register B1 is transferred to data register B2 and finally the data in register A is transferred to register B1. On this first capture the FLAG line is not activated, and the value in register B2 is meaningless. On the second and subsequent captures, the FLAG line is activated when the data in register A is transferred to register B1.

When the second edge of the same polarity is detected, the counter bus value is latched into data register A, the data in register B1 is transferred to data register B2, the FLAG line is activated to signify that the beginning and end points of a complete period have been captured, and finally the data in register A is transferred to register B1. This sequence of events is repeated for each subsequent capture. Reading data register B returns the value in register B2.

If a 32-bit coherent operation is in progress when an edge (except for the first edge) is detected, the transfer of data from B1 to B2 is deferred until the coherent operation is completed. At any time, the input level present on the input pin can be read on the PIN bit.

The input pulse period is calculated by subtracting the value in data register B from the value in data register A.

Figure 17-15 provides an example of how the MDASM can be used for input period measurement.



Notes: 1. These values are accessible to the software.
2. These values are internal and are not accessible.

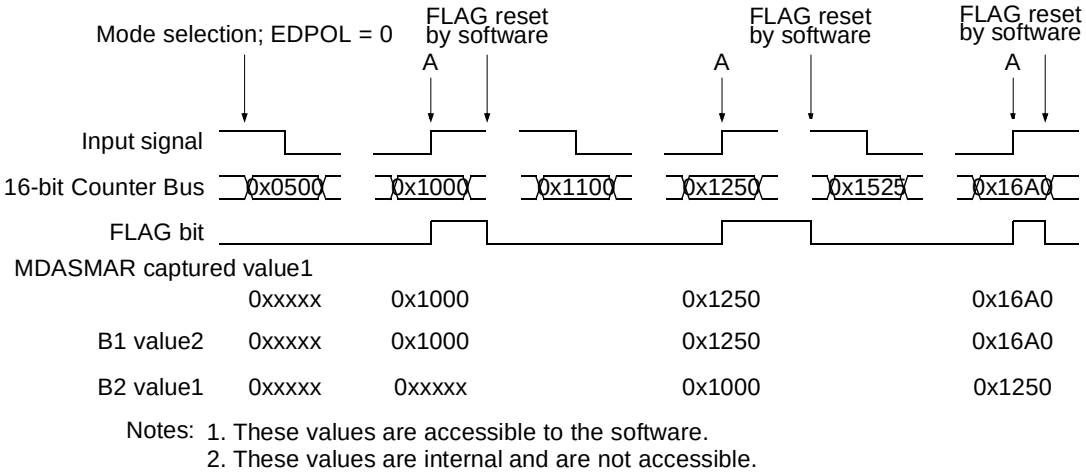
Figure 17-15 Input Period Measurement Example

17.12.15 Input Capture (IC) Mode

IC mode is selected by setting MODE[3:0] to 0011.

This mode is identical to the input period measurement mode (IPM) described above, with the exception that the FLAG line is also activated at the occurrence of the first detected edge of the selected polarity. In this mode the MDASM functions as a standard input capture function. In this case the value latched in channel B can be ignored.

Figure 17-16 provides an example of how the MDASM can be used for input capture.



Notes: 1. These values are accessible to the software.
2. These values are internal and are not accessible.

Figure 17-16 MDASM Input Capture Example

17.12.15.1 Output Compare (OCB and OCAB) Modes

Output compare mode (either OCA or OCB) is selected by setting MODE[3:0] to 010x. The MODE0 bit controls the activation criteria for the FLAG line, (i.e., when a compare occurs only on channel B or when a compare occurs on either channel).

This mode allows the MDASM to perform four different output functions:

- Single-shot output pulse (two edges), with FLAG line activated on the second edge
- Single-shot output pulse (two edges), with FLAG line activated on both edges
- Single-shot output transition (one edge)
- Output port pin, with output compare function disabled

In this mode the leading and trailing edges of variable width output pulses are generated by calculated output compare events occurring on channels A and B, respectively. OC mode may also be used to perform a single output compare function, or may be used as an output port bit.

In this mode, channel B is accessed via register B2. A write to register B2 writes the same value to register B1 even though the contents of B1 are not used in this mode. Both channels work together to generate one ‘single shot’ output pulse signal. Channel A defines the leading edge of the output pulse, while channel B defines the trailing edge of the pulse. FLAG line activation can be done when a match occurs on channel B only or when a compare occurs on either channel (as defined by the MODE0 bit in the MDASMSCR register).

When this mode is first selected, (i.e., coming from disable mode, both comparators are disabled). Each comparator is enabled by writing to its data register; it remains enabled until the next successful comparison is made on that channel, whereupon it

is disabled. The values stored in registers A and B are compared with the count value on the selected 16-bit counter bus when their corresponding comparators are enabled.

The output flip-flop is set when a match occurs on channel A. The output flip-flop is reset when a match occurs on channel B. The polarity of the output signal is selected by the EDPOL bit. The output flip-flop level can be obtained at any time by reading the PIN bit.

If subsequent enabled output compares occur on channels A and B, the output pulses continue to be output, regardless of the state of the FLAG bit.

At any time, the FORCA and FORCB bits allow the software to force the output flip-flop to the level corresponding to a comparison on channel A or B, respectively.

NOTE

The FLAG line is not affected by these ‘force’ operations.

Totem pole or open-drain output circuit configurations can be selected using the WOR bit in the MDASMSCR register.

NOTE 1

If both channels are loaded with the same value, the output flip-flop provides a logic zero level output and the flag bit is still set on the match.

NOTE 2

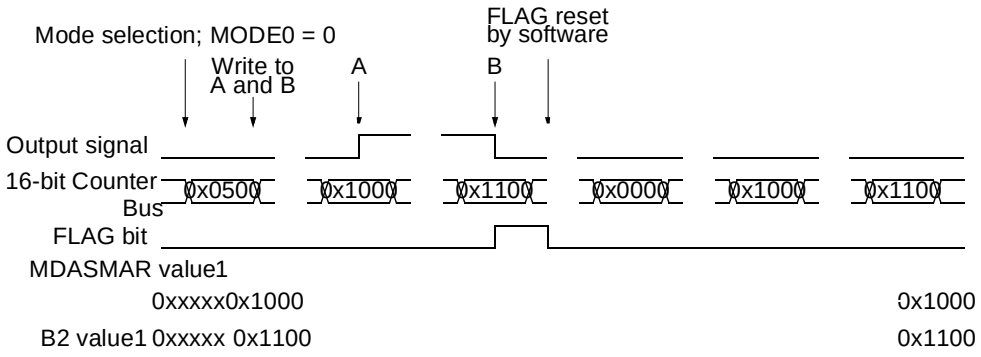
16-bit counter bus compare only occurs when the 16-bit counter bus is updated.

17.12.15.2 Single Shot Output Pulse Operation

The single shot output pulse operation is selected by writing the leading edge value of the desired pulse to data register A and the trailing edge value to data register B. A single pulse will be output at the desired time, thereby disabling the comparators until new values are written to the data registers. To generate a single shot output pulse, the OCB mode should be used to only generate a flag on the B match.

In this mode, registers A and B2 are accessible to the user software (at consecutive addresses).

Figure 17-17 provides an example of how the MDASM can be used to generate a single output pulse.



Note: 1. These values are accessible to the software.

Figure 17-17 Single Shot Output Pulse Example

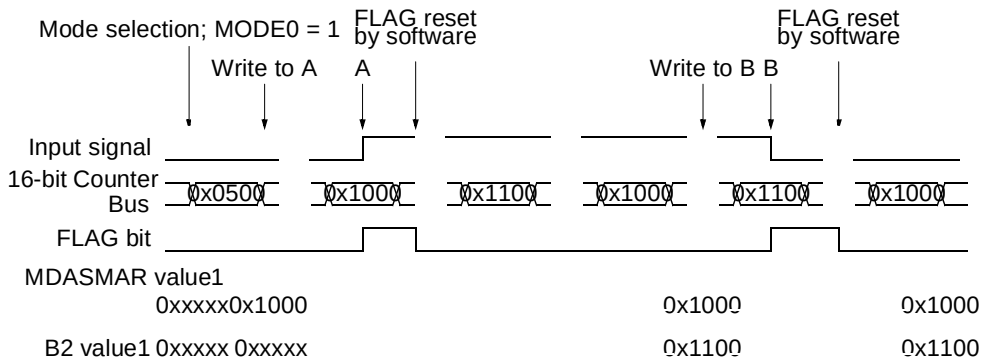
17.12.15.3 Single Output Compare operation

The single output compare operation is selected by writing to only one of the two data registers (A or B), thus enabling only one of the comparators. Following the first successful match on the enabled channel, the output level is fixed and remains at the same level indefinitely with no further software intervention being required. To generate a single output compare, the OCAB mode should be used to generate a flag on both the A and the B match.

NOTE

In this mode, registers A and B2 are accessible to the user software (at consecutive addresses).

Figure 17-18 provides an example of how the MDASM can be used to perform a single output compare.



Note: 1. These values are accessible to the software.

Figure 17-18 Single Shot Output Transition Example

17.12.15.4 Output Port Bit operation

The output port bit operation is selected by leaving both channels disabled, (i.e., by writing to neither register A nor B). The EDPOL bit alone controls the output value. The same result can be achieved by keeping EDPOL at zero and using the FORCA and FORCB bits to obtain the desired output level.

17.12.15.5 Output Pulse Width Modulation (OPWM) mode

OPWM mode is selected by setting MODE[3:0] to 1xxx. The MODE[2:0] bits allow some of the comparator bits to be masked.

This mode allows pulse width modulated output waveforms to be generated, with eight selectable frequencies. Frequencies are only relevant as such if the counter bus is driven by a counter as a time reference. Both channels (A and B) are used to generate one PWM output signal on the MDASM pin.

Channel B is accessed via register B1. Register B2 is not accessible. Channels A and B define respectively the leading and trailing edges of the PWM output pulse. The value in register B1 is transferred to register B2 each time a match occurs on either channel A or B.

NOTE

A FORCA or FORCB does not cause a transfer from B1 to B2.

The value loaded in register A is compared with the value on the 16-bit counter bus each time the counter bus is updated. When a match on A occurs, the FLAG line is activated and the output flip-flop is set. The value loaded in register B2 is compared with the value on the 16-bit counter bus each time the counter bus is updated. When a match occurs on B, the output flip-flop is reset.

NOTE

If both channels are loaded with the same value, when a simultaneous match on A and B occurs, the submodule behaves as if a simple match on B had occurred except for the FLAG line which is activated. The output flip-flop is reset and the value in register B1 is transferred to register B2 on the match.

The polarity of the PWM output signal is selected by the EDPOL bit. The output flip-flop level can be obtained at any time by reading the PIN bit.

If subsequent compares occur on channels A and B, the PWM pulses continue to be output, regardless of the state of the FLAG bit.

At any time, the FORCA and FORCB bits allow the software to force the output flip-flop to the level corresponding to a comparison on A or B respectively. Note that the FLAG line is not activated by the FORCA and FORCB operations.

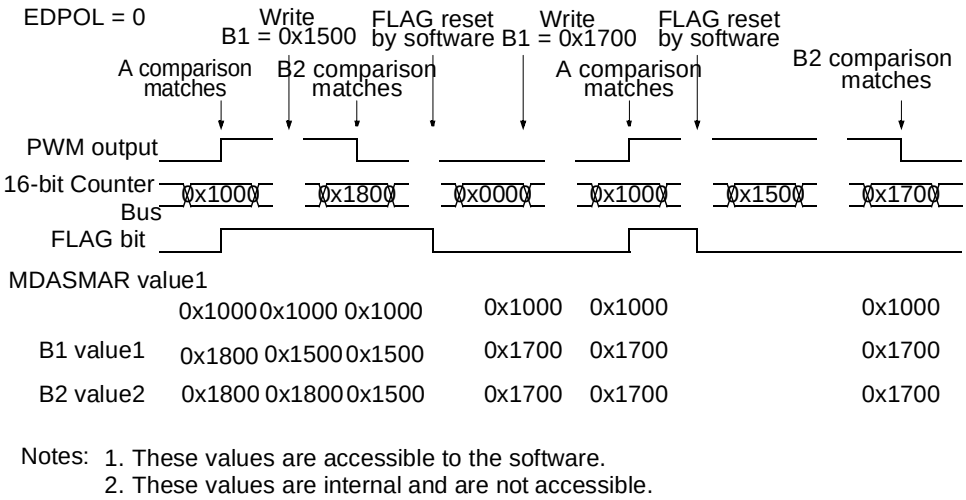
WARNING

Data registers A and B must be loaded with the values needed to produce the desired PWM output pulse.

NOTE

16-bit counter bus compare only occurs when the 16-bit counter bus is updated.

Figure 17-19 provides an example of how the MDASM can be used for pulse width modulation.



Notes: 1. These values are accessible to the software.
2. These values are internal and are not accessible.

Figure 17-19 MDASM Output Pulse Width Modulation Example

To generate PWM output pulses of different frequencies, the 16-bit comparator can have some of its bits masked. This is controlled by bits MODE2, MODE1 and MODE0. The frequency of the PWM output (f_{PWM}) is given by the following equation (assuming the MDASM is connected to a 16-bit counter bus used as time reference and f_{SYS} is the frequency of the MIOS CLOCK):

$$f_{PWM} = \frac{f_{SYS}}{N_{MCPSM} \bullet N_{COUNTER} \bullet N_{MDASM}} \quad [1]$$

where:

- N_{MCPSM} is the overall MCPSM clock divide ratio (2, 3, 4,...,16).
- $N_{COUNTER}$ is the divide ratio of the prescaler of the counter (used as a time reference) that drives the 16-bit counter bus.
- N_{MDASM} is the maximum count reachable by the counter when using n bits of resolution (this count is equal to 2^n).

A few examples of frequencies and resolutions that can be obtained are shown in **Table 17-25**.

Table 17-25 MDASM PWM Example Output Frequencies/Resolutions at $f_{[SYS]}$ = 40 MHz

Resolution (bits)	N_{MCPSM}	$N_{COUNTER}$	N_{MDASM}	PWM output frequency (Hz)[1]
16	16	256	65536	0.15
16	2	1	65536	305.17
15	16	256	32768	0.29
15	2	1	32768	610.35
14	16	256	16384	0.59
14	2	1	16384	1 220.70
13	16	256	8192	1.19
13	2	1	8192	2 441.41
12	16	256	4096	2.38
12	2	1	4096	4 882.81
11	16	256	2048	4.77
11	2	1	2048	9 765.63
9	16	256	512	19.07
9	2	1	512	39 062.50
7	16	256	128	76.29
7	2	1	128	156 250

NOTES:
1. This table is valid only if the MDASM is connected to an MMCSM operating as a free-running counter.

When using 16 bits of resolution on the comparator (MODE[2:0] = 000), the output can vary from a 0% duty cycle up to a duty cycle of 65535/65536. In this case it is not possible to have a 100% duty cycle. In cases where 16-bit resolution is not needed, it is possible to have a duty cycle ranging from 0% to 100%. Setting bit 15 of the value stored in register B to one results in the output being ‘always set’. Clearing bit 15 (to zero) allows normal comparisons to occur and the normal output waveform is obtained. Changes to and from the 100% duty cycle are done synchronously on an A or B match, as are all other width changes.

In the OPWM mode, the WOR bit selects whether the output is totem pole driven or open-drain.

17.12.16 Modular I/O Bus (MIOB) Interface

- The MDASM is connected to all the signals in the read/write and control bus, to allow data transfer from and to the MDASM registers, and to control the MDASM in the different possible situations.
- The MDASM is connected to four 16-bit counter buses available to that submod-

ule instance, so that the MDASM can select by software which one to use.

- The MDASM uses the request bus to transmit the FLAG line to the request sub-module (RQSM).

17.12.17 Effect of RESET on MDASM

When the RESET signal is asserted, the MDASM registers are reset according to the values specified in **17.12.18 MDASM Registers**.

17.12.18 MDASM Registers

The privilege level to access the MDASM registers depends on the MIOS14MCR SUPV bit. The privilege level is unrestricted after reset and can be changed to supervisor by software.

17.12.18.1 MDASM Registers Organization

The MDASM register map comprises four 16-bit register locations. As shown in below, the register block contains four MDASM registers. Note that the MDASMSCRD is the duplication of the MDASMSCR. This is done to allow 32-bit aligned accesses.

WARNING

Do not write directly to the address of the MDASMSCRD. This register's address may be reserved for future use and should not be accessed by the software to ensure future software compatibility.

All unused bits return zero when read by the software. All register addresses in this section are specified as offsets from the base address of the MDASM.

Table 17-26 MDASM Address Map

Address	Register
MDASM11	
0x30 6058	MDASM11 Data A Register (MDASMAR) See **17.12.18.2 MDASM DataA (MDASMAR) Register Bits** for bit descriptions.
0x30 605A	MDASM11 Data B Register (MDASMBR) See **17.12.18.3 MDASM DataB (MDASMBR) Register Bits** for bit descriptions.
0x30 605C	MDASM11 Status/Control Register Duplicated (MDASMSCRD) See **Table 17-29** for bit descriptions.
0x30 605E	MDASM11 Status/Control Register (MDASMSCR) See **Table 17-29** for bit descriptions.
MDASM12	
0x30 6060	MDASM12 Data A Register (MDASMAR)
0x30 6062	MDASM12 Data B Register (MDASMBR)
0x30 6064	MDASM12 Status/Control Register Duplicated (MDASMSCRD)
0x30 6066	MDASM12 Status/Control Register (MDASMSCR)

Table 17-26 MDASM Address Map (Continued)

Address	Register
MDASM13	
0x30 6068	MDASM13 Data A Register (MDASMAR)
0x30 606A	MDASM13 Data B Register (MDASMBR)
0x30 606C	MDASM13 Status/Control Register Duplicated (MDASMSCRD)
0x30 606E	MDASM13 Status/Control Register (MDASMSCR)
MDASM14	
0x30 6070	MDASM14 Data A Register (MDASMAR)
0x30 6072	MDASM14 Data B Register (MDASMBR)
0x30 6074	MDASM14 Status/Control Register Duplicated (MDASMSCRD)
0x30 6076	MDASM14 Status/Control Register (MDASMSCR)
MDASM15	
0x30 6078	MDASM15 Data A Register (MDASMAR)
0x30 607A	MDASM15 Data B Register (MDASMBR)
0x30 607C	MDASM15 Status/Control Register Duplicated (MDASMSCRD)
0x30 607E	MDASM15 Status/Control Register (MDASMSCR)
MDASM27	
0x30 60D8	MDASM27 Data A Register (MDASMAR)
0x30 60DA	MDASM27 Data B Register (MDASMBR)
0x30 60DC	MDASM27 Status/Control Register Duplicated (MDASMSCRD)
0x30 60DE	MDASM27 Status/Control Register (MDASMSCR)
MDASM28	
0x30 60E0	MDASM28 Data A Register (MDASMAR)
0x30 60E2	MDASM28 Data B Register (MDASMBR)
0x30 60E4	MDASM28 Status/Control Register Duplicated (MDASMSCRD)
0x30 60E6	MDASM28 Status/Control Register (MDASMSCR)
MDASM29	
0x30 60E8	MDASM29 Data A Register (MDASMAR)
0x30 60EA	MDASM29 Data B Register (MDASMBR)
0x30 60EC	MDASM29 Status/Control Register Duplicated (MDASMSCRD)
0x30 60EE	MDASM29 Status/Control Register (MDASMSCR)
MDASM30	
0x30 60F0	MDASM30 Data A Register (MDASMAR)
0x30 60F2	MDASM30 Data B Register (MDASMBR)
0x30 60F4	MDASM30 Status/Control Register Duplicated (MDASMSCRD)
0x30 60F6	MDASM30 Status/Control Register (MDASMSCR)
MDASM31	
0x30 60F8	MDASM31 Data A Register (MDASMAR)
0x30 60FA	MDASM31 Data B Register (MDASMBR)
0x30 60FC	MDASM31 Status/Control Register Duplicated (MDASMSCRD)
0x30 60FE	MDASM31 Status/Control Register (MDASMSCR)

17.12.18.2 MDASM DataA (MDASMAR) Register Bits

MDASMAR — MDASM DataA Register

0x30 6058
0x30 6060
0x30 6068
0x30 6070
0x30 6078
0x30 60D8
0x30 60E0
0x30 60E8
0x30 60F0
0x30 60F8

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-27 MDASMAR Bit Descriptions

Bit(s)	Name	Description
0:15	AR15 — AR0	MDASMAR is the data register associated with channel A; its use varies with the different modes of operation: In the DIS mode, MDASMAR can be accessed to prepare a value for a subsequent mode selection. In the IPWM mode, MDASMAR contains the captured value corresponding to the trailing edge of the measured pulse. In the IPM and IC modes, MDASMAR contains the captured value corresponding to the most recently detected dedicated edge (rising or falling edge). In the OCB and OCAB modes, MDASMAR is loaded with the value corresponding to the leading edge of the pulse to be generated. Writing to MDASMAR in the OCB and OCAB modes also enables the corresponding channel A comparator until the next successful comparison. In the OPWM mode, MDASMAR is loaded with the value corresponding to the leading edge of the PWM pulse to be generated. **NOTE:** In IC, IPM, or IPWM mode, when a read to register A or B occurs at the same time as a counter bus capture into that register and the counter bus is changing value, then the counter bus capture to that register is delayed.

17.12.18.3 MDASM DataB (MDASMBR) Register Bits

MDASMBR — MDASM DataB Register

0x30 605A
0x30 6062
0x30 606A
0x30 6072
0x30 607A
0x30 60DA
0x30 60E2
0x30 60EA
0x30 60F2
0x30 60FA

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-28 MDASMBR Bit Descriptions

Bit(s)	Name	Description
0:15	BR15 — BR0	MDASMBR is the data register associated with channel B; its use varies with the different modes of operation. Writing to register B always writes to B1 and, depending on the mode selected, sometimes to B2. Reading register B either reads B1 or B2 depending on the mode selected. In the DIS mode, MDASMBR can be accessed to prepare a value for a subsequent mode selection. In this mode, register B1 is accessed in order to prepare a value for the OPWM mode. Unused register B2 is hidden and cannot be read, but is written with the same value when register B1 is written. In the IPWM mode, MDASMBR contains the captured value corresponding to the leading edge of the measured pulse. In this mode, register B2 is accessed; buffer register B1 is hidden and is not readable. In the IPM and IC modes, MDASMBR contains the captured value corresponding to the previously dedicated edge (rising or falling edge). In this mode, register B2 is accessed; buffer register B1 is hidden and is not readable. In the OCB and OCAB modes, MDASMBR is loaded with the value corresponding to the trailing edge of the pulse to be generated. Writing to MDASMBR in the OCB and OCAB modes also enables the corresponding channel B comparator until the next successful comparison. In this mode, register B2 is accessed; buffer register B1 is hidden and is not readable. In the OPWM mode, MDASMBR is loaded with the value corresponding to the trailing edge of the PWM pulse to be generated. In this mode, register B1 is accessed; buffer register B2 is hidden and cannot be accessed. NOTE In IC, IPM, or IPWM mode, when a read to register A or B occurs at the same time as a counter bus capture into that register and the counter bus is changing value, then the counter bus capture to that register is delayed.

17.12.19 MDASMSCRD — MDASM Status/Control Register (Duplicated)

The MDASMSCRD and the MDASMSCR are the same registers accessed at two different addresses.

Reading or writing to one of these two addresses has exactly the same effect.

WARNING

The user should not write directly to the address of the MDASMSCRD. This register's address may be reserved for future use and should not be accessed by the software to ensure future software compatibility.

The duplication of the SCR register allows coherent 32-bit accesses when using an RCPU.

17.12.20 MDASMSCR — MDASM Status/Control Register

The status and control register gathers a read only bit reflecting the status of the MDASM pin as well as read/write bits related to its control and configuration.

The pin input status bit reflects the status of the corresponding pin when in input mode. When in output mode, the PIN bit only reflects the status of the output flip-flop .

MDASMSCR — MDASM Status/Control Register

0x30 605E
0x30 6066
0x30 606E
0x30 6076
0x30 607E
0x30 60DE
0x30 60E6
0x30 60EE
0x30 60F6
0x30 60FE

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PIN	WOR	FREN	RESERV	EDPOL	FORCA	FORCB	RESERVED		BSL1	BSL0	RESERV	MOD3	MOD2	MOD1	MOD0
SRESET:															
—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-29 MDASMSCR Bit Descriptions

Bit(s)	Name	Description
0	PIN	
1	WOR	Wired-OR bit — In the DIS, IPWM, IPM and IC modes, the WOR bit is not used; reading this bit returns the value that was previously written. In the OCB, OCAB and OPWM modes, the WOR bit selects whether the output buffer is configured for open-drain or totem pole operation. 1 = Output buffer is open-drain. 0 = Output buffer is totem pole. The WOR bit is cleared by reset.
2	FREN	Freeze enable bit — This active high read/write control bit enables the MDASM to recognize the MIOB freeze signal. 1 = The MDASM is frozen if the MIOB freeze line is active. 0 = The MDASM is not frozen even if the MIOB freeze line is active. The FREN is cleared by reset.
3	—	Reserved
4	EDPOL	Polarity bit — In the DIS mode, this bit is not used; reading it returns the last value written. In the IPWM mode, this bit is used to select the capture edge sensitivity of channels A and B. 1 = Channel A captures on a falling edge. Channel B captures on a rising edge. 0 = Channel A captures on a rising edge. Channel B captures on a falling edge. In the IPM and IC modes, the EDPOL bit is used to select the input capture edge sensitivity of channel A. 1 = Channel A captures on a falling edge. 0 = Channel A captures on a rising edge. In the OCB, OCAB and OPWM modes, the EDPOL bit is used to select the voltage level on the output pin. 1 = The complement of the output flip-flop logic level appears on the output pin: a match on channel A resets the output pin; a match on channel B sets the output pin. 0 = The output flip-flop logic level appears on the output pin: a match on channel A sets the output pin, a match on channel B resets the output pin. The EDPOL bit is cleared by reset.
5	FORCA	Force A bit — In the OCB, OCAB and OPWM modes, the FORCA bit allows the software to force the output flip-flop to behave as if a successful comparison had occurred on channel A (except that the FLAG line is not activated). Writing a one to FORCA sets the output flip-flop; writing a zero to it has no effect. In the DIS, IPWM, IPM and IC modes, the FORCA bit is not used and writing to it has no effect. FORCA is cleared by reset and is always read as zero. Writing a one to both FORCA and FORCB simultaneously resets the output flip-flop.
6	FORCB	Force B bit — In the OCB, OCAB and OPWM modes, the FORCB bit allows the software to force the output flip-flop to behave as if a successful comparison had occurred on channel B (except that the FLAG line is not activated). Writing a one to FORCB resets the output flip-flop; writing a zero to it has no effect. In the DIS, IPWM, IPM and IC modes, the FORCB bit is not used and writing to it has no effect. FORCB is cleared by reset and is always read as zero. Writing a one to both FORCA and FORCB simultaneously resets the output flip-flop.
7:8	—	Reserved
9:10	BSL1 — BSL0	Bus select bits — These bits are used to select which of the four 16-bit counter buses is used by the MDASM. **NOTE:** Unconnected counter buses inputs are grounded.

Table 17-29 MDASMSCR Bit Descriptions (Continued)

Bit(s)	Name	Description
11	—	Reserved
12:15	MOD3 — MOD0	Mode select bits — The four mode select bits select the mode of operation of the MDASM. To avoid spurious interrupts, it is recommended that MDASM interrupts are disabled before changing the operating mode. The mode select bits are cleared by reset. **NOTE:** The reserved modes should not be set; if these modes are set, the MDASM behavior is undefined.

17.13 Pulse Width Modulation Submodule (MPWMSM)

In this section the values taken by the bits in the registers are given according to the following rule:

- 0 -> reset (negated))
- 1 -> set (asserted)
- u -> undefined
- - -> unaffected

17.13.1 MPWMSM Overview Description

The MIOS pulse width modulation submodule (MPWMSM) is a function included in the MIOS library. It allows pulse width modulated signals to be generated over a wide range of frequencies, independently of other MIOS output signals and with no software intervention. The output pulse width can vary from 0% to 100%. The minimum pulse width is twice the minimum MIOS CLOCK period (i.e., the minimum pulse width is 50 ns when f_{SYS} is 40 MHz). The MWPMSM can run in a double-buffered mode, to avoid spurious update.

The following sections describe the MPWMSM in detail. A block diagram of the MPWMSM is shown in **Figure 17-20**.

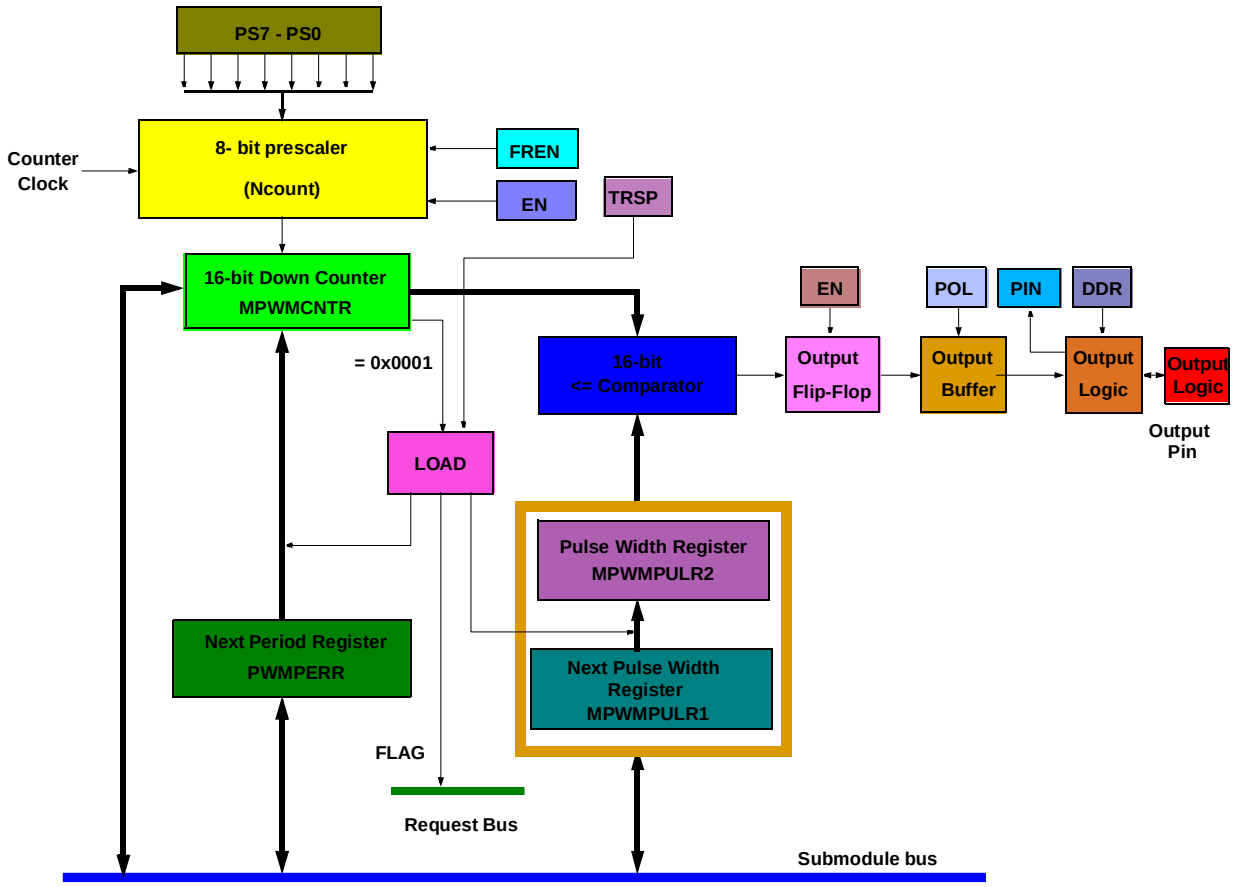


Figure 17-20 MPWMSM Block Diagram

17.13.2 MPWMSM Terminology

Bits of resolution — The MPWMSM contains a 16-bit modulus down-counter that counts from the desired loaded value to 0x0001. The term “bits of resolution” is used in this document to indicate the size of the equivalent free running binary counter. To cover the worst case, the number of bits is rounded to the lower number. For example, if the counter is preset with a value between 128 and 255, it is said to have seven bits of resolution. If it is preset with a value between 256 and 511, it is said to have eight bits of resolution, and so on.

Resolution — The term “resolution” is used in this document to define the minimum MPWMSM output increment in time units.

17.13.2.1 MPWMSM Features

— Output pulse width modulated (PWM) signal generation with no software intervention
— Built-in 8-bit programmable prescaler clocked by the MCPSM
— PWM period and pulse width values provided by software:

- Double-buffered for glitch-free period and pulse width changes
- Minimum output period/pulse-width increment: 50 ns (assuming f_{SYS} = 40 MHz)
- Maximum 50% duty-cycle output frequency: 10 MHz (assuming f_{SYS} = 40 MHz)
- Up to 16 bits of resolution for the output pulse width
- Wide range of periods
  - 16 bits of resolution: period range from 3.27 ms (with 50-ns steps) to 6.71 s (with 102.4 µs steps)
  - Eight bits of resolution: period range from 12.8 µs (with 50-ns steps) to 26.2 ms (with 102.4-µs steps)
- Wide range of frequencies
  - Maximum output frequency at f_{SYS} = 40 MHz with 16 bits of resolution and divide-by-2 prescaler selection: 305 Hz (3.27 ms.)
  - Minimum output frequency at f_{SYS} = 40 MHz with 16 bits of resolution and divide-by-4096 prescaler selection: 0.15 Hz (6. 7s.)
  - Maximum output frequency at f_{SYS} = 40 MHz with 8 bits of resolution and divide-by-2 prescaler selection: 78125 Hz (12.8 µs.)
  - Minimum output frequency at f_{SYS} = 40 MHz with 8 bits of resolution and divide-by-4096 prescaler selection: 38.15 Hz (26. 2ms.)
- Programmable duty cycle from 0% to 100%
- Possible interrupt generation at start of every period
- Software selectable output pulse polarity
- Software readable output pin status
- Possible use of pin as I/O port when PWM function is not needed

17.13.3 MPWMSM Description

The purpose of the MPWMSM is to create a variable pulse width output signal at a wide range of frequencies, independently of other MIOS output signals. The MPWMSM includes its own counter, and thus does not use the MIOS counter bus set. However the MPWMSM uses the prescaled clock bus that originates in the MIOS counter prescaler submodule (MCPSM) (See **17.13.3 MPWMSM Description**). The MPWMSM pulse width can vary from 0.0 percent to 100.0 percent, with up to 16 bits of resolution. The finest output resolution is the MIOS CLOCK period multiplied by two (for a MIOS CLOCK with f_{SYS} = 40 MHz, the finest output pulse width resolution is 50 ns). With the full 16 bits of resolution and the MCPSM set to divide by two, the period of the output signal can range from 3.276 ms to 6.7 1s (assuming f_{SYS} = 40 MHz).

By reducing the amount of bits of resolution, the output signal period can be reduced. For example, the period can be as fast as 204.8 µs (4882 Hz) with 12 bits of resolution, as fast as 12.8 µs (78.125 KHz) with eight bits of resolution, and as fast as 3.2 µs (312.5 KHz) with six bits of resolution (still assuming a f_{SYS} = 40 MHz and the MCPSM set to divide by two).

The MPWMSM is composed of:

- An output flip-flop with output buffer and polarity control
- An input/output pin with data direction control
- An 8-bit prescaler and clock selection logic
- A 16-bit down-counter (MPWMCNTR)
- A register to hold the next period values (MPWMPERR)
- Two registers to hold the current and next pulse width values (MPWMPULR)
- A less-than or equal comparator
- A status and control register (MPWMSCR)

17.13.3.1 Clock Selection

The MPWMSM contains an 8-bit prescaler clocked by the output signal from the MIOS counter prescaler submodule ($f_{SYS}/2$ to $f_{SYS}/16$). The MPWMSM clock selector allows the choice, by software, of one of 256 divide ratios which give to the MPWMSM a large choice of frequencies available for the down-counter. The MPWMSM down-counter is thus capable of counting with a clock frequency ranging from $f_{SYS}/2$ to $f_{SYS}/4096$.

Switching the MPWMSM from disable to enable will reload the value of CP7-CP0 into the 8-bit prescaler counter.

17.13.3.2 Counter

A 16-bit down-counter in the MPWMSM provides the time reference for the output signal. The counter is software writable. When writing to the counter (i.e., at the MPWMCNTR address), it also writes to the MPWMPERR register. When in transparent mode (TRSP = 1), writing to the MPWMPERR will also write to the counter. The down-counter is readable at anytime. The value loaded in the down-counter corresponds to the period of the output signal.

When the MPWMSM is enabled, the counter begins counting. As long as it is enabled, the counter counts down freely. The counter counts at the rate established by the prescaler. When the count down reaches 0x0001, the load operation is executed and the value in the MPWMPERR register is loaded in the MPWMCNTR register, (i.e., the counter). Then the counter restarts to count down from that value.

17.13.3.3 Period Register

The period section is composed of a 16-bit data register (MPWMPERR). The software establishes the period of the output signal in register MPWMPERR.

When the MPWMSM is running in transparent mode, the period value in register MPWMPERR is immediately transferred to the counter on a write to the MPWMPERR.

When the MPWMSM is running in double-buffered mode, the period value in register MPWMPERR can be changed at any time without affecting the current period of the

output signal. The new value MPWMPERR will be transferred to the counter only when the counter reaches the value of 0x0001 and generates a load signal.

Period values of 0x0000, 0x0001 and 0x0002 are MPWMSM special cases:

- The value 0x0000 in the period register, causes the counter to act like a free running counter. This condition creates a period of 65536 PWM clock periods.
- The value 0x0001 in the period register will always cause a period match to occur and the counter will never decrement below 0x0001. This condition is defined as a period of “1” PWM clock count. The output flip-flop is always set unless the value in the MPWMPULR = 0x0000, when the output flip-flop is always reset. Refer to **17.13.3.5 0% and 100% Duty Cycles** for details about 0% and 100% duty cycles.
- Writing value 0x0002 in the period register causes a period match to occur every two clock periods. The counter decrements from 0x0002 to 0x0001, and then it is initialized back to 0x0002. This condition is defined as a period of “2” clock count. Note that the value 0x0002 loaded in the period register and a value of 0x0001 in the pulse width register is the condition to obtain the maximum possible output frequency for a given clock period.

The relationship between the output frequency obtained (F_{PWMO}) and the MIOS CLOCK frequency (f_{SYS}), the MCPSM clock divide ratio (N_{MCPSM}), the counter divide ratio (N_{MPWMSM}) and the value loaded in the counter ($V_{COUNTER}$) is given by the following equation:

$$F_{PWMO} = \frac{F_{SYS}}{N_{MCPSM} \bullet N_{MPWMSM} \bullet V_{COUNTER}}$$

17.13.3.4 Pulse Width Registers

The pulse width section is composed of two 16-bit data registers (MPWMPULR1 and MPWMPULR2). Only register MPWMPULR1 is accessible by software. The software establishes the pulse width of the MPWMSM output signal in register MPWMPULR1. Register MPWMPULR2 is used as a double buffer of register MPWMPULR1.

When the MPWMSM is running in transparent mode, the pulse width value in register MPWMPULR1 is immediately transferred in the register MPWMPULR2 so that the new value takes effect immediately.

NOTE

When the MPWMSM is in disable mode, writing to MPWMPULR1 will write automatically to MPWMPULR2.

When the MPWMSM is not running in double-buffered mode, the pulse width value in register MPWMPULR1 can be changed at any time without affecting the current pulse width of the output signal. The new value MPWMPULR1 will be transferred to MPWMPULR2 only when the down-counter reaches the value of 0x0001.

When the counter first reaches the value in register MPWMPULR2, the output flip-flop is set. The output is reset when the counter reaches 0x0001. The pulse width match starts the width of the output signal, it does not affect the counter. Register MPWMPULR1 is software readable and writable at any time. The MPWMSM does not modify the content of register MPWMPULR1.

The PWM output pulse width can be as wide as one period minus one MPWMSM clock count: (i.e., MPWMPULR2 = MPWMPERR — [one MPWMSM clock count]). At the other end of the pulse width range, register MPWMPULR2 can contain 0x0001 to create a pulse width of one PWM clock count.

EXAMPLE

With 0x00FF in the counter and 0x0002 in MPWMPULR2, the period is 255 PWM clock count and the pulse width is two PWM clock counts.

For a given system clock frequency, with a given counter divide ratio and clock selection divide ratio, the output pulse width is given by the following equation:

$$Pulse\_Width = \frac{N_{MCPSM} \bullet N_{MPWMSM} \bullet V_{MPWMB2}}{F_{SYS}}$$

where V_{MPWMB2} is the value in the register B2

In such conditions, the minimum output pulse width that can be obtained is given by:

$$Minimum\_Pulse\_Width = \frac{N_{MCPSM} \bullet N_{MPWMSM}}{F_{SYS}}$$

and the maximum pulse width by:

$$Maximum\_Pulse\_Width = \frac{N_{MCPSM} \bullet N_{MPWMSM} \bullet (2^{Bit\_of\_Resolution} - 1)}{F_{SYS}}$$

17.13.3.5 0% and 100% Duty Cycles

The 0% and 100% duty cycles are special cases to give flexibility to the software to create a full range of outputs. The “always set” and “always clear” conditions of the output flip-flop are established by the value in register MPWMPULR2. These boundary conditions are generated by software, just like another pulse. When the PWM output is being used to generate an analog level, the 0% and 100% represent the full scale values.

The 0% output is created with a 0x0000 in register MPWMPULR2, which prevents the output flip-flop from ever being set.

The 100% output is created when the content of register MPWMPULR2 is equal to or greater than the content of register MPWMPERR. Thus, the width register match

occurs on counter reload. The state sequencer provides the timing to ensure that the first appearance of a 100% value in register MPWMPULR2 causes a glitchless always-set condition of the output flip-flop when TRSP = ‘0’.

NOTE 1

Even if the output is forced to 100%, the 16-bit up counter continues its counting and that output changes to or from the 100% value are done synchronously to the selected period.

NOTE 2

When a PWM output period is selected to be 65536 PWM clocks by loading 0x0000 in the period register, it is not possible to have an 100% duty cycle output signal. In this case, the maximum duty cycle available is of 65535/65536.

17.13.3.6 Tables

Table 17-30 and **Table 17-31** summarize the frequency and minimum pulse width values that can be obtained respectively with divide-by-1 and divide-by-256 MPWMSM clock prescaler options, while using a MIOS CLOCK frequency of 40 MHz, and for each MCPSM clock divide ratios.

Table 17-30 PWM Pulse/Frequency Ranges (in Hz) Using /1 Option (40 MHz)

Minimum Pulse Width	Bits of Resolution															
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
50 ns/2	305	610	1220	2441	4882	9765	19.5K	39 K	78 K	156 K	312 K	625 K	1250 K	2500 K	5000 K	10000 K
75 ns/3	203	407	814	1628	3255	6510	13K	26 K	52 K	104 K	208 K	416 K	833 K	1666 K	3333 K	6666 K
100 ns/4	152	305	610	1220	2441	4882	9765	19.5 K	39 K	78 K	156 K	312 K	625 K	1250 K	2500 K	5000K
125 ns/5	122	244	488	976	1953	3906	7812	15.6 K	31.3 K	62.5 K	125 K	250 K	500 K	1000 K	2000 K	4000K
150 ns/6	101	203	407	814	1628	3255	6510	13 K	26 K	52 K	104 K	208 K	416 K	833 K	1666 K	3333K
175 ns/7	87.2	174	348	697	1395	2790	5580	11.1 K	22.3 K	44.6 K	89.3 K	178 K	357 K	714 K	1428 K	2857K
200 ns/8	76.3	152	305	610	1220	2441	4882	9765	19.5 K	39 K	78 K	156 K	312 K	625 K	1250 K	2500K
225 ns/9	67.8	135	271	542	1085	2170	4340	8680	17.3 K	34.7 K	69.4 K	138 K	277 K	555 K	1111 K	2222K
250 ns/10	61	122	244	488	976	1953	3906	7812	15.6 K	31.3 K	62.5 K	125 K	250 K	500 K	1000 K	2000K
275 ns/11	55.5	111	222	443	887	1775	3551	7102	14.2 K	28.4 K	56.8 K	113 K	227 K	454 K	909 K	1818 K
300 ns/12	50.8	101	203	407	814	1628	3255	6510	13 K	26 K	52 K	104 K	208 K	416 K	833 K	1666 K
325 ns/13	46.9	93.9	187	375	751	1502	3004	6009	12 K	24 K	48 K	96.1 K	192 K	384 K	769 K	1538 K
350 ns/14	43.6	87.2	174	348	697	1395	2790	5580	11.1 K	22.3 K	44.6 K	89.3 K	178 K	357 K	714 K	1428K
375 ns/15	40.7	81.4	162	325	651	1302	2604	5208	10.4 K	20.8 K	41.6 K	83.3 K	166 K	333 K	666 K	1333 K
400 ns/16	38.1	76.3	152	305	610	1220	2441	4882	9765	19.5 K	39 K	78 K	156 K	312 K	625 K	1250 K

17.13.3.7 MPWMSM Status and Control Register (SCR)

One register is used to initialize the MPWMSM and monitor its operation. Control bits are included to allow the software to enable the PWM generator, establish the output signal polarity, select the counter clock rate and set the glitch-free mode. A status bit is included to allow the software to read the state of the output pin.

Table 17-31 PWM Pulse/frequency Ranges (in Hz) Using /256 Option (40 MHz)

Minimum Pulse Width	Bits of Resolution															
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
12.8 µs/512	1.192	2.384	4.768	9.536	19.07	38.14	76.29	152.5	305.1	610.3	1220	2441	4882	9765	19.5 K	39 K
19.2 µs/768	0.794	1.589	3.178	6.357	12.71	25.43	50.86	101.7	203.4	406.9	813.8	1627	3255	6510	13 K	26 K
25.6 µs/1024	0.596	1.192	2.384	4.768	9.536	19.07	38.14	76.29	152.5	305.1	610.3	1220	2441	4882	9765	19.5 K
32 µs/1280	0.476	0.953	1.907	3.814	7.629	15.24	30.51	61.03	122	244.1	488.2	976.5	1953	3906	7812	15.6 K
38.4 µs/1536	0.397	0.795	1.589	3.179	6.358	12.71	25.43	50.86	101.7	203.5	406.9	813.8	1627	3255	6510	13 K
44.8 µs/1792	0.34	0.681	1.362	2.724	5.449	10.89	21.80	43.59	87.19	174.4	348.8	697.5	1395	2790	5580	11.1 K
51.2 µs/2048	0.298	0.596	1.192	2.384	4.768	9.536	19.07	38.14	76.29	152.5	305.1	610.3	1220	2441	4882	9765
57.6 µs/2304	0.264	0.529	1.059	2.119	4.238	8.477	16.95	33.90	67.81	135.6	271.2	542.5	1085	2170	4340	8680
64 µs/2560	0.238	0.476	0.953	1.907	3.814	7.629	15.24	30.51	61.03	122	244.1	488.2	976.5	1953	3906	7812
70.4 µs/2816	0.216	0.433	0.867	1.734	3.468	6.936	13.87	27.74	55.48	110.9	221.9	443.9	887.8	1775	3551	7102
76.8 µs/3072	0.198	0.397	0.795	1.589	3.179	6.358	12.71	25.43	50.86	101.7	203.5	406.9	813.8	1627	3255	6510
83.2 µs/3328	0.183	0.366	0.733	1.467	2.934	5.869	11.74	23.47	46.95	93.9	187.8	375.6	751.2	1502	3004	6009
89.6 µs/3584	0.170	0.340	0.681	1.362	2.724	5.449	10.89	21.80	43.59	87.19	174.4	348.8	697.5	1395	2790	5580
96 µs/3840	0.159	0.318	0.636	1.271	2.543	5.086	10.17	20.34	40.69	81.38	162.8	325.5	651	1302	2604	5208

17.13.3.8 MPWMSM Interrupt

A valid MPWMSM interrupt is recognized when a pulse occurs on the flag line to set the flag bit and the interrupt enable bit is set for the corresponding level in the request submodule (Refer to **17.9.1 Interrupts** for details about interrupts). A set flag pulse is generated at the start of every period.

The flag bit is a status bit which indicates, when set, that the output period has started and that registers MPWMPERR and MPWMPULR1 are available for updates when in double-buffered mode. The level of the resulting interrupt is determined in the request submodule.

17.13.3.9 MPWMSM Port Functions

The MPWMSM has one dedicated I/O external pin.

The output flip-flop is the basic output of the MPWMSM. Except when the pulse width is at 100% or 0%, the output flip-flop is reset at the beginning of each period and is set at the beginning of the designated pulse width until the end of the period. As a software option, the polarity of the signal presented to the output pin may be the state of the output flip-flop or the inverse of the output flip-flop.

The MPWMSM is connected to an external, input/output pin. When in the disabled mode, the POL bit (polarity) and the DDR bit (data direction) in the SCR register allow the MPWMSM to be used as an I/O port.

17.13.3.10 MPWMSM Data Coherency

Byte accesses to MPWMPULR and MPWMPERR are supported, but are not recommended as the transfer from the primary registers to the secondary registers are done as a 16-bit word transfer.

For most MPWMSM operations, 16-bit accesses are sufficient and long word accesses (32-bit) are treated as two 16-bit accesses, with one exception — a long word write to the period/pulse width registers. In this case, if the long word write takes place within the PWM period, there is no visible effect on the output signal and the new values stored in MPWMPERR and MPWMPULR are ready to be loaded into the buffer registers at the start of the next period. If, however, the long word write coincides with the end of the period, then the transfer of values from the primary to the secondary registers is delayed until the end of the next period; during this period the previous values are used for the period and width This feature enables updates of the period and pulse-width values without getting erroneous pulses.

17.13.4 MIO Bus (MIOB) Interface

- The MPWMSM is connected to all the signals in the read/write and control bus, to allow data transfer from and to the MPWMSM registers, and to control the MPWMSM in the different possible situations.
- The MPWMSM is not using any of the 16-bit counter buses
- The MPWMSM uses the request bus to transmit to the request submodule

17.13.5 Effect of RESET on MPWMSM

The MPWMSM is affected by reset according to what is described in the section related to register description.

The MPWMPERR, MPWMPULR, and MPWMCNTR registers, together with the clock prescaler register bits, must be initialized by software, since they are undefined after hardware reset.

A value must be written to the MPWMCNTR (which writes the same value into the MPWMPERR) and a pulse width value written to MPWMPULR, before the MPWMSCR is written to. The latter access initializes the clock prescaler.

17.13.6 MPWMSM Registers

The privilege level to access to the MPWMSM registers depends on the MIOS14MCR SUPV bit. The privilege level is unrestricted after reset and can be change to supervisor by software.

17.13.6.1 MPWMSM Registers Organization

The MPWMSM register map comprises four 16-bit register locations, as shown below. All unused bits return zero when read by the software. All register addresses in this section are specified as offsets from the base address of the MPWMSM.

Table 17-32 MPWMSM Address Map

Address	Register
MPWMSM0	
0x30 6000	MPWMSM0 Period Register (MPWMSMPERR) See **Table 17-33** for bit descriptions.
0x30 6002	MPWMSM0 Pulse Register (MPWMSMPULR) See **Table 17-34** for bit descriptions.
0x30 6004	MPWMSM0 Count Register (MPWMSMCNTR) See **Table 17-35** for bit descriptions.
0x30 6006	MPWMSM0 Status/Control Register (MPWMSMSCR) See **Table 17-36** for bit descriptions.
MPWMSM1	
0x30 6008	MPWMSM1 Period Register (MPWMSMPERR)
0x30 600A	MPWMSM1 Pulse Register (MPWMSMPULR)
0x30 600C	MPWMSM1 Count Register (MPWMSMCNTR)
0x30 600E	MPWMSM1 Status/Control Register (MPWMSMSCR)
MPWMSM2	
0x30 6010	MPWMSM2 Period Register (MPWMSMPERR)
0x30 6012	MPWMSM2 Pulse Register (MPWMSMPULR)
0x30 6014	MPWMSM2 Count Register (MPWMSMCNTR)
0x30 6016	MPWMSM2 Status/Control Register (MPWMSMSCR)
MPWMSM3	
0x30 6018	MPWMSM3 Period Register (MPWMSMPERR)
0x30 601A	MPWMSM3 Pulse Register (MPWMSMPULR)
0x30 601C	MPWMSM3 Count Register (MPWMSMCNTR)
0x30 601E	MPWMSM3 Status/Control Register (MPWMSMSCR)
MPWMSM4	
0x30 6020	MPWMSM4 Period Register (MPWMSMPERR)
0x30 6022	MPWMSM4 Pulse Register (MPWMSMPULR)
0x30 6024	MPWMSM4 Count Register (MPWMSMCNTR)
0x30 6026	MPWMSM4 Status/Control Register (MPWMSMSCR)
MPWMSM5	
0x30 6028	MPWMSM5 Period Register (MPWMSMPERR)
0x30 602A	MPWMSM5 Pulse Register (MPWMSMPULR)
0x30 602C	MPWMSM5 Count Register (MPWMSMCNTR)
0x30 602E	MPWMSM5 Status/Control Register (MPWMSMSCR)
MPWMSM16	
0x30 6080	MPWMSM16 Period Register (MPWMSMPERR)
0x30 6082	MPWMSM16 Pulse Register (MPWMSMPULR)
0x30 6084	MPWMSM16 Count Register (MPWMSMCNTR)
0x30 6086	MPWMSM16 Status/Control Register (MPWMSMSCR)

Table 17-32 MPWMSM Address Map (Continued)

Address	Register
MPWMSM17	
0x30 6088	MPWMSM17 Period Register (MPWMSMPERR)
0x30 608A	MPWMSM17 Pulse Register (MPWMSMPULR)
0x30 608C	MPWMSM17 Count Register (MPWMSMCNTR)
0x30 608E	MPWMSM17 Status/Control Register (MPWMSMSCR)
MPWMSM18	
0x30 6090	MPWMSM18 Period Register (MPWMSMPERR)
0x30 6092	MPWMSM18 Pulse Register (MPWMSMPULR)
0x30 6094	MPWMSM18 Count Register (MPWMSMCNTR)
0x30 6096	MPWMSM18 Status/Control Register (MPWMSMSCR)
MPWMSM19	
0x30 6098	MPWMSM19 Period Register (MPWMSMPERR)
0x30 609A	MPWMSM19 Pulse Register (MPWMSMPULR)
0x30 609C	MPWMSM19 Count Register (MPWMSMCNTR)
0x30 609E	MPWMSM19 Status/Control Register (MPWMSMSCR)
MPWMSM20	
0x30 60A0	MPWMSM20 Period Register (MPWMSMPERR)
0x30 60A2	MPWMSM20 Pulse Register (MPWMSMPULR)
0x30 60A4	MPWMSM20 Count Register (MPWMSMCNTR)
0x30 60A6	MPWMSM20 Status/Control Register (MPWMSMSCR)
MPWMSM21	
0x30 60A8	MPWMSM21 Period Register (MPWMSMPERR)
0x30 60AA	MPWMSM21 Pulse Register (MPWMSMPULR)
0x30 60AC	MPWMSM21 Count Register (MPWMSMCNTR)
0x30 60AE	MPWMSM21 Status/Control Register (MPWMSMSCR)

17.13.6.2 MPWMPERR — MPWMSM Period Register

MPWMPERR address: MPWMSM base address

The period register contains the binary value corresponding to the period to be generated.

MPWMPERR — MPWMSM Period Register

0x30 6000
0x30 6008
0x30 6010
0x30 6018
0x30 6020
0x30 6028
0x30 6080
0x30 6088
0x30 6090
0x30 6098
0x30 60A0
0x30 60A8

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PER[15:0]															
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-33 MPWMPERR Bit Descriptions

Bit(s)	Name	Description
0:15	PER15 — PER0	Period. These bits contain the binary value corresponding to the period to be generated.

17.13.6.3 MPWMPULR — MPWMSM Pulse Width Register

The pulse width register contains the binary value of the pulse width to be generated.

MPWMPULR — MPWMSM Pulse Width Register

0x30 6002
0x30 600A
0x30 6012
0x30 601A
0x30 6022
0x30 602A
0x30 6082
0x30 608A
0x30 6092
0x30 609A
0x30 60A2
0x30 60AA

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PUL15	PUL14	PUL13	PUL12	PUL11	PUL10	PUL9	PUL8	PUL7	PUL6	PUL5	PUL4	PUL3	PUL2	PUL1	PUL0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-34 MPWMPULR Bit Descriptions

Bit(s)	Name	Description
0:15	PUL15 — PUL0	Pulse width. These bits contain the binary value of the pulse width to be generated.

17.13.6.4 MPWMCNTR — MPWMSM Counter Register

The counter register reflects the actual value of the MPWMSM counter.

This register is writable only through the period register (PWMPERR). Writes to the counter register will write the same value to the period register.

MPWMCNTR — MPWMSM Counter Register

0x30 6004
0x30 600C
0x30 6014
0x30 601C
0x30 6024
0x30 602C
0x30 6084
0x30 608C
0x30 6094
0x30 609C
0x30 60A4
0x30 60AC

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
CNT[15:0]															
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-35 MPWMCNTR Bit Descriptions

Bit(s)	Name	Description
0:15	CNT[15:0]	Counter. These bits reflect the actual value of the MPWMSM counter.

17.13.6.5 MPWMSCR — MPWMSM Status/Control Register

The status and control register gathers read only bits reflecting the status of the MPWMSM pin as well as read/write bits related to its control and configuration.

MPWMSCR — MPWMSM Status/Control Register

0x30 6006
0x30 600E
0x30 6016
0x30 601E
0x30 6026
0x30 602E
0x30 6086
0x30 608E
0x30 6096
0x30 609E
0x30 60A6
0x30 60AE

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PIN	DDR	FREN	TRSP	POL	EN	RESERVED		CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-36 MPWMSCR Bit Descriptions

Bit(s)	Name	Description
0	PIN	Pin input status bit — The PIN bit reflects the state present on the MPWMSM pin. The software can thus monitor the signal on the pin. The PIN bit is a read-only bit. Writing to the PIN bit has no effect.
1	DDR	Data direction register — The DDR bit indicates the direction for the pin when the PWM function is not used (disable mode). 0 = pin is in input. 1 = pin is in output. The DDR bit is cleared by reset. **Table 17-37** lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit.
2	FREN	Freeze enable bit — This active high read/write control bit enables the MPWMSM to recognize the freeze signal on the MIOB. 0 = MPWMSM not frozen even if the MIOB freeze line is active. 1 = MPWMSM frozen if the MIOB freeze line is active. The FREN is cleared by reset.
3	TRSP	Transparent mode — The TRSP bit indicates that the MPWMSM is in transparent mode. In transparent mode, when the software writes to either the MPWMPERR or MPWMPULR1 register the value written is immediately transferred to the counter or register MPWMPULR2 respectively. 0 = Double-buffered mode. 1 = Transparent mode. The TRSP bit is cleared by reset.
4	POL	Output polarity control bit — The POL bit works in conjunction with the EN bit and controls whether the MPWMSM drives the pin with the direct or the inverted value of the output flip-flop. **Table 17-37** lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit.

Table 17-36 MPWMSCR Bit Descriptions (Continued)

Bit(s)	Name	Description
5	EN	Enable PWM signal generation — The EN bit defines whether the MPWMSM generates a PWM signal or is used as an I/O channel: 0 = PWM generation disabled (pin can be used as I/O). 1 = PWM generation enabled (the pin is in output mode). Each time the submodule is enabled, the value of CP7-CP0 is loaded into the prescaler. The EN bit is cleared by reset.
6:7	—	Reserved
8:15	CP7 — CP0	Clock prescaler — This 8-bit read/write data register stores the modulus value for loading into the built-in 8-bit clock prescaler. The value loaded defines the divide ratio for the signal that clocks the MPWMSM. The new value is loaded into the prescaler counter on the prescaler counter overflow, or upon the EN bit of the MPWMSCR being set. **Table 17-38** gives the clock divide ratio according to the CP7..CP0 values:

Table 17-37 PWMSM Output Pin Polarity Selection

Control Bits			Pin Direction	Pin State	Periodic Edge	Variable Edge	Optional Interrupt On
POL	EN	DDR					
0	0	0	Input	INPUT	—	—	—
0	0	1	Output	Always Low	—	—	—
0	1	—	Output	High Pulse	Falling Edge	Rising Edge	Falling Edge
1	0	0	Input	INPUT	—	—	—
1	0	1	Output	Always High	—	—	—
1	1	—	Output	Low Pulse	Rising Edge	Falling Edge	Rising Edge

Table 17-38 Prescaler Values

Prescaler Value (CP7..CP0 in Hex)	MCPSM Divide Ratio:
FF	1
FE	2
FD	3
FC	4
FB	5
FA	6
F9	7
F8	8
.....	.....
02	254 (2^8 -2)
01	255 (2^8 -1)
00	256 (2^8)

17.14 Parallel Port I/O Submodule (MPIOSM)

In this section the values taken by the bits in the registers are given according to the following rule:

- 0 -> reset (negated))
- 1 -> set (asserted)
- u -> undefined
- - -> unaffected

17.14.1 MPIOSM Overview Description

The MIOS parallel port I/O submodule (MPIOSM) is a function included in the MIOS library in order to provide the required port I/O capability. The MPIOSM can operate without the involvement of other MIOS submodules.

Each implemented MPIOSM provides I/O capability for up to 16 pins. Any number of required MPIOSM could be implemented as long as the total number of submodules do not exceed the limit described in **17.1.4 MIOS14 Module/Submodule Addressing**.

The following sections describe the MPIOSM in detail. A block diagram of one bit of the MPIOSM is shown in **Figure 17-21**. The MPIOSM contains 16 such blocks.

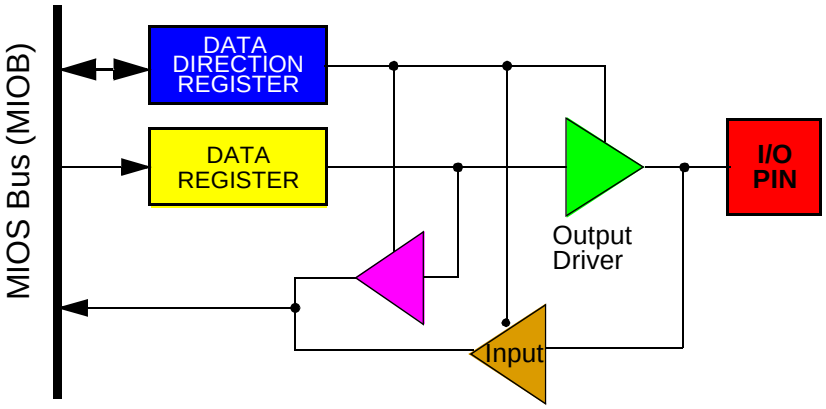


Figure 17-21 MPIOSM 1-Bit Block Diagram

17.14.2 MPIOSM features

- A submodule of the MIOS library
- Uses two 16-bit registers in the address space
- Up to 16 bidirectional parallel input/output pins
- Simple DDR (data direction register) concept for pin direction selection

17.14.3 MPIOSM Pin Functions

Table 17-39 shows the MPIOSM I/O pin functions according to the setting of the DDR when writing to or reading from the DR.

Table 17-39 MPIOSM I/O Pin Function

Operation Performed	DDR	I/O Pin Function
Write	0	The I/O pin is in input mode. Data is written into the DR.
Write	1	Data is written into the DR and output to the I/O pin.
Read	0	The I/O pin is in input mode. The state of the I/O pin is read.
Read	1	The I/O pin is in an output mode. The DR is read.

17.14.4 MPIOSM Description

17.14.4.1 MPIOSM Port function

A MIOS parallel port I/O submodule can handle up to 16 input/output pins. The number of I/O pins is determined at the time of silicon implementation.

The MPIOSM has two 16-bit registers: the data register (DR) and the data direction register (DDR). Each pin of the MPIOSM may be programmed as an input or an output, determined by the state of the corresponding bit in the DDR.

The data direction register can be written to or read by the processor. During the programmed output state, a read of the data register reads the value of the output data latch and not the I/O pin. See **Figure 17-21** and **Table 17-39**.

During reset, all MPIOSM pins are configured as inputs. The contents of the data register are undefined after reset.

As a general practice, it is recommended to write a value in the data register before configuring its corresponding I/O pin as an output.

17.14.4.2 Non-Bonded MPIOSM Pads

A non-bonded MPIOSM pad reads ‘0’ when it is configured as an input. When configured as an output, it indicates the current state of the output data latch.

17.14.5 Modular I/O Bus (MIOB) Interface

- The MPIOSM is connected to all the signals in the read/write and control bus, to allow data transfer from and to the MPIOSM registers, and to control the MPIOSM in the different possible situations.
- The MPIOSM does not use the counter bus set and is therefore not connected to it.
- The MPIOSM does not generate any interrupts and is therefore not connected to this bus.

17.14.6 Effect of RESET on MPIOSM

When the RESET signal is asserted, all the DDR bits are cleared. The data bits are undefined after reset.

17.14.7 MPIOSM Testing

No special test logic has been implemented in this submodule. To be flexible while selecting the number of implemented pins, the test patterns are implemented in a bit per bit modular fashion.

17.14.8 MPIOSM Registers

The privilege level to access to the MPIOSM registers depends on the MIOS14MCR SUPV bit. The privilege level is unrestricted after reset and can be change to supervisor by software.

17.14.9 MPIOSM Register Organization

MPIOSM— Register Organization

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
0x30 6100	MPIOSM Data Register (MPIOSMDR)														
0x30 6102	MPIOSM Data Direction Register (MPIOSMDDR)														
0x30 6104	Reserved														
0x30 6106	Reserved														

17.14.9.1 MPIOSMDR — MPIOSM Data Register

MPIOSMDR — MPIOSM Data Register **0x30 6100**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
SRESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 17-40 MPIOSMDR Bit Descriptions

Bit(s)	Name	Description
0:15	DATA15 — DATA0	These bits are read/write data bits that define the value to be driven to the pad in output mode, for each implemented I/O pin of the MPIOSM

17.14.9.2 MPIOSMDDR — MPIOSM Data Direction Register

MPIOSMDDR — MPIOSM Data Direction Register **0x30 6102**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
DDR15	DDR14	DDR13	DDR12	DDR11	DDR10	DDR9	DDR8	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
SRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17-41 MPIOSMDDR Bit Descriptions

Bit(s)	Name	Description
0:15	DDR15 — DDR0	These bits are read/write data bits that define the data direction status for each implemented I/O pin of the MPIOSM 0 = corresponding pin is input. 1 = corresponding pin is output.

17.15 Real-Time Clock Submodule (MRTCSM)

In this section the values taken by the bits in the registers are given according to the following rule:

- 0 → reset (negated)

- 1 → set (asserted)
- u → undefined
- - → unaffected

17.15.1 MRTCSM Overview Description

The MIOS real-time clock submodule (MRTCSM) is a function included in the MIOS library. It is a software-programmable counter suitable for keeping track of the time of the day, maintaining calendar information or timestamping incoming system events.

The purpose of the MRTCSM is to provide a real time function independently of other MIOS submodules, which may be sustained on a separate standby power supply. The MRTCSM was designed to minimize current drained from battery when in standby.

This time counter is driven by a dedicated 32.768-KHz low-power oscillator. The core of the MRTCSM is a 47-bit counter chain, split as a 15-bit prescaler and a 32-bit free-running counter. Seconds, minutes, hours and days can be derived by software from the 32-bit counter. The MRTCSM can maintain a unique one-second count over a period of approximately 136 years. The prescaler provides additional sub-second information for precise timestamping.

The MRTCSM has interrupt generation capability for one of eight delays ranging from one second to 2^{23} seconds (approximately three months).

17.15.1.1 MRTCSM Terminology

In this section, the following terminology is used:

Update — The term “update” indicates the buffers are updated from the counter and/or prescaler.

Transfer — The term “transfer” is used to indicate a data transfer from the buffer to the counter and prescaler.

17.15.1.2 MRTCSM Features

- Programmable 47-bit free-running ripple counter for minimum power consumption split into a 15-bit prescaler and a 32-bit second counter
- Buffering of the 47-bit free-running counter to guaranty 32-bit and 47-bit coherent accesses on the 16-bit MIOB bus
- Possibility of suppressing 15-bit prescaler update
- Software shutdown of the dedicated low power oscillator to maintain battery shelf life

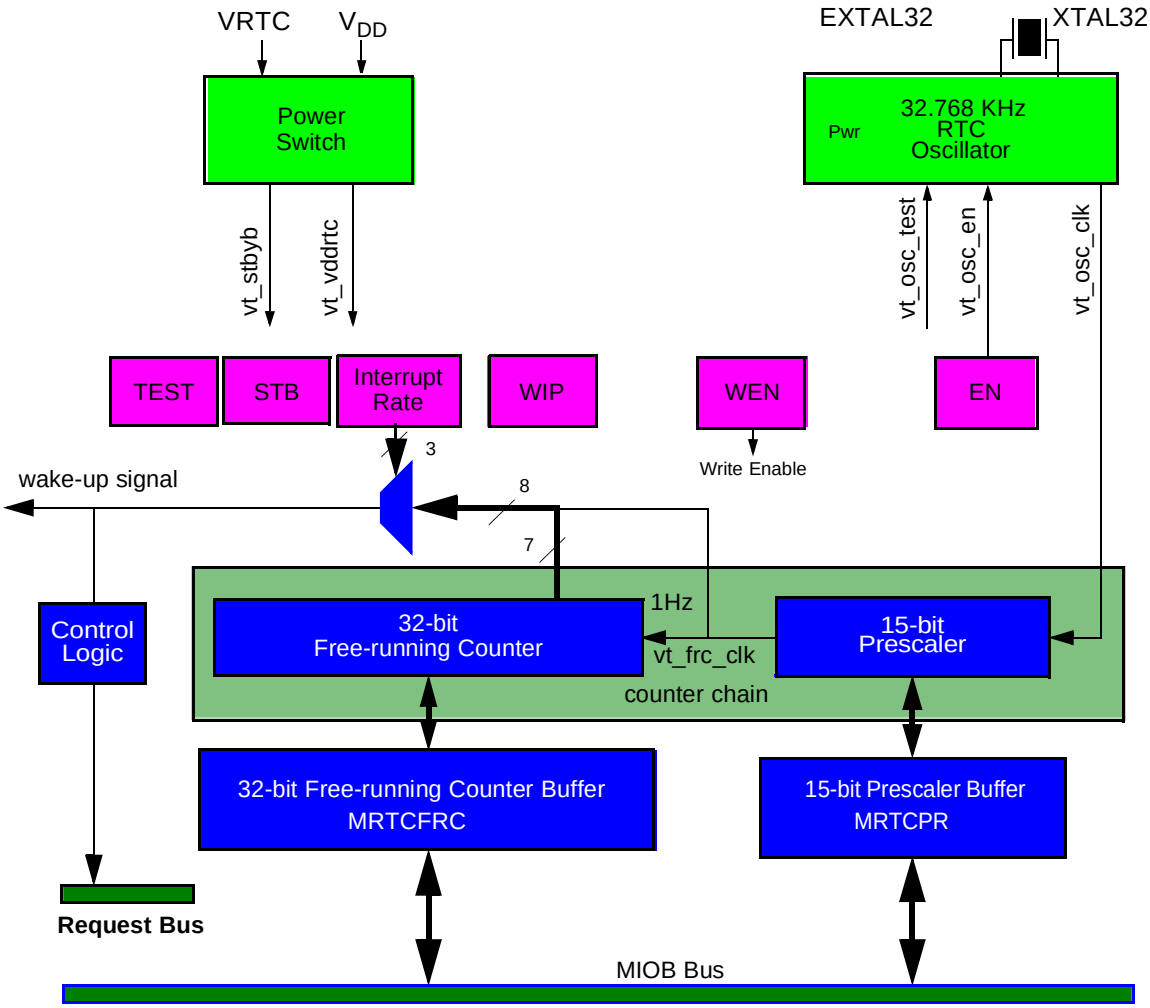


Figure 17-22 MRTCSM Block Diagram

- Flag setting and possible interrupt generation according to eight software selectable rates
- Wake-up signal generation for chip level usage
- Automatic hardware power supply selection through dedicated power switch
- Customized to use low cost standard 32.768-KHz crystal for internal clocking of the 32-bit counter at one Hz
- Software accessible precision of 2^{-15} second and unique time indication in seconds over a span of 136 years (2^{32} seconds)
- Eliminates risk of time inaccuracy due to interrupt overruns appearing in systems with software accumulated time

17.15.1.3 MRTCSM Pad Functions

The MRTCSM has no dedicated pads. However its dedicated power switch needs two pads for the 32.768-KHz crystal while its dedicated power switch needs one.

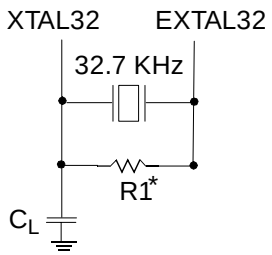
17.15.2 MRTCSM Description

This section describes the MRCTSM and its dedicated oscillator and power switch. Refer to the specifications of these two external modules for more information. Refer to **Figure 17-22** for a block diagram of the MRTCSM.

17.15.2.1 Oscillator

The basic time base for the MRTCSM is a 32.768-KHz dedicated low power oscillator. This oscillator uses an external crystal connected between the XTAL32 and EXTAL32 pads as a reference frequency source. The dedicated 32.768-KHz oscillator is in the chip periphery with the pads for the 32.768-KHz crystal. Having a dedicated oscillator with its uninterruptable power supply allows the counter chain (15-bit prescaler and 32-bit free-running counter) to run while the rest of the chip is powered down. The 32.768-KHz clock signal which is output by the oscillator is called vt_osc_clk. The frequency of the oscillator is called OSC_FREQ. The EXTAL32 pin has an internal load capacitor. Therefore an external load capacitor is not require on EXTAL32. The C_L on the XTAL32 side of the crystal should be according to the crystal manufacturer, typically 12 pF. The MIOS RTC oscillator circuit is shown in **Figure 17-23**.

The enable bit (EN) in the MRTCSM control register (MRTCSCR) can disable the oscillator and counter chain for maximum power saving. When enabled, the oscillator supplies the clock to the counter chain.



*Resistor is not currently required on the board but room should be left on the board for its addition in the future.

Figure 17-23 MIOS RTC Oscillator Circuit

17.15.2.2 Standby Supply and Power Switch

The MRTCSM power switch selects either the main power V_{DD} or dedicated standby power V_{RTC} as power supply (vt_vddrtc) for the MRTCSM. The power switch also generates the internal vt_stbyb signal which indicates in the MRTCSM which of the two supplies is selected:

- vt_stbyb = 0, standby mode, V_{RTC} supply selected

• vt_stbyb = 1, normal mode, V_{DD} supply selected

Normal mode is selected when V_{DD} is greater than V_{RTC}. The MRTCSM is supplied by V_{DD} and all the MRTCSM functions are allowed. Read and write operations to the MRTCSM registers comply to the description given in **17.15.1 MRTCSM Overview Description**.

The standby mode is selected automatically by hardware when the main V_{DD} supply becomes lower than the VRTC supply. While in standby mode, the MRTCSM is supplied by the VRTC supply. The counter chain continues to count the time from the dedicated 32.768-KHz oscillator. However, the buffers of the counter chain are no longer updated. If, despite being in standby mode, a buffer read or write operation occurs, a bus error is returned. Write operations to any of the MRTCSM registers have no effect.

The loss of primary power V_{DD} does not cause the counter chain to be affected as long as the VRTC power pad is above its minimum operating voltage. Only the loss of primary and standby power cause the content of the counter chain to be lost.

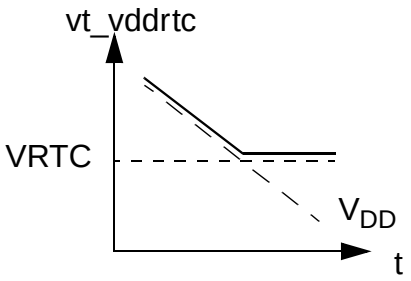


Figure 17-24 Selection of vt_vddrtc

17.15.2.3 Counter Chain

The MRTCSM avoids the software burden of servicing periodic interrupts to count time of day and calendar information. The software needs an initialization procedure that determines the preset state of the counter chain. After initialization, the software can calculate the current time and the current date from the contents of the counter chain. The software fetches the contents of the counter chain either regularly, with a periodic interrupt or as a low priority task in the application's software loop, or whenever needed. In any case, software response time problems during intensive CPU usage will not affect the counter chain accuracy.

When the EN bit in MRTCSCR is set, the MRTCSM oscillator and the counter chain are running. The counter chain is clocked with every rising edge of vt_osc_clk. Refer to **Figure 17-25** for timing details.

17.15.2.4 15-Bit Prescaler

The prescaler is a 15-bit presetable ripple counter designed to require minimum power consumption. The input clock is vt_osc_clk. The output is the vt_frc_clk clock signal used by the 32-bit free-running counter and runs at one Hz.

The 15-bit prescaler is double buffered in order to synchronize the available data and to allow easy coherent register accesses. The 15-bit prescaler can only be accessed through the 15-bit prescaler buffer (MRTCPR)

17.15.2.5 32-Bit Free-running Counter

The MRTCSM has a 32-bit presetable binary free-running counter that increments every second. The input to this counter is vt_frc_clk which comes directly from the 15-bit prescaler. The counter chain overflows approximately every 136 years.

The 32-bit free-running counter is double buffered in order to synchronize the available data and to allow easy coherent register accesses. The 32-bit free-running counter can only be accessed through the 32-bit free-running counter buffer (MRTCFRC).

17.15.2.6 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers

The 15-bit prescaler buffer (MRTCPR) and 32-bit free-running counter buffer (MRTCFRC) shown in **Figure 17-22** serve two purposes:

- Synchronize the counter chain signals (vt_osc_clk and vt_frc_clk) to the peripheral bus system clock
- Provide coherent access to 47-bit or 32-bit data on a 16-bit data bus

MRTCFRC and MRTCPR can be read at any time. They must be written in conjunction and can only be written if the write enable bit (WEN) is set. Refer to **17.15.1.2 MRTCSM Features** for details concerning write operations to the buffers.

When doing regular byte or word read operations, the coherency of subsequent accesses is not guaranteed. Specific hardware is implemented that allows coherent accesses by using long word operations. Refer to **17.12.20 MDASMSCR — MDASM Status/Control Register** for the description of coherent accesses.

17.15.3 Modes of Operation

The following subsections describe how MRTCPR and MRTCFRC are updated and how they should be accessed by software.

17.15.3.1 Enabling the MRTCSM

The EN enable bit of the MRTCSCR register selects whether the oscillator and counter chain are running or not. The MRTCSM can be disabled (EN = 0) by software for maximum power saving (e.g., to maintain battery shelf life).

When the MRTCSM is disabled, writing to MRTCPR and MRTCFRC may give unpredictable results.

17.15.3.2 15-Bit Prescaler and 32-Bit Free-Running Counter Buffer Updates

When the MRTCSM is enabled (EN = 1), MRTCPR and MRTCFRC are updated at the OSC_FREQ rate. The timing for updating the buffers is shown in **Figure 17-25**. The 47-bit counter chain is incremented at every rising edge of vt_osc_clk. A pulse is generated after the falling edge of vt_osc_clk to synchronize transfers and updates of the buffers to/from the counter chain. In this document, this synchronized pulse is called vt_sync.

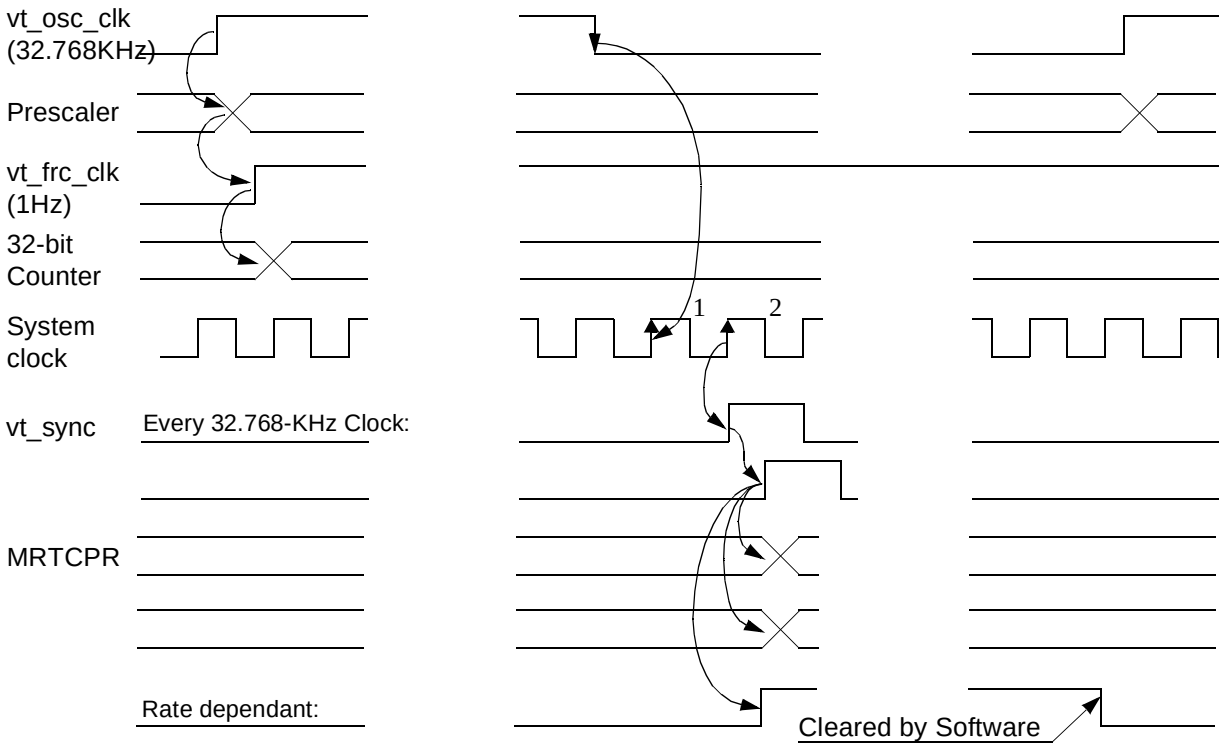


Figure 17-25 15-Bit Prescaler and 32-Bit Free-Running Counter Buffer Updates

In standby mode (vt_stbyb = 0), the update of MRTCPR and MRTCFRC is stopped to reduce power consumption. Access to all the MRTCSM registers is then inhibited. When exiting standby mode, the update of MRTCPR and MRTCFRC is reestablished at the regular OSC_FREQ rate starting on the next vt_sync.

In some particular conditions, the update of MRTCPR can be disabled. Refer to **17.15.2.2 Standby Supply and Power Switch** for more details.

17.15.3.3 Read of 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers

The addresses of the different MRTCSM registers are given in **17.15.9 MRTCSM Registers**. Byte or word accesses to MRTCPR, MRTCFRCH and MRTCFRCL can be performed at any time. However, the coherency between reads is not guaranteed

when using byte or word accesses since these buffers may be updated in between read operations.

In order to guarantee coherent reads, the following procedure should be followed:

1. Execute a long word read of MRTCFRC (at address MRTCFRCH)
2. Execute a word read of MRTCPR (optional)

If vt_sync occurs while a long word read operation of MRTCFRC is in progress, the update of the buffer is deferred until the end of the long word read.

Long word reads to MRTCFRC disable the update of MRTCPR until the next word read of MRTCPR. Once a 15-bit prescaler buffer read operation is performed, MRTCPR updates resume at the OSC_FREQ rate, starting with the next vt_sync.

17.15.3.4 Write to 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers

Write operations to the buffers have no effect if WEN is reset.

In order to write a new value coherently to the complete counter chain, the following sequence must be performed:

1. Set the WEN bit in the MRTCSCR register
2. Execute a long word write to MRTCFRC (at address MRTCFRCH), or two word writes to MRTCFRCH and MRTCFRCL
3. Execute a word write to MRTCPR

When the WEN bit is set, the update of MRTCPR and MRTCFRC is stopped. When MRTCPR is written to, the WEN bit is reset and the buffers become read only. The written values will then be transferred to the counter chain at the next vt_sync pulse. Following this sequence, the buffers will be updated from the counter chain at their regular OSC_FREQ rate, as described in **17.15.3.2 15-Bit Prescaler and 32-Bit Free-Running Counter Buffer Updates**. The option of disabling the update of MRTCPR from the counter chain is not affected by the write operation.

Once WEN is set, write MRTCFRC before MRTCPR. Not doing so transfers an old value of MRTCFRC to the counter chain.

When a word write to MRTCPR happens after setting the WEN bit, the WIP read only bit in the MRTCSCR register is set. This bit is reset once the transfer has occurred. The WIP bit indicates to the programmer that a write procedure is in progress

While doing a coherent write, once the prescaler buffer has been written to, the WEN bit cannot be set again until the full contents of MRTCPR and MRTCFRC have been transferred to the counter chain. Trying to set the WEN bit before this operation is completed has no effect.

If a reset appears while doing a coherent write or after a coherent write before the next vt_sync, the write operation is aborted and the buffers are updated as usual from the counter chain at the next vt_sync pulse.

17.15.4 MRTCSM Interrupt

The MRTCSM is capable of generating interrupts at a fixed time interval. The value of the interrupt rate is determined by the MRTCSCR bits IR2, IR1 and IR0. These three bits control which bit in the counter chain will be monitored for a positive edge. Therefore, the interrupt rates are powers of two of the vt_frc_clk period. The interrupt flag is updated synchronously with vt_sync.

The possible rates which can be selected are shown in **Table 17-46**.

Interrupts are not generated when writing a new value to the counter chain.

When exiting low power mode with the peripheral bus clock stopped or standby mode, buffers contain unpredictable values until the next vt_sync and the periodic interrupt flag is undetermined until the second vt_sync. The programmer should consider clearing the corresponding RQSM interrupt enable bit before entering these low power or standby modes to avoid possible interrupts when exiting these modes.

17.15.5 Chip Wake-Up Feature

In the case of main power supply shut-down, the chip clocks are stopped. A wake-up signal is available at the MIOS14 periphery that allows the MRTCSM to wake up the chip periodically. This signal reflects the status of one of the bits of the counter chain. The period is programmable by setting IR2, IR1 and IR0 appropriately, and is the same as the interrupt signal period (refer to **Table 17-46**).

EXAMPLE

This feature can be used to get the chip out of the low power mode. Refer to the chip specification for details about the use of the wake-up signal.

17.15.6 Modular I/O Bus (MIOB) Interface

- The MRTCSM is connected to all the signals in the read/write and control bus, to allow data transfer from and to the MRTCSM registers, and to control the MRTCSM
- The MRTCSM does not use the counter bus set
- The MRTCSM uses the request bus to transmit the FLAG line to its request submodule (RQSM)

17.15.6.1 Low Power Mode — Peripheral Bus Clock Running

As long as the peripheral bus clock is running, the MRTCSM is running normally.

17.15.6.2 Low Power Mode — Peripheral Bus Clock Stopped

If the peripheral bus clock is stopped, the update of the prescaler and counter buffers is not possible. The interrupt flag is also not updated and consequently cannot be used to exit this low power mode. However, the operation of the wake-up signal, the dedi-

cated 32.768-KHz oscillator and the counter chain are not disturbed by this mode. The wake-up signal can still be used to exit this mode.

As soon as this low power mode is exited, the update of MRTCPR and MRTCFRC is done at their regular OSC_FREQ rate, starting on the next vt_sync. Until this update occurs, the buffers contain unpredictable values. Refer to **17.15.4 MRTCSM Interrupt** for a description of the effect of this mode on the interrupt flag.

When a coherent write operation is performed, it is mandatory to wait for the vt_sync following the completion of this operation before entering this low power mode.

17.15.7 Effect of Standby Mode on MRTCSM

When in standby mode, the MRTCSM is supplied by the VRTC power supply. The counter chain continues to count clocked by the 32.768-KHz oscillator. However, the update of MRTCPR and MRTCFRC is stopped. The interrupt flag is also not updated and consequently cannot be used to exit this mode.

In order to prevent loss of data in a run away situation during power-up and power-down sequences, the access to all the MRTCSM registers is inhibited. It is recommended to use an external LVI circuit asserting the RESET pin when the main V_{DD} supply is below the minimum specified value.

When exiting the standby mode, the update of MRTCPR and MRTCFRC is done at the regular OSC_FREQ rate, starting on the next vt_sync. Until this update occurs, the buffers contain unpredictable values. Refer to **17.15.4 MRTCSM Interrupt** for a description of the effect of this mode on the interrupt flag.

The standby mode should not be entered during a coherent write operation or while WIP is set. If this happens, the correct transfer to the counter chain is not guaranteed.

The prescaler update power saving feature described in **17.15.3.3 Read of 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers** is not affected by standby mode.

17.15.8 Effect of RESET on MRTCSM

When the MIOB reset is asserted, the access to all the MRTCSM registers is blocked. The operation of the MRTCSM oscillator, counter chain and buffer updates is not affected by reset. The interrupt rate selection and the prescaler update power saving feature are not affected by reset. Only the WEN, TEST, STB and WIP bits of the MRTCSCR register are affected by reset. Refer to **17.15.9 MRTCSM Registers** for more details.

Reset should not occur during a coherent write operation or while WIP is set. If this happens, the transfer operation is not guaranteed.

Since the interrupt rate and the power saving feature are not affected by the reset, initialize these options when the device is powered for the first time.

On a power-on reset, after a standby mode, buffers contain unpredictable values and the periodic interrupt flag is undetermined until the second vt_sync. However, the interrupt enable will have been cleared by reset in the corresponding RQSM.

17.15.9 MRTCSM Registers

The privilege level to access the MRTCSM registers depends on the MIOS14MCR SUPV bit. This privilege level is reset to user and can be changed to supervisor by software.

17.15.10 MRTCSM Register Organization

The MRTCSM register map comprises four 16-bit register locations.

All unused bits return zero when read by the software. All register addresses in this section are specified as offsets from the base address of the MRTCSM.

MRTCSM— Register Organization

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
0x30 6050	MRTCSM Free-running counter buffer high register (MRTCFRCH)														
0x30 6052	MRTCSM Free-running counter buffer low register (MRTCFRCL)														
0x30 6054	MRTCSM Prescaler buffer register (MRTCPR)														
0x30 6056	MRTCSM status and control register (MRTCSCR)														

17.15.10.1 MRTCSM Free-Running Counter High Buffer (MRTCFRCH) Register Bits

MRTCSMFRCH — MRTCSM 32-Bit Counter High Buffer Register **0x30 6050**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
SRESET:															
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 17-42 MRTCSMFRCH Bit Descriptions

Bit(s)	Name	Description
0:15	CH15 — CH0	MRTCFRCH is the data register associated with the 32-bit free-running counter high buffer. It contains the synchronized high word value of the 32-bit free-running counter or the value to be loaded into the high word 32-bit free-running counter. The MRTCFRCH register is not affected by reset.

17.15.10.2 MRTCSM Free-Running Counter Low Buffer (MRTCFRCL) Register Bits

MRTCSMFRCL — MRTCSM 32-Bit Counter Low Buffer Register **0x30 6052**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
SRESET:															
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 17-43 MRTCSMFRCL Bit Descriptions

Bit(s)	Name	Description
0:15	CL15 — CL0	MRTCFRCL is the data register associated with the 32-bit free-running counter low buffer. It contains the synchronized low word value of the 32-bit free-running counter or the value to be loaded into the low word 32-bit free-running counter. The MRTCFRCL register is not affected by reset.

17.15.10.3 MRTCSM Prescaler Counter Buffer (MRTCPR) Register Bits

MRTCPR — MRTCSM Prescaler Counter Buffer Register **0x30 6054**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	0
SRESET:															
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 17-44 MRTCPR Bit Descriptions

Bit(s)	Name	Description
0:15	PR15 — PR0	MRTCPR is the data register associated with the prescaler buffer. It contains the synchronized value of the 15-bit prescaler or the value to be loaded into the 15-bit prescaler. The MRTCPR register is not affected by reset.

17.15.10.4 MRTCSMSCR — MRTCSM Status/Control Register

The status and control register gathers read/write bits related to its control and configuration.

MRTCSMSCR — MRTCSM Status/Control Register **0x30 6056**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
WIP	RESERVED			WEN	EN	RESERVED		TEST	STB	RESERVED			IR2	IR1	IR0
SRESET:															
0	0	0	0	0	—	0	0	0	0	0	0	0	—	—	—

Table 17-45 MRTCSMSCR Bit Descriptions

Bit(s)	Name	Description
0	WIP	Write in progress status bit — This read only bit indicates that a transfer from the buffers to the counter chain is in progress. This bit is set when writing to MRTCPR during the coherent write procedure and is reset once the transfer to the counter chain has occurred. 0 = No transfer from buffers to counter chain in progress. 1 = Transfer from buffers to counter chain in progress. The WIP bit is cleared by reset.
1:3	—	Reserved
4	WEN	Write enable control bit — This active high control bit allows the counter chain to be written to. MRTCPR and MRTCFRC are read only registers and regular write operations to these registers have no effect. When the WEN bit is set, it enables writing to the counter chain buffers. **17.15.3.4 Write to 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers** describes the coherent write procedure to be used. **NOTE:** The WEN bit cannot be set while the WIP bit is set. The WEN bit is cleared by reset.
5	EN	Enable control bit — This active high bit enables real time clock operation. It selects whether the MRTCSM is running or not. 0 = MRTCSM is not running. Oscillator, counter chain and associated logic is not running, thus completely disabling the MRTCSM for maximum power saving. 1 = MRTCSM is running, all MRTCSM functions are enabled. The EN bit is not affected by reset and is undefined after the first power-up of the MRTCSM. **17.15.3.1 Enabling the MRTCSM** describes the enabling of the MRTCSM. **NOTE:** The EN bit cannot be modified while the WIP bit is set.
6:7	—	Reserved
9	TEST	This bit is reserved for factory testing only and should never be writen to one. The TEST bit is cleared by reset.
10	STB	This bit is reserved for factory testing only and must always be zero. The STB bit is cleared by reset.
10:12	—	Reserved
13:15	IR[2:0]	Interrupt rate control bits — The three interrupt rate control bits select the rate of the timer interrupt. Refer to **Table 17-46** to determine the rate of the real time clock interrupt.

Table 17-46 Interrupt Rate Selection

MRTCSM Control Register Bits			**Monitored Counter Chain Bit #N**	**MRTCSM Interrupt Rate When vt_osc_clk = 32.768KHz (2N/32768)**
IR2	**IR1**	**IR0**		
0	0	0	15 (output of prescaler)	1 second
0	0	1	21	64 seconds = 1.1 minutes
0	1	0	25	1024 seconds = 17.1 minutes
0	1	1	27	4096 seconds = 1.1 hours
1	0	0	31	65536 second = 18.2 hours
1	0	1	34	524288 seconds = 6.1 days
1	1	0	36	2097152 seconds = 24.3 days
1	1	1	38	8388608 seconds = 3.2 months

The interrupt rate control bits are unaffected by reset and unknown after the first power-up of the MRTCSM.