APPENDIX A
MPC509L3C25 ELECTRICAL CHARACTERISTICS

The MPC509L3C25 is the first implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors designed for embedded control. This document contains pertinent physical characteristics of the MPC509L3C25. For functional characteristics of a similar processor bus, refer to the ***MPC500 Family RCPU Reference Manual*** **(RCPURM/AD)**.

A.1 MPC509L3C25 Overview

The MPC509L3C25 is the first implementation of the PowerPC based family of embedded control RISC microprocessors. The MPC509L3C25 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits.

The MPC509L3C25 is a processor capable of issuing and retiring one instruction per clock; one instruction to one of four execution units. Instructions can complete out of order for increased performance; however, the MPC509L3C25 makes execution appear sequential.

The MPC509L3C25 integrates four execution units: an integer unit (IU), an integer multiply and divide unit (IMU), a load/store unit (LSU) and a floating-point unit (FPU). The use of simple instructions with rapid execution times yield high efficiency and throughput for MPC509L3C25-based systems. Most integer instructions execute in one clock cycle. The FPU is designed to provide a high functionality, cost effective solution to most mathematical problems including a single and double-precision multiply-add instruction.

The MPC509L3C25 includes an on-chip, 4-Kbyte, two-way set-associative, physically addressed, instruction cache, chip select logic to reduce and usually eliminate external decoding logic, 28-Kbyte static RAM, and extensive processor debugging functionality.

The MPC509L3C25 has a high-bandwidth, 32-bit data bus and a 32-bit address bus. The MPC509L3C25 statically supports 16-bit memories. The MPC509L3C25 supports single-beat and burst data transfers for memory accesses; it also supports memory-mapped I/O.

The MPC509L3C25 uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

The reset configuration word is 0xD3DBF0A3.

A.2 MPC509L3C25 Features

Major features of the MPC509L3C25 are as follows:

- High-performance, embedded control microprocessor
  - — As many as four instructions in execution per clock (one to each of the four execution units)
  - — Single clock cycle execution for most instructions
  - — Single-precision and double-precision FPU
- High instruction and data throughput
  - — Branch folding capability during execution (zero cycle branch execution time)
  - — Static branch prediction on unresolved conditional branches
  - — A prefetch queue that can hold as many as four instructions
  - — Four-Kbyte cache: two-way set-associative, LRU replacement algorithm
  - — Run-time reordering of loads and stores
- Facilities for enhanced system performance
  - — 32-bit external data bus
  - — 16-bit static bus sizing for cost sensitive applications
  - — Address pipelinable external data bus with 4 beat burst transfers
  - — Chip select logic which generates all signals for memory system designs
  - — Six different address ranges for the chip select logic with 12 different pins

A.3 MPC509L3C25 Electrical Characteristics

This section provides both the AC and DC electrical characteristics for the MPC509L3C25 microprocessor.

NOTE

The following information is preliminary and subject to change without notice.

A.3.1 MPC509L3C25 DC Electrical Characteristics

Table A-1 provides the maximum ratings for the MPC509L3C25.

Table A-1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage*	V_{DD}	4.0	V
EXTAL input voltage (Note: V_{in} must not exceed the maximum supply voltage)	V_{in}	V_{DD} + 0.3	V
TTL-compatible input voltage	V_{in}	5.6	V
Operating temperature range	T_A	-40 to +85	°C
Storage temperature range*	T_{stg}	-55 to +150	°C

Table A-2 provides the DC electrical characteristics for the MPC509L3C25.

Table A-2 . DC Electrical Characteristics

Characteristic	Notes	Symbol	Min	Max	Unit
Supply voltage		V_{DD}	3.0	3.6	V
Input high voltage EXTAL TTL-compatible inputs		V_{IH}	.75 * V_{DD}	V_{DD} + 0.3 5.5	V
Input low voltage		V_{IL}	V_{SS} – 0.3	0.3 * V_{DD}	V
Output high voltage I_{OH}=-100 µA * I_{OH}=-800 µA	1	 V_{OH} V_{OH}	 V_{DD} – 0.20 0.8 * V_{DD}	 — —	 V V
Output low voltage I_{OL}=100 µA * I_{OL}=1.2 mA	1	 V_{OL} V_{OL}	 — —	 0.20 0.2 * V_{DD}	 V V
Output high current Address and address attributes Data Control CLK, ECROUT, $\overline{\text{RESETOUT}}$ XTAL		I_{OH}	 -0.8 -0.5	 — —	 mA mA
Output low current Address and address attributes Data Control CLK, ECROUT, $\overline{\text{RESETOUT}}$ XTAL		I_{OL}	0.8 0.5	— —	mA
Leakage with 5-V input			-3.1	+3.1	µA
Input leakage current: Pins without internal pull-up or pull-down devices(normal operation).	$V_{SS} < V_{in} < V_{DD}$	I_{in}	-2.5	2.5	µA
Pins with internal pull-up devices: $\overline{\text{AACK}}$, $\overline{\text{ARETRY}}$, $\overline{\text{BB}}$, $\overline{\text{BI}}$, $\overline{\text{CR}}$, IRQ[6:0], $\overline{\text{TA}}$, $\overline{\text{TEA}}$, TDI, TMS, $\overline{\text{TRST}}$	Normal operation	I_{in}	2.0	50.0	µA
Pins with internal pull-up devices: A[0:29], DATA[0:31], $\overline{\text{BE}}$[0:3], CT[0:3], AT[0:1], $\overline{\text{WP}}$[0:5], VF[0:2], VFLS[0:1], $\overline{\text{IRQ}}$[0:6], $\overline{\text{WR}}$, $\overline{\text{TS}}$, $\overline{\text{AACK}}$, $\overline{\text{TA}}$, $\overline{\text{TEABR}}$, $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{BI}}$, $\overline{\text{BURST}}$, $\overline{\text{BDIP}}$, $\overline{\text{ARETRY}}$, $\overline{\text{CR}}$, $\overline{\text{RESET}}$, DSCK, DSDI, MODCK	For JTAG external pull-up test only	I_{in}	2.0	50.0	µA
Pins with internal pull-down devices: $\overline{\text{BG}}$, DSCK, DSDI, TCK	Normal operation	I_{in}	5.0	150.0	µA

Table A-2 . DC Electrical Characteristics (Continued)

Characteristic	Notes	Symbol	Min	Max	Unit
Hi-Z (off-state) leakage current	@ 125°C	I_{oz}	-2.5	2.5	µA
Capacitance (see Note)* V_{in} = 0 V, f = 1 MHz		C_{in}	—	10	pF
V_{DD} supply current RUN @ 24 MHz LPSTOP, VCO & XTAL active LPSLEEP, VCO & XTAL off		I_{DD}	— — —	175 3 100	mA mA µA
Clock synthesizer operating voltage*		V_{DDSYN}	V_{DD} – 0.1V	V_{DD} + 0.1 V	V
Keep alive supply voltage* (V_{DDI} = V_{DDE} = ON)		V_{DDKAP1} V_{DDKAP2}	V_{DD} – 0.3 V V_{DD} – 0.3 V	V_{DD} + 0.3 V V_{DD} + 0.3 V	V V
Standby supply current (V_{DDE} = V_{DDI} = OFF) V_{DDKAP1} only V_{DDKAP2} only (RAM standby current) V_{DDKAP1} & V_{DDKAP2}		I_{SB}	— — —	2.0 50 2.0	mA µA mA
V_{DDSYN} supply current VCO on, default f_{sys},normal mode		I_{DDSYN}	—	2.0	mA
RAM standby voltage *		V_{SB}	1.8	—	V

Notes: Capacitance is periodically sampled rather than 100% tested.
*Guaranteed by design/characterization
[1]Voltage specs use V_{ss} = 0 V for a reference.

A.3.2 MPC509L3C25 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC509L3C25. Note that all AC electrical specifications pertain to 25-Mhz operation. If the frequency of operation is slower than 25-Mhz output valid times will be greater. To determine output valid specifications for slower frequencies, use the formula:

Output valid time for slower frequency = output valid time for 25 Mhz – $P_{25\ Mhz}/4 + P_{slow}/4$

where P_{slow} is the period of the slower frequency.

A.3.2.1 Input AC Characteristics

Table A-3 provides the clock AC timing specifications for the MPC509L3C25 as defined in **Figure A-1**.

Table A-3 . Clock AC Timing Specifications

V_{DD} = 3.3 Vdc ± 0.3, GND = 0 Vdc, T_J MAX = 125° C, θ_j = 37° C/Watt[1]

Num	Characteristic	Symbol	25 Mhz		Unit
			Min	Max	
	Frequency of operation [3] (Note: 0 Hz not tested)	f_{sys}	0	25	MHz
1	System clock period [3,6]	Clk	—	40.0	ns
	Output clock jitter [6]	T_{CLKJ}	—	2	%
	Output clock duty cycle [6]	DC_{CLK}	48.5	51.5	%
2	Clock rise time [6]	t_{cr}	—	3	ns
3	Clock fall time [6]	t_{cf}	—	3	ns
	ECROUT jitter [6]	T_{ECRJ}	—	.5	%
	ECROUT duty cycle [6]	DC_{ECR}	48	52	%
	ECROUT rise time [6]	T_{ECRR}	—	3	ns
	ECROUT fall time [6]	T_{ECRF}	—	3	ns
	PLL start time	t_{SPLLL}	—	15	ms
	PLL lock time [2,5]	t_{PLLL}	—	5	ms
	PLL normal mode reference frequency range[4,6] (4.000 MHz is tested)	f_{XTAL}	3	5	MHz
	PLL one-to-one mode reference frequency range (12 MHz is tested)		15	25	MHz
	PLL one-to-one mode clock skew (CLKIN to CLKOUT)[6]		0	5	ns
	PLL by-pass mode reference frequency range[6] (100 kHz – 300 kHz is tested)		0	50	MHz
	PLL by-pass mode clock skew (CLKIN to CLKOUT)[6]		0	7	ns
	PLL by-pass mode reference clock duty cycle[6]		45	55	%

NOTES:
2. Proper PCB layout procedures must be followed to achieve specifications.
3. All internal registers retain data at 0.0 Hz.
4. If 10-Mhz reference clock is used then PLL multiplication factor should be set to 4x (MF = b000).
5. Worst-case lock time considered to be 3 Mhz to 25 Mhz., assuming a 0.1 µF capacitor. Lock time may vary depending upon capacitor used.
6. Guaranteed by design or characterization.

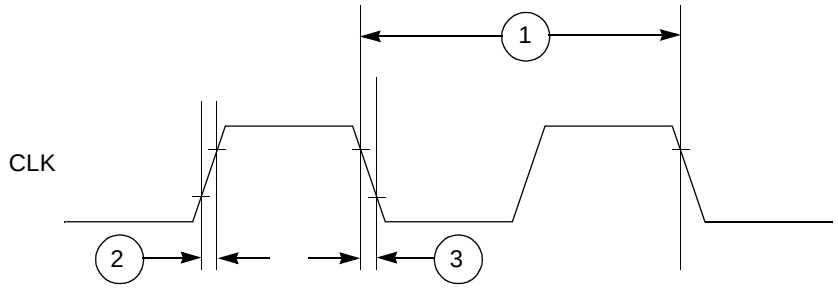

Figure A-1 Clock Input Timing Diagram

Table A-4 : MPC509L3C25 Input AC Timing Specifications

(V_{CC} = 3.3 ± 0.3 V_{dc}, GND = 0 V_{dc}). See **Figure A-2**.

Num	Characteristic	Symbol	25 Mhz		Unit
			Min	Max	
	Reset input assertion time				
6	Input valid to CLK (input setup)				
6a	$\overline{AACK}$[2]		7	—	ns
6b	$\overline{TA}$[2]		8	—	ns
6bb	$\overline{BB}$[2]		7.5	—	ns
6c	$\overline{BI}$[2]		8	—	ns
6d	$\overline{BG}$[3]		8	—	ns
6e	$\overline{TEA}$[2]		10	—	ns
6f	$\overline{ARTRY}$[2]		10	—	ns
6g	$\overline{CR}$[2]		8	—	ns
7	Input valid to CLK (input setup) Data		6	—	ns
8	Input valid to CLK (input setup) IRQ[0:6][2]		6	—	ns
	Input valid to CLK (input setup)				
10a	DSCK[3] & DSDI[3]		10	—	ns
10b	Ports		20	—	ns
11	Input hold				
11a	$\overline{AACK}$[2]		2.5	—	ns
11b	$\overline{TA}$[2]		2.5	—	ns
11bb	$\overline{BB}$[2]		2.5	—	ns
11c	$\overline{BI}$[2]		2.5	—	ns
11d	$\overline{BG}$[3]		2.5	—	ns
11e	$\overline{TEA}$[2]		2.5	—	ns
11f	$\overline{ARTRY}$[2]		2.5	—	ns
11g	$\overline{CR}$[2]		2.5	—	ns
12	Input hold Data		4	—	ns
13	Input hold IRQ[0:6][2]		4	—	ns

Table A-4 : MPC509L3C25 Input AC Timing Specifications (Continued)

(V_{CC} = 3.3 ± 0.3 V_{dc}, GND = 0 V_{dc}). See **Figure A-2**.

Num	Characteristic	Symbol	25 Mhz		Unit
			Min	Max	
	Input hold				
15a	DSCK[3] & DSDI[3]		4	—	ns
15b	Ports		4	—	ns

Notes:

1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input CLK. Both input and output timings are measured at the pin. See **Figure A-2**.
2. Internal pull-up resistors are on these pins.
3. Internal pull-down resistors are on these pins.

Table A-5 : MPC509L3C25 Output AC Timing Specifications

(V_{CC} = 3.3 ± 0.3 V_{dc}, GND = 0 V_{dc}) See **Figure A-2**.

Num	Characteristic	Symbol	25 Mhz		Unit
			Min	Max	
16	CLK to $\overline{\text{CS\_BOOT}}$, A1:A5 valid (configured as a chip enable)	t_{cev}	—	25	ns
17	CLK to $\overline{\text{CS\_BOOT}}$, A0:A11 valid (configured as an output enable in synchronous mode)	t_{oev}	—	25	ns
18	CLK to $\overline{\text{CS\_BOOT}}$, A0:A11 valid (configured as a write enable or output enable in asynchronous mode)	t_{wev}	—	30	ns
19	CLK to A0:A29 valid configured as the address bus	t_{addv}	—	29	ns
20	CLK to A0:A15 valid configured as a general purpose port	t_{pv}	—	25	ns
21	CLK to D0:D31 valid	t_{dv}	—	22.5	ns
22	CLK to control pins valid				
22a	WR	t_{wrv}	—	25	ns
22b	BDIP	t_{bipv}	—	25	ns
22c	Burst	t_{bv}	—	25	ns
22d	BE[0:3]	t_{bev}	—	25	ns
22e	AT[0:1]	t_{atv}	—	25	ns
22f	CT[0:3]	t_{ctv}	—	25	ns
22g	TS	t_{tsv}	—	25	ns
22h	BR & BB	t_{bav}	—	25	ns
23	CLK to debug pins valid				
23a	VF[0:2]	t_{vfv}	—	25	ns
23b	VFLS[0:1]	t_{vflsv}	—	25	ns
23c	WP[0:5]	t_{bv}	—	25	ns
23d	DSDO	t_{bev}	—	25	ns
25a	CLK to all other output pins valid	t_{v}	—	25	ns
25b	CLK to port pins valid	t_{portv}	—	25	ns

Table A-5 : MPC509L3C25 Output AC Timing Specifications (Continued)

(V_{CC} = 3.3 ± 0.3 V_{dc}, GND = 0 V_{dc}) See **Figure A-2**.

Num	Characteristic	Symbol	25 Mhz		Unit
			Min	Max	
26	CLK to $\overline{\text{CS\_BOOT}}$, A1:A5 output hold (configured as a chip enable)	t_{ceh}	4	—	ns
27	CLK to $\overline{\text{CS\_BOOT}}$, A0:A11 output hold (configured as an output enable in synchronous mode)	t_{oeh}	4	—	ns
28	CLK to $\overline{\text{CS\_BOOT}}$, A0:A11 output hold (configured as a write enable or output enable in asynchronous mode)	t_{weh}	2	—	ns
29	CLK to A0:A29 output hold configured as the address bus	t_{addh}	4	—	ns
30	CLK to A0:A15 output hold configured as a general purpose port	t_{ph}	4	—	ns
31	CLK to D0:D31 output hold	t_{dh}	4	—	ns
32	CLK to control pins output hold				
32a	WR	t_{wrh}	4	—	ns
32b	BDIP	t_{biph}	4	—	ns
32c	Burst	t_{bh}	4	—	ns
32d	BE[0:3]	t_{beh}	4	—	ns
32e	AT[0:1]	t_{ath}	4	—	ns
32f	CT[0:3]	t_{cth}	4	—	ns
32g	TS	t_{tsh}	4	—	ns
32h	BR & BB	t_{bah}	4	—	ns
33	CLK to debug pins output hold				
33a	VF[0:2]	t_{vfh}	4	—	ns
33b	VFLS[0:1]	t_{vflsh}	4	—	ns
33c	WP[0:5]	t_{bh}	4	—	ns
33d	DSDO	t_{beh}	4	—	ns
35	CLK to all other output pins output hold	t_h	2	—	ns
35a	CLK to port pins output hold	t_{porth}	2	—	ns

NOTES:

1. All output specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the CLKOUT. Both input and output timings are measured at the pin.
2. All maximum timing specifications assume C_L = 50 pF.
3. $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$ and $\overline{\text{IRQ}}$ are not intended to be at a high impedance therefore they can not be left floating.
4. All other output are: $\overline{\text{WR}}$, $\overline{\text{BURST}}$, $\overline{\text{BE0:BE3}}$, AT0:AT1, CT0:CT3, $\overline{\text{TS}}$, $\overline{\text{BDIP}}$, $\overline{\text{BR}}$, $\overline{\text{BB}}$, VF0:VF2, VFLS0:VFLS1, DSDO, WP0:WP5.
5. Output to tristate timing is guaranteed by design to be:
   a) no more than 1/4 system clock after the negation of bg_l (followed by the negation of bb_l, or
   b) no more that 1 system clock after the negation of bb_l (followed by the negation of bg_l).
   Remember, actual output time to tristate will depend on hardware board characteristics.

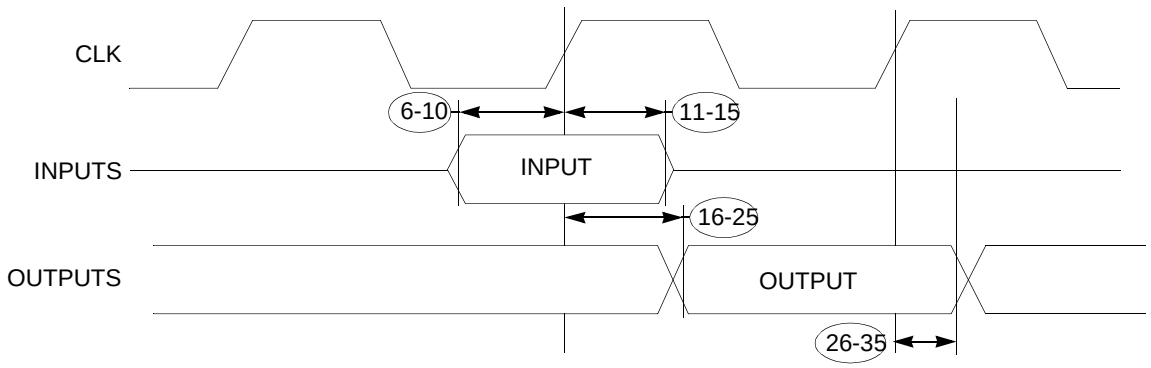

Figure A-2 Input Timing Diagram

Table A-6 JTAG AC Timing Characteristics (Independent of CLK)

Num	Characteristic	Min	Max	Unit
	TCK frequency of operation[2] (0 MHz not tested)	0	8	MHz
J1	TCK cycle time	125	—	ns
J2	TCK clock pulse width measured at 2.0 V	62.5	—	ns
J3	TCK rise and fall times	0	2	ns
J4	TRST setup time for negation to TCK rising edge[2]	10	—	ns
J5	TRST assert time	20	—	ns
J6	Boundary scan input data setup time to rising edge of TCK	20	—	ns
J7	Boundary scan input data hold time to rising edge of TCK	45	—	ns
J8	TCK falling edge to output data valid	0	55	ns
J9	TCK falling edge to output high impedance	0	70	ns
J10	TMS, TDI data setup time to rising edge of TCK	20	—	ns
J11	TMS, TDI data hold time to rising edge of TCK	45	—	ns
J12[1]	TCK falling edge to TDO data valid	0	30	ns
J13[1]	TCK falling edge to TDO high impedance	0	65	ns

Notes:
1.Load capacitance = 50pF.
2. Guaranteed by design/characterization.

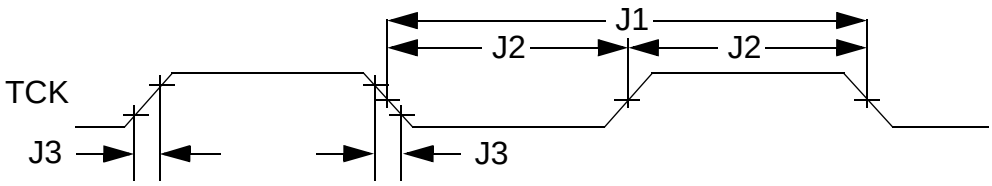

Figure A-3 JTAG Clock Input Timing Diagram

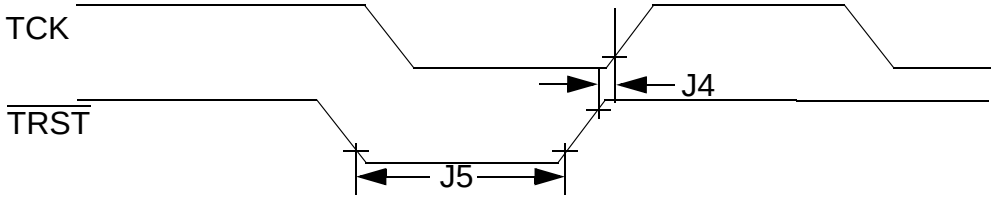

Figure A-4 TRST Timing Diagram

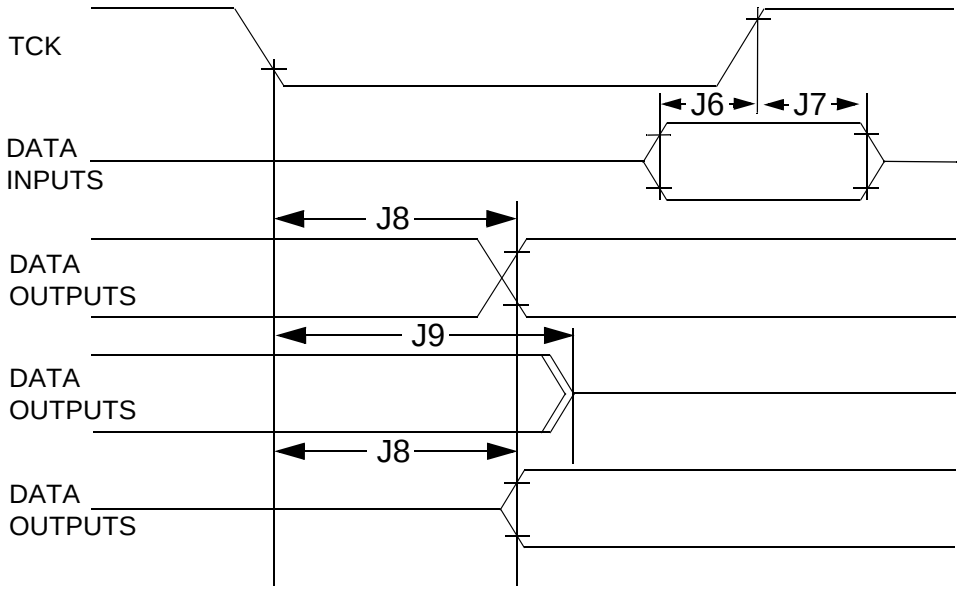

Figure A-5 Boundary Scan Timing Diagram

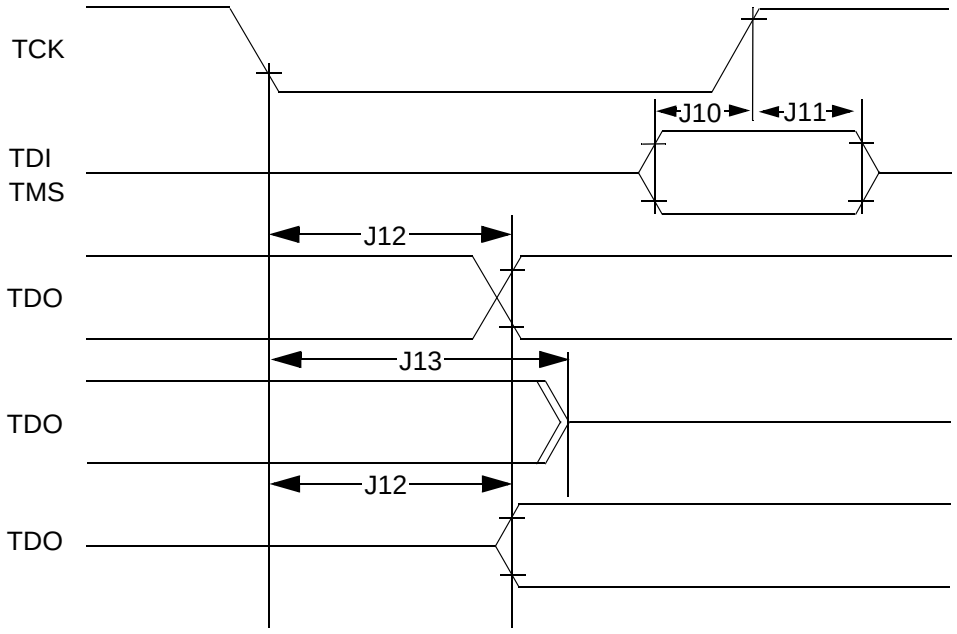

Figure A-6 Test Access Port Timing Diagram

A.4 Timing Examples

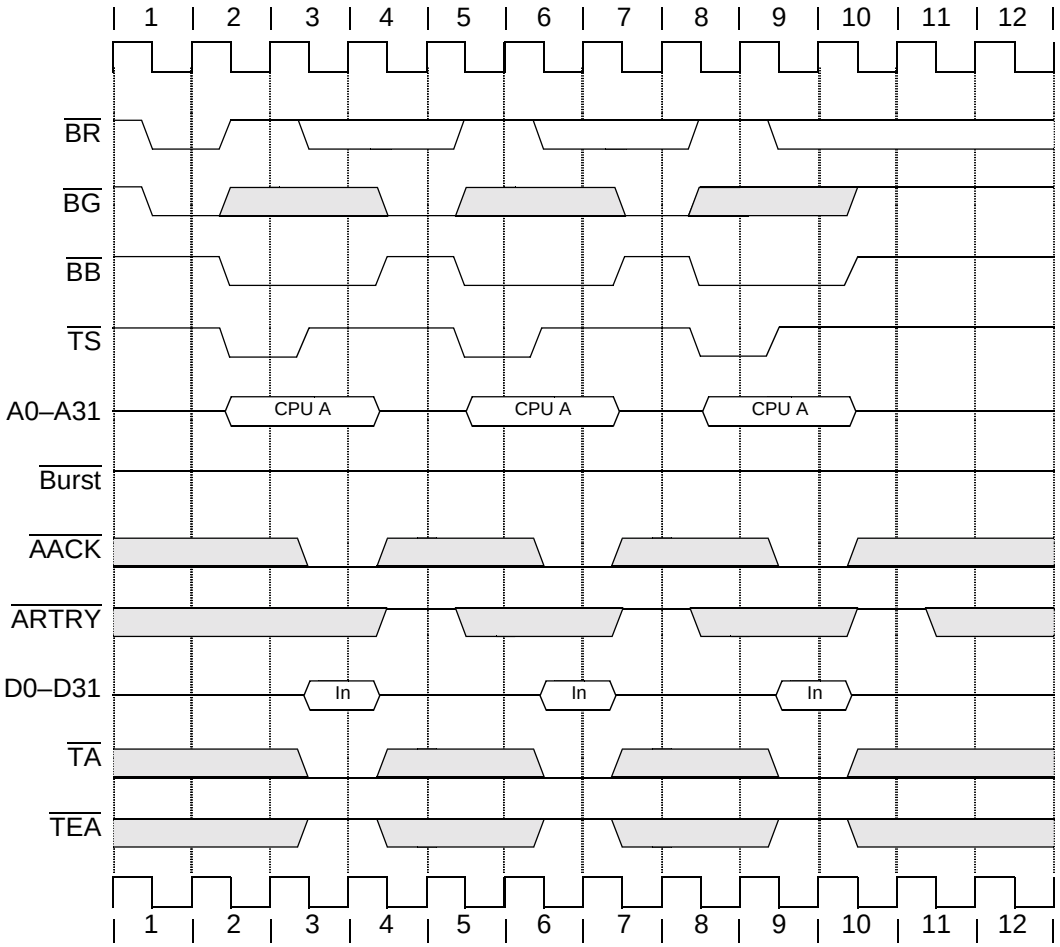

Figure A-7 Fastest Single Beat Read

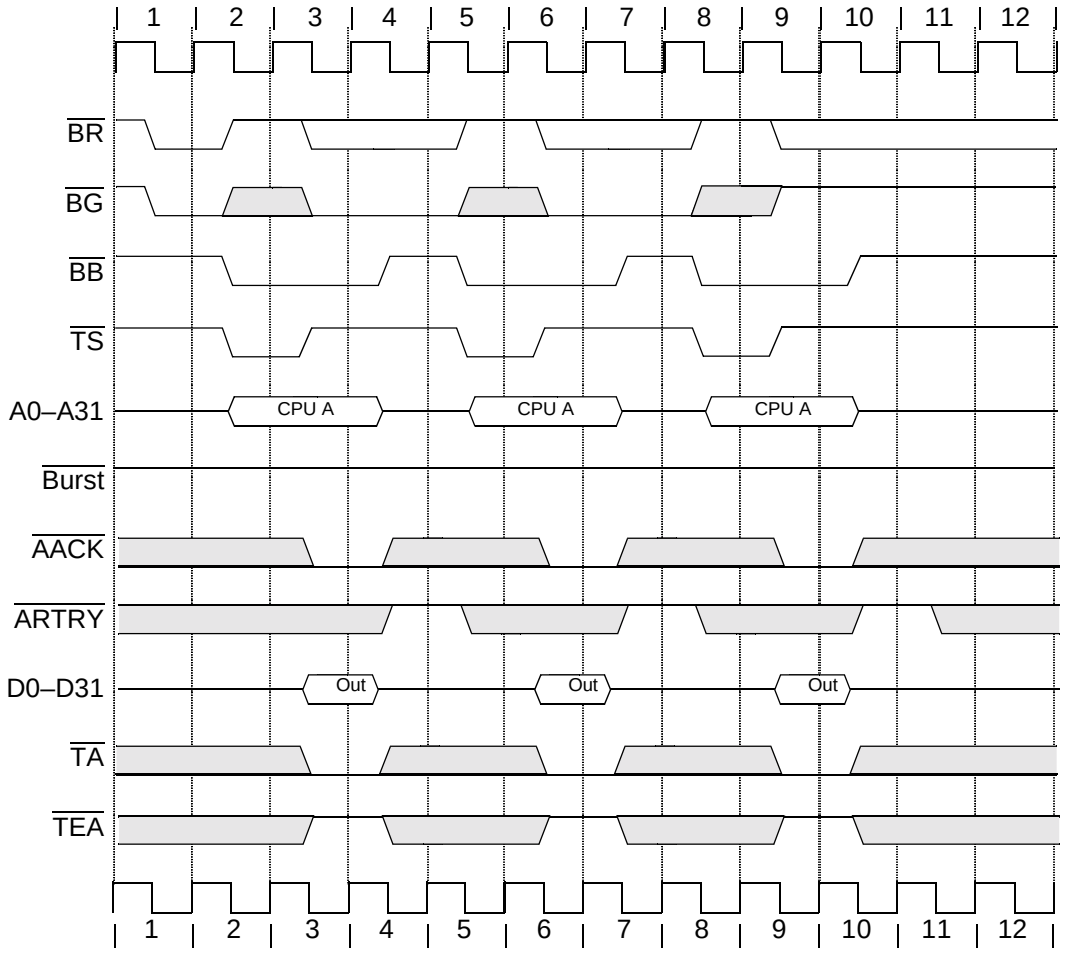

Figure A-8 Fastest Single Beat Writes

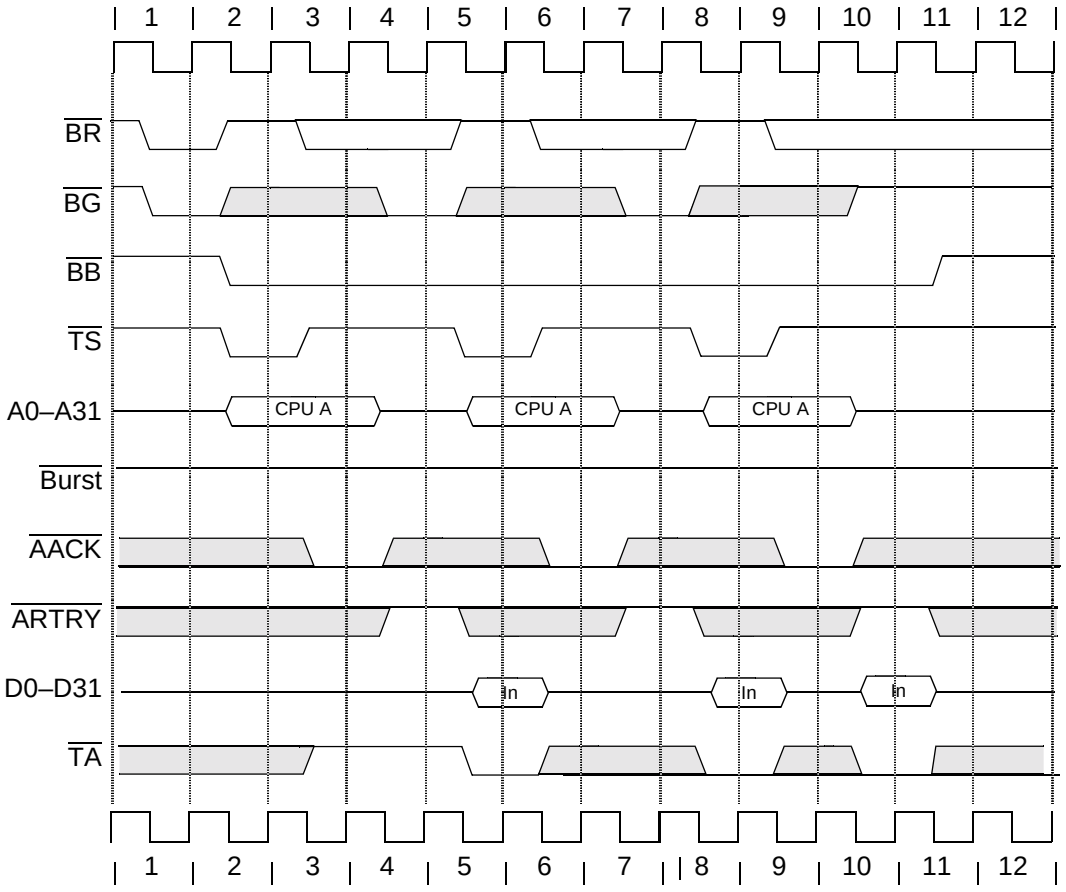

Figure A-9 Single-Beat Reads Showing Data-Delay Controls

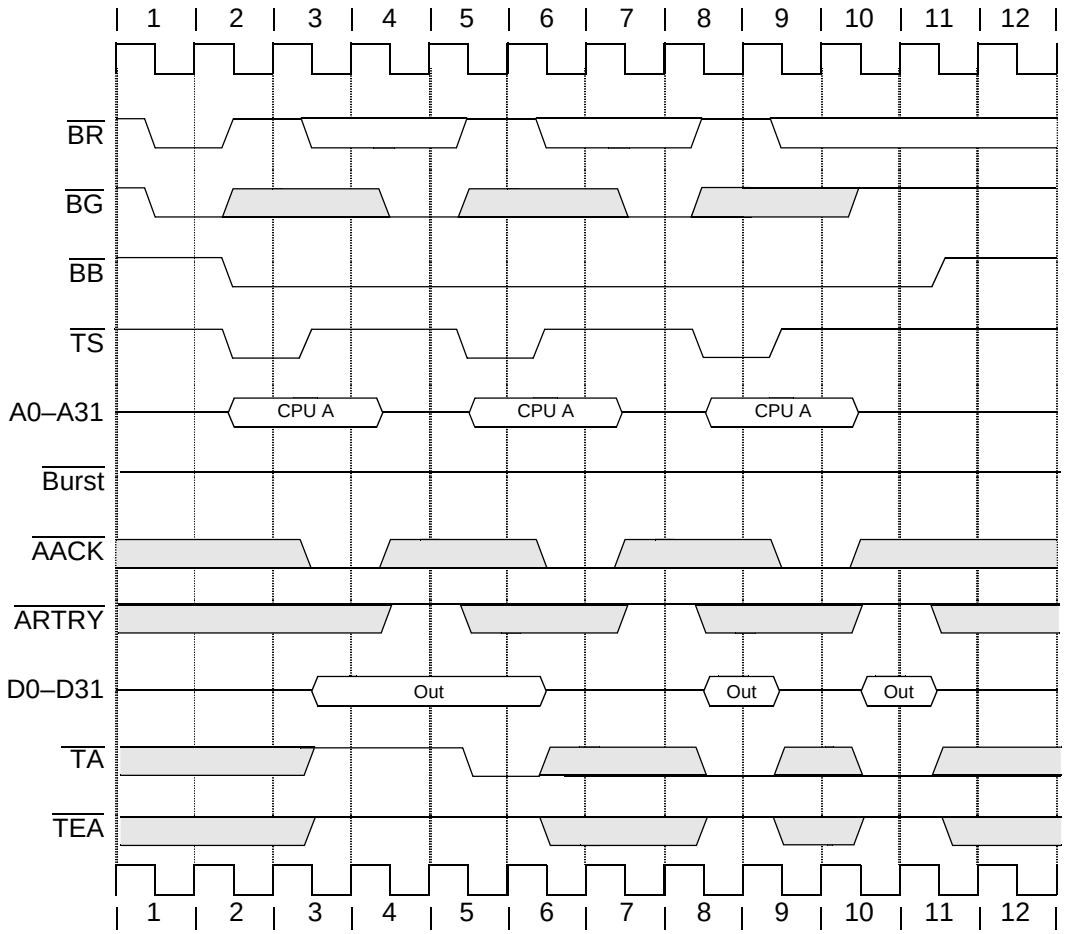

Figure A-10 Single-Beat Writes Showing Data Delay Controls

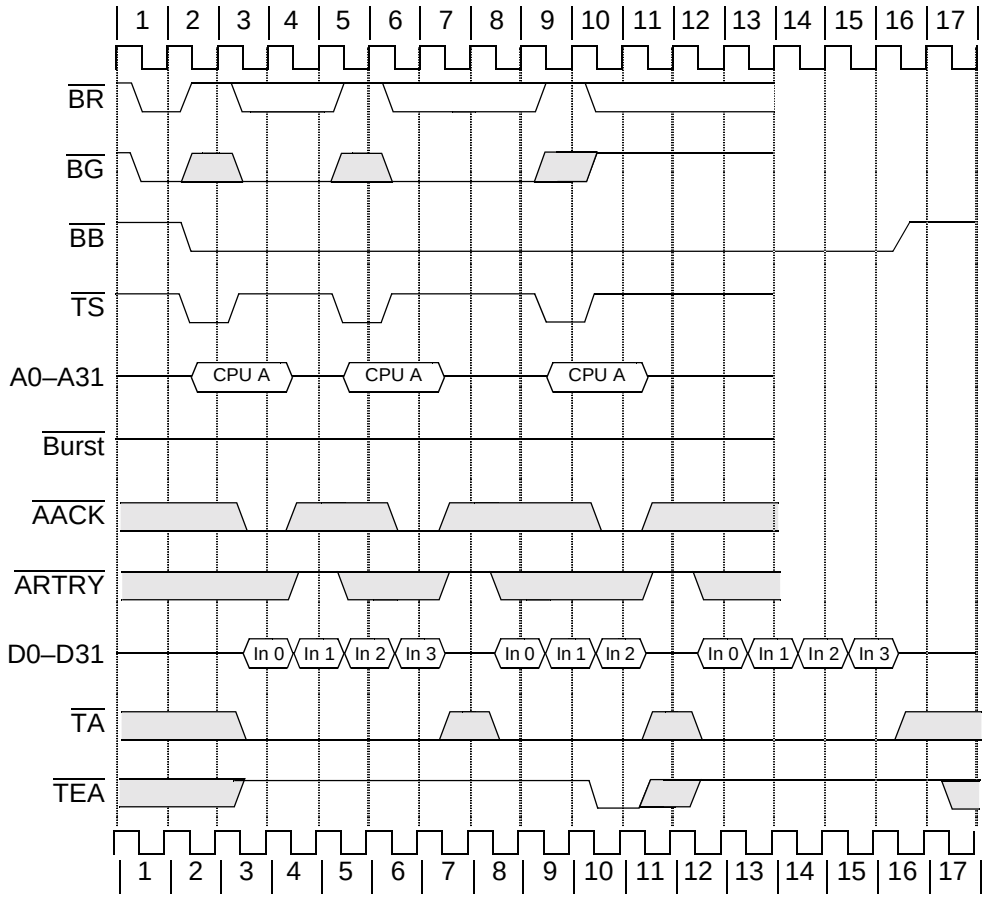

Figure A-11 Use of Transfer Error Acknowledge ($\overline{\text{TEA}}$)

A.5 MPC509L3C25 Pinout

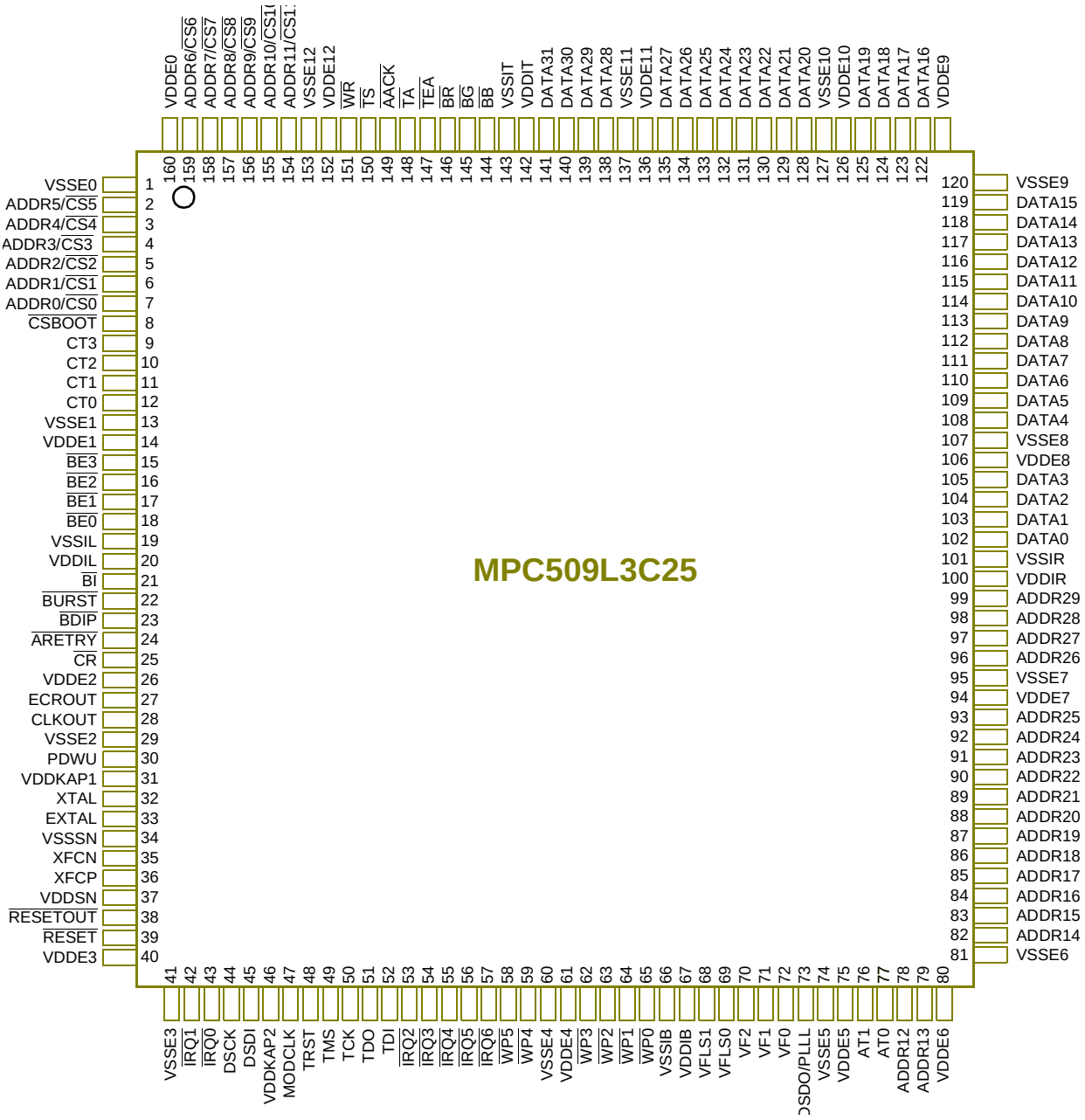

Figure A-12 MPC509L3C25 Pinout