APPENDIX A
INTERNAL MEMORY MAP

The tables below use the following notations.

In the Access column:

S = Supervisor Access Only
U = User Access
T = Test Access

In the Reset column:

A = Affected by $\overline{\text{RESET}}$
U = Unchanged
X = Unknown

The codes in the Reset column indicate which reset has an effect on register values.

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Table A-1 QADC64 (1) (Queued Analog-to-Digital Converter)

Address	Access	Symbol	Register	Size	Reset
0xYF F000	S	QADC64MCR	QADC64 Module Configuration Register. See **Table 8-7** for bit descriptions.	16	X
0xYF F002	T	QADC64TEST	QADC64 Test Register	16	X
0xYF F004	S	QADC64INT	Interrupt Register. See **Table 8-8** for bit descriptions.	16	X
0xYF F006	S	PORTQA/ PORTQB	Port A and Port B Data. See **Table 8-9** for bit descriptions.	16	X
0xYF F008	S	DDRQA	Port A Data Direction Register. See **Table 8-10** for bit descriptions.	16	X
0xYF F00A	S	QACR0	QADC64 Control Register 0. See **Table 8-11** for bit descriptions.	16	X
0xYF F00C	S	QACR1	QADC64 Control Register 1. See **Table 8-12** for bit descriptions.	16	X
0xYF F00E	S	QACR2	QADC64 Control Register 2. See **Table 8-14** for bit descriptions.	16	X
0xYF F010	S	QASR0	QADC64 Status Register 0. See **Table 8-16** for bit descriptions.	16	X
0xYF F012	S	QASR1	QADC64 Status Register 1. See **Table 8-18** for bit descriptions.	16	X
0xYF F014 – 0xYF F0FE	—	—	Reserved	—	—

Table A-2 TouCAN (1) (CAN 2.0B Controller)

0xYF F100 — 0xYF F10F	S/U	MBUFF0	TouCAN Message Buffer 0. See **Table 10-5** and **Table 10-6** for message buffer definitions.	—	U
0xYF F110 — 0xYF F11F	S/U	MBUFF1	TouCAN Message Buffer 1. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F120 — 0xYF F12F	S/U	MBUFF2	TouCAN Message Buffer 2. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F130 — 0xYF F13F	S/U	MBUFF3	TouCAN Message Buffer 3. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F140 — 0xYF F14F	S/U	MBUFF4	TouCAN Message Buffer 4. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F150 — 0xYF F15F	S/U	MBUFF5	TouCAN Message Buffer 5. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F160 — 0xYF F16F	S/U	MBUFF6	TouCAN Message Buffer 6. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F170 — 0xYF F17F	S/U	MBUFF7	TouCAN Message Buffer 7. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F180 — 0xYF F18F	S/U	MBUFF8	TouCAN Message Buffer 8. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U

Table A-2 TouCAN (1) (CAN 2.0B Controller) (Continued)

0xYF F190 — 0xYF F19F	S/U	MBUFF9	TouCAN Message Buffer 9. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F1A0 — 0xYF F1AF	S/U	MBUFF10	TouCAN Message Buffer 10. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F1B0 — 0xYF F1BF	S/U	MBUFF11	TouCAN Message Buffer 11. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F1C0 — 0xYF F1CF	S/U	MBUFF12	TouCAN Message Buffer 12. See **Table 10-5** and **Table 10-6** for message buffer definitions.	—	U
0xYF F1D0 — 0xYF F1DF	S/U	MBUFF13	TouCAN Message Buffer 13. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F1E0 — 0xYF F1EF	S/U	MBUFF14	TouCAN Message Buffer 14. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U
0xYF F1F0 — 0xYF F1FF	S/U	MBUFF15	TouCAN Message Buffer 15. See **Table 10-4** and **Table 10-2** for message buffer definitions.	—	U

Table A-3 QADC64 (2) (Queued Analog-to-Digital Converter)

0xYF F300 – 0xYF F37F	S	CCW	QADC64 Conversion Command Word Table. See **Table 8-19** for bit descriptions.	16	X
0xYF F380 – 0xYF F3FE	S	RJURR	QADC64 Result Word Table Right-Justified, Unsigned Result Register. See **8.12.10 Conversion Command Word Table** for bit descriptions.	16	X
0xYF F300 – 0xYF F37E	S	LJSRR	QADC64 Result Word Table Left-Justified, Signed Result Register. See **8.12.11 Result Word Table** for bit descriptions.	16	X
0xYF F380 – 0xYF F3FE	S	LJURR	QADC64 Result Word Table Left-Justified, Unsigned Result Register. See **8.12.11 Result Word Table** for bit descriptions.	16	X

Table A-4 QSM_B (Queued Serial Module B)

Address	Access	Symbol	Register	Size	Reset
0xYF F400	S	QSMCR_B	QSM Module Configuration Register. See **Table 7-3** for bit descriptions.	16	X
0xYF F402	T	QTEST_B	QSM Test Register.	16	X
0xYF F404	S	QILR/QIVR_B	QSM Interrupt Level/interrupt Vector Register. See **Table 7-8** and **Table 7-9** for bit descriptions.	16	X
0xYF F406	S	—	Reserved	—	X
0xYF F408	S	SCCR0_B	SCI1 Control Register 0. See **Table 7-22** for bit descriptions.	16	X
0xYF F40A	S	SCCR1_B	SCI1Control Register 1. See **Table 7-24** for bit descriptions.	16	X

Table A-4 QSM_B (Queued Serial Module B) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F40C	S	SCSR_B	SCI1 Status Register. See **Table 7-26** for bit descriptions.	16	X
0xYF F40E	S	SCDR_B	SCI1 Data Register. See **Table 7-27** for bit descriptions.	16	X
0xYF F410 – 0xYF F412	S	—	Reserved	—	X
0xYF F414	S	PORTQS_B	QSMCM Port QS Data Register. See **7.2.3.1 QSM Port Data Register (PORTQS)** for bit descriptions.	16	X
0xYF F416	S	PQSPAR_B / DDRQST_B	QSMCM Port QS Pin Assignment Register/ QSMCM Port QS Data Direction Register. See **Table 7-11** and **Table 7-13** for bit descriptions.	16	X
0xYF F418	S	SPCR0_B	QSPI Control Register 0. See **Table 7-14** for bit descriptions.	16	X
0xYF F41A	S	SPCR1_B	QSPI Control Register 1. See **Table 7-16** for bit descriptions.	16	X
0xYF F41C	S	SPCR2_B	QSPI Control Register 2. See **Table 7-17** for bit descriptions.	16	X
0xYF F41E	S	SPCR3_B / SPSR_B	QSPI Control Register 3/QSPI Status Register. See **Table 7-18** and **Table 7-19** for bit descriptions.	16	X
0xYF F420 — 0xYF F4FF	S	—	Reserved	16	X
0xYF F500 — 0xYF F51F	S	SCRQ_B	QSPI Receive Queue Locations. See **7.4.4 Receiver Operation** for bit descriptions.	16	X
0xYF F520 — 0xYF F53F	S	SCTQ_B	QSPI Transmit Queue Locations. See **7.4.3 Transmitter Operation** for bit descriptions.	16	X
0xYF F540 — 0xYF F54F	S	QSPIRAM_B	QSPI Transmit Queue Locations. See **Table 7-20** for bit descriptions.	16	X

Table A-5 DLCMD (Data Link Controller Module)

Address	Access	Symbol	Register	Size	Reset
0xYF F600	S	MCR	DLCMD Module Configuration Register See **Table 11-6** for bit descriptions.	16	X
0xYF F602	S	—	Reserved	16	X
0xYF F604	S	IPR	DLCMD Interrupt Pending Register See **Table 11-8** for bit descriptions.	16	X
0xYF F606 / 0xYF F607	S	ILR / IVR	DLCMD Interrupt Level Register / Interrupt Vector Register See **Table 11-9** and **Table 11-10** for bit descriptions.	16	X
0xYF F608	S / U	SCTL	DLCMD Symbol Timing Control and Pre-Scaler Register See **Table 11-11** for bit descriptions.	16	X
0xYF F60A	S / U	SDATA	DLCMD Symbol Timing Data Register See **Table 11-13** for bit descriptions.	16	X

Table A-5 DLCMD (Data Link Controller Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F60C	S / U	CMD/TDATA	DLCMD Command Register / Transmit Data Register See **Table 11-15** and **Table 11-18** for bit descriptions.	16	X
0xYF F60D/ 0xYF F60E	S	RDATA/STAT	DLCMD Receive Data Register / Status Register / See **Table 11-27** and **Table 11-21** for bit descriptions.	16	X

Table A-6 DPTRAM (Dual-Port TPU RAM)

Address	Access	Symbol	Register	Size	Reset
0xYF F680	S	DPTMCR	DPT module configuration register. See **Table 6-2** for bit descriptions.	16	X
0xYF F682	T	DPTTCR	DPT test register.	16	X
0xYF F684	S	DPTBAR	DPT array address register. See **Table 6-3** for bit descriptions.	16	X
0xYF F686	S	MISRH	DPT multiple input signature register high. See **6.4.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	16	X
0xYF F688	S	MISRL	DPT multiple input signature register low. See **6.4.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	16	X
0xYF F68A	S	MISCNT	DPT multiple input signature counter. See **6.4.5 MISC Counter (MISCNT)** for bit descriptions.	16	X

Table A-7 FASRAM Module (Fast Access Static Random Access Memory)

Address	Access	Symbol	Register	Size	Reset
0xYF F6C0	S	FMCR	FASRAM module configuration register. See **Table 4-2** for bit descriptions.	16	X
0xYF F6C2	S	FTEST	FASRAM module test register. See **Table 4-1** for bit descriptions.	16	X
0xYF F6C4	S	FBAR-H	FASRAM base address register. See **Table 4-3** for bit descriptions.	16	X
0xYF F6C6	S	FBAR-L	FASRAM base address register. See **Table 4-3** for bit descriptions.	16	X
0xYF F6C8	S	FCCR0	FASRAM comparator value 0 register. See **Table 4-4** for bit descriptions.	16	X
0xYF F6CA	S	FCCR1	FASRAM comparator value 1 Register. See **Table 4-4** for bit descriptions.	16	X
0xYF F6CE	S	FMATCH	FASRAM most recent match address Register. See **4.9.3 Most Recent Match Address (FMATCH)** for bit descriptions.	16	X
0xYF F610	S	FSTATUS	FASRAM most recent match status register. See **Table 4-1** for bit descriptions.	16	X
0xYF F612	S	—	Reserved.	16	X
0xYF F61E	S	—	Reserved.	16	X

Table A-8 CTM9 (Configurable Timer Module)

Address	Access	Symbol	Register	Size	Reset
BIUSM (CTM9 Bus Interface Unit Submodule)					
0xYF F700	S	BIUMCR	BIUSM Module Configuration Register. See **Table 9-19** and **9.8.4.1 BIUMCR — BIUSM Module Configuration Register** for bit descriptions.	16	X
0xYF F702	T	BIUTEST	BIUSM Test Register.	16	X
0xYF F704	S	BIUTBR	BIUSM Time Base Register. See **9.8.4.2 BIUTBR — BIUSM Time Base Register** for bit descriptions.	16	X
CPSM (CTM9 Counter Prescaler Submodule)					
0xYF F708	S	CPCR	CPSM Control Register. See **Table 9-21** and **9.9.2.1 CPCR — CPSM Control Register** for bit descriptions.	16	X
0xYF F70A	T	CPTR	CPSM Test Register.	16	X
MCSM2 (CTM9 Modulus Counter Submodule 2)					
0xYF F710	S	MCSM2SIC	MCSM2 Status/Interrupt/Control Register. See **Table 9-5** for bit descriptions.	16	X
0xYF F712	S	MCSM2CNT	MCSM2 Counter Register. See **9.3.2 The MCSM Counter** for bit descriptions.	16	X
0xYF F714	S	MCSM2ML	MCSM2 Modulus Latch Register. See **9.3.11 MCSMML — MCSM Modulus Latch Register** for bit descriptions.	16	X
DASM3 (CTM9 Double-Action Submodule 3)					
0xYF F718	S	DASM3SIC	DASM3 Status/Interrupt/Control Register. See **Table 9-11** and **9.5.5.1 DASMSIC — DASM Status/Interrupt Control Register** for bit descriptions.	16	X
0xYF F71A	S	DASM3A	DASM3 Register A. See **9.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F71C	S	DASM3B	DASM3 Register B. See **9.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
DASM4 (CTM9 Double-Action Submodule 4)					
0xYF F720	S	DASM4SIC	DASM4 Status/Interrupt/Control Register. See **Table 9-11** and **9.5.5.1 DASMSIC — DASM Status/Interrupt Control Register** for bit descriptions.	16	X
0xYF F722	S	DASM4A	DASM4 Register A. See **9.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F724	S	DASM4B	DASM4 Register B. See **9.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
PWM5 (CTM9 Pulse Width Modulation Submodule 5)					
0xYF F728	S	PWM5SIC	PWM5 Status, Interrupt and Control Register. See **Table 9-15** and **9.7.13.1 PWMSIC — Status, Interrupt and Control Register** for bit descriptions.	16	X

Table A-8 CTM9 (Configurable Timer Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F72A	S	PWM5A	PWM5 Period Register. See **9.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F72C	S	PWM5B	PWM5 Pulse Width Register. See **9.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F72E	S	PWM5C	PWM5 Counter Register. See **9.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X
PWM6 (CTM9 Pulse Width Modulation Submodule 6)					
0xYF F730	S	PWM6SIC	PWM6 Status, Interrupt and Control Register. See **Table 9-15** and **9.7.13.1 PWMSIC — Status, Interrupt and Control Register** for bit descriptions.	16	X
0xYF F732	S	PWM6A	PWM6 Period Register. See **9.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F734	S	PWM6B	PWM6 Pulse Width Register. See **9.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F736	S	PWM6C	PWM6 Counter Register. See **9.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X
PWM7 (CTM9 Pulse Width Modulation Submodule 7)					
0xYF F738	S	PWM7SIC	PWM7 Status, Interrupt and Control Register. See **Table 9-15** and **9.7.13.1 PWMSIC — Status, Interrupt and Control Register** for bit descriptions.	16	X
0xYF F73A	S	PWM7A	PWM7 Period Register. See **9.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F73C	S	PWM7B	PWM7 Pulse Width Register. See **9.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F73E	S	PWM7C	PWM7 Counter Register. See **9.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X
PWM8 (CTM9 Pulse Width Modulation Submodule 8)					
0xYF F740	S	PWM8SIC	PWM8 Status, Interrupt and Control Register. See **Table 9-15** and **9.7.13.1 PWMSIC — Status, Interrupt and Control Register** for bit descriptions.	16	X
0xYF F742	S	PWM8A	PWM8 Period Register. See **9.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F744	S	PWM8B	PWM8 Pulse Width Register. See **9.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F746	S	PWM8C	PWM8 Counter Register. See **9.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X

Table A-8 CTM9 (Configurable Timer Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
DASM9 (CTM9 Double-Action Submodule 9)					
0xYF F748	S	DASM9SIC	DASM9 Status/Interrupt/Control Register. See **Table 9-11** and **9.5.5.1 DASMSIC — DASM Status/Interrupt Control Register** for bit descriptions.	16	X
0xYF F74A	S	DASM9A	DASM9 Register A. See **9.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F74C	S	DASM9B	DASM9 Register B. See **9.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
DASM10 (CTM9 Double-Action Submodule 10)					
0xYF F750	S	DASM10SIC	DASM10 Status/Interrupt/Control Register. See **Table 9-11** and **9.5.5.1 DASMSIC — DASM Status/Interrupt Control Register** for bit descriptions.	16	X
0xYF F752	S	DASM10A	DASM10 Register A. See **9.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F754	S	DASM10B	DASM10 Register B. See **9.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
MCSM11 (CTM9 Modulus Counter Submodule 11)					
0xYF F758	S	MCSM11SIC	MCSM11 Status/Interrupt/Control Register. See **Table 9-5** for bit descriptions.	16	X
0xYF F75A	S	MCSM11CNT	MCSM11 Counter Register. See **9.3.2 The MCSM Counter** for bit descriptions.	16	X
0xYF F75C	S	MCSM11ML	MCSM11 Modulus Latch Register. See **9.3.11 MCSMML — MCSM Modulus Latch Register** for bit descriptions.	16	X
FCSM (CTM9 Free Running Counter Submodule)					
0xYF F760	S	FCSMSIC	FCSM Status, Interrupt and Control Register. See **Table 9-2** for bit descriptions.	16	X
0xYF F762	S	FCSMCNT	FCSM Counter Register. See **9.2.7.2 FCSMCNT — FCSM Counter Register** for bit descriptions.	16	X
SASM14 (CTM9 Single-Action Submodule 14)					
0xYF F770	S	S14ICA	SASM14 Status/Interrupt/Control Register A. See **Table 9-7** and **9.4.4.1 SICA — SASM Status/Interrupt Control Register A** for bit descriptions.	16	X
0xYF F772	S	S14DATA	SASM14 Data Register A. See **9.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F774	S	S14ICB	SASM14 Status/Interrupt/Control Register B. See **9.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F776	S	S14DATB	SASM14 Data Register B. See **9.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X

Table A-8 CTM9 (Configurable Timer Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
SASM16 (CTM9 Single-Action Submodule 16)					
0xYF F780	S	S16ICA	SASM16 Status/Interrupt/Control Register. See **Table 9-7** and **9.4.4.1 SICA — SASM Status/Interrupt Control Register A** for bit descriptions.	16	X
0xYF F782	S	S16DATA	SASM16 Data Register. See **9.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F784	S	S16ICB	SASM16 Status/Interrupt/Control Register B. See **9.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F786	S	S16DATB	SASM16 Data Register B. See **9.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X
SASM18 (CTM9 Single-Action Submodule 18)					
0xYF F790	S	S18ICA	SASM18 Status/Interrupt/Control Register. See **Table 9-7** and **9.4.4.1 SICA — SASM Status/Interrupt Control Register A** for bit descriptions.	16	X
0xYF F792	S	S18DATA	SASM18 Data Register. See **9.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F794	S	S18ICB	SASM18 Status/Interrupt/Control Register B. See **9.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F796	S	S18DATB	SASM18 Data Register B. See **9.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X
SASM20 (CTM9 Single-Action Submodule 20)					
0xYF F7A0	S	S20ICA	SASM20 Status/Interrupt/Control Register. See **Table 9-7** and **9.4.4.1 SICA — SASM Status/Interrupt Control Register A** for bit descriptions.	16	X
0xYF F7A2	S	S20DATA	SASM20 Data Register. See **9.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F7A4	S	S20ICB	SASM20 Status/Interrupt/Control Register B. See **9.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F7A6	S	S20DATB	SASM20 Data Register B. See **9.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X

Table A-9 TPU3_B (1) (Time Processor Unit)

Address	Access	Symbol	Register	Size	Reset
0xYF F800	S	TPUMCR_B	TPU3 module configuration register See **Table 5-7** for bit descriptions.	16	X
0xYF F802	T	TCR_B	TPU3 test configuration register	16	X
0xYF F804	S	DSCR_B	Development support control register See **Table 5-8** for bit descriptions.	16	X

Table A-9 TPU3_B (1) (Time Processor Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F806	S	DSSR_B	Development support status register See **Table 5-9** for bit descriptions.	16	X
0xYF F808	S	TICR_B	TPU3 interrupt configuration register See **Table 5-10** for bit descriptions.	16	X
0xYF F80A	S	CIER_B	Channel interrupt enable register See **Table 5-11** for bit descriptions.	16	X
0xYF F80C	S	CFSR0_B	Channel function selection register 0 See **Table 5-12** for bit descriptions.	16	X
0xYF F80E	S	CFSR1_B	Channel function selection register 1 See **Table 5-12** for bit descriptions.	16	X
0xYF F810	S	CFSR2_B	Channel function selection register 2 See **Table 5-12** for bit descriptions.	16	X
0xYF F812	S	CFSR3_B	Channel function selection register 3 See **Table 5-12** for bit descriptions.	16	X
0xYF F814	S	HSQR0_B	Host sequence register 0 See **Table 5-13** for bit descriptions.	16	X
0xYF F816	S	HSQR1_B	Host sequence register 1 See **Table 5-13** for bit descriptions.	16	X
0xYF F818	S	HSRR0_B	Host service request register 0 See **Table 5-13** for bit descriptions.	16	X
0xYF F81A	S	HSRR1_B	Host service request register 1 See **Table 5-14** for bit descriptions.	16	X
0xYF F81C	S	CPR0_B	Channel priority register 0 See **Table 5-15** for bit descriptions.	16	X
0xYF F81E	S	CPR1_B	Channel priority register 1 See **Table 5-15** for bit descriptions.	16	X
0xYF F820	S	CISR_B	Channel interrupt status register See **Table 5-17** for bit descriptions.	16	X
0xYF F822	T	LR_B	Link register	16	X
0xYF F824	T	SGLR_B	Service grant latch register	16	X
0xYF F826	T	DCNR_B	Decoded channel number register	16	X
0xYF F828	S	TPUMCR2_B	TPU module configuration register 2 See **Table 5-18** for bit descriptions.	16	X
0xYF F82A	S	TPUMCR3_B	TPU module configuration 3 See **Table 5-21** for bit descriptions.	16	X
0xYF F82C	T	ISDR_B	Internal scan data register	16	X
0xYF F82E	T	ISCR_B	Internal scan control register	16	X

Table A-10 SRAM Modules (1)
(Static Random Access Memory)

Address	Access	Symbol	Register	Size	Reset
SRAM(A)					
0xYF F840	S	RAMMCR1	SRAM1 Module Configuration Register. See **Table 12-1** for bit descriptions.	16	X
0xYF F842	T	RAMTST1	SRAM1 Test Register.	16	X
0xYF F844	S	RAMBAH1	SRAM1 Base Address High Register. See **Table 12-3** for bit descriptions.	16	X
0xYF F846	S	RAMBAL1	SRAM1 Base Address Low Register. See **Table 12-3** for bit descriptions.	16	X

Table A-10 SRAM Modules (1)
(Static Random Access Memory) (Continued)

Address	Access	Symbol	Register	Size	Reset
SRAM(B)					
0xYF F848	S	RAMMCR2	SRAM2 Module Configuration Register. See **Table 12-1** for bit descriptions.	16	X
0xYF F84A	T	RAMTST2	SRAM2 Test Register.	16	X
0xYF F84C	S	RAMBAH2	SRAM2 Base Address High Register. See **Table 12-3** for bit descriptions.	16	X
0xYF F84E	S	RAMBAL2	SRAM2 Base Address Low Register. See **Table 12-3** for bit descriptions.	16	X
SRAM(C)					
0xYF F850	S	RAMMCR3	SRAM3 Module Configuration Register. See **Table 12-1** for bit descriptions.	16	X
0xYF F852	T	RAMTST3	SRAM3 Test Register.	16	X
0xYF F854	S	RAMBAH3	SRAM3 Base Address High Register. See **Table 12-3** for bit descriptions.	16	X
0xYF F856	S	RAMBAL3	SRAM3 Base Address Low Register. See **Table 12-3** for bit descriptions.	16	X
SRAM(D)					
0xYF F858	S	RAMMCR4	SRAM4 Module Configuration Register. See **Table 12-1** for bit descriptions.	16	X
0xYF F85A	T	RAMTST4	SRAM4 test register.	16	X
0xYF F85C	S	RAMBAH4	SRAM4 base address high register. See **Table 12-3** for bit descriptions.	16	X
0xYF F85E	S	RAMBAL4	SRAM4 base address low register. See **Table 12-3** for bit descriptions.	16	X

Table A-11 TPU3_B (2) (Time Processor Unit)

0xYF F900 – 0xYF F90F	S	—	Channel 0 parameter registers	16	X
0xYF F910 – 0xYF F91F	S	—	Channel 1 parameter registers	16	X
0xYF F920 – 0xYF F92F	S	—	Channel 2 parameter registers	16	X
0xYF F930 – 0xYF F93F	S	—	Channel 3 parameter registers	16	X
0xYF F940 – 0xYF F94F	S	—	Channel 4 parameter registers	16	X
0xYF F950 – 0xYF F95F	S	—	Channel 5 Parameter Registers	16	X
0xYF F960 – 0xYF F96F	S	—	Channel 6 parameter registers	16	X
0xYF F970 – 0xYF F97F	S	—	Channel 7 parameter registers	16	X
0xYF F980 – 0xYF F98F	S	—	Channel 8 parameter registers	16	X
0xYF F990 – 0xYF F99F	S	—	Channel 9 parameter registers	16	X
0xYF F9A0 – 0xYF F9AF	S	—	Channel 10 parameter registers	16	X

Table A-11 TPU3_B (2) (Time Processor Unit) (Continued)

0xYF F9B0 – 0xYF F9BF	S	—	Channel 11 parameter registers	16	X
0xYF F9C0 – 0xYF F9CF	S	—	Channel 12 parameter registers	16	X
0xYF F9D0 – 0xYF F9DF	S	—	Channel 13 parameter registers	16	X
0xYF F9E0 – 0xYF F9EF	S	—	Channel 14 parameter registers	16	X
0xYF F9F0 – 0xYF F9FF	S	—	Channel 15 parameter registers	16	X

Table A-12 BIM Module

Address	Access	Symbol	Register	Size	Reset
0xYF FA00	S	MCR	Module configuration register. See **Table 3-8** for bit descriptions.	16	X
0xYF FA02	S	MTR	BIM module test register. See **Table 3-8** for bit descriptions.	16	X
0xYF FA04	S	BIMTR/MDR	BIM test register/Module disable register See **Table 3-10** for bit descriptions.	16	X
0xYF FA06	S	—	Reserved.	16	X
0xYF FA08	S	SYNCR	Clock synthesizer control register. See **Table 3-62** for bit descriptions.	16	X
0xYF FA0A	S	SYNST/RSR	Clock synthesizer status/reset status registers. See **Table 3-63** and **Table 3-65** for bit descriptions.	16	X
0xYF FA0C	S	—	Reserved	16	X
0xYF FA0E	T	PCON	Port/clock configuration shadow register. See **Table 3-11** for bit descriptions.	16	X
0xYF FA10	S	PORTA/PORTB	Port A output data / port B output data register. See **Table 3-14** amd **Table 3-16** for bit descriptions.	16	X
0xYF FA12	S	PORTAP/ PORTBP	Port A pin data / port B pin data register. See **Table 3-14** and **Table 3-16** for bit descriptions.	16	X
0xYF FA14	S	DDRAB	Port A/B data direction register. See **Table 3-13** for bit descriptions.	16	X
0xYF FA16	T	—	Reserved	16	X
0xYF FA18	S	PORTC/PORTD	Port C output data / port D output data register. See **Table 3-22** and **Table 3-24** for bit descriptions.	16	X
0xYF FA1A	S	PORTCP/ PORTDP	Port C pin data register / port D pin data register. See **Table 3-23** and **Table 3-28** for bit descriptions.	16	X
0xYF FA1C	S	DDRC/DDRD	Port C data direction / port D data direction register. See **Table 3-21** and **Table 3-26** for bit descriptions.	16	X

Table A-12 BIM Module (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FA1E	T	PCPAR/PDPAR	Port C pin assignment / port D pin assignment register. See Table 3-19 and Table 3-25 for bit descriptions.	16	X
0xYF FA20	S	PORTK/PORTE	Port K output data / port E output data register. See Table 3-53 and Table 3-32 for bit descriptions.	16	X
0xYF FA22	S	PORTKP/ PORTEP	Port K pin data / port E pin data register. See Table 3-54 and Table 3-33 for bit descriptions.	16	X
0xYF FA24	S	DDRK/DDRE	Port K direction / port E direction register. See Table 3-52 and Table 3-31 for bit descriptions.	16	X
0xYF FA26	T	PKPAR/PEPAR	Port K pin assignment / port E pin assignment register. See Table 3-51 and Table 3-30 for bit descriptions.	16	X
0xYF FA28	S	PORTG/PORTH	Port G output data / port H output data register. See Table 3-45 and Table 3-48 for bit descriptions.	16	X
0xYF FA2A	S	PORTGP/ PORTHP	Port G pin data / port H pin data register. See Table 3-46 and Table 3-49 for bit descriptions.	16	X
0xYF FA2C	S	DDRG/DDRH	Port G data direction / port H data direction register. See Table 3-44 and Table 3-47 for bit descriptions.	16	X
0xYF FA2E	S	—	Reserved	16	X
0xYF FA30	S	PORTF	Port F output data. See Table 3-38 for bit descriptions.	16	X
0xYF FA32	S	PORTFP	Port F pin data register. See Table 3-39 for bit descriptions.	16	X
0xYF FA34	S	DDRF	Port F data direction register. See Table 3-37 for bit descriptions.	16	X
0xYF FA36	S	PFPAR	Port F pin assignment register. See Table 3-36 for bit descriptions.	16	X
0xYF FA38	S	PORTFE	Port F edge flags register. See Table 3-40 for bit descriptions.	16	X
0xYF FA3A	S	PFIACK/PFEER	Port F IACK response / port F edge-detect enable register. See Table 3-41 for bit descriptions.	16	X
0xYF FA3C		PFLVR	Port F level register. See Table 3-42 for bit descriptions.		
0xYF FA3E		—	Reserved		
0xYF FA40		MSRA	Test module master shift A register. See Table 3-7 for bit descriptions.		
0xYF FA42		MSRB	Test module master shift B register. See Table 3-7 for bit descriptions.		
0xYF FA44		SCRA	Test module shift count A register. See Table 3-7 for bit descriptions.		
0xYF FA46		REPS	Test module repetition counter register. See Table 3-7 for bit descriptions.		

Table A-12 BIM Module (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FA48		CREG	Test module control register register. See **Table 3-7** for bit descriptions.		
0xYF FA4A		DREG	Test module distributed register. See **Table 3-7** for bit descriptions.		
0xYF FA4C		BCSOR2	Burst chip select option register 2 register. See **Table 3-7** for bit descriptions.		
0xYF FA4E		—	Reserved.		
0xYF FA50		SYPCR	System protect control register. See **Table 3-67** for bit descriptions.		
0xYF FA52		TIC	Timer control register. See **Table 3-68** for bit descriptions.		
0xYF FA53		TIV	Timer interrupt vector register. See **Table 3-69** for bit descriptions.		
0xYF FA54		—	Reserved		
0xYF FA55		SWS	SWDOG service register. See **Table 3-70** for bit descriptions.		
0xYF FA56		PRE	Prescaler (read-only) register. See **Table 3-71** for bit descriptions.		
0xYF FA58		SWI	Software watchdog internal register See **Table 3-72** for bit descriptions.		
0xYF FA5A		RTI	Real-time interval register. See **Table 3-73** for bit descriptions.		
0xYF FA5C		SWIT	Software watchdog interval timer operation register. See **Table 3-74** for bit descriptions.		
0xYF FA5E		RTDC	Real-time downcounter (read-only) register. See **Table 3-7** for bit descriptions.		
0xYF FA5F		RTIT	Real-time interval counter and RTC operation register. See **Table 3-75** for bit descriptions.		
0xYF FA60		CSBAR1	Chip select base address register 1. See **Table 3-80** for bit descriptions.		
0xYF FA62		CSOR1	Asynchronous chip select option register 1. See **Table 3-81** for bit descriptions.		
0xYF FA64		CSBAR2	Chip select base address register 2. See **Table 3-80** for bit descriptions.		
0xYF FA66		CSOR2	Chip select option register 2. See **Table 3-80** for bit descriptions.		
0xYF FA68		CSBAR3	Chip select base address register 3. See **Table 3-80** for bit descriptions.		
0xYF FA6A		CSOR3	Chip select option register 3. See **Table 3-80** for bit descriptions.		
0xYF FA6C		CSBAR4	Chip select base address register 4. See **Table 3-80** for bit descriptions.		
0xYF FA6E		CSOR4	Chip select option register 4. See **Table 3-80** for bit descriptions.		
0xYF FA70		CSBAR5	Chip select base address register 5. See **Table 3-80** for bit descriptions.		
0xYF FA72		CSOR5	Chip select option register 5. See **Table 3-80** for bit descriptions.		
0xYF FA74		CSBAR6	Chip select base address register 6. See **Table 3-80** for bit descriptions.		

Table A-12 BIM Module (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FA76		CSOR6	Chip select option register 6. See **Table 3-80** for bit descriptions.		
0xYF FA78		CSBAR7	Chip select base address register 7. See **Table 3-80** for bit descriptions.		
0xYF FA7A		CSOR7	Asynchronous chip select option register 7. See **Table 3-81** for bit descriptions.		
0xYF FA7C		BCSBAR	Base address register 7. See **Table 3-84** for bit descriptions.		
0xYF FA7E		BCSOR1	Base option register 1. See **Table 3-85** for bit descriptions.		

Table A-13 TouCAN (2) (CAN 2.0B Controller)

Address	Access	Symbol	Register	Size	Reset
0xYF FA80	S	TCNMCR	TouCAN Module Configuration Register. See **Table 10-13** for bit descriptions.	16	X
0xYF FA82	T	TTR	TouCAN Test Register	16	X
0xYF FA84	S	CANICR	TouCAN Interrupt Configuration Register. See **Table 10-14** for bit descriptions.	16	X
0xYF FA86	S	CANCTRL0/ CANCTRL1	TouCAN Control Register 0/ TouCAN Control Register 1. See **Table 10-15** and **Table 10-18** for bit descriptions.	16	X
0xYF FA88	S	PRESDIV/ CANCTRL2	TouCAN Control and Prescaler Divider Register/TouCAN Control Register 2. See **Table 10-19** and **Table 10-20** for bit descriptions.	16	X
0xYF FA8A	S	TIMER	TouCAN Free-Running Timer Register. See **Table 10-21** for bit descriptions.	16	X
0xYF FA90	S	RXGMASKHI	TouCAN Receive Global Mask High. See **Table 10-22** for bit descriptions.	16	X
0xYF FA92	S	RXGMASKLO	TouCAN Receive Global Mask Low. See **Table 10-22** for bit descriptions.	16	X
0xYF FA94	S	RX14MASKHI	TouCAN Receive Buffer 14 Mask High.	16	X
0xYF FA96	S	RX14MASKLO	TouCAN Receive Buffer 14 Mask Low.	16	X
0xYF FA98	S	RX15MASKHI	TouCAN Receive Buffer 15 Mask High.	16	X
0xYF FA9A	S	RX15MASKLO	TouCAN Receive Buffer 15 Mask Low.	16	X
0xYF FAA0	S	ESTAT	TouCAN Error and Status Register. See **Table 10-23** for bit descriptions.	16	X
0xYF FAA2	S	IMASK	TouCAN Interrupt Masks. See **Table 10-26** for bit descriptions.	16	X
0xYF FAA4	S	IFLAG	TouCAN Interrupt Flags. See **Table 10-27** for bit descriptions.	16	X
0xYF FAA6	S	RXECTR/ TXECTR	TouCAN Receive Error Counter/ TouCAN Transmit Error Counter. See **Table 10-28** for bit descriptions.	16	X

Table A-14 SRAM Modules (2)
(Static Random Access Memory)

SRAM(E)					
0xYF FB00	S	RAMMCR	SRAM4 Module Configuration Register. See **Table 12-1** for bit descriptions.	16	X
0xYF FB02	T	RAMTST	SRAM4 test register.	16	X
0xYF FB04	S	RAMBAH	SRAM4 base address high register. See **Table 12-3** for bit descriptions.	16	X
0xYF FB06	S	RAMBAL	SRAM4 base address low register. See **Table 12-3** for bit descriptions.	16	X

Table A-15 QSM_A (Queued Serial Module A)

0xYF FC00	S	QSMCR_A	QSM Module Configuration Register. See **Table 7-7** for bit descriptions.	16	X
0xYF FC02	T	QTEST_A	QSM Test Register.	16	X
0xYF FC04	S	QILR/QIVR_A	QSM Interrupt Level/interrupt Vector Register. See **Table 7-8** and **Table 7-9** for bit descriptions.	16	X
0xYF FC06	S	—	Reserved	—	X
0xYF FC08	S	SCCR0_A	SCI1 Control Register 0. See **Table 7-22** for bit descriptions.	16	X
0xYF FC0A	S	SCCR1_A	SCI1Control Register 1. See **Table 7-24** for bit descriptions.	16	X
0xYF FC0C	S	SCSR_A	SCI1 Status Register. See **Table 7-26** for bit descriptions.	16	X
0xYF FC0E	S	SCDR_A	SCI1 Data Register. See **Table 7-27** for bit descriptions.	16	X
0xYF FC10 – 0xYF FC12	S	—	Reserved	—	X
0xYF FC14	S	PORTQS_A	QSMCM Port QS Data Register. See **7.2.3.1 QSM Port Data Register (PORTQS)** for bit descriptions.	16	X
0xYF FC16	S	PQSPAR_A / DDRQST_A	QSMCM Port QS Pin Assignment Register/ QSMCM Port QS Data Direction Register. See **Table 7-11** and **Table 7-12** for bit descriptions.	16	X
0xYF FC18	S	SPCR0_A	QSPI Control Register 0. See **Table 7-14** for bit descriptions.	16	X
0xYF FC1A	S	SPCR1_A	QSPI Control Register 1. See **Table 7-16** for bit descriptions.	16	X
0xYF FC1C	S	SPCR2_A	QSPI Control Register 2. See **Table 7-17** for bit descriptions.	16	X
0xYF FC1E	S	SPCR3_A / SPSR_A	QSPI Control Register 3/QSPI Status Register. See **Table 7-18** and **Table 7-19** for bit descriptions.	16	X
0xYF FC20 — 0xYF FDFF	S	—	Reserved	16	X
0xYF FD00 — 0xYF FD1F	S	SCRQ_A	QSPI Receive Queue Locations. See **7.4.4 Receiver Operation** for bit descriptions.	16	X

Table A-15 QSM_A (Queued Serial Module A)

0xYF FD20 — 0xYF FD3F	S	SCTQ_A	QSPI Transmit Queue Locations. See **7.4.3 Transmitter Operation** for bit descriptions.	16	X
0xYF FD40 — 0xYF FD4F	S	QSPIRAM_A	QSPI Transmit Queue Locations. See **Table 7-20** for bit descriptions.	16	X

Table A-16 TPU3_A (Time Processor Unit)

0xYF FE00	S	TPUMCR_A	TPU3 module configuration register.	16	X
0xYF FE02	T	TCR_A	TPU3 test configuration register	16	X
0xYF FE04	S	DSCR_A	Development support control register.	16	X
0xYF FE06	S	DSSR_A	Development support status register.	16	X
0xYF FE08	S	TICR_A	TPU3 interrupt configuration register.	16	X
0xYF FE0A	S	CIER_A	Channel interrupt enable register.	16	X
0xYF FE0C	S	CFSR0_A	Channel function selection register 0.	16	X
0xYF FE0E	S	CFSR1_A	Channel function selection register 1.	16	X
0xYF FE10	S	CFSR2_A	Channel function selection register 2.	16	X
0xYF FE12	S	CFSR3_A	Channel function selection register 3.	16	X
0xYF FE14	S	HSQR0_A	Host sequence register 0.	16	X
0xYF FE16	S	HSQR1_A	Host sequence register 1.	16	X
0xYF FE18	S	HSRR0_A	Host service request register 0.	16	X
0xYF FE1A	S	HSRR1_A	Host service request register 1.	16	X
0xYF FE1C	S	CPR0_A	Channel priority register 0.	16	X
0xYF FE1E	S	CPR1_A	Channel priority register 1.	16	X
0xYF FE20	S	CISR_A	Channel interrupt status register.	16	X
0xYF FE22	T	LR_A	Link register	16	X
0xYF FE24	T	SGLR_A	Service grant latch register	16	X
0xYF FE26	T	DCNR_A	Decoded channel number register	16	X
0xYF FE28	S	TPUMCR2_A	TPU module configuration register 2.	16	X
0xYF FE2A	S	TPUMCR3_A	TPU module configuration 3.	16	X
0xYF FE2C	T	ISDR_A	Internal scan data register	16	X
0xYF FE2E	T	ISCR_A	Internal scan control register	16	X
0xYF FF00 – 0xYF FF0F	S	—	Channel 0 parameter registers	16	X
0xYF FF10 – 0xYF FF1F	S	—	Channel 1 parameter registers	16	X
0xYF FF20 – 0xYF FF2F	S	—	Channel 2 parameter registers	16	X
0xYF FF30 – 0xYF FF3F	S	—	Channel 3 parameter registers	16	X
0xYF FF40 – 0xYF FF4F	S	—	Channel 4 parameter registers	16	X
0xYF FF50 – 0xYF FF5F	S	—	Channel 5 Parameter Registers	16	X
0xYF FF60 – 0xYF FF6F	S	—	Channel 6 parameter registers	16	X
0xYF FF70 – 0xYF FF7F	S	—	Channel 7 parameter registers	16	X
0xYF FF80 – 0xYF FF8F	S	—	Channel 8 parameter registers	16	X

Table A-16 TPU3_A (Time Processor Unit) (Continued)

0xYF FF90 – 0xYF FF9F	S	—	Channel 9 parameter registers	16	X
0xYF FFA0 – 0xYF FFAF	S	—	Channel 10 parameter registers	16	X
0xYF FFB0 – 0xYF FFBF	S	—	Channel 11 parameter registers	16	X
0xYF FFC0 – 0xYF FFCF	S	—	Channel 12 parameter registers	16	X
0xYF FFD0 – 0xYF FFDF	S	—	Channel 13 parameter registers	16	X
0xYF FFE0 – 0xYF FFEF	S	—	Channel 14 parameter registers	16	X
0xYF FFF0 – 0xYF FFFF	S	—	Channel 15 parameter registers	16	X