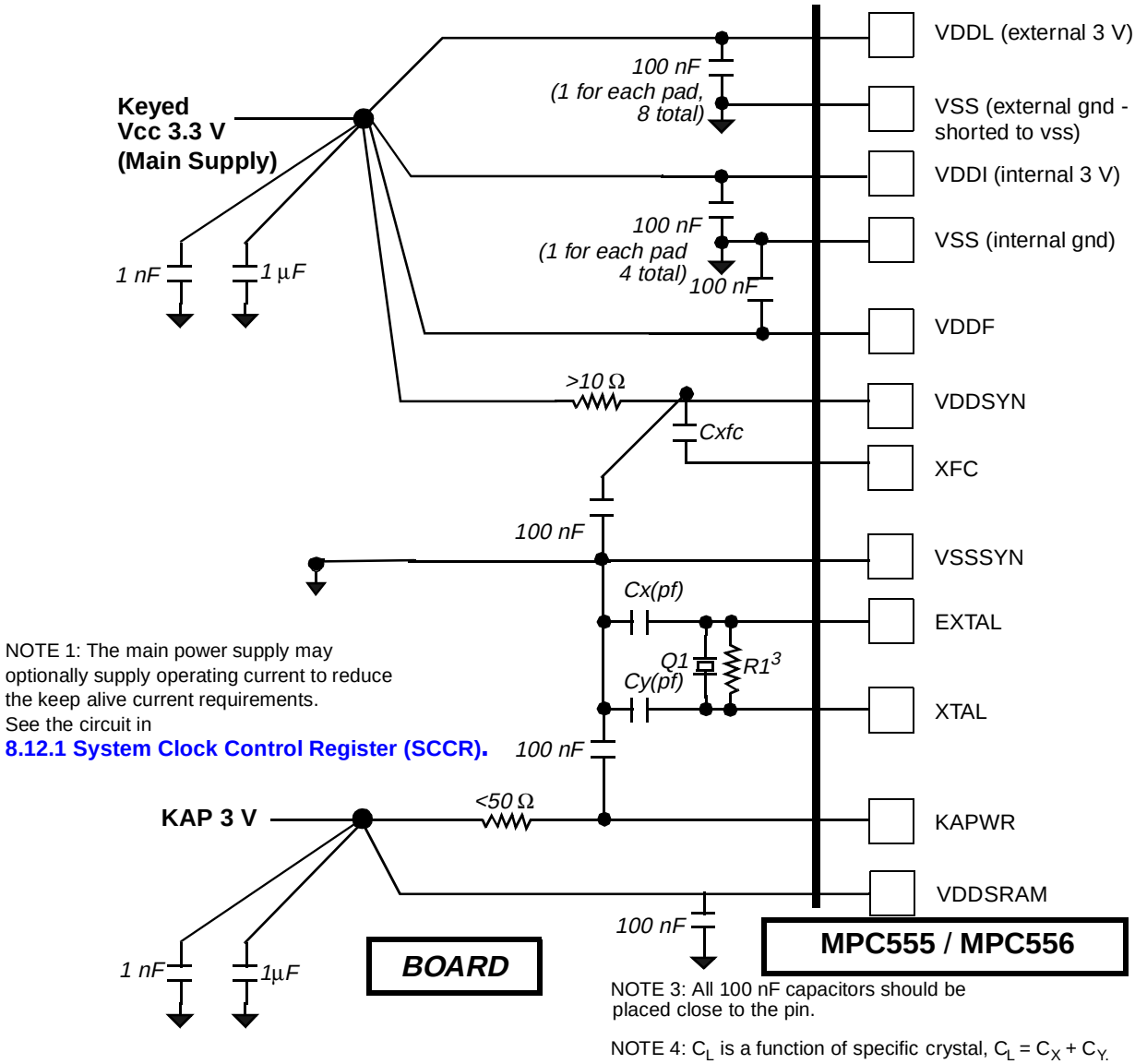
APPENDIX E
CLOCK AND BOARD GUIDELINES

E.1 INTRODUCTION

The MPC555 / MPC556 built-in PLL, oscillator, and other analog and sensitive circuits, require that the board design follow special layout guidelines to ensure proper operation of the chip clocks. This appendix describes how the clock supplies and external components should be connected in the board. These guidelines must be fulfilled to reduce switching noise which is generated on internal and external buses during operation. Any noise injected into the sensitive clock and PLL logic reduces clock performance. The USIU maintains a PLL loss-of-lock warning indication that can be used to determine the clock stability in the MPC555 / MPC556.

E.2 MPC555 / MPC556 Family Power Distribution



NOTE 1: The main power supply may optionally supply operating current to reduce the keep alive current requirements. See the circuit in **8.12.1 System Clock Control Register (SCCR).**

NOTE 2: Resistor R_1 is currently not required. Space should be left on the board to add it in the future if necessary.

NOTE 3: All 100 nF capacitors should be placed close to the pin.

NOTE 4: C_L is a function of specific crystal, $C_L = C_X + C_Y$.

Figure E-1 MPC555 / MPC556 Family Power Distribution Diagram — 3 V

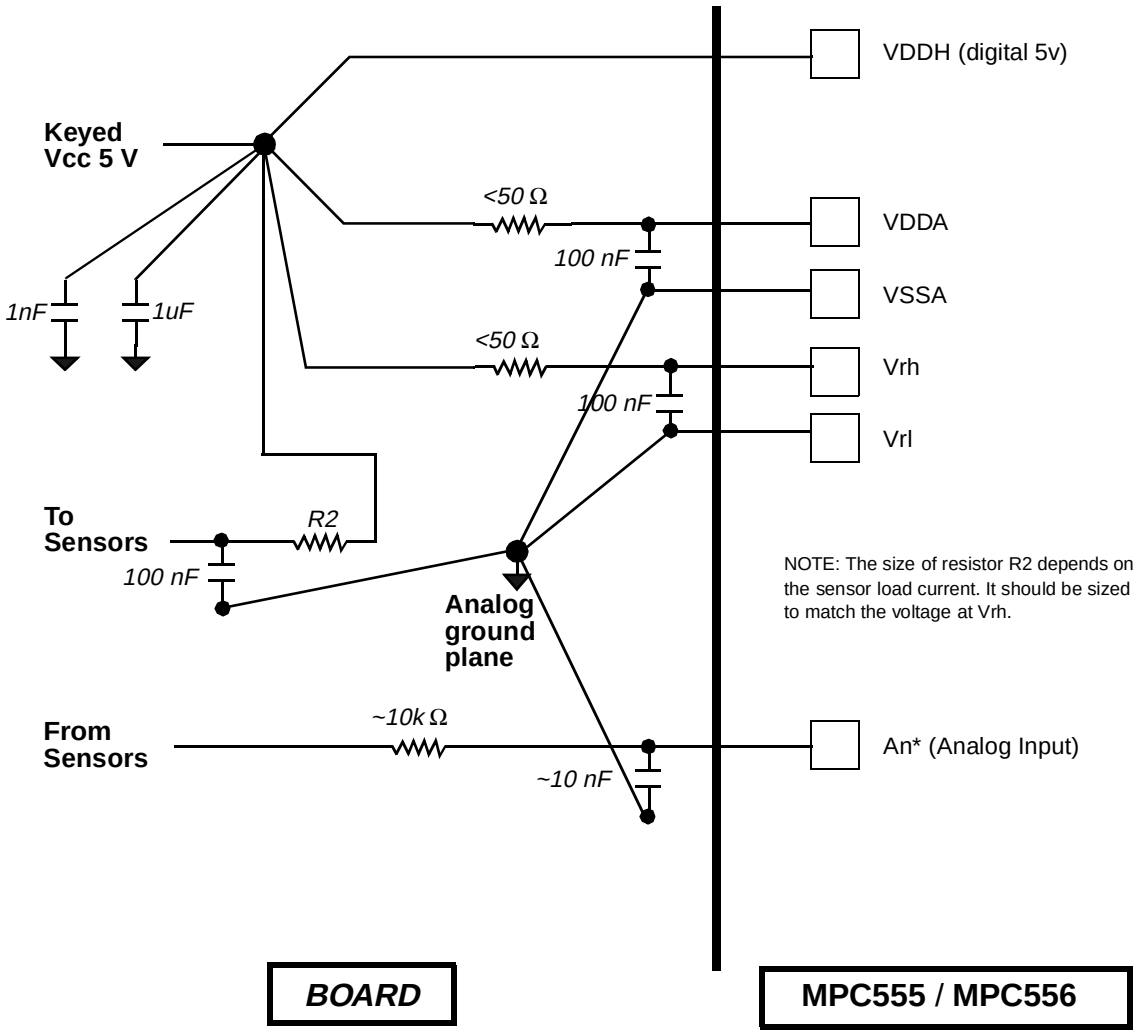


Figure E-2 MPC555 / MPC556 Family Power Distribution Diagram — 5 V and Analog

E.3 PLL and Crystal Oscillator External Components

E.3.1 Crystal Oscillator External Components

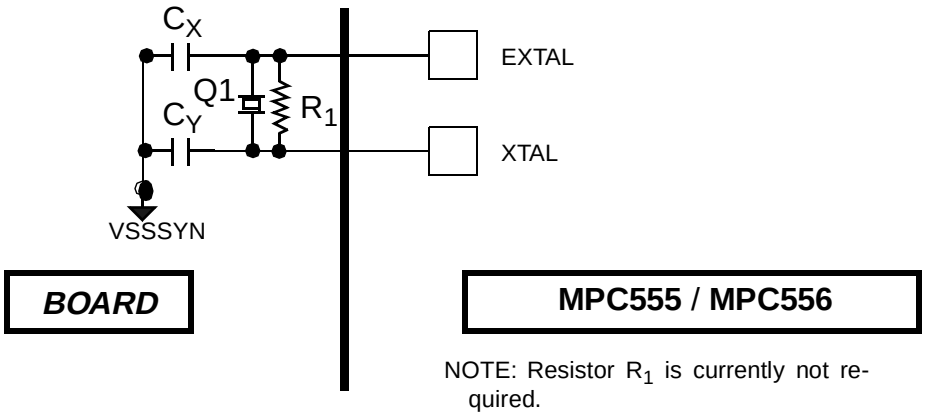


Figure E-3 Crystal Oscillator Circuit

Table E-1 External Components Value For Different Crystals (Q1)

Component	NDK CP32C 20 MHz	KINSEKI CX-11F 20 MHz	MURATA CCSTC 4 MHz	Units
C_L[1]	6	14	—	pF
R_1[3]	1MEG[3]	1MEG[3]	1MEG[3]	Ohm
C_X	6	16	—[2]	pF
C_Y	6	16	—	pF

NOTES:
1. C_L according to crystal specification, $C_L = C_X + C_Y$.
2. The Murata ceramic resonator includes the load capacitors. (8pF should be selected)
3. Resistor R_1 is currently not required. Space should be left on the board to add it in the future if necessary.

Load capacitances specified in the table include all stray capacitance.

Tolerance of the capacitors are ±10%.

The oscillator capacitors were calculated as follows:

$$C_{XX} = C_{YY} = 2C_L$$

$$C_{XX} = C_X + C_{pad} + C_{socket}$$

$$C_{YY} = C_Y + C_{pad} + C_{socket}$$

Where C_X is “real” capacitor

C_{pad} is pad capacitance

C_{socket} is socket and trace capacitance

C_L is load capacitance

Capacitance of the socket $C \leq 1pF$

Capacitance of the board trace $C \leq 1pF$. It should be low since the crystal must be located very close to the chip.

Capacitance of the MPC555 / MPC556 XTAL pin is $C_{pad} \sim 7pF$

Capacitance of the MPC555 / MPC556 EXTAL pin i $C_{pad} \sim 7pF$ s

Tolerance of the capacitors taken into account is ±10%

E.3.2 KAPWR Filtering

KAPWR pin is the MPC555 / MPC556 keep-alive power. KAPWR is used for the crystal oscillator circuit, and should be isolated from the noisy supplies. It is recommended that an RC filter be used on KAPWR, or bypass capacitors which are located as close as possible to the part.

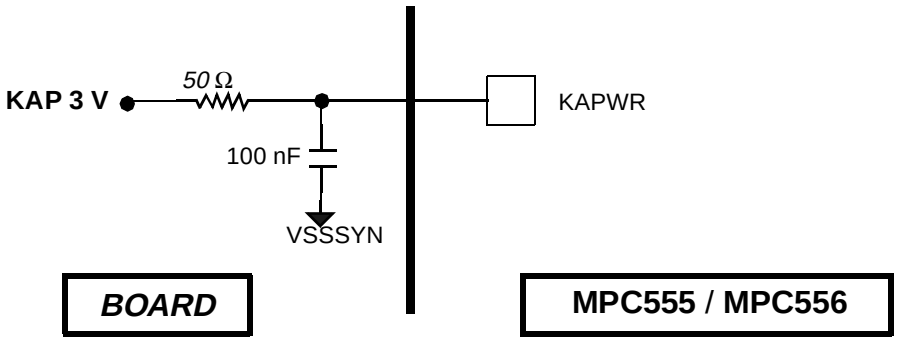


Figure E-4 RC Filter Example

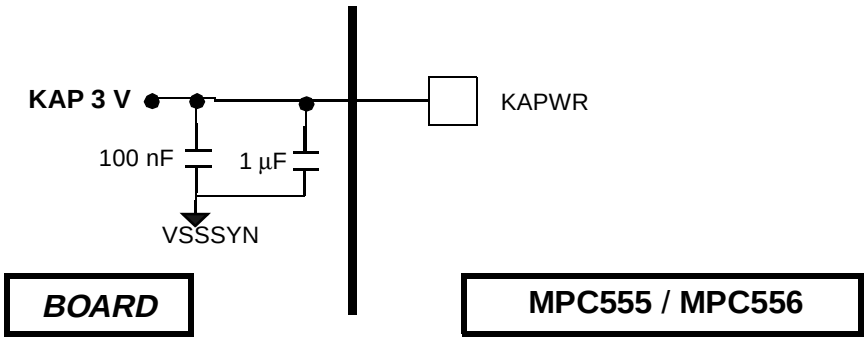


Figure E-5 Bypass Capacitors Example (Alternative)

E.3.3 PLL External Components

VDDSYN and VSSSYN are the PLL dedicated power supplies. These supplies must be used only for the PLL and isolated from all other noisy signals in the board. VDDSYN could be isolated with RC filter (see **Figure E-1**), or LC filter. The maximum noise allowed on VDDSYN, and VSSSYN is 50 mV with typical cut-off frequency of 500 Hz.

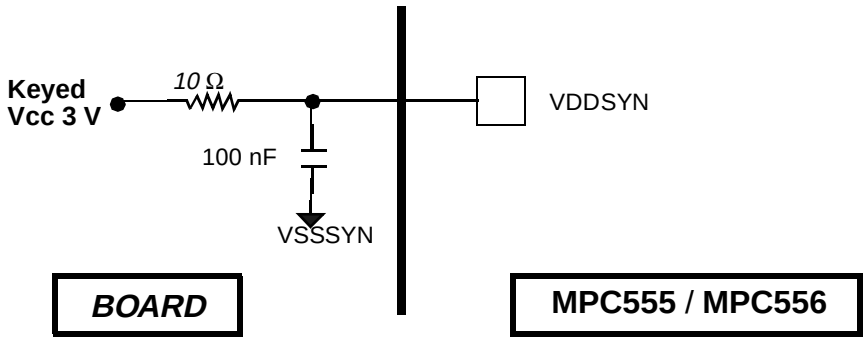


Figure E-6 RC Filter Example

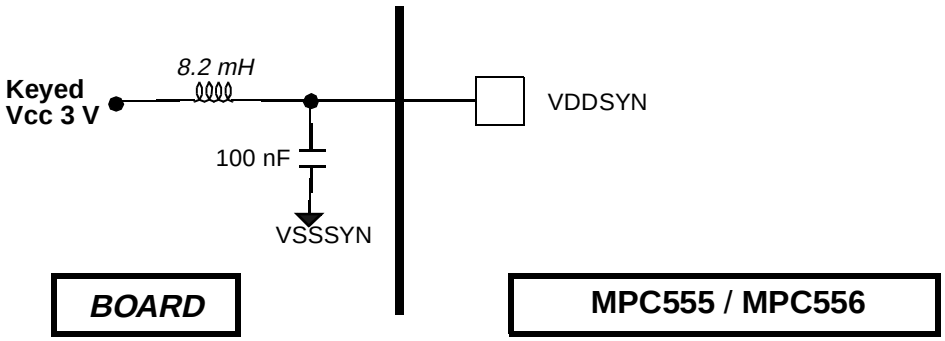


Figure E-7 LC Filter Example (Alternative)

E.3.4 PLL Off-Chip Capacitor C_{XFC}

C_{XFC} is the PLL feedback capacitor. It must be located as close as possible to the XFC, and VDDSYN pads. The maximum noise allowed on XFC is 50 mV peak to peak with typical cut-off frequency of 500 Hz.

The required values for C_{XFC} are:

$$0 < (MF + 1) < 4(680 \times (MF + 1) - 120)pF$$

$$(MF + 1) \geq 4\ 1100 \times (MF + 1)pF$$

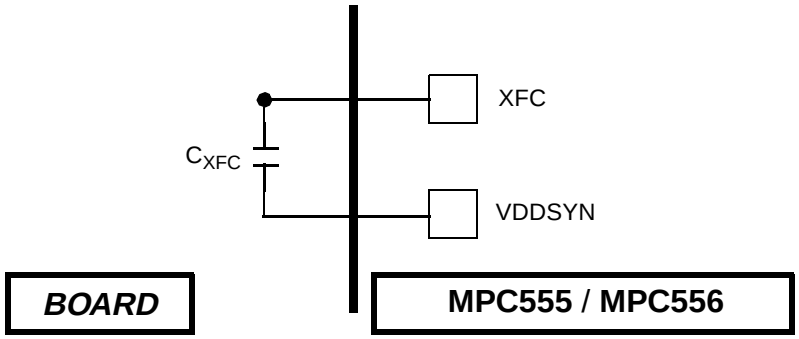


Figure E-8 PLL Off-Chip Capacitor Example

E.4 Clock Oscillator and PLL External Components Layout Requirements

E.4.1 Traces and Placement

Traces connecting capacitors, crystal, resistor should be as short as possible. Therefore, the components (crystal, resistor and capacitors) should be placed as close to the oscillator pins of the MPC555 / MPC556 as possible.

The voltage to the VDDSYN pin should be well regulated and the pin should be provided with an extremely low impedance path from the VDDSYN filter to the VDDSYN pad.

The VSSSYN pin should be provided with an extremely low impedance path in the board. All the filters for the supplies should be located as close as possible to the chip package. It is recommended to design individual VSSSYN plane to improve VSSSYN quietness.

E.4.2 Grounding/Guarding

The traces from the oscillator pins and PLL pins of the MPC555 / MPC556 should be guarded from all other traces to reduce crosstalk. It can be provided by keeping other traces away from the oscillator circuit and placing a ground plane around the components and traces.