APPENDIX G
ELECTRICAL CHARACTERISTICS

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing characteristics of the MPC555 / MPC556. The MPC555 / MPC556 is designed to operate at 40 MHz with nominal 3.3-V and 5.0-V power supplies.

G.1 Absolute Maximum Ratings (V_{SS} = 0 V)

Table G-1 Absolute Maximum Ratings

Rating	Symbol	Min. Value	Max. Value	Unit
3-V Supply Voltage[1],[2]	V_{DDL}/V_{DDI}	-6.0	4.0	V
Flash Supply Voltages[3]	V_{PP}	-6.0	6.0	V
Flash Core Voltage[1]	V_{DDF}	-6.0	4.0	V
Oscillator, Keep Alive Reg. Supply Voltage[1]	KAPWR	-6.0	4.0	V
SRAM Supply Voltage[1]	V_{DDSRAM}	-6.0	4.0	V
Clock Synthesizer Supply Voltage[1]	V_{DDSYN}	-6.0	4.0	V
QADC Supply Voltage[4]	V_{DDA}	-6.0	6.0	V
5-V Supply Voltage	V_{DDH}	-0.3	6.0	V
DC Input Voltages[5]	V_{IN}	V_{SS} -0.3	V_{DDH} +0.3	V
Reference Supply V_{RH}, with Reference to V_{RL}	$V_{RH} - V_{RL}$	-0.3	6.0	V
V_{SS} Differential Voltage	$V_{SS} - V_{SSA}$	-0.1	0.1	V
V_{DD} Differential Voltage[6]	$V_{DDL} - V_{DDA}$	-6.0	4.0	V
V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	-6.0	0.3	V
Maximum Input Current per pin [7, 8, 9]	I_{MA}	-25	25	mA
QADC Maximum Input Current per Pin	I_{max}	-25	25	mA
Operating Temperature Range (Packaged)	T_A	-40 (T_L)	+125 (T_H)	°C
Operating Temperature Range (Die Form) (Maximum junction temperature for packaged devices)	T_J	-40	+150	°C
Storage Temperature Range	T_{STG}	-55	+155	°C
Maximum Solder Temperature[10]	T_{sdr}		220	°C
Moisture Sensitivity Level[11]	MSL		3	

NOTES:

1. For internal digital supply of V_{DDL} = 3.3 V typical.
2. V_{DDL} and V_{DDI} should always be connected to the same potential with no differential voltage.

3. During program/erase operation the value of V_{PP} must be 5.0 V ± 5%.
4. V_{DDA} = 5.0 V ±10%.
5. All 3-V input pins are 5-V tolerant. This applies to all input pins.
6. Refers to allowed random sequencing of power supplies.
7. Maximum continuous current on I/O pins provided the overall power dissipation is below the power dissipation of the package. Proper operation is not guaranteed at this condition.
8. Condition applies to one pin at a time.
9. Transitions within the limit do not affect device reliability or cause permanent damage. Exceeding limit may cause permanent conversion error on stressed channels and on unstressed channels.
10. Solder profile per CDF-AEC-Q100, current revision.
11. Moisture sensitivity per JEDEC test method A112.

Functional operating conditions are given in **G.7 DC Electrical Characteristics**. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

G.2 Target Failure Rate

Target failure rate of **TBD** ppm pending characterization and evaluation of qualifiable silicon.

G.3 Package

The MPC555 / MPC556 is available in two forms, packaged and die. The package is a 272-ball PBGA, Motorola case outline 1135A-01 (See **Figure 2-1** of the MPC555 User's Manual for a case drawing or contact Motorola.) For die characteristics, contact the Motorola factory.

G.4 EMI Characteristics

G.4.1 Reference Documents

The documents referenced for the EMC testing of MPC555 / MPC556 are listed below.

1. SAE J1752/3 Issued 1995-03
2. VDE UK 767.14/ZVEI-Ad-Hoc-HL-AK Version1.0 May 1994

G.4.2 Definitions and Acronyms

EMC — Electromagnetic compatibility

EMI — Electromagnetic interference

TEM cell — Transverse electromagnetic mode cell

G.4.3 Testing Characteristics

1. Scan range: 150 kHz — 1000 MHz
2. Operating frequency: 20 MHz, 40 MHz
3. Operating voltages: 3.3 V, 5.0 V
4. Max spikes: 50 dBuV
5. I/O port waveforms: 50% duty cycle @ 100 µs period
6. Temperature: 25°C (-40°C, 125°C if available)

G.5 Thermal Characteristics

Table G-2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
BGA Package Thermal Resistance, Junction to Ambient — Natural Convection	$R_{\theta JA}$	42.8[1,2]	°C/W
BGA Package Thermal Resistance, Junction to Ambient — Four layer (2s2p) board, natural convection	$R_{\theta MA}$	30.4[3,4]	°C/W
BGA Package Thermal Resistance, Junction to Board	$R_{\theta JB}$	19.9[5]	°C/W
BGA Package Thermal Resistance, Junction to Case (top)	$R_{\theta JC}$	6.3[6]	°C/W
BGA Package Thermal Resistance, Junction to Package Top, Natural Convection	θ_{JT}	2.7[7]	°C/W

NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the board thermal resistance.
2. Per SEMI G38-87 and JESD51-2 with the board horizontal.
3. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the board thermal resistance.
4. Per JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed circuit board (Four layer [2s2p] board, natural convection).
6. Indicates the thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction to ambient resistance (°C/W)

P_D = power dissipation in package

The junction to ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. Unfortunately, the answer is only an estimate; test cases have demonstrated that errors of a factor of two are possible. As a result, more detailed thermal characterization is supplied.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta JA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

The simplest thermal model of a package which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction to board and a junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board. temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_B = board temperature (°C)

$R_{\theta JB}$ = package junction to board resistance (°C/W)

P_D = power dissipation in package (W)

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction to board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation. Consultation on the creation of the complex model is available.

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JA} \times P_D)$$

where:

T_T = thermocouple temperature on top of package (°C)

$R_{\theta JA}$ = thermal characterization parameter

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 characteristic published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

G.5.1 Thermal References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) characteristics are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC characteristics are available on the WEB at: **http://www.jedec.org**

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

G.6 ESD Protection

Table G-3 ESD Protection

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ω
	C	100	pF
ESD Target for Machine Model (MM)		200	V
MM Circuit Description	R1	0	Ω
	C	200	pF
Number of Pulses Per Pin Positive Pulses (MM) Negative Pulses (MM) Positive Pulses (HBM) Negative Pulses (HBM)	—	 3 3 1 1	—
Interval of Pulses	—	1	Second

Notes:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device characteristic requirements. Complete DC parametric and functional testing shall be performed per applicable device characteristic at room temperature followed by hot temperature, unless specified otherwise in the device characteristic.

G.7 DC Electrical Characteristics

Table G-4 DC Electrical Characteristics

(V_{DDL} = 3.3 V ± 0.3 V, V_{DDH} = 5.0 V ± 0.5 V, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
3-V only Input High Voltage[1] Except EXTAL and EXTCLK	V_{IH3}	2.0	V_{DDH} +0.3	V
3-V Input High Voltage EXTCLK	V_{IHC}	2.4	V_{DDH} +0.3	V
5-V Input Only High Voltage [2]	V_{IH5}	0.7*V_{DDH}	V_{DDH} +0.3	V
5-V Input High Voltage (QADC PQA, PQB)	V_{IHA5}	0.7*V_{DDA}	V_{DDA} +0.3	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr. (Port A), Data (Port D), and Control (Port C)) 3-V Input High Voltage Addr. (Port A), Data (Port D), Control (Port C) 5-V Input High Voltage (GPIO)	V_{IH3M} V_{IH5M}	2.0 0.7*V_{DDH}	V_{DDH} +0.3 V_{DDH} +0.3	V
3-V Input Low Voltage Except EXTCLK	V_{IL3}	V_{SS} -0.3	0.8	V
3-V Input Low Voltage EXTCLK	V_{IL3C}	V_{SS} -0.3	0.4	V
5-V Input Low Voltage	V_{IL5}	V_{SS} -0.3	0.4*V_{DDH}	V
5-V Input Low Voltage (QADC PQA, PQB)	V_{ILA5}	V_{SSA} -0.3	0.4*V_{DDA}	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr. (Port A), Data (Port D), and Control (Port C)) 3-V Input Low Voltage (Addr. (Port A), Data (Port D), Control (Port C)) 5-V Input Low Voltage (GPIO)	V_{IL3M} V_{IL5M}	V_{SS} -0.3 V_{SS} -0.3	0.8 0.4*V_{DDH}	V V
QADC Analog Input Voltage[3]	V_{INDC}	V_{SSA} -0.3	V_{DDA} +0.3	V
3-V Mode Select Current Pull-up @ 0 V to V_{IL3}, Pull-down @ V_{IH3} to V_{DDL}	$I_{act3\ V}$	20	130	µA
5-V Mode Select Current Pull-up @ 0 to V_{IL5}, Pull-down @ V_{IH5} to V_{DDH}	$I_{act5\ V}$	20	130	µA
3-V Input Leakage Current Pull-up/down Inactive	$I_{inact3\ V}$	—	1.0	µA
5-V Input Leakage Current Pull-up/down Inactive	$I_{inact5\ V}$	—	1.0	µA
QADC64 Input Current, Channel Off [4] PQA PQB	I_{OFF}	 -200 -150	 200 150	nA

Table G-4 DC Electrical Characteristics (Continued)

(V_{DDL} = 3.3 V ± 0.3 V, V_{DDH} = 5.0 V ± 0.5 V, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
3-V Output High Voltage $V_{DD} = V_{DDL}$ (I_{OH} = -2 mA)	V_{OH3}	2.4	—	V
5-V Output High Voltage $V_{DD} = V_{DDH}$ (I_{OH} = -2 mA) All 5-V Only Outputs Except TPU.	V_{OH5}	V_{DDH} -0.7	—	V
5-V Output High Voltage $V_{DD} = V_{DDH}$ (I_{OH} = -5 mA) For TPU Pins Only	V_{OHTP5}	V_{DDH} -0.65	—	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr. (Port A), Data (Port D), and Control (Port C)) 3-V Output High Voltage (I_{OH} = -2 mA) 5-V Output High Voltage (I_{OH} = -2 mA)	V_{OH3M} V_{OH5M}	2.4 V_{DDH} -0.7	—	V
3-V Output Low voltage $V_{DD} = V_{DDL}$ (I_{OL} = 3.2 mA)	V_{OL3}	—	0.5	V
5-V Output Low Voltage $V_{DD} = V_{DDH}$ (I_{OL} = 2 mA) All 5-V Only Outputs Except TPU.	V_{OL5}	—	0.45	V
5-V Output Low Voltage $V_{DD} = V_{DDH}$ For TPU Pins Only IOL = 10 mA IOL = 2 mA	V_{OLTP5}	—	 1.0 0.45	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr. (Port A), Data (Port D), and Control (Port C)) 3-V Output Low Voltage (I_{OL} = 3.2 mA) 5-V Output Low Voltage (I_{OL} = 2 mA)	V_{OL3M} V_{OL5M}	—	0.5 0.45	V
Output Low Current CLKOUT @ V_{OL} = 0.5 V	I_{OL}	2.0	—	mA
Output High Current CLKOUT @ V_{OH} = 2.4 V	I_{OH}	2.0	—	mA
CLKOUT Capacitance (@ 40 MHz) COM[1:0] of SCCR = 0b01 COM[1:0] of SCCR = 0b00	C_{clk}	—	 30[5] 90	pF
ENGCLK Capacitance@20Mhz EECLK[1:0] of SCCR = 0b01 EECLK[1:0] of SCCR = 0b00	C_{eng}	—	 25[5] 50[6]	pF
Capacitance for Input, Output, and Bidirectional V_{in} = 0 V, f = 1 MHz (except QADC)	C_{in}	—	7	pF
Load Capacitance for Bus Pins Only[7] COM[1:0] of SCCR = 0bX1 COM[1:0] of SCCR = 0bX0	C_L	—	 25 50	pF
QADC Total Input Capacitance PQA Not Sampling PQB Not Sampling Incremental Capacitance Added During Sampling	C_{IN}	 — — —	 15 10 5	pF
Hysteresis (Only IRQ, TPU, MIOS, GPIO, QADC [Digital Inputs] and $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)[8]	V_H	0.5	—	V

Table G-4 DC Electrical Characteristics (Continued)

(V_{DDL} = 3.3 V ± 0.3 V, V_{DDH} = 5.0 V ± 0.5 V, T_A = T_L to T_H)

Characteristic	Symbol	Min	Max	Unit
Operating Current (3-V Supplies) @ 33 MHz Expanded V_{DDL} / V_{DDI} KAPWR V_{DDSRAM} V_{DDSYN} (Crystal Frequency: 20 Mhz) V_{DDF}[9] Single Chip V_{DDL} / V_{DDI} KAPWR V_{DDSRAM} V_{DDSYN} (Crystal Frequency: 20 Mhz) V_{DDF}[9]	 I_{DDL} I_{DDKAP} I_{DDSRM} I_{DDSYN} I_{DDF} I_{DDL} I_{DDKAP} I_{DDSRM} I_{DDSYN} I_{DDF}		 206 6.6 1.7 1.7 8.3 206 6.6 1.7 1.7 8.3	mA
Operating Current (5-V Supplies)@ 33 MHz V_{DDH} V_{DDA} V_{PP}[10]	 I_{DDH5} I_{DDA} I_{DDPP}		 16.5 5 30	mA
Operating Current (3-V Supplies)@ 40 MHz[11] Expanded V_{DDL} / V_{DDI} KAPWR V_{DDSRAM} V_{DDSYN} (Crystal Frequency: 20 Mhz) V_{DDF}[9] Single Chip V_{DDL} / V_{DDI} KAPWR V_{DDSRAM} V_{DDSYN} (Crystal Frequency: 20 Mhz) V_{DDF}[9]	 I_{DDL} I_{DDKAP} I_{DDSRM} I_{DDSYN} I_{DDF} I_{DDL} I_{DDKAP} I_{DDSRM} I_{DDSYN} I_{DDF}		 250 8.0 2.0 2.0 10 250 8.0 2.0 2 10	mA
Operating Current (5-V Supplies)@ 40 MHz V_{DDH} V_{DDA}[12] V_{PP}[10]	 I_{DDH5} I_{DDA} I_{DDVPP}		 20 5.0 30	mA
QADC64 Low Power Stop Mode (V_{DDA})	I_{DDA}		10	µA
Low Power Current @ 40 MHz (VDDI) DOZE, Active PLL and Active Clocks SLEEP, Active PLL with Clocks off DEEP SLEEP[13] PLL and Clocks off	 I_{DDDZ} I_{DDSLP} $I_{DDDPSLP}$		 100 10 4	 mA mA mA
V_{DDL}, V_{DDI}, V_{DDF} Operating Voltage	V_{DDL}, V_{DDI}, V_{DDF}	3.0	3.6	V
V_{PP} Flash Operating Voltage	V_{PP}	V_{DDF} -0.35 V	5.50	V

Table G-4 DC Electrical Characteristics (Continued)

(V_{DDL} = 3.3 V ± 0.3 V, V_{DDH} = 5.0 V ± 0.5 V, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
V_{PP} Flash Programming Voltage	V_{PP}	4.75	5.25	V
Oscillator, Keep Alive Registers Operating Voltage during normal operation (V_{DDL} powered-up)[13,14]	KAPWR	V_{DDL} -0.2	V_{DDL} +0.2	V
Oscillator, Keep Alive Registers Operating Voltage during powered-down operation	KAPWR	3.0	3.6	V
SRAM Operating Voltage during normal operation (V_{DDL} powered-up)[14]	V_{DDSRAM}	V_{DDL} -0.2	V_{DDL} + 0.2	V
V_{DDH} Operating Voltage	V_{DDH}	4.5	5.5	V
QADC Operating Voltage	V_{DDA}	4.5	5.5	V
Clock Synthesizer Operating Voltage[13]	V_{DDSYN}	V_{DDL} -0.2	V_{DDL} +0.2	V
V_{SS} Differential Voltage	$V_{SS} - V_{SSA}$	-100	100	mV
QADC64 Reference Voltage Low[15]	V_{RL}	V_{SSA}	V_{SSA} +0.1	V
QADC64 Reference Voltage High[16]	V_{RH}	V_{DDA} -0.3	V_{DDA}	V
QADC64 V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	4.5	5.5	V
QADC64 Reference Supply Current, DC QADC64 Reference Supply Current, Transient Measured on V_{RH}	I_{REF} I_{REF}	— —	500 4.0	µA mA
Standby Supply Current KAPWR Only V_{DDSRAM} Only (RAM Standby Current) @ T_J = 90°C V_{DDSRAM} Only (RAM Standby Current) @ T_J = 90°C with Low Voltage Protection Circuitry V_{DDSRAM} Only (RAM Standby Current) @ T_J = 150°C			 4 100 150 250	 mA µA µA µA
RAM Standby Voltage for Data Retention (Powered-down Mode) Specified V_{DD} Applied ($V_{DD} = V_{SS}$)	V_{DDSRAM}	1.4[17]	3.6	V
DC Injection Current per Pin GPIO, TPU, MIOS, QSM, EPEE and 5 V [18,19]	I_{IC5}	-1.0	1.0	mA
DC Injection Current Per Pin 3 V [18, 19]	I_{IC3}	-1.0	1.0	mA
QADC64 Disruptive Input Current [18, 20]	I_{NA}	-3	3	mA
Power Dissipation -40 MHz 33 MHz	PD		1 0.8	W

NOTES:

1. This spec is for 3-V output and 5-V input friendly pins.
2. This spec is for 5-V output and 5-V input pins.
3. Within this range, no significant injection will be seen. See QADC64 disruptive input current (I_{NA}).
4. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 – 12°C, in the ambient temperature range of 50 – 125°C.
5. 45 pF maximum for mask sets prior to K62N

6. 90 pF maximum for mask sets prior to K62N
7. All bus pins support two drive strengths capabilities, 25 pF and 50 pF. Current drive is less at the 25-pF capacitive load. Both modes achieve 40-MHz timing.
8. Only IRQ, TPU, MIOS, GPIO, QADC (when digital inputs) and RESET pins have hysteresis, thus there is no hysteresis characteristic required for all other pins
9. The worst case V_{DDF} occurs during $\overline{\text{HRESET}}$ active (booting), other modules will not be running.
10. Maximum occurs during programming and erase. Read I_{PP} is lower.
11. All power consumption characteristics assume 50-pF loads and running a typical application.The power consumption of some modules could go up is they are exercised heavier, but the power consumption of other modules would decrease.
12. Current measured at maximum system clock frequency with QADC active.
13. This parameter is periodically sampled rather than 100% tested.
14. KAPWR and V_{DDSRAM} are powered up prior to any other supply.
15. To obtain full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$
16. To obtain full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$
17. The voltage at which the LVSRS bits in the VSRMCR register will be set ranges from 1.5 – 2.4 V.
18. All injection current is transferred to the V_{DDH}. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
19. Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.
20. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \le V_{DDA}$ and $V_{RL} \ge V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

G.8 Oscillator and PLL Electrical Characteristics

Table G-5 Oscillator and PLL

Characteristic	Symbol	Min	Typical	Max	Unit
Oscillator Startup Time (For Typical Crystal Capacitive Load) 4-MHz Crystal 20-MHz Crystal	 OSCstart4 OSCstart20			 10 10	mS
PLL Lock Time	T_{LOCK}			500	Input Clocks
PLL Operating Range	F_{VCOOUT}	30		80	MHz
Crystal Operating Range, MODCK[1:3]=0b010, or 0b110 MODCK[1:3] = 0b001, 0b011, 0b100, 0b101, 0b111	$F_{CRYSTAL}$	 2 15		 5 25	MHz
PLL Jitter PLL Jitter (averaged over 10 µs) MF < 20	F_{JIT} F_{JIT10}	-1% -0.3		+1% +0.3	—
Limp Mode Clock Frequency	F_{LIMP}	3[1]	7	12[1]	MHz
Oscillator Bias Current (XTAL) 4 MHz 20 MHz	I_{BIAS}	 — —		 -0.4[1] -0.8[1]	mA
Oscillator Drive (XTAL)	Iosc	8[1]		25[1]	mA
Oscillator Bias Resistor	R_{OSC}	0.72[1]	1.1	1.93[1]	MΩ

NOTES:
1. Values to be evaluated upon further characterization.

G.9 Power Up/Down Sequencing

See **SECTION 8 CLOCKS AND POWER CONTROL**.

G.10 FLASH Electrical Characteristics

NOTE

See **APPENDIX H FLASH ELECTRICAL CHARACTERISTICS FOR ALL J76N MASK SETS AND 0K02A AND 1K02A ONLY** for flash electrical characteristics for all J76N, 0K02A, and 1K02A mask sets. Contact Motorola for flash electrical characteristics for all J12F mask sets.

Table G-6 Program and Erase Characteristics

(V_{DDF} = 3.3 V ± 0.3 V, V_{PP}= 4.75 V to 5.25 V, $T_A = T_L$ to T_H)

Symbol	Meaning	Value			Units
		Minimum	Typical	Maximum	
E_{PULSE}	Number of Erase Pulses	8	8	27	
T_{ERASE}	Erase Pulse Time	98	100	102	mS
$P_{PULSE(4.75\ Vpp)}$	Number of Program Pulses @V_{PP} = 4.75	—	45000	48000[1,2]	Pulses
$P_{PULSE(5.0\ Vpp)}$	Number of Program Pulses @V_{PP} = 5.00	—	800	7000	Pulses
$P_{PULSE(5.25\ Vpp)}$	Number of Program Pulses @V_{PP} = 5.25	—	250	2000[3]	Pulses
T_{PROG}	Program Pulse Time	48	50	256.5	µS
$C_{PULSE(4.75\ Vpp)}$	Number of CENSOR Clear Pulses @V_{PP} = 4.75	47	87	700	Pulses
$C_{PULSE(5.0\ Vpp)}$	Number of CENSOR Clear Pulses @V_{PP} = 5.00	11	17	57	Pulses
$C_{PULSE(5.25\ Vpp)}$	Number of CENSOR Clear Pulses @V_{PP} = 5.25	8	10	37	Pulses
T_{CLEAR}	CENSOR Clear Pulse Time	98	100	102	mS
$S_{PULSE(4.75\ Vpp)}$	Number of CENSOR Set Pulses @V_{PP} = 4.75	47	87	700	Pulses
$S_{PULSE(5.0Vpp)}$	Number of CENSOR Set Pulses @V_{PP} = 5.00	11	17	57	Pulses
$S_{PULSE(5.25\ Vpp)}$	Number of CENSOR Set Pulses @V_{PP} = 5.25	8	10	37	Pulses
T_{SET}	CENSOR Set Pulse Time	98	100	102	mS

NOTES:
1. The worst case programming time occurs at V_{PP} = 4.75 V and T_A = -40 °C.
2. This value is based on initial device characterization and may not be tested in production.
3. The best case (fastest) programming time of < 50 pulses is at V_{PP} = 5.25 V and T_A = 125°C.

Table G-7 CMF AC and DC Power Supply Characteristics

Symbol	Meaning	Min. Value	Max Value	Unit
V_{DDF}	Operating Voltage Read, Program or Erase	3.0	3.6	V
I_{DDF}	Operating Current at 40.0 MHz, V_{DDF} = 3.3 V for a 256-Kbyte Module Read, Program or Erase Operation Disabled	 — —	 10 5	mA
V_{PP}	External Program or Erase Voltage Read Program or Erase	V_{DDF} -0.35 4.75	5.5 5.25	V
I_{DDPP}	External Program and Erase Current[1] Read, V_{PP} = 5 V Program, V_{PP} = 5.25 V Erase, V_{PP} = 5.25 V		<100 30[1] 30[1]	µA mA mA

NOTES:
1. Average current is less than 30 mA when programming both modules simultaneously.

G.10.1 Flash Module Life

Table G-8 Flash Module Life

Symbol	Meaning	Value
P/E Cycles[1]	Maximum Number of Program/Erase Cycles[2] to Guarantee Data Retention Array Blocks	100[3,4]
P/E Cycles[1]	Maximum Number of Program/Erase Cycles[2] to Guarantee Data Retention Censor Bits	10^4
Retention	Data Retention at Average Operating Temperature of 85 °C	Minimum 10 years

NOTES:
1. Target failure rate at specified number of program/erase cycles of 2ppm pending characterization of production silicon.
2. A program/erase cycle is defined as switching the bits from 1 → 0 → 1.
3. Reprogramming of a CMF array block prior to erase is not required.
4. Number of program/erase cycles to be adjusted pending characterization of production silicon.

G.10.2 Programming and Erase Algorithm

Table G-9 CMF Programming Algorithm (v6 and Later)

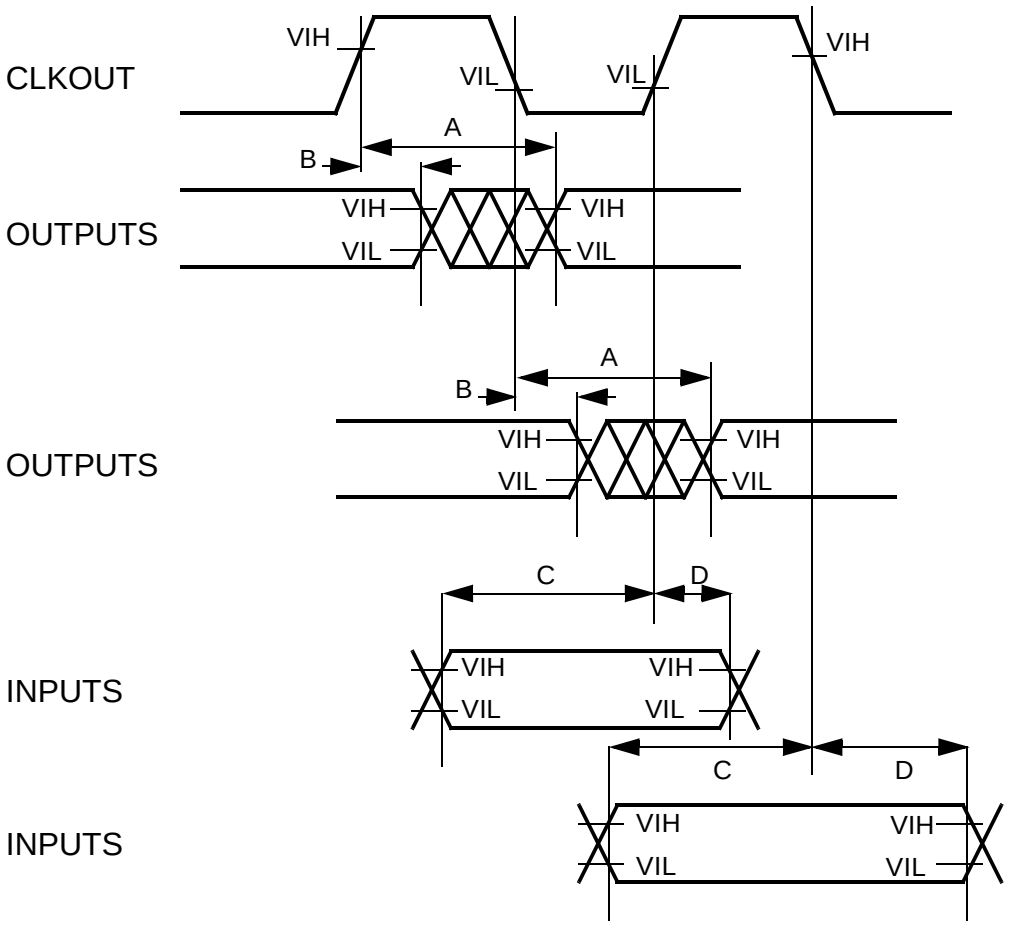
No. of Pulses	Pulse Width	NVR	PAWs	GDB	PAWs Mode	Description
4	256 µs	1	100	1	Mode 4NL	Negative gate ramp (low range)
4	256 µs	1	101	1	Mode 5NL	
4	256 µs	1	110	1	Mode 6NL	
4	256 µs	1	111	1	Mode 7NL	
20	50 µs	0	100	1	Mode 4NL	Negative gate ramp (high range)
20	50 µs	0	101	1	Mode 5NL	
20	50 µs	0	110	1	Mode 6NL	
max. 48,000	50 µs	0	111	1	Mode 7NL	

Table G-10 CMF Erase Algorithm (v6)

No. of Pulses	Pulse Width	NVR	PAWs	GDB	PAWs Mode	Description
1	100 ms[1]	1	100	1	Mode 4NL	Negative gate ramp (low range)
1	100 ms[1]	1	101	1	Mode 5NL	
1	100 ms[1]	1	110	1	Mode 6NL	
1	100 ms[1]	1	111	1	Mode 7NL	
1	100 ms[1]	0	100	1	Mode 4NL	Negative gate ramp (high range)
1	100 ms[1]	0	101	1	Mode 5NL	
1	100 ms[1]	0	110	1	Mode 6NL	
20	100 ms[2]	0	111	1	Mode 7NL	

NOTES:
1. No margin read after pulse.
2. Do margin read after each pulse.

G.11 Generic Timing



A. Maximum Output Delay Characteristic

B. Minimum Output Hold Time

C. Minimum input Setup Time Characteristic

D. Minimum input Hold Time Characteristic

Figure G-1 CLKOUT Timing

Table G-11 Bus Operation Timing

($T_A = T_L$ to T_H)

	Characteristic	Expression[1]	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
1	CLKOUT Period	TC	30.30		25		ns
1a	ENGCLK[2]			20		20	MHz
2	Clock Pulse Width Low		15 – 2%		12.5 – 2%		ns
3	Clock Pulse Width High		15 – 2%		12.5 – 2%		ns
4	CLKOUT Rise Time			5		5	ns
4a	ENGCLK Rise Time			20		20	ns
5	CLKOUT Fall Time			5		5	ns
5a	ENGCLK Fall Time			20		20	ns
6	Circuit Parameter	TCC	8		7.75		ns
7	CLKOUT to Signal Invalid (Hold Time) A[0:31] RD/$\overline{WR}$ BURST D[0:31]	0.2TC – 1.0	5		4		ns
7a	CLKOUT to Signal Invalid: (Hold Time) TSIZ[0:1] $\overline{RSV}$ AT[0:3] $\overline{BDIP}$	0.2TC – 1.0	5		4		ns
7b	CLKOUT to Signal Invalid (Hold Time)[3] $\overline{BR}$ $\overline{BG}$ FRZ VFLS[0:1] VF[0:2] IWP[0:2] LWP[0:1] $\overline{PTR}$ $\overline{RETRY}$ $\overline{STS}$[4]	0.2TC – 1.0	5		4		ns
7c	Slave mode CLKOUT to Signal Invalid D[0:31]	0.25TC + TCC	5		4		ns
8	CLKOUT to Signal Valid A[0:31] RD/$\overline{WR}$ BURST	0.25TC + TCC	7.5	14	6.25	14	ns

Table G-11 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression[1]	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
8a	CLKOUT to Signal Valid TSIZ[0:1] $\overline{RSV}$ AT[0:3] $\overline{BDIP}$	0.25TC + TCC	7.5	15	6.25	15	ns
8b	CLKOUT to Signal Valid[3] $\overline{BR}$ $\overline{BG}$ VFLS[0:1] VF[0:2] IWP[0:2] FRZ LWP[0:1] $\overline{PTR}$ $\overline{RETRY}$ $\overline{MTS}$	0.25TC + TCC	7.5	15	6.25	14	ns
8c	Slave Mode CLKOUT to Signal Valid D[0:31]	0.25TC + TCC + 4	7.5	15	6.25	14	ns
8d	CLKOUT to Signal Valid D[0:31]	0.25TC + TCC	7.5	14	6.25	14	ns
9	CLKOUT to Signal invalid A[0:31] RD/$\overline{WR}$ $\overline{BURST}$ D[0:31] TSIZ[0:1] $\overline{RSV}$ AT[0:3] $\overline{PTR}$ $\overline{RETRY}$	0.25TC + TCC	7.5	15	6.25	13	ns
10	CLKOUT to $\overline{TS}$, $\overline{BB}$ Assertion	0.25TC + TCC	7.5	15	6.25	14	ns
10a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Assertion (When Driven by the Memory Controller)	—		10		10	ns
10b	CLKOUT to $\overline{RETRY}$ Assertion (When Driven by the Memory Controller)	—		10		10	ns
11	CLKOUT to $\overline{TS}$, $\overline{BB}$ Negation	0.25TC + TCC	7.5	15	6.25	14	ns
11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Negation (When Driven by the Memory Controller)	—		11		11	ns
11b	CLKOUT to $\overline{RETRY}$ Negation (When Driven by the Memory Controller)	—		11		11	ns
12	CLKOUT to $\overline{TS}$, $\overline{BB}$ Signal invalid	0.25TC + 14	7.5	21	6.25	20	ns

Table G-11 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression[1]	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Signal invalid (When Driven by the Memory Controller)			15		15	ns
13	CLKOUT to $\overline{TEA}$ Assertion			11		11	ns
14	CLKOUT to $\overline{TEA}$ Signal invalid			15		15	ns
15	Input Valid to CLKOUT (Setup Time) $\overline{TA}$ $\overline{TEA}$ $\overline{BI}$[3]		13		12		ns
15a	Input Valid to CLKOUT (Setup Time) $\overline{KR}$ $\overline{CR}$ $\overline{RETRY}$		11		10		ns
15b	Input Valid to CLKOUT (Setup Time) $\overline{BB}$ $\overline{BG}$ $\overline{BR}$[5]		10		8		ns
16	CLKOUT to Signal Invalid (Hold Time) $\overline{TA}$ $\overline{TEA}$ $\overline{BI}$ $\overline{BB}$ $\overline{BG}$ $\overline{BR}$ [4]		2		2		ns
16a	CLKOUT to Signal Invalid (Hold Time) $\overline{RETRY}$ $\overline{KR}$ $\overline{CR}$		2		2		ns
17	Signal Valid to CLKOUT Rising Edge (Setup Time) D[0:31][6]		7		6		ns
18	CLKOUT Rising Edge to Signal Invalid (Hold Time) D[0:31][6]		1		1		ns
19	CLKOUT Rising Edge to $\overline{CS}$ asserted -GPCM- ACS = 00	0.25TC + TCC + 1	7.5	16	6.25	14	ns
19a	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0 or 1	TCC + 1		9		8	ns
19b	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0 or 1	0.25TC + TCC + 1	7.5	16	6.25	14	ns

Table G-11 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression[1]	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
19c	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1	0.25TC + TCC + 4	7.5	20	6.25	17	ns
20	CLKOUT Rising Edge to $\overline{CS}$ Negated -GPCM- Read Access or Write Access When CSNT = 0 or Write Access When CSNT = 1 and ACS = 00	TCC + 1	1	9	1	8	ns
21	A[0:31] to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0		2		1.5		ns
21a	A[0:31] to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0		8		7		ns
22	CLKOUT Rising Edge to $\overline{OE}$, $\overline{WE[0:3]}$ Asserted			11		9	ns
23	CLKOUT Rising Edge to $\overline{OE}$ Negated		2	11	0	8	ns
24	A[0:31] to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 1		30		25		ns
24a	A[0:31] to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 1		38		32		ns
25	CLKOUT Rising Edge to $\overline{WE[0:3]}$ Negated -GPCM-Write Access CSNT = '0'			9		8	ns
25a	CLKOUT Falling Edge to $\overline{WE[0:3]}$ Negated -GPCM-Write Access TRLX = '0' or '1', CSNT = '1, EBDF = 0'.	0.25TC + TCC + 1	7.5	6.25	5	14	ns
25b	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0' or '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0	0.25TC + TCC + 1	7.5	16	5	14	ns
25c	CLKOUT Falling Edge to $\overline{WE[0:3]}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1, EBDF = 1'.	0.25TC +TCC + 4	7.5	20	6.25	17	ns
25d	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	0.25TC +TCC + 4	7.5	20	6.25	17	ns
26	$\overline{WE[0:3]}$ Negated to D[0:31] Signal invalid -GPCM- Write Access, CSNT = '0'		0		0		ns
26a	$\overline{WE[0:3]}$ Negated to D[0:31] Signal invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 0		5		4		ns

Table G-11 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression[1]	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
26b	$\overline{CS}$ Negated to D[0:31], Signal invalid -GPCM- Write Access, ACS = '00', TRLX = '0' & CSNT = '0'		0		0		ns
26c	$\overline{CS}$ Negated to D[0:31], Signal invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0		5		4		ns
26d	$\overline{WE}$[0:3] Negated to D[0:31] Signal invalid -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 0		38		29		ns
26e	$\overline{CS}$ Negated to D[0:31] Signal invalid -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0		38		29		ns
26f	$\overline{WE}$[0:3] Negated to D[0:31] Signal Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 1		12		5		ns
26g	$\overline{CS}$ Negated to D[0:31] Signal invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1		12		5		ns
26h	$\overline{WE}$[0:3] Negated to D[0:31] Signal invalid -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 1		30		24		ns
26i	$\overline{CS}$ Negated to D[0:31] Signal invalid -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1		30		24		ns
27	$\overline{CS}$, $\overline{WE}$[0:3] Negated to A[0:31] Invalid -GPCM- Write Access[7]		0		0		ns
27a	$\overline{WE}$[0:3] Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1'. $\overline{CS}$ Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 0		18		4		ns

Table G-11 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression[1]	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
27b	$\overline{WE}$[0:3] Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '1', CSNT = '1'. $\overline{CS}$ Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = 10, ACS = ='11', EBDF = 0		38		29		ns
27c	$\overline{WE}$[0:3] Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1'. $\overline{CS}$ Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 1		5		4		ns
27d	$\overline{WE}$[0:3] Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '1', CSNT = '1'. CS Negated to A[0:31] Invalid -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 1		30		24		ns
28	A[0:31], TSIZ[0:1], RD/$\overline{WR}$, $\overline{BURST}$, $\overline{BDIP}$ Valid to CLKOUT Rising Edge. (Slave Mode Setup Time)		11		9		ns
28a	Slave Mode D[0:31] Valid to CLKOUT Rising Edge				7		ns
29	$\overline{TS}$ Valid to CLKOUT Rising Edge (Setup Time)		9		7		ns
30	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time).		2		2		ns

NOTES:

1. Expressions are approximate equations only.
2. This is the maximum frequency at which ENGCLK will meet output drive and rise/fall time specifications.
3. The timing for $\overline{BR}$ ouput is relevant when the MPC555 / MPC556 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC555 / MPC556 is selected to work with internal bus arbiter.
4. The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by the external device (and not the memory controller).
5. The timing required for $\overline{BR}$ input is relevant when the MPC500 family microcontroller is selected to work with internal bus arbiter. The timing for $\overline{BG}$ is relevant when the MPC500 is selected to work with external bus arbiter.
6. The D[0:31] input timings 17 and 18 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.
7. The timing 27 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE}$[0:3] when CSNT = '0'.

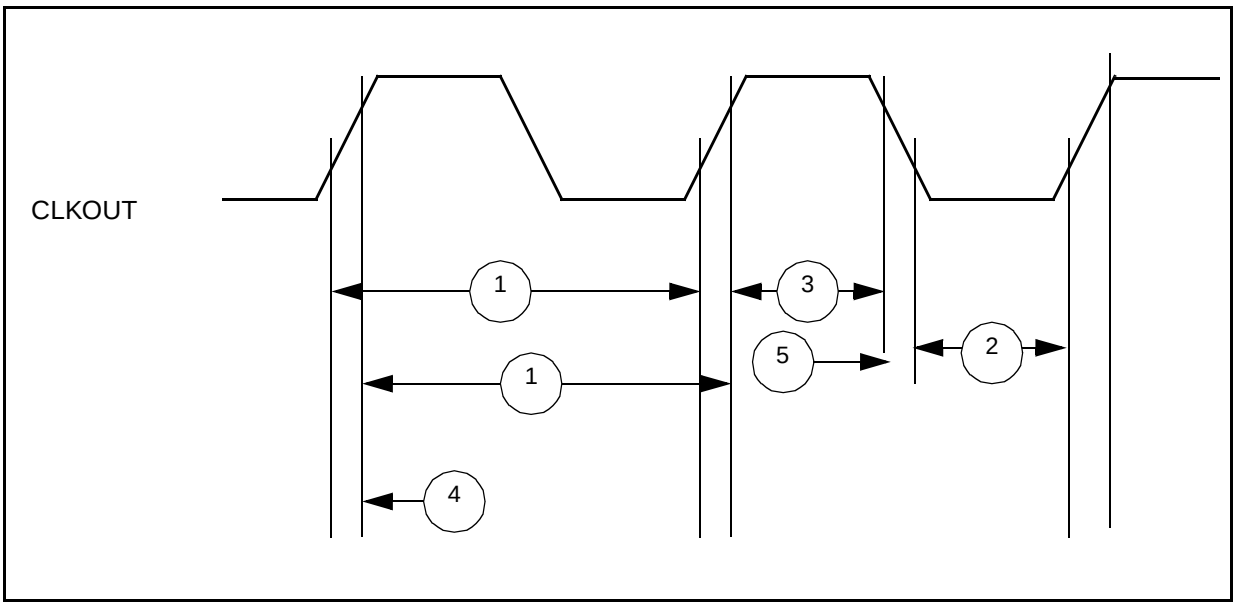


Figure G-2 External Clock Timing

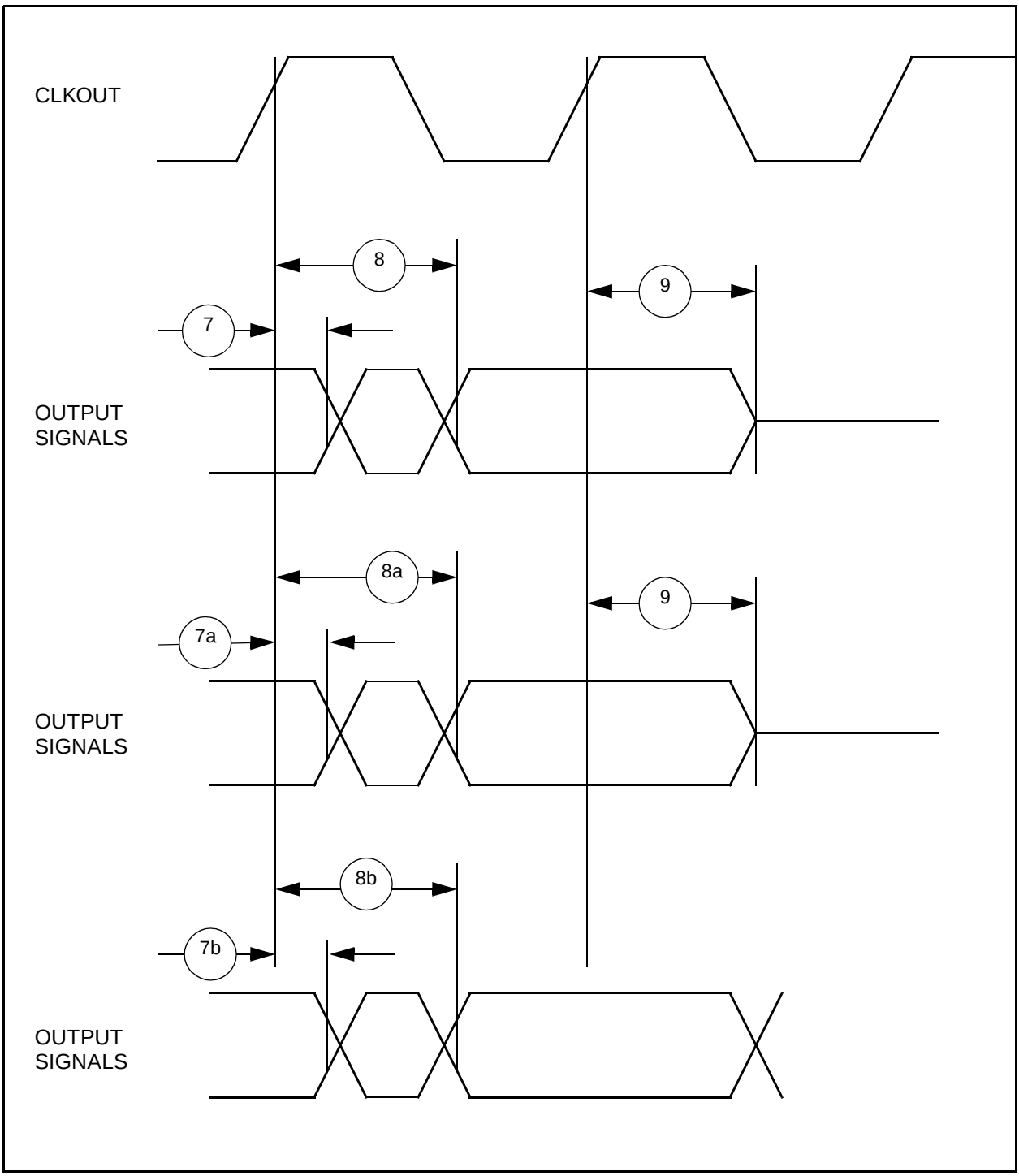


Figure G-3 Synchronous Output Signals Timing

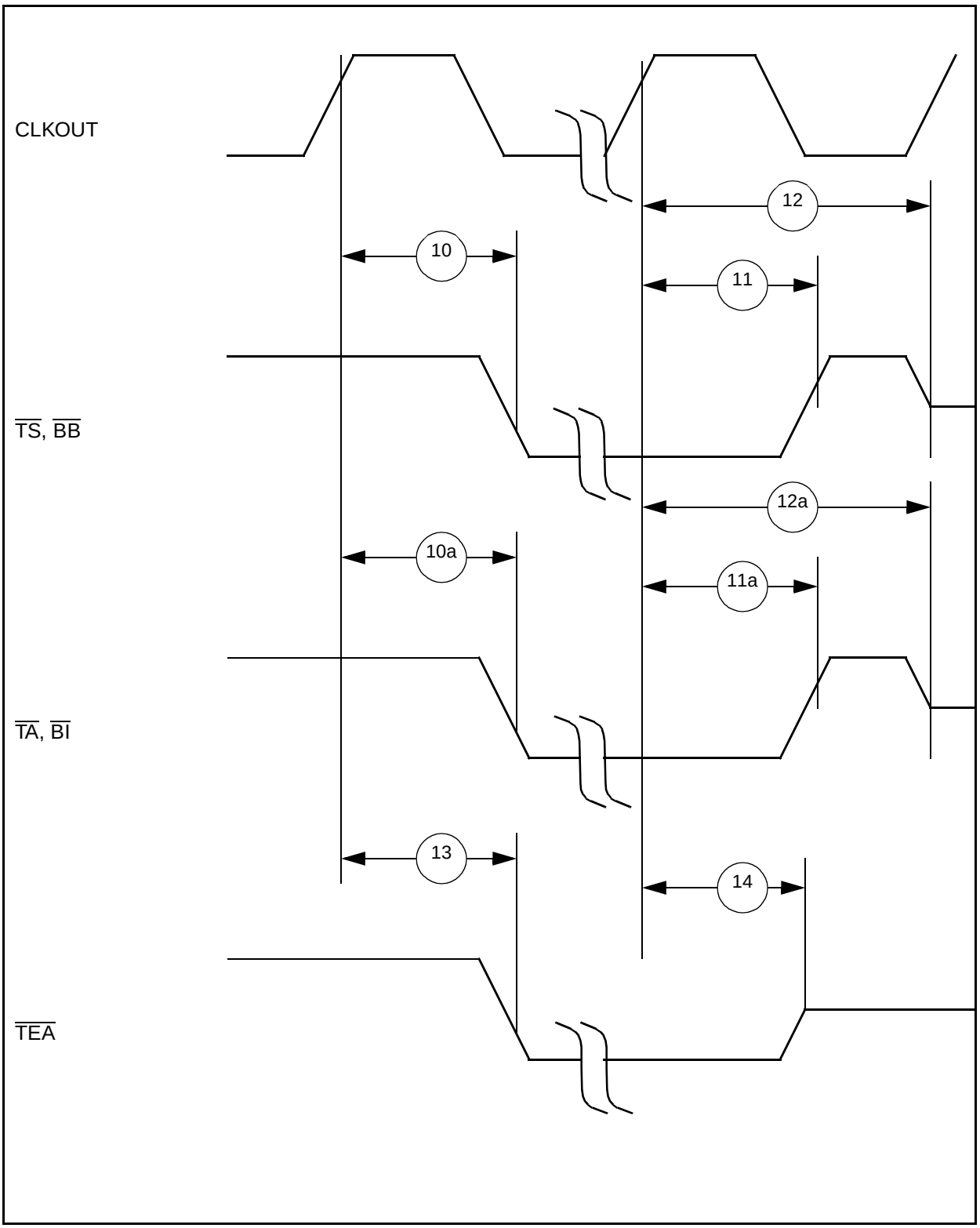


Figure G-4 Synchronous Active Pull-Up and Open Drain Outputs Signals Timing

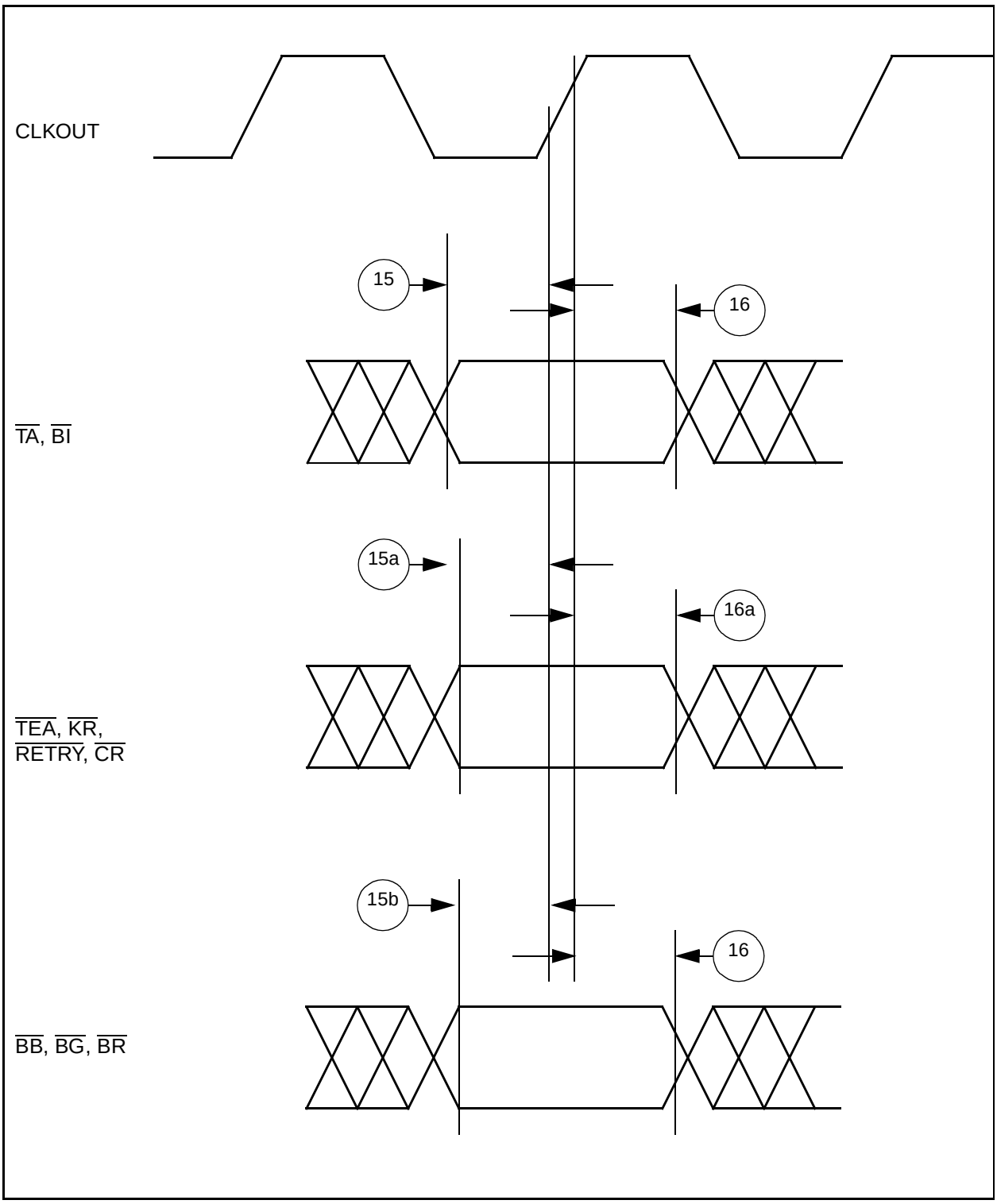


Figure G-5 Synchronous Input Signals Timing

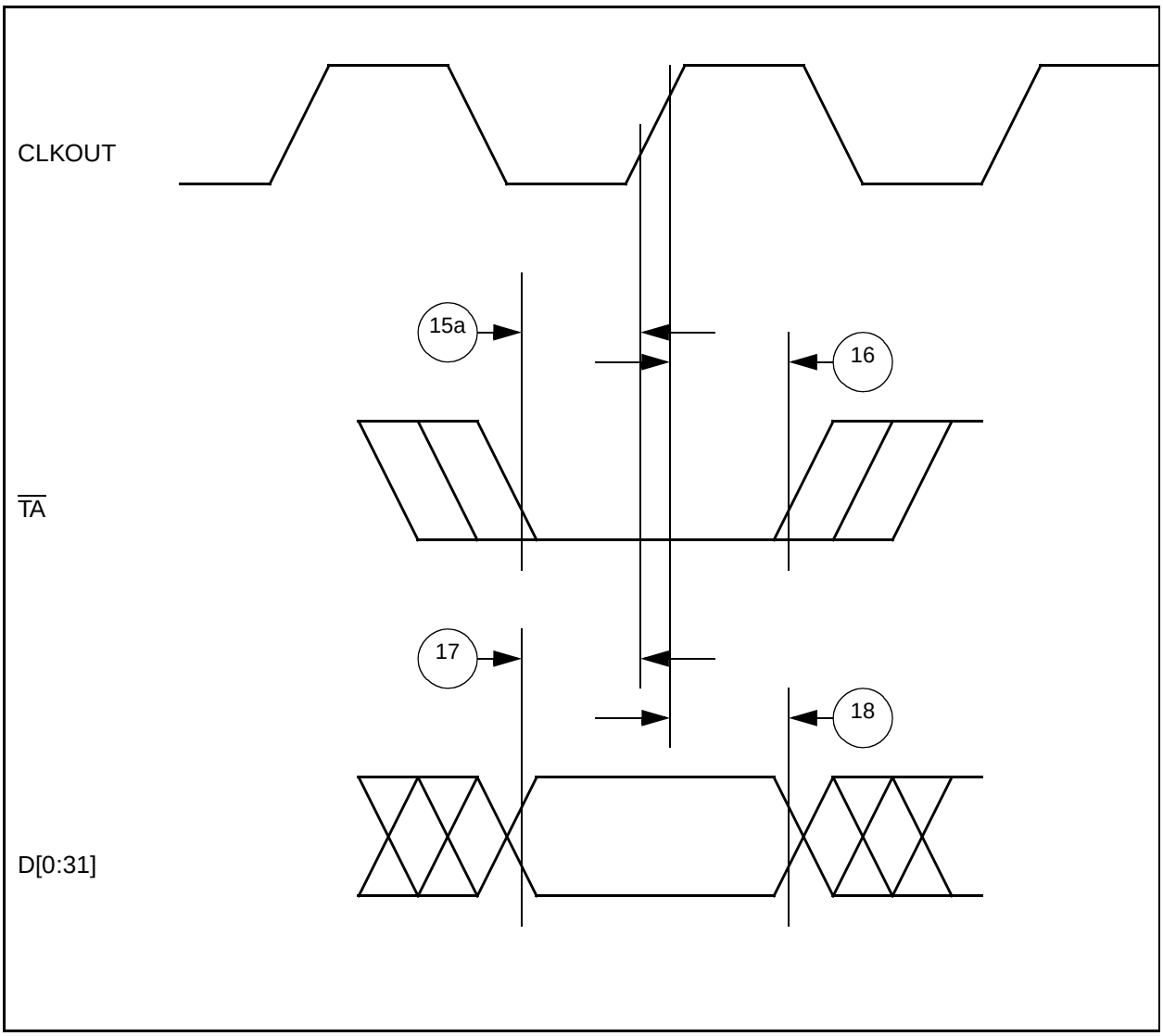


Figure G-6 Input Data Timing in Normal Case

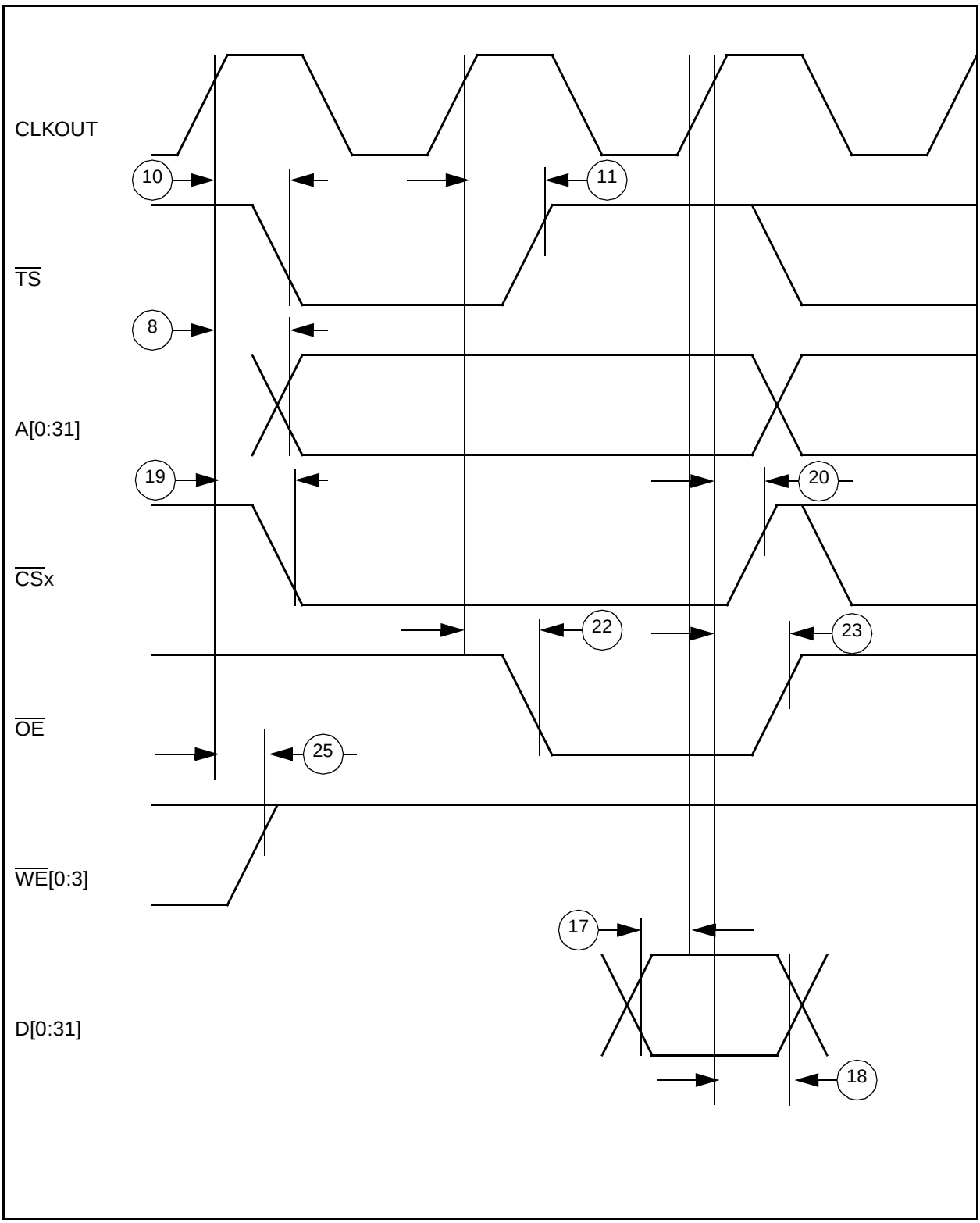


Figure G-7 External Bus Read Timing (GPCM Controlled — ACS = ‘00’)

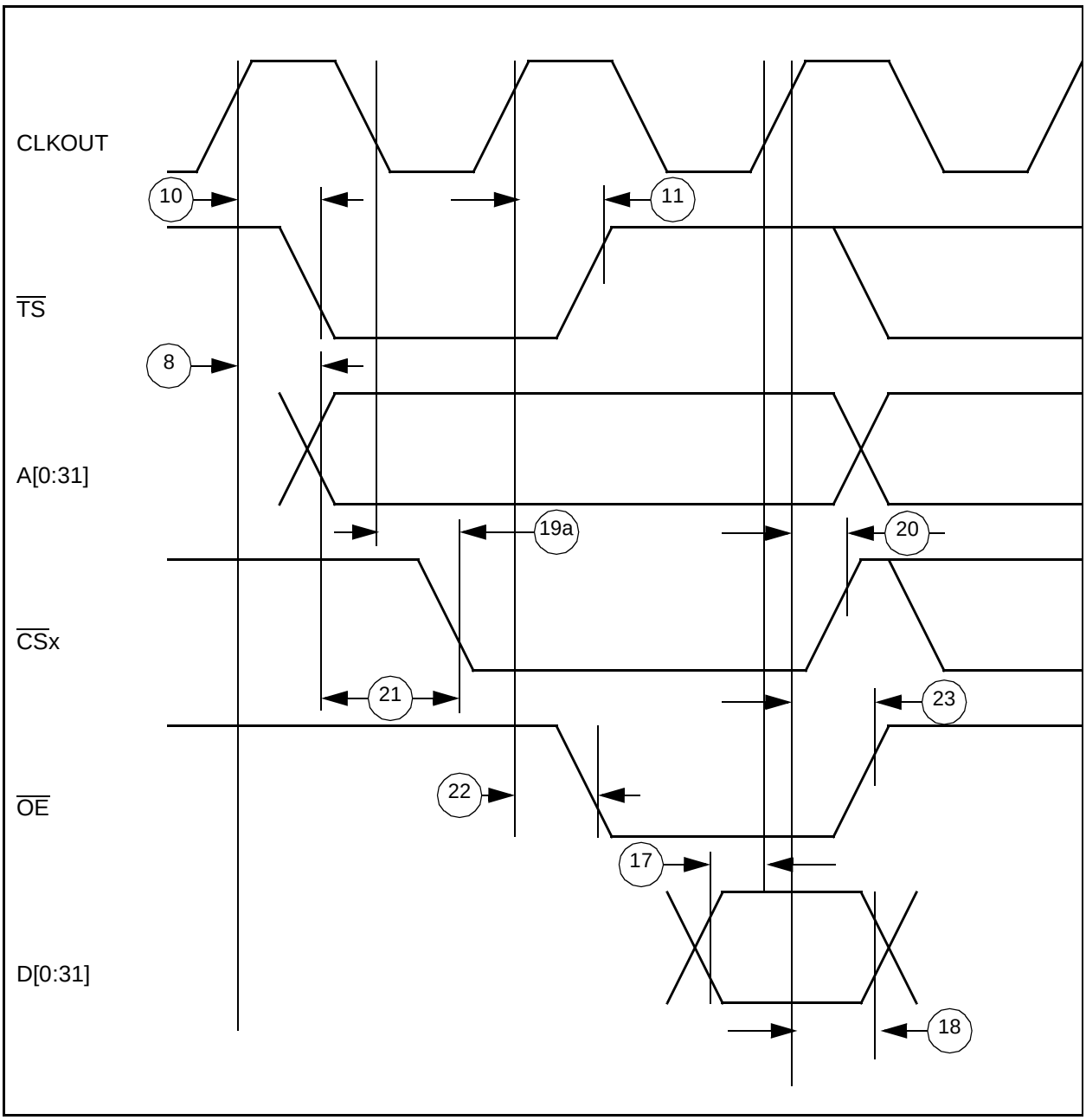


Figure G-8 External Bus Read Timing (GPCM Controlled — TRLX = ‘0’ ACS = ‘10’)

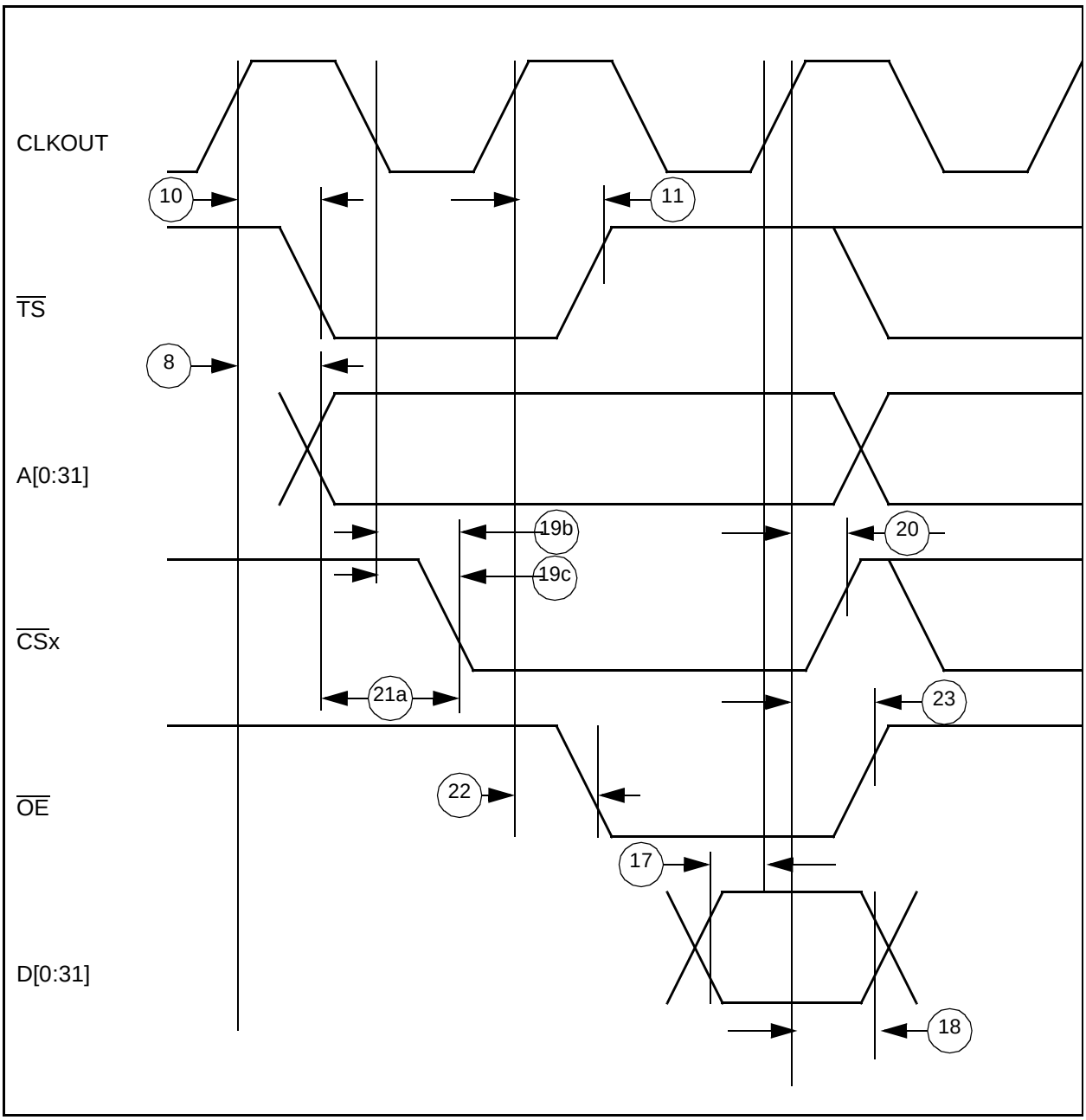


Figure G-9 External Bus Read Timing (GPCM Controlled — TRLX = ‘0’ ACS = ‘11’)

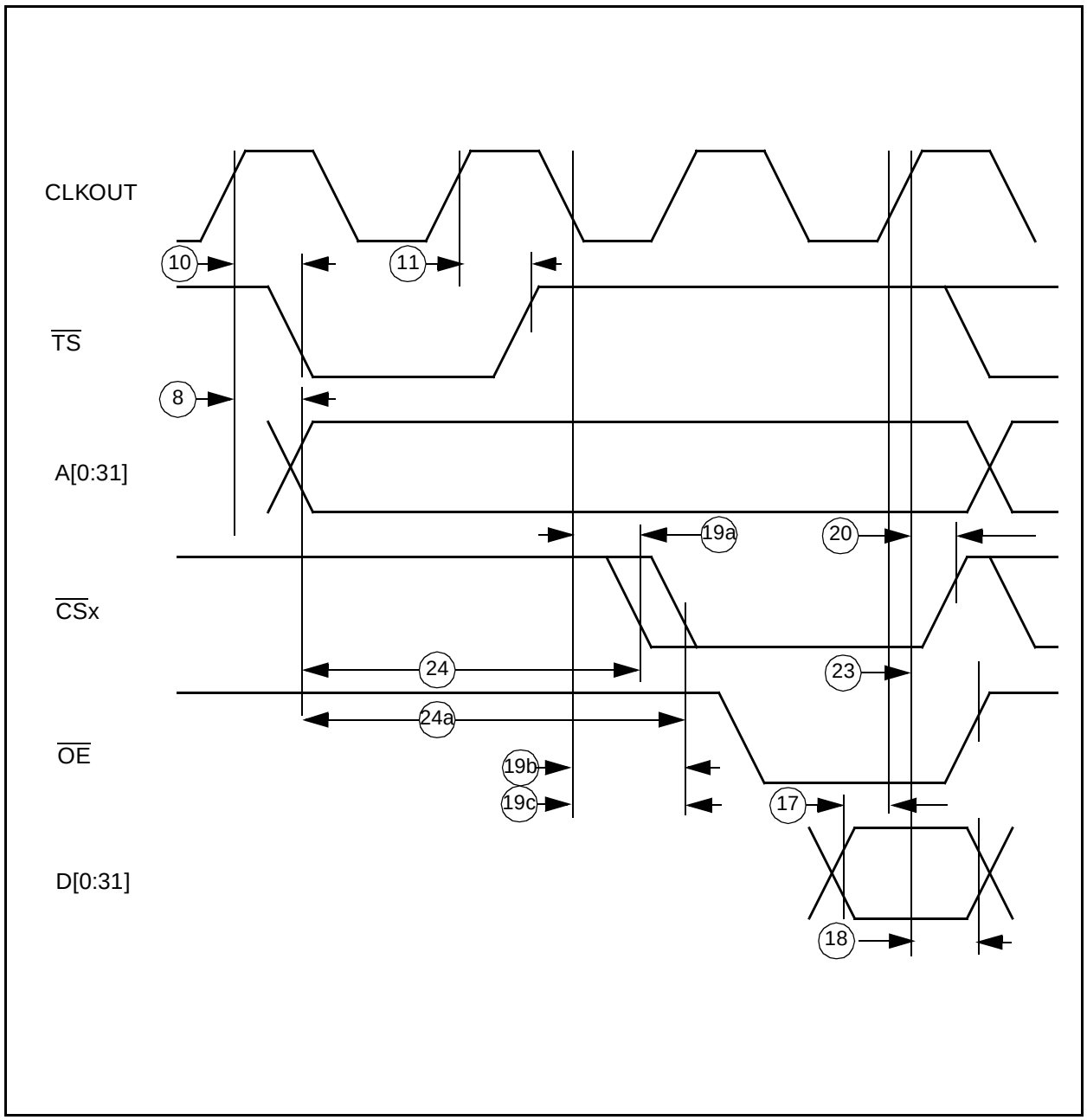


Figure G-10 External Bus Read Timing
(GPCM Controlled — TRLX = ‘1’, ACS = ‘10’, ACS = ‘11’)

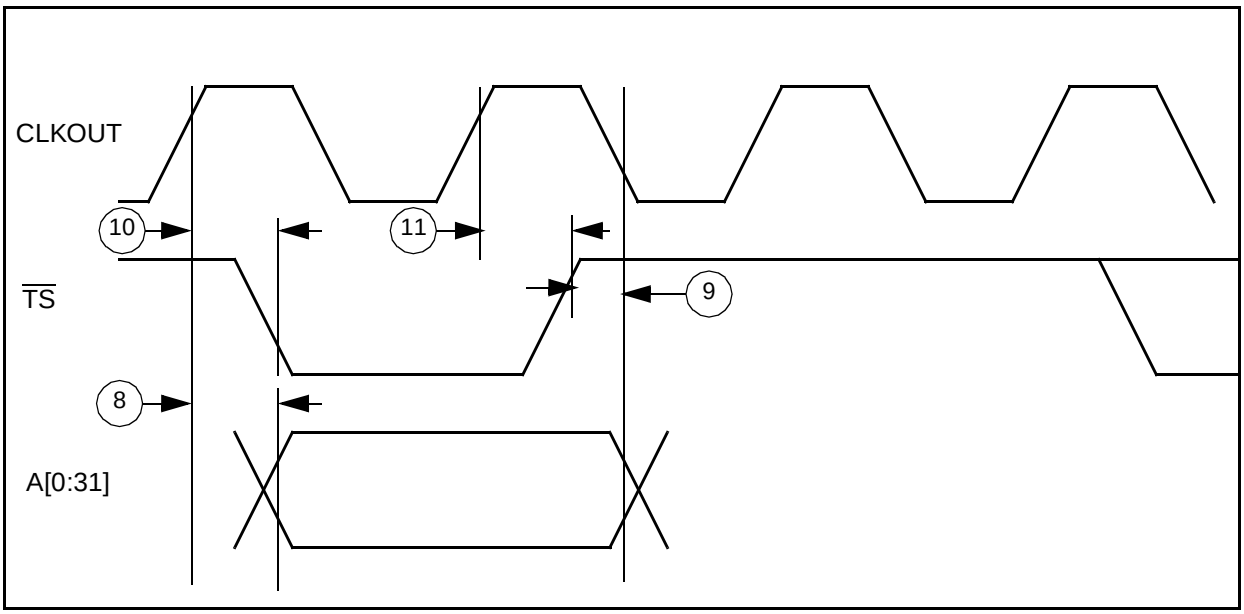


Figure G-11 Address Show Cycle Bus Timing

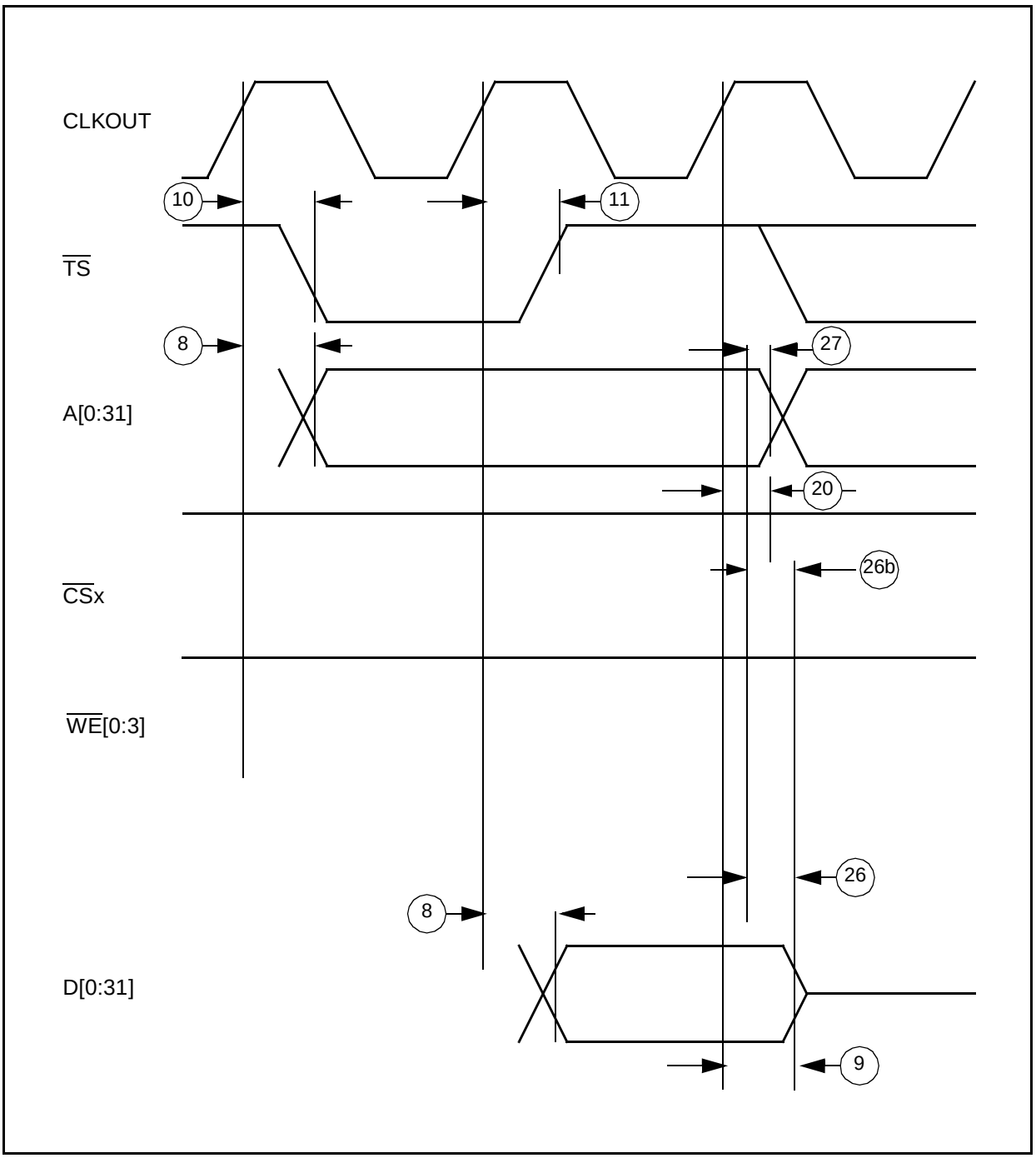


Figure G-12 Address and Data Show Cycle Bus Timing

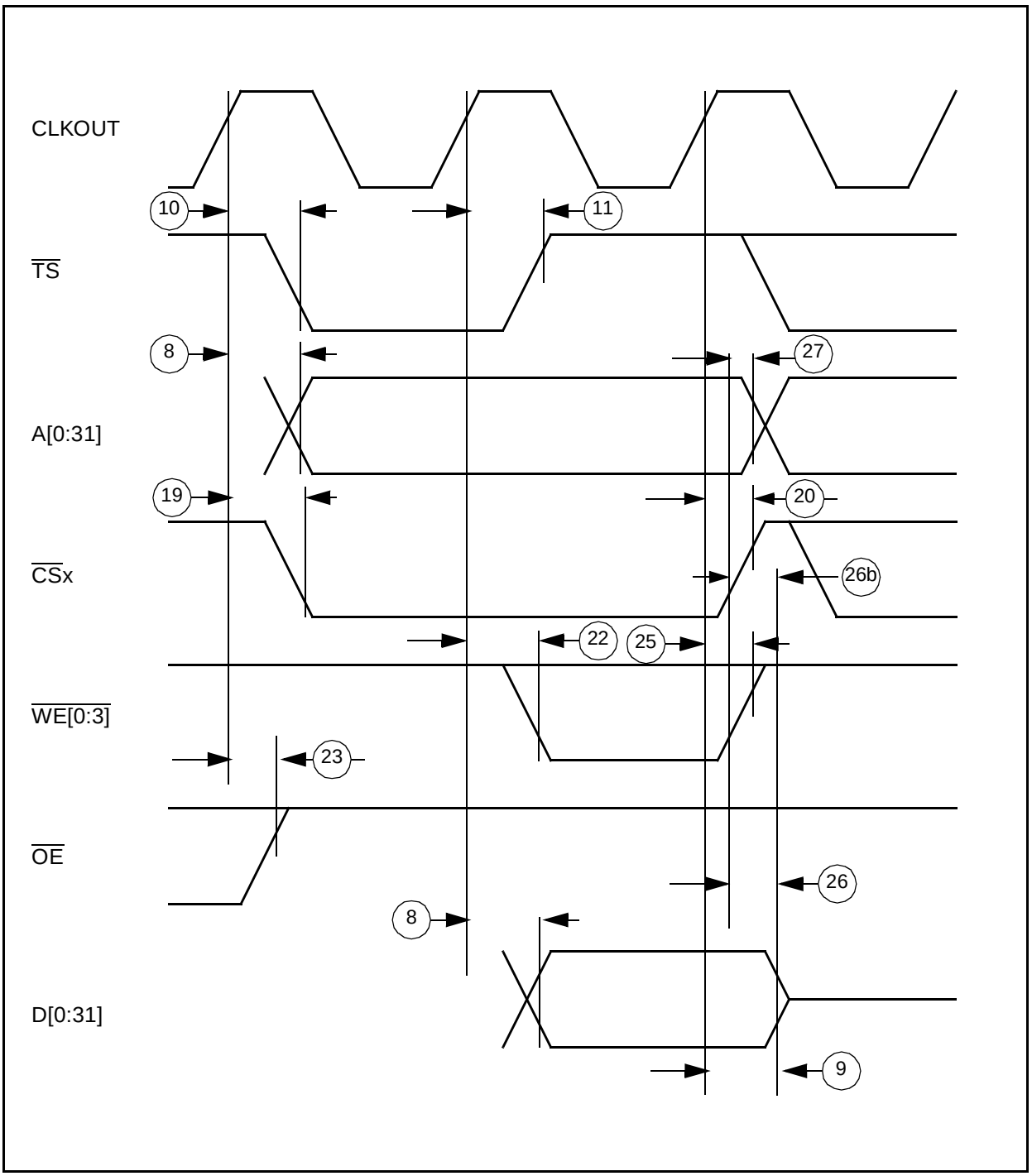


Figure G-13 External Bus Write Timing (GPCM Controlled — TRLX = '0', CSNT = '0')

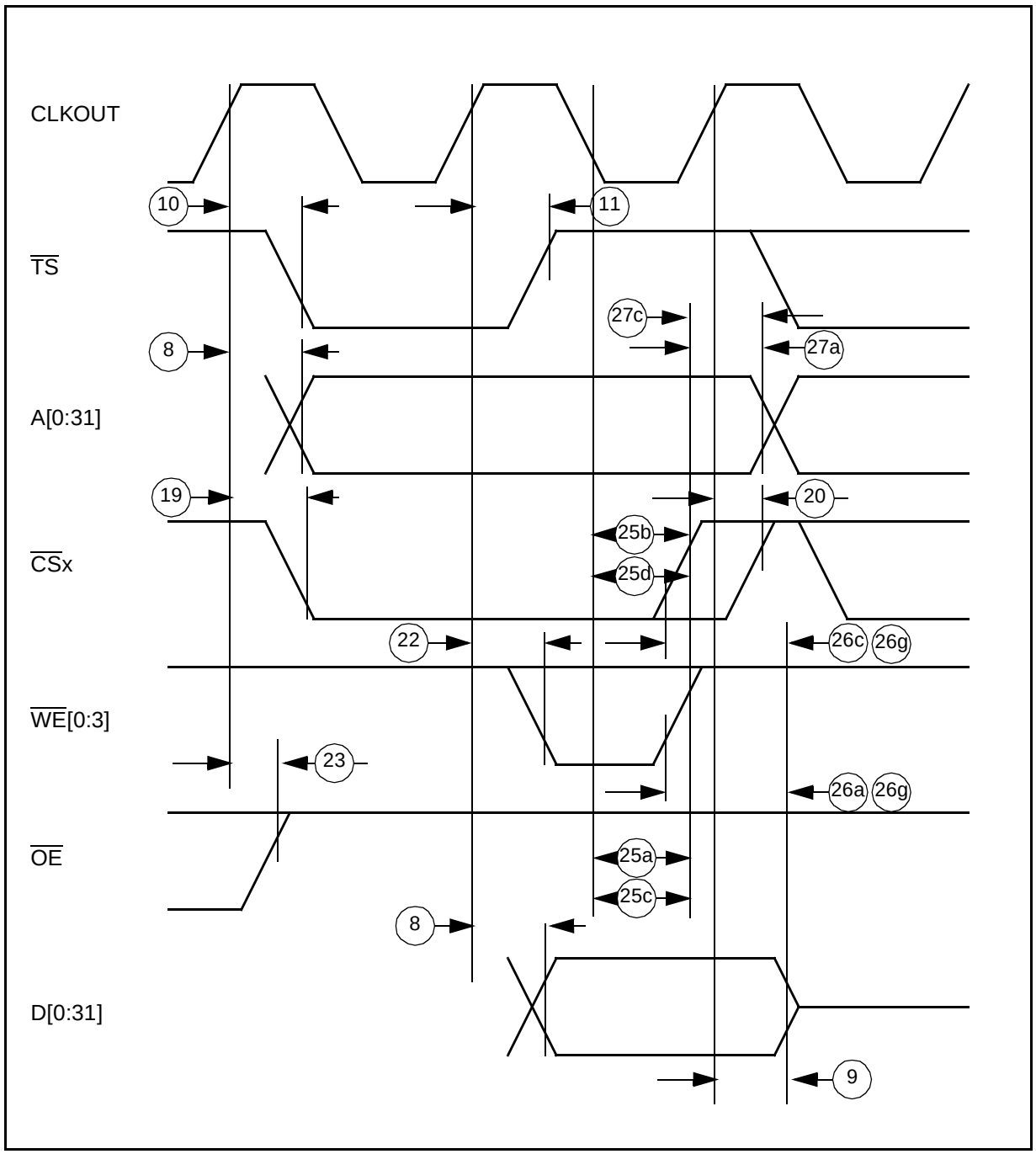


Figure G-14 External Bus Write Timing (GPCM Controlled — TRLX = ‘0’, CSNT = ‘1’)

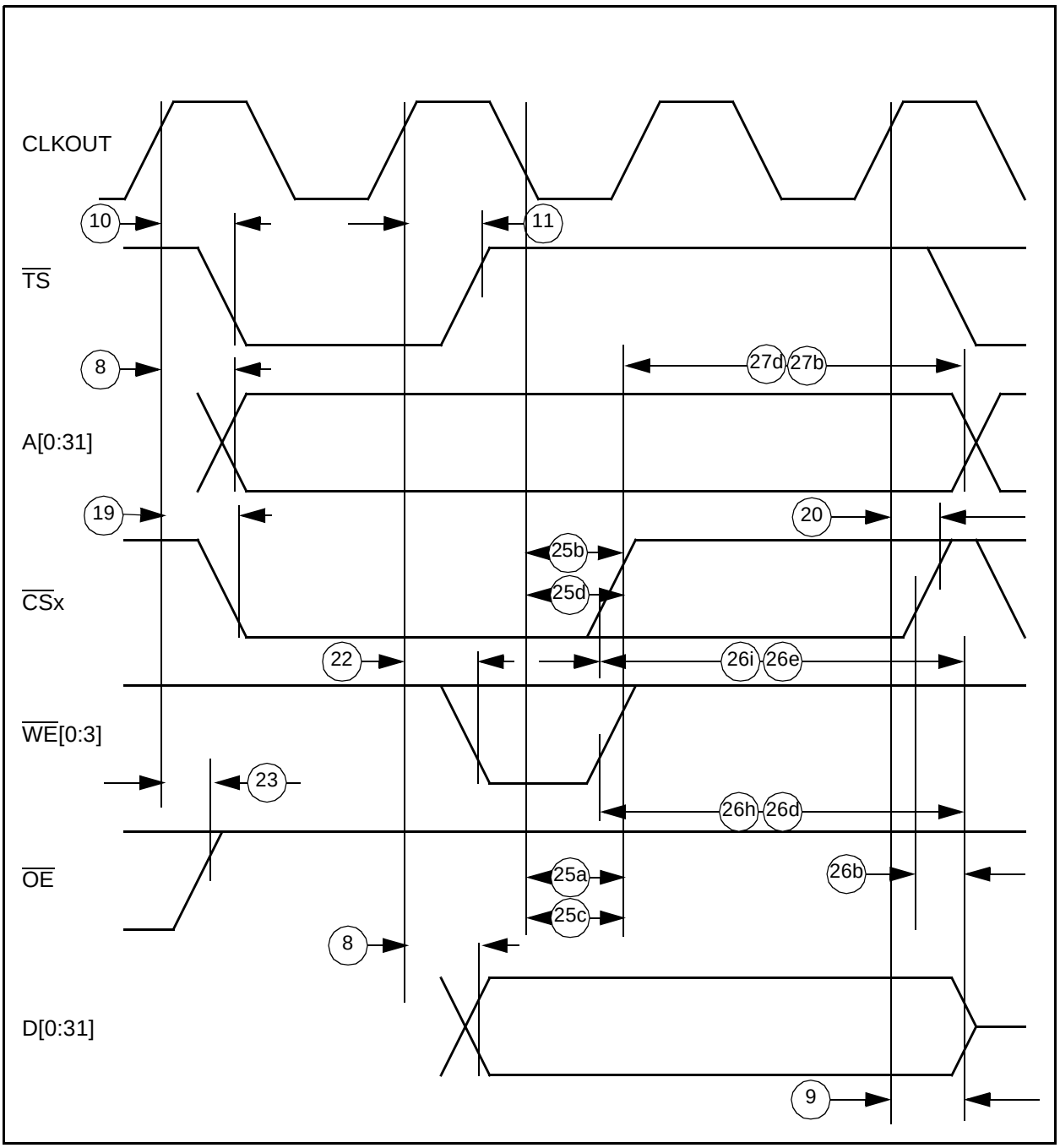


Figure G-15 External Bus Write Timing (GPCM Controlled — TRLX = '1', CSNT = '1')

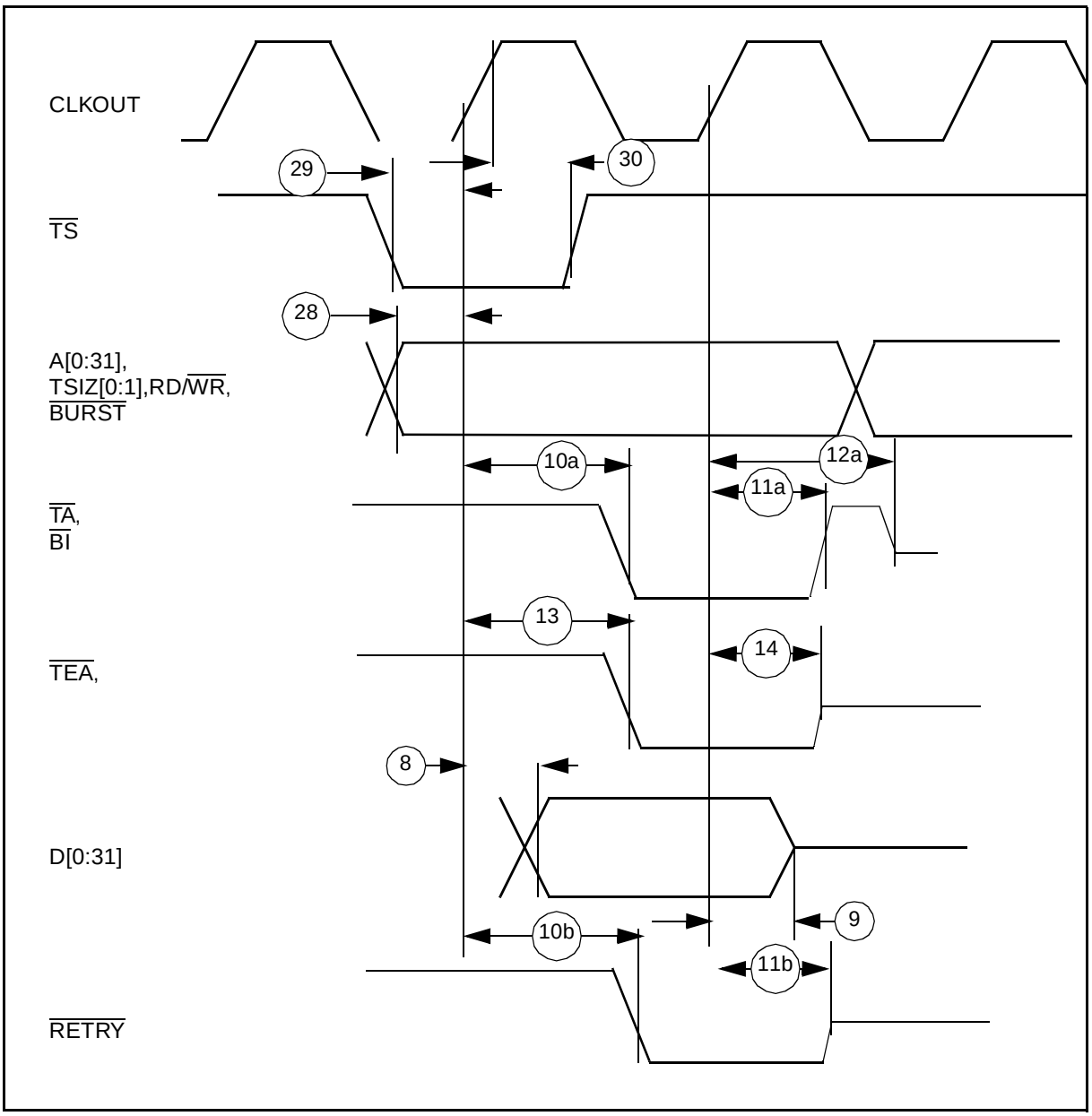


Figure G-16 External Master Read from Internal Registers Timing

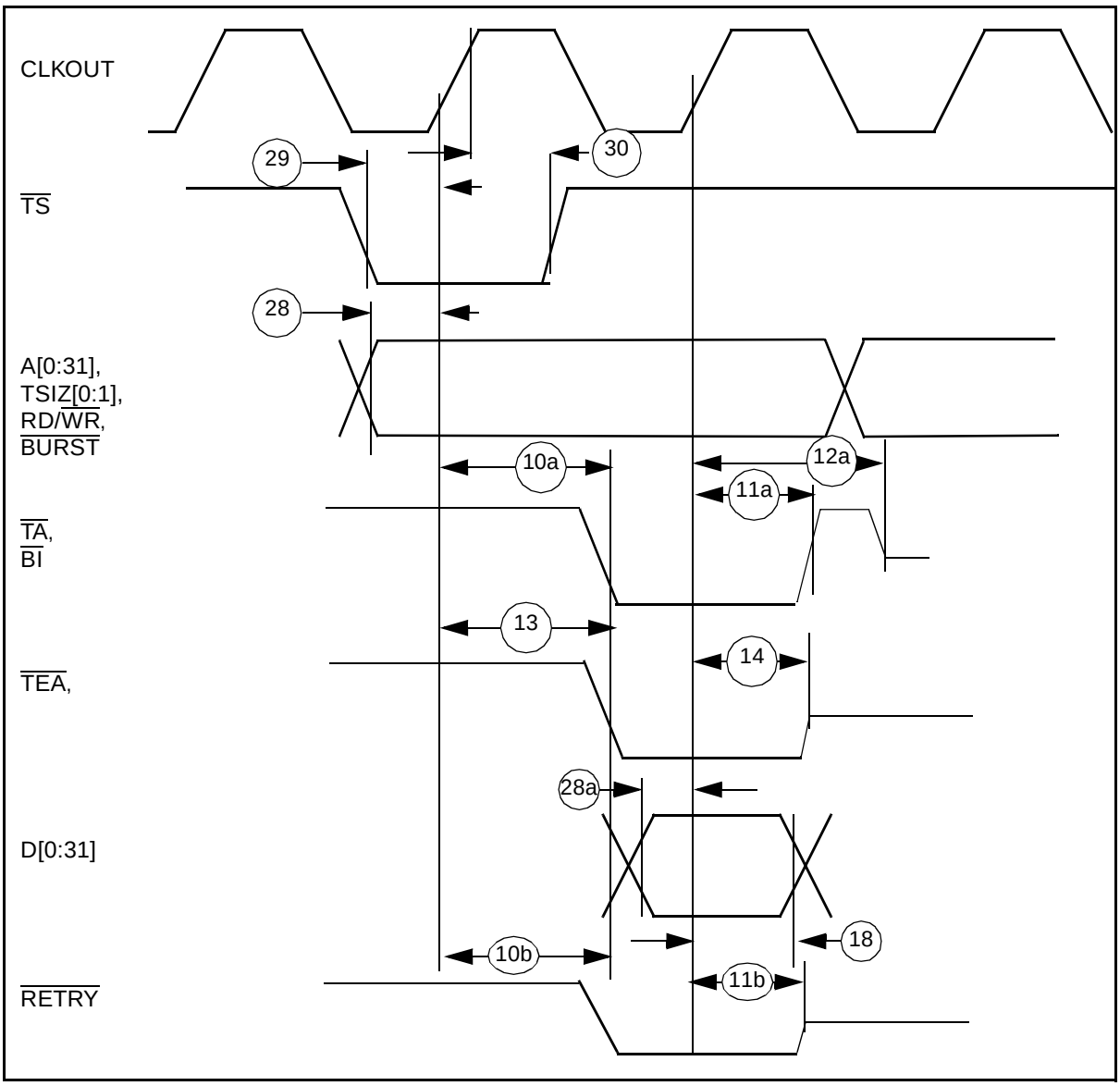


Figure G-17 External Master Write to Internal Registers Timing

G.12 Interrupt Timing

Table G-12 Interrupt Timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
31	$\overline{IRQ}$x Valid to CLKOUT Rising Edge (Setup Time)[1]		10		10		ns
32	$\overline{IRQ}$x Hold Time After CLKOUT[1]		2		2		ns
33	$\overline{IRQ}$x Pulse Width Low		3		3		ns
34	$\overline{IRQ}$x Pulse Width High		3		3		ns
35	$\overline{IRQ}$x Edge to Edge Time	4*TC	121		100		ns

NOTES:

1. The timings 31 and 32 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

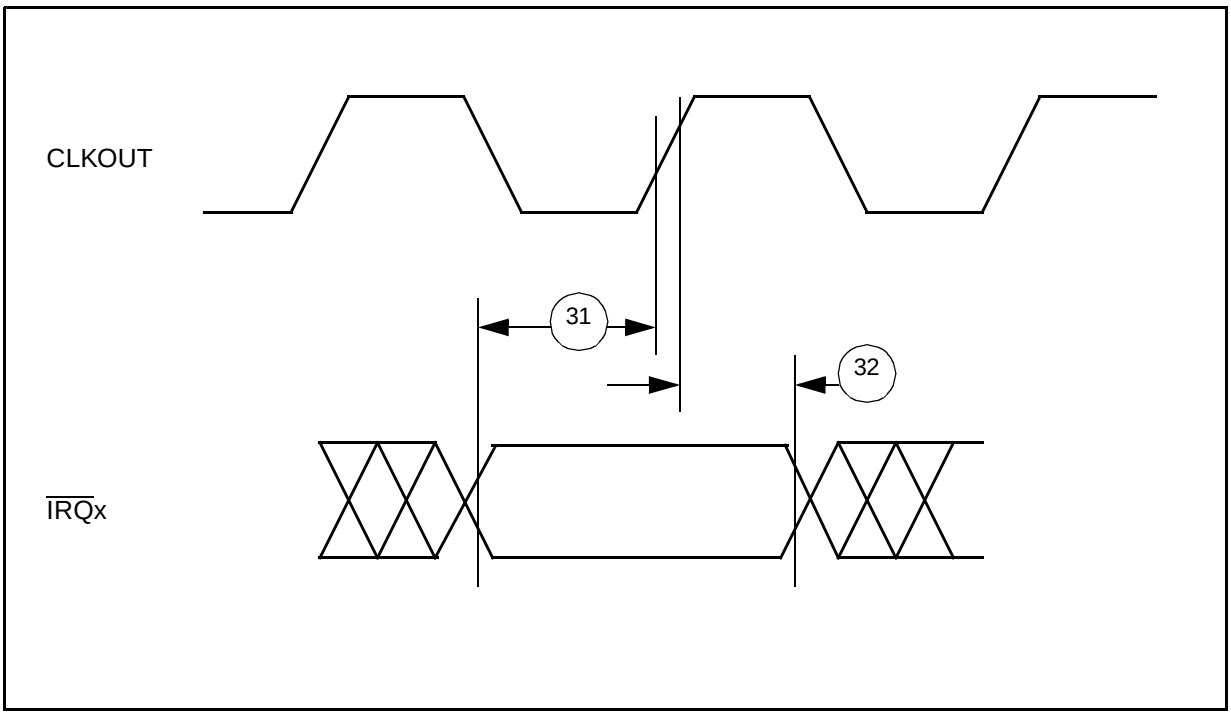


Figure G-18 Interrupt Detection Timing for External Level Sensitive Lines

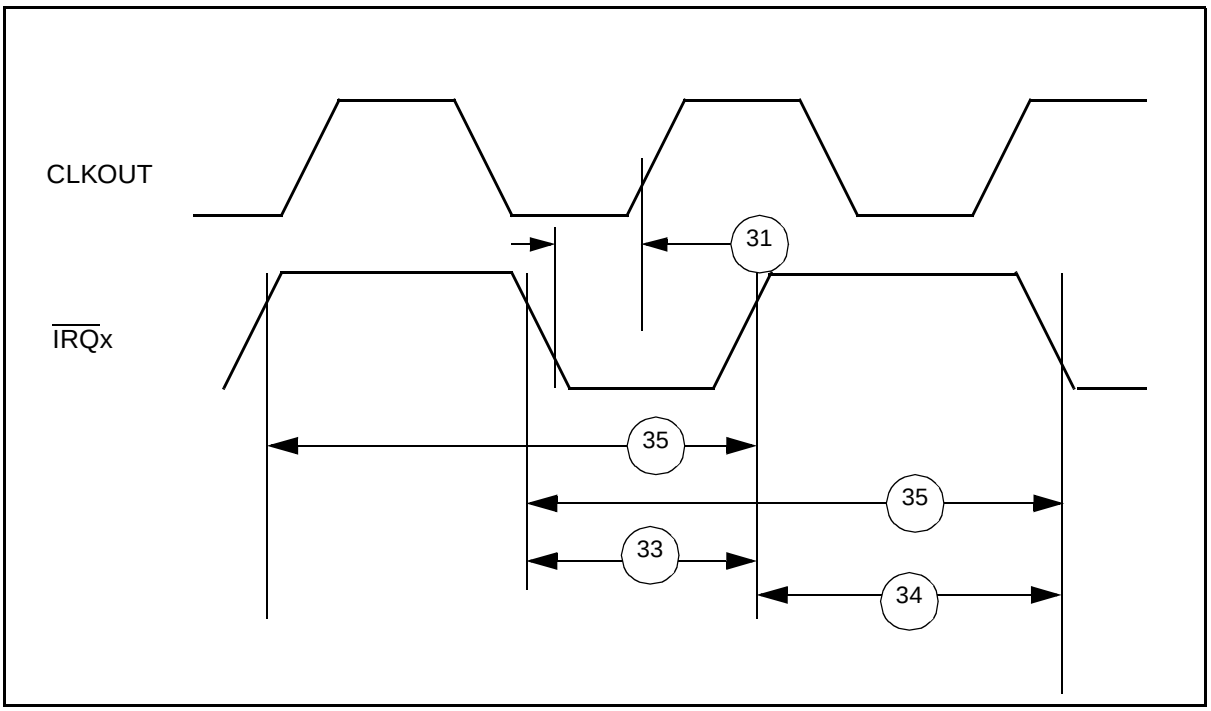


Figure G-19 Interrupt Detection Timing for External Edge Sensitive Lines

G.13 Debug Port Timing

Table G-13 Debug Port timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
36	DSCK Cycle Time		120	—	60	—	ns
37	DSCK Clock Pulse Width		50	—	25	—	ns
38	DSCK Rise and Fall Times		0	3	0	3	ns
39	DSDI Input Data Setup Time		12	—	12	—	ns
40	DSDI Data Hold Time		5	—	5	—	ns
41	DSCK low to DSDO Data Valid		0	18	0	18	ns
42	DSCK low to DSDO Invalid		0	—	0	—	ns

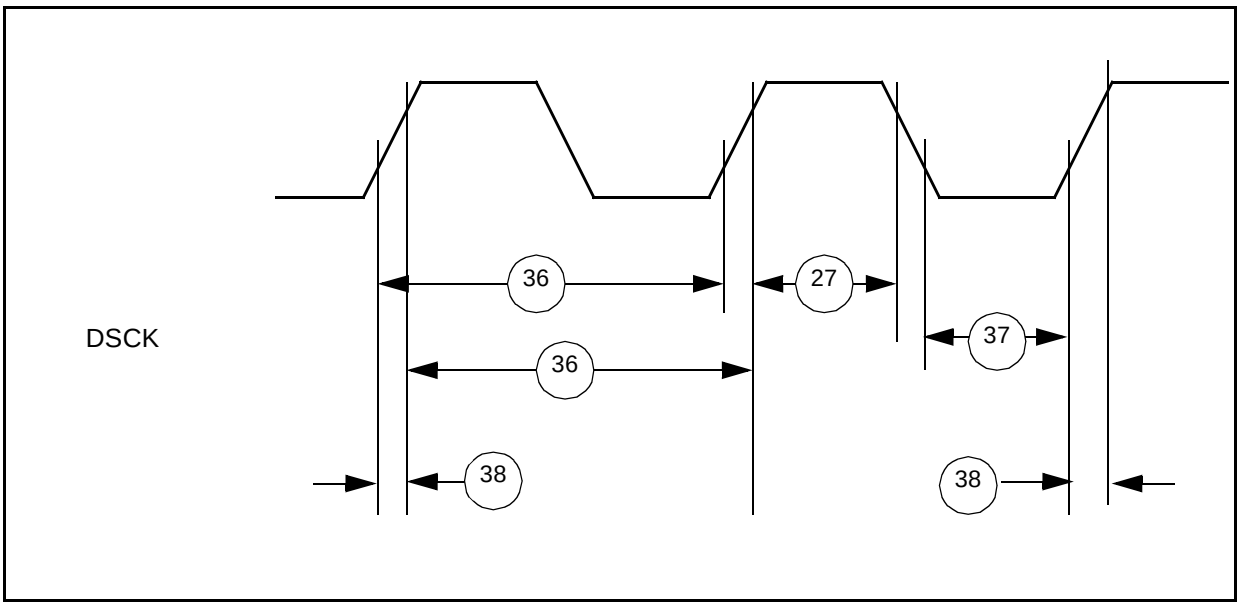


Figure G-20 Debug Port Clock Input Timing

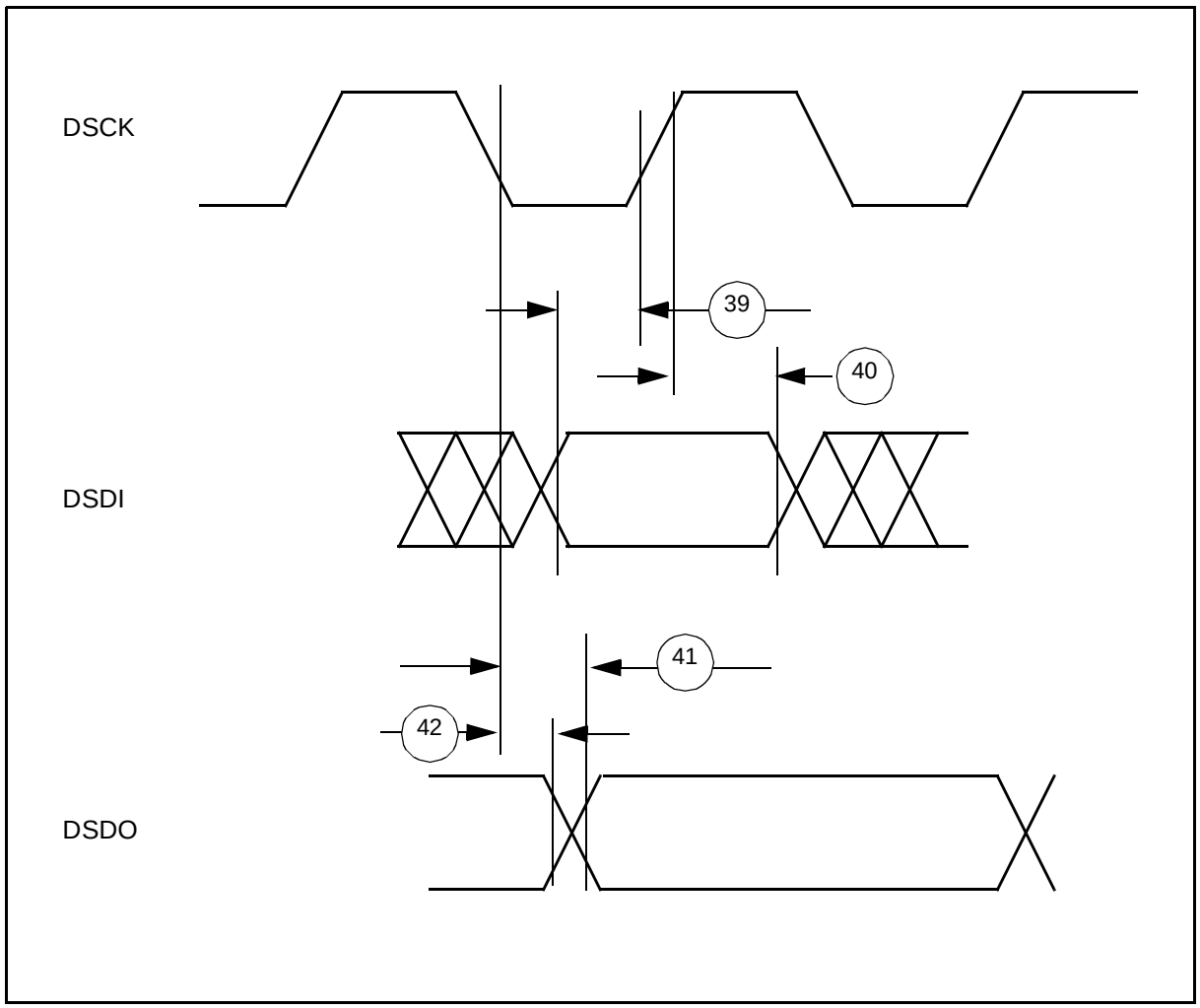


Figure G-21 Debug Port Timings

G.14 Reset Timing

Table G-14 RESET Timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
43	CLKOUT to HRESET High Impedance			20		20	ns
44	CLKOUT to SRESET High Impedance			20		20	ns
45	RSTCONF Pulse Width	17*TC	515		425		ns
46	Configuration Data to HRESET Rising Edge Setup Time	15*TC + TCC	463		382		ns
47	Configuration Data to RSTCONF Rising Edge Set Up Time	15*TC + TCC	463		382		ns
48	Configuration Data Hold Time After RSTCONF Negation		0		0		ns
49	Configuration Data Hold Time After HRESET Negation		0		0		ns
49a	RSTCONF Hold Time After HRESET Negation[1]		60		50		ns
50	HRESET and RSTCONF Asserted to Data Out Drive		25		25		ns
51	RSTCONF Negated to Data Out High Impedance.		25		25		ns
52	CLKOUT of Last Rising Edge Before Chip Tristates HRESET to Data Out High Impedance.		25		25		ns
53	DSDI, DSCK Set Up	3*TC	91		75		ns
54	DSDI, DSCK hold time		0		0		ns
55	SRESET Negated to CLKOUT Rising Edge for DSDI and DSCK Sample	8*TC	243		200		ns
55a	HRESET, SRESET, PORESET Pulse Width [2]		100		100		ns

NOTES:

1. Weak pullups and pulldowns used for Reset timing will comply with the 130 µA mode select current outlined in **Table G-4**.The simplest way to insure meeting this requirement in systems that require the use of the TEXP function, is to connect RSTCONF/TEXP to SRESET. The maximum rise time of HRESET should be less than six clock cycles.
2. HRESET, SRESET and PORESET have a glitch detector to ensure that spikes less than 20 ns are rejected. The internal HRESET, SRESET and PORESET will assert only if these signals are asserted for more than 100 ns.

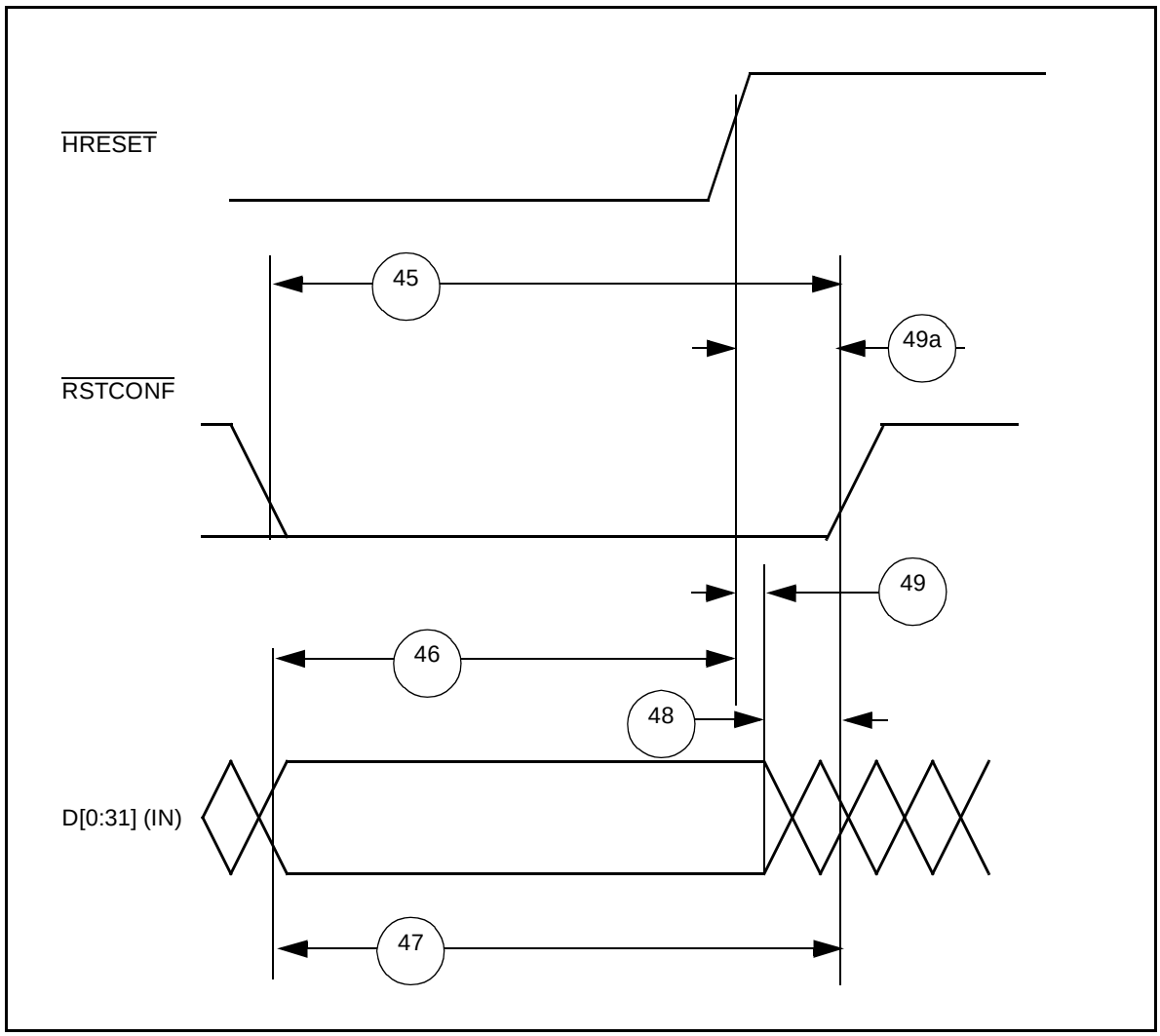


Figure G-22 Reset Timing — Configuration from Data Bus

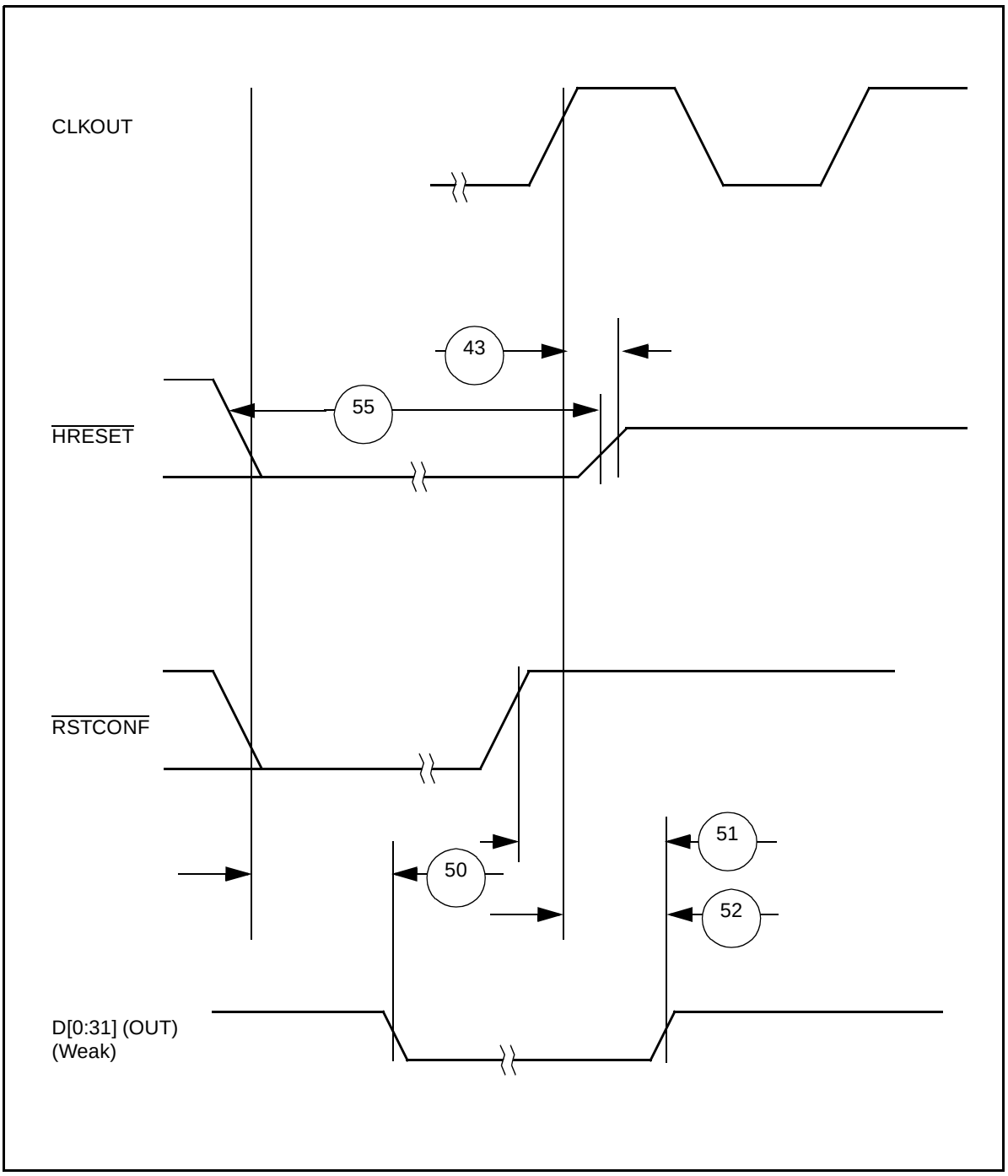


Figure G-23 Reset Timing — Data Bus Weak Drive During Configuration

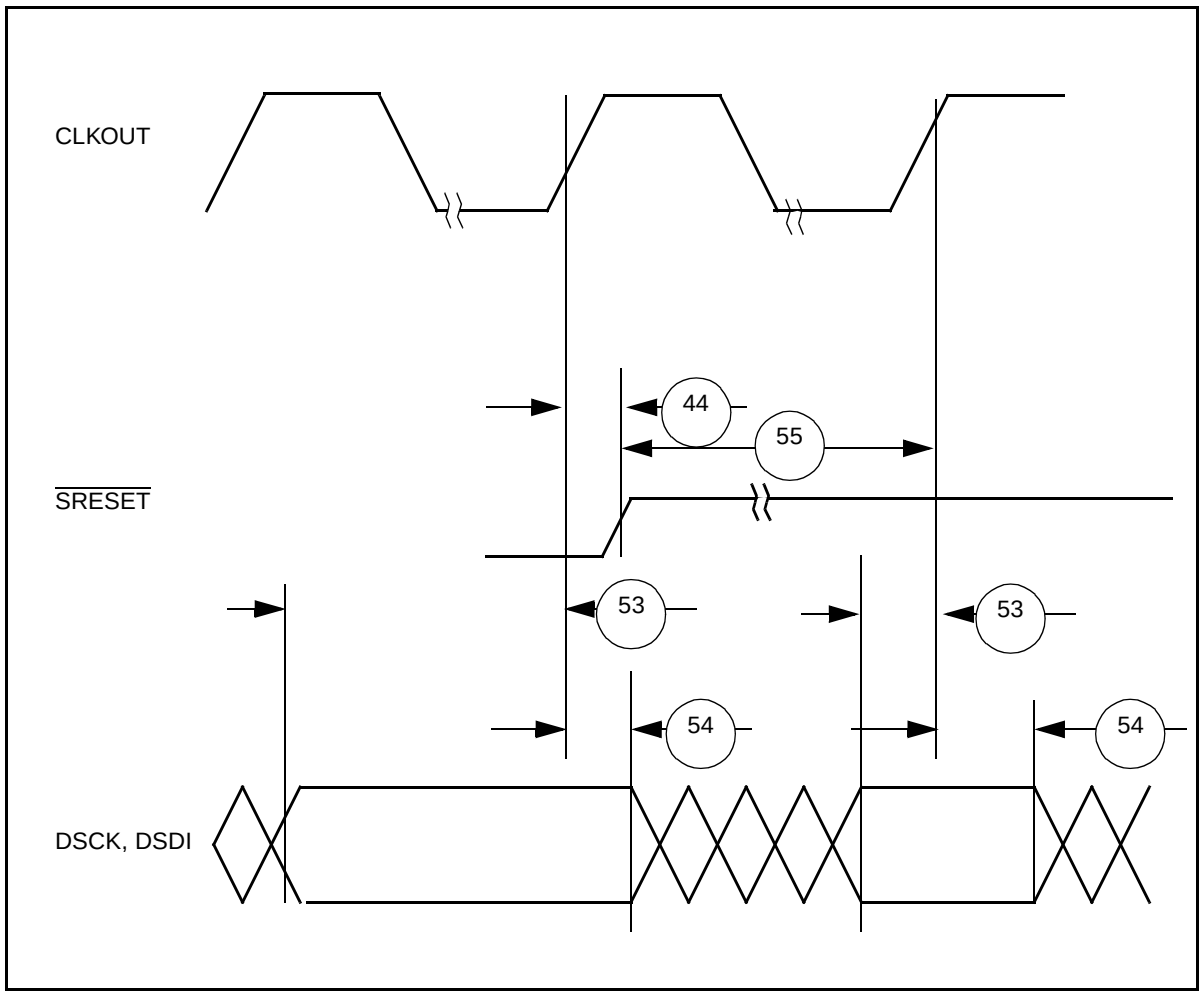


Figure G-24 Reset Timing — Debug Port Configuration

Table G-15 JTAG Timing[1]

($T_A = T_L$ to T_H)

	Characteristic	Expression	33 MHz		40 MHz		Unit
			Min	Max	Min	Max	
56	TCK Cycle Time		100	—	100	—	ns
57	TCK Clock Pulse Width Measured at $V_{DD}/2$		40	—	40	—	ns
58	TCK Rise and Fall Times		0	10	0	10	ns
59	TMS, TDI Data Setup Time		5	—	5	—	ns
60	TMS, TDI Data Hold Time		25	—	25	—	ns
61	TCK Low to TDO Data Valid		—	20	—	20	ns
62	TCK Low to TDO Data Invalid		0	—	0	—	ns
63	TCK Low to TDO High Impedance		—	20	—	20	ns
64	$\overline{\text{TRST}}$ Assert Time		100	—	100	—	ns
65	$\overline{\text{TRST}}$ Setup Time to TCK Low		40	—	40	—	ns
66	TCK Falling Edge to Output Valid		—	50	—	50	ns
67	TCK Falling Edge to Output Valid out of High Impedance		—	50	—	50	ns
68	TCK Falling Edge to Output High Impedance		—	50	—	50	ns
69	Boundary Scan Input Valid to TCK Rising Edge		50	—	50	—	ns
70	TCK Rising Edge to Boundary Scan Input Invalid		50	—	50	—	ns

NOTES:
1. JTAG timing is only tested at 10 MHz

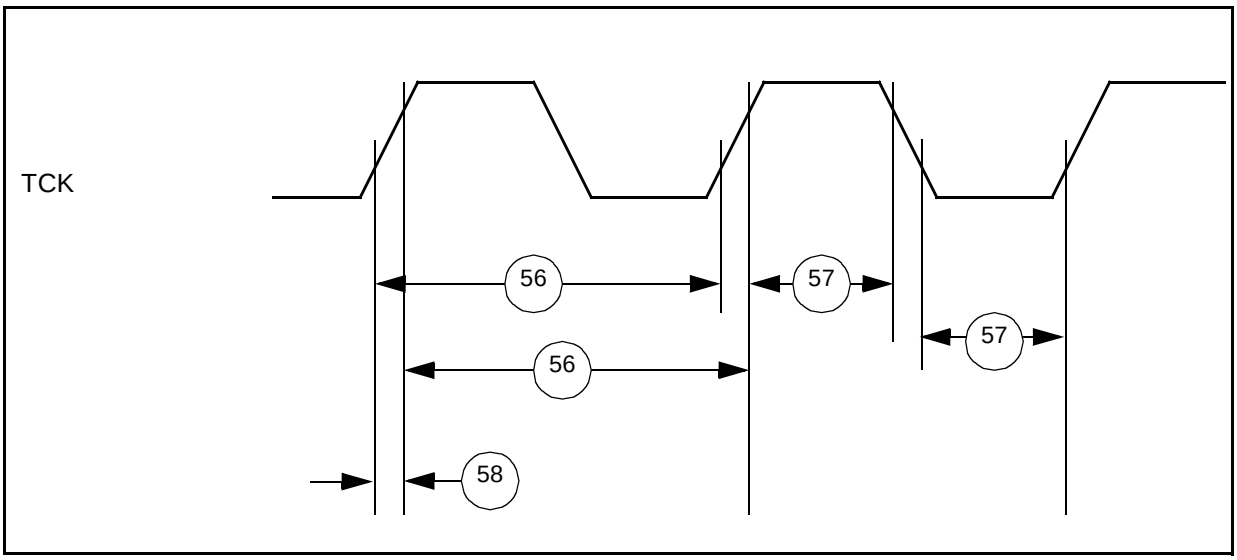


Figure G-25 JTAG Test Clock Input Timing

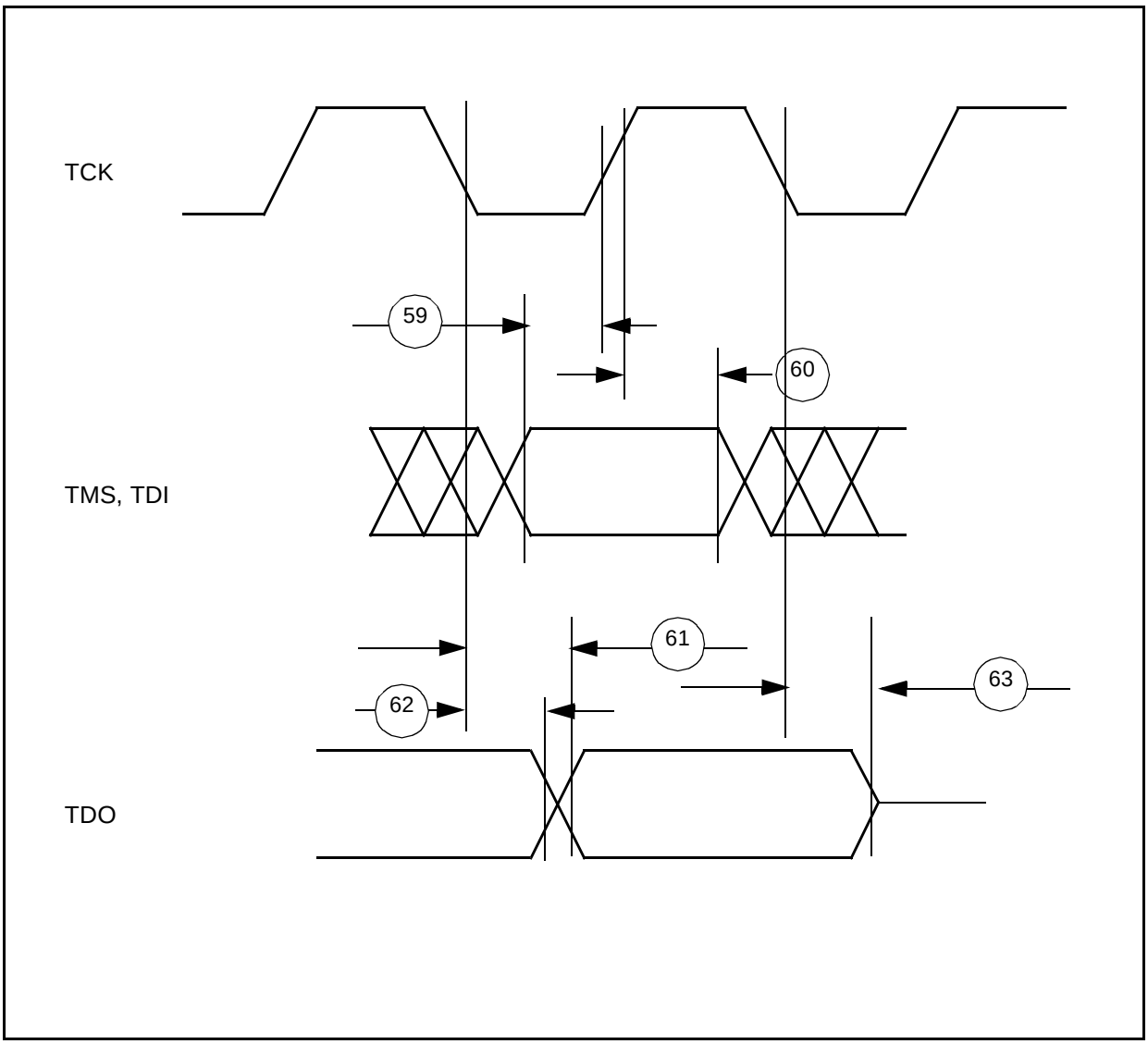


Figure G-26 JTAG — Test Access Port Timing Diagram

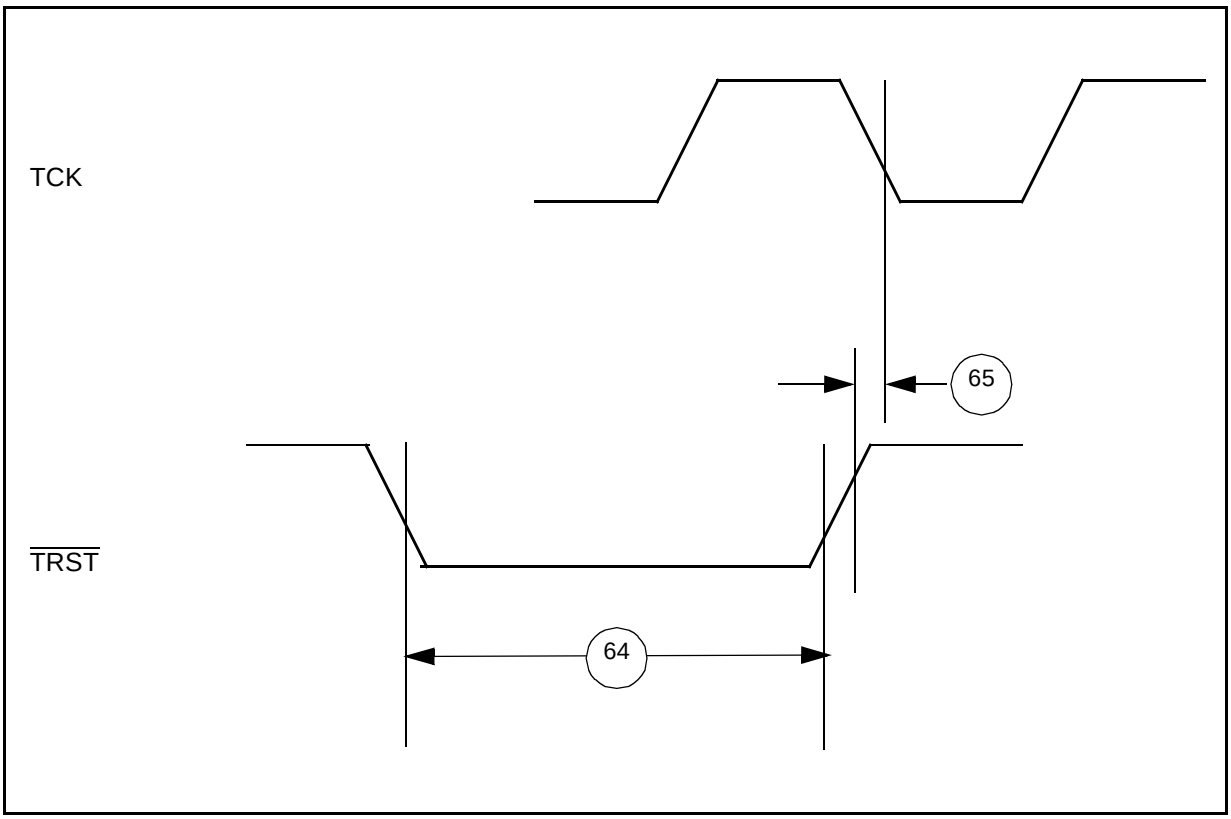


Figure G-27 JTAG — $\overline{\text{TRST}}$ Timing Diagram

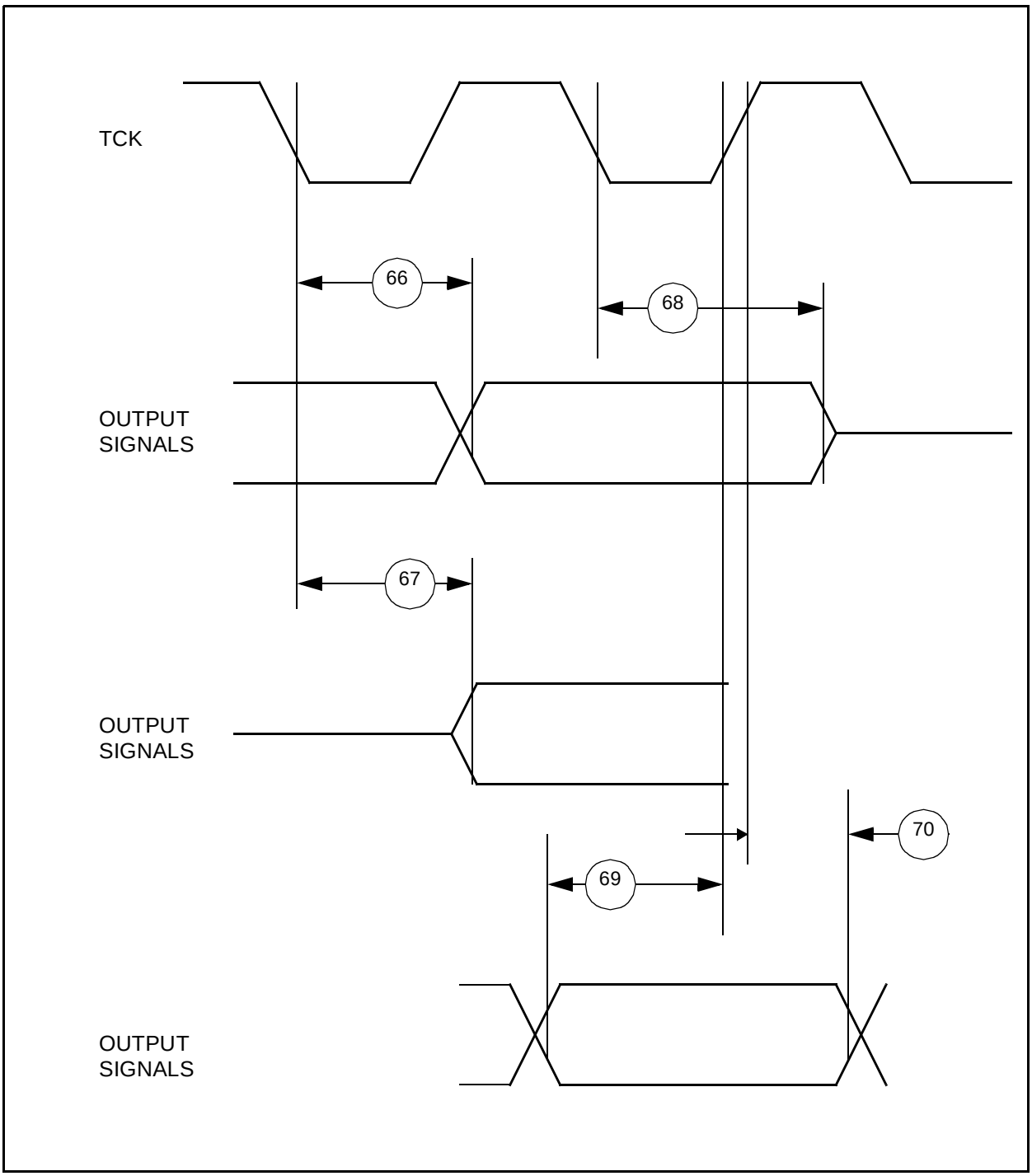


Figure G-28 Boundary Scan (JTAG) Timing Diagram

Table G-16 QADC64 Conversion Characteristics (Operating)

($T_A = T_L$ to T_H)

Num	Parameter	Symbol	Min	Max	Units
97	QADC Clock (QCLK) Frequency[1]	F_{QCLK}	0.5	3.0	MHz
98	Conversion Cycles[2]	CC	14	28	QCLK cycles
99	Conversion Time[3] F_{QCLK} = 2.0 MHz[1,4] Min = CCW/IST = 0b00 Max = CCW/IST = 0b11	T_{CONV}	7.0	14.0	µs
100	Stop Mode Recovery Time	T_{SR}	—	10	µs
101	Resolution[5]	—	5	—	mV
102	Absolute (Total Unadjusted) Error[6, 7, 8, 9] F_{QCLK} = 2.0 MHz[3], 2 Clock Input Sample Time	AE	-2.0	2.0	Counts
103	DC Disruptive Input Injection Current[10, 11, 12, 13, 14]	I_{INJ}[15] I_{INJ}[16]	-3 -1	3 1	mA
104	Current Coupling Ratio[17] PQA PQB	K	— —	$8x10^{-5}$ $8x10^{-5}$	
105	Incremental Error Due to Injection Current All Channels Have Same 10 KΩ < Rs < 100 KΩ Channel Under Test has Rs = 10 KΩ, I_{INJ} = ±3 mA	E_{INJ}		±1.0 ±1.0	Counts
106	Source Impedance At Input [18]	R_S	—	100	KΩ
107	Incremental Capacitance During Sampling [19]	C_{SAMP}	—	5	pF

NOTES:

1. Conversion characteristics vary with F_{QCLK} rate. Reduced conversion accuracy occurs at max F_{QCLK} rate.
2. The number of conversion cycles is dependent on the IST bits in the CCW register.
3. Assumes that f_{SYS} = 40 MHz
4. Assumes F_{QCLK} = 2.00 MHz, with clock prescaler values of:
   QACR0: PSH =0b01111, PSA = 0b0, PSL = 0b011)
   CCW: BYP = 0b0
5. At $V_{RH} - V_{RL}$ = 5.12 V, one count = 5 mV (at 5.0 V, one count = 4.8875 mV).
6. Accuracy tested and guaranteed at $V_{RH} - V_{RL}$ = 5.0 V ± 0.5 V
7. This parameter is periodically sampled rather than 100% tested.
8. Absolute error includes 1/2 count (~2.5 mV) of inherent quantization error and circuit (differential, integral, and offset) error. Characteristic assumes that adequate low-pass filtering is present on analog input pins — capacitive filter with 0.01 µF to 0.1 µF capacitor between analog input and analog ground, typical source isolation impedance of 10 Kbytes.
9. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals may affect the conversion accuracy of other channels.
10. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} <= V_{DDA}$ and $V_{RL} <= V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
11. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

12. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP}$ = (the lower of V_{DDA} or V_{DDH}) + 0.3 V and $V_{NEGCLAMP}$ = -0.3 V, then use the larger of the calculated values. The diode drop voltage is a function of current and varies approximately 0.4 to 0.8 volts over temperature
13. This parameter is periodically sampled rather 100% tested.
14. Derate linearly to 0.3 mA if V_{DDH} - V_{DDA} = 1 volt. This characteristic is preliminary and may change after further characterization.
15. Condition applies to two adjacent pins.
16. Condition applies to all analog channels.
17. Current coupling ratio, K, is defined as the ratio of the output current, I_{out}, measured on the pin under test to the injection current, I_{inj}, when both adjacent pins are overstressed with the specified injection current. $K = I_{out} / I_{inj}$ The input voltage error on the channel under test is calculated as $V_{err} = I_{inj} * K * R_S$
18. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.
    Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{errj}):
    $V_{errj} = R_S * I_{OFF}$
    where I_{OFF} is a function of operating temperature.
    Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the filtering capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance
19. For a maximum sampling error of the input voltage <= 1LSB, then the external filter capacitor, C_f >= 1024 * C_{SAMP}. The value of C_{SAMP} in the new design may be reduced.

G.17 QSMCM Electrical Characteristics

Table G-17 QSPI Timing

($T_A = T_L$ to T_H, 50 pF load on all QSPI pins except as noted)

Name	Function	Symbol	Min	Max	Unit
108	Operating Frequency[1] Master Slave	f_{op}	 DC DC	 $F_{SYS}/4$ $F_{SYS}/4$	Hz
109	Cycle Time Master Slave	t_{qcyc}	 4*TC 4*TC	 510*TC[2] —	ns
110	Enable Lead Time Master Slave	t_{lead}	 2*TC 2*TC	 128*TC —	ns
111	Enable Lag Time Master Slave	t_{lag}	 — 2*TC	 SCK/2 —	ns
112	Clock (SCK) High or Low Time Master Slave[3]	t_{sw}	 2*TC – 60 2*TC – n	 255*TC —	ns
113	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	 17*TC 13*TC	 8192*TC —	ns
114	Data Setup Time (Inputs) Master Slave	t_{su}	 30 20	 — —	ns

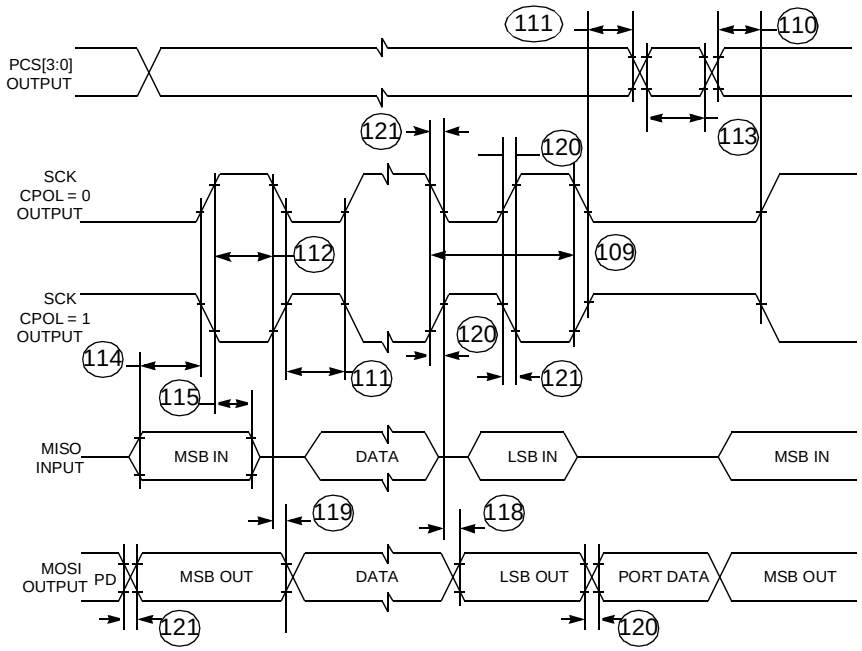
Table G-17 QSPI Timing (Continued)

($T_A = T_L$ to T_H, 50 pF load on all QSPI pins except as noted)

Name	Function	Symbol	Min	Max	Unit
115	Data Hold Time (Inputs) Master Slave	t_{hi}	 0 20	 — —	ns
116	Slave Access Time	t_a	—	TC	ns
117	Slave MISO Disable Time	t_{dis}	—	2*TC	ns
118	Data Valid (After SCK Edge) Master Slave	t_v	 — —	 50 50	ns
119	Data Hold Time (Outputs) Master Slave	t_{ho}	 0 0	 — —	ns
120	Rise Time Input Output up to 50 pF Load, SLRC Bit of PDMCR = “0” up to 200 pF Load, SLRC Bit of PDMCR = “0” up to 50 pF, SLRC Bit of PDMCR = “1”	 t_{ri} t_{ro}	 — 10 20 2	 1 50 100 25	 µs ns ns ns
121	Fall Time Input Output up to 50 pF Load, SLRC Bit of PDMCR = “0” up to 200 pF Load, SLRC Bit of PDMCR = “0” up to 50 pF, SLRC Bit of PDMCR = “1”	 t_{fi} t_{fo}	 — 10 20 2	 1 50 100 25	 µs ns ns ns

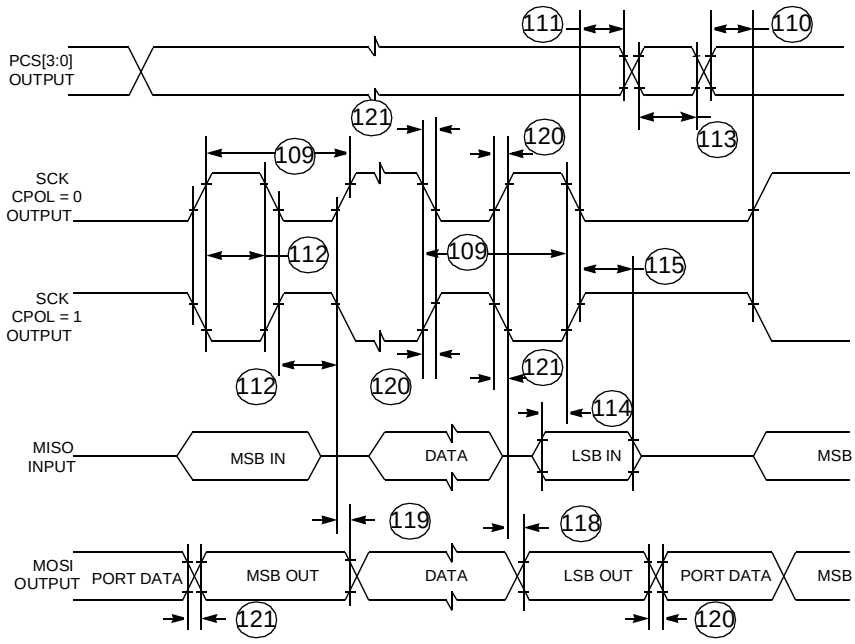
NOTES:

1. All AC timing is tested to the 5-V levels outlined in **Table G-4**.
2. TC is defined to be the clock period of f_{SYS} (IMB Clock).
3. For high time, n = External SCK rise time; for low time, n = External SCK fall time.



QSPI MAST CPHA0

Figure G-29 QSPI Timing — Master, CPHA = 0



QSPI MAST CPHA1

Figure G-30 QSPI Timing — Master, CPHA = 1

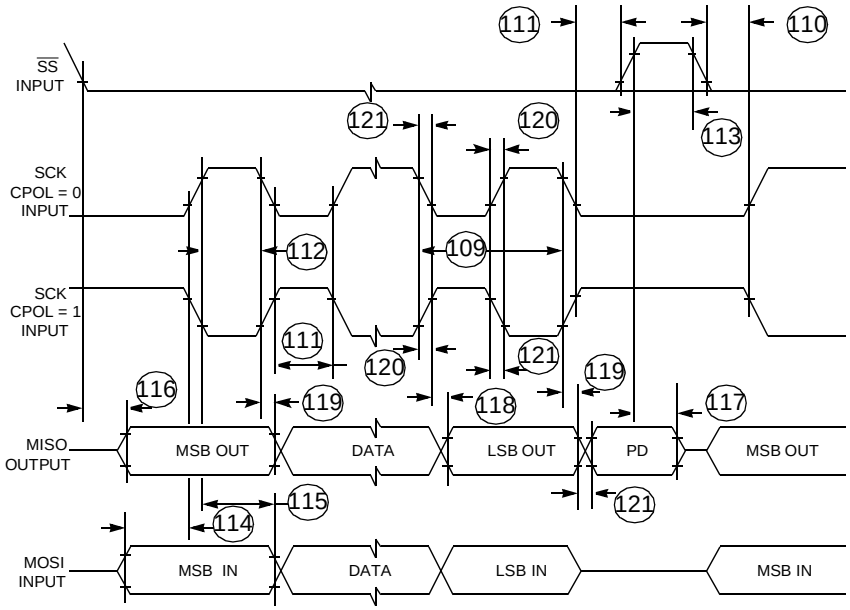


Figure G-31 QSPI Timing — Slave, CPHA = 0

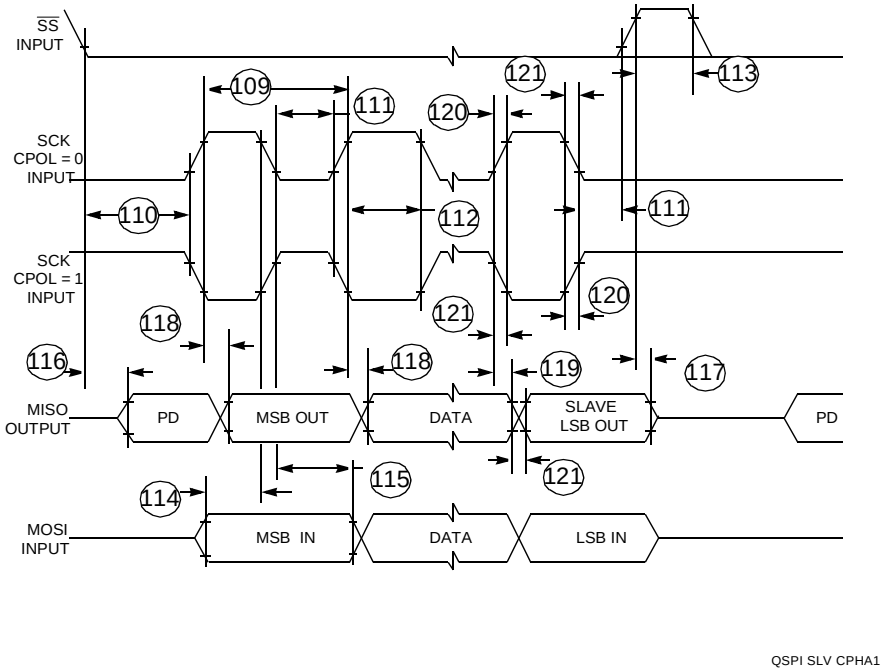


Figure G-32 QSPI Timing — Slave, CPHA = 1

G.18 GPIO Electrical Characteristics

Table G-18 GPIO Timing[1]

($T_A = T_L$ to T_H)

Num	Rating	Symbol	Min	Max	Unit
122	Rise Time Input Output[2] (SLR0 of PDMCR = 0), 50 pF to 200 pF Load Output[2] (SLR0 of PDMCR = 0), up to 20 nF Load[3] Output (SLR0 of PDMCR = 1), up to 50 pF Load	t_{ri} t_{ro}	— 90 2000 3	1 600 7500 25	µs ns ns ns
123	Fall Time Input Output[2](SLR0 of PDMCR = 0), 50 pF to 200 pF Load Output[2] (SLR0 of PDMCR = 0), up to 20 nF Load[3] Output (SLR0 of PDMCR = 1), up to 50 pF Load	t_{fi} t_{fo}	— 90 2000 3	1 600 7500 25	µs ns ns ns

NOTES:

1. GPIO applies to all pins used as GPIO: SGPIOA[8:31], SQPIOD[0:31], SGPIOC[0:7], QGPIO[0:6], QGPO[1:2], MPIO[0:15], A_PQA[0:7], B_PQA[0:7], A_PQB[0:7] (inputs only), B_PQB[0:7] (inputs only).
2. This parameter is tested during initial characterization and is not tested in production.
3. Care should be taken to insure that the total power dissipation of the device remain below the absolute maximum rating under this condition. See **Table G-1**. With a capacitive load > 20 nF (up to 100 nF maximum), the user must insure that the pin is always configured as an output and set to slow slew rate mode (SLR0 of PDMCR = 0). Do not change SLR0 of PDMCR to a 1 under these conditions.

G.19 TPU3 Electrical Characteristics

Table G-19 TPU3 Timing

($T_A = T_L$ to T_H)

Num	Rating	Symbol	Min	Max	Unit
124	Slew Rate of TPU Output Channel Valid[1,2] (SLR0 of PDMCR = 0, 50 pF to 200 pF Load) (SLR0 of PDMCR = 0, up to 20 nF Load)[3] (SLR0 of PDMCR = 1, up to 50 pF Load)	t_{CHTOV}	92 2000 3	650 7550 25	ns
125	CLKOUT High to TPU Output Channel Hold	t_{CHTOH}	0	15	ns
126	TPU Input Channel Pulse Width[4]	t_{TIPW}	4	—	t_{cyc}

NOTES:

1. AC timing is shown with respect to 10% V_{DDH} and 90% V_{DDH} levels. Total slew rate from 0 to V_{DDH} will be larger.
2. Timing not valid for external T2CLK input.
3. Care should be taken to insure that the total power dissipation of the device remain below the absolute maximum rating under this condition. See **Table G-1**. With a capacitive load > 20 nF, the user must insure that the pin is always configured as an output.
4. t_{cyc} is defined as the IMB Clock Period.

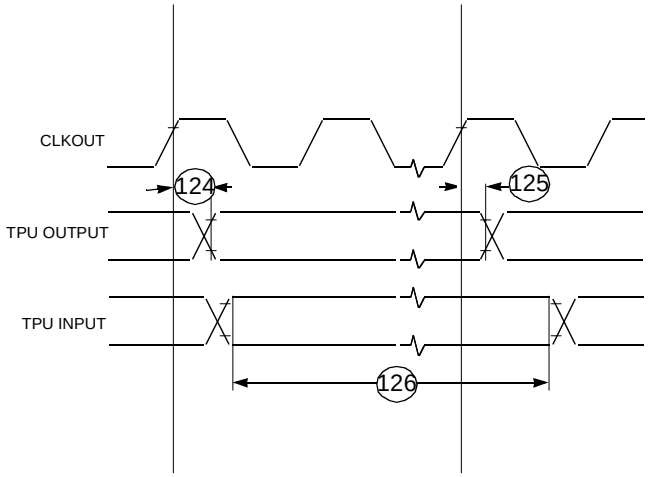


Figure G-33 TPU3 Timing

G.20 TouCAN Electrical Characteristics

Table G-20 TouCAN Timing[1]

($T_A = T_L$ to T_H)

Num	Rating	Symbol	Min	Max	Unit
127	CNTX0 (Delay from ICLOCK)	t_{CNTX0}	19	—	ns
128	CNRX0 (Set-Up to ICLOCK Rise)	t_{CNRX0}	0	—	ns
129	Rise Time Input Output Up to 50 pF Load, SLRC Bit of PDMCR = “0” Up to 200 pF Load, SLRC Bit of PDMCR = “0” Up to 50 pF Load, SLRC Bit of PDMCR = “1”	 t_{ri} t_{ro}	 — 10 20 2	 1 50 100 25	 µs ns ns ns
130	Fall Time Input Output Up to 50 pF Load, SLRC Bit of PDMCR = “0” Up to 200 pF Load, SLRC bit of PDMCR = “0” Up to 50 pF Load, SLRC Bit of PDMCR = “1”	 t_{fi} t_{fo}	 — 10 20 2	 1 50 100 25	 µs ns ns ns
	Serial Pins	t_f	—	1	Mhz

NOTES:
1. AC timing is shown is tested to the 5-V levels outlined in **Table G-4**.

G.21 MIOS Timing Characteristics

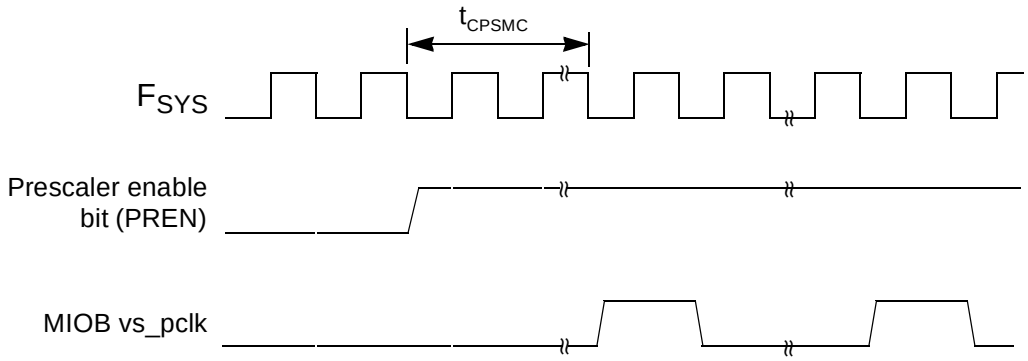
All MIOS output pins are slew rate controlled. Slew rate control circuitry adds 90 ns as minimum to the output timing and 650 ns as a maximum. This slew rate is from 10% V_{DDH} to 90% V_{DDH}, an additional 100 ns should be added for total 0 to V_{DDH} slew rate.

Table G-21 MCPSM Timing Characteristics

Characteristic	Symbol	Delay	Unit
MCPSM Enable to vs_pclk Pulse[1]	t_{CPSMC}	(MCPSMSCR_PSL[3:0]) -1[2]	IMB Clock Cycles

NOTES:

1. The MCPSM clock prescaler value (MCPSMSCR_PSL[3:0]) should be written to the MCPSMSCR (MCPSM status/control register) before rewriting the MCPSMSCR to set the enable bit (MCPSMSCR_PREN). If this is not done the prescaler will start with the old value in the MCPSMSCR_PSL[3:0] before reloading the new value into the counter.
   vs_pclk is the MIOS prescaler clock which is distributed to all the counter (e.g., MPWMSM and MMCSM) submodules.
2. After reset MCPSMSCR_PSL[3:0] is set to 0b0000.



Note 1: f_{SYS} is the internal IMB clock for the IMB3 bus.
Note 2: The numbers associated with the f_{SYS} ticks refer to the IMB3 internal state.
Note 3: vs_pclk is the MIOS prescaler clock which is distributed around the MIOS to counter modules such as th MMCSM and MPWMSM.

Figure G-34 MCPSM Enable to vs_pclk Pulse Timing Diagram

G.21.1 MPWMSM Timing Characteristics

Table G-22 MPWMSM Timing Characteristics

(All delays are in IMB clock periods)

Characteristic	Symbol	Min	Max
PWMSM Output Resolution	t_{PWMR}	– [1]	2.0 [2]
PWM Output Pulse[3]	t_{PWMO}	2.0	—
mpwmi Input Pin to MPWMSCR_PIN Status Set	t_{PIN}	1	2
CPSM Enable To Output Set[4]	t_{PWMP}	(MPWMPERR – MPWMPULR+ 1) * (256 – MPWMSCR_CP) * MCPSMSCR_PSL +1	
MPWMSM Enable to Output Set (MIN)[5]	t_{PWME}	(MPWMPERR – MPWMPULR) * (256 – MPWMSCR_CP) * MCPSMSCR_PSL +3 + (255 – MPWMSCR_CP) * MCPSMSCR_PSL [6]	
MPWMSM Enable to Output Set (MAX)[5]	t_{PWME}	t_{PWME}(MIN) + MCPSMSCR_PSL – 1 [6]	
Interrupt Flag to Output Pin Reset (Period Start)[7]	t_{FLGP}	(256 – MPWMSCR_CP) * MCPSMSCR_PSL – 1 [6]	

NOTES:

1. Minimum output resolution depends on MPWMSM and MCPSM prescaler settings.
2. Maximum resolution is obtained by setting CPSMPSL[3:0] =0x2 and MPWMSCR_CP[7:0] =0xFF.
3. Excluding the case where the output is always “0”.
4. With MPWMSM enabled before enabling the MCPSM. Please also see Note *1 on the MCPSM timing information.
5. The exact timing from mpwmsm enable to the pin being set depends on the timing of the register write and the MCPSM vs_pclk.
6. When MCPSMSCR_PSL = 0x0000, this gives a prescale value of 16 and it is 16 which should be used in these calculations. When MCPSMSCR_PSL = 0x0001, the CPSM is inactive.
7. Note: the interrupt is set before the output pin is reset (Signifying the start of a new period).

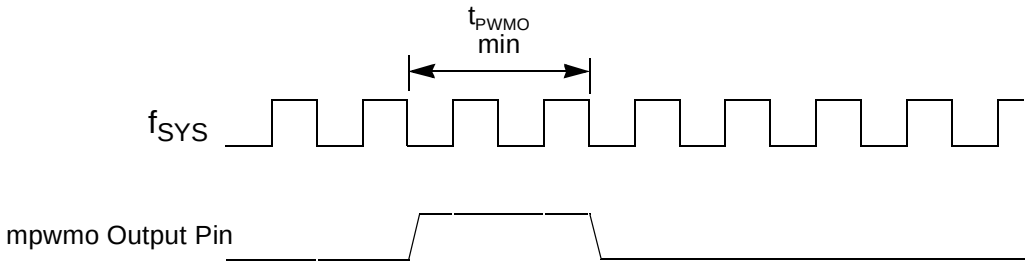
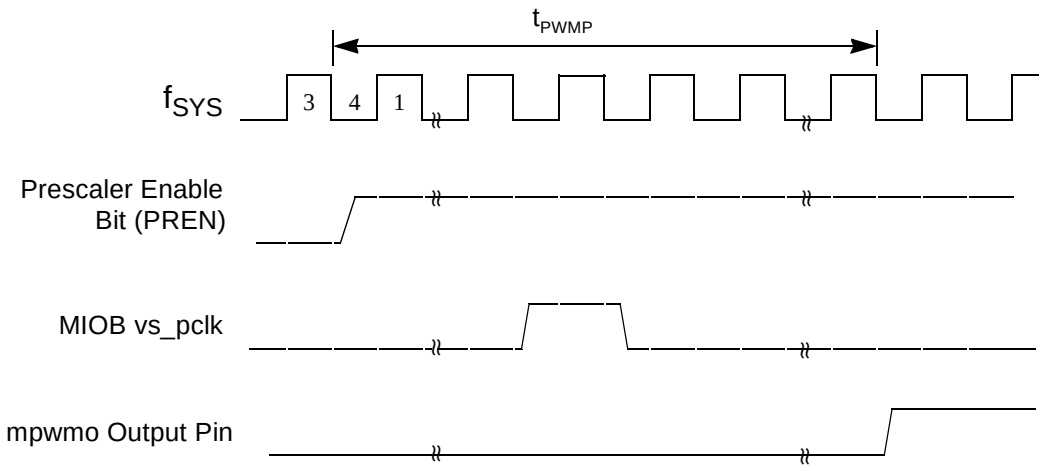


Figure G-35 MPWMSM Minimum Output Pulse Example Timing Diagram



Note: F_{SYS} is the internal IMB clock for the IMB3 bus.

Figure G-36 MCPSM Enable to MPWMO Output Pin Rising Edge Timing Diagram

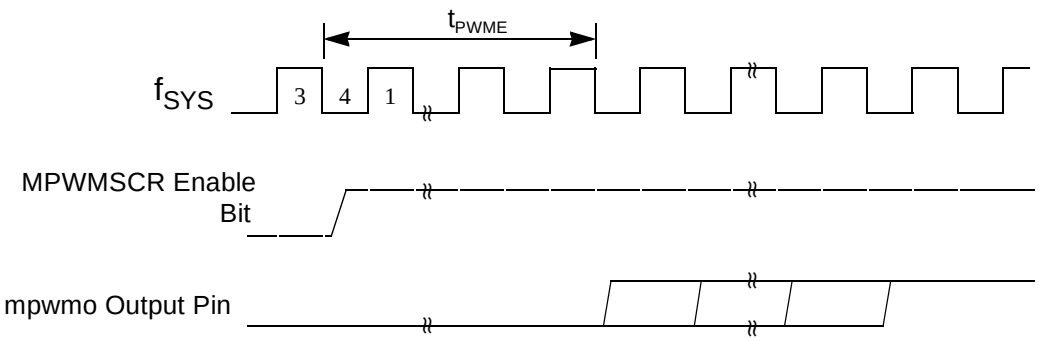


Figure G-37 MPWMSM Enable to MPWMO Output Pin Rising Edge Timing Diagram

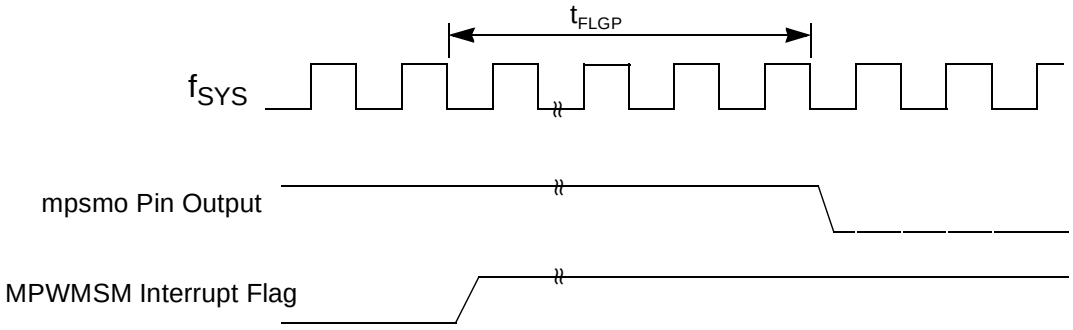


Figure G-38 MPWMSM Interrupt Flag to MPWMO Output Pin Falling Edge Timing Diagram

G.21.2 MMCSM Timing Characteristics

Table G-23 MMCSM Timing Characteristics

(All delays are in IMB clock periods.)

Characteristic	Symbol	Min	Max
MMCSM Input Pin Period	t_{PPER}	4	—
MMCSM Pin Low Time	t_{PLO}	2	—
MMCSM Pin High Time	t_{PHI}	2	—
Clock Pin to Counter Bus Increment	t_{PCCB}	1	2
Load Pin to New Counter Bus Value	t_{PLCB}	1	2
Clock Pin to PINC Delay	t_{PINC}	1	2
Load Pin to PINL Delay	t_{PINL}	1	2
Counter Bus Resolution	t_{CBR}	–[1]	2^2
Counter Bus Overflow Reload to Interrupt Flag	t_{CBFLG}	1	
MCPSM Enable to Counter Bus Increment	t_{MCMP}	(256 – MMCSMSCR_CP) * MCPSMSCR_PSL + 2^3	
MMCSM Enable to Counter Bus Increment (MIN)[4]	t_{MCME}	4 + MCPSMSCR_PSL* (255 – MMCSMSCR_CP)^3	
MMCSM Enable to Counter Bus Increment (MAX)[4]	t_{MCME}	4 + MCPSMSCR_PSL * (255 – MMCSMSCR_CP) + (MCPSMSCR_PSL – 1)^3	

NOTES:

1. Minimum output resolution depends on MMCSM and MCPSM prescaler settings.
2. Maximum resolution is obtained by setting CPSMPSL[3:0] = 0x2 and MMCSMSCR_CP[7:0] = 0xFF.
3. When MCPSMSCR_PSL = 0x0000, this gives a prescale value of 16 and it is 16 which should be used in these calculations. When MCPSMSCR_PSL = 0x0001, the CPSM is inactive.
4. The exact timing from MMCSM enable to the pin being set depends on the timing of the MMCSMSCR register write and the MCPSM vs_pclk. The MMCSM enable is taken to mean the MMCSMSCR_CLS[1:0] being written to 2'b11.

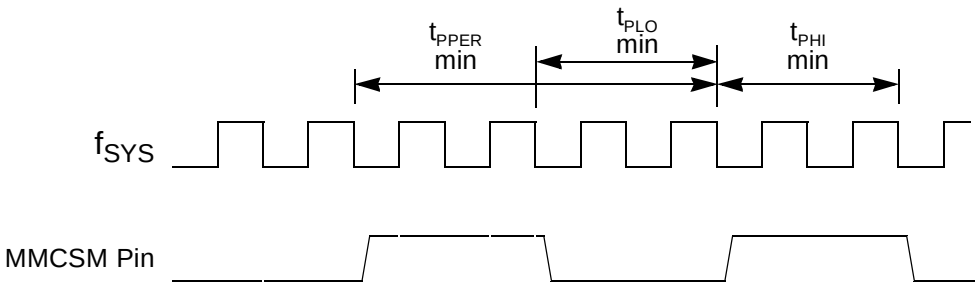
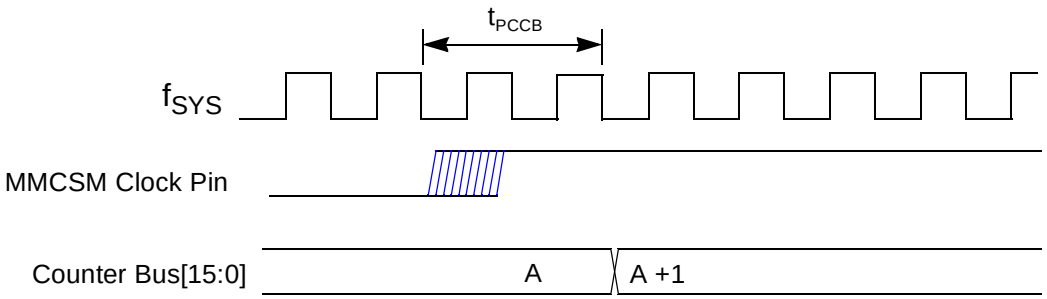


Figure G-39 MMCSM Minimum Input Pin (Either Load or Clock) Timing Diagram



Note: F_{SYS} is the internal IMB clock for the IMB3 bus.

Figure G-40 MMCSM Clock Pin to Counter Bus Increment Timing Diagram

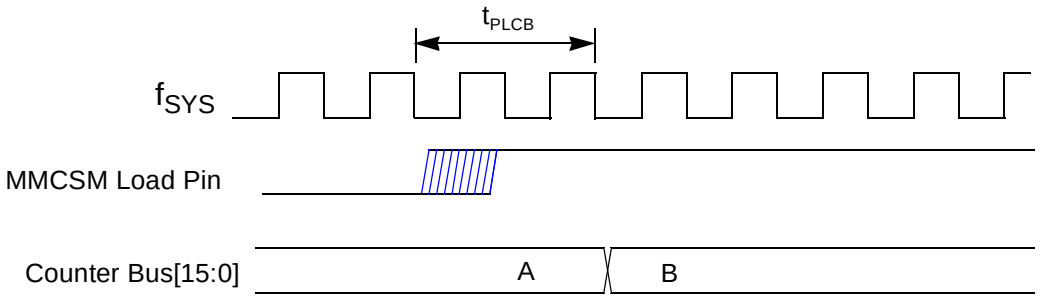


Figure G-41 MMCSM Load Pin to Counter Bus Reload Timing Diagram

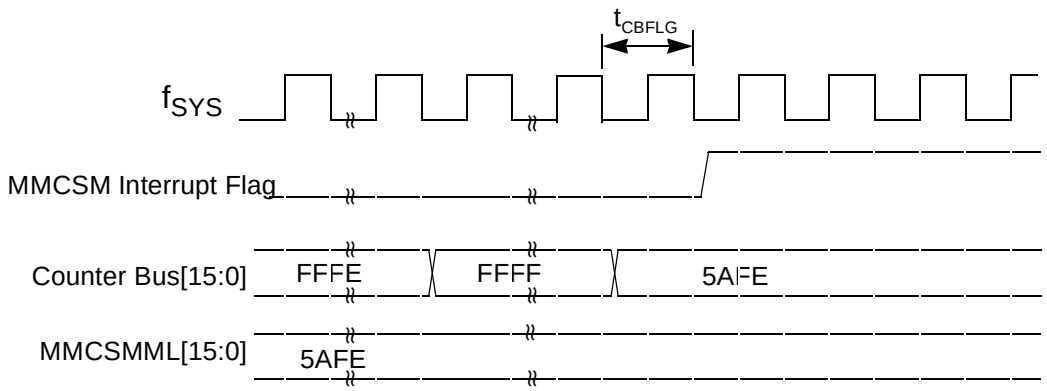


Figure G-42 MMCSM Counter Bus Reload to Interrupt Flag Setting Timing Diagram

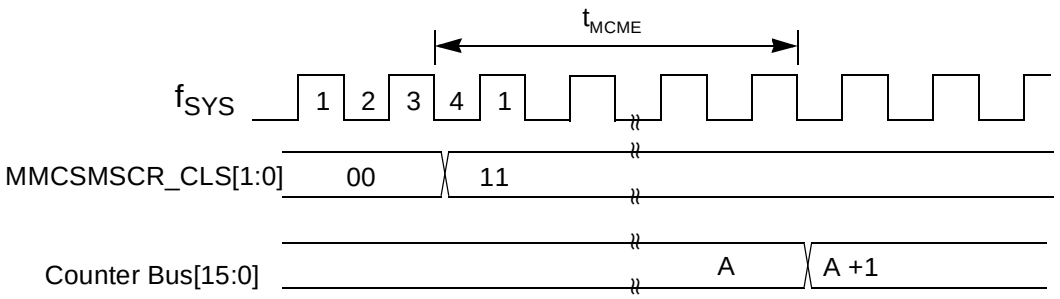


Figure G-43 MMCSM Prescaler Clock Select to Counter Bus Increment Timing Diagram

G.21.3 MDASM Timing Characteristics

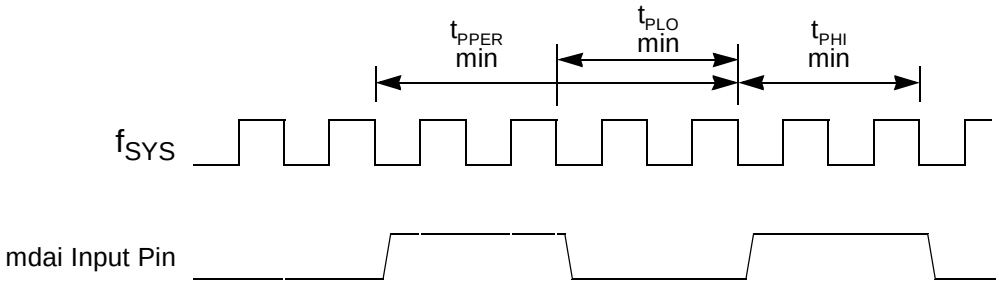
Table G-24 MDASM Timing Characteristics

(All delays are in IMB clock periods.)

Characteristic	Symbol	Min	Max
Input Modes: (IPWM, IPM, IC, DIS)			
MDASM Input Pin Period	t_{PPER}	4	—
MDASM Pin Low Time	t_{PLO}	2	—
MDASM Pin High Time	t_{PHI}	2	—
Input Capture Resolution	t_{CAPR}	—	2
Input Pin to Counter Bus Capture Delay	t_{PCAP}	1	3[1]
Input Pin to Interrupt Flag Delay	t_{PFLG}	2	3
Input Pin to PIN Delay	t_{PIN}	1	2
Counter Bus Resolution	t_{CBR}	—	2[2]
Output Modes: (OC, OPWM)			
Output Pulse Width[3]	t_{PULW}	2	—
Compare Resolution	t_{COMR}	—	2[2]
Counter Bus to Pin Change	t_{CBP}	3	
Counter Bus to Interrupt Flag Set.	t_{CBFLG}	3	

NOTES:

1. If the counter bus capture occurs when the counter bus is changing then the capture is delayed one cycle. In situations where the counter bus is stable when the input capture occurs the t_{PCAP} has a maximum delay of 2 cycles. (the 1 cycle uncertainty is due to the synchronizer).
2. Maximum resolution is obtained by setting CPSMPSL[3:0] = 0x2 and MDASMSCR_CP[7:0] = 0xFF.
3. Maximum output resolution and pulse width depends on counter (e.g., MMCSM) and MCPSM prescaler settings.



f_{SYS} is the internal IMB clock for the IMB3 bus.

Figure G-44 MDASM Minimum Input Pin Timing Diagram

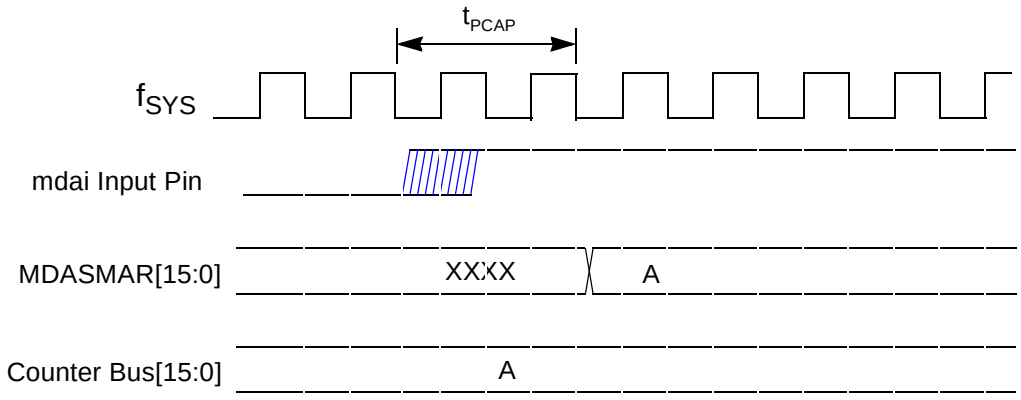


Figure G-45 MDASM Input Pin to Counter Bus Capture Timing Diagram

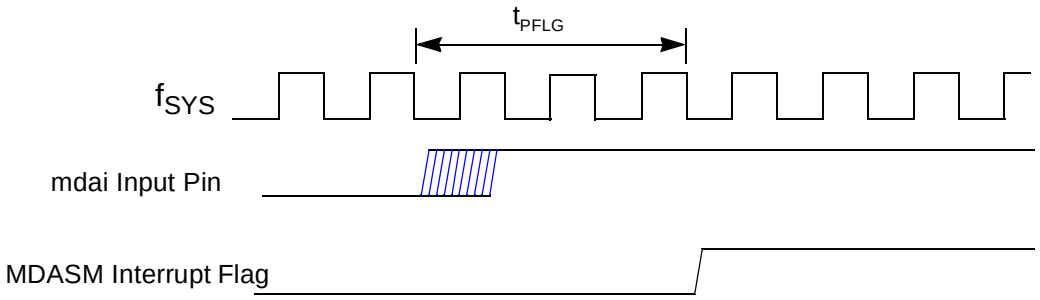


Figure G-46 MDASM Input Pin to MDASM Interrupt Flag Timing Diagram

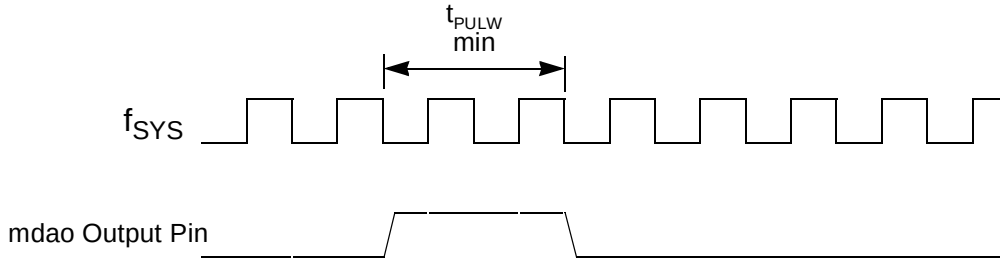


Figure G-47 MDASM Minimum Output Pulse Width

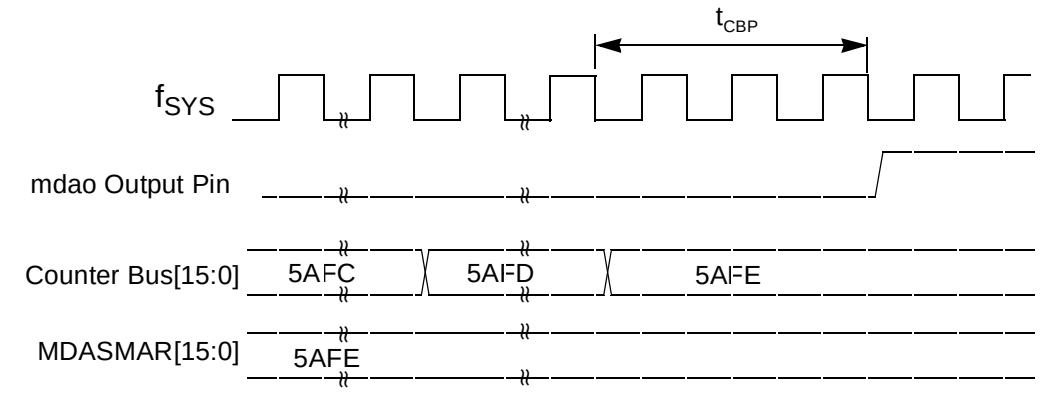


Figure G-48 Counter Bus to MDASM Output Pin Change Timing Diagram

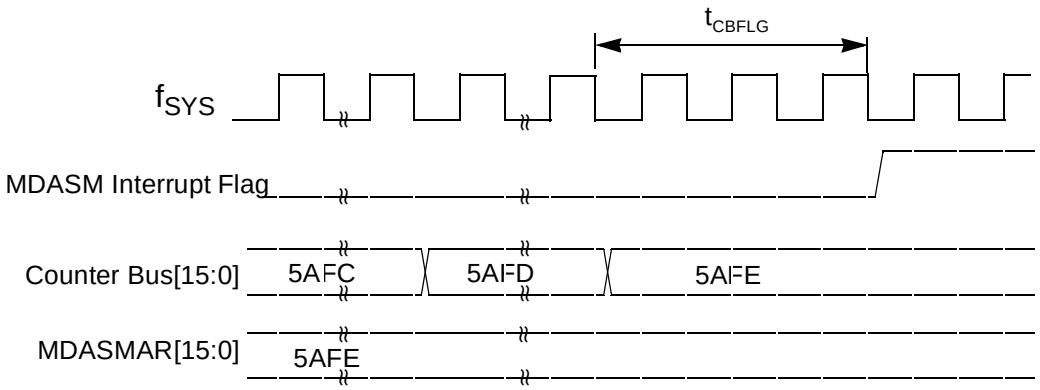


Figure G-49 Counter Bus to MDASM Interrupt Flag Setting Timing Diagram

G.21.4 MPIOSM Timing Characteristics

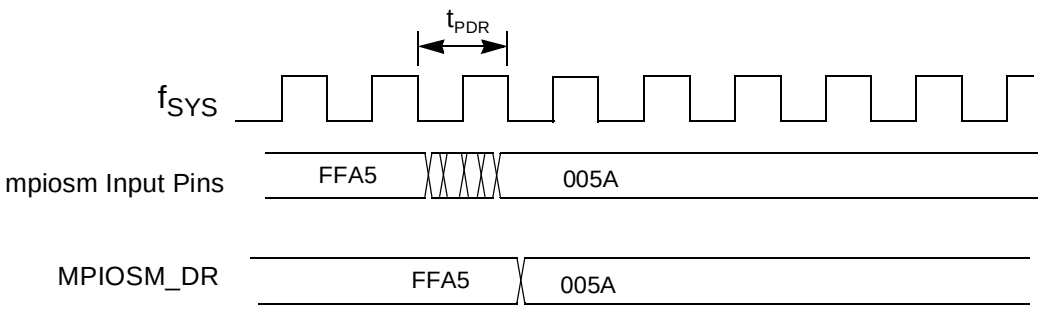
Table G-25 MPIOSM Timing Characteristics

(All delays are in IMB clock periods.)

Characteristic	Symbol	Min	Max
Input Mode			
MPIOSM Input Pin Period	t_{PPER}	—[1]	—
MPIOSM Pin Low Time	t_{PLO}	—[1]	—
MPIOSM Pin High Time	t_{PHI}	—[1]	—
Input Pin to MPIOSM_DR Delay	t_{PDR}	0	1
Output Mode			
Output Pulse Width[2]	t_{PULW}	—[2]	—

NOTES:

1. The minimum input pin period, pin low and pin high times depend on the rate at which the MPIOSM_DR register is polled.
2. The minimum output pulse width depends on how quickly the CPU updates the value inside the MIOPSM_DR register. The MPC555 RCPU core takes six clock cycles to access the MIOPSM_DR register, therefore the minimum output pulse will be 12 IMB clocks.



F_{SYS} is the internal IMB clock for the IMB3 bus.

Figure G-50 MPIOSM Input Pin to MPIOSM_DR (Data Register) Timing Diagram