SECTION 2
SIGNAL DESCRIPTIONS

2.1 Pad Function Description

Table 2-1 shows a summary of the functions of the pads of MPC565 / MPC566. The total signals column (total number of pads) shows the pads on the module used. The pads used column (number of pads used) shows how many pads are bonded out on the MPC565 / MPC566.

Table 2-1 MPC565 / MPC566 Pad Function Summary

Functional Group Description	Signals[1]	Total No. Signals	5 V / 2.6 V
24 Address lines (16 Mbytes address space)	A[8:31] — 24 SGPIO	24	2.6-V BUS/ 5-V GPIO
32-bit data bus	D[0:31] — 32 SGPIO	32	
External Interrupts	IRQ[0] — SGPIOC[0]	1	2.6-V BUS/ 2.6-V GPIO[2]
	IRQ[1] — $\overline{\text{RSV}}$ — SGPIOC[1]	6	2.6-V BUS/ 5-V GPIO
	IRQ[2] — $\overline{\text{CR}}$ — SGPIOC[2] — $\overline{\text{MTS}}$		
	IRQ[3] — $\overline{\text{KR}}$ — $\overline{\text{RETRY}}$ — SGPIOC[3]		
	IRQ[4] — AT[2] — SGPIOC[4]		
	IRQ[6:7] — MODCK[2:3]		
	IRQ[5] — MODCK[1] — SPGIOC[5]	1	2.6 V
Bus Control	TSIZ[0:1], RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, $\overline{\text{BDIP}}$, $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{OE}}$	11	2.6 V
	$\overline{\text{RSTCONF}}$ — TEXP		
	$\overline{\text{BI}}$ — $\overline{\text{STS}}$		
Development and Debug Support	PTR — FRZ — SGPIOC[6]	7	2.6-V BUS/ 5-V GPIO
	IRQ_OUT — LWP[0] — SGPIOC[7]		
	$\overline{\text{BG}}$ — VF[0] — LWP[1]		
	$\overline{\text{BR}}$ — VF[1] — IWP[2]		
	$\overline{\text{BB}}$ — VF[2] — IWP[3]		
	VFLS[0:1] — IWP[0:1]		
Chip Selects	CS[0:3]	4	2.6 V
Write Enables / Byte Enables	$\overline{\text{WE}}$[0:3] — $\overline{\text{BE}}$[0:3] — AT[0:3]	4	2.6 V
Reset Pins	$\overline{\text{PORESET}}$/$\overline{\text{TRST}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	3	2.6 V
JTAG/BDM	TMS, TDI — DSDI, TCK — DSCK, TDO — DSDO, JCOMP	5	2.6 V
READI Port	MCKO, MDO[3:0], $\overline{\text{MSEO}}$, MCKI, MDI[1:0], $\overline{\text{MSEI}}$, $\overline{\text{EVTI}}$, $\overline{\text{RSTI}}$	12	2.6 V
	MDO[4:7] (Shared with MIOS14 GPIO pins)	4 pins, MUXed with MIOS14	2.6 V

Table 2-1 MPC565 / MPC566 Pad Function Summary (Continued)

Functional Group Description	Signals[1]	Total No. Signals	5 V / 2.6 V
Clocks and PLL	XTAL, EXTAL, XFC, CLKOUT, KAPWR, EXTCLK, V_{DDSYN}, V_{SSSYN}, ENGCLK	9	2.6 V
DLCMD2 (J1850) — Shared with QSMCM_B pins	RX, TX	2 0 Pins, MUXed with QSMCMB pins	5 V
TOUCAN_A	CNTX0_A, CNRX0_A	2	5 V
TOUCAN_B	CNTX0_B, CNRX0_B	2	5 V
TOUCAN_C — Shared with MIOS14 GPIO pins	CNTX0_B, CNRX0_B	2 0 Pins, MUXed with MIOS14	5 V
UC3F Flash EEPROM	EPEE, B0EPEE, VFLASH VDDF, VSSF	5	5-V VFLASH, others 2.6 V
CALRAM, DPTRAM	VDDSRAM1, VDDSRAM2, VDDSRAM3	3	2.6 V
QADC64_A QADC64_B	40 analog channels, 2 pwr (VDDA, VSSA), 2 ref, ALTREF, 2 trig	47	5 V
QSMCM_A	PCS[0] — $\overline{SS}$ — QGPIO[0]	12	5 V
	PCS[1:3] — QGPIO[1:3]		
	MISO — QGPIO[4], MOSI — QGPIO[5], SCK — QGPIO[6]		
	TXD[1:2] — QGPO[1:2]		
	RXD[1:2] — QGPI[1:2]		
	ECK		
QSMCM_B, DLCMD2 (J1850)	PCS[3] — J1850_TX	12	5 V
	PCS[0] — $\overline{SS}$ — QGPIO[0]		
	PCS[1:2], MISO — QGPIO[4], MOSI — QGPIO[5], SCK — QGPIO[6]		
	TXD[1:2] — QGPO[1:2]		
	RXD2 — J1850_RX		
	RXD1 — QGPI[1], ECK		
MIOS14	MDA[11:15] MDA[27:31] MPWM[0:3] MPWM[16:19]	18	5 V
	VF[0:2] — MPIO32B[0:2]	5	2.6-V / 5-V GPIO
	VFLS[0:1] — MPIO32B[3:4]		
	C_CNTX0 — MPIO32B[13] C_CNRX0 — MPIO32B[14] MPWM[4:5, 20:21] — MPIO32B[5:6, 11:12]	6	5 V
	READI:MDO[4:7] — MPIO32B[7:10]	4	5 V / 2.6 V
	MPIO32B[15]	1	5 V
	MRTCSM:VDDRTC, VSSRTC, EXTAL32, XTAL32	4	2.6 V

Table 2-1 MPC565 / MPC566 Pad Function Summary (Continued)

Functional Group Description	Signals[1]	Total No. Signals	5 V / 2.6 V
TPU3_A	TPU3_A_CH[0:15]	16	5 V
	TCR2	1	
TPU3_B	TPU3_B_CH[0:15]	16	5 V
	TCR2	1	
TPU3_C	TPU3_C_CH[0:15]	16	5 V
	TCR2	1	

NOTES:
1. "—" implies that the corresponding functions are multiplexed on the pin.
2. This pin was 5-V GPIO on mask set K85H.

2.1.1 MPC565 / MPC566 Pin Sharing

This section describes the additional pin multiplexing on the MPC565 / MPC566. This multiplexing is used to share pins between modules. These functions are described in **Table 2-2**.

Table 2-2 MPC565 / MPC566 Pin Sharing Description

Pin Name	Function
c_cntx0_mpio32b13, c_cnrx0_mpio32b14	TOUCAN_C shared with MIOS14 GPIO
mdo_4_mpio32b10, mdo_5_mpio32b9, mdo_6_mpio32b8, mdo_7_mpio32b7	READI shared with MIOS14 GPIO
mpwm20_mpio32b11, mpwm21_mpio32b12, mpwm4_mpio32b5, mpwm5_mpio32b6	MIOS14 PWM submodule shared with MIOS14 GPIO
vf0_mpio32b0, vf1_mpio32b1, vf2_mpio32b2,	VF pins shared with MIOS14 GPIO
vfls0_mpio32b3, vfls1_mpio32b4	VFLS shared with MIOS14 GPIO
b_pcs3_j1850_tx, b_rxd2_j1850_rx	QSMCM_B pins are muxed with DLCMD2 (J1850). These pins are transmit and receive pins. See **2.4.2 QSMCM_A/QSMCM_B/ DLCMD2 (J1850) PADS.**

2.2 Pad Module Configuration Register (PDMCR)

The slew rate and weak pull-up/pull-down characteristics of some pins are controlled by bits in the PDMCR. This register resides in the SIU memory map. The contents of

the PDMCR are illustrated below. The $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ signal resets all the PDMCR bits asynchronously.

PDMCR — Pads Module Configuration Register **0x2F C03C**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SLRC				Reserved		PRDS	SPRDS	T2CLK_PU	PULL_DIS						Re-served
$\overline{\text{HRESET}}$:															
0				0		0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
SPULL_DIS	Reserved														
$\overline{\text{HRESET}}$:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2-3 PDMCR Bit Descriptions

Bit(s)	Name	Description
0	SLRC0	SLRC0 controls the slew rate of pins on the following modules: TPU3, QADC64, USIU_GPIO0 0 = Slow slew rate for pins. (200 nsec). 1 = Normal slew rate for pins.
1	SLRC1	SLRC1 controls the slew rate of pins on the following modules: QSPI, TOUCAN_A, TOUCAN_B. 0 = Slow slew rate for pins. (50 nsec). 1 = Normal slew rate for pins.
2	SLRC2	SLRC2 controls the slew rate of pins on the QSCI in QSMCM_A and QSMCM_B. 0 = Slow slew rate for pins. (200 ns). 1 = Normal slew rate for pins.
3	SLRC3	SLRC3 controls the slew rate of pins on the following modules: MIOS14, TOUCAN_C 0 = Slow slew rate for pins. (50 ns for TOUCAN_C, 200 nsec for others). 1 = Normal slew rate for pins.
4:5	—	Reserved
6	PRDS	When set, the PRDS bit disables weak pull-up-or-down devices which are enabled at the assertion of $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ or $\overline{\text{HRESET}}$. The pads affected by this bit are as follows: All SGPIO, all TPU3 except for T2CLK, all QADC with GPIO, all QSMCM pads. The pads are shown in **Table 2-6**. 0 = Enable weak pull-up/pull-down devices on pads controlled by this signal. 1 = Disable weak pull-up/pull-down devices on pads controlled by this signal.
7	SPRDS	When set, the SPRDS bit disables weak pull up-or-down devices which are enabled at the assertion of $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ or $\overline{\text{HRESET}}$. The pads affected by this bit are as follows: $\overline{\text{BDIP}}$, $\overline{\text{TA}}$, $\overline{\text{TS}}$, $\overline{\text{TEA}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{BB}}$, TSIZ, $\overline{\text{BI}}$/$\overline{\text{STS}}$, $\overline{\text{BURST}}$. The pads are shown in **Table 2-6**. 0 = Enable weak pull-up/pull-down devices on pads controlled by this signal. 1 = Disable weak pull-up/pull-down devices on pads controlled by this signal.
8	T2CLK_PU	This bit controls the pull-up on the TPU T2CLK pins. 0 = pull-ups are enabled if the T2CLK pins are defined as inputs 1 = Pull-ups are disabled on the T2CLK pins

Table 2-3 PDMCR Bit Descriptions (Continued)

Bit(s)	Name	Description
9:14	PULL_DIS	When set, the PULL_DIS bits disables weak pull up-or-down devices which are enabled at the assertion of PORESET/TRST or HRESET. The pads affected by these bits are as follows: PULL_DIS[0] (bit 9): all MIOS input pins except C_CNTX0/MPIO32B[13] and C_CNRX0/ MPIO32B[14][1] PULL_DIS[1] (bit 10): all QSMCM input pins[2] PULL_DIS[2] (bit 11): all QADC input pins, except ETRIG1 and ETRIG2[3] PULL_DIS[3] (bit 12): all TouCAN input pins[4] PULL_DIS[4] (bit 13): READI module input pins PULL_DIS[5] (bit 14): ETRIG1 and ETRIG2[5] 0 = Enable weak pull-up/pull-down devices on pads controlled by this signal. 1 = Disable weak pull-up/pull-down devices on pads controlled by this signal.
15	—	Reserved
16:17	SPULL_DIS	When set, the SPULL_DIS bits disables weak pull up-or-down devices which are enabled at the assertion of poreset_b_trst_b or hreset_b. The pads affected by these bits are as follows: SPULL_DIS[0] (bit 16): IRQ5_SGPIO5_MODCK1 SPULL_DIS[1] (bit 17): JTAG/BDM pins (TMS, TDI/DSDI, JCOMP, TCK/DSCK) 0 = Enable weak pull-up/pull-down devices on pads controlled by this signal. 1 = Disable weak pull-up/pull-down devices on pads controlled by this signal.
31:18	—	Reserved

NOTES:
1. Was ETRIG1, ETRIG2 in mask set K85H.
2. Was None in mask set K85H.
3. Was TOUCAN_A, TOUCAN_B in mask set K85H.
4. Was TOUCAN_C and MIOS MPIO32B13 and MPIO32B14 in mask set K85H.
5. Was RESERVED in mask set K85H.

2.3 Pad Module Configuration Register (PDMCR2)

The PDMCR2 controls the pre-discharge circuitry for the data bus. This allows for 5-V friendliness on the data bus.

PDMCR2 — Pads Module Configuration Register 2 **0x2F C038**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PREDIS_EN	RESERVED														
HRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RESERVED															
HRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2-4 PDMCR2 Bit Descriptions

Bit(s)	Name	Description
0	PREDIS_EN	PREDIS_EN 0 = Bus pre-discharge disabled 1 = Bus pre-discharge enabled
1:31	—	Reserved

2.4 Signal Descriptions

The pad ring supports 352 functional pins (388 including all power and ground). Each pin and the functionality it supports are described in this section.

2.4.1 USIU Pads

2.4.1.1 ADDR[8:31]/SGPIOA[8:31]

Pin Name: addr_sgpioa8 – addr_sgpioa31 (24 pins)

Address Bus – Specifies the physical address of the bus transaction. The address is driven onto the bus and kept valid until a transfer acknowledge is received from the slave. ADDR8 is the most significant signal for this bus.

Port SGPIOA[8:31] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.1.2 DATA[0:31]/SGPIOD[0:31]

Pin Name: data_sgpiod0 – data_sgpiod31 (32 pins)

Data Bus – Provides the general-purpose data path between the chip and all other devices. Although the data path is a maximum of 32 bits wide, it can be sized to support 8-, 16-, or 32-bit transfers. DATA[0] is the MSB of the data bus.

Port SGPIOD[0:31] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.1.3 $\overline{\text{IRQ}}$[0]/SGPIOC[0]

Pin Name: irq0_b_sgpioc0

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU. IRQ0 is a nonmaskable interrupt (NMI).

Port SGPIOC[0] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.1.4 $\overline{\text{IRQ}}$[1]/$\overline{\text{RSV}}$/SGPIOC[1]

Pin Name: irq1_b_rsv_b_sgpioc1

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Reservation – This line used together with the address bus to indicate that the internal core initiated a transfer as a result of a STWCX or a LWARX instruction.

Port SGPIOC[1] – This function allows the pins to be used as general-purpose inputs/ outputs.

2.4.1.5 $\overline{\text{IRQ}}$[2]/$\overline{\text{CR}}$/SGPIOC[2]/$\overline{\text{MTS}}$

Pin Name: irq2_b_cr_b_sgpioc2_mts_b

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Cancel Reservation – Instructs the chip to clear its reservation, some other master has touched its reserved space. An external bus snooper would assert this signal.

Port SGPIOC[2] – This function allows the pins to be used as general-purpose inputs/ outputs.

Memory Transfer Start – This pin is the transfer start signal from the MPC565 / MPC566 memory controller to allow external memory access by an external bus master.

2.4.1.6 $\overline{\text{IRQ}}$[3]/$\overline{\text{KR}}$/$\overline{\text{RETRY}}$/SGPIOC[3]

Pin Name: irq3_b_kr_b_retry_b_sgpioc3

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Kill Reservation – In case of a bus cycle initiated by a STWCX instruction issued by the CPU core to a non-local bus on which the storage reservation has been lost, this signal is used by the non-local bus interface to back-off the cycle.

Retry – Indicates to a master that the cycle is terminated but should be repeated. As an input, it is driven by the external slave to retry a cycle.

Port SGPIOC[3] – This function allows the pins to be used as general-purpose inputs/ outputs.

2.4.1.7 $\overline{\text{IRQ}}$[4]/AT[2]/SGPIOC[4]

Pin Name: irq4_b_at2_sgpioc4

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Address Type – A bit from the address type bus which indicates one of the 16 “address types” to which the address applies. The address type signals are valid at the rising edge of the clock in which the special transfer start ($\overline{\text{STS}}$) is asserted.

Port SGPIOC[4] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.1.8 $\overline{\text{IRQ}}$[5]/SGPIOC[5]/MODCK[1]

Pin Name: irq5_b_sgpioc5_modck1

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Port SGPIOC[5] – This function allows the pins to be used as general-purpose inputs/outputs.

Mode Clock [1] – Sampled at the negation of $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ in order to configure the phase-locked loop (PLL)/clock mode of operation.

2.4.1.9 $\overline{\text{IRQ}}$[6:7]/MODCK[2:3]

Pin Name: irq6_b_modck2 – irq7_b_modck3 (two pins)

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Mode Clock [2:3] – Sampled at the negation of $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ in order to configure the PLL/clock mode of operation.

2.4.1.10 TSIZ[0:1]

Pin Name: tsiz0 – tsiz1 (two pins)

Transfer size – Indicates the size of the requested data transfer in the current bus cycle.

2.4.1.11 RD/$\overline{\text{WR}}$

Pin Name: rd_wr_b

Read/Write – Indicates the direction of the data transfer for a transaction. A logic one indicates a read from a slave device; a logic zero indicates a write to a slave device.

2.4.1.12 $\overline{\text{BURST}}$

Pin Name: burst_b

Burst Indicator – Indicates whether the current transaction is a burst transaction or not.

2.4.1.13 $\overline{\text{BDIP}}$

Pin Name: bdip_b

Burst Data In Progress – Indicates to the slave that there is a data beat following the current data beat.

2.4.1.14 $\overline{\text{TS}}$

Pin Name: ts_b

Transfer Start – Indicates the start of a bus cycle that transfers data to/from a slave device. This signal is driven by the master only when it has gained ownership of the bus. Every master should negate this signal before the bus is relinquished. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

2.4.1.15 $\overline{\text{TA}}$

Pin Name: ta_b

Transfer Acknowledge – This line indicates that the slave device addressed in the current transaction has accepted the data transferred by the master (write) or has driven the data bus with valid data (read). The slave device negates the $\overline{\text{TA}}$ signal after the end of the transaction and immediately three-state it to avoid contentions on the line if a new transfer is initiated addressing other slave devices. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

2.4.1.16 $\overline{\text{TEA}}$

Pin Name: tea_b

Transfer Error Acknowledge – This signal indicates that a bus error occurred in the current transaction. The MCU asserts this signal when the bus monitor does not detect a bus cycle termination within a reasonable amount of time. The assertion of $\overline{\text{TEA}}$ causes the termination of the current bus cycle, regardless of the state of $\overline{\text{TEA}}$. An external pull-up device is required to negate $\overline{\text{TEA}}$ quickly, before a second error is detected. That is, the pin must be pulled up within one clock cycle of the time it was three-stated by the MPC565 / MPC566.

2.4.1.17 $\overline{\text{RSTCONF}}$/TEXP

Pin Name: rstconf_b_texp

Reset Configuration – Input. This input line is sampled by the chip during the assertion of the $\overline{\text{HRESET}}$ signal in order to sample the reset configuration. If the line is asserted, the configuration mode is sampled from the external data bus. When this line is negated, the configuration mode adopted by the chip is the default one.

Timer Expired – Output. This output line reflects the status of the TEXPS bit in the PLPRCR register in the USIU. This indicates an expired timer value.

2.4.1.18 $\overline{\text{OE}}$

Pin Name: oe_b

Output Enable – This output line is asserted when a read access to an external slave controlled by the GPCM in the memory controller is initiated by the chip.

2.4.1.19 $\overline{\text{BI}}$/$\overline{\text{STS}}$

Pin Name: bi_b_sts_b

Burst Inhibit – This bidirectional, active low, three-state line indicates that the slave device addressed in the current burst transaction is not able to support burst transfers. When the chip drives out the signal for a specific transaction, it asserts or negates $\overline{\text{BI}}$ during the transaction according to the value specified in the appropriate control registers. Negation of the signal occurs after the end of the transaction followed by the immediate three-state. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

Special Transfer Start – This output signal is driven by the chip to indicate the start of a transaction on the external bus or signals the beginning of an internal transaction in showcycle mode.

2.4.1.20 $\overline{\text{CS}}$[0:3]

Pin Name: cs0_b – cs3_b (4 pins)

Chip Select – These output signals enable peripheral or memory devices at programmed addresses if defined appropriately in the memory controller. $\overline{\text{CS}}$[0] can be configured to be the global chip select for the boot device.

2.4.1.21 $\overline{\text{WE}}$[0:3]/$\overline{\text{BE}}$[0:3]/AT[0:3]

Pin Name: we_b_at0 – we_b_at3 (4 pins)

Write Enable[0:3]/Byte Enable[0:3] – This output line is asserted when a write access to an external slave controlled by the memory controller is initiated by the chip. It can be optionally be asserted on all read and write accesses. See WEBS bit definition in **Table 10-7**. $\overline{\text{WE}}$[0]/$\overline{\text{BE}}$[0] is asserted if the data lane DATA[0:7] contains valid data to be stored by the slave device. $\overline{\text{WE}}$[1]/$\overline{\text{BE}}$[1] is asserted if the data lane DATA[8:15] contains valid data to be stored by the slave device. $\overline{\text{WE}}$[2]/$\overline{\text{BE}}$[2] is asserted if the data line DATA[16:23] contains valid data to be stored by the slave device. $\overline{\text{WE}}$[3]/$\overline{\text{BE}}$[3] is asserted if the data lane DATA[24:31] contains valid data to be stored by the slave device.

Address Type – Indicates one of the 16 address types to which the address applies. The address type signals are valid at the rising edge of the clock in which the special transfer start ($\overline{\text{STS}}$) is asserted.

2.4.1.22 $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$

Pin Name: poreset_b_trst_b

Power-On Reset – This pin should be activated as a result of a voltage failure on the keep-alive power pins. The pin has a glitch detector to ensure that low spikes of less than 20 ns are rejected. The internal PORESET/TRST signal is asserted only if PORESET/TRST is asserted for more than 100 ns. See **SECTION 7 RESET** for more details on timing.

Test Reset – This input provides asynchronous reset to the test logic (JTAG).

2.4.1.23 HRESET

Pin Name: hreset_b

Hard Reset – The chip can detect an external assertion of HRESET only if it occurs while the chip is not asserting reset. After negation of HRESET or SRESET is detected, a 16-cycle period is taken before testing the presence of an external reset. The internal HRESET signal is asserted only if HRESET is asserted for more than 100 ns. To meet external timing requirements, an external pull-up device is required to negate HRESET. See **SECTION 7 RESET** for more details on timing.

2.4.1.24 SRESET

Pin Name: sreset_b

Soft Reset – The chip can detect an external assertion of SRESET only if it occurs while the chip is not asserting reset. After negation of HRESET or SRESET is detected, a 16-cycle period is taken before testing the presence of an external soft reset. To meet external timing requirements, an external pull-up device is required to negate SRESET. See **SECTION 7 RESET** for more details on timing.

2.4.1.25 SGPIOC[6]/FRZ/PTR

Pin Name: sgpioc6_frz_ptr_b

Port SGPIOC[6] – This function allows the pins to be used as general-purpose inputs/outputs.

Freeze – Indicates that the RCPU is in debug stopped mode.

Program Trace – Indicates an instruction fetch is taking place in order to allow program flow tracking.

2.4.1.26 SGPIOC[7]/IRQOUT/LWP[0]

Pin Name: sgpioc7_irqout_b_lwp0

Port SGPIOC[7] – This function allows the pin to be used as general-purpose inputs/outputs.

Interrupt Out – Indicates that an interrupt has been requested to all external devices.

Load/Store Watchpoint 0 – This output line reports the detection of a data watchpoint in the program flow executed by the RCPU. See **SECTION 22 DEVELOPMENT SUPPORT** for more details.

2.4.1.27 $\overline{\text{BG}}$/VF[0]/LWP[1]

Pin Name: bg_b_vf0_lwp1

Bus Grant – Indicates external data bus status. Is asserted low when the arbiter of the external bus grants to the specific master the ownership of the bus.

Visible Instruction Queue Flush Status – This output line together with VF[1] and VF[2] is output by the chip when a program instructions flow tracking is required. VF report the number of instructions flushed from the instruction queue in the internal core. See **SECTION 22 DEVELOPMENT SUPPORT** for more details.

Load/Store Watchpoint – This output line reports the detection of a data watchpoint in the program flow executed by the RCPU.

2.4.1.28 $\overline{\text{BR}}$/VF[1]/IWP[2]

Pin Name: br_b_vf1_iwp2

Bus Request – Indicates that the data bus has been requested for external cycle.

Visible Instruction Queue Flush Status – This output line together with VF[1] and VF[2] is output by the chip when a program instructions flow tracking is required. VF report the number of instructions flushed from the instruction queue in the internal core. See **SECTION 22 DEVELOPMENT SUPPORT** for more details.

Instruction Watchpoint 2 – This output line reports the detection of an instruction watchpoint in the program flow executed by the RCPU.

2.4.1.29 $\overline{\text{BB}}$/VF[2]/IWP[3]

Pin Name: bb_b_vf2_iwp3

Bus Busy – Indicates that the master is using the bus. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

Visible Instruction Queue Flush Status – This output line together with VF[0] and VF[1] is output by the chip when a program instructions flow tracking is required. VF report the number of instructions flushed from the instruction queue in the internal core.

Instruction Watchpoint 3 – This output line reports the detection of an instruction watchpoint in the program flow executed by the internal core.

2.4.1.30 IWP[0:1]/VFLS[0:1]

Pin Name: iwp0_vfls0 – iwp1_vfls1 (two pins)

Instruction Watchpoint – These output lines report the detection of an instruction watchpoint in the program flow executed by the RCPU.

Visible History Buffer Flush Status – These signals are output by the chip to enable program instruction flow tracking. They report the number of instructions flushed from the history buffer in the RCPU. See **SECTION 22 DEVELOPMENT SUPPORT** for details.

2.4.1.31 TMS

Pin Name: tms

Test Mode Select – This input controls test mode operations for on-board test logic (JTAG).

2.4.1.32 TDI/DSDI

Pin Name: tdi_dsdi

Test Data In – This input is used for serial test instructions and test data for on-board test logic (JTAG).

Development Serial Data Input – This input line is the data in for the debug port interface. See **SECTION 22 DEVELOPMENT SUPPORT** for details.

2.4.1.33 TCK/DSCK

Pin Name: tck_dsck

Test Clock – This input provides a clock for on-board test logic (JTAG).

Development Serial Clock – This input line is the clock for the debug port interface. See **SECTION 22 DEVELOPMENT SUPPORT** for details.

2.4.1.34 TDO/DSDO

Pin Name: tdo_dsdo

Test Data Out – This output is used for serial test instructions and test data for on-board test logic (JTAG).

Development Serial Data Output – This output line is the data-out line of the debug port interface. See **SECTION 22 DEVELOPMENT SUPPORT** for details.

2.4.1.35 JCOMP

Pin Name: jcomp_b

JTAG Compliancy – This signal enables the IEEE1149.1 JTAG circuitry in the MPC565 / MPC566. JTAG circuitry in the MPC565 / MPC566. This pin was $\overline{\text{TRST}}$ on the K85H mask set of the MPC566.

2.4.1.36 XTAL

Pin Name: xtal

XTAL – This output line is one of the connections to an external crystal for the internal oscillator circuitry.

2.4.1.37 EXTAL

Pin Name: extal

EXTAL – This line is one of the connections to an external crystal for the internal oscillator circuitry. If this pin is unused, it must be grounded.

2.4.1.38 XFC

Pin Name: xfc

External Filter Capacitance – This input line is the connection pin for an external capacitor filter for the PLL circuitry.

2.4.1.39 CLKOUT

Pin Name: clkout

Clock Out – This output line is the clock system frequency. The CLKOUT drive strength can be configured to full strength, half strength, quarter strength, or disabled. The drive strength is configured using the COM[0:1] bits and CQDS bits in the SCCR register in the USIU.

2.4.1.40 EXTCLK

Pin Name: extclk

EXTCLK – Input. This is the external frequency source for the chip. If this is unused, the pin must be grounded.

2.4.1.41 VDDSYN

Pin Name: vddsyn

VDDSYN – This is the power supply of the PLL circuitry.

2.4.1.42 VSSSYN

Pin Name: vsssyn

VSSSYN – This is the ground reference of the PLL circuitry.

2.4.1.43 ENGCLK/BUCLK

Pin Name: engclk_buclk

ENGCLK – This is the engineering clock output. Drive voltage can be configured to 2.6 V, 5 V (with slew-rate control) or disabled. The drive voltage is configured using the EECLK[0:1] bits in the SCCR register in the SIU.

BUCLK – When the chip is in limp mode, it is operating from a less precise on-chip ring oscillator to allow the system to continue minimum functionality until the system clock is fixed. This backup clock can be seen externally if selected by the values of the EECLK[0:1] bits in the SCCR register in the USIU.

2.4.1.44 PULLSEL

Pin Name: pullsel

Pull Select – This pin determines whether the pull devices on the MIOS and TPU pins are pull-ups or pull-downs. When pull-ups are selected, the pull-ups are to5.0 V. The following MIOS pins pins always have pull down resistors unless disabled in the PDMCR register: VF[0:2]/MPIO32B[0:2], VFLS[0:1]/MPIO32B[3:4], and MDO[7:4]/ MPIO32B[7:10].

2.4.2 QSMCM_A/QSMCM_B/DLCMD2 (J1850) PADS

The MPC565 / MPC566 has two QSMCM modules, QSMCM_A and QSMCM_B. QSMCM_A has identical function to the MPC555/MPC556. QSMCMB has its RXD2 and PCS[3] pins muxed with the DLCMD2 (J1850) module. The muxing of the pins is controlled by the QPAPCS3 bit in QSMCM_B pin assignment reg. ($\overline{\text{PQSPAR}}$), according to **Table 2-5**. The muxed pins default to DLCMD2 function at reset. Since the normal function of the PCS pins within the QSMCM require that this bit be written before the PCS pin is used, the muxing appears transparent to both the QSMCM_B and the DLCMD2. However, only one of the modules, DLCMD2 or QSMCM_B can use the pins in a system. Because of this muxed function on QSMCM_B, the general-purpose input and output functions are not available on the B_PCS[3] and B_RXD2 pins

Table 2-5 DLCMD2 / QSMCM_B SCI2 Pin MUX Control

QPAPCS3 Bit Value	QSMCM_B / DLCMD2 Pin Function
0	B_PCS[3]/J1850_TX pin assigned to J1850_TX. B_RXD2/J1850_RX pin assigned to J1850_RX. Pins are assigned to DLCMD2 (J1850_TX & J1850_RX)
1	B_PCS[3]/J1850_TX pin assigned to PCS[3]. B_RXD2/J1850_RX pin assigned to B_RXD2. Pins are assigned to QSMCMB SCI2 (B_PCS[3], B_RXD2)

2.4.2.1 PCS[0]/$\overline{\text{SS}}$/QGPIO[0]

Pin Name: a_pcs0_ss_b_qgpio0, b_pcs0_ss_b_qgpio0

PCS[0] – This signal provides QSPI peripheral chip select 0.

$\overline{SS}$ – Assertion of this bidirectional signal places the QSPI in slave mode.

Port QGPIO[0] – When this pin is not needed for a QSPI application it can be configured as a general-purpose input/output.

2.4.2.2 PCS[1:2]/QGPIO[1:2]

Pin Name: a_pcs1_qgpio1, a_pcs1_qgpio1, b_pcs1_qgpio1, b_pcs2_qgpio2

PCS[1:2] – These signals provide two QSPI peripheral chip selects.

Port QGPIO[1:2] – When these pins are not needed for QSPI applications they can be configured as general-purpose input/outputs.

2.4.2.3 PCS[3]/QGPIO[3]/J1850_TX

Pin Name: a_pcs3_qgpio3, b_pcs3_j1850_tx

PCS3 – These signals provide two QSPI peripheral chip selects.

Port QGPIO[3] – When the QSMCM_A PCS3 pin is not needed for QSPI applications it can be configured as a general-purpose input/output.

J1850_TX – The QSMCM_B PCS3 pin can be configured as the J1850 transmit pin for the DLCMC2 module.

2.4.2.4 MISO/QGPIO[4]

Pin Name: a_miso_qgpio4, b_miso_qgpio4

Master-In Slave-Out (MISO) – This bidirectional signal furnishes serial data input to the QSPI in master mode, and serial data output from the QSPI in slave mode.

Port QGPIO[4] – When this pin is not needed for a QSPI application it can be configured as a general-purpose input/output.

2.4.2.5 MOSI/QGPIO[5]

Pin Name: a_mosi_qgpio5, b_mosi_qgpio5

Master-Out Slave-In (MOSI) – This bidirectional signal furnishes serial data output from the QSPI in master mode and serial data input to the QSPI in slave mode.

Port QGPIO[5] – When this pin is not needed for a QSPI application it can be configured as a general-purpose input/output.

2.4.2.6 SCK/QGPIO[6]

Pin Name: a_sck_qgpio6, b_sck_qgpio6

SCK – This bidirectional signal furnishes the clock from the QSPI in master mode or furnishes the clock to the QSPI in slave mode.

Port QGPIO[6] – When this pin is not needed for a QSPI application, it can be configured as a general-purpose input/output. When the QSPI is enabled for serial transmitting, the pin can *not* function as a GPIO.

2.4.2.7 TXD[1:2]/QGPO[1:2]

Pin Name: a_txd1_qgpo1, b_txd1_qgpo1, a_txd2_qgpo2, b_txd2_qgpo2

Transmit Data – These output signals are the serial data outputs from the SCI1 and SCI2.

Port QGPO[1:2] – When these pins are not needed for a SCI applications, they can be configured as general-purpose outputs. When the transmit enable bit in the SCI control register is set to a logic 1, these pins can *not* function as general-purpose outputs

2.4.2.8 RXD[1:2]/QGPI[1:2], RXD[1]/QGPI1, RXD[2]/J1850_RX

Pin Name: a_rxd1_qgpi1, a_rxd2_qgpi2, b_rxd1_qgpi1, b_rxd2_j1850_rx

Receive Data (RXD1, RXD2) – These input signals furnish serial data inputs to the SCI1 and SCI2.

Port QGPI[1:2] – When this pin is not needed for SCI1 applications, it can be configured as a general-purpose input. When the receive enable bit in the SCI control register is set to a logic 1, this pin can *not* function as a general-purpose input.

J1850_RX – The QSMCM_B RXD2 pin can be configured as the J1850 transmit pin for the DLCMC2 module.

2.4.2.9 ECK

Pin Name: b_eck

External Baud Clock (ECK) – This signal provides an external baud clock used by SCI1 and SCI2. (Note: this pin is not usable on the MPC565 / MPC566.)

2.4.3 MIOS14 Pads

Some of the MIOS14 signals are shared with other functions. Only one function can be used at a time. These extra functions include debug (VF[0:2], VFLS[0:1]), READI (MDO[4:7]), TouCAN (C_CNTX0, C_CNRX0), and the additional MIOS14 functions MPWM[4:5, 20:21], and 32KCLKOUT. For additional information about MIOS14 testing and pin usage, see **17.10.2.2 MIOS14 Test and Pin Control Register (MIOS14TPCR)**.

2.4.3.1 MDA[11, 13, 27, 30]

Pin Name: mda11, mda13, mda27, mda30 (four pins)

Double Action – Each of these pins provide a path for two 16-bit input captures and two 16-bit output compares.

Clock Input – Each of these pins provide a clock input to the modulus counter submodule. MDA11 can be used as the clock input to the MMCSM6 modulus counter. MDA13 can be used as the clock input to the MMCSM22 modulus counter.

2.4.3.2 MDA[12, 14, 28, 31]

Pin Name: mda12, mda14, mda28, mda31(four pins)

Double Action – Each of these pins provide a path for two 16-bit input captures and two 16-bit output compares.

Load Input – Each of these pins provide a load input to the modulus counter submodule. MDA12 can be used as the load input to the MMCSM6 modulus counter. MDA14 can be used as the load input to the MMCSM22 modulus counter.

2.4.3.3 MDA[15], [27:31]

Pin Name: mda15, mda27 – mda31 (six pins)

Double Action – Each of these pins provide a path for two 16-bit input captures and two 16-bit output compares.

2.4.3.4 MPWM[0:3]

Pin Name: mpwm0 – mpwm3 (four pins)

Pulse Width Modulation – These pins provide variable pulse width output signals at a wide range of frequencies.

2.4.3.5 MPWM[16, 18]

Pin Name: mpwm16, mpwm18 (two pins)

Pulse Width Modulation – These pins provide variable pulse width output signals at a wide range of frequencies.

Clock Input – Each of these pins provide a clock input to the modulus counter submodule. MPWM16 can be used as the clock input to the MMCSM6 modulus counter. MPWM18 can be used as the clock input to the MMCSM22 modulus counter.

2.4.3.6 MPWM[17, 19]

Pin Name: mpwm17, mpwm19 (two pins)

Pulse Width Modulation – These pins provide variable pulse width output signals at a wide range of frequencies.

Load Input – Each of these pins provide a load input to the modulus counter submodule. MPWM17 can be used as the load input to the MMCSM6 modulus counter. MPWM19 can be used as the load input to the MMCSM22 modulus counter.

2.4.3.7 VF[0:2]/MPIO32B[0:2]

Pin Name: vf0_mpio32b0 – vf2_mpio32b2 (three pins)

Visible Instruction Queue Flush Status – These lines output by the chip when program instruction flow tracking is required. VF reports the number of instructions flushed from the instruction queue in the internal core.

Port MIOS GPIO[0:2] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.3.8 VFLS[0:1]/MPIO32B[3:4]

Pin Name: vfls0_mpio32b3 – vfls1_mpio32b4 (two pins)

Visible History Buffer Flush Status – These signals are output by the chip to allow program instruction flow tracking. They report the number of instructions flushed from the history buffer in the RCPU. See **SECTION 22 DEVELOPMENT SUPPORT** for details.

MIOS GPIO – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.3.9 MPWM[4:5]/MPIO32B[5:6]

Pin Names: mpwm4_mpio32b5 – mpwm5_mpio32b6

Pulse Width Modulation – These pins provide variable pulse width output signals at a wide range of frequencies.

Port MIOS GPIO[5:6] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.3.10 MDO[7:4]/MPIO32B[7:10]

Pin Names: mdo_7_mpio32b7, mdo_6_mpio32b8, mdo_5_mpio32b9, mdo_4_mpio32b10

Port MIOS GPIO[7:10] – This function allows the pins to be used as general-purpose inputs/outputs.

READI (NEXUS) Data Out – This function allows the pins to be used by the READI modules as NEXUS data output pins.

2.4.3.11 MPWM[20:21]/MPIO32B[11:12]

Pin Names: mpwm20_mpio32b11– mpwm21_mpio32b12

Pulse Width Modulation – These pins provide variable pulse width output signals at a wide range of frequencies.

Port MIOS GPIO[11:12] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.3.12 C_CNTX0/C_CNRX0/MPIO32B[13:14]

Pin Names: c_cntx0_mpio32b13 – c_cnrx0_mpio32b14

Port MIOS GPIO[13:14] – This function allows the pins to be used as general-purpose inputs/outputs.

TOUCAN_C Receive/Transmit – These pins provide the receive and transmit pins for the TOUCAN_C module.

2.4.3.13 MPIO32B15

Pin Name: mpio32b15

Port MIOS GPIO[15] – This function allows the pins to be used as general-purpose inputs/outputs.

2.4.4 32-KHz Oscillator Pads

2.4.4.1 XTAL32

Pin Name: xtal32

XTAL32 – This output line is one of the connections to an external 32-KHz crystal for the MIOS14 real-time clock submodule (MRTCSM).

2.4.4.2 EXTAL32

Pin Name: extal32

EXTAL32 – This line is one of the connections to an external 32-KHz crystal for the internal oscillator circuitry used by the MRTCSM. If this pin is unused, it must be grounded.

2.4.4.3 VDDRTC

Pin Name: VDDRTC

VDDRTC – This is the power supply of the 32-KHz oscillator circuitry and the MRTCSM.

2.4.4.4 VSSRTC

Pin Name: VSSRTC

VSSRTC – This is the power supply of the 32-KHz oscillator circuitry.

2.4.5 TPU3_A/TPU3_B/TPU3_C Pads

2.4.5.1 TPUCH[0:15]

Pin Name: a_tpuch0 – a_tpuch15 (16 pins for TPU3_A), b_tpuch0 -– b_tpuch15 (16 pins for TPU3_B), c_tpuch0 – c_tpuch15 (16 pins for TPU3_C)

TPU Channels – These signals provide each TPU3 with 16 input/output programmable timed events.

2.4.5.2 T2CLK

Pin Name: a_t2clk (one pin for TPU3_A) – b_t2clk (one pin for TPU3_B) – c_t2clk (one pin for TPU3_C)

T2CLK – This signal is used to clock or gate the timer count register 2 (TCR2) within the TPU. This pin is an output-only in special test mode.

2.4.6 QADC64_A/QADC64_B Pads

2.4.6.1 ETRIG[1:2]

Pin Name: etrig1 – etrig2

ETRIG – These are the external trigger inputs to the QADC64_A and QADC64_B modules. ETRIG[1] can be configured to be used by both QADC64_A and QADC64_B. Likewise, ETRIG[2] can be used for both QADC64_B and QADC64_A. The trigger input pins are associated with the scan queues.

2.4.6.2 AN[44]/ANw/PQB[0]

Pin Name: an44_anw_a_pqb0

Analog Channel (AN[44]) – Internally multiplexed input-only analog channels. Passed on as a separate signal to the QADC64E.

Multiplexed Analog Input (ANw) – Externally multiplexed analog input.

Port (A_PQB[0]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.3 AN[45]/ANx/PQB[1]

Pin Name: an45_anx_a_pqb1

Analog Channel (AN[45]) – Internally multiplexed input-only analog channels. Passed on as a separate signal to the QADC64E.

Multiplexed Analog Input (ANx) – Externally multiplexed analog input.

Port (A_PQB[1]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.4 AN[46]/ANy/PQB[2]

Pin Name: an46_any_a_pqb2

Analog Channel (AN[46]) – Internally multiplexed input-only analog channel. The input is passed on as a separate signal to the QADC64E.

Multiplexed Analog Input (ANy) – Externally multiplexed analog input.

Port (A_PQB[2]) –When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.5 AN[47]/ANz/PQB[3]

Pin Name: an47_anz_a_pqb3

Analog Input (AN[47]) – Internally multiplexed input-only analog channel. The input is passed on as a separate signal to the QADC64E.

Multiplexed Analog Input (ANz) – Externally multiplexed analog input.

Port (A_PQB[3]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.6 AN[48:51]/PQB[4:7]

Pin Name: an48_a_pqb4 – an51_a_pqb7

Analog Input (AN[48:51]) – Analog input channel. The input is passed on as a separate signal to the QADC64E.

Port (A_PQB[4:7]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.7 AN[52:54]/MA[0:2]/PQA[0:2]

Pin Name: an52_a_ma0_pqa0 – an54_a_ma2_pqa2

Analog Input (AN[52:54]) – Input-only. The input is passed on as a separate signal to the QADC64E.

Multiplexed Address (MA[0:2]) – Output. Provides a three-bit multiplexed address output to the external multiplexer chip to allow selection of one of the eight inputs.

Port (A_PQA[0:2]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.8 AN[55:59]/PQA[3:7]

Pin Name: an55_a_pqa3 – an59_a_pqa7

Analog Input (AN[55:59]) – Input-only. The input is passed on as a separate signal to the QADC64E.

Port (A_PQA[3:7]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.9 AN[64:71]/PQB[0:7]

Pin Name: an64_b_pqb0 – an71_b_pqb7

Analog Input (AN[55:59]) – Input-only. The input is passed on as a separate signal to the QADC64E.

Port (B_PQB[3:7]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.10 AN[72:74]/MA[0:2]/PQA[0:2]

Pin Name: an72_b_ma0_pqa0 – an74_b_ma2_pqa2

Analog Input (AN[72:74]) – Input-only. The input is passed on as a separate signal to the QADC64E.

Multiplexed Address (MA[0:2]) – Output. Provides a three-bit multiplexed address output to the external multiplexer chip to allow selection of one of the eight inputs.

Port (B_PQA[0:2]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.11 AN[75:79]/PQA[3:7]

Pin Name: an75_b_pqa3 – an79_b_pqa7

Analog Input (AN[75:79]) – Input-only. The input is passed on as a separate signal to the QADC64E.

Port (B_PQA[3:7]) – When this pin is not needed for QADC converter functions, it can be used as a general-purpose input or output.

2.4.6.12 AN[80:87]

Pin Name: an80 – an87

Analog Input (AN[80:87]) – Input-only. The input is passed on as a separate signal to the QADC64E by the AMUX.

2.4.6.13 VRH

Pin Name: vrh

VRH – Input pin for high reference voltage for the QADC64_A and QADC64_B modules.

2.4.6.14 VRL

Pin Name: vrl

VRL – Input pin for low reference voltage for the QADC64_A and QADC64_B modules.

2.4.6.15 ALTREF

Pin Name: altref

ALTREF – Input pin for alternate reference voltage for the QADC64_A and QADC64_B modules.

2.4.6.16 VDDA

Pin Name: vdda

VDDA – Power supply input to analog subsystems of the QADC64_A and QADC64_B modules.

2.4.6.17 VSSA

Pin Name: vssa

VSSA – Input. Ground level for analog subsystems of the QADC64_A and QADC64_B modules.

2.4.7 TOUCAN_A / TOUCAN_B / TOUCAN_C Pads

2.4.7.1 CNTX0

Pin Name: a_cntx0 (one pin for first CAN), b_cntx0 (one pin for second CAN), c_cntx0_mpio32b13 (one pin for CAN_C, muxed with a MIOS14 GPIO)

TouCAN Transmit Data 0 – This signal is the serial data output.

2.4.7.2 CNRX0

Pin Name: a_cnrx0 (one pin for first CAN), b_cnrx0 (one pin for second CAN), c_cnrx0_mpio32b14 (one pin for CAN_C, MUXed with a MIOS14 GPIO)

TouCAN Receive Data – This signal furnishes serial input data.

2.4.8 READI Pads

Some READI pads are shared with MIOS14 functions, see **2.4.3 MIOS14 Pads**.

2.4.8.1 $\overline{\text{MSEO}}$

Pin Name: mseo_b

$\overline{\text{MSEO}}$ – Message start/end out ($\overline{\text{MSEO}}$) is an output pin which indicates when a message on the MDO pins has started, when a variable length packet has ended, and when the message has ended. External latching of $\overline{\text{MSEO}}$ occurs on rising edge of MCKO.

2.4.8.2 MDO[0:3]

Pin Name: mdo_3

MDO[0:3] – Message Data Output. Message data out (MDO[7:0] or MDO[1:0]) are output pins used for uploading OTM, BTM, DTM, and read/write accesses. External

latching of MDO occurs on rising edge of MCKO. Eight pins are implemented; four (MDO[4:7]) are shared with MIOS14 GPIO.

2.4.8.3 MCKO

Pin Name: mcko

MCKO – Output. Message clock-out (MCKO) is a free-running output clock to development tools for timing of MDO and MSEO pin functions. MCKO is the same as the MCU system clock.

2.4.8.4 $\overline{\text{RSTI}}$

Pin Name: rsti_b

$\overline{\text{RSTI}}$ – Reset In. $\overline{\text{RSTI}}$ is the NEXUS port reset input.

2.4.8.5 $\overline{\text{EVTI}}$

Pin Name: evti_b

$\overline{\text{EVTI}}$ – Event in (EVTI) is level sensitive when configured for breakpoint generation, otherwise it is edge sensitive.

2.4.8.6 $\overline{\text{MSEI}}$

Pin Name: msei_b

$\overline{\text{MSEI}}$ – Message Start/End Input. The $\overline{\text{MSEI}}$ input is a NEXUS input pin which indicates when a message on the MDI pins has started, when a variable length packet has ended, and when the message has ended. Internal latching of $\overline{\text{MSEI}}$ occurs on rising edge of MCKI.

2.4.8.7 MDI[0:1]

Pin Name: mdi_1

MDI[0:1] – Message Data Input. MDI[1:0] or MDI[0] are NEXUS input pins used for downloading configuration information, writes to user resources, etc. Internal latching of MDI will occur on rising edge of MCKI.

2.4.8.8 MCKI

Pin Name: mcki

MCKI – Message Clock Input. MCKI is the NEXUS message clock input.

2.4.9 UC3F Pads

2.4.9.1 EPEE

Pin Name: epee

EPEE – Input. This control signal externally controls the program or erase operations. When low, program or erase operations in both of the UC3F modules (UC3F_512KA and UC3F_512KB) are disabled.

2.4.9.2 B0EPEE

Pin Name: b0epee

B0EPEE – Input. This control signal externally controls the program or erase operations of block 0 of UC3F_512KA. When low, program or erase operations in block 0 of the UC3F_512KA module are disabled.

2.4.9.3 VFLASH

Pin Name: vflash

VFLASH – Input. Flash supply voltage (5-V supply) used during all operations of the UC3F.

2.4.9.4 VDDF

Pin Name: vddf

VDDF – Flash core voltage input (2.6-V supply).

2.4.9.5 VSSF

Pin Name: vssf

VSSF – Flash core zero supply input.

2.4.10 Global Power Supplies

2.4.10.1 NVDDL

Pin Name: nvddl

NVDDL – Noisy 2.6-V voltage supply input. This supplies the final output stage of the 2.6-V pad output drivers.

The NVDDL and QVDDL supplies should be connected to the same power supply in a user's system.

2.4.10.2 QVDDL

Pin Name: qvddl

QVDDL – Quiet 2.6-V voltage supply input. This supplies all pad logic and pre-driver circuitry, except for the the final output stage of the 2.6-V pad output drivers.

The NVDDL and QVDDL supplies should be connected to the same power supply in a user's system.

2.4.10.3 VDDH

Pin Name: vddh

VDDH – 5-V voltage supply input.

2.4.10.4 VDD

Pin Name: vdd

VDD – 2.6-V voltage supply input for internal logic.

2.4.10.5 KAPWR

Pin Name: kapwr

Keep-Alive Power – 2.6-V voltage supply input for the oscillator and keep-alive registers.

2.4.10.6 VDDSRAM1

Pin Name: vddsram1

SRAM Keep-Alive Power – 2.6-V voltage supply input for the keep-alive section of the CALRAM_A (32K) module. This pin supplies only keep-alive power to the CALRAM_A (32K) module. Run current is supplied by normal VDD.

2.4.10.7 VDDSRAM2

Pin Name: vddsram2

SRAM Keep-Alive Power – 2.6-V voltage supply input for the CALRAM_B (4 Kbyte) module. This pin supplies only keep-alive power to the CALRAM_B (4 Kbyte) module. Run current is supplied by normal VDD.

2.4.10.8 VDDSRAM3

Pin Name: vddsram3

SRAM Keep-Alive Power – 2.6-V voltage supply input for the arrays in the DPTRAM_AB (6 Kbytes), DPTRAM_C (4 Kbytes), and the BBC DECRAM (4 Kbytes) modules. This pin supplies only keep-alive power to both DPTRAM arrays and the DECRAM module. Run current is supplied by normal VDD.

2.4.10.9 VSS

Pin Name: vss

VSS – Ground level reference input.

2.5 Reset State

All input pins, with the exception of the power supply and clock related pins, are “weakly pulled” to a value during reset by a 130-µA (maximum) resistor based on cer-

tain conditions. See **APPENDIX E ELECTRICAL CHARACTERISTICS** for minimum specifications. In reset state all I/O pins become inputs, and all outputs except CLKOUT, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, are pulled only by the pull-up/pull-down.

2.5.1 Pin Functionality Configuration Out of Reset

The functionality out of reset of some pins that support multiple functionality is defined in the SIUMCR through the reset configuration word. For details on which multiplexed pins are configured by the reset configuration word and how they are configured, refer to **7.5.2 Hard Reset Configuration Word**.

The 2.6-V related pins have selectable output buffer drive strengths which are controlled by the COM[0] bit in the USIU's system clock and reset control register (SCCR). The control is as follows:

0 = 2.6-V bus pins full drive (50-pF load)*
1 = 2.6-V bus pins reduced drive (25-pF load)

* The bus pin drive selectability definition is inverted from the selectability of the pin control in the PDMCR register (for the TPU, QADC64E, USIU (SGPIO), QSPI, TouCAN, QSCI, and MIOS pins).

2.5.2 Pin State During Reset

While $\overline{\text{HRESET}}$ is asserted, the reset configuration value is latched from the data bus into various bits on the part. The function of many pins depends upon the value latched. If the value on the data bus changes, then the function of various pins may also change. This is especially true if the reset configuration word (RCW) comes from the flash, since the flash won't drive the RCW until 256 clocks after the start of $\overline{\text{HRESET}}$. However, the pins must not cause any spurious conditions or consume an excessive amount of power during reset. To prevent these conditions, the pins need to have a defined reset state. **Table 2-6** describes the reset state of the pins based on pin functionality.

All pins are initialized to a "reset state" during reset. This state remains active until reset is negated or until software disables the pull-up or pull-down device based on the pin functionality. Upon assertion of the corresponding bits in the pin control registers and negation of reset, the pin acquires the functionality that was programmed.

2.5.3 Power-On Reset and Hard Reset

Power-on reset and hard reset affect the functionality of the pins out of reset. (During soft reset, the functionality of the pins is unaltered.) Upon assertion of the power-on reset signal ($\overline{\text{PORESET}}$/$\overline{\text{TRST}}$) the functionality of the pin is not yet known. The weak pull-up or weak pull-down resistors are enabled. The reset configuration word configures the system, and towards the end of reset the pin functionality is known. Based upon pin functionality, the pull-up or pull-down devices are either disabled immediately at the negation of reset or remain enabled. This is shown in **Table 2-6**.

NOTE

PD refers to a weak pull-down, PU_2.6V refers to a weak pull-up to 2.6 V, and PU_5V refers to a weak pull-up to 5 V. All control of the weak-pull devices is in the PDMCR, described in **Table 2-3**

Hard reset can occur at any time, and there may be a bus cycle pending. For this reason, the bits in PDMCR that control the enabling and disabling of the pull-up or pull-down resistors in the pads are set or reset synchronously. (PORESET/TRST affects these bits asynchronously.) This causes the pull-up or pull-down resistors to be enabled at a time when they do not cause contention on the pins and are disabled before they can cause any contention on the pins.

CAUTION

2.6-V inputs are 5-V tolerant, but 2.6-V outputs are not. Do not connect 2.6-V outputs to a driver or pull-up greater than 3.1 V.

2.5.4 Pin Reset States

Table 2-6 summarizes the reset states of all the pins on the MPC565 / MPC566.

Table 2-6 Pin Reset State

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
USIU					
ADDR[8:31]/ SGPIOA[8:31]	ADDR[8:31][1]	I/O	2.6 V	PD until reset negates[2]	Controlled by SC bit in the reset config word. See **Table 6-11**
	SGPIOA[8:31][3]	I/O	5 V	PD until PRDS is set	
DATA[0:31]/ SGPIOD[0:31]	DATA[0:31][1]	I/O	2.6 V	PD until reset negates	Controlled by SC bit in the reset config word. See **Table 6-11**.
	SGPIOD[0:31][3]	I/O	5 V	PD until PRDS is set	
IRQ[0]/SGPIOC[0]	IRQ[0]	I	2.6 V	Pin floats during reset, ext. PU required.	IRQ[0]
	SGPIOC[0]	I/O	2.6 V[4]	Pin floats during reset	
IRQ[1]/ RSV/SGPIOC[1]	IRQ[1]	I	2.6 V	PD until reset negates[2,5]	IRQ[1]
	RSV[6]	O	2.6 V	PD until reset negates[2]	
	SGPIOC[1][3]	I/O	5 V	PD until PRDS is set	
IRQ[2]/ CR/SGPIOC[2]/ MTS	IRQ[2]	I	2.6 V	PD until reset negates[2,5]	IRQ[2]
	CR	I	2.6 V	PD until reset negates[2,5]	
	SGPIOC[2][3]	I/O	5 V	PD until PRDS is set	
	MTS[6]	O	2.6 V	PD until PRDS negates	
IRQ[3]/ KR, RETRY/ SGPIOC[3]	IRQ[3]	I	2.6 V	PD until reset negates[2,5]	IRQ[3]
	KR, RETRY[6]	I/O	2.6 V	PD when driver not enabled[7]	
	SGPIOC[3][3]	I/O	5 V	PD until PRDS is set	

Table 2-6 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
IRQ[4]/ AT[2]/ SGPIOC[4]	IRQ[4]	I	2.6 V	PD until reset negates[2,5]	IRQ[4]
	AT[2][6]	O	2.6 V	PD until reset negates[2]	
	SGPIOC[4]	I/O	5 V	PD until PRDS is set	
IRQ[5]/ SGPIOC[5]/ MODCK[1][8]	IRQ[5]	I	2.6 V	PU_2.6V until reset negates[2,9]	MODCK[1] until reset negates
	SGPIOC[5][6]	I/O	2.6 V	PU_2.6V until SPULL_DIS0 is set	
	MODCK[1]	I	2.6 V	PU_2.6V until reset negates[2]	
IRQ[6:7]/ MODCK[2:3][8]	IRQ[6:7]	I	2.6 V	PU_2.6V until SPRDS is set[9]	MODCK[2:3] until reset negates
	MODCK[2:3]	I	2.6 V	PU_2.6V until reset negates	
TSIZ[0:1]	TSIZ[0:1][6]	I/O	2.6 V	PD when driver not enabled or until SPRDS is set	TSIZ[0:1]
RD/WR	RD/WR[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	RD/WR
BURST	BURST[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	BURST
BDIP	BDIP[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	BDIP
TS[10]	TS[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set An external pull-up is required in order to guarantee the pin does not assert between bus cycles.	TS
TA[10]	TA[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	TA
TEA	TEA[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set An external pull-up is required in order to negate the pin in appropriate time	TEA
RSTCONF/TEXP[8]	RSTCONF	I	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	RSTCONF until reset negates. Following reset, the function is defined by the RCTX bit in the SIUMCR. See **Table 6-5**.
	TEXP[6]	O	2.6 V		
OE	OE[6]	O	2.6 V	PU_2.6V until reset negates	OE
BI/STS	BI[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	Controlled by DBGC in the reset config word. See **Table 6-8**.
	STS[6]	O	2.6 V		
CS[0:3]	CS[0:3][6]	O	2.6 V	PU_2.6V until reset negates	CS[0:3]
WE[0:3]/BE[0:3]/ AT[0:3]	WE[0:3]/BE[0:3][6]	O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	Controlled by bit ATWC (bit 12) of the Reset Configuration Word. See **Table 6-7**.
	AT[0:3][6]	O	2.6 V		

Table 2-6 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
PORESET/ TRST[8, 11]	PORESET/TRST	I	2.6 V	—	PORESET/TRST
HRESET[8]	HRESET	I/O	2.6 V[12]	PU_2.6V when driver not enabled An external pull-up is required in order to negate the pin in appropriate time	HRESET
SRESET[8]	SRESET	I/O	2.6 V[12]	PU_2.6V when driver not enabled An external pull-up is required in order to negate the pin in appropriate time	SRESET
SGPIOC[6]/ FRZ/ PTR	SGPIOC[6][3]	I/O	5 V	PD until PRDS is set	PTR
	FRZ[6]	O	2.6 V	PD until reset negates[2]	
	PTR[6]	O	2.6 V	PD until reset negates[2]	
SGPIOC[7]/ IRQOUT/LWP[0]	SGPIOC[7][3]	I/O	5 V	PD until PRDS is set	LWP[0]
	IRQOUT[6]	O	2.6 V	PD until reset negates[2]	
	LWP[0][6]	O	2.6 V	PD until reset negates[2]	
BG/ VF[0]/ LWP[1]	BG[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	Controlled by DBGC in reset config word. See **Table 6-8**.
	VF[0][6]	O	2.6 V		
	LWP[1][6]	O	2.6 V		
BR/ VF[1]/ IWP[2]	BR[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	Controlled by DBGC in reset config word. See **Table 6-8**.
	VF[1][6]	O	2.6 V		
	IWP[2][6]	O	2.6 V		
BB/ VF[2]/ IWP[3]	BB4[6]	I/O	2.6 V	PU_2.6V when driver not enabled or until SPRDS is set	Controlled by DBGC in reset config word. See **Table 6-8**
	VF[2][6]	O	2.6 V		
	IWP[3][6]	O	2.6 V		
IWP[0:1]/ VFLS[0:1]	IWP[0:1][6]	O	2.6 V	Output Only, no weak pull	Controlled by DBGC in the reset config word. See **Table 6-8**.
	VFLS[0:1][6]	O	2.6 V		
TMS	TMS	I	2.6 V	PU_2.6V until SPULL_DIS1 is set	TMS
TDI/ DSDI	TDI	I	2.6 V	PU_2.6V until SPULL_DIS1 is set	Controlled by DBPC in reset config word. See **Table 6-9**
	DSDI	I	2.6 V		
TCK/ DSCK	TCK	I	2.6 V	PD until SPULL_DIS1 is set	Controlled by DBPC in reset config word. See **Table 6-9**
	DSCK	I	2.6 V		
TDO/ DSDO	TDO[6]	O	2.6 V	—	Controlled by DBPC in reset config word. See **Table 6-9**
	DSDO[6]	O	2.6 V		
JCOMP	JCOMP[13]	I	2.6 V	—	JCOMP

Table 2-6 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
XTAL[8]	XTAL	I	2.6 V	—	XTAL
EXTAL[8]	EXTAL	I	2.6 V	—	EXTAL
XFC	XFC	I	2.6 V	—	XFC
CLKOUT	CLKOUT[6]	O	2.6 V	—	CLKOUT
EXTCLK[8]	EXTCLK	I	2.6 V	—	EXTCLK
ENGCLK/ BUCLK	ENGCLK[3, 6]	O	2.6 / 5 V	—	ENGCLK (2.6 V)
	BUCLK[6]	O	2.6 V	—	
VDDSYN	VDDSYN	I	2.6 V	—	VDDSYN
VSSSYN	VSSSYN	I	0 V	—	VSSSYN
PULL_SEL[14]	PULL_SEL	I	5 V	PU_5	PULL_SEL
QSMCM_A/QSMCM_B/DLCMD2					
A_PCS[0]/$\overline{SS}$/ QGPIO[0]	PCS[0]	I/O	5 V	PU_5V until PRDS is set	A_QGPIO[0]
	$\overline{SS}$	I/O	5 V		
	QGPIO[0]	I/O	5 V		
A_PCS[1:3]/ QGPIO[1:3]	PCS[1:3]	I/O	5 V	PU_5V until PRDS is set	A_QGPIO[1:3]
	QGPIO[1:3]	I/O	5 V		
A_MISO/ QGPIO[4]	MISO	I/O	5 V	PU_5V until PRDS is set	A_QGPIO[4]
	QGPIO[4]	I/O	5 V		
A_MOSI/ QGPIO[5]	MOSI	I/O	5 V	PU_5V until PRDS is set	A_QGPIO[5]
	QGPIO[5]	I/O	5 V		
A_SCK/ QGPIO[6]	SCK	I/O	5 V	PU_5V until PRDS is set	A_QGPIO[6]
	QGPIO[6]	I/O	5 V		
A_TXD[1:2]/ QGPO[1:2]	TXD[1:2]	O	5 V	PU_5V until PRDS is set	A_QGPO[1:2]
	QGPO[1:2]	O	5 V		
A_RXD[1:2]/ QGPI[1:2]	RXD[1:2]	I	5 V	None	A_QGPI[1:2]
	QGPI[1:2]	I	5 V		
B_PCS[0]/ $\overline{SS}$/ QGPIO[0]	PCS[0]	I/O	5 V	PU_5V until PRDS is set	B_QGPIO[0]
	$\overline{SS}$	I/O	5 V		
	QGPIO[0]	I/O	5 V		
B_PCS[1:2]/ QGPIO[1:2]	PCS[1:2]	I/O	5 V	PU_5V until PRDS is set	B_QGPIO[1:2]
	QGPIO[1:2]	I/O	5 V		
B_PCS[3]/ J1850_TX	PCS[3]	I/O	5 V	PU_5V until PRDS is set	J1850_TX
	J1850_TX	I/O	5 V		
B_MISO/ QGPIO[4]	MISO	I/O	5 V	PU_5V until PRDS is set	B_QGPIO[4]
	QGPIO[4]	I/O	5 V		
B_MOSI/ B_QGPIO[5]	MOSI	I/O	5 V	PU_5V until PRDS is set	B_QGPIO[5]
	QGPIO[5]	I/O	5 V		
B_SCK/QGPIO[6]	SCK	I/O	5 V	PU_5V until PRDS is set	B_QGPIO[6]
	QGPIO[6]	I/O	5 V		

Table 2-6 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
B_TXD[1:2]/ QGPO[1:2]	TXD[1:2]	O	5 V	PU_5V until PRDS is set	B_QGPO[1:2]
	QGPO[1:2]	O	5 V		
B_RXD[1]/ QGPI[1]	RXD[1]	I	5 V	None	B_QGPI[1]
	QGPI[1]	I	5 V		
B_RXD[2]/ J1850_RX	RXD[2]	I	5 V	None	J1850_RX
	J1850_RX	I	5 V		
B_ECK	B_ECK	I	5 V	PU_5V until PRDS is set	—
MIOS14					
MDA[11:15], [27:31]	MDA[11:15], [27:31]	I/O	5 V	Pull device enabled until PULL_DIS[0] is set [15]	MDA[11:15], [27:31]
MPWM[0:3], [16:19]	MPWM[0:3], [16:19]	I/O	5 V	Pull device enabled until PULL_DIS[0] is set [15]	MPWM[0:3], [16:19]
VF[0:2]/ MPIO32B[0:2]	VF[0:2][6]	O	2.6 V	Pull down until PULL_DIS[0] is set	MPIO32B[0:2]
	MPIO32B[0:2][3]	I/O	5 V		
VFLS[0:1]/ MPIO32B[3:4]	VFLS[0:1][6]	O	2.6 V	Pull down until PULL_DIS[0] is set	MPIO32B[3:4]
	MPIO32B[3:4][3]	I/O	5 V		
MPWM[4:5]/ MPIO32B[5:6]	MPWM[4:5]	I/O	5 V	Pull device enabled until PULL_DIS[0] is set[15]	MPIO32B[5:6]
	MPIO32B[5:6]	I/O	5 V		
MDO[7:4]/ MPIO32B[7:10]	MDO[7:4][6]	O	2.6 V	Pull down until PULL_DIS[0] is set	Controlled by READI enable ($\overline{EVTI}$ and MDI[0])
	MPIO32B[7:10][3]	I/O	5 V		
MPWM[20:21]/ MPIO32B[11:12]	MPWM[20:21]	I/O	5 V	Pull device enabled until PULL_DIS[0] is set[15]	MPIO32B[11:12]
	MPIO32B[11:12]	I/O	5 V		
C_CNTX0/ MPIO32B[13]	C_CNTX0	I/O	5 V	Pull device enabled until PULL_DIS[3] is set[16]	MPIO32B[13]
	MPIO32B[13]	I/O	5 V		
C_CNRX0/ MPIO32B[14]	C_CNRX0	I/O	5 V	Pull device enabled until PULL_DIS[3] is set[16]	MPIO32B[14]
	MPIO32B[14]	I/O	5 V		
MPIO32B[15]	MPIO32B[15]	I/O	5 V	Pull device enabled until PULL_DIS[0] is set[15]	MPIO32B[15]
EXTAL32	EXTAL32	I	2.6 V	—	EXTAL32
XTAL32	XTAL32	I	2.6 V	—	XTAL32
VDDRTC	VDDRTC	I	2.6 V	—	VDDRTC
VSSRTC	VSSRTC	I	0 V	—	VSSRTC
TPU3_A/TPU3_B/TPU3_C					
A_TPUCH[0:15]	A_TPUCH[0:15]	I/O	5 V	Pull device enabled until PRDS is set[17]	A_TPUCH[0:15]
A_T2CLK	A_T2CLK	I/O	5 V	Pull up enabled until T2CLK_PU is set	A_T2CLK
B_TPUCH[0:15]	B_TPUCH[0:15]	I/O	5 V	Pull device enabled until PRDS is set[17]	B_TPUCH[0:15]
B_T2CLK	B_T2CLK	I/O	5 V	Pull up enabled until T2CLK_PU is set	B_T2CLK

Table 2-6 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
C_TPUCH[0:15]	C_TPUCH[0:15]	I/O	5 V	Pull device enabled until PRDS is set[17]	C_TPUCH[0:15]
C_T2CLK	C_T2CLK	I/O	5 V	Pull up enabled until T2CLK_PU is set	C_T2CLK
QADC64_A/QADC64_B					
ETRIG[1:2]	ETRIG[1:2]	I	5 V	PD until PULL_DIS0 is set	ETRIG[1:2]
AN[44]/ANW/ A_PQB[0]	AN[44]	I	5 V	PU_5V until PRDS is set	AN[44]
	ANW	I	5 V	PU_5V until PRDS is set	
	A_PQB[0]	I	5 V	PU_5V until PRDS is set	
AN[45]/ANX/ A_PQB[1]	AN[45]	I	5 V	PU_5V until PRDS is set	AN[45]
	ANX	I	5 V	PU_5V until PRDS is set	
	A_PQB[1]	I	5 V	PU_5V until PRDS is set	
AN[46]/ANY/ A_PQB[2]	AN[46]	I	5 V	PU_5V until PRDS is set	AN[46]
	ANY	I	5 V	PU_5V until PRDS is set	
	A_PQB[2]	I	5 V	PU_5V until PRDS is set	
AN[47]/ANZ/ A_PQB[3]	AN[47]	I	5 V	PU_5V until PRDS is set	AN[47]
	ANZ	I	5 V	PU_5V until PRDS is set	
	A_PQB[3]	I	5 V	PU_5V until PRDS is set	
AN[48:51]/ A_PQB[4:7]	AN[48:51]	I	5 V	PU_5V until PRDS is set	AN[48:51]
	A_PQB[4:7]	I	5 V	PU_5V until PRDS is set	
AN[52:54]/ A_MA[0:2]/ PQA[0:2]	AN[52:54]	I	5 V	PU_5V until PRDS is set	AN[52:54]
	A_MA[0:2]	I	5 V	PU_5V until PRDS is set	
	A_PQA[0:2]	I/O	5 V	PU_5V until PRDS is set	
AN[55:59]/ A_PQA[3:7]	AN[55:59]	I	5 V	PU_5V until PRDS is set	AN[55:59]
	A_PQA[3:7]	I/O	5 V	PU_5V until PRDS is set	
AN[64:71]/ B_PQB[0:7]	AN[64:71]	I	5 V	PU_5V until PRDS is set	AN[64:71]
	B_PQB[0:7]	I	5 V	PU_5V until PRDS is set	
AN[72:74]/ B_MA[0:2]/ B_PQA[0:2]	AN[72:74]	I	5 V	PU_5V until PRDS is set	AN[72:74]
	B_MA[0:2]	I	5 V	PU_5V until PRDS is set	
	B_PQA[0:2]	I/O	5 V	PU_5V until PRDS is set	
AN[75:79]/ B_PQA[3:7]	AN[75:79]	I	5 V	PU_5V until PRDS is set	AN[75:79]
	B_PQA[3:7]	I/O	5 V	PU_5V until PRDS is set	
AN[80:87]	AN[80:87]	I	5 V	None	AN[80:87]
VRH	VRH	I	5 V	—	VRH
VRL	VRL	I	—	—	VRL
VDDA	VDDA	I	5 V	—	VDDA
VSSA	VSSA	I	—	—	VSSA
TouCAN_A/TouCAN_B					
A_CNTX0	A_CNTX0	O	5 V	PU_5V until PULL_DIS2 is set	A_CNTX0
B_CNTX0	B_CNTX0	O	5 V	PU_5V until PULL_DIS2 is set	B_CNTX0
A_CNRX0	A_CNRX0	I	5 V	PU_5V until PULL_DIS2 is set	A_CNRX0

Table 2-6 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State	Function After PORESET/TRST or HRESET
B_CNRX0	B_CNRX0	I	5 V	PU_5V until PULL_DIS2 is set	B_CNRX0
UC3F					
EPEE	EPEE	I	2.6 V	PU_2.6V	EPEE
B0EPEE	B0EPEE	I	2.6 V	PU_2.6V	B0EPEE
VFLASH	VFLASH	I	5 V	—	VFLASH
VDDF	VDDF	I	2.6 V	—	VDDF
VSSF	VSSF	I	2.6 V	—	VSSF
READI					
$\overline{\text{MSEO}}$	$\overline{\text{MSEO}}$[6]	O	2.6 V	PU_2.6V while $\overline{\text{RSTI}}$ is asserted	$\overline{\text{MSEO}}$
MDO[3]	MDO[3][6]	O	2.6 V	PU_2.6V while $\overline{\text{RSTI}}$ is asserted	MDO[3]
MDO[2]	MDO[2][6]	O	2.6 V	PU_2.6V while $\overline{\text{RSTI}}$ is asserted	MDO[2]
MDO[1]	MDO[1][6]	O	2.6 V	PU_2.6V while $\overline{\text{RSTI}}$ is asserted	MDO[1]
MDO[0]	MDO[0][6]	O	2.6 V	PU_2.6V while $\overline{\text{RSTI}}$ is asserted	MDO[0]
MCKO	MCKO[6]	O	2.6 V	PU_2.6V while $\overline{\text{RSTI}}$ is asserted	MCKO
$\overline{\text{RSTI}}$	$\overline{\text{RSTI}}$	I	2.6 V	PD until PULL_DIS4 is set	$\overline{\text{RSTI}}$
$\overline{\text{EVTI}}$	$\overline{\text{EVTI}}$	I	2.6 V	PU_2.6V until PULL_DIS4 is set	$\overline{\text{EVTI}}$
$\overline{\text{MSEI}}$	$\overline{\text{MSEI}}$	I	2.6 V	PU_2.6V until PULL_DIS4 is set	$\overline{\text{MSEI}}$
MDI[1]	MDI[1]	I	2.6 V	PU_2.6V until PULL_DIS4 is set	MDI[1]
MDI[0]	MDI[0]	I	2.6 V	PU_2.6V until PULL_DIS4 is set	MDI[0]
MCKI	MCKI	I	2.6 V	PU_2.6V until PULL_DIS4 is set	MCKI
Global Power Supplies					
QVDDL	QVDDL	I	2.6 V	—	QVDDL
NVDDL	NVDDL	I	2.6 V	—	NVDDL
VDDH	VDDH	I	5 V	—	VDDH
VDD	VDD	I	2.6 V	—	VDD
VSS	VSS	I	0 V	—	VSS
KAPWR[8]	KAPWR	I	2.6 V	—	KAPWR
VDDSRAM[1:3]	VDDSRAM[1:3]	I	2.6 V	—	VDDSRAM[1:3]

NOTES:

1. 2.6-V outputs cannot be connected to a pull-up or driver greater than 3.1 V.
2. During reset, the output enable to the pad driver is negated and the PD is active. After reset is negated, the PD is disabled.
3. Care should be taken that neither a pull-up to greater than 3.1 V or an external output that can drive greater than 3.1 V is connected to this pin while the 2.6-V driver is enabled.
4. SGPIO[0] was 5 V on mask set K85H.
5. This pin requires a pull-up to 2.6 V if interrupts are ever enabled for this IRQ input.
6. 2.6-V outputs cannot be connected to a pull-up or driver greater than 3.1 V.
7. Pull-up/pull-down is active when pin is defined as an input and/or during reset; therefore, output enable is negated. This also means that external pull-up/pull-down is *not* required unless specified.
8. These pins are powered by KAPWR (keep-alive power supply).

9. The MODCK[1:3] are shared functions with $\overline{\text{IRQ}}$[5:7]. If $\overline{\text{IRQ}}$[5:7] are used as interrupts, the interrupt source should be removed during $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ to insure the MODCK pins are in the correct state on the rising edge of $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$.
10. This pin is an active negate signal and require an external pull-up resister. On dual-voltage type 4 pads, hysteresis is always enabled on the 5-V input buffer, and hysteresis affects only the 2.6-V input buffers on which hysteresis is enabled.
11. This pin was $\overline{\text{PORESET}}$ only on mask set K85H.
12. This pin is 5-V tolerant, even when in output mode.
13. This pin was $\overline{\text{TRST}}$ in mask set K85H.
14. This pin was A_ECK in mask set K85H.
15. Whether the Pull device is a pull-up or a pull-down is determined by the state of the PULL_SEL pin.
16. Whether the Pull device is a pull-up or a pull-down is determined by the state of the PULL_SEL pin.
17. Whether the Pull device is a pull-up or a pull-down is determined by the state of the PULL_SEL pin.

2.6 Pad Types

There are different pad types based on functional characteristics. Even pads with the same functionality may be different due to different electrical characteristics. All 5-V inputs have hysteresis. Refer to **Figure 2-1**.

Table 2-7 Functional Pad Types

Type	Name	V	Dir.	Delay (ns)		Drive Strength (Rise/Fall)	Drive Load	Weak Devices	Hyst.
				In	Out[1]	Fast; Slow	Fast; Slow	PU; PD	
1	pad_5vsa	5 V	IO	5	17 ; 400	10 ns ; 200 ns	50 pF ; 50 pF	Selectable	Selectable
2	pad_5vfa	5 V	IO	5	17 ; 100	10 ns ; 40 ns	50 pF ; 50 pF	Selectable	Selectable
					16 ; 100	9 ns ; 40 ns	45 pF ; 45 pF		
					27 ; 110	18 ns ; 47 ns	90 pF ; 90 pF		
3	pad_26v	2.6 V	IO	4	5 ; 5	2.9 ns ; 2.9 ns	25 pF ; 50 pF	Selectable	Selectable
4	pad_26v5vs	2.6 V	IO	4	5 ; 5	2.9 ns ; 2.9 ns	25 pF ; 50 pF	PD Selectable	Selectable
		5 V	IO	5	17 ; 400	10 ns ; 200 ns	50 pF ; 50 pF	PD Selectable	Enabled
5	pad_5vh	5 V	IO	5	30 ; 400	21 ns ; 200 ns	200 pF ; 50 pF	Selectable	Selectable
6	pad_5vido	5 V	I	5	NA	NA	NA	NA	Selectable
7	pad_extclk	2.6 V	I		NA	NA	NA	NA	NA
8	pad_e_xtal_oscpll	2.6 V	IO	NA	NA	NA ; NA	NA ; NA	NA	NA
9	pad_e_xtal_osc32	2.6 V	IO	NA	NA	NA ; NA	NA ; NA	NA	NA
10	pad_26vf	2.6 V	IO	4	5 ; 5	2.3 ns ; 2.3 ns	25 pF ; 50 pF	Selectable	Selectable
11	pad_26vs5vr	2.6 V	IO	4	11 ; 11	7 ns ; 7 ns	25 pF ; 50 pF	PD Selectable	Selectable
		5 V	IO	5	12 ; 50	6 ns ; 25 ns	25 pF ; 25 pF	PD Selectable	Enabled

NOTES:

1. Output delay includes pad prop delay (out) + rise/fall time.

Table 2-8 Other Pad Types

Name	V	Used For
pad_vddh	5 V	VDDH
pad_nvddl	2.6 V	NVDDL
pad_qvddl	2.6 V	QVDDL
pad_vddint	2.6 V	VDD, VDDSRAM[1:3], VDDF, VDDSYN, VDDRTC
pad_vdda	5 V	VDDA
pad_vss		VSS
pad_vssint		VSSA, VSSF, VRL
pad_vsssyn		VSSSYN, VSSRTC
pad_vflashvrh	5 V	VFLASH, VRH, ALTREF
pad_kapwr	2.6 V	KAPWR
pad_xfc	2.6 V	XFC
pad_esdcnrcell		CORNER

2.7 Electrical Characteristics

2.7.1 Target DC Characteristics

Table 2-9 Target DC Electrical Characteristics

Spec	Characteristic	Symbol	Min	Max	Unit
1	2.6-V Supply Voltage	VDDI	2.5	2.7	V
2	5-V Supply Voltage	VDDH	4.75	5.25	V
3	2.6-V Input High Voltage	VIH_L	2.0	VDDH + 0.3	V
4	5-V Input High Voltage	VIH_H	0.7 * VDDH	VDDH + 0.3	V
5	2.6-V Input Low Voltage	VIL_L	VSS - 0.3	0.8	V
6	5-V Input Low Voltage	VIL_H	VSS - 0.3	0.48 * VDDH	V
7	Input Hysteresis	VHYS	500 (target spec)		mV
8	Mode Select/Pull-up/Pull-down Current	IACT	20	130	µA
9	Input Leakage Current (pull-up/pull-down inactive)	IINACT	—	2.5	µA
10	2.6-V Output High Voltage [IOH_L = -1 mA] (IOH_L = -2 mA)	VOH_L	[2.4] [2.3]	—	V
11	5-V Output High Voltage (IOH_H = -2 mA)	VOH_H	VDDH - 0.7	—	V
12	2.6-V Output Low Voltage [IOL_L = 3.2 mA] (Iol_l =2mA)	VOL_L	—	[0.5] [0.45]	V
13	5-V Output Low Voltage (IOL_H = 2 mA)	VOL_H	—	0.5	V

These DC characteristics are not all inclusive and any individual pad. Electrical characteristics may have other requirements. In case of a conflict, the **APPENDIX E ELECTRICAL CHARACTERISTICS** gives the actual electrical characteristics of any particular pin, but **Table 2-9** can be useful to show general capabilites of the pads.

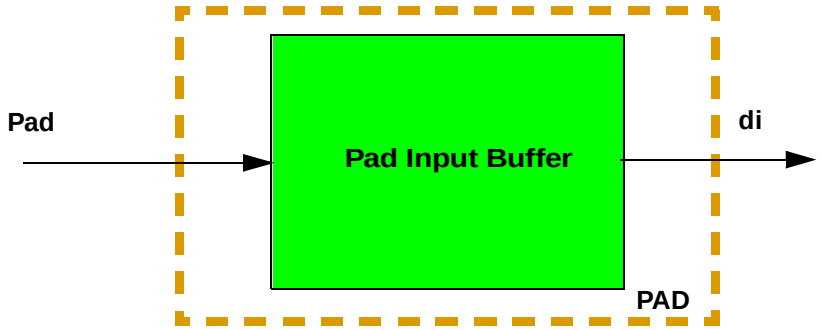
2.7.2 Pad Measurement Criteria

- Pad rise/fall times measured between VOL and VOH of output driver. (For 2.6-V drivers, lowest minimum VOH is used.)
- Pad prop delays for outputs are measured at VDD/2 for internal signals to VOL or VOH at pin load.
- Propagation delays for inputs are measured from VIL for a falling input or VIH for a rising input at the pin, to VDD/2 at internal signal load. Rise/fall times for the input signal at the internal signal load are measured from 10% to 90% of VDD. The rise/fall time for the input signal at the pad shall be two ns for the full swing from VSS to VDD.
- All inputs except the oscillator are 5-V friendly.

- Minimum input buffer hysteresis is 500 mV.
- Weak pull-up current is measured at VIL and weak pull-down current is measured at VIH.

2.7.2.1 Input Buffer

1. Voltages received above VIH min. guarantee a logical “1” response.
2. Voltages received below VIL max guarantee a logical “0” response.
3. Received voltages that fall between the two thresholds may be interpreted by the input buffer as a “1”, as a “0”, or as an indeterminate state.



Input prop delay measured from pad to di_line.

Figure 2-1 Input Propagation Delay

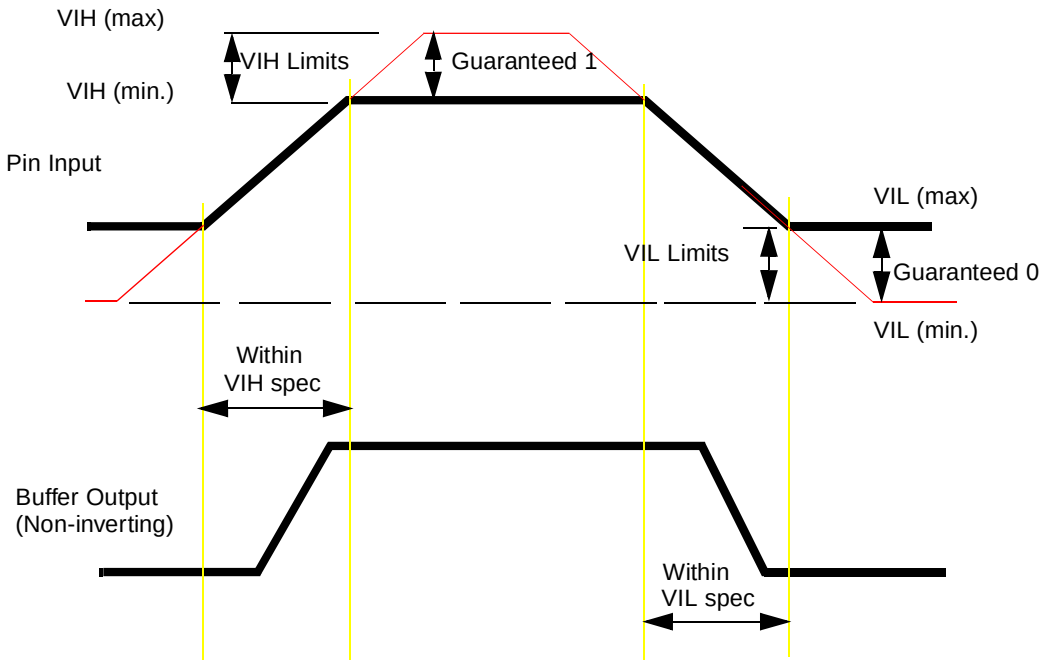
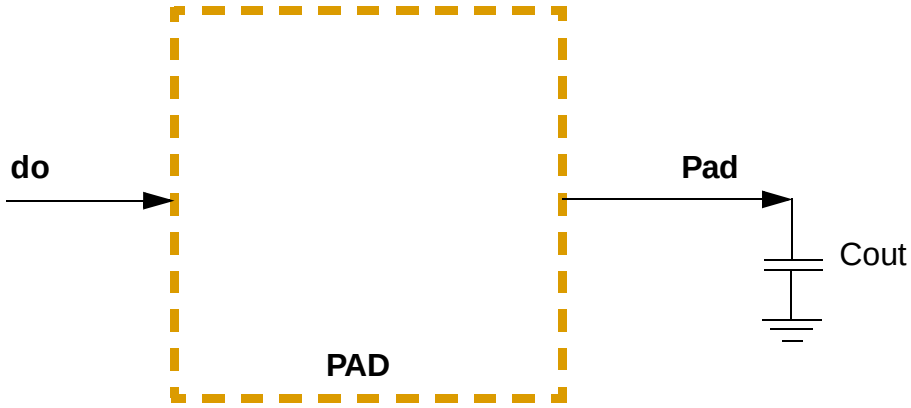


Figure 2-2 Input Levels

2.7.2.2 Output Driver



NOTE: Package parasitic resistance and inductance have been added to simulation delay path.

Figure 2-3 Output Propagation Delay

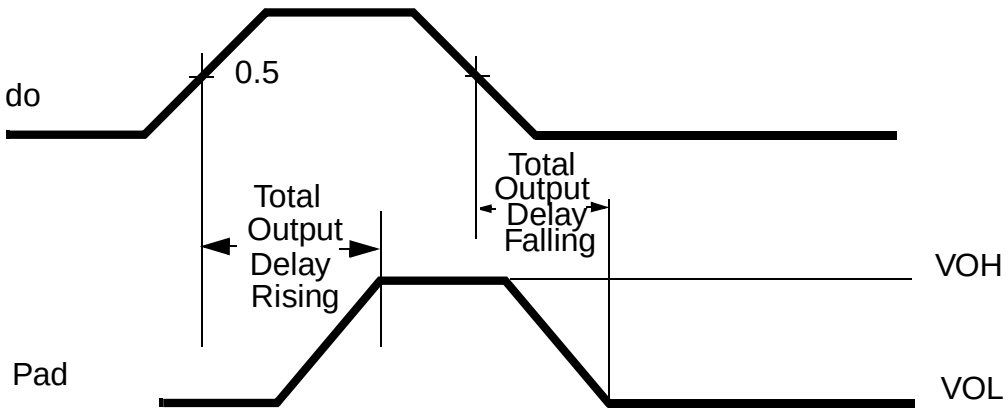


Figure 2-4 Output Levels and Timing

Table 2-10 Pin Names and Abbreviations

Pin List	Pin Name	Ball	Pad Type
DATA[0:31]/SGPIOD[0:31]	data_sgpiod[0]	AF3	26v5vs
	data_sgpiod[1]	AE4	26v5vs
	data_sgpiod[2]	AF4	26v5vs
	data_sgpiod[3]	AE5	26v5vs
	data_sgpiod[4]	AF5	26v5vs
	data_sgpiod[5]	AE6	26v5vs
	data_sgpiod[6]	AF6	26v5vs
	data_sgpiod[7]	AE7	26v5vs
	data_sgpiod[8]	AF7	26v5vs
	data_sgpiod[9]	AE8	26v5vs
	data_sgpiod[10]	AF8	26v5vs
	data_sgpiod[11]	AE9	26v5vs
	data_sgpiod[12]	AF9	26v5vs
	data_sgpiod[13]	AE10	26v5vs
	data_sgpiod[14]	AF10	26v5vs
	data_sgpiod[15]	AE11	26v5vs
	data_sgpiod[16]	AF11	26v5vs
	data_sgpiod[17]	AE12	26v5vs
	data_sgpiod[18]	AF12	26v5vs
	data_sgpiod[19]	AD13	26v5vs
	data_sgpiod[20]	AC12	26v5vs
	data_sgpiod[21]	AD12	26v5vs
	data_sgpiod[22]	AC11	26v5vs
	data_sgpiod[23]	AD11	26v5vs
	data_sgpiod[24]	AC10	26v5vs
	data_sgpiod[25]	AD10	26v5vs
	data_sgpiod[26]	AD9	26v5vs
	data_sgpiod[27]	AC8	26v5vs
	data_sgpiod[28]	AD8	26v5vs
	data_sgpiod[29]	AC7	26v5vs
	data_sgpiod[30]	AD7	26v5vs
	data_sgpiod[31]	AD6	26v5vs

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
ADDR[8:31]/SGPIOA[8:31]	addr_sgpioa[8]	U3	26v5vs
	addr_sgpioa[9]	V3	26v5vs
	addr_sgpioa[10]	V4	26v5vs
	addr_sgpioa[11]	W3	26v5vs
	addr_sgpioa[12]	W4	26v5vs
	addr_sgpioa[13]	Y3	26v5vs
	addr_sgpioa[14]	Y4	26v5vs
	addr_sgpioa[15]	AA3	26v5vs
	addr_sgpioa[16]	U1	26v5vs
	addr_sgpioa[17]	U2	26v5vs
	addr_sgpioa[18]	V1	26v5vs
	addr_sgpioa[19]	V2	26v5vs
	addr_sgpioa[20]	W1	26v5vs
	addr_sgpioa[21]	W2	26v5vs
	addr_sgpioa[22]	Y1	26v5vs
	addr_sgpioa[23]	Y2	26v5vs
	addr_sgpioa[24]	AA1	26v5vs
	addr_sgpioa[25]	AA2	26v5vs
	addr_sgpioa[26]	AB1	26v5vs
	addr_sgpioa[27]	AB2	26v5vs
	addr_sgpioa[28]	AC1	26v5vs
	addr_sgpioa[29]	AD1	26v5vs
	addr_sgpioa[30]	AA4	26v5vs
	addr_sgpioa[31]	AB3	26v5vs
$\overline{\text{IRQ}}$[0]/SGPIOC[0]	irq0_b_sgpioc0	AF16	26v
$\overline{\text{IRQ}}$[1]/$\overline{\text{RSV}}$/SGPIOC[1]	irq1_b_rsv_b_sgpioc1	AF13	26v5vs
$\overline{\text{IRQ}}$[2]/CR/SGPIOC[2]/MTS	irq2_b_cr_b_sgpio2_mts	AD16	26v5vs
$\overline{\text{IRQ}}$[3]/$\overline{\text{KR}}$, $\overline{\text{RETRY}}$/SGPIOC[3]	irq3_b_kr_b_retry_b_sgpioc3	AE13	26v5vs
$\overline{\text{IRQ}}$[4]/AT[2]/SGPIOC[4]	irq4_b_at2_sgpioc4	AD14	26v5vs
$\overline{\text{IRQ}}$[5]/SGPIOC[5]/MODCK[1]	irq5_b_sgpioc5_modck1	AD25	26v5vs
$\overline{\text{IRQ}}$[6:7]/MODCK[2:3]	irq6_b_modck2	AB24	26v
	irq7_b_modck3	AC25	26v
TSIZ[0:1]	tsiz0	AD19	26v
	tsiz1	AF19	26v
RD/$\overline{\text{WR}}$	rd_wr_b	AE15	26v
$\overline{\text{BURST}}$	burst_b	AE19	26v
$\overline{\text{BDIP}}$	bdip_b	AE21	26v
$\overline{\text{TS}}$	ts_b	AE20	26v
$\overline{\text{TA}}$	ta_b	AF20	26v
$\overline{\text{TEA}}$	tea_b	AD15	26v
$\overline{\text{RSTCONF}}$/TEXP	rstconf_b_texp	AB25	26v
$\overline{\text{OE}}$	oe_b	AE16	26v

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
$\overline{BI}/\overline{STS}$	bi_b_sts_b	AC19	26v
$\overline{CS}$[0:3]	cs0_b	AE18	26v
	cs1_b	AD18	26v
	cs2_b	AF18	26v
	cs3_b	AC18	26v
$\overline{WE}$[0:3]/$\overline{BE}$[0:3]/AT[0:3]	we_b_be_b_at[0]	AE17	26v
	we_b_be_b_at[1]	AC16	26v
	we_b_be_b_at[2]	AD17	26v
	we_b_be_b_at[3]	AF17	26v
$\overline{PORESET}/\overline{TRST}$[1]	poreset_b_trst_b	AA23	26v
$\overline{HRESET}$	hreset_b	AB23	26v (Rev0); 5vsa (RevA)
$\overline{SRESET}$	sreset_b	AC24	26V (Rev0); 5vsa (RevA)
SGPIOC[6]/FRZ/$\overline{PTR}$	sgpioc6_frz_ptr_b	T4	26v5vs
SGPIOC[7]/$\overline{IRQOUT}$/LWP[0]	sgpioc7_irqout_b_lwp0	AC14	26v5vs
$\overline{BG}$/VF[0]/LWP[1]	bg_b_vf0_lwp1	AF14	26v
$\overline{BR}$/VF[1]/IWP[2]	br_b_vf1_iwp2	AF15	26v
$\overline{BB}$/VF[2]/IWP[3]	bb_b_vf2_iwp3	AE14	26v
IWP[0:1]/VFLS[0:1]	iwp0_vfls0	T3	26v
	iwp1_vfls1	R4	26v
TMS	tms	N1	26v
TDI/DSDI	tdi_dsdi	M1	26v
TCK/DSCK	tck_dsck	L2	26v
TDO/DSDO	tdo_dsdo	R2	26v
JCOMP[2]	jcomp_b	P2	26v
XTAL	xtal	AA26	extal_oscpll
EXTAL	extal	AB26	extal_oscpll
XFC	xfc	AD26	xfc
CLKOUT	clkout	AD21	26vf
EXTCLK	extclk	Y24	extclk
VDDSYN	vddsyn	AE26	vddint
VSSSYN	vsssyn	AC26	vsssyn
ENGCLK/BUCLK	engclk_buclk	AF22	26v5vsr
PULL_SEL[3]	pullsel	W26	5vfa

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
QSMCM_A			
A_PCS[0]/$\overline{SS}$/QGPIO[0]	a_pcs0_ss_b_qgpio0	V23	5vfa
A_PCS[1:3]/QGPIO[1:3]	a_pcs1_qgpio1	W25	5vfa
	a_pcs2_qgpio2	U23	5vfa
	a_pcs3_qgpio3	U26	5vfa
A_MISO/QGPIO[4]	a_miso_qgpio4	T24	5vh
A_MOSI/QGPIO[5]	a_mosi_qgpio5	U25	5vh
A_SCK/QGPIO[6]	a_sck_qgpio6	T26	5vh
A_TXD[1:2]/QGPO[1:2]	a_txd1_qgpo1	T23	5vsa
	a_txd2_qgpo2	V24	5vsa
A_RXD[1:2]/QGPI[1:2]	a_rxd1_qgpi1	U24	5vido
	a_rxd2_qgpi2	V25	5vido
B_PCS[0]/$\overline{SS}$/QGPIO[0]	b_pcs0_ss_b_qgpio0	N25	5vfa
B_PCS[1:2]/QGPIO[1:2]	b_pcs1_qgpio1	N26	5vfa
	b_pcs2_qgpio2	R24	5vfa
B_PCS[3]/J1850_TX	b_pcs3_j1850_tx	P25	5vfa
B_MISO/QGPIO[4]	b_miso_qgpio4	P24	5vh
B_MOSI/QGPIO[5]	b_mosi_qgpio5	P26	5vh
B_SCK/QGPIO[6]	b_sck_qgpio6	R23	5vh
B_TXD[1:2]/QGPO[1:2]	b_txd1_qgpo1	R25	5vsa
	b_txd2_qgpo2	R26	5vsa
B_RXD[1]/QGPI[1]	b_rxd1_qgpi1	V26	5vido
B_RXD[2]/J1850_RX	b_rxd2_j1850_rx	T25	5vsa
B_ECK	b_eck	P23	5vsa
MIOS14/TOUCAN_C			
MDA[11:15], MDA[27:31]	mda11	F25	5vsa
	mda12	G23	5vsa
	mda13	F26	5vsa
	mda14	K24	5vsa
	mda15	K23	5vsa
	mda27	G24	5vsa
	mda28	G25	5vsa
	mda29	G26	5vsa
	mda30	H23	5vsa
	mda31	H24	5vsa

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
MPWM[0:3], [16:19]	mpwm0	H25	5vsa
	mpwm1	H26	5vsa
	mpwm2	J24	5vsa
	mpwm3	J23	5vsa
	mpwm16	J25	5vsa
	mpwm17	E26	5vsa
	mpwm18	F24	5vsa
	mpwm19	L25	5vsa
VF[0:2]/MPIO32B[0:2]	vf0_mpio32b0	L26	26v5vs
	vf1_mpio32b1	M23	26v5vs
	vf2_mpio32b2	M24	26v5vs
VFLS[0:1]/MPIO32B[3:4]	vfls0_mpio32b3	M26	26v5vs
	vfls1_mpio32b4	N24	26v5vs
MPWM[4:5]/MPIO32B[5:6]	mpwm4_mpio32b5	M25	5vsa
	mpwm5_mpio32b6	F23	5vsa
MDO[7:4]/MPIO32B[7:10]	mdo7_mpio32b7	P1	26v5vs
	mdo6_mpio32b8	N3	26v5vs
	mdo5_mpio32b9	N4	26v5vs
	mdo4_mpio32b10	N2	26v5vs
MPWM[20:21]/MPIO32B[11:12]	mpwm20_mpio32b11	J26	5vsa
	mpwm21_mpio32b12	K25	5vsa
C_CNTX0/MPIO32B[13]	c_cntx0_mpio32b13	K26	5vfa
C_CNRX0/MPIO32B[14]	c_cnrx0_mpio32b14	L23	5vsa
MPIO32B[15]	mpio32b15	L24	5vsa
EXTAL32	extal32	D1	26v
XTAL32	xtal32	E1	26v
VDDRTC	vddrtc	C1	vddint
VSSRTC	vssrtc	F1	vsssyn

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
TPU3_A/TPU3_B/TPU3_C			
A_TPUCH[0:15]	a_tpuch0	D20	5vsa
	a_tpuch1	A21	5vsa
	a_tpuch2	A16	5vsa
	a_tpuch3	D17	5vsa
	a_tpuch4	A17	5vsa
	a_tpuch5	B17	5vsa
	a_tpuch6	A18	5vsa
	a_tpuch7	D18	5vsa
	a_tpuch8	B18	5vsa
	a_tpuch9	C18	5vsa
	a_tpuch10	A19	5vsa
	a_tpuch11	B19	5vsa
	a_tpuch12	C19	5vsa
	a_tpuch13	D19	5vsa
	a_tpuch14	A20	5vsa
	a_tpuch15	C20	5vsa
A_T2CLK	a_t2clk	B20	5vsa
B_TPUCH[0:15]	b_tpuch0	D26	5vsa
	b_tpuch1	E24	5vsa
	b_tpuch2	D25	5vsa
	b_tpuch3	B21	5vsa
	b_tpuch4	C21	5vsa
	b_tpuch5	A22	5vsa
	b_tpuch6	B22	5vsa
	b_tpuch7	B23	5vsa
	b_tpuch8	C23	5vsa
	b_tpuch9	D21	5vsa
	b_tpuch10	A23	5vsa
	b_tpuch11	C22	5vsa
	b_tpuch12	A24	5vsa
	b_tpuch13	B24	5vsa
	b_tpuch14	A25	5vsa
	b_tpuch15	C26	5vsa
B_T2CLK	b_t2clk	E25	5vsa

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
C_TPUCH[0:15]	c_tpuch0	K3	5vsa
	c_tpuch1	K2	5vsa
	c_tpuch2	K1	5vsa
	c_tpuch3	J3	5vsa
	c_tpuch4	K4	5vsa
	c_tpuch5	J2	5vsa
	c_tpuch6	J1	5vsa
	c_tpuch7	H2	5vsa
	c_tpuch8	H3	5vsa
	c_tpuch9	H1	5vsa
	c_tpuch10	G1	5vsa
	c_tpuch11	G2	5vsa
	c_tpuch12	G3	5vsa
	c_tpuch13	J4	5vsa
	c_tpuch14	F2	5vsa
	c_tpuch15	F3	5vsa
C_T2CLK	c_t2clk	H4	5vsa
QADC64_A/QADC64_B			
ETRIG[1:2]	etrig1	C16	5vsa
	etrig2	B16	5vsa
AN[44]/ANw/A_PQB[0]	an44_anw_a_pqb0	B3	5vsa
AN[45]/ANx/A_PQB[1]	an45_anx_a_pqb1	C4	5vsa
AN[46]/ANy/A_PQB[2]	an46_any_a_pqb2	C7	5vsa
AN[47]/ANz/A_PQB[3]	an47_anz_a_pqb3	D8	5vsa
AN[48:51]/A_PQB[4:7]	an48_a_pqb4	A7	5vsa
	an49_a_pqb5	B7	5vsa
	an50_a_pqb6	C8	5vsa
	an51_a_pqb7	D9	5vsa
AN[52:54]/A_MA[0:2]/PQA[0:2]	an52_a_ma0_pqa0	B8	5vsa
	an53_a_ma1_pqa1	A8	5vsa
	an54_a_ma2_pqa2	C9	5vsa
AN[55:59]/A_PQA[3:7]	an55_a_pqa3	D10	5vsa
	an56_a_pqa4	B9	5vsa
	an57_a_pqa5	C10	5vsa
	an58_a_pqa6	B10	5vsa
	an59_a_pqa7	D11	5vsa

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
AN[64:71]/B_PQB[0:7]	an64_b_pqb0	A2	5vsa
	an65_b_pqb1	A14	5vsa
	an66_b_pqb2	B14	5vsa
	an67_b_pqb3	A13	5vsa
	an68_b_pqb4	D14	5vsa
	an69_b_pqb5	B13	5vsa
	an70_b_pqb6	C14	5vsa
	an71_b_pqb7	C13	5vsa
AN[72:74]/B_MA[0:2]/PQA[0:2]	an72_b_ma0_pqa0	A12	5vsa
	an73_b_ma1_pqa1	B12	5vsa
	an74_b_ma2_pqa2	D13	5vsa
AN[75:79]/B_PQA[3:7]	an75_b_pqa3	C12	5vsa
	an76_b_pqa4	A11	5vsa
	an77_b_pqa5	B11	5vsa
	an78_b_pqa6	D12	5vsa
	an79_b_pqa7	C11	5vsa
AN[80:87]	an80	A6	5vsa
	an81	B6	5vsa
	an82	D7	5vsa
	an83	C6	5vsa
	an84	A5	5vsa
	an85	B5	5vsa
	an86	D6	5vsa
	an87	C5	5vsa
VRH	vrh	A3	vflashvrh
VRL	vrl	A4	vssint
ALTREF	altref	B4	vflashvrh
VDDA	vdda	A9	vdda
VSSA	vssa	A10	vssint
TOUCAN_A/TOUCAN_B			
A_CNTX0	a_cntx0	Y25	5vfa
B_CNTX0	b_cntx0	E2	5vfa
A_CNRX0	a_cnrx0	AA24	5vsa
B_CNRX0	b_cnrx0	C17	5vsa
UC3F			
EPEE	epee	AF21	26v
B0EPEE	b0epee	AD20	26v
VFLASH	vflash	W24	vflashvrh
VDDF	vddf	Y23	vddint
VSSF	vssf	AA25	vssint

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
READI			
$\overline{\text{MSEO}}$	mseo_b	T2	26v
MDO[3]	mdo_3	T1	26v
MDO[2]	mdo_2	R3	26v
MDO[1]	mdo_1	R1	26v
MDO[0]	mdo_0	P4	26v
MCKO	mcko	P3	26v
$\overline{\text{RSTI}}$	rsti_b	M3	26v
$\overline{\text{EVTI}}$	evti_b	M2	26v
$\overline{\text{MSEI}}$	msei_b	M4	26v
MDI[1]	mdi_1	L3	26v
MDI[0]	mdi_0	L1	26v
MCKI	mcki	L4	26v
Global Power Supplies			
NVDDL	nvddl	F4, U4, AC9, AC13, D22, W23, AC15, AC17	nvddl
QVDDL	qvddl	AB4, AC3, AD2, AE1, A15, B15, C15, D15, AC23, AE25, AF26, AD24	qvddl
VDDH	vddh	AC6, D16, N23, AC20, D5	vddh
KAPWR	kapwr	Y26	kapwr
VDDSRAM1	vddsram1	E3	vddint
VDDSRAM2	vddsram2	D2	vddint
VDDSRAM3	vddsram3	G4	vddint

Table 2-10 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Ball	Pad Type
VDD	vdd	D24, E23, AC21, AD22, AE23, AF24, A1, B2, B26, C25, C3, D4, AC5, AD4, AE3, AF2	vddint

Table 2-10 Pin Names and Abbreviations (Continued)

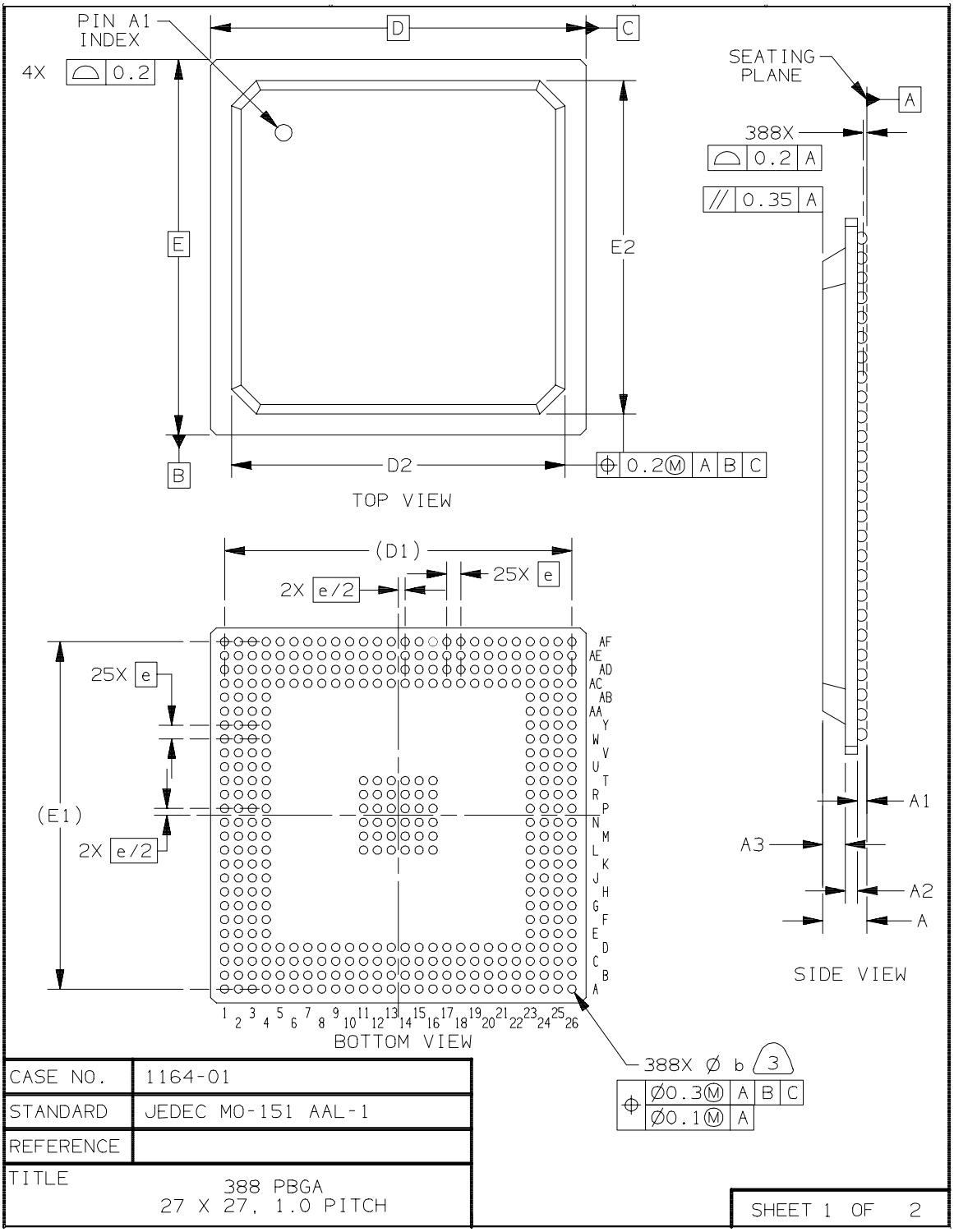
Pin List	Pin Name	Ball	Pad Type
VSS	vss	A26, B25, AC22, D23, B1, N14, N15, N16, D3, M14, M15, M16, C2, E4, L14, L15, L16, P14, P15, P16, AD23, AE24, AF25, L11, L12, L13, M11, M12, M13, N11, N12, N13, P11, P12, P13, R11, R12, R13, T11, T12, T13, AC4, AD3, AE2, AF1, R14, R15, R16, T14, T15, T16, C24	vss
NC	no_connect	AE22, AF23, AC2, AD5	

NOTES:
1. This pin was $\overline{\text{PORESET}}$ only on mask set K85H.
2. This pin was $\overline{\text{TRST}}$ in mask set K85H.
3. This pin was A_ECK in mask set K85H.

2.8 Package Description

2.8.1 Package Diagrams

The package for the MPC565 / MPC566 is the 352/388 PBGA (27 x 27 mm, 1.0 mm ball pitch). This package has 352 balls in the four perimeter rows and 36 ground balls in the center island for a total of 388 balls. The ball footprint is shown in **Figure 2-5**.



NOTE: Top Down View

Figure 2-5 MPC565 / MPC566 Package Footprint (1 of 2)

NOTES

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS IN MILLIMETERS.

3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM A.

4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.95	2.55							
A1	0.40	0.60							
A2	0.50	0.70							
A3	1.05	1.25							
b	0.50	0.70							
D	27.00 BSC								
D1	25.00 REF								
D2	23.30	24.70							
E	27.00 BSC								
E1	25.00 REF								
E2	23.30	24.70							
e	1.00 BSC								

CASE NO.	1164-01
STANDARD	JEDEC MO-151 AAL-1
REFERENCE	
TITLE	388 PBGA 27 X 27, 1.0 PITCH

SHEET 2 OF 2

Figure 2-5 MPC565 / MPC566 Package Footprint (2 of 2)

2.8.2 Bumped Die

The MPC565 / MPC566 is available as known good die (KGD) in a bumped die configuration. The bump pitch is seven mils. The bump configuration is shown in **Figure 2-6** through **Figure 2-9**. **Figure 2-7**, along with **Figure 2-8**, shows the categories of function pins. **Figure 2-9** shows the pins in a larger diagram in black and white.

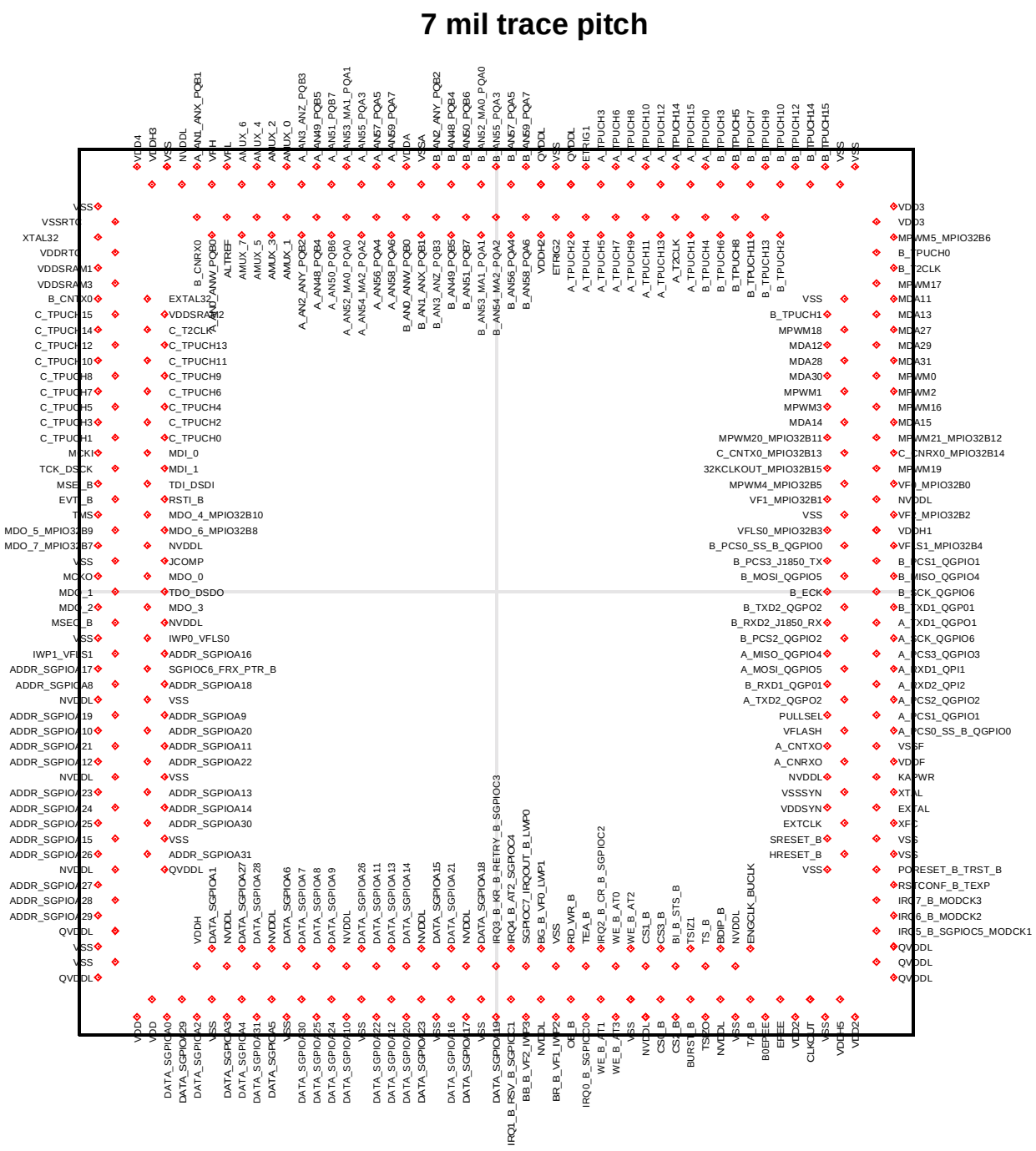


Figure 2-6 MPC565 / MPC566 Redistributed Bump Map

2.8.3 MPC565 / MPC566 Ball Diagram

The ball diagram of the MPC565 / MPC566 is shown in **Figure 2-7**.

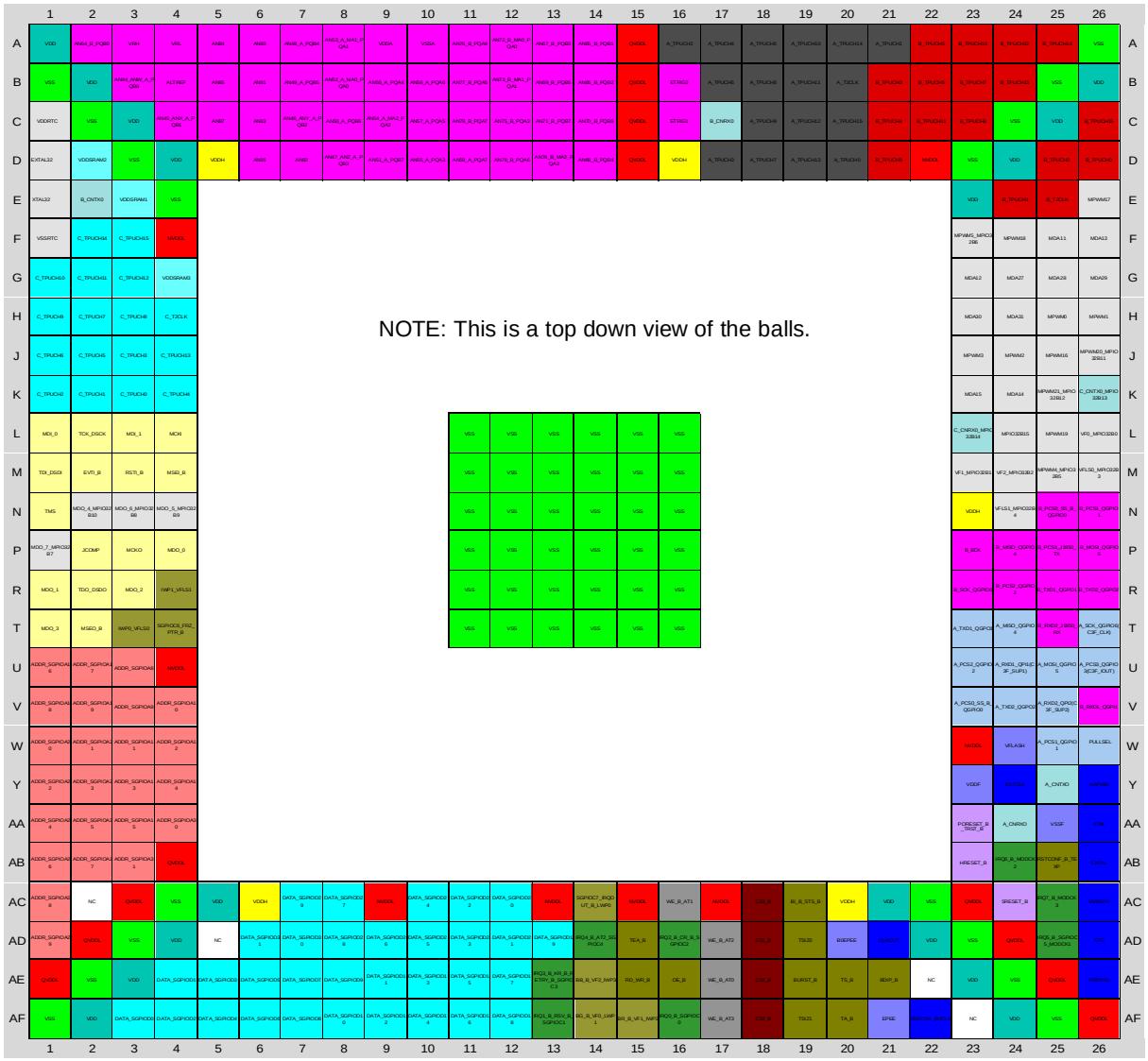


Figure 2-7 MPC565 / MPC566 Ball Diagram

GROUP NAME	COLOR CODE
ADDRESS BUS	
BUS CONTROL	
CHIP SELECT	
CLOCK/PLL	
DATA BUS	
DEBUG	
FLASH	
INTERRUPTS	
JTAG	
MIOS	
NC	
NVDDL	
NVSS	
QADC A	
QADC B	
QSM A	
QSM B	
QVDDL	
READI	
READI	
RESET	
SRAM	
TOUCAN A	
TOUCAN B	
TPU3 A	
TPU3 B	
TPU3 C	
VDD	
VDDH	
VSS	
WRITE ENABLE	

Figure 2-8 MPC565 / MPC566 Ball Diagram Legend

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VDD	AN64_B_PQB0	VRH	VRL	AN84	AN80	AN48_A_PQB4	AN53_A_MA1_PQA1	VDDA	VSSA	AN76_B_PQA4	AN72_B_MA0_PQA0	AN67_B_PQB3
B	VSS	VDD	AN44_ANW_A_PQB0	ALTREF	AN85	AN81	AN49_A_PQB5	AN52_A_MA0_PQA0	AN56_A_PQA4	AN58_A_PQA6	AN77_B_PQA5	AN73_B_MA1_PQA1	AN69_B_PQB5
C	VDDRTC	VSS	VDD	AN45_ANX_A_PQB1	AN87	AN83	AN46_ANY_A_PQB2	AN50_A_PQB6	AN54_A_MA2_PQA2	AN57_A_PQA5	AN79_B_PQA7	AN75_B_PQA3	AN71_B_PQB7
D	EXTAL32	VDDSRAM2	VSS	VDD	VDDH	AN86	AN82	AN47_ANZ_A_PQB3	AN51_A_PQB7	AN55_A_PQA3	AN59_A_PQA7	AN78_B_PQA6	AN74_B_MA2_PQA2
E	XTAL32	B_CNTX0	VDDSRAM1	VSS									
F	VSSRTC	C_TPUCH14	C_TPUCH15	NVDDL									
G	C_TPUCH10	C_TPUCH11	C_TPUCH12	VDDSRAM3									
H	C_TPUCH9	C_TPUCH7	C_TPUCH8	C_T2CLK									
J	C_TPUCH6	C_TPUCH5	C_TPUCH3	C_TPUCH13									
K	C_TPUCH2	C_TPUCH1	C_TPUCH0	C_TPUCH4									
L	MDI_0	TCK_DSCK	MDI_1	MCKI							VSS	VSS	VSS
M	TDI_DSDI	EVTI_B	RSTI_B	MSEI_B							VSS	VSS	VSS
N	TMS	MDO_4_MPIO32B10	MDO_6_MPIO32B8	MDO_5_MPIO32B9							VSS	VSS	VSS

NOTE: This pinout is a top down view of the package.

Figure 2-9 MPC565 / MPC566 Ball Map (Black and White, page 1)

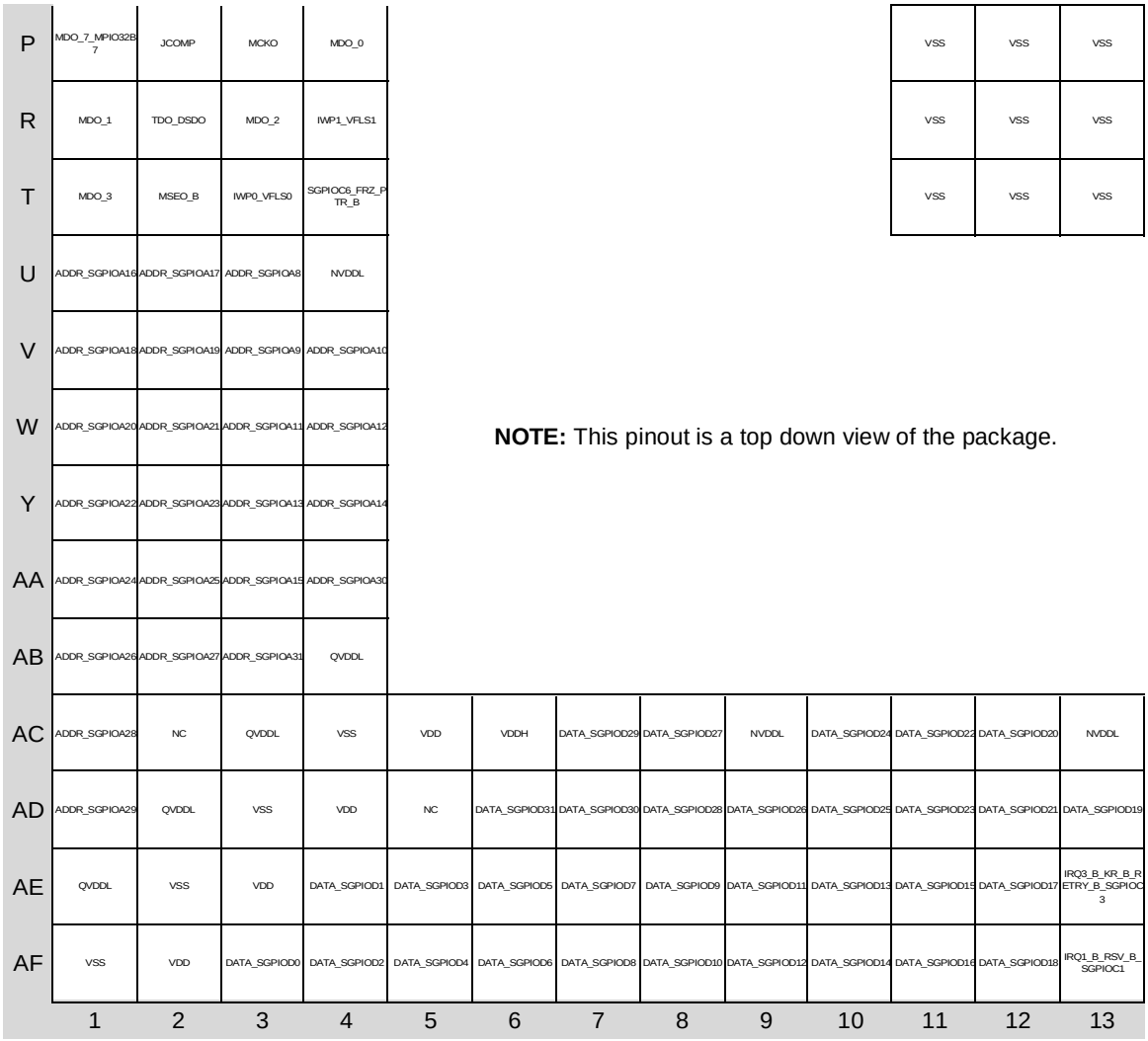
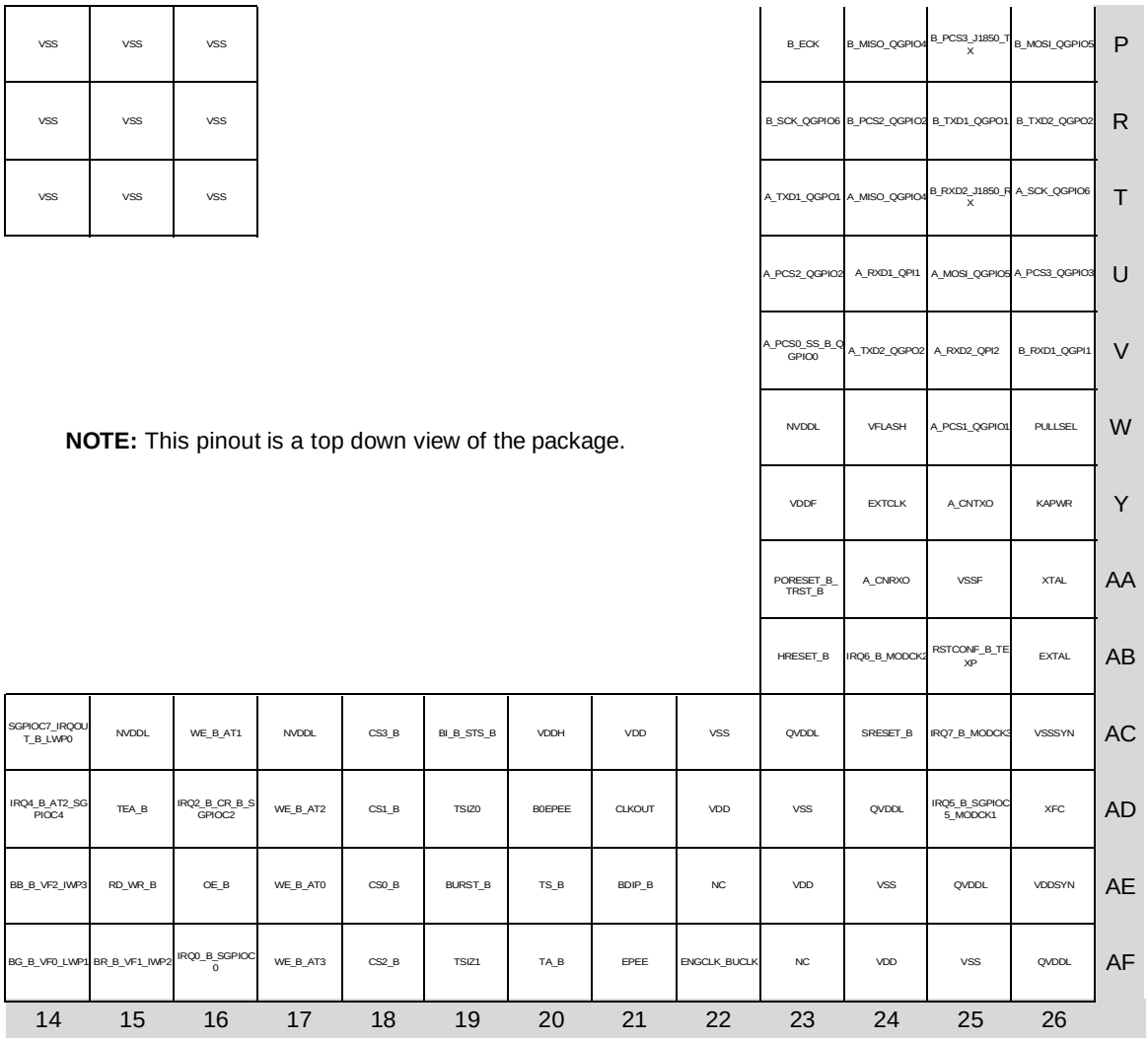


Figure 2-9 MPC565 / MPC566 Ball Map (Black and White, page 2)

14	15	16	17	18	19	20	21	22	23	24	25	26	
AN65_B_PQB1	QVDDL	A_TPUCH2	A_TPUCH4	A_TPUCH6	A_TPUCH10	A_TPUCH14	A_TPUCH1	B_TPUCH5	B_TPUCH10	B_TPUCH12	B_TPUCH14	VSS	A
AN66_B_PQB2	QVDDL	ETRIG2	A_TPUCH5	A_TPUCH8	A_TPUCH11	A_T2CLK	B_TPUCH3	B_TPUCH6	B_TPUCH7	B_TPUCH13	VSS	VDD	B
AN70_B_PQB6	QVDDL	ETRIG1	B_CNRX0	A_TPUCH9	A_TPUCH12	A_TPUCH15	B_TPUCH4	B_TPUCH11	B_TPUCH8	VSS	VDD	B_TPUCH15	C
AN68_B_PQB4	QVDDL	VDDH	A_TPUCH3	A_TPUCH7	A_TPUCH13	A_TPUCH0	B_TPUCH9	NVDDL	VSS	VDD	B_TPUCH2	B_TPUCH0	D
									VDD	B_TPUCH1	B_T2CLK	MPWM17	E
									MPWM5_MPIO32B6	MPWM18	MDA11	MDA13	F
									MDA12	MDA27	MDA28	MDA29	G
									MDA30	MDA31	MPWM0	MPWM1	H
									MPWM3	MPWM2	MPWM16	MPWM20_MPIO32B11	J
									MDA15	MDA14	MPWM21_MPIO32B12	C_CNTX0_MPIO32B13	K
VSS	VSS	VSS							C_CNRX0_MPIO32B14	MPIO32B15	MPWM19	VF0_MPIO32B0	L
VSS	VSS	VSS							VF1_MPIO32B1	VF2_MPIO32B2	MPWM4_MPIO32B5	VFLS0_MPIO32B3	M
VSS	VSS	VSS							VDDH	VFLS1_MPIO32B4	B_PCS0_SS_B_QGPIO0	B_PCS1_QGPIO1	N

NOTE: This pinout is a top down view of the package.

Figure 2-9 MPC565 / MPC566 Ball Map (Black and White, page 3)



NOTE: This pinout is a top down view of the package.

Figure 2-9 MPC565 / MPC566 Ball Map (Black and White, page 4)