SECTION 1
OVERVIEW DESCRIPTION

1.1 Introduction

The MC68F375 is a member of the MC68300/68HC16 family of modular microcontrollers. This family includes a series of modules from which numerous microcontrollers (MCU's) are derived. These modules are connected on-chip via the intermodule bus (IMB). This section includes a list of pins that are available to each module on the chip, see **Table 1-1**.

1.2 MC68F375 Feature List

The major features of the MC68F375 are listed below. A block diagram of the device is shown in **Figure 1-1**.

- Modular architecture.
- 32-bit 68000 family CPU with upward object code compatibility (CPU32):
  - — Virtual memory implementation.
  - — Loop mode for instruction execution.
  - — Improved exception handling for controller applications.
  - — Table lookup and interpolate instruction.
- Single chip integration module (SCIM2E):
  - — External bus support.
  - — Parallel ports option on address and data bus in single chip modes and partially expanded modes.
  - — Nine programmable chip select outputs.
  - — Two special emulation-specific chip select outputs.
  - — System protection logic.
  - — System clock based on slow (~32 KHz) or Fast (~4 MHz) crystal reference or external clock operation (2X).
  - — Periodic interrupt timer, watchdog timer, clock monitor and bus monitor.
- 10-bit queued analog-to-digital converter with AMUX (QADC64):
  - — Up to 16 channels on the QADC64 (25 total including the 16 AMUX Channels).
  - — 4 automatic channel selection and conversion modes.
  - — 2 channel scan queues of variable length.
  - — 64 result registers and 3 result alignment formats.
  - — Programmable input sample time.
  - — Analog multiplexer capable of multiplexing 16 analog channels.
- Queued serial multi-channel communication module with three serial I/O subsystems (QSMCM):
  - — 2 enhanced SCI (UART): modulus baud rate generator, parity. One SCI has 16 level Rx and Tx queues.
  - — Queued SPI: 160-byte RAM, up to 32 automatic transfers, continuous cycling, 8-to-16 bits per transfer, LSB/MSB first.

— Dual function I/O port pins.

- Time processing unit (TPU3):
  - — 16 channels – each is associated with a pin.
  - — Each channel can perform any time function.
  - — Each time function may be assigned to more than one channel.
  - — Each channel has an event register comprised of: 16-bit capture register, 16-bit compare/match register, 16-bit greater-than-or-equal-to comparator.
  - — Each channel can be programmed to perform match or capture operations with one or both of the two 16-bit free running timer count registers (TCR1 and TCR2).
  - — TCR1 is clocked from the internal TPU3 system clock.
  - — TCR2 may be clocked or gated from the external T2CLK pin.
  - — All time primitives are microcoded.
  - — 4 Kbytes of microstore program ROM space.
  - — All channels have eight 16-bit parameter registers.
  - — A hardware scheduler with three priority levels is included.
  - — Resolution is one system clock period.
  - — Modulus prescaler (DIV 2, 4, 6..... 62, 64)
- 6-Kbyte TPU emulation RAM (DPTRAM).
  - — Can be used as system RAM or TPU microcode storage.
- 256K Byte 1T Flash EEPROM (CMFI).
  - — 5 V program/erase.
  - — Block 0 protected by an external pin.
- SRAM
  - — External V_{STBY} pin for separate standby supply.
  - — 8-Kbyte static RAM (SRAM):
  - — 4 x 512-byte static RAM (SRAM):
  - — 512-byte modules can overlay any 512-byte portion (on 512-byte boundaries) of the CMFI module.
- Late programmable read only memory – ROM:
  - — 8-Kbyte array, accessible as bytes or words.
  - — User selectable default base address.
  - — User selectable bootstrap ROM function.
- CAN2.0B controller module (TouCAN™):
  - — Full implementation of CAN protocol specification – Version 2.0B.
  - — Standard/extended data and remote frames (up to 109/127 bits long).
  - — Programmable bit rate up to 1 Mbit/sec, derived from system clock.
  - — 16 Rx/Tx message buffers of 0-8 bytes data length, of which 2 buffers are configurable to work as Rx buffers with specific programmable masks.
  - — Programmable global Rx masks.
  - — Programmable transmit-first scheme: lowest ID or lowest buffer number.
  - — Low power “SLEEP” mode, with programmable “WAKE UP” on bus activity.
  - — Automatic time-stamping of received and transmitted messages.
- Configurable timer module 9 (CTM9):
  - — 1 bus interface unit submodule (BIUSM).
  - — 1 counter prescaler submodule (CPSM).
  - — 1 free-running counter submodule (FCSM).

— 2 modulus counter submodules (MCSM).
— 4 single action submodules (SASM).
— 4 double action submodules (DASM).
— 4 dedicated PWM submodules (PWMSM)

- Package: flip chip and 217-ball 23 x 23 mm PBGA.
- Operating temperature: -40° C through 125° C
- Operating frequency: 33.00 MHz system clock at V_{DDL} = 3.3 V / V_{DDH} = 5.0 V.

1.3 Module Descriptions

A short description of each module of the MC68F375 appears in the following sections. For more details on each module, please refer to the specific module section as indicated.

1.3.1 Central Processing Unit Module – CPU32

The CPU32 is upward-compatible with the M68000 family which excels at processing calculation-intensive algorithms and supporting high level languages. All of the MC68010 and most of the MC68020 enhancements such as virtual memory support, loop mode execution, and 32-bit mathematical operations are supported. New instructions such as table lookup and interpolate and low-power stop support the specific requirements of controller applications. Refer to **SECTION 3 CENTRAL PROCESSOR UNIT**.

1.3.2 Single Chip Integration Module – SCIM2E

The MC68F375 contains the single chip integration module 2 (SCIM2E). The SCIM2E consists of several submodules: the external bus interface, the system protection submodule, the test submodule, the clock synthesizer, and the chip select submodule. Refer to **SECTION 4 SINGLE-CHIP INTEGRATION MODULE 2 (SCIM2E)**.

The MC68F375 SCIM2E includes improvements to the regular SCIM. This enhanced SCIM includes improvements to the clock synthesizer. These changes are defined in detail in **4.3.2 Clock Synthesizer Submodule**. Please refer to the *SCIM Reference Manual* (SCIMRM/AD) for more details on the characteristics of this module.

1.3.3 Queued Analog to Digital Converter Module – QADC64

The queued analog-to-digital converter 64 (QADC64) provides the microcontroller unit (MCU) with two conversion sequence control mechanisms (queues); a 16 channel expandable multiplexer; a 10-bit A/D converter; and digital port logic. Refer to **SECTION 5 QUEUED ANALOG-TO-DIGITAL CONVERTER MODULE-64**.

- The queue RAM stores the sequence of channels to convert, conversion parameters, and stores conversion results.
- The queue control logic provides the trigger/run modes, interrupt control, queue status, etc.
- The 10-bit A/D converter selects and convert the desired channel, using a successive approximation technique. The absolute accuracy (total unadjusted error) compared to an ideal transfer curve is +/-2 counts.

- The port logic provides up to 8 input-only and 8 bidirectional digital interface pins. Pins which are used as analog channels should be masked out of the digital data.

1.3.4 Analog Multiplexer – AMUX

The analog multiplexer (AMUX) submodule expands the channel capacity of the QADC64 analog-to-digital converter inputs by a maximum of 32 analog channels. 16 analog channels are bonded out on the MC68F375. The AMUX does not have an intermodule bus (IMB3) interface; control is through the QADC64. Refer to **5.13 Analog Multiplexer Submodule**.

1.3.5 Queued Serial Multi-Channel Communications Module – QSMCM

The queued serial multi-channel module (QSMCM) provides the microcontroller unit (MCU) with three serial communication interfaces divided into three submodules: the queued serial peripheral interface (QSPI) and two serial communications interfaces (SCI). These submodules communicate with the CPU via a common slave bus interface unit (SBIU). Refer to **SECTION 5 QUEUED ANALOG-TO-DIGITAL CONVERTER MODULE-64**.

The QSPI is a full-duplex, synchronous serial interface for communicating with peripherals and other MCUs. It is enhanced from the original QSM to include a total of 160 bytes of queue RAM to accommodate more receive, transmit, and control information.

The duplicate, independent, SCIs are full-duplex universal asynchronous receiver transmitter (UART) serial interface. The original QSM SCI is enhanced by the addition of an SCI, a common external baud clock source, receive and transmit buffers on one SCI.

1.3.6 TouCAN Module

The TouCAN module is a communication controller implementing the CAN protocol. It contains all the logic needed to implement the CAN2.0B protocol, supporting both standard ID format and extended ID. The protocol is a CSMA/CD type, with collision detection without loss, used mainly for vehicle systems communication and industrial applications. The module contains 16 message buffers used for transmit and receive, and masks used to qualify the received message ID before comparing it to the receive buffers. Refer to **SECTION 7 CAN 2.0B CONTROLLER MODULE**.

1.3.7 Enhanced Time Processing Unit – TPU3

The TPU3 is an intelligent, semi-autonomous co-processor designed for timing control. Operating simultaneously with the CPU, the TPU processes microinstructions, schedules and processes real-time hardware events, performs input and output, and accesses shared data without CPU intervention. Consequently, for each timer event the CPU setup and service time are minimized or eliminated.

The TPU3 can be viewed as a special-purpose microcomputer that performs a programmable series of two operations, match and capture. Each occurrence of either operation is called an event. A programmed series of events is called a function. TPU3

functions replace software functions that would require host CPU interrupt service. Refer to **SECTION 8 TIME PROCESSOR UNIT 3**.

1.3.8 DPTRAM TPU Emulation RAM Module – DPTRAM

The RAM module with TPU microcode storage support (DPTRAM) consists of a control register block and a 6-Kbyte array of static RAM which can be used as a microcode storage for TPU3 or general purpose memory. Microcode initialization is done by the host CPU through standard IMB modes of access. Refer to **SECTION 9 DUAL-PORT TPU RAM (DPTRAM)**.

The DPTRAM interface includes an IMB3 bus Interface and two[1] TPU3 interfaces. When the RAM is being used in microcode mode, the array may only be accessed by the TPU3 via a separate local bus, and not via the intermodule bus.

1.3.9 1T Flash Electrically Erasable Read Only Memory – CMFI

The MC68F375 contains an electrically erasable, programmable 256-Kbyte FLASH memory (CMFI). The primary function of the CMFI module is to serve as electrically programmable and erasable non-volatile memory (NVM) to store program instructions and/or data. It is a non-volatile solid state silicon memory device consisting of an array of isolated elements, a means for selectively adding and removing charge to the elements electrically and a means of selectively sensing the stored charge in the elements. When power is removed from the device, the stored charge of the isolated elements will be retained. Refer to **SECTION 10 CDR MoneT FLASH FOR THE IMB3 (CMFI)**.

1.3.10 Static RAM – SRAM

There are two types of SRAM in the MC68F375:

- 8K Static RAM – SRAM. This module is a fast access (2 clocks) general purpose static RAM (SRAM) for the MCU and is accessed via the IMB.
- 2K (4 x 512 Byte) Patch Static RAM – SRAM. These modules are fast access (2 clocks) general purpose static RAMs (SRAM) for the MCU with a patch option which provides a method to overlay the internal CMFI memory for emulation.

Refer to **SECTION 11 STATIC RANDOM ACCESS MEMORY (SRAM)**.

1.3.11 Mask Programmable Read Only Memory – ROM

The Mask ROM module is designed to be used with the inter-module bus (IMB3) and consequently any CPU capable of operating on the IMB. A size of 8192 (8K) bytes was selected to reside on the MC68F375 MCU. The ROM is a “late programmable” type which means that programming of the array and control register options occurs later in the processing flow, allowing reduction in cycle time between software code changes from the user to available devices.

During master reset the ROM will monitor one DATA line (DATA14) to determine if it should respond as a memory mapped ROM, or be disabled. If the state of DATA14 is

[1] Note: the MC68F375 contains only a single TPU3. The second TPU3 interface is inactive.

1, the STOP bit in the ROMMCR register will be cleared to 0 and the array will respond normally to the bootstrap address range and the ROM array base address. If DATA14 is 0, the STOP bit will be set and the bootstrap address range and the ROM array will be disabled until the STOP bit is cleared either by an IMB write or until the next master reset which occurs with DATA14 = 1. When STOP is set, the array will not respond to the bootstrap address range or the ROM Array base address in ROMBAH and ROMBAL, allowing an external device to respond to the ROM Array's address space, and/or provide bootstrap information. This allows the ROM to be disabled from outside of the device if necessary. Refer to **SECTION 12 MASK ROM MODULE**.

1.3.12 Configurable Timer Module 9 – CTM9

The configurable timer module (CTM) is a family of timer modules for the Motorola Modular Microcontroller Family (MMF). The timer architecture is modular—before the chip is manufactured the user can specify the number of time-bases (counter submodules) and channels (action submodules, or timer I/O pins) that are included. Refer to **SECTION 13 CONFIGURABLE TIMER MODULE (CTM9)**. The major blocks in the CTM9 are:

- Bus interface unit submodule (BIUSM)
- Single action submodule (SASM)
- Double action submodule (DASM)
- Pulse width modulation submodule (PWMSM)
- Counter prescaler submodule (CPSM)
- Free-running counter submodule (FCSM)
- Modulus counter submodule (MCSM)

1.4 Referenced Documents

- ***CPU32 Central Processor Unit Reference Manual* (CPU32RM/AD).**
- ***SCIM Reference Manual* (SCIMRM/AD)**.
- ***QSM Reference Manual* (QSMRM/AD or QSM section of MC68332UM/AD)**.
- ***CTM Reference Manual* (CTMRM/D)**.
- ***TPU Reference Manual* (TPURM/AD)**.

1.5 MC68F375 Functional Block Diagram

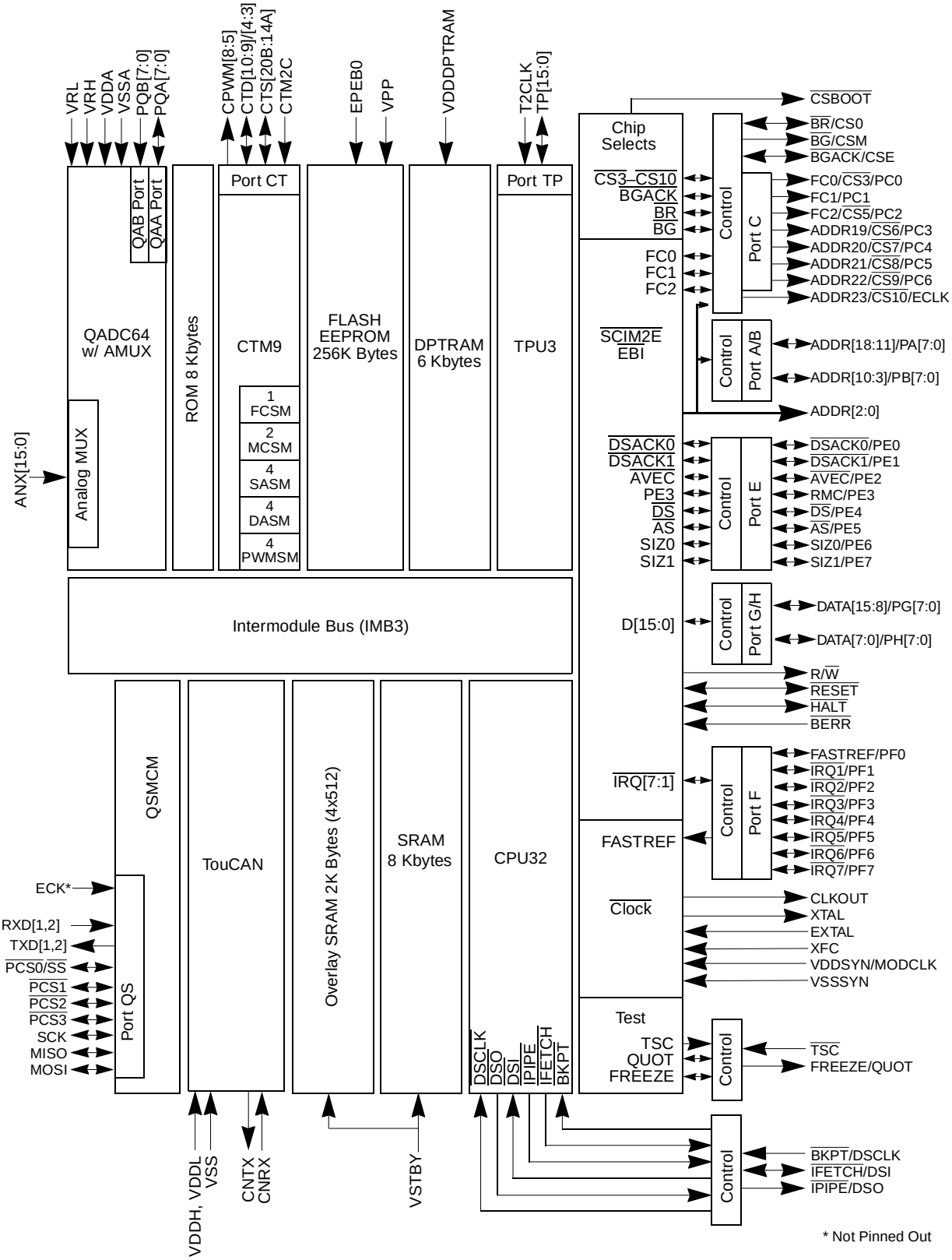


Figure 1-1 MC68F375 Block Diagram

1.6 MC68F375 Pin Usage

Table 1-1 shows the MC68F375 pin usage. For more information on an individual pin, refer to the corresponding module documentation.

Table 1-1 MC68F375 Pin Usage

Functions	Total Pins	Port Pins
CPU32		
BDM	3	
Total	**3**	
SCIM2E		
Port A, Port B	16	16
Port G, Port H	16	16
Port F	8	8
Port C	7	7
Port E	8	8
Bus Control, A[2:0], CSBOOT, TSC, RESET	13	
CLKOUT, PLL	4	
Total	**72**	**55**
QADC64/AMUX		
Channels	16	16
Analog Mux	**16**	
Total	**32**	**16**
QSMCM		
SCI1, SCI2	4	4
SPI	7	7
ECK		
Total	**11**	**11**
TPU3		
Channels	16	16
Clock	1	
Total	**17**	**16**
TouCAN		
Receive	1	
Transmit	1	
Total	**2**	
CTM9		
PWMSM	4	4
SASM	8	8
DASM	4	4
Clock	1	
Total	**17**	**16**
CMFI		
EPEB0	1	
Total	1	

Table 1-1 MC68F375 Pin Usage (Continued)

Functions	Total Pins	Port Pins
Power (V_{DDH}, V_{DDL}, V_{SS})		
I/O Pad Power (V_{DDH})	14	
Logic Power (V_{DDL})	3	
Ground (V_{SS})	16	
SRAM (V_{STBY})	1	
DPTRAM ($V_{DDDPTRAM}$)	1	
CMFI (V_{PP})	1	
SCIM2E Clock (V_{DDSYN}/V_{SSSYN})	2	
QADC64 Power (V_{DDA}/V_{SSA})	2	
QADC64 Reference (V_{RH}/V_{RL})	2	
Total	**42**	
Total	**199**	**114**

1.7 Address Map

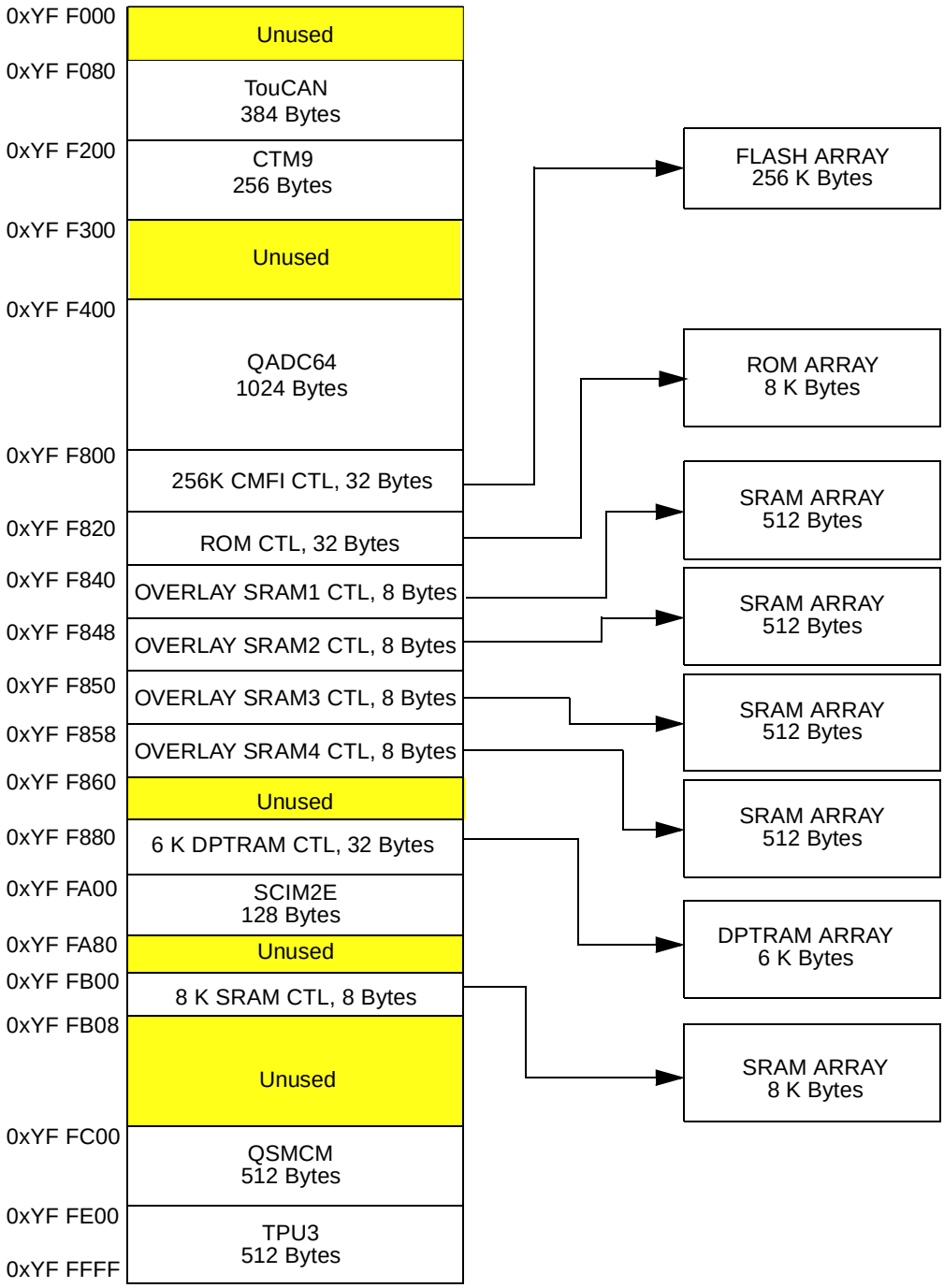
Each MC68300/MC68HC16 derivative MCU has a 4-Kbyte block in the memory map that is assigned to internal module registers. The MSB of the block address is user-programmable via the MM (MODMAP) bit in the SCIMMCR register, see **1.7.1 Address Bus Decoding**. Within this 4-Kbyte block are sub-blocks that are assigned to the individual modules, as shown in the MC68F375 address map in **Figure 1-2**. These sub-blocks vary in size, depending on the register requirements for each module. Positioning of registers within the module sub-blocks is dependent on the individual modules and is specified in the respective module specifications. The RAM, ROM, and CMFI array spaces are not shown with an assigned address because the arrays are not enabled after reset. The arrays are enabled and the base address is set by writing to the control blocks of each array.

Each module that is assigned a sub-block is responsible for responding to any accesses within its assigned address range. Modules do not respond to any register address within the module address space which is not implemented and not reserved. These addresses are mapped outside the MC68F375. An access to a register at an address which is reserved returns zeros, as do accesses to reserved bits within registers.

If the SUPV bit in the module configuration register (MCR) within a module is set, any user mode accesses to the module are mapped externally.

1.7.1 Address Bus Decoding

The internal MODMAP line is compared to internal address line A[23] while A[22:0] are decoded by each module. If a module control block address is decoded, the access will be internal. The value of A[22] down to the module block size is defined in **Figure 1-2** for each module. These bits are fixed for this particular derivative device and are specified by Motorola. The value of MODMAP is specified by the MM control bit in the SCIM2E module configuration register (SCIMMCR), see **4.2.2 Module Mapping**.



Y = M111, where M is the logic state of the module mapping (MM) bit in the SCIM2E configuration register (SCIMMCR).

Figure 1-2 MC68F375 Address Map