APPENDIX A
INTERNAL MEMORY MAP

The tables below use the following notations.

In the Access column:

S = Supervisor Access Only
U = User Access
T = Test Access

In the Reset column:

A = Affected by $\overline{\text{RESET}}$
U = Unchanged
X = Unknown

The codes in the Reset column indicate which reset has an effect on register values.

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Table A-1 TouCAN (CAN 2.0B Controller)

Address	Access	Symbol	Register	Size	Reset
0xYF F000 – 0xYF F07F	—	—	Reserved	—	—
0xYF F080	S	TCNMCR	TouCAN Module Configuration Register. See **Table 7-11** for bit descriptions.	16	X
0xYF F082	T	TTR	TouCAN Test Register	16	X
0xYF F084	S	CANICR	TouCAN Interrupt Configuration Register. See **Table 7-12** for bit descriptions.	16	X
0xYF F086	S	CANCTRL0/ CANCTRL1	TouCAN Control Register 0/ TouCAN Control Register 1. See **Table 7-13** and **Table 7-16** for bit descriptions.	16	X
0xYF F088	S	PRESDIV/ CANCTRL2	TouCAN Control and Prescaler Divider Register/ TouCAN Control Register 2. See **Table 7-17** and **Table 7-18** for bit descriptions.	16	X
0xYF F08A	S	TIMER	TouCAN Free-Running Timer Register. See **Table 7-19** for bit descriptions.	16	X
0xYF F090	S	RXGMASKHI	TouCAN Receive Global Mask High. See **Table 7-20** for bit descriptions.	16	X
0xYF F092	S	RXGMASKLO	TouCAN Receive Global Mask Low. See **Table 7-20** for bit descriptions.	16	X
0xYF F094	S	RX14MASKHI	TouCAN Receive Buffer 14 Mask High. See **7.8.9 Receive Buffer 14 Mask Registers** for bit descriptions.	16	X
0xYF F096	S	RX14MASKLO	TouCAN Receive Buffer 14 Mask Low. See **7.8.9 Receive Buffer 14 Mask Registers** for bit descriptions.	16	X
0xYF F098	S	RX15MASKHI	TouCAN Receive Buffer 15 Mask High. See **7.8.10 Receive Buffer 15 Mask Registers** for bit descriptions.	16	X
0xYF F09A	S	RX15MASKLO	TouCAN Receive Buffer 15 Mask Low. See **7.8.10 Receive Buffer 15 Mask Registers** for bit descriptions.	16	X
0xYF F0A0	S	ESTAT	TouCAN Error and Status Register. See **Table 7-21** for bit descriptions.	16	X
0xYF F0A2	S	IMASK	TouCAN Interrupt Masks. See **Table 7-24** for bit descriptions.	16	X
0xYF F0A4	S	IFLAG	TouCAN Interrupt Flags. See **Table 7-25** for bit descriptions.	16	X
0xYF F0A6	S	RXECTR/ TXECTR	TouCAN Receive Error Counter/ TouCAN Transmit Error Counter. See **Table 7-26** for bit descriptions.	16	X
0xYF F100 — 0xYF F10F	S/U	MBUFF0	TouCAN Message Buffer 0. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F110 — 0xYF F11F	S/U	MBUFF1	TouCAN Message Buffer 1. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F120 — 0xYF F12F	S/U	MBUFF2	TouCAN Message Buffer 2. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U

Table A-1 TouCAN (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F130 — 0xYF F13F	S/U	MBUFF3	TouCAN Message Buffer 3. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F140 — 0xYF F14F	S/U	MBUFF4	TouCAN Message Buffer 4. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F150 — 0xYF F15F	S/U	MBUFF5	TouCAN Message Buffer 5. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F160 — 0xYF F16F	S/U	MBUFF6	TouCAN Message Buffer 6. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F170 — 0xYF F17F	S/U	MBUFF7	TouCAN Message Buffer 7. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F180 — 0xYF F18F	S/U	MBUFF8	TouCAN Message Buffer 8. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F190 — 0xYF F19F	S/U	MBUFF9	TouCAN Message Buffer 9. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F1A0 — 0xYF F1AF	S/U	MBUFF10	TouCAN Message Buffer 10. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F1B0 — 0xYF F1BF	S/U	MBUFF11	TouCAN Message Buffer 11. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F1C0 — 0xYF F1CF	S/U	MBUFF12	TouCAN Message Buffer 12. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F1D0 — 0xYF F1DF	S/U	MBUFF13	TouCAN Message Buffer 13. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F1E0 — 0xYF F1EF	S/U	MBUFF14	TouCAN Message Buffer 14. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U
0xYF F1F0 — 0xYF F1FF	S/U	MBUFF15	TouCAN Message Buffer 15. See **Figure 7-3** and **Figure 7-4** for message buffer definitions.	—	U

Table A-2 CTM9 (Configurable Timer Module)

Address	Access	Symbol	Register	Size	Reset
BIUSM (CTM9 Bus Interface Unit Submodule)					
0xYF F200	S	**BIUMCR**	**BIUSM Module Configuration** Register. See **Table 13-19** for bit descriptions.	16	X
0xYF F202	T	**BIUTEST**	**BIUSM Test** Register.	16	X
0xYF F204	S	**BIUTBR**	**BIUSM Time Base** Register. See **13.8.4.2 BIUTBR — BIUSM Time Base Register** for bit descriptions.	16	X
CPSM (CTM9 Counter Prescaler Submodule)					
0xYF F208	S	CPCR	CPSM Control Register. See **Table 13-21** for bit descriptions.	16	X
0xYF F20A	T	CPTR	CPSM Test Register.	16	X
MCSM2 (CTM9 Modulus Counter Submodule 2)					
0xYF F210	S	MCSM2SIC	MCSM2 Status/Interrupt/Control Register. See **Table 13-5** for bit descriptions.	16	X
0xYF F212	S	MCSM2CNT	MCSM2 Counter Register. See **13.3.10 MCSMCNT — MCSM Counter Register** for bit descriptions.	16	X
0xYF F214	S	MCSM2ML	MCSM2 Modulus Latch Register. See **13.3.11 MCSMML — MCSM Modulus Latch Register** for bit descriptions.	16	X
DASM3 (CTM9 Double-Action Submodule 3)					
0xYF F218	S	DASM3SIC	DASM3 Status/Interrupt/Control Register. See **Table 13-11** for bit descriptions.	16	X
0xYF F21A	S	DASM3A	DASM3 Register A. See **13.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F21C	S	DASM3B	DASM3 Register B. See **13.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
DASM4 (CTM9 Double-Action Submodule 4)					
0xYF F220	S	DASM4SIC	DASM4 Status/Interrupt/Control Register. See **Table 13-11** for bit descriptions.	16	X
0xYF F222	S	DASM4A	DASM4 Register A. See **13.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F224	S	DASM4B	DASM4 Register B. See **13.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
PWM5 (CTM9 Pulse Width Modulation Submodule 5)					
0xYF F228	S	PWM5SIC	PWM5 Status, Interrupt and Control Register. See **Table 13-15** for bit descriptions.	16	X
0xYF F22A	S	PWM5A	PWM5 Period Register. See **13.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F22C	S	PWM5B	PWM5 Pulse Width Register. See **13.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F22E	S	PWM5C	PWM5 Counter Register. See **13.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X

Table A-2 CTM9 (Configurable Timer Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
PWM6 (CTM9 Pulse Width Modulation Submodule 6)					
0xYF F230	S	PWM6SIC	PWM6 Status, Interrupt and Control Register. See **Table 13-15** for bit descriptions.	16	X
0xYF F232	S	PWM6A	PWM6 Period Register. See **13.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F234	S	PWM6B	PWM6 Pulse Width Register. See **13.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F236	S	PWM6C	PWM6 Counter Register. See **13.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X
PWM7 (CTM9 Pulse Width Modulation Submodule 7)					
0xYF F238	S	PWM7SIC	PWM7 Status, Interrupt and Control Register. See **Table 13-15** for bit descriptions.	16	X
0xYF F23A	S	PWM7A	PWM7 Period Register. See **13.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F23C	S	PWM7B	PWM7 Pulse Width Register. See **13.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F23E	S	PWM7C	PWM7 Counter Register. See **13.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X
PWM8 (CTM9 Pulse Width Modulation Submodule 8)					
0xYF F240	S	PWM8SIC	PWM8 Status, Interrupt and Control Register. See **Table 13-15** for bit descriptions.	16	X
0xYF F242	S	PWM8A	PWM8 Period Register. See **13.7.13.2 PWMA — PWM Period Register** for bit descriptions.	16	X
0xYF F244	S	PWM8B	PWM8 Pulse Width Register. See **13.7.13.3 PWMB — PWM Pulse Width Register** for bit descriptions.	16	X
0xYF F246	S	PWM8C	PWM8 Counter Register. See **13.7.13.4 PWMC — PWM Counter Register** for bit descriptions.	16	X
DASM9 (CTM9 Double-Action Submodule 9)					
0xYF F248	S	DASM9SIC	DASM9 Status/Interrupt/Control Register. See **Table 13-11** for bit descriptions.	16	X
0xYF F24A	S	DASM9A	DASM9 Register A. See **13.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X
0xYF F24C	S	DASM9B	DASM9 Register B. See **13.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
DASM10 (CTM9 Double-Action Submodule 10)					
0xYF F250	S	DASM10SIC	DASM10 Status/Interrupt/Control Register. See **Table 13-11** for bit descriptions.	16	X
0xYF F252	S	DASM10A	DASM10 Register A. See **13.5.5.2 DASMA — DASM Data Register A** for bit descriptions.	16	X

Table A-2 CTM9 (Configurable Timer Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F254	S	DASM10B	DASM10 Register B. See **13.5.5.3 DASMB — DASM Data Register B** for bit descriptions.	16	X
MCSM11 (CTM9 Modulus Counter Submodule 11)					
0xYF F258	S	MCSM11SIC	MCSM11 Status/Interrupt/Control Register. See **Table 13-5** for bit descriptions.	16	X
0xYF F25A	S	MCSM11CNT	MCSM11 Counter Register. See **13.3.10 MCSMCNT — MCSM Counter Register** for bit descriptions.	16	X
0xYF F25C	S	MCSM11ML	MCSM11 Modulus Latch Register. See **13.3.11 MCSMML — MCSM Modulus Latch Register** for bit descriptions.	16	X
FCSM12 (CTM9 Free Running Counter Submodule 12)					
0xYF F260	S	FCSM12SIC	FCSM12 Status, Interrupt and Control Register. See **Table 13-3** for bit descriptions.	16	X
0xYF F262	S	FCSM12CNT	FCSM12 Counter Register. See **13.2.7.2 FCSMCNT — FCSM Counter Register** for bit descriptions.	16	X
SASM14 (CTM9 Single-Action Submodule 14)					
0xYF F270	S	S14ICA	SASM14 Status/Interrupt/Control Register A. See **Table 13-7** for bit descriptions.	16	X
0xYF F272	S	S14DATA	SASM14 Data Register. See **13.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F274	S	S14ICB	SASM14 Status/Interrupt/Control Register B. See **13.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F276	S	S14DATB	SASM14 Data Register B. See **13.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X
SASM16 (CTM9 Single-Action Submodule 16)					
0xYF F280	S	S16ICA	SASM16 Status/Interrupt/Control Register. See **Table 13-7** for bit descriptions.	16	X
0xYF F282	S	S16DATA	SASM16 Data Register. See **13.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F284	S	S16ICB	SASM16 Status/Interrupt/Control Register B. See **13.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F286	S	S16DATB	SASM16 Data Register B. See **13.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X
SASM18 (CTM9 Single-Action Submodule 18)					
0xYF F290	S	S18ICA	SASM18 Status/Interrupt/Control Register. See **Table 13-7** for bit descriptions.	16	X
0xYF F292	S	S18DATA	SASM18 Data Register. See **13.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F294	S	S18ICB	SASM18 Status/Interrupt/Control Register B. See **13.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X

Table A-2 CTM9 (Configurable Timer Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F296	S	S18DATB	SASM18 Data Register B. See **13.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X
SASM20 (CTM9 Single-Action Submodule 20)					
0xYF F2A0	S	S20ICA	SASM20 Status/Interrupt/Control Register. See **Table 13-7** for bit descriptions.	16	X
0xYF F2A2	S	S20DATA	SASM20 Data Register. See **13.4.4.2 SDATA — SASM Data Register A** for bit descriptions.	16	X
0xYF F2A4	S	S20ICB	SASM20 Status/Interrupt/Control Register B. See **13.4.4.3 SICB — SASM Status/Interrupt Control Register B** for bit descriptions.	16	X
0xYF F2A6	S	S20DATB	SASM20 Data Register B. See **13.4.4.4 SDATB — SASM Data Register B** for bit descriptions.	16	X

Table A-3 QADC64 (Queued Analog-to-Digital Converter)

Address	Access	Symbol	Register	Size	Reset
0xYF F400	S	QADC64MCR	QADC64 Module Configuration Register. See **Table 5-7** for bit descriptions.	16	X
0xYF F402	T	QADC64TEST	QADC64 Test Register	16	X
0xYF F404	S	QADC64INT	Interrupt Register. See **Table 5-8** for bit descriptions.	16	X
0xYF F406	S	PORTQA/ PORTQB	Port A and Port B Data. See **Table 5-9** for bit descriptions.	16	X
0xYF F408	S	DDRQA	Port A Data Direction Register. See **Table 5-10** for bit descriptions.	16	X
0xYF F40A	S	QACR0	QADC64 Control Register 0. See **Table 5-11** for bit descriptions.	16	X
0xYF F40C	S	QACR1	QADC64 Control Register 1. See **Table 5-12** for bit descriptions.	16	X
0xYF F40E	S	QACR2	QADC64 Control Register 2. See **Table 5-14** for bit descriptions.	16	X
0xYF F410	S	QASR0	QADC64 Status Register 0. See **Table 5-16** for bit descriptions.	16	X
0xYF F412	S	QASR1	QADC64 Status Register 1. See **Table 5-18** for bit descriptions.	16	X
0xYF F414 – 0xYF F5FE	—	—	Reserved	—	—
0xYF F600 – 0xYF F67F	S	CCW	QADC64 Conversion Command Word Table. See **Table 5-19** for bit descriptions.	16	X
0xYF F680 – 0xYF F6FE	S	RJURR	QADC64 Result Word Table Right-Justified, Unsigned Result Register. See **5.12.11 Result Word Table** for bit descriptions.	16	X

Table A-3 QADC64 (Queued Analog-to-Digital Converter) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F700 – 0xYF F77E	S	LJSRR	QADC64 Result Word Table Left-Justified, Signed Result Register. See **5.12.11 Result Word Table** for bit descriptions.	16	X
0xYF F780 – 0xYF F7FE	S	LJURR	QADC64 Result Word Table Left-Justified, Unsigned Result Register. See **5.12.11 Result Word Table** for bit descriptions.	16	X

Table A-4 CMFI (CDR MoneT FLASH FOR THE IMB3)

Address	Access	Symbol	Register	Size	Reset
0xYF F800	S	CMFIMCR	CMFI Module Configuration Register. See **Table 10-4** for bit descriptions.	16	X[1]
0xYF F802	—	—	Reserved	—	—
0xYF F804	S	CMFITST	CMFI Module Test Register. See **Table 10-5** for bit descriptions.	16	X
0xYF F806	—	—	Reserved	—	—
0xYF F808	S	CMFIBAH	CMFI Base Address High Register. See **Table 10-8** for bit descriptions.	16	X[1]
0xYF F80A	S	CMFIBAL	CMFI Base Address Low Register. See **Table 10-8** for bit descriptions.	16	X[1]
0xYF F80C	S	CMFICTL1	CMFI High Voltage Control Register 1. See **Table 10-9** for bit descriptions.	16	X[1]
0xYF F80E	S	CMFICTL2	CMFI High Voltage Control Register 2. See **Table 10-10** for bit descriptions.	16	X[1]
0xYF F810 – 0xYF F816	S	CMFIBS[3:0]	CMFI Shadow Block Registers. See **10.6.6.3 Programming Shadow Information** for bit descriptions.	16	X

NOTES:
1. Reset state determined by contents of the shadow row.

Table A-5 ROM Module

Address	Access	Symbol	Register	Size	Reset
0xYF F820	S	ROMMCR	ROM Module Configuration Register. See **Table 12-2** for bit descriptions.	16	X
0xYF F824	S	ROMBAH	ROM Module Base Address High Register. See **Table 12-3** for bit descriptions.	16	X
0xYF F826	S	ROMBAL	ROM Module Base Address Low Register. See **Table 12-3** for bit descriptions.	16	X
0xYF F828	S	SIGHI	ROM Module Signature High Register. See **Table 12-4** for bit descriptions.	16	X
0xYF F82A	S	SIGLO	ROM Module Signature Low Register. See **Table 12-5** for bit descriptions.	16	X
0xYF F830 – 0xYF F836	S	ROMBS[0:4]	ROM Module Bootstrap Information Words. See **12.5 Bootstrap Information Words (ROMBS0–ROMBS3)** for bit descriptions.	16	X

Table A-6 Overlay SRAM Modules (Static Random Access Memory)

Address	Access	Symbol	Register	Size	Reset
SRAM1					
0xYF F840	S	RAMMCR1	SRAM1 Module Configuration Register. See **Table 11-1** for bit descriptions.	16	X
0xYF F842	T	RAMTST1	SRAM1 Test Register.	16	X
0xYF F844	S	RAMBAH1	SRAM1 Base Address High Register. See **Table 11-3** for bit descriptions.	16	X
0xYF F846	S	RAMBAL1	SRAM1 Base Address Low Register. See **Table 11-3** for bit descriptions.	16	X
SRAM2					
0xYF F848	S	RAMMCR2	SRAM2 Module Configuration Register. See **Table 11-1** for bit descriptions.	16	X
0xYF F84A	T	RAMTST2	SRAM2 Test Register.	16	X
0xYF F84C	S	RAMBAH2	SRAM2 Base Address High Register. See **Table 11-3** for bit descriptions.	16	X
0xYF F84E	S	RAMBAL2	SRAM2 Base Address Low Register. See **Table 11-3** for bit descriptions.	16	X
SRAM3					
0xYF F848	S	RAMMCR3	SRAM3 Module Configuration Register. See **Table 11-1** for bit descriptions.	16	X
0xYF F84A	T	RAMTST3	SRAM3 Test Register.	16	X
0xYF F84C	S	RAMBAH3	SRAM3 Base Address High Register. See **Table 11-3** for bit descriptions.	16	X
0xYF F84E	S	RAMBAL3	SRAM3 Base Address Low Register. See **Table 11-3** for bit descriptions.	16	X
SRAM4					
0xYF F848	S	RAMMCR4	SRAM4 Module Configuration Register. See **Table 11-1** for bit descriptions.	16	X
0xYF F84A	T	RAMTST4	SRAM4 Test Register.	16	X
0xYF F84C	S	RAMBAH4	SRAM4 Base Address High Register. See **Table 11-3** for bit descriptions.	16	X
0xYF F84E	S	RAMBAL4	SRAM4 Base Address Low Register. See **Table 11-3** for bit descriptions.	16	X

Table A-7 DPTRAM (Dual-Port TPU RAM)

Address	Access	Symbol	Register	Size	Reset
0xYF F880	S	DPTMCR	DPT Module Configuration Register. See **Table 9-2** for bit descriptions.	16	X
0xYF F882	T	DPTTCR	DPT Test Register.	16	X
0xYF F884	S	DPTBAR	DPT Array Address Register. See **Table 9-3** for bit descriptions.	16	X
0xYF F886	S	MISRH	DPT Multiple Input Signature Register High. See **9.4.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	16	X

Table A-7 DPTRAM (Dual-Port TPU RAM) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF F888	S	MISRL	DPT Multiple Input Signature Register Low. See **9.4.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	16	X
0xYF F88A	S	MISCNT	DPT Multiple Input Signature Counter. See **9.4.5 MISC Counter (MISCNT)** for bit descriptions.	16	X

Table A-8 SCIM2E (Single-Chip Integration Module)

Address	Access	Symbol	Register	Size	Reset
0xYF FA00	S	SCIMMCR	SCIM2E Module Configuration Register. See **Table 4-1** for bit descriptions.	16	X
0xYF FA04	S	SYNCR	SCIM2E Synthesizer Control Register. See **4.3.6 Clock Synthesizer Control Register** for bit descriptions.	16	X
0xYF FA06	S	RSR	SCIM2E Rest Status Register. See **Table 4-23** for bit descriptions.	16	X
0xYF FA0A	S	PORTA	SCIM2E Port A Data Register. See **4.10.2 Port A and B Data Registers** for bit descriptions.	16	X
0xYF FA0B	S	PORTB	SCIM2E Port B Data Register. See **4.10.2 Port A and B Data Registers** for bit descriptions.	16	X
0xYF FA0C	S	PORTG	SCIM2E Port G Data Register. See **4.10.5.1 Port G and H Data Registers** for bit descriptions.	16	X
0xYF FA0D	S	PORTH	SCIM2E Port HData Register. See **4.10.5.1 Port G and H Data Registers** for bit descriptions.	16	X
0xYF FA0E	S	DDRG	SCIM2E Port G Data Direction Register. See **4.10.5.2 Port G and H Data Direction Registers** for bit descriptions.	16	X
0xYF FA0F	S	DDRH	SCIM2E Port H Data Direction Register. See **4.10.5.2 Port G and H Data Direction Registers** for bit descriptions.	16	X
0xYF FA11	S	PORTE0	SCIM2E Port E0 Data Register. See **4.10.3.1 Port E Data Register** for bit descriptions.	8	X
0xYF FA13	S	PORTE1	SCIM2E Port E1 Data Register. See **4.10.3.1 Port E Data Register** for bit descriptions.	8	X
0xYF FA14	S	DDRAB	SCIM2E Port A/B Data Direction Register. See **4.10.3.2 Port E Data Direction Register** for bit descriptions.	16	X
0xYF FA15	S	DDRE	SCIM2E Port E Data Direction Register. See **4.10.3.2 Port E Data Direction Register** for bit descriptions.	16	X
0xYF FA17	S	PEPAR	SCIM2E Port E Pin Assignment Register. See **4.10.3.3 Port E Pin Assignment Register** for bit descriptions.	8	X
0xYF FA19	S	PORTF0	SCIM2E Port F Data Register 0. See **4.10.4.1 Port F Data Register** for bit descriptions.	8	X

Table A-8 SCIM2E (Single-Chip Integration Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FA1B	S	PORTF1	SCIM2E Port F Data Register 1. See **4.10.4.1 Port F Data Register** for bit descriptions.	8	X
0xYF FA1F	S	PFPAR	SCIM2E Port F Pin Assignment Register 1. See **4.10.4.3 Port F Pin Assignment Register** for bit descriptions.	8	X
0xYF FA1D	S	DDRF	SCIM2E Port F Data Direction Register 1. See **4.10.4.2 Port F Data Direction Register** for bit descriptions.	8	X
0xYF FA21	S	SYPCR	SCIM2E System Protection Control Register. See **Table 4-15** for bit descriptions.	8	X
0xYF FA22	S	PICR	SCIM2E Periodic Interrupt Control Register. See **Table 4-9** for bit descriptions.	16	X
0xYF FA24	S	PITR	SCIM2E Periodic Interrupt Timer Register. See **Table 4-9** for bit descriptions.	16	X
0xYF FA27	S	SWSR	SCIM2E Software Watchdog Service Register. See **4.4.6.1 Software Watchdog Service Register** for bit descriptions.	8	X
0xYF FA29	S	PORTFE	SCIM2E Port F Edge-Detect Flag Register. See **4.10.4.4 Port F Edge-Detect Flag Register** for bit descriptions.	8	X
0xYF FA2B	S	PFIVR	SCIM2E Port F Edge-Detect Interrupt Vector Register. See **4.10.4.5 Port F Edge-Detect Interrupt Vector** for bit descriptions.	8	X
0xYF FA2D	S	PFLVR	SCIM2E Port F Edge-Detect Interrupt Level Register. See **4.10.4.6 Port F Edge-Detect Interrupt Level** for bit descriptions.	8	X
0xYF FA41	S	PORTC	SCIM2E PORTC Data Register. See **4.9.1.1 Port C Data Register** for bit descriptions.	8	X
0xYF FA44	S	CSPAR0	SCIM2E Chip-Select Pin Assignment Register 0. See **4.9.1 Chip-Select Pin Assignment Register** for bit descriptions.	16	X
0xYF FA46	S	CSPAR1	SCIM2E Chip-Select Pin Assignment Register 1. See **4.9.1 Chip-Select Pin Assignment Register** for bit descriptions.	16	X
0xYF FA48	S	CSBARBT	SCIM2E Chip-Select Base Address Register Boot. See **Table 4-36** for bit descriptions.	16	X
0xYF FA4A	S	CSORBT	SCIM2E Chip-Select Option Register Boot. See **Table 4-37** for bit descriptions.	16	X
0xYF FA4C	S	CSBAR0	SCIM2E Chip-Select Base Address Register 0. See **Table 4-36** for bit descriptions.	16	X
0xYF FA4E	S	CSOR0	SCIM2E Chip-Select Option Register 0. See **Table 4-37** for bit descriptions.	16	X
0xYF FA50 – 0xYF FA56	S	—	Reserved	—	X
0xYF FA58	S	CSBAR3	SCIM2E Chip-Select Base Address Register 3. See **Table 4-36** for bit descriptions.	16	X
0xYF FA5A	S	CSOR3	SCIM2E Chip-Select Option Register 3. See **Table 4-37** for bit descriptions.	16	X
0xYF FA5C – 0xYF FA5E	S	—	Reserved	—	X

Table A-8 SCIM2E (Single-Chip Integration Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FA60	S	CSBAR5	SCIM2E Chip-Select Base Address Register 5. See **Table 4-36** for bit descriptions.	16	X
0xYF FA62	S	CSOR5	SCIM2E Chip-Select Option Register 5. See **Table 4-37** for bit descriptions.	16	X
0xYF FA64	S	CSBAR6	SCIM2E Chip-Select Base Address Register 6. See **Table 4-36** for bit descriptions.	16	X
0xYF FA66	S	CSOR6	SCIM2E Chip-Select Option Register 6. See **Table 4-37** for bit descriptions.	16	X
0xYF FA68	S	CSBAR7	SCIM2E Chip-Select Base Address Register 7. See **Table 4-36** for bit descriptions.	16	X
0xYF FA6A	S	CSOR7	SCIM2E Chip-Select Option Register 7. See **Table 4-37** for bit descriptions.	16	X
0xYF FA6C	S	CSBAR8	SCIM2E Chip-Select Base Address Register 8. See **Table 4-36** for bit descriptions.	16	X
0xYF FA6E	S	CSOR8	SCIM2E Chip-Select Option Register 8. See **Table 4-37** for bit descriptions.	16	X
0xYF FA70	S	CSBAR9	SCIM2E Chip-Select Base Address Register 9. See **Table 4-36** for bit descriptions.	16	X
0xYF FA72	S	CSOR9	SCIM2E Chip-Select Option Register 9. See **Table 4-37** for bit descriptions.	16	X
0xYF FA74	S	CSBAR10	SCIM2E Chip-Select Base Address Register 10. See **Table 4-36** for bit descriptions.	16	X
0xYF FA76	S	CSOR10	SCIM2E Chip-Select Option Register 10. See **Table 4-37** for bit descriptions.	16	X

Table A-9 SRAM Module (Static Random Access Memory)

Address	Access	Symbol	Register	Size	Reset
0xYF FB00	S	RAMMCR	RAM Module Configuration Register. See **Table 11-1** for bit descriptions.	16	X
0xYF FB02	S	RAMTST	RAM Module Configuration Register.	16	X
0xYF FB04	S	RAMBAH	RAM Module Base Address High Register. See **Table 11-3** for bit descriptions.	16	X
0xYF FB06	S	RAMBAL	RAM Module Base Address Low Register. See **Table 11-3** for bit descriptions.	16	X

Table A-10 QSMCM (Queued Serial Multi-Channel Module)

Address	Access	Symbol	Register	Size	Reset
0xYF FC00	S	QSMCMMCR	QSMCM Module Configuration Register. See **Table 6-3** for bit descriptions.	16	X
0xYF FC02	T	QTEST	QSMCM Test Register.	16	X
0xYF FC04	S	QILR	QSMCM Interrupt Level, Interrupt Vector Register See **Table 6-4** for bit descriptions.	8	X
0xYF FC05	S	QIVR	QSMCM Interrupt Level, Interrupt Vector Register See **Table 6-5** for bit descriptions.	8	X
0xYF FC06	S	—	Reserved	—	X
0xYF FC07	S	QSPI_IL	QSMCM Interrupt Level, QSPI interrupt level. See **Table 6-6** for bit descriptions.	8	X

Table A-10 QSMCM (Queued Serial Multi-Channel Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FC08	S	SCC1R0	SCI1Control Register 0. See **Table 6-23** for bit descriptions.	16	X
0xYF FC0A	S	SCC1R1	SCI1Control Register 1. See **Table 6-24** for bit descriptions.	16	X
0xYF FC0C	S	SC1SR	SCI1 Status Register. See **Table 6-25** for bit descriptions.	16	X
0xYF FC0E	S	SC1DR	SCI1 Data Register. See **Table 6-26** for bit descriptions.	16	X
0xYF FC10 – 0xYF FC12	S	—	Reserved	—	X
0xYF FC14	S	PORTQS	QSMCM Port QS Data Register. See **6.6.1 Port QS Data Register (PORTQS)** for bit descriptions.	16	X
0xYF FC16	S	PQSPAR/ DDRQST	QSMCM Port QS PIn Assignment Register/ QSMCM Port QS Data Direction Register. See **Table 6-10** and **Table 6-11** for bit descriptions.	16	X
0xYF FC18	S	SPCR0	QSPI Control Register 0. See **Table 6-13** for bit descriptions.	16	X
0xYF FC1A	S	SPCR1	QSPI Control Register 1. See **Table 6-15** for bit descriptions.	16	X
0xYF FC1C	S	SPCR2	QSPI Control Register 2. See **Table 6-16** for bit descriptions.	16	X
0xYF FC1E	S	SPCR3	QSPI Control Register 3. See **Table 6-17** for bit descriptions.	16	X
0xYF FC1F	S	SPSR	QSPI Status Register 3. See **Table 6-18** for bit descriptions.	8	X
0xYF FC20	S	SCC2R0	SCI2 Control Register 0. See **Table 6-23** for bit descriptions.	16	X
0xYF FC22	S	SCC2R1	SCI2 Control Register 1. See **Table 6-24** for bit descriptions.	16	X
0xYF FC24	S	SC2SR	SCI2 Status Register. See **Table 6-24** for bit descriptions.	16	X
0xYF FC26	S	SC2DR	SCI2 Data Register. See **Table 6-26** for bit descriptions.	16	X
0xYF FC28	S	QSCI1CR	QSCI1 Control Register. See **Table 6-31** for bit descriptions.	16	X
0xYF FC2A	S	QSCI1SR	QSCI1 Status Register. See **Table 6-32** for bit descriptions.	16	X
0xYF FC2C – 0xYF FC4A	S	SCTQ	Transmit Queue Locations. See **6.8.7.5 Transmitter Operation** for bit descriptions.	16	X
0xYF FC4C – 0xYF FC6A	S	SCRQ	Receive Queue Locations. See **6.8.7.6 Receiver Operation** for bit descriptions.	16	X
0xYF FD40 – 0xYF FD7F	S/U	REC.RAM	Receive Data RAM See **6.7.2.1 Receive RAM** for bit descriptions.		
0xYF FD80 – 0xYF FDBF	S/U	TRAN.RAM	Transmit Data RAM See **6.7.2.2 Transmit RAM** for bit descriptions.		
0xYF FDC0 – 0xYF FDDF	S/U	COMD.RAM	Command RAM See **Table 6-19** for bit descriptions.		

Table A-11 TPU3 (Time Processor Unit)

Address	Access	Symbol	Register	Size	Reset
0xYF FE00	S	TPUMCR	TPU3 Module Configuration Register See **Table 8-6** for bit descriptions.	16	X
0xYF FE02	T	TCR	TPU3 Test Configuration Register	16	X
0xYF FE04	S	DSCR	Development Support Control Register See **Table 8-7** for bit descriptions.	16	X
0xYF FE06	S	DSSR	Development Support Status Register See **Table 8-8** for bit descriptions.	16	X
0xYF FE08	S	TICR	TPU3 Interrupt Configuration Register See **Table 8-9** for bit descriptions.	16	X
0xYF FE0A	S	CIER	Channel Interrupt Enable Register See **Table 8-10** for bit descriptions.	16	X
0xYF FE0C	S	CFSR0	Channel Function Selection Register 0 See **Table 8-11** for bit descriptions.	16	X
0xYF FE0E	S	CFSR1	Channel Function Selection Register 1 See **Table 8-11** for bit descriptions.	16	X
0xYF FE10	S	CFSR2	Channel Function Selection Register 2 See **Table 8-11** for bit descriptions.	16	X
0xYF FE12	S	CFSR3	Channel Function Selection Register 3 See **Table 8-11** for bit descriptions.	16	X
0xYF FE14	S	HSQR0	Host Sequence Register 0 See **Table 8-12** for bit descriptions.	16	X
0xYF FE16	S	HSQR1	Host Sequence Register 1 See **Table 8-12** for bit descriptions.	16	X
0xYF FE18	S	HSRR0	Host Service Request Register 0 See **Table 8-13** for bit descriptions.	16	X
0xYF FE1A	S	HSRR1	Host Service Request Register 1 See **Table 8-13** for bit descriptions.	16	X
0xYF FE1C	S	CPR0	Channel Priority Register 0 See **Table 8-14** for bit descriptions.	16	X
0xYF FE1E	S	CPR1	Channel Priority Register 1 See **Table 8-14** for bit descriptions.	16	X
0xYF FE20	S	CISR	Channel Interrupt Status Register See **Table 8-16** for bit descriptions.	16	X
0xYF FE22	T	LR	Link Register	16	X
0xYF FE24	T	SGLR	Service Grant Latch Register	16	X
0xYF FE26	T	DCNR	Decoded Channel Number Register	16	X
0xYF FE28	S	TPUMCR2	TPU Module Configuration Register 2 See **Table 8-17** for bit descriptions.	16	X
0xYF FE2A	S	TPUMCR3	TPU Module Configuration 3 See **Table 8-20** for bit descriptions.	16	X
0xYF FE2C	T	ISDR	Internal Scan Data Register	16	X
0xYF FE2E	T	ISCR	Internal Scan Control Register	16	X
0xYF FF00 – 0xYF FF0F	S	—	Channel 0 Parameter Registers	16	X
0xYF FF10 – 0xYF FF1F	S	—	Channel 1 Parameter Registers	16	X
0xYF FF20 – 0xYF FF2F	S	—	Channel 2 Parameter Registers	16	X

Table A-11 TPU3 (Time Processor Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0xYF FF30 – 0xYF FF3F	S	—	Channel 3 Parameter Registers	16	X
0xYF FF40 – 0xYF FF4F	S	—	Channel 4 Parameter Registers	16	X
0xYF FF50 – 0xYF FF5F	S	—	Channel 5 Parameter Registers	16	X
0xYF FF60 – 0xYF FF6F	S	—	Channel 6 Parameter Registers	16	X
0xYF FF70 – 0xYF FF7F	S	—	Channel 7 Parameter Registers	16	X
0xYF FF80 – 0xYF FF8F	S	—	Channel 8 Parameter Registers	16	X
0xYF FF90 – 0xYF FF9F	S	—	Channel 9 Parameter Registers	16	X
0xYF FFA0 – 0xYF FFAF	S	—	Channel 10 Parameter Registers	16	X
0xYF FFB0 – 0xYF FFBF	S	—	Channel 11 Parameter Registers	16	X
0xYF FFC0 – 0xYF FFCF	S	—	Channel 12 Parameter Registers	16	X
0xYF FFD0 – 0xYF FFDF	S	—	Channel 13 Parameter Registers	16	X
0xYF FFE0 – 0xYF FFEF	S	—	Channel 14 Parameter Registers	16	X
0xYF FFF0 – 0xYF FFFF	S	—	Channel 15 Parameter Registers	16	X