APPENDIX E
ELECTRICAL CHARACTERISTICS

E.1 Absolute Maximum Ratings

Table E-1 Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	3.3V Supply Voltage[1, 2, 6] 5V Supply Voltage	V_{DDL}, $V_{DDDP-TRAM}$ V_{DDH}	– 0.3 to + 4.0 – 0.3 to + 6.0	V
2	Input Voltage[1, 2, 4, 6]	V_{in}	– 0.3 to + 5.5	V
3	Instantaneous Maximum Current Single pin limit (applies to all pins)[1, 4, 5, 6]	I_D	25	mA
4	Operating Maximum Current Digital Input Disruptive Current [3, 4, 5, 6, 7] $V_{NEGCLAMP} \cong$ – 0.3 V $V_{POSCLAMP} \cong V_{DD}$ + 0.3	I_{ID}	– 500 to 500	µA
5	Operating Temperature Range No Suffix “C” Suffix “V” Suffix “M” Suffix	T_A	T_L to T_H 0 to 70 – 40 to 85 – 40 to 105 – 40 to 125	°C
6	Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL and XFC are internally clamped to V_{DD}. Does not include QADC64 pins (see **Table E-10**).
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions except for V_{PP}.
6. This parameter is periodically sampled rather than 100% tested.
7. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

E.2 Radiated Emissions

Characterization of device emissions will be performed per SAE J1752/3 issued March 1995.

E.3 Thermal Characteristics

Table E-2 Thermal Characteristics

Num	Characteristic	Symbol	Value	Unit
1	Thermal Resistance Thermal Resistance 217 /P4 PBGA Package	Θ_{JA}	TBD	°C/W

The average chip-junction temperature (T_J) in C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \qquad (1)$$

where:

T_A = Ambient Temperature, °C
Θ_{JA}= Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT}= I_{DD} \times V_{DD}$, Watts — Chip Internal Power
$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_{D^2} \qquad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

E.4 DC Characteristics

Table E-3 DC Characteristics

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1a	3v Input High Voltage, EPEB0	V_{IH3}	2.0	V_{DDH} + 0.3	V
1b	5v Input High Voltage[1] Groups 2 and 7 pins, except EPEB0 Groups 1, 5, and 6 pins	V_{IH5}	 0.7 (V_{DDH}) 3.3	 V_{DDH} + 0.3 $V_{DD}H$ + 0.3	 V V
2a	3v Input Low Voltage, EPEB0	V_{IL3}	V_{SS} – 0.3	0.8	V
2b	5v Input Low Voltage[1] Groups 2 and 7 pins, except EPEB0 Groups 1, 5, and 6 pins	V_{IL5}	 V_{SS} – 0.3 V_{SS} – 0.3	 0.2 (V_{DDH}) 2.3	 V V
3	Input Hysteresis $\overline{BKPT}$/DSCLK, CTM2C, Port CT, $\overline{IPIPE}$/DSO, Port A, Port B, Port E[7:3], Port F, Port G, Port H, $\overline{RESET}$, $\overline{IFETCH}$/DSI, Port TP, T2CLK	V_{HYS}	0.5	—	V
4	3v and 5v Input Leakage Current[1] $V_{in} = V_{DD}$ or V_{SS} all I/O and Input-only pins	I_{in}	–1.0	1.0	µA
5	High Impedance (Off-State) Leakage Current[1] $V_{in} = V_{DD}$ or V_{SS} All I/O and Output-only pins	I_{OZ}	–1.0	1.0	µA

Table E-3 DC Characteristics (Continued)

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
6	3v Output High Voltage I_{OH} = –.01 mA XTAL	V_{OH3}	2.4	—	V
6a	5v Fast Output High Voltage[1, 2] IOH = –2.0 mA Groups 3 and 4 Output-only and Groups 5, 6, and 7 I/O pins	V_{OH5}	V_{DDH} – 0.7	—	V
6b	5v Slow Output High Voltage[2] I_{OH} = –0.4 mA Ports A, B, C, E, F, G, H	V_{OH5S}	V_{DDH} – 0.7	—	V
7	3v Output Low Voltage I_{OL} = .01 mA XTAL	V_{OL3}	—	0.4	V
7a	5v Fast Output Low Voltage[1] I_{OL}= 4.0 mA Group 4 Output-only and Groups 5 I/O pins I_{OL}= 2.0 mA Group 3 Output-only and Groups 6 and 7 I/O pins	V_{OL5}	—	0.4	V
7b	5v Slow Output Low Voltage I_{OL} = 0.4 mA Ports A, B, C, E, F, G, H	V_{OL5S}	—	0.4	V
8	Data Bus Mode Select Pull-up Current V_{in} = V_{IL} DATA[15:0] V_{in} = V_{IH} DATA[15:0]	I_{MSP}	— –15	–120 —	µA
9	V_{DD} Supply Current[3] RUN[4] RUN, TPU3 emulation mode CMFI Program/Erase Adder[5] LPSTOP, 4.194MHz crystal, VCO Off (STSIM = 0) LPSTOP (External clock input frequency = maximum f_{sys})	I_{DDL} I_{DDH} I_{DDL} S_{IDD} S_{IDD}	— — — — —	190 40 210 100 500 10	mA mA mA mA µA mA
10	Clock Synthesizer Operating Voltage	V_{DDSYN}	3.0	3.6	V
11	V_{DDSYN} Supply Current[3] 4.194 MHz crystal, VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, 4.194MHz crystal, VCO off (STSIM = 0) 4.194 MHz crystal, V_{DD} powered down	I_{DDSYN} I_{DDSYN} S_{IDDSYN} I_{DDSYN}	— — — —	10 7 5 5	mA mA mA mA
12	RAM Standby Voltage[6] Specified V_{DD} applied V_{DD} = V_{SS}	V_{SB}	0.0 3.0	3.6 3.6	V
12A	DPTRAM Voltage[7]	$V_{DDDP-TRAM}$	3.0	3.6	V
13	RAM Standby Current[3, 6, 8] Normal RAM operation $V_{DD} > V_{SB} – 0.5$ V Transient condition $V_{SB} – 0.5$ V ≥ V_{DD} ≥ V_{SS} + 0.5 V Standby operation $V_{DD} < V_{SS}$ + 0.5 V	I_{SB}	— — —	10 3 25	µA mA µA

Table E-3 DC Characteristics (Continued)

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
13A	DPTRAM Current[3, 7, 8]	I_{DPTRAM}	—	20	mA
14	Power Dissipation[9]	P_D	—	1.07	W
15	Input Capacitance[1, 10]	—	—		pF
	All Input-only pins		—	10	
	All I/O pins		—	20	
16	Load Capacitance[1]	C_L	—		pF
	Groups 4 and 5 I/O pins		—	70	
	Group 3 Output-Only and Groups 6 and 7 I/O pins		—	50	

NOTES:

1. Input-Only Pins:
   - Group 1:
     - $\overline{BKPT}$/DSCLK, TSC, CTM2C, $\overline{BERR}$/$\overline{SCEN}$, $\overline{T2CLK}$
   - Group 2:
     - Port QS - PQS8/RXD1, PQS10/RXD2
     - Other — XFC, EXTAL, ANX[15:0], CNRX, EPEB0

   Output-Only Pins:
   - Group 3:
     - Port CT — $\overline{CPWM}$[8:5]
     - Other — $\overline{CNTX}$
   - Group 4:
     - Port C — $\overline{ADDR23}$/$\overline{CS10}$/$\overline{ECLK}$, $\overline{ADDR}$[22:19]/$\overline{CS}$[9:6]/$\overline{PC}$[6:3], $\overline{FC2}$/$\overline{CS5}$/$\overline{PC2}$, $\overline{FC1}$/$\overline{PC1}$, $\overline{FC0}$/$\overline{CS3}$/$\overline{PC0}$
     - Other — $\overline{IPIPE}$/$\overline{DS0}$, $\overline{CSBOOT}$, $\overline{BG}$/CSM, $\overline{CLKOUT}$, $\overline{FREEZE}$/QOUT, $\overline{ADDR}$[2:0], R/$\overline{W}$
   - Group 8:
     - Other — $\overline{XTAL}$

   Input/Output Pins:
   - Group 5:
     - Port A — PA[7:0]/ADDR[18:11]
     - Port B — PB[7:0]/ADDR[10:3]
     - Port E — PE[7:6]/$\overline{SIZ}$[1:0], PE5/$\overline{AS}$, PE4/$\overline{DS}$, PE[1:0]/$\overline{DSACK}$[1:0]
     - Port F — PF[7:5]/$\overline{IRQ}$[7:5], PF0/FASTREF
     - Port G — PG[7:0]/DATA[15:8]
     - Port H — PH[7:0]/DATA[7:0]
     - Other — $\overline{HALT}$, $\overline{RESET}$, $\overline{BGACK}$/$\overline{CSE}$, $\overline{BR}$/$\overline{CS0}$, $\overline{IFETCH}$/DSI
   - Group 6:
     - Port CT — $\overline{CTD}$[10:9]/[4:3], $\overline{CTS}$[20A/B:18A/B:16A/B14A/B]
     - Port TP — $\overline{TP}$[15:0]
   - Group 7:
     - Port QS — PQS7/TXD1, PQS9/TXD2, PQS[6:4]/PCS[3:1], PQS3/PCS0/$\overline{SS}$, PQS2/SCK, PQS1/MOSI, PQS0/MISO

   Pin groups do not include QADC64 pins. See **Table E-10** through **Table E-13** for information concerning the QADC64.
2. Use of an active pulldown device is recommended during reset to select operating mode.
3. Total operating current is the sum of the appropriate I_{DDH}, I_{DDL} , I_{DDSYN}, I_{DDA}, I_{DPTRAM}, and I_{SB} values.
4. Current measured at 24 MHz system clock frequency, all modules active.
5. Add current if CMFI is being programed or erased.
6. The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 volts. The SRAM array cannot be accessed while the module is in standby mode.
7. The DPTRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 volts. The DPTRAM array cannot be accessed while the module is in standby mode.
8. When V_{DD} is transitioning during power-up or power down sequence, and V_{SB} is applied, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the V_{DD} and V_{STBY} pins can contribute to this condition.
9. Power dissipation measured at 24 MHz system clock frequency, all modules active, not in TPU emulation mode, not programming or erasing the CMFI. Add for TPU emulation and/or CMFI program/erase operation. Power dissipation can be calculated using the following expression:

   P_D = Maximum V_{DDH} (I_{DDH} + I_{DDA}) + Maximum V_{DDL} (I_{DDL} + I_{DDSYN} +I_{DPTRAM} + I_{SB})
10. This parameter is periodically sampled rather than 100% tested.

E.5 AC Characteristics

Table E-4 Clock Control Timing

(V_{DDL} and V_{DDSYN} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H.)

Num	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL Reference Frequency Range Indirect: Fast reference mode Slow reference mode	f_{ref}	 1 25	 6 50	 MHz KHz
2	System Frequency [1] On-Chip PLL System Frequency: Fast reference mode Slow reference mode External Clock Operation	f_{sys}	DC $(f_{ref})/128$ $4(f_{ref})$ dc	33.6 33.6 33.6 33.6	MHz
3	PLL Lock Time Changing W or Y in SYNCR or exiting from LPSTOP[2] Warm Start-up[3] Cold start (fast mode only)[4]	t_{lpll}	 — — —	 20 50 75	ms
4	VCO frequency[5]	f_{VCO}	—	$2(f_{sys}$ max)	MHz
5	Limp Mode Clock Frequency [6]	f_{limp}	0.1	f_{sys} max/2	MHz
6	CLKOUT Jitter[7,8] Slow Reference Mode (32.768 kHz): Short term (5 µs interval) Long term (500 µs interval) Fast Reference Mode (4.194 MHz): Short term (3 system clocks) Long term (2 ms interval)	J_{CLK}	 -0.5 -0.05 -1.0 -0.01	 0.5 0.05 1.0 0.01	 %

NOTES:

1. All internal registers retain data at 0 Hz.
2. Assumes that V_{DDSYN} and V_{DD} are stable, that an external filter is attached to the XFC pin, and that the crystal oscillator is stable.
3. Assumes that V_{DDSYN} is stable, that an external filter is attached to the XFC pin, and that the crystal oscillator is stable, followed by V_{DD} ramp-up. Lock time is measured from VDD at specified minimum to $\overline{\text{RESET}}$ negated.
4. Cold start is measured from V_{DDSYN} and V_{DD} at specified minimum to $\overline{\text{RESET}}$ negated.
5. Internal VCO frequency (f_{VCO}) is determined by SYNCR W and Y bit values. The SYNCR X bit controls a divide-by-two circuit that is not in the synthesizer feedback loop. When X = 0, the divider is enabled, and $f_{sys} = f_{VCO}/4$. When X = 1, the divider is disabled, and $f_{sys} = f_{VCO}/2$. X must equal one when operating at maximum specified f_{sys}.
6. Determined by internal loss-of-clock oscillator operating frequency.
7. Jitter is the average deviation from programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via power supply pins and variation in crystal oscillator frequency increase the stability percentage for a given interval. The use of reference frequencies and system frequencies very much different than those shown here may require different XFC filter values than shown in **4.3.7.2 Phase Comparator and Filter** to maintain optimum jitter performance.
8. This parameter is periodically sampled rather than 100% tested.

Table E-5 AC Timing

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} and V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation	f_{SLW}	0.13	33.6	MHz
1	Clock Period	t_{cyc}	29.8	—	ns
1A	ECLK Period	t_{Ecyc}	$8*t_{cyc}$	—	ns
1B	External Clock Input Period[2,3]	t_{Xcyc}	14.9	—	ns
2, 3	Clock Pulse Width	t_{CW}	$0.5t_{cyc}$-3	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	t_{cyc}-7	—	ns
2B, 3B	External Clock Input High/Low Time[2]	t_{XCHL}	7.45	—	ns
4, 5	Clock Rise and Fall Time	t_{Crf}	—	3	ns
4A, 5A	Rise and Fall Time SCIM2E pins: CSBOOT, CLKOUT, $\overline{BKPT}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{BG}$, $\overline{BR}$, $\overline{BGACK}$, A[23,2:0], FREEZE, $\overline{BERR}$, R/$\overline{W}$, $\overline{HALT}$, $\overline{RESET}$ FC[2:0], A[22:3], D[15:0], SIZE[1:0], $\overline{AS}$, $\overline{DS}$, RMC, AVEC, $\overline{DSACK}$[1:0][4] Fast[5] Slow[5.] IRQ[7:1], FASTREF[6]	t_{rf}	—	3 3 >200 >200	ns
4B, 5B	External Clock Rise and Fall Time[7]	t_{XCrf}	—	3	ns
6	Clock High to Address, FC, SIZE Valid	t_{CHAV}	0	0.5	t_{cyc}
7	Clock High to Address, Data, FC, SIZE High Impedance	t_{CHAZx}	0	1.0	t_{cyc}
8	Clock High to Address, FC, SIZE Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	$0.5t_{cyc}$	ns
9A	$\overline{AS}$, to $\overline{DS}$, or $\overline{CS}$ Asserted (Read)[8]	t_{STSA}	–15	8	ns
9C	Clock Low to $\overline{IFETCH}$, $\overline{IPIPE}$ Asserted	t_{CLIA}	2	11	ns
11	Address, FC, SIZE Valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Asserted	t_{AVSA}	0.25	—	t_{cyc}
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	1	15	ns
12A	Clock Low to $\overline{IFETCH}$, $\overline{IPIPE}$ Negated	t_{CLIN}	1	11	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to Address, FC, SIZE Invalid (Address Hold)	t_{SNAI}	0.25	—	t_{cyc}
14	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Read) Width Asserted	t_{SWA}	50	—	ns
14A	$\overline{DS}$, $\overline{CS}$ Width Asserted (Write)	t_{SWAW}	23	—	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted (Fast Write Cycle)	t_{SWDW}	20	—	ns
15	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated[9]	t_{SN}	20	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	30	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to R/$\overline{W}$ Negated	t_{SNRN}	0.25	—	t_{cyc}
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	0.5	t_{cyc}

Table E-5 AC Timing (Continued)

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} and V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	0.5	t_{cyc}
21	R/$\overline{W}$ Asserted to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	0.25	—	t_{cyc}
22	R/$\overline{W}$ Low to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{RASA}	35	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	0.5	t_{cyc}
24	Data Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$ (Fast Write Cycle)	t_{DVASN}	0.25	—	t_{cyc}
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	0.25	—	t_{cyc}
26	Data Out Valid to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{DVSA}	0.25	—	t_{cyc}
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	3	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	10	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACK[1]}$, $\overline{BERR}$, $\overline{HALT}$ Negated	t_{SNDN}	0	40	ns
29	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)[10]	t_{SNDI}	0	—	ns
29A	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance [10, 11]	t_{SHDI}	—	28	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold)[10]	t_{CLDI}	0.25	—	t_{cyc}
30A	CLKOUT Low to Data In High Impedance[10]	t_{CLDH}	—	45	ns
31	$\overline{DSACK[1]}$ Asserted to Data In Valid[12]	t_{DADI}	—	25	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBAN}	—	0.5	t_{cyc}
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted[13]	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
39	$\overline{BG}$ Width Negated	t_{GH}	1	—	t_{cyc}
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	t_{cyc}
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	75	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Write or Read Cycle)	t_{RWAS}	45	—	ns
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1]}$, $\overline{BERR}$, $\overline{HALT}$	t_{AIST}	3	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	8	—	ns
48	$\overline{DSACK[1]}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted[14]	t_{DABA}	—	0.5	t_{cyc}
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	14	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	20	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	t_{HRPW}	512	—	t_{cyc}
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	t_{BNHN}	0	—	ns
70	Clock Low to Data Bus Driven (Show)	t_{SCLDD}	0	0.5	t_{cyc}
71	Data Setup Time to Clock Low (Show)	t_{SCLDS}	8	—	ns
72	Data Hold from Clock Low (Show)	t_{SCLDH}	5	—	ns

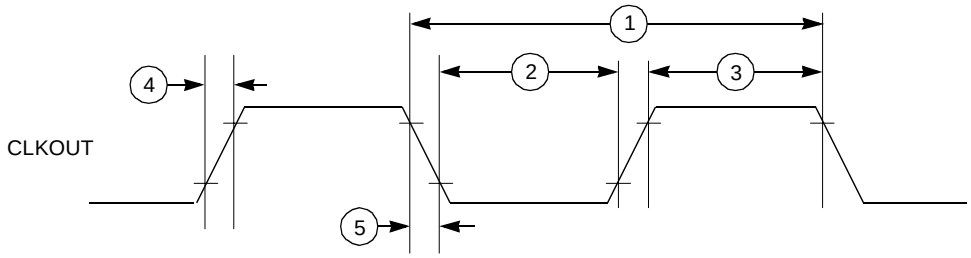
Table E-5 AC Timing (Continued)

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} and V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	0.25	—	t_{cyc}
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	5	—	ns
75	Mode Select Setup Time	t_{MSS}	10	—	t_{cyc}
76	Mode Select Hold Time	t_{MSH}	0	—	ns
77	$\overline{RESET}$ Assertion Time[15]	t_{RSTA}	2	—	t_{cyc}
78	$\overline{RESET}$ Rise Time[16,17]	t_{RSTR}	—	10	t_{cyc}

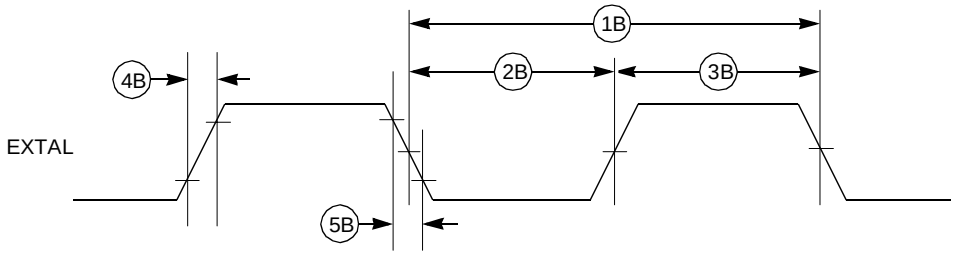
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When an external clock is used, minimum high and low times are based on a 50% duty cycle. The minimum allowable t_{Xcyc} period is reduced when the duty cycle of the external clock varies. The relationship between external clock input duty cycle and minimum t_{Xcyc} is expressed:
   Minimum t_{Xcyc} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).
3. Due to the requirement by the CMFI module, the SCIM2E on this device requires an external clock equal to 2X system frequency to be driven when in external clock mode.
4. Rev B silicon has these pins forced in FAST mode.
5. Pins are set to FAST mode when they are configured as bus and bus control pins. Pins are set to SLOW mode when they are digital I/O. The SCIM2E has a bit in the MCR to force FAST Mode.
6. These pins have fast and slow rise fall times of 3 and >200, depending on the state of the SLOWE bit in the SCIMMCR.
7. Parameters for an external clock signal applied while the internal PLL is disabled (VDDSYN/MODCLK pin held low during reset). Does not pertain to an external reference clock source while the PLL is enabled (VDDSYN/MODCLK pin held high during reset). When the PLL is enabled, the clock synthesizer detects successive transitions of the reference signal. If transitions occur within the correct clock period, rise/fall times and duty cycle are not critical.
8. The amount of skew depends on the relative loading of these signals.
9. If multiple chip selects are used, $\overline{CS}$ width negated applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
10. Hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
11. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
12. If the asynchronous setup time requirements are satisfied, the $\overline{DSACK[1]}$ low to data setup time and $\overline{DSACK[1]}$ low to $\overline{BERR}$ low setup time can be ignored. The data must only satisfy the data-in to clock low setup time for the following clock cycle. $\overline{BERR}$ must satisfy only the late $\overline{BERR}$ low to clock low setup time for the following clock cycle.
13. To ensure coherency during every operand transfer, $\overline{BG}$ is not asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete.
14. In the absence of $\overline{DSACK[1]}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time.
    Address access time = (2.5 + WS) t_{cyc} – t_{CHAV} – t_{DICL}
    Chip select access time = (2 + WS) t_{cyc} – t_{CLSA} – t_{DICL}
    Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = –1.
15. After external $\overline{RESET}$ negation is detected, a short transition period (approximately 2 t_{cyc}) elapses, then the Integration Module drives $\overline{RESET}$ low for 512 tcyc.
16. External assertion of the $\overline{RESET}$ input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, $\overline{RESET}$ must be asserted for at least 590 CLKOUT cycles.
17. External logic must pull $\overline{RESET}$ high during this period in order for normal MCU operation to begin.



68300 CLKOUT TIM

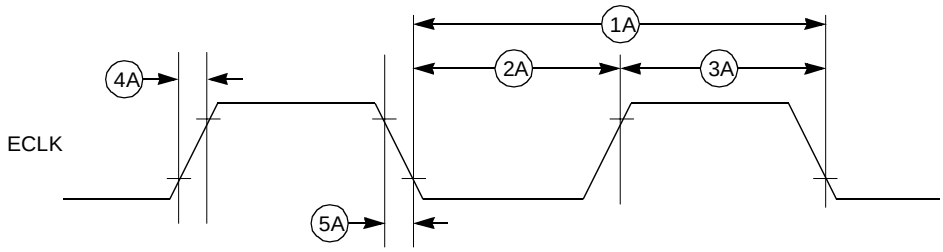
Figure E-1 CLKOUT Output Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}.
PULSE WIDTH SHOWN WITH RESPECT TO 50% V_{DD}.

68300 EXT CLK INPUT TIM

Figure E-2 External Clock Input Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}

68300 ECLK OUTPUT TIM

Figure E-3 ECLK Output Timing Diagram

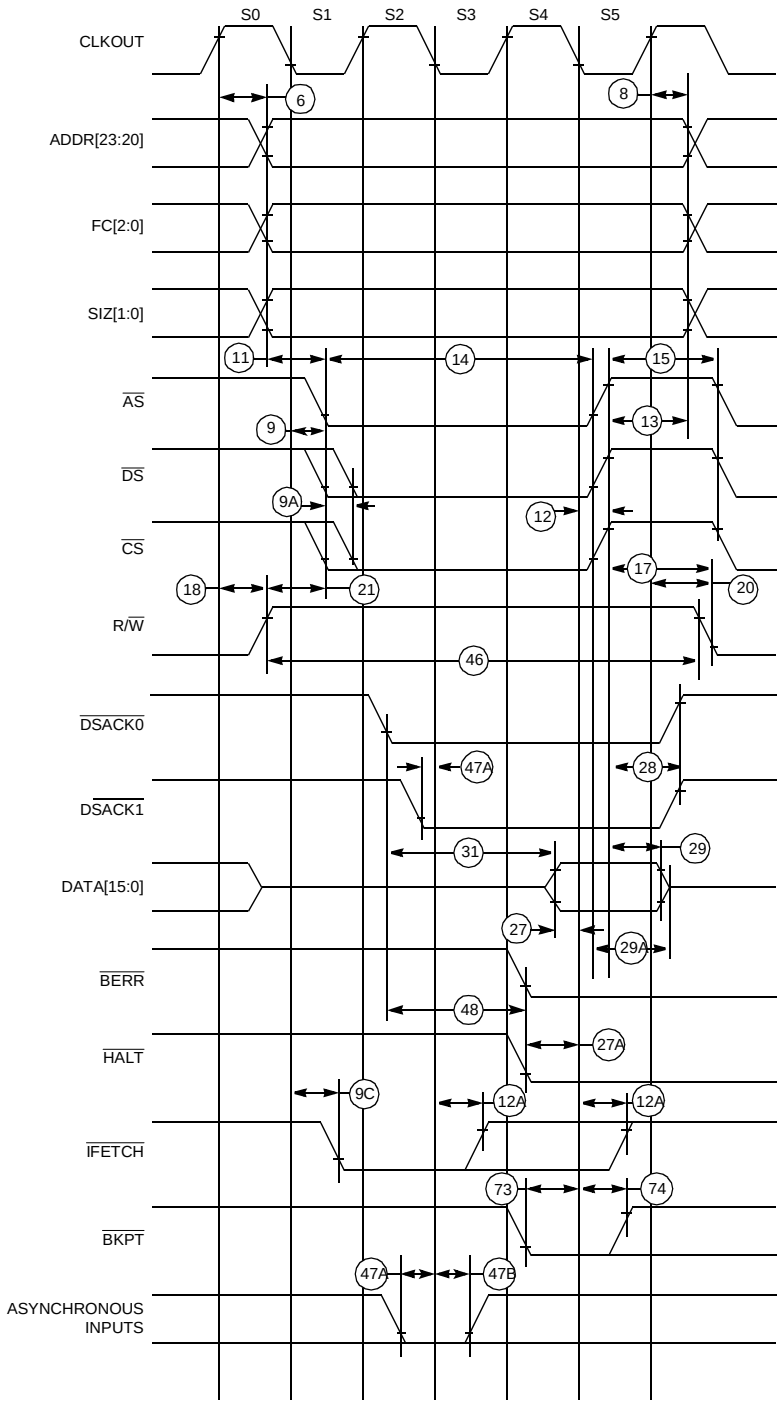


Figure E-4 Read Cycle Timing Diagram

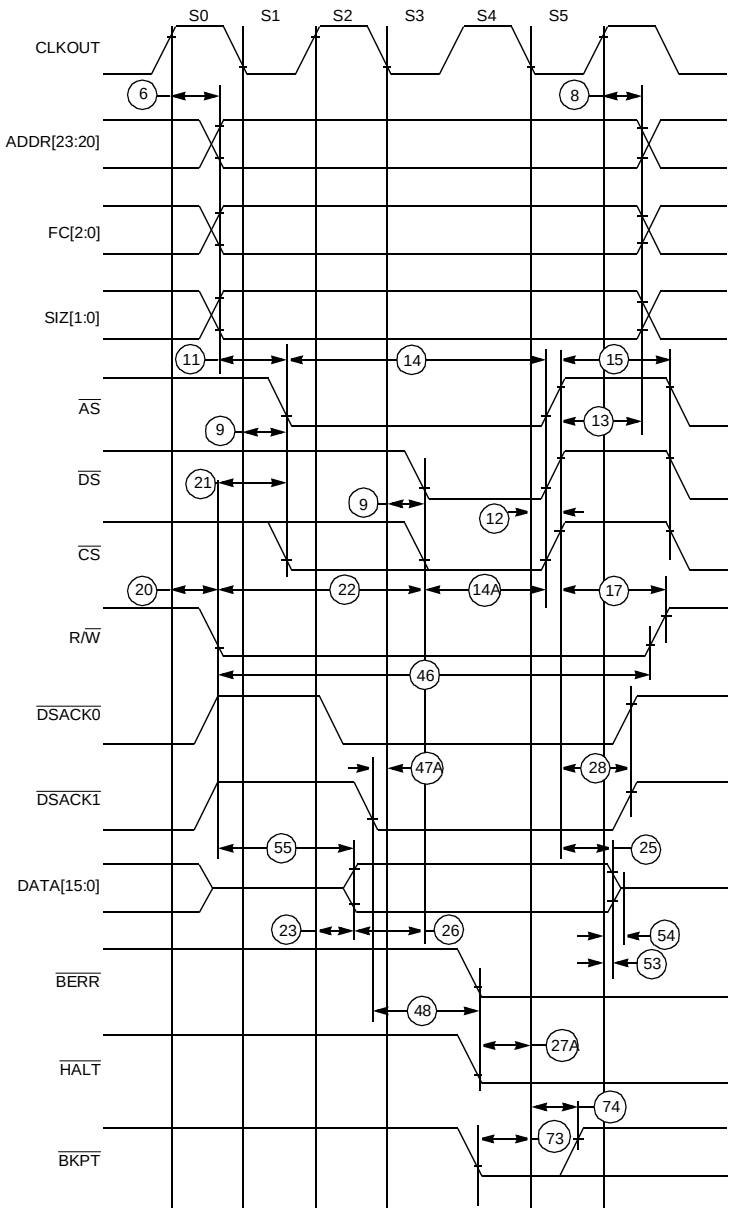


Figure E-5 Write Cycle Timing Diagram

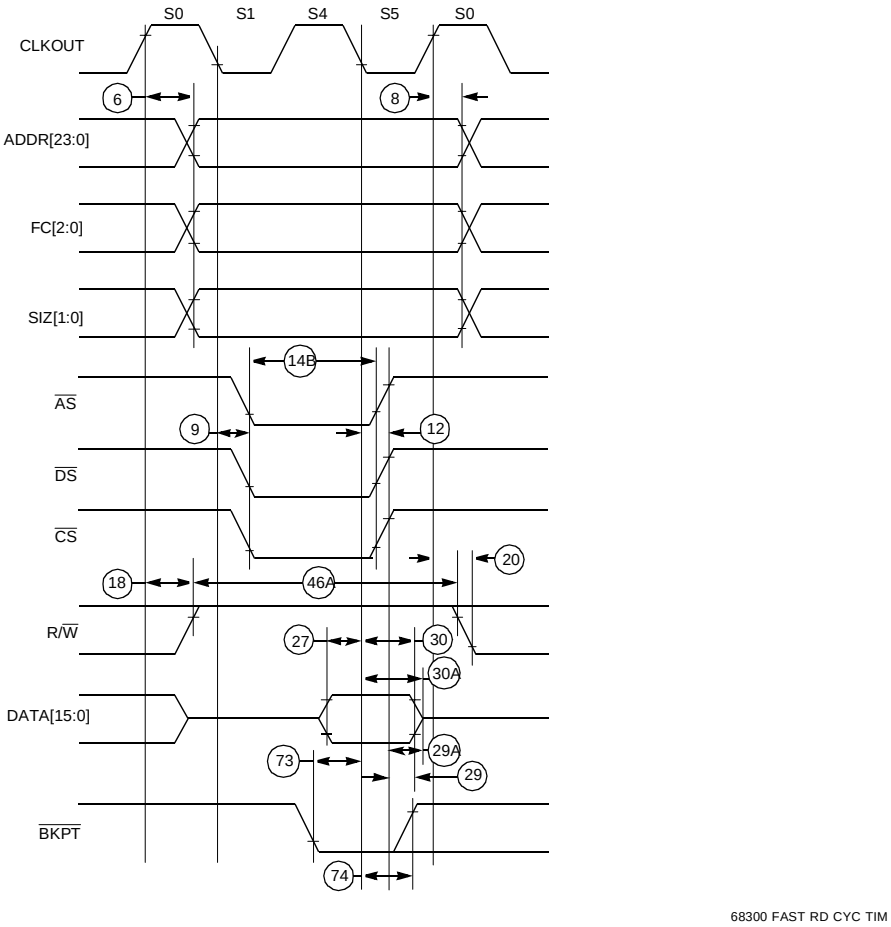


Figure E-6 Fast Termination Read Cycle Timing Diagram

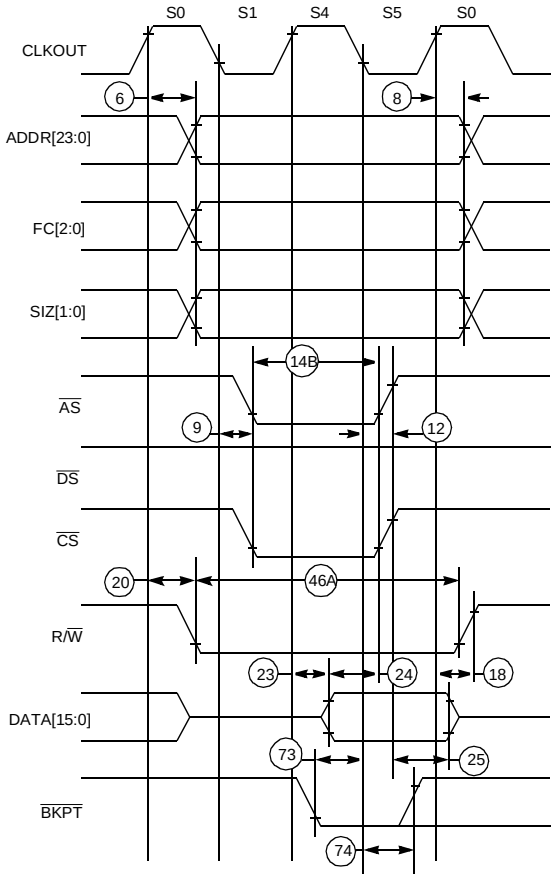


Figure E-7 Fast Termination Write Cycle Timing Diagram

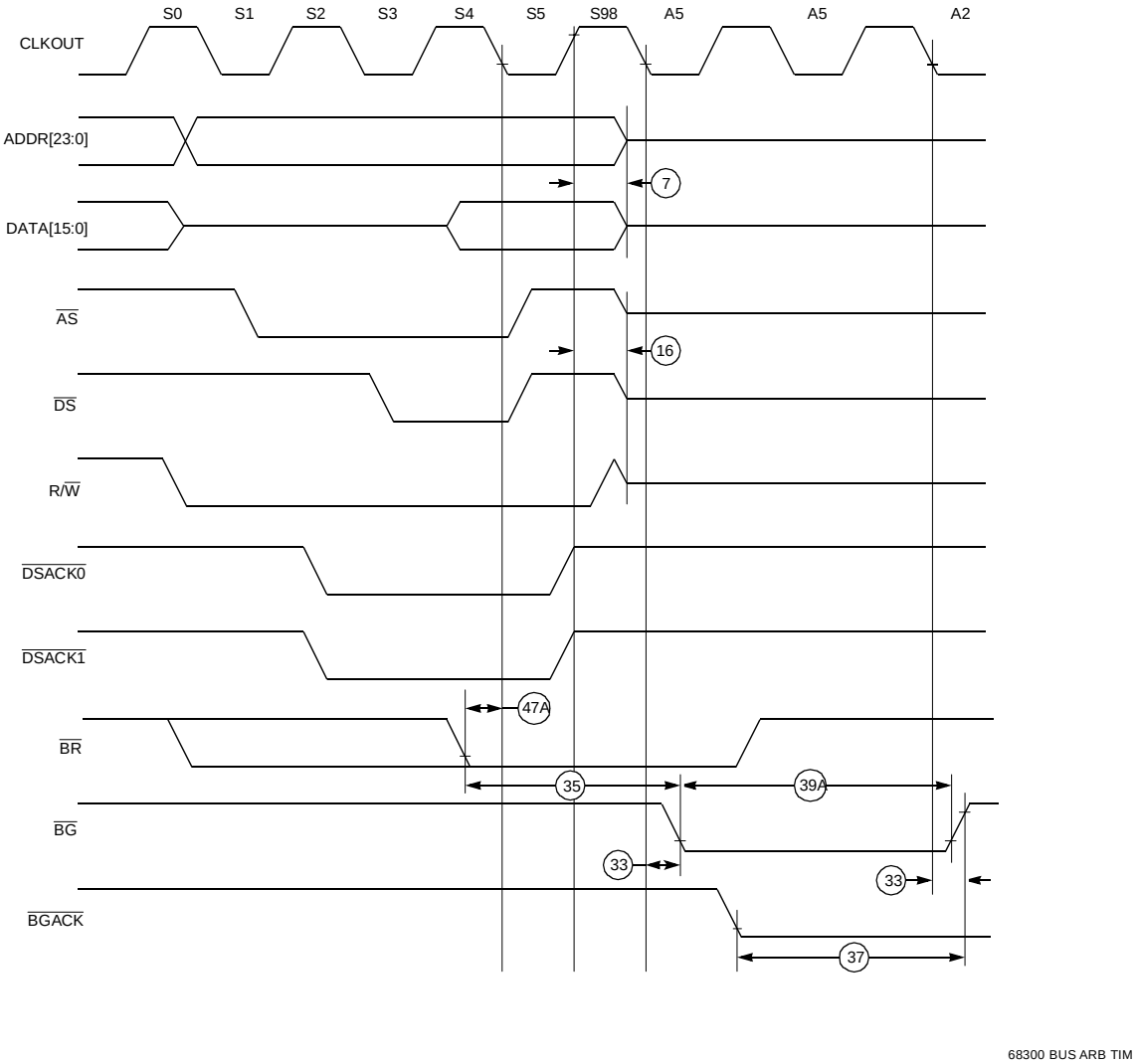


Figure E-8 Bus Arbitration Timing Diagram — Active Bus Case

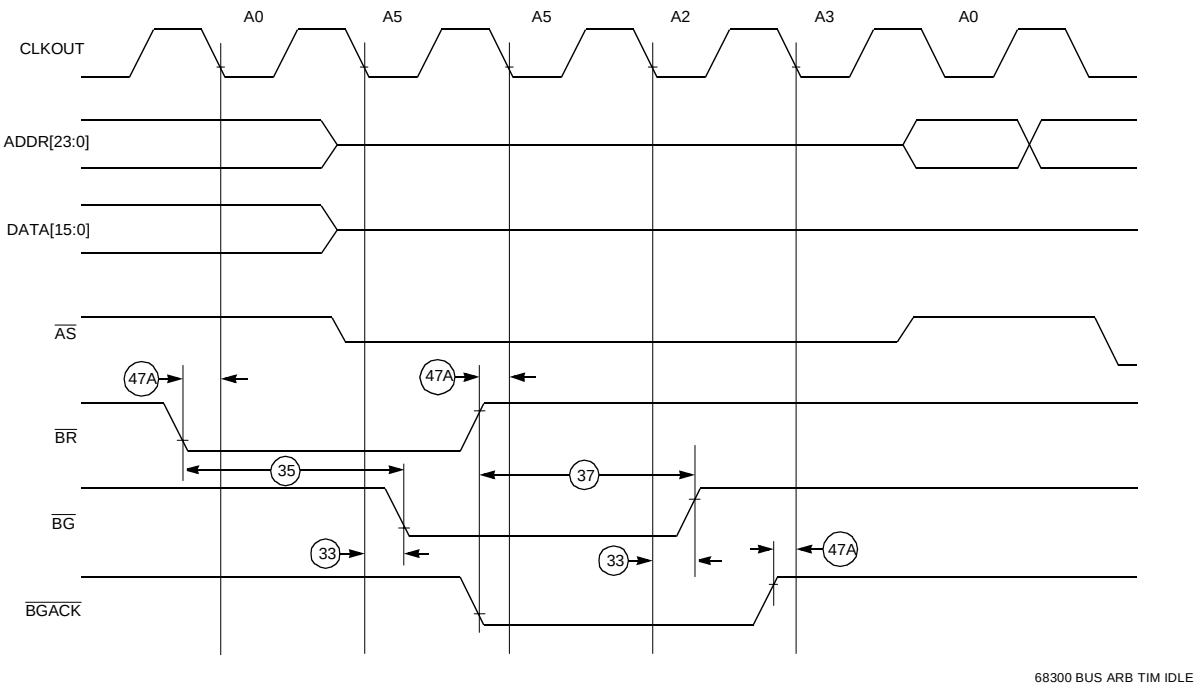
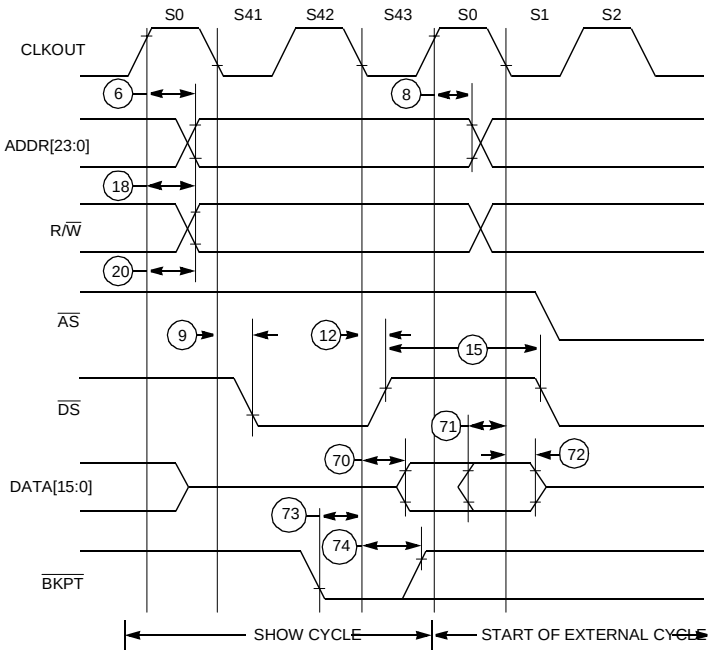


Figure E-9 Bus Arbitration Timing Diagram — Idle Bus Case



NOTE:
Show cycles can stretch during clock phase S42 when bus accesses take longer than two cycles due to IMB module wait-state insertion.

68300 SHW CYC TIM

Figure E-10 Show Cycle Timing Diagram

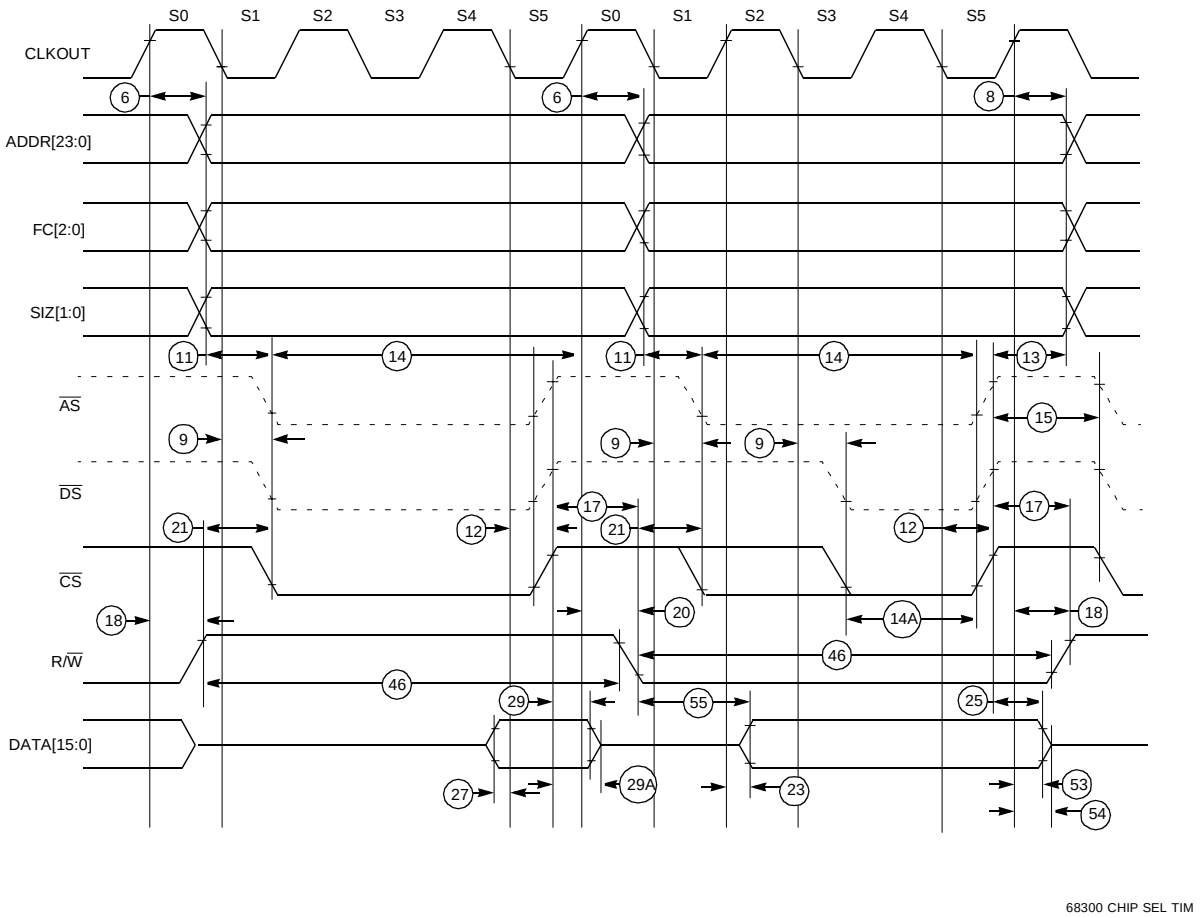


Figure E-11 Chip-Select Timing Diagram

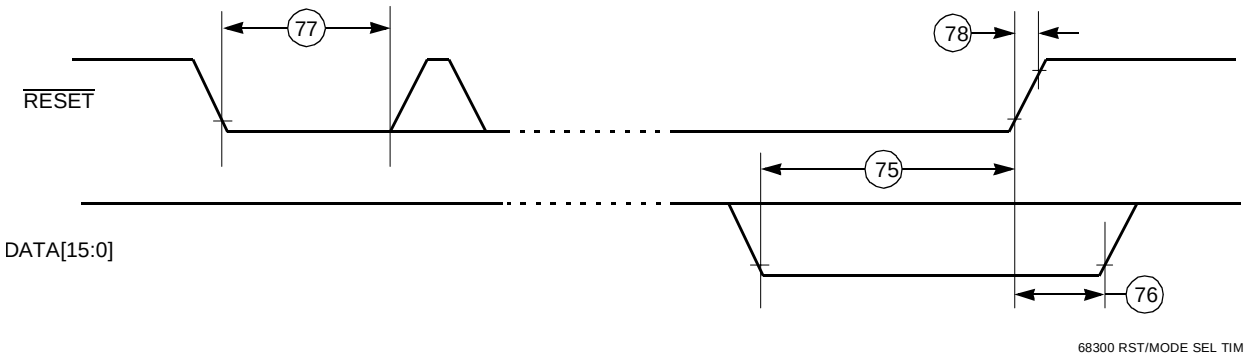


Figure E-12 Reset and Mode Select Timing Diagram

Table E-6 Background Debugging Mode Timing

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} and V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	8	—	ns
B1	DSI Input Hold Time	tDSIH	5	—	ns
B2	DSCLK Setup Time	tDSCSU	8	—	ns
B3	DSCLK Hold Time	tDSCH	5	—	ns
B4	DSO Delay Time	tDSOD	—	13	ns
B5	DSCLK Cycle Time	tDSCCYC	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	tFRZAN	—	25	ns
B7	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	tIFZ	—	25	ns
B8	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	tIF	—	25	ns
B9	DSCLK Low Time	tDSCLO	1	—	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.

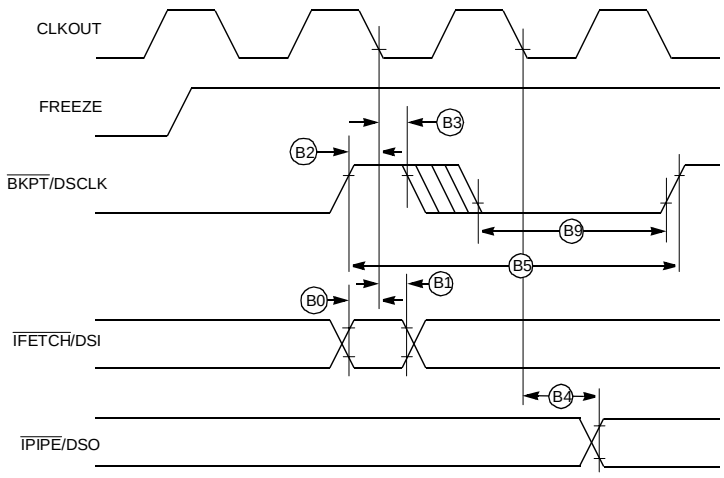


Figure E-13 Background Debugging Mode Timing — Serial Communication

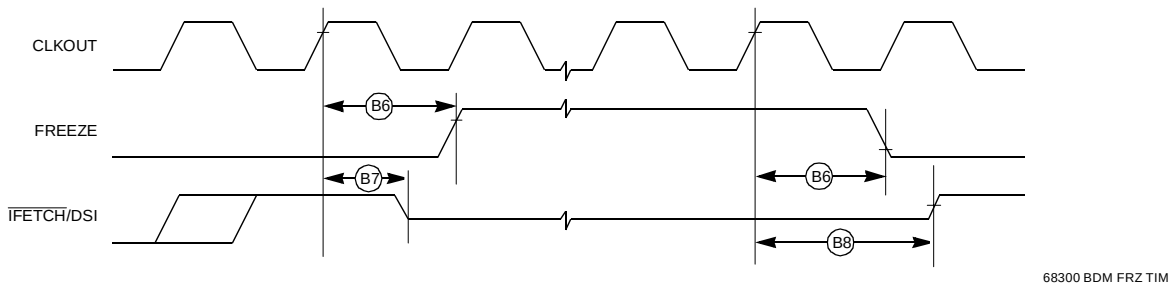


Figure E-14 Background Debugging Mode Timing — Freeze Assertion

Table E-7 ECLK Bus Timing

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDL} and V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
E1	ECLK Low to Address Valid[2]	t_{EAD}	—	60	ns
E2	ECLK Low to Address Hold	t_{EAH}	10	—	ns
E3	ECLK Low to $\overline{CS}$ Valid ($\overline{CS}$ Delay)	t_{ECSD}	—	150	ns
E4	ECLK Low to $\overline{CS}$ Hold	t_{ECSH}	15	—	ns
E5	$\overline{CS}$ Negated Width	t_{ECSN}	30	—	ns
E6	Read Data Setup Time	t_{EDSR}	30	—	ns
E7	Read Data Hold Time	t_{EDHR}	15	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	60	ns
E9	$\overline{CS}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{CS}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	5	—	ns
E13	$\overline{CS}$ Negated to Data Hold (Write)	t_{ECHW}	0	—	ns
E14	Address Access Time (Read)[3]	t_{EACC}	386	—	ns
E15	Chip-Select Access Time (Read)[4]	t_{EACS}	296	—	ns
E16	Address Setup Time	t_{EAS}		1/2	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{ECYC} - t_{EAD} - t_{EDSR}$.
4. Chip-select access time = $t_{ECYC} - t_{ECSD} - t_{EDSR}$.

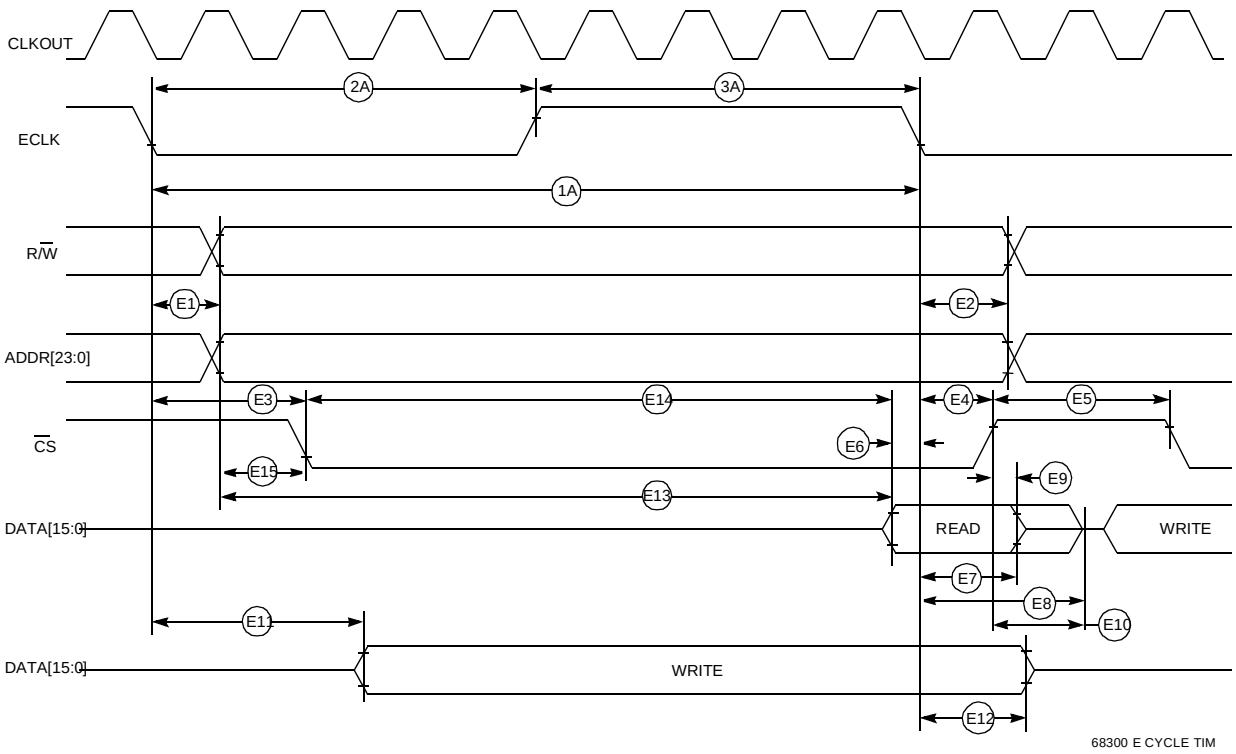


Figure E-15 ECLK Timing Diagram

E.6 QSPI Characteristics

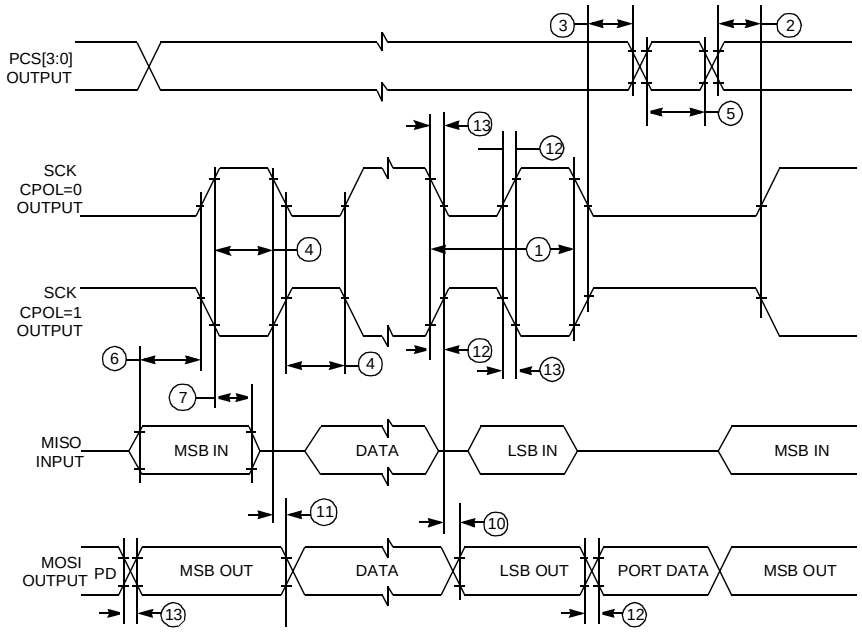
Table E-8 QSPI Timing

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H 50 pF load on all QSPI pins)[1]

Num	Function	Symbol	Min	Max	Unit
0	Operating Frequency Master Slave	f_{op}	 DC DC	 1/4 1/4	 System Clock Frequency System Clock Frequency
1	Cycle Time Master Slave	t_{qcyc}	 4 4	 510 —	 t_{cyc} t_{cyc}
2	Enable Lead Time Master Slave	t_{lead}	 2 2	 128 —	 t_{cyc} t_{cyc}
3	Enable Lag Time Master Slave	t_{lag}	 — 2	 1/2 —	 SCK t_{cyc}
4	Clock (SCK) High or Low Time Master Slave[2]	t_{sw}	 2 tcyc – 60 2 tcyc – n	 255 tcyc —	 ns ns
5	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	 17 13	 8192 —	 t_{cyc} t_{cyc}
6	Data Setup Time (Inputs) Master Slave	t_{su}	 30 20	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	t_{hi}	 0 20	 — —	 ns ns
8	Slave Access Time	t_a	—	1	t_{cyc}
9	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
10	Data Valid (after SCK Edge) Master Slave	t_v	 — —	 50 50	 ns ns
11	Data Hold Time (Outputs) Master Slave	t_{ho}	 0 0	 — —	 ns ns
12	Rise Time Input Output	 t_{ri} t_{ro}	 — —	 1 50	 µs ns
13	Fall Time Input[3] Output	 t_{fi} t_{fo}	 — —	 1 50	 µs ns

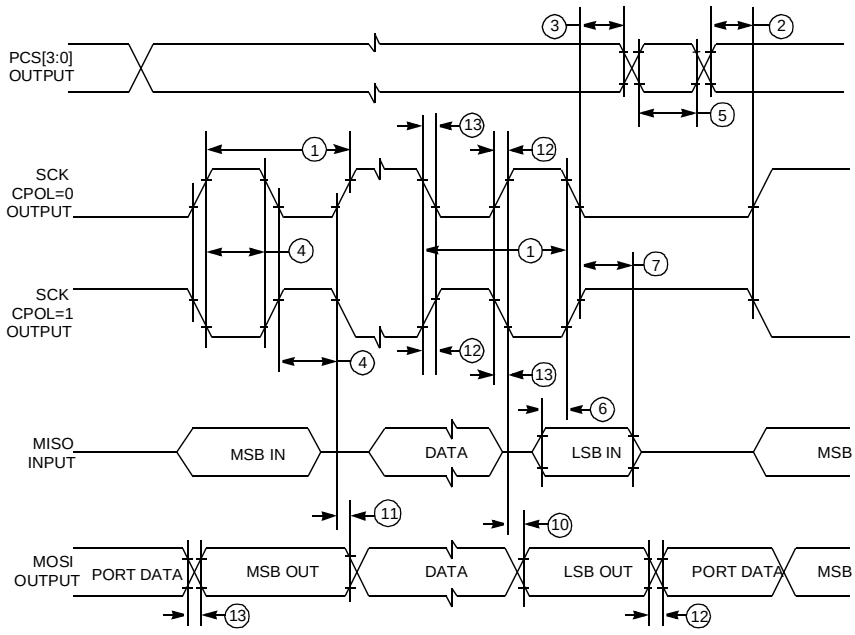
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. For high time, n = External SCK rise time; for low time, n = External SCK fall time.
3. Data can be recognized properly with longer transition times as long as MOSI/MISO signals from external sources are at valid VOH/VOL prior to SCK transitioning between valid VOL and VOH. Due to process variation, logic decision point voltages of the data and clock signals can differ, which can corrupt data if slower transition times are used.



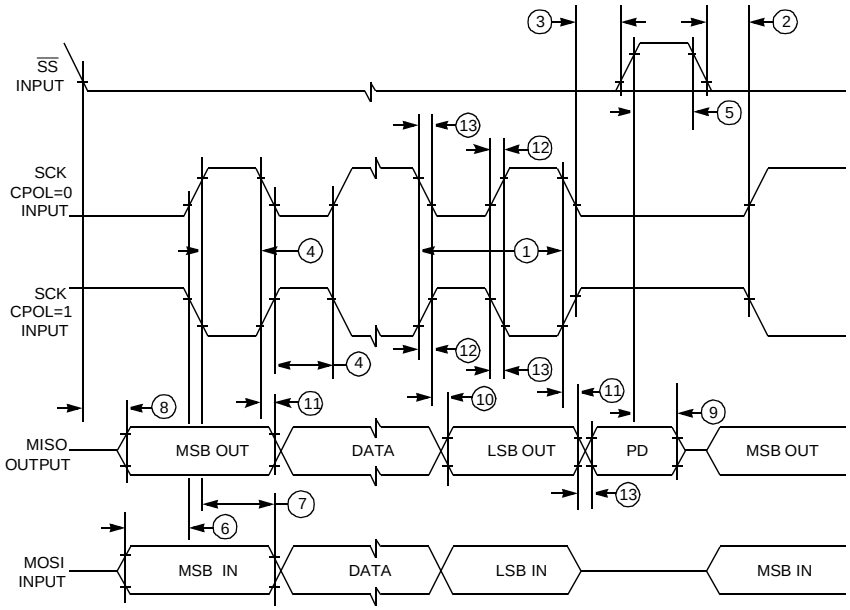
QSPI MAST CPHA0

Figure E-16 QSPI Timing — Master, CPHA = 0



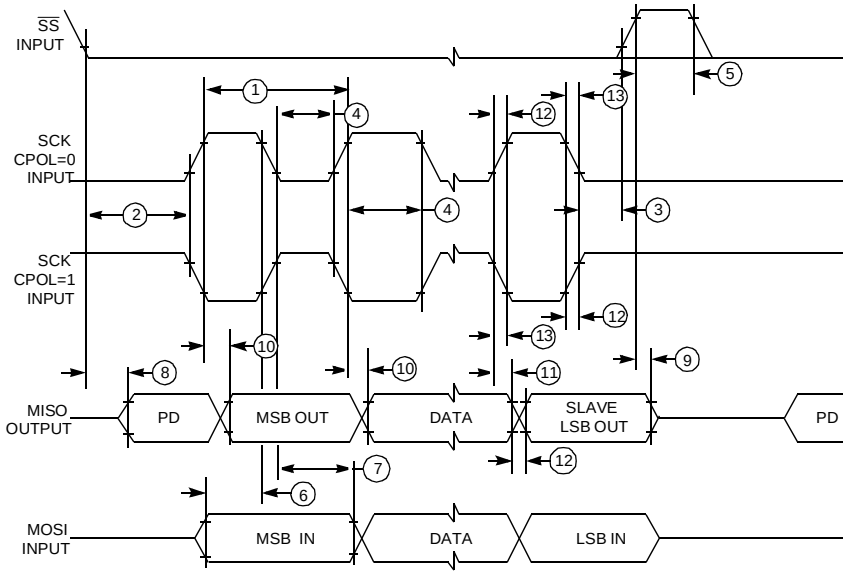
QSPI MAST CPHA1

Figure E-17 QSPI Timing — Master, CPHA = 1



QSPI SLV CPHA0

Figure E-18 QSPI Timing — Slave, CPHA = 0



QSPI SLV CPHA1

Figure E-19 QSPI Timing — Slave, CPHA = 1

E.7 TPU3 Characteristics

Table E-9 Time Processor Unit (TPU3) Timing

(V_{DDH} = 5.0 Vdc ± 10%, V_{DDSYN} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, f_{sys} = 20.97 MHz)[1, 2]

Num	Rating	Symbol	Min	Max	Unit
1	CLKOUT High to TPU3 Output Channel Valid	t_{CHTOV}	2	23	ns
2	CLKOUT High to TPU3 Output Channel Hold	t_{CHTOH}	0	20	ns
3	TPU3 Input Channel Pulse Width	t_{TIPW}	4	—	t_{cyc}

NOTES:
1. AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels.
2. Timing not valid for external T2CLK input.

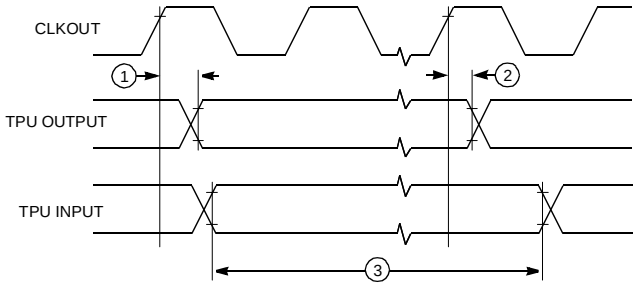


Figure E-20 TPU Timing Diagram

E.8 QADC64 and AMUX Characteristics

Table E-10 QADC64 Maximum Ratings

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply, with reference to V_{SSA}	V_{DDA}	– 0.3	6.0	V
2	Digital Supply, with reference to V_{SS}	V_{DDL}	– 0.3	4.0	V
3	Reference Supply, with reference to V_{RL}	V_{RH}	– 0.3	6.0	V
4	V_{SS} Differential Voltage	$V_{SS} - V_{SSA}$	– 0.1	0.1	V
5	V_{DD} Differential Voltage	$V_{DDL} - V_{DDA}$	– 6.0	4.0	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 0.3	6.0	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 6.0	6.0	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 0.3	0.3	V
9	Disruptive Input Current[1, 2, 3, 4, 5, 6, 7] $V_{NEGCLAMP}$ = -0.3 $V_{POSCLAMP}$ = TBD (8 – 12 V)	I_{NA}	– 500	500	µA
10	Positive Overvoltage Current Coupling Ratio[1, 5, 6, 8] PQA PQB	K_P	 2000 2000	 — —	—
11	Negative Overvoltage Current Coupling Ratio[1, 5, 6, 8] PQA PQB	K_N	 125 500	 — —	—
12	Maximum Input Current[3, 4, 6] $V_{NEGCLAMP}$ = -0.3 V $V_{POSCLAMP}$ = TBD (8 – 12 V)	I_{MA}	– 25	25	mA

NOTES:

1. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
2. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also affect the conversion accuracy of other channels.
3. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using positive and negative clamp values, then use the larger of the calculated values.
5. This parameter is periodically sampled rather 100% tested.
6. Condition applies to one pin at a time.
7. Determination of actual maximum disruptive input current, which can affect operation, is related to external system component values.
8. Current coupling is the ratio of the current induced from overvoltage (positive or negative, through an external series coupling resistor), divided by the current induced on adjacent pins. A voltage drop may occur across the external source impedances of the adjacent pins, impacting conversions on these adjacent pins.

Table E-11 QADC64 DC Electrical Characteristics (Operating)

(V_{SS} and V_{SSA} = 0 Vdc, F_{QCLK} = 2.1 MHz, T_A within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Digital Supply[1]	V_{DD}	3.0	3.6	V
3	V_{SS} Differential Voltage	$V_{SS} - V_{SSA}$	– 100	100	mV
4	V_{DD} Differential Voltage	$V_{DD} - V_{DDA}$	– 1.0	1.0	V
5	Reference Voltage Low[2]	V_{RL}	V_{SSA}	V_{SSA} +0.1	V
6	Reference Voltage High[2]	V_{RH}	V_{DDA} - 0.1	V_{DDA}	V
7	V_{REF} Differential Voltage[3]	V_{RH} - V_{RL}	4.5	5.5	V
8	Mid-Analog Supply Voltage	V_{DDA} / 2	2.25	2.75	V
9	Input Voltage	V_{INDC}	V_{SSA}-0.3	V_{DDA}+0.3	V
10	Input High Voltage, PQA and PQB	V_{IH}	0.7 (V_{DDA})	V_{DDA} + 0.3	V
11	Input Low Voltage, PQA and PQB	V_{IL}	V_{SSA} – 0.3	0.4(V_{DDA})	V
12	Input Hysteresis[4]	V_{HYS}	0.5	—	V
13	Output Low Voltage, PQA[5] IOL = 5.0 mA IOL = 10.0 µA	V_{OL}	 — —	 0.4 0.2	V
14	Analog Supply Current Normal Operation[6] Low-Power Stop	I_{DDA}	 — —	 15.0 10.0	 mA µA
15	Reference Supply Current	I_{REF}	—	250	µA
16	Load Capacitance, PQA	C_L	—	50	pF
17	Input Current, Channel Off[7] PQA PQB	I_{OFF}	 — —	 200 150	nA
18	Total Input Capacitance[8] PQA Not Sampling PQA Sampling PQB Not Sampling PQB Sampling	C_{IN}	 — — — —	 15 20 10 15	pF

NOTES:

1. Refers to operation over full temperature and frequency range.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Accuracy tested and guaranteed at V_{RH} - V_{RL} = 5.0V ± 10%.
4. Parameter applies to the following pins:
   Port A: PQA[7:0]/AN[59:58]/ETRIG[2:1]
   Port B: PQB[7:0]/AN[3:0]/AN[51:48]/AN[Z:W]
5. Open drain only.
6. Current measured at maximum system clock frequency with QADC64 active.
7. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10° C decrease from maximum temperature.
8. This parameter is periodically sampled rather than 100% tested.

Table E-12 QADC64 AC Electrical Characteristics (Operating)

(V_{DDL} = 3.3 Vdc ± 10%, V_{DDH} and V_{DDA} = 5.0 Vdc ± 10%, V_{SS} and V_{SSA} = 0Vdc, T_A within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	QADC64 Clock (QCLK) Frequency[1]	F_{QCLK}	0.5	2.1	MHz
2	QADC64 Clock Duty Cycle[2, 3] High Phase Time ($T_{PSL} \leq T_{PSH}$)	T_{PSH}	500	—	ns
3	Conversion Cycles[4]	CC	20	32	QCLK cycles
4	Conversion Time[4, 4, 5] F_{QCLK} = 0.987 MHz[6] Min = CCW/IST =%00 Max = CCW/IST =%11 F_{QCLK} = 2.098 MHz[1, 7] Min = CCW/IST =%00 Max = CCW/IST =%11	T_{CONV}	 18.0 8.58	 32 15.24	 µs
5	Stop Mode Recovery Time	T_{SR}	—	10	µs

NOTES:

1. Conversion characteristics vary with F_{QCLK} rate. Reduced conversion accuracy occurs at max F_{QCLK} rate.
2. Duty cycle must be as close as possible to 75% to achieve optimum performance.
3. Minimum applies to 1.0 MHz operation.
4. Assumes that short input sample time has been selected (IST = 0).
5. Assumes that f_{sys} = 16.78 MHz.
6. Assumes F_{QCLK} = 0.987 MHz, with clock prescaler values of:
   QACR0: PSH =%01100, PSA =%0, PSL = %011
   CCW: BYP =%0
7. Assumes F_{QCLK} = 2.098 MHz, with clock prescaler values of:
   QACR0: PSH =%00101, PSA =%0, PSL = %001
   CCW: BYP =%0

Table E-13 QADC64 Conversion Characteristics (Operating)

(V_{DDL}= 3.3 Vdc ± ± 10%, V_{DDH}, V_{DDA} = 5.0 Vdc ± 10%, V_{SS} and V_{SSA} = 0 Vdc, T_A within operating temperature range0.5 MHz ≤ F_{QCLK} ≤ 2.1 MHz, 2 clock input sample time)

Num	Parameter	Symbol	Min	Typ	Max	Unit
1	Resolution[1]	1 Count	—	5	—	mV
3	Integral nonlinearity	INL	—	—	±2.0	Counts
4	Absolute error[2,3,4] F_{QCLK} = 0.987MHz[5] PQA PQB F_{QCLK} = 2.098 MHz[6] PQA PQB	AE	 — — — —	 — — — —	 ±2.5 ±2.5 ±4.0 ±4.0	Counts
5	Source impedance at input[7]	R_S	—	100	—	KΩ

NOTES:

1. At V_{RH} - V_{RL} = 5.12 V, one count = 5 mV.
2. This parameter is periodically sampled rather that 100% tested.
3. Absolute error includes 1/2 count (2.5mV) of inherent quantization error and circuit (differential, integral, and offset) error. Specification assumes that adequate low-pass filtering is present on analog input pins — capacitive filter with 0.01µF to 0.1 µF capacitor between analog input and analog ground, typical source isolation impedance of 20 KΩ.
4. Assumes f_{sys} = 16.78 MHz.
5. Assumes clock prescaler values of:
   QACR0: PSH =%01100, PSA =%0, PSL = %011
   CCW: BYP =%0
6. Assumes clock prescaler values of:
   QACR0: PSH =%00101, PSA =%0, PSL = %001
   CCW: BYP =%0
7. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{errj}):

   $$V_{errj} = R_S \times I_{OF}$$

   where IOFF is a function of operating temperature. (See **Table E-11, note 7**).
   Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the decoupling capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance.

Table E-14 AMUX_HV Absolute Maximum Ratings

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply, with reference to V_{SSA}	V_{DDA}	– 0.3	6.0	V
2	Internal Digital Supply[1], with reference to V_{SSI}	V_{DDI}	– 0.3	4.0	V
3	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 0.1	0.1	V
4	V_{DD} Differential Voltage[2]	$V_{DDI} - V_{DDA}$	– 6.0	4.0	V
5	Maximum Input Current[3,4,5]	I_{MA}	– 25	25	mA

NOTES:

1. For internal digital supply of V_{DDI} = 3.3 V typical.
2. Refers to allowed random sequencing of power supplies.
3. Transitions within the limit do not affect device reliability or cause permanent damage. Exceeding limit may cause permanent conversion error on stressed channels and on unstressed channels.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.3$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.
5. Condition applies to one pin at a time.

Table E-15 AMUX_HV DC Electrical Characteristics (Operating)

(V_{SSI} and V_{SSA} = 0 Vdc, F_{QCLK} = 2.0 MHz, T_A within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Internal Digital Supply[1]	V_{DDI}	3.0	3.6	V
3	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 100	100	mV
4	Input Voltage	V_{INDC}	V_{SSA}	V_{DDA}	V
5	Analog Supply Current[2]	I_{DDA}	—	10	µA
6	Input Current, Channel Off[3]	I_{OFF}	– 200nA	200	nA
7	Total Input Capacitance[4] ANXx Not Sampling ANXx Sampling[5]	C_{IN}	— —	15 20	pF
8	Disruptive Input Injection Current[6]	I_{INJ}	– 3	+3	mA

NOTES:

1. Refers to operation over full temperature and frequency range.
2. VDDA is used only for a pin stress protection circuit. It draws DC current only when the pin voltage is above VDDA. It draws a minimal capacitive switching current when the channel is changed.
3. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10° C decrease from maximum temperature.
4. This parameter is periodically sampled rather than 100% tested.
5. Sampling adds an incremental capacitance of roughly 5pF.
6. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

Table E-16 AMUX_HV Conversion Characteristics (Operating)

(V_{DDI} = 3.3 Vdc ± 0.3 V, V_{DDA} = 5.0 Vdc ± 10%, V_{SSI} and V_{SSA} = 0 Vdc, T_A within operating temperature range, 0.5 MHz ≤ F_{QCLK} ≤ 2.1 MHz, 4[1] clock input sample time, AMUX/QADC64 configured for internal multiplexing only.)

Num	Parameter	Symbol	Min	Typ	Max	Unit
1	Source impedance at input[2,3]	R_S	—	7.5	—	KΩ

NOTES:

1. Input sample time was increased from the 2 clocks used on channels connected directly to the QADC64 (AN0–AN4, AN48–AN59) to 4 on extended channels (ANX0–ANX31). This is to compensate for additional series resistance of the AMUX. It is possible that this can change back to 2 after characterization.
2. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.
   Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{errj}):
   $$V_{errj} = R_S * I_{OFF}$$
   where I_{OFF} is a function of operating temperature. (See **Table E-15**, Note **3.**).
   Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the filtering capacitor used. Error levels are best determined empirically. Charge-sharing leakage for AMUX inputs will be larger due to the increased internal parasitic capacitances. In general, continuous conversion of the same channel may not be compatible with high source impedance.
3. AMUX/QADC64 configured for internal multiplexing only.

E.9 CTM9 Electrical Characteristics

The electrical and timing characteristics of the CTM9 are the same as those of other MC68300/MC68HC16 family MCUs.

E.9.1 5 V, 16.78 MHz Operating Conditions

Table E-17 CTM9 5 V, 16.78 MHz Operating Conditions

	Condition	Symbol	Min	Typ	Max	Units
Operating Temperature		Temp	-40		+125	°C
Main Supply Voltage		V_{DD}	4.50	5.00	5.50	V
Operating Frequency	Main Clock	F_{clk}	0		16.78	MHz

E.9.2 5 V, 25.0 MHz Operating Conditions

Table E-18 CTM9 5 V, 25 MHz Operating Conditions

	Condition	Symbol	Min	Typ	Max	Units
Operating Temperature		Temp	-40		+125	°C
Main Supply Voltage		V_{DD}	4.50	5.00	5.50	V
Operating Frequency	Main Clock	F_{clk}	0		25.0	MHz

Table E-19 FCSM Timing Characteristics

(V_{DDL} = 3.3 Vdc ± 10%, V_{DDH} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin frequency[1]	f_{PCNTR}	0	$f_{sys}/4$	MHz
2	Input pin low time[1]	t_{PINL}	$2.0/f_{sys}$	—	µs
3	Input pin high time[1]	t_{PINH}	$2.0/f_{sys}$	—	µs
4	Clock pin to counter increment	t_{PINC}	$4.5/f_{sys}$	$6.5/f_{sys}$	µs
5	Clock pin to new TBB value	t_{PTBB}	$5.0/f_{sys}$	$7.0/f_{sys}$	µs
6	Clock pin to COF set ($FFFF)	t_{PCOF}	$4.5/f_{sys}$	$6.5/f_{sys}$	µs
7	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
8	Flag to IMB interrupt request	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs
9	Counter resolution[2]	t_{CRES}	—	$2.0/f_{sys}$	µs

NOTES:

1. Value applies when using external clock.
2. Value applies when using internal clock. Minimum counter resolution depends on prescaler divide ratio selection.

Table E-20 MCSM Timing Characteristics

(V_{DDL} = 3.3 Vdc ± 10%, V_{DDH} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin frequency[1]	f_{PCNTR}	0	$f_{sys}/4$	MHz
2	Input pin low time[1]	t_{PINL}	$2.0/f_{sys}$	—	µs
3	Input pin high time[1]	t_{PINH}	$2.0/f_{sys}$	—	µs
4	Clock pin to counter increment	t_{PINC}	$4.5/f_{sys}$	$6.5/f_{sys}$	µs
5	Clock pin to new TBB value	t_{PTBB}	$5.0/f_{sys}$	$7.0/f_{sys}$	µs
6	Clock pin to COF set ($FFFF)	t_{PCOF}	$4.5/f_{sys}$	$6.5/f_{sys}$	µs
7	Load pin to new counter value	t_{PLOAD}	$2.5/f_{sys}$	$3.5/f_{sys}$	µs
8	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
9	Flag to IMB interrupt request	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs
10	Counter resolution[2]	t_{CRES}	—	$2.0/f_{sys}$	µs

NOTES:

1. Value applies when using external clock.
2. Value applies when using internal clock. Minimum counter resolution depends on prescaler divide ratio selection.

Table E-21 SASM Timing Characteristics

(V_{DDL} = 3.3 Vdc ± 10%, V_{DDH} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	t_{PINL}	$2.0/f_{sys}$	—	µs
2	Input pin high time	t_{PINH}	$2.0/f_{sys}$	—	µs
3	Input capture resolution[1]	t_{RESCA}	—	$2.0/f_{sys}$	µs
4	Pin to input capture delay	t_{PCAPT}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
5	Pin to FLAG set	t_{PFLAG}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
6	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
7	OCT output pulse	t_{OCT}	$2.0/f_{sys}$	—	µs
8	Compare resolution[1]	t_{RESCM}		$2.0/f_{sys}$	µs
9	TBB change to FLAG set	t_{CFLAG}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
10	TBB change to pin change[2]	t_{CPIN}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
11	Flag to IMB interrupt request[2]	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs

NOTES:
1. Minimum resolution depends on counter and prescaler divide ratio selection.
2. Time given from when new value is stable on time base bus.

Table E-22 DASM Timing Characteristics

(V_{DDL} = 3.3 Vdc ± 10%, V_{DDH} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	t_{PINL}	$2.0/f_{sys}$	—	µs
2	Input pin high time	t_{PINH}	$2.0/f_{sys}$	—	µs
3	Input capture resolution[1]	t_{RESCA}	—	$2.0/f_{sys}$	µs
4	Pin to input capture delay	t_{PCAPT}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
5	Pin to FLAG set	t_{PFLAG}	$2.5/f_{sys}$	$4.5/f_{sys}$	µs
6	Pin to IN bit delay	t_{PINB}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs
7	OCT output pulse	t_{OCT}	$2.0/f_{sys}$	—	µs
8	Compare resolution[1]	t_{RESCM}	—	$2.0/f_{sys}$	µs
9	TBB change to FLAG set	t_{CFLAG}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
10	TBB change to pin change[2]	t_{CPIN}	$1.5/f_{sys}$	$1.5/f_{sys}$	µs
11	Flag to IMB interrupt request[2]	t_{FIRQ}	$1.0/f_{sys}$	$1.0/f_{sys}$	µs

NOTES:
1. Minimum resolution depends on counter and prescaler divide ratio selection.
2. Time given from when new value is stable on time base bus.

Table E-23 PWMSM Timing Characteristics

(V_{DDL} = 3.3 Vdc ± 10%, V_{DDH} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	PWMSM output resolution[1]	t_{PWMR}	—	—	µs
2	PWMSM output pulse[2]	t_{PWMO}	$2.0/f_{sys}$	—	µs
3	PWMSM output pulse[3]	t_{PWMO}	$2.0/f_{sys}$	$2.0/f_{sys}$	µs
4	CPSM enable to output set PWMSM enabled before CPSM, DIV23 = 0 PWMSM enabled before CPSM, DIV23 = 1	t_{PWMP}	 $3.5/f_{sys}$ $6.5/f_{sys}$	—	µs
5	PWM enable to output set PWMSM enabled before CPSM, DIV23 = 0 PWMSM enabled before CPSM, DIV23 = 1	t_{PWME}	 $3.5/f_{sys}$ $5.5/f_{sys}$	 $4.5/f_{sys}$ $6.5/f_{sys}$	µs
6	FLAG to IMB interrupt request	t_{FIRQ}	$1.5/f_{sys}$	$2.5/f_{sys}$	µs

NOTES:
1. Minimum output resolution depends on counter and prescaler divide ratio selection.
2. Excluding the case where the output is always zero.
3. Excluding the case where the output is always zero.

E.10 TouCAN Characteristics

Table E-24 TouCAN AC Characteristics[1]

Num	Parameter	Symbol	Value	Unit
1	CNTX0 – Delay from ICLOCK	—	19	ns
2	CNRX0 – Set-up to rise ICLOCK	—	0	ns
3	TOUCAN serial (Tx, Rx pins) max frequency	—	1	MHz

NOTES:
1. Measured at: 4.5V, 150°C

E.11 CMFI FLASH Characteristics

Table E-25 CMFI Program and Erase Characteristics

(VDDF = 3.3V ± 0.3V, VPP= 4.75V to 5.25V, TA = T_L to T_H)[1]

Symbol	Meaning	Value			Units
		Minimum	Typical	Maximum	
E_{PULSE}	Number of erase pulses	8	8	27	Pulses
T_{ERASE}	Erase pulse time	98	100	102	mS
P_{PULSE}	Number of program pulses	—	800	48000[2]	Pulses
T_{PROG}	Program pulse time	48	50	256.5	µS

NOTES:
1. T_L is defined to be -40 °C and T_H is defined to be 125 °C.
2. The worse case condition for programming time is at T_A = -40 °C and VPP = 4.75 volts.

Table E-26 CMFI AC and DC Power Supply Characteristics

Symbol	Meaning	Value
V_{DDF}=V_{DDL}	Operating voltage Read, Program or Erase	3.0 V to 3.6 V
I_{DDF}	Operating current at 40.0MHz, V_{DDF} = 3.3V for a 256K-byte Read, Program or Erase operation Disabled	 50 mA maximum 5 mA maximum
V_{PP}	External Program or Erase voltage Read Program or Erase	 (V_{DDF} - 350 m V) to 5.5 V 5.0 V ± 5%
I_{PP}	External Program and Erase current Read, V_{PP} = 5V Program, V_{PP} = 5V Erase, V_{PP} = 5V	 <100 µA 30 mA maximum 30 mA maximum

Table E-27 CMFI FLASH EEPROM Module Life

Symbol	Meaning	Value
P/E Cycles[1]	Maximum number of Program/ Erase cycles[2] before failure.	100[3,4]
Retention	Data retention at average operating temperature of 85 °C.	10 years

1) A Program/Erase cycle is defined as switching the bits from 1→ 0 →1.
2) Reprogramming of a CMFI array block prior to erase is not required.
3) Number of Program/Erase cycles to be adjusted pending characterization of production silicon.
4) Target failure rate at specified number of program/erase cycles of 2ppm pending characterization of production silicon.

E.11.1 EPEB0 Pin Timing

The EPEB0 pin uses a two-period clock synchronizer that switches the signal CMF_EPEE after two consecutive values of EPEB0 as shown in **Figure E-21**. At first the value of CMF_EPEE is unknown as the prior information for the EPEB0 pin is not provided. After two clocks with EPEB0 low the signal CMF_EPEE is low. One high or low clock of EPEB0 will not cause CMF_EPEE to switch. After two high or low clocks of EPEB0 CMF_EPEE will switch to the value of EPEB0.

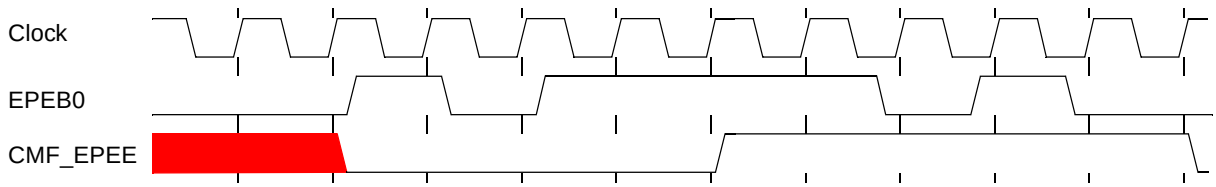


Figure E-21 EPEB0 Pin Timing

E.11.2 FLASH Program/Erase Voltage Conditioning

A voltage of at least V_{DDL} -0.35 V must be applied at all times to the V_{PP} pins or damage to the FLASH module can occur. FLASH modules can be damaged by power on and power off V_{PP} transients. V_{PP} must not rise to programming level while V_{DDL} is below the specified minimum value, and must not fall below the minimum specified value while V_{DDL} is applied. shows the V_{PP} and V_{DDL} operating envelope.

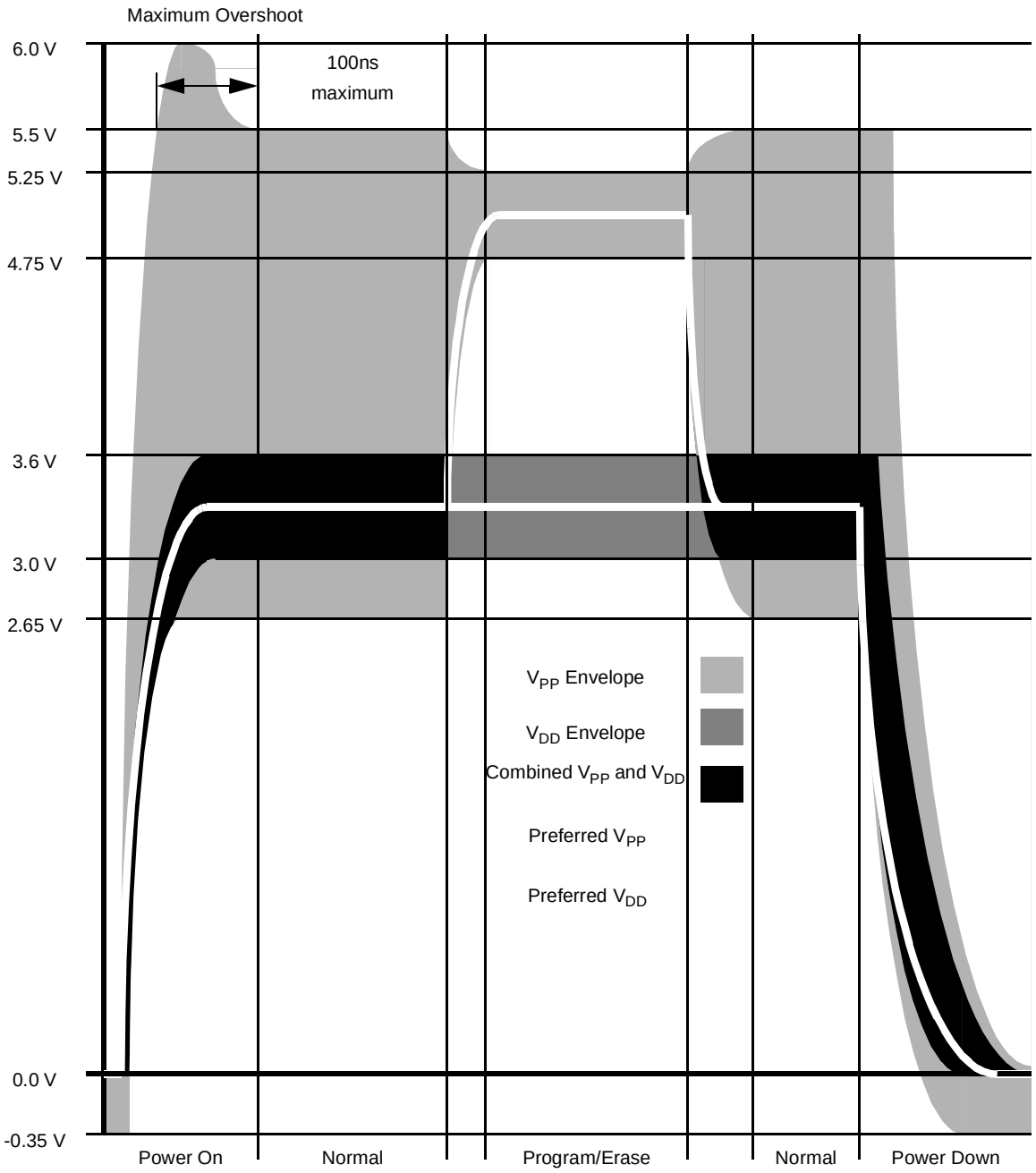


Figure E-22 V_{PP} and V_{DD} Power Sequencing

Use of an external circuit to condition V_{PP} is recommended. **Figure E-23** shows a simple circuit that maintains required voltages and filters transients. V_{PP} is pulled up to V_{DDL} via Schottky diode D2, protecting V_{DDL} from excessive reverse current. D2 also protects the FLASH from damage should the programming voltage go to zero. Programming power supply voltage must be adjusted to compensate for the forward-bias drop across D1. R1 provides a discharge bleed path for C1. Allow for RC charge and discharge time constants when applying and removing power. When using this circuit,

keep leakage from external devices connected to the VPP pin low, to minimize diode voltage drop.

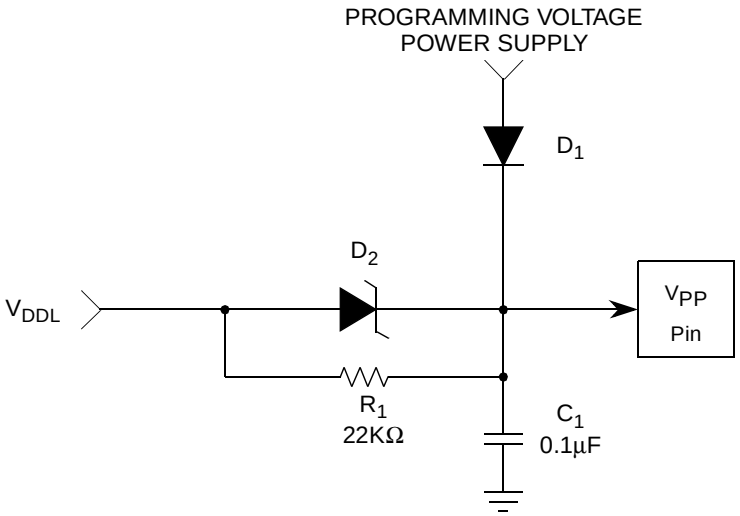


Figure E-23 A Recommended External V_{PP} Pin Conditioning Circuit

E.12 ROM Electrical Specifications

Table E-28 IMB3 ROM AC/DC Characteristics

Normal Operating Specifications		
V_{DDL}	Operating Voltage	+3.3V +/- 0.3V
f_{max}	Maximum Operating Frequency	33 MHz
T	Operating Temperature range	-40° to +125 °C