SECTION 5
TIME PROCESSOR UNIT 3

There are two time processor unit 3's (TPU3). This enhanced version of the original TPU is an intelligent, semi-autonomous microcontroller designed for timing control. The TPU3 is fully compatible to the TPU2. Operating simultaneously with the CPU, the TPU3 modules process micro-instructions, schedules and processes real-time hardware events, performs input and output, and accesses shared data without CPU intervention. Consequently, for each timer event, the CPU setup and service times are minimized or eliminated. **Figure 5-1** is a simplified block diagram of the TPU3.

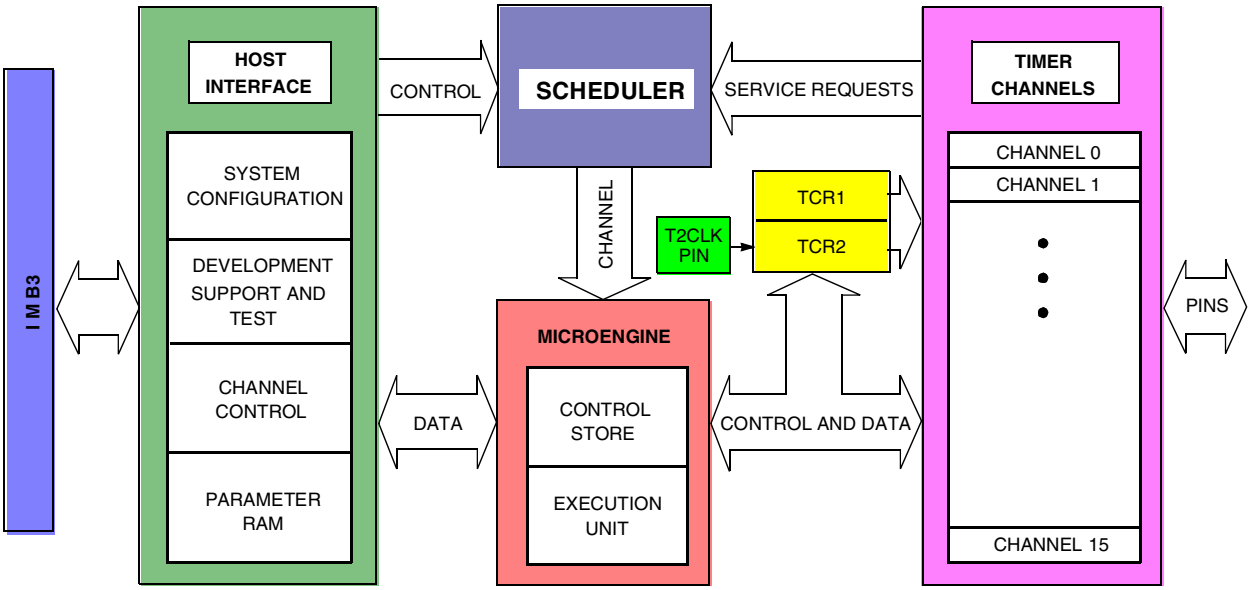

Figure 5-1 TPU3 Block Diagram

5.1 Overview

The TPU3 can be viewed as a special-purpose microcomputer that performs a programmable series of two operations, match and capture. Each occurrence of either operation is called an event. A programmed series of events is called a function. TPU functions replace software functions that would require CPU interrupt service.

The microcode ROM TPU3 functions that are available in the MC68377 are described in **APPENDIX D TPU ROM FUNCTIONS**.

5.2 TPU3 Components

Each TPU3 consists of two 16-bit time bases, 16 independent timer channels, a task scheduler, a microengine, and a host interface. In addition, a dual-ported parameter RAM is used to pass parameters between the module and the CPU.

5.2.1 Time Bases

Two 16-bit counters provide reference time bases for all output compare and input capture events. Prescalers for both time bases are controlled by the CPU via bit fields in the TPU3 module configuration register (TPUMCR) and TPU module configuration register two (TPUMCR2). Timer count registers TCR1 and TCR2 provide access to the current counter values. TCR1 and TCR2 can be read by TPU microcode but are not directly available to the CPU. The TCR1 clock is always derived from the system clock. The TCR2 clock can be derived from the system clock or from an external input via the T2CLK clock pin. The duration between active edges on the T2CLK clock pin must be at least nine system clocks.

5.2.2 Timer Channels

The TPU3s have 16 independent channels, each connected to an MCU pin. The channels have identical hardware and are functionally equivalent in operation. Each channel consists of an event register and pin control logic. The event register contains a 16-bit capture register, a 16-bit compare/match register, and a 16-bit greater-than-or-equal-to comparator. The direction of each pin, either output or input, is determined by the TPU microengine. Each channel can either use the same time base for match and capture, or can use one time base for match and the other for capture.

5.2.3 Scheduler

When a service request is received, the scheduler determines which TPU3 channel is serviced by the microengine. A channel can request service for one of four reasons: for host service, for a link to another channel, for a match event, or for a capture event. The host system assigns each active channel one of three priorities: high, middle, or low. When multiple service requests are received simultaneously, a priority-scheduling mechanism grants service based on channel number and assigned priority.

5.2.4 Microengine

The microengine is composed of a control store and an execution unit. Control-store ROM holds the microcode for each factory-masked time function. When assigned to a channel by the scheduler, the execution unit executes microcode for a function assigned to that channel by the CPU. Microcode can also be executed from the dual-port RAM (DPTRAM) module instead of the control store. The DPTRAM allows emulation and development of custom TPU microcode without the generation of a microcode ROM mask. Refer to **5.3.6 Emulation Support** for more information.

5.2.5 Host Interface

The host interface registers allow communication between the CPU and the TPU3, both before and during execution of a time function. The registers are accessible from the IMB through the TPU3 bus interface unit. Refer to **5.4 Programming Model** for register bit/field definitions and address mapping.

5.2.6 Parameter RAM

Parameter RAM occupies 256 bytes at the top of the system address map. Channel parameters are organized as 128 16-bit words. Channels zero through 15 each have eight parameters. The parameter RAM address map in **5.4.13 TPU3 Parameter RAM** shows how parameter words are organized in memory.

The CPU specifies function parameters by writing to the appropriate RAM address. The TPU3 reads the RAM to determine channel operation. The TPU3 can also store information to be read by the CPU in the parameter RAM. Detailed descriptions of the parameters required by each time function are beyond the scope of this manual. Refer to Motorola's ***TPU Literature Package*, TPULITPAK/D,** for the available TPU documentation.

5.3 TPU Operation

All TPU3 functions are related to one of the two 16-bit time bases. Functions are synthesized by combining sequences of match events and capture events. Because the primitives are implemented in hardware, the TPU3 can determine precisely when a match or capture event occurs, and respond rapidly. An event register for each channel provides for simultaneous match/capture event occurrences on all channels.

When a match or input capture event requiring service occurs, the affected channel generates a service request to the scheduler. The scheduler determines the priority of the request and assigns the channel to the microengine at the first available time. The microengine performs the function defined by the content of the control store or emulation RAM, using parameters from the parameter RAM.

5.3.1 Event Timing

Match and capture events are handled by independent channel hardware. This provides an event accuracy of one time-base clock period, regardless of the number of channels that are active. An event normally causes a channel to request service. The time needed to respond to and service an event is determined by which channels and the number of channels requesting service, the relative priorities of the channels requesting service, and the microcode execution time of the active functions. Worst-case event service time (latency) determines TPU3 performance in a given application. Latency can be closely estimated. Refer to Motorola's ***TPU Literature Package*, TPULITPAK/D,** for the available TPU documentation.

5.3.2 Channel Orthogonality

Most timer systems are limited by the fixed number of functions assigned to each pin. All TPU3 channels contain identical hardware and are functionally equivalent in oper-

ation, so that any channel can be configured to perform any time function. The user controls the combination of time functions.

5.3.3 Interchannel Communication

The autonomy of the TPU3 is enhanced by the ability of a channel to affect the operation of one or more other channels without CPU intervention. Interchannel communication can be accomplished by issuing a link service request to another channel, by controlling another channel directly, or by accessing the parameter RAM of another channel.

5.3.4 Programmable Channel Service Priority

The TPU3 provides a programmable service priority level to each channel. Three priority levels are available. When more than one channel of a given priority requests service at the same time, arbitration is accomplished according to channel number. To prevent a single high-priority channel from permanently blocking other functions, other service requests of the same priority are performed in channel order after the lowest-numbered, highest-priority channel is serviced.

5.3.5 Coherency

For data to be coherent, all available portions of the data must be identical in age, or must be logically related. As an example, consider a 32-bit counter value that is read and written as two 16-bit words. The 32-bit value is read-coherent only if both 16-bit portions are updated at the same time, and write-coherent only if both portions take effect at the same time. Parameter RAM hardware supports coherent access of two adjacent 16-bit parameters. The host CPU must use a long-word operation to guarantee coherency.

5.3.6 Emulation Support

Although factory-programmed time functions can perform a wide variety of control tasks, they may not be ideal for all applications. The TPU3 provides emulation capability that allows the user to develop new time functions. Emulation mode is entered by setting the EMU bit in TPUMCR. In emulation mode, an auxiliary bus connection is made between the DPTRAM and the TPU3, and access to DPTRAM via the intermodule bus is disabled. A 9-bit address bus, a 32-bit data bus, and control lines transfer information between the modules. To ensure exact emulation, DPTFLASH module access timing remains consistent with access timing of the TPU microcode ROM control store.

To support changing TPU application requirements, Motorola has established a TPU function library. The function library is a collection of TPU functions written for easy assembly in combination with each other or with custom functions. Refer to Motorola's ***TPU Literature Package*, TPULITPAK/D,** for the available TPU documentation.

5.3.7 TPU3 Interrupts

Each of the TPU channels can generate an interrupt service request. Interrupts for each channel must be enabled by writing to the appropriate control bit in the channel interrupt enable register (CIER). The channel interrupt status register (CISR) contains one interrupt status flag per channel. Time functions set the flags. Setting a flag bit causes the TPU to make an interrupt service request if the corresponding channel interrupt enable bit is set and the interrupt request level is non-zero.

The value of the channel interrupt request level (CIRL) field in the TPU interrupt configuration register (TICR) determines the priority of all TPU interrupt service requests. CIRL values correspond to MCU interrupt request signals IRQ[7:1]. IRQ7 is the highest-priority request signal; IRQ1 has the lowest priority. Assigning a value of 0b111 to CIRL causes IRQ7 to be asserted when a TPU interrupt request is made; lower field values cause corresponding lower-priority interrupt request signals to be asserted. Assigning CIRL a value of 0b000 disables all interrupts.

The CPU32 recognizes only interrupt requests of a priority greater than the value contained in the interrupt priority (IP) mask in the CPU status register. When the CPU32 acknowledges an interrupt request, the priority of the acknowledged interrupt is written to the IP mask and is driven out onto the IMB address lines.

When the IP mask value driven out on the address lines is the same as the CIRL value, the TPU contends for arbitration priority. The IARB field in TPUMCR contains the TPU arbitration number. Each module that can make an interrupt service request must be assigned a unique non-zero IARB value in order to implement an arbitration scheme. Arbitration is performed by means of serial assertion of IARB field bit values. The IARB of TPUMCR is initialized to 0x0 during reset.

When the TPU wins arbitration, it must respond to the CPU32 interrupt acknowledge cycle by placing an interrupt vector number on the data bus. The vector number is used to calculate displacement into the exception vector table. Vectors are formed by concatenating the 4-bit value of the CIBV field in TICR with the 4-bit number of the channel requesting interrupt service. Since the CIBV field has a reset value of 0x0, it must be assigned a value corresponding to the upper nibble of a block of 16 user-defined vector numbers before TPU interrupts are enabled. Otherwise, a TPU interrupt service request could cause the CPU32 to take one of the reserved vectors in the exception vector table.

5.3.8 Prescaler Control for TCR1

Timer count register 1 (TCR1) is clocked from the output of a prescaler. The following fields control TCR1:

- The PSCK and TCR1P fields in TPUMCR
- The DIV2 field in TPUMCR2
- The EPSCKE and EPSCK fields in TPUMCR3.

The rate at which TCR1 is incremented is determined as follows:

- The user selects either the standard prescaler (by clearing the enhanced prescaler enable bit, EPSCKE, in TPUMCR3) or the enhanced prescaler (by setting EPSCKE).
  - — If the standard prescaler is selected (EPSCKE = 0), the the PSCK bit determines whether the standard prescaler divides the system clock input by 32 (PSCK = 0) or four (PSCK = 1)
  - — If the enhanced prescaler is selected (EPSCKE = 1), the EPSCK bits select a value by which the system clock is divided. The lowest frequency for TCR1 clock is system clock divided by 64x8. The highest frequency for TCR1 clock is system clock divided by two (2 x 1). See **Table 5-1**.

Table 5-1 Enhanced TCR1 Prescaler Divide Values

EPSCK Value	Divide System Clock By
0x00	2
0x01	4
0x02	6
0x03	8
0x04, 0x05,...0x1d	10,12,...60
0x1e	62
0x1f	64

  - — The output of either the standard prescaler or the enhanced prescaler is then divided by 1, 2, 4, or 8, depending on the value of the TCR1P field in the TPUMCR.

Table 5-2 TCR1 Prescaler Values

TCR1P Value	Divide by
0b00	1
0b01	2
0b10	4
0b11	8

  - — If the DIV2 bit is one, the TCR1 counter increments at a rate of the internal clock divided by two. If DIV2 is zero, the TCR1 increment rate is defined by the output of the TCR1 prescaler (which, in turn, takes as input the output of either the standard or enhanced prescaler).

Figure 5-2 shows a diagram of the TCR1 prescaler control block.

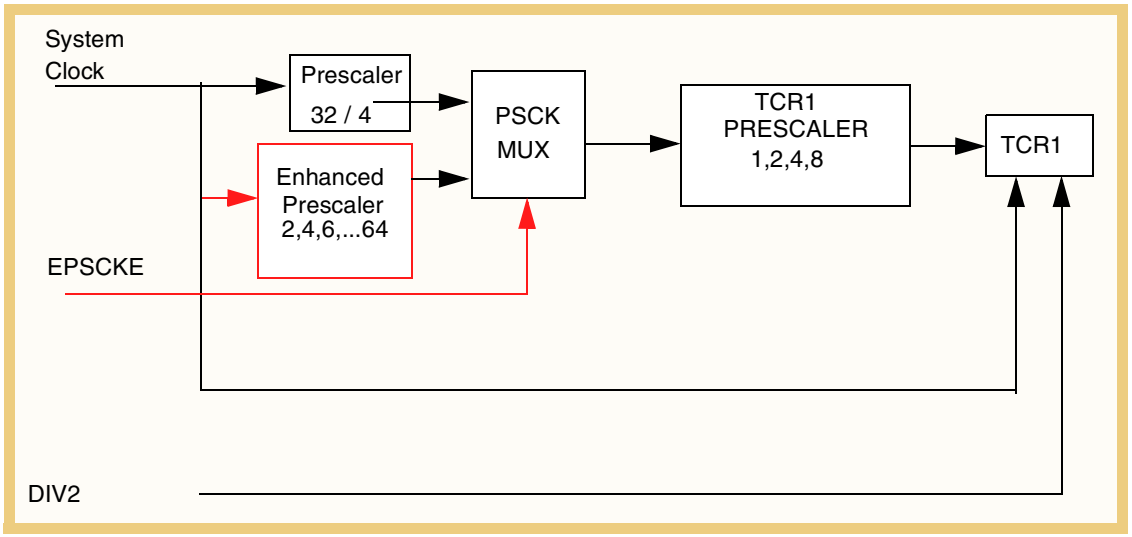

Figure 5-2 TCR1 Prescaler Control

5.3.9 Prescaler Control for TCR2

Timer count register 2 (TCR2), like TCR1, is clocked from the output of a prescaler. The T2CG (TCR2 clock/gate control) bit and the T2CSL (TCR2 counter clock edge) bit in TPUMCR determine T2CR2 pin functions. Refer to **Table 5-3**.

Table 5-3 TCR2 Counter Clock Source

T2CSL	T2CG	TCR2 Clock
0	0	Rise transition T2CLK
0	1	Gated system clock
1	0	Fall transition T2CLK
1	1	Rise & fall transition T2CLK

The function of the T2CG bit is shown in **Figure 5-3**.

When T2CG is set, the external T2CLK pin functions as a gate of the DIV8 clock (the TPU3 system clock divided by eight). In this case, when the external TCR2 pin is low, the DIV8 clock is blocked, preventing it from incrementing TCR2. When the external TCR2 pin is high, TCR2 is incremented at the frequency of the DIV8 clock. When T2CG is cleared, an external clock from the TCR2 pin, which has been synchronized and fed through a digital filter, increments TCR2. The duration between active edges on the T2CLK clock pin must be at least nine system clocks.

The TCR2PSCK2 bit in TPUMCR3 determines whether the clock source is divided by two before it is fed into the TCR2 prescaler. The TCR2 field in TPUMCR specifies the value of the prescaler: 1, 2, 4, or 8. Channels using TCR2 have the capability to

resolve down to the TPU3 system clock divided by eight. **Figure 5-3** illustrates the TCR2 pre-divider and pre-scaler control.

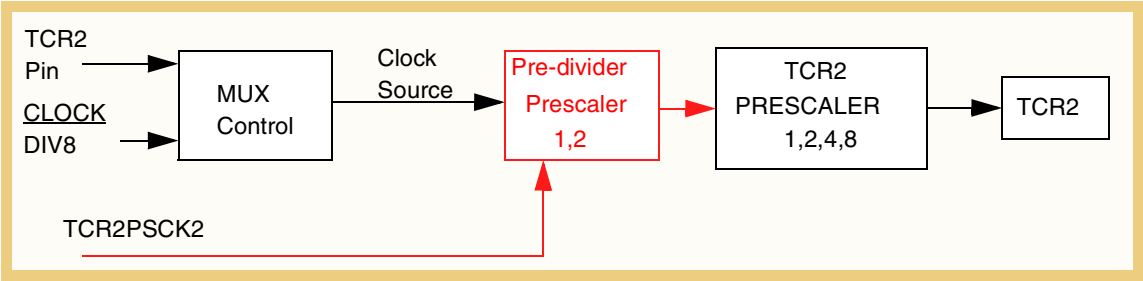

Figure 5-3 TCR2 Prescaler Control

Table 5-4 is a summary of prescaler output (assuming a divide-by-one value for the pre-divider prescaler.

Table 5-4 TCR2 Prescaler Control

TCR2 Prescaler	Divide By	Internal Clock Divided By	External Clock Divided By
00	1	8	1
01	2	16	2
10	4	32	4
11	8	64	8

5.4 Programming Model

The TPU3 memory map contains three groups of registers:

- System configuration registers
- Channel control and status registers
- Development support and test verification registers

All registers except the channel interrupt status register (CISR) must be read or written by means of half-word (16-bit) or word (32-bit) accesses. The address space of the TPU3 memory map occupies 512 bytes. Unused registers within the 512-byte address space return zeros when read.

Table 5-6 shows the TPU3 address map.

Table 5-5 TPU3_B Register Map

MSB 15 Address	LSB 0 Register
0xYF F800	TPU3 module configuration register (TPUMCR) See **Table 5-7** for bit descriptions.
0xYF F802	TPU3 test configuration register (TCR)
0xYF F804	Development support control register (DSCR) See **Table 5-8** for bit descriptions.
0xYF F806	Development support status register (DSSR) See **Table 5-9** for bit descriptions.
0xYF F808	TPU3 interrupt configuration register (TICR) See **Table 5-10** for bit descriptions.
0xYF F80A	Channel interrupt enable register (CIER) See **Table 5-11** for bit descriptions.
0xYF F80C	Channel function selection register 0 (CFSR0) See **Table 5-12** for bit descriptions.
0xYF F80E	Channel function selection register 1 (CFSR1) See **Table 5-12** for bit descriptions.
0xYF F810	Channel function selection register 2 (CFSR2) See **Table 5-12** for bit descriptions.
0xYF F812	Channel function selection register 3 (CFSR3) See **Table 5-12** for bit descriptions.
0xYF F814	Host sequence register 0 (HSQR0) See **Table 5-13** for bit descriptions.
0xYF F816	Host sequence register 1 (HSQR1) See **Table 5-13** for bit descriptions.
0xYF F818	Host service request register 0 (HSRR0) See **Table 5-14** for bit descriptions.
0xYF F81A	Host service request register 1 (HSRR1) See **Table 5-14** for bit descriptions.
0xYF F81C	Channel priority register 0 (CPR0) See **Table 5-15** for bit descriptions.
0xYF F81E	Channel priority register 1 (CPR1) See **Table 5-15** for bit descriptions.
0xYF F820	Channel interrupt status register (CISR) See **Table 5-17** for bit descriptions.
0xYF F822	Link register (LR)
0xYF F824	Service grant latch register (SGLR)
0xYF F826	Decoded channel number register (DCNR)
0xYF F828	TPU module configuration register 2 (TPUMCR2) See **Table 5-18** for bit descriptions.
0xYF F82A	TPU module configuration 3 (TPUMCR3) See **Table 5-21** for bit descriptions.
0xYF F82C	Internal scan data register (ISDR)
0xYF F82E	Internal scan control register (ISCR)
0xYF F900 – 0xYF F90F	Channel 0 parameter registers
0xYF F910 – 0xYF F91F	Channel 1 parameter registers

Table 5-5 TPU3_B Register Map (Continued)

MSB 15 Address	LSB 0 Register
0xYF F920 – 0xYF F92F	Channel 2 parameter registers
0xYF F930 – 0xYF F93F	Channel 3 parameter registers
0xYF F940 – 0xYF F94F	Channel 4 parameter registers
0xYF F950 – 0xYF F95F	Channel 5 parameter registers
0xYF F960 – 0xYF F96F	Channel 6 parameter registers
0xYF F970 – 0xYF F97F	Channel 7 parameter registers
0xYF F980 – 0xYF F98F	Channel 8 parameter registers
0xYF F990 – 0xYF F99F	Channel 9 parameter registers
0xYF F9A0 – 0xYF F9AF	Channel 10 parameter registers
0xYF F9B0 – 0xYF F9BF	Channel 11 parameter registers
0xYF F9C0 – 0xYF F9CF	Channel 12 parameter registers
0xYF F9D0 – 0xYF F9DF	Channel 13 parameter registers
0xYF F9E0 – 0xYF F9EF	Channel 14 parameter registers
0xYF F9F0 – 0xYF F9FF	Channel 15 parameter registers

Table 5-6 TPU3_A Register Map

MSB 15 Address	LSB 0 Register
0xYF FE00	TPU3 module configuration register (TPUMCR) See **Table 5-7** for bit descriptions.
0xYF FE02	TPU3 test configuration register (TCR)
0xYF FE04	Development support control register (DSCR) See **Table 5-8** for bit descriptions.
0xYF FE06	Development support status register (DSSR) See **Table 5-9** for bit descriptions.
0xYF FE08	TPU3 interrupt configuration register (TICR) See **Table 5-10** for bit descriptions.
0xYF FE0A	Channel interrupt enable register (CIER) See **Table 5-11** for bit descriptions.
0xYF FE0C	Channel function selection register 0 (CFSR0) See **Table 5-12** for bit descriptions.
0xYF FE0E	Channel function selection register 1 (CFSR1) See **Table 5-12** for bit descriptions.
0xYF FE10	Channel function selection register 2 (CFSR2) See **Table 5-12** for bit descriptions.
0xYF FE12	Channel function selection register 3 (CFSR3) See **Table 5-12** for bit descriptions.
0xYF FE14	Host sequence register 0 (HSQR0) See **Table 5-13** for bit descriptions.
0xYF FE16	Host sequence register 1 (HSQR1) See **Table 5-13** for bit descriptions.

Table 5-6 TPU3_A Register Map (Continued)

MSB 15 Address	LSB 0 Register
0xYF FE18	Host service request register 0 (HSRR0) See **Table 5-14** for bit descriptions.
0xYF FE1A	Host service request register 1 (HSRR1) See **Table 5-14** for bit descriptions.
0xYF FE1C	Channel priority register 0 (CPR0) See **Table 5-15** for bit descriptions.
0xYF FE1E	Channel priority register 1 (CPR1) See **Table 5-15** for bit descriptions.
0xYF FE20	Channel interrupt status register (CISR) See **Table 5-17** for bit descriptions.
0xYF FE22	Link register (LR)
0xYF FE24	Service grant latch register (SGLR)
0xYF FE26	Decoded channel number register (DCNR)
0xYF FE28	TPU module configuration register 2 (TPUMCR2) See **Table 5-18** for bit descriptions.
0xYF FE2A	TPU module configuration 3 (TPUMCR3) See **Table 5-21** for bit descriptions.
0xYF FE2C	Internal scan data register (ISDR)
0xYF FE2E	Internal scan control register (ISCR)
0xYF FF00 – 0xYF FF0F	Channel 0 parameter registers
0xYF FF10 – 0xYF FF1F	Channel 1 parameter registers
0xYF FF20 – 0xYF FF2F	Channel 2 parameter registers
0xYF FF30 – 0xYF FF3F	Channel 3 parameter registers
0xYF FF40 – 0xYF FF4F	Channel 4 parameter registers
0xYF FF50 – 0xYF FF5F	Channel 5 parameter registers
0xYF FF60 – 0xYF FF6F	Channel 6 parameter registers
0xYF FF70 – 0xYF FF7F	Channel 7 parameter registers
0xYF FF80 – 0xYF FF8F	Channel 8 parameter registers
0xYF FF90 – 0xYF FF9F	Channel 9 parameter registers
0xYF FFA0 – 0xYF FFAF	Channel 10 parameter registers
0xYF FFB0 – 0xYF FFBF	Channel 11 parameter registers
0xYF FFC0 – 0xYF FFCF	Channel 12 parameter registers
0xYF FFD0 – 0xYF FFDF	Channel 13 parameter registers
0xYF FFE0 – 0xYF FFEF	Channel 14 parameter registers
0xYF FFF0 – 0xYF FFFF	Channel 15 parameter registers

5.4.1 TPU Module Configuration Register

TPUMCR — TPU Module Configuration Register

0xYF F800
0xYF FE00

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
STOP	TCR1P		TCR2P		EMU	T2CG	STF	SUPV	PSCK	TPU3	T2CSL	IARB[3:0]			
RESET:															
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 5-7 TPUMCR Bit Settings

Bit(s)	Name	Description
15	STOP	Low-power stop mode enable. If the STOP bit in TPUMCR is set, the TPU3 shuts down its internal clocks, shutting down the internal microengine. TCR1 and TCR2 cease to increment and retain the last value before the stop condition was entered. The TPU3 asserts the stop flag (STF) in TPUMCR to indicate that it has stopped. 0 = Enable TPU3 clocks 1 = Disable TPU3 clocks
14:13	TCR1P	Timer count register 1 prescaler control. TCR1 is clocked from the output of a prescaler. The prescaler divides its input by 1, 2, 4, or 8. This is a write-once field unless the PWOD bit in TPUMCR3 is set. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 Refer to **5.3.8 Prescaler Control for TCR1** for more information.
12:11	TCR2P	Timer count register 2 prescaler control. TCR2 is clocked from the output of a prescaler. The prescaler divides this input by 1, 2, 4, or 8. This is a write-once field unless the PWOD bit in TPUMCR3 is set. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 Refer to **5.3.9 Prescaler Control for TCR2** for more information.
10	EMU	Emulation control. In emulation mode, the TPU3 executes microinstructions from DPTRAM exclusively. Access to the DPTRAM via the IMB3 is blocked, and the DPTRAM is dedicated for use by the TPU3. After reset, this bit can be written only once. 0 = TPU3 and DPTRAM operate normally 1 = TPU3 and DPTRAM operate in emulation mode
9	T2CG	TCR2 clock/gate control 0 = TCR2 pin used as clock source for TCR2 1 = TCR2 pin used as gate of DIV8 clock for TCR2 Refer to **5.3.9 Prescaler Control for TCR2** for more information.
8	STF	Stop flag. 0 = TPU3 is operating normally 1 = TPU3 is stopped (STOP bit has been set)
7	SUPV	Supervisor data space 0 = Assignable registers are accessible from user or supervisor privilege level 1 = Assignable registers are accessible from supervisor privilege level only
6	PSCK	Standard prescaler clock. Note that this bit has no effect if the extended prescaler is selected (EPSCKE = 1). 0 = $f_{SYS} \div 32$ is input to TCR1 prescaler, if standard prescaler is selected 1 = $f_{SYS} \div 4$ is input to TCR1 prescaler, if standard prescaler is selected

Table 5-7 TPUMCR Bit Settings (Continued)

Bit(s)	Name	Description
5	TPU3	TPU3 enable. The TPU3 enable bit provides compatibility with the TPU. If running TPU code on the TPU3, the microcode size should not be greater than 2 Kbytes and the TPU3 enable bit should be cleared to zero. The TPU3 enable bit is write-once after reset. The reset value is one, meaning that the TPU3 will operate in TPU3 mode. 0 = TPU mode; zero is the TPU reset value 1 = TPU3 mode; one is the TPU3 reset value **NOTE**: The programmer should not change this value unless necessary when developing custom TPU microcode.
4	T2CSL	TCR2 counter clock edge. This bit and the T2CG control bit determine the clock source for TCR2. Refer to **5.3.9 Prescaler Control for TCR2** for details.
3:0	IARB[3:0]	Interrupt Arbitration ID. The IARB field is used to arbitrate between simultaneous interrupt requests of the same priority. Each module that can generate interrupt requests must be assigned a unique, non-zero IARB field value.

5.4.2 Development Support Control Register

DSCR — Development Support Control Register **0xYF F804**
0xYF FE04

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
HOT4	RESERVED				BLC	CLKS	FRZ		CCL	BP	BC	BH	BL	BM	BT
RESET:															
0					0	0	0	0	0	0	0	0	0	0	0

Table 5-8 DSCR Bit Settings

Bit(s)	Name	Description
15	HOT4	Hang on T4 0 = Exit wait on T4 state caused by assertion of HOT4 1 = Enter wait on T4 state
14:11	—	Reserved
10	BLC	Branch latch control 0 = Latch conditions into branch condition register before exiting halted state 1 = Do not latch conditions into branch condition register before exiting the halted state or during the time-slot transition period
9	CLKS	Stop clocks (to TCRs) 0 = Do not stop TCRs 1 = Stop TCRs during the halted state
8:7	FRZ	FREEZE assertion response. The FRZ bits specify the TPU microengine response to the IMB3 FREEZE signal 00 = Ignore freeze 01 = Reserved 10 = Freeze at end of current microcycle 11 = Freeze at next time-slot boundary
6	CCL	Channel conditions latch. CCL controls the latching of channel conditions (MRL and TDL) when the CHAN register is written. 0 = Only the pin state condition of the new channel is latched as a result of the write CHAN register microinstruction 1 = Pin state, MRL, and TDL conditions of the new channel are latched as a result of a write CHAN register microinstruction

Table 5-8 DSCR Bit Settings (Continued)

Bit(s)	Name	Description
5	BP	µPC breakpoint enable 0 = Breakpoint not enabled 1 = Break if µPC equals µPC breakpoint register
4	BC	Channel breakpoint enable 0 = Breakpoint not enabled 1 = Break if CHAN register equals channel breakpoint register at beginning of state or when CHAN is changed through microcode
3	BH	Host service breakpoint enable 0 = Breakpoint not enabled 1 = Break if host service latch is asserted at beginning of state
2	BL	Link service breakpoint enable 0 = Breakpoint not enabled 1 = Break if link service latch is asserted at beginning of state
1	BM	MRL breakpoint enable 0 = Breakpoint not enabled 1 = Break if MRL is asserted at beginning of state
0	BT	TDL breakpoint enable 0 = Breakpoint not enabled 1 = Break if TDL is asserted at beginning of state

5.4.3 Development Support Status Register

DSSR — Development Support Status Register **0xYF F806**
0xYF FE06

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED								BKPT	PCBK	CHBK	SRBK	TPUF	RESERVED		
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-9 DSSR Bit Settings

Bit(s)	Name	Description
15:8	—	Reserved
7	BKPT	Breakpoint asserted flag. If an internal breakpoint caused the TPU3 to enter the halted state, the TPU3 asserts the BKPT signal on the IMB and sets the BKPT flag. BKPT remains set until the TPU3 recognizes a breakpoint acknowledge cycle, or until the IMB FREEZE signal is asserted.
6	PCBK	µPC breakpoint flag. PCBK is asserted if a breakpoint occurs because of a µPC (microprogram counter) register match with the µPC breakpoint register. PCBK is negated when the BKPT flag is cleared.
5	CHBK	Channel register breakpoint flag. CHBK is asserted if a breakpoint occurs because of a CHAN register match with the CHAN register breakpoint register. CHBK is negated when the BKPT flag is cleared.
4	SRBK	Service request breakpoint flag. SRBK is asserted if a breakpoint occurs because of any of the service request latches being asserted along with their corresponding enable flag in the development support control register. SRBK is negated when the BKPT flag is cleared.

Table 5-9 DSSR Bit Settings (Continued)

Bit(s)	Name	Description
3	TPUF	TPU3 FREEZE flag. TPUF is set whenever the TPU3 is in a halted state as a result of FREEZE being asserted. This flag is automatically negated when the TPU3 exits the halted state because of FREEZE being negated.
2:0	—	Reserved

5.4.4 TPU3 Interrupt Configuration Register

TICR — TPU3 Interrupt Configuration Register **0xYF F808**
0xYF FE08

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED					CIRL			CIBV				RESERVED			
RESET:					0	0	0	0	0	0	0				

Table 5-10 TICR Bit Settings

Bit(s)	Name	Description
15:11	—	Reserved
10:8	CIRL	Channel interrupt request level. This three-bit field specifies the interrupt request level for all channels. T field is used in conjunction with the ILBS field to determine the request level of TPU3 interrupts.
7:4	CIBV	Channel interrupt base vector. The TPU is assigned 16 unique interrupt vector numbers, one vector number for each channel. The CIBV field specifies the most significant nibble of all 16 TPU channel interrupt vector numbers. The lower nibble of the TPU interrupt vector number is determined by the channel number on which the interrupt occurs.
3:0	—	Reserved.

5.4.5 Channel Interrupt Enable Register

The channel interrupt enable register (CIER) allows the CPU to enable or disable the ability of individual TPU3 channels to request interrupt service. Setting the appropriate bit in the register enables a channel to make an interrupt service request; clearing a bit disables the interrupt.

CIER — Channel Interrupt Enable Register **0xYF FE0A**
0xYF FE0A

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-11 CIER Bit Settings

Bit(s)	Name	Description
15:0	CH[15:0]	Channel interrupt enable/disable 0 = Channel interrupts disabled 1 = Channel interrupts enabled **NOTE:** The MSB (bit 0 in big-endian mode) represents CH15, and the LSB (bit 15 in big-endian mode) represents CH0.

5.4.6 Channel Function Select Registers

Encoded 4-bit fields within the channel function select registers specify one of 16 time functions to be executed on the corresponding channel. Encodings for predefined functions will be provided in a subsequent draft of this document.

CFSR0 — Channel Function Select Register 0 **0xYF F80C 0xYF FE0C**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 15				CH 14				CH 13				CH 12			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CFSR1 — Channel Function Select Register 1 **0xYF F80E 0xYF FE0E**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 11				CH 10				CH 9				CH 8			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CFSR2 — Channel Function Select Register 2 **0xYF F810 0xYF FE10**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 7				CH 6				CH 5				CH 4			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CFSR3 — Channel Function Select Register 3 **0xYF F812 0xYF FE12**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 3				CH 2				CH 1				CH 0			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-12 CFSRx Bit Settings

Name	Description
CH[15:0]	Encoded time function for each channel. Encoded four-bit fields in the channel function select registers specify one of 16 time functions to be executed on the corresponding channel.

5.4.7 Host Sequence Registers

The host sequence field selects the mode of operation for the time function selected on a given channel. The meaning of the host sequence bits depends on the time function specified. Meanings of host sequence bits and host service request bits for predefined time functions will be provided in a subsequent draft of this document.

HSQR0 — Host Sequence Register 0 **0xYF F814**
0xYF FE14

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 15		CH 14		CH 13		CH 12		CH 11		CH 10		CH 9		CH 8	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HSQR1 — Host Sequence Register 1 **0xYF F816**
0xYF FE16

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 7		CH 6		CH 5		CH 4		CH 3		CH 2		CH 1		CH 0	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-13 HSQRx Bit Settings

Name	Description
CH[15:0]	Encoded host sequence. The host sequence field selects the mode of operation for the time function selected on a given channel. The meaning of the host sequence bits depends on the time function specified.

5.4.8 Host Service Request Registers

The host service request field selects the type of host service request for the time function selected on a given channel. The meaning of the host service request bits is determined by time function microcode. Refer to Motorola's ***TPU Literature Package, TPULITPAK/D,*** for the available TPU documentation.

HSRR0 — Host Service Request Register 0

0xYF F818
0xYF FE18

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 15		CH 14		CH 13		CH 12		CH 11		CH 10		CH 9		CH 8	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HSRR1 — Host Service Request Register 1

0xYF F81A
0xYF FE1A

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 7		CH 6		CH 5		CH 4		CH 3		CH 2		CH 1		CH 0	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-14 HSSRx Bit Settings

Name	Description
CH[15:0]	Encoded type of host service. The host service request field selects the type of host service request for the time function selected on a given channel. The meaning of the host service request bits depends on the time function specified. A host service request field cleared to 0b00 signals the host that service is completed by the microengine on that channel. The host can request service on a channel by writing the corresponding host service request field to one of three non-zero states. The CPU must monitor the host service request register until the TPU3 clears the service request to 0b00 before any parameters are changed or a new service request is issued to the channel.

5.4.9 Channel Priority Registers

The channel priority registers (CPR1, CPR2) assign one of three priority levels to a channel or disable the channel.

CPR0 — Channel Priority Register 0

0xYF F81C
0xYF FE1C

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 15		CH 14		CH 13		CH 12		CH 11		CH 10		CH 9		CH 8	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CPR1 — Channel Priority Register 1

0xYF F81E
0xYF FE1E

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 7		CH 6		CH 5		CH 4		CH 3		CH 2		CH 1		CH 0	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-15 CPRx Bit Settings

Name	Description
CH[15:0]	Encoded channel priority levels. **Table 5-16** indicates the number of time slots guaranteed for each channel priority encoding.

Table 5-16 Channel Priorities

CHx[1:0]	Service	Guaranteed Time Slots
00	Disabled	—
01	Low	1 out of 7
10	Middle	2 out of 7
11	High	4 out of 7

5.4.10 Channel Interrupt Status Register

The channel interrupt status register (CISR) contains one interrupt status flag per channel. Time functions specify via microcode when an interrupt flag is set. Setting a flag causes the TPU3 to make an interrupt service request if the corresponding CIER bit is set. To clear a status flag, read CISR, then write a zero to the appropriate bit. CISR is the only TPU3 register that can be accessed on a byte basis.

CISR — Channel Interrupt Status Register

0xYF F820
0xYF FE20

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-17 CISR Bit Settings

Bit(s)	Name	Description
15:0	CH[15:0]	Channel interrupt status 0 = Channel interrupt not asserted 1 = Channel interrupt asserted

5.4.11 TPU3 Module Configuration Register 2

TPUMCR2 — TPU Module Configuration Register 2 **0xYF F828**
0xYF FE28

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED							DIV2	SOFT RST	ETBANK		FPSCK			T2CF	DTPU
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-18 TPUMCR2 Bit Settings

Bit(s)	Name	Description
15:9	—	Reserved
8	DIV2	Divide by two control. When asserted, the DIV2 bit, along with the TCR1P bit and the PSCK bit in the TPUMCR, determines the rate of the TCR1 counter in the TPU3. If set, the TCR1 counter increments at a rate of two system clocks. If negated, TCR1 increments at the rate determined by control bits in the TCR1P and PSCK fields. 0 = TCR1 increments at rate determined by control bits in the TCR1P and PSCK fields of the TPUMCR register 1 = Causes TCR1 counter to increment at a rate of the system clock divided by two
7	SOFT RST	Soft reset. The TPU3 performs an internal reset when both the SOFT RST bit in the TPUMCR2 and the STOP bit in TPUMCR are set. The CPU must write zero to the SOFT RST bit to bring the TPU3 out of reset. The SOFT RST bit must be asserted for at least nine clocks. 0 = Normal operation 1 = Puts TPU3 in reset until bit is cleared **NOTE**: Do not attempt to access any other TPU3 registers when this bit is asserted. When this bit is asserted, it is the only accessible bit in the register.
6:5	ETBANK	Entry table bank select. This field determines the bank where the microcoded entry table is situated. After reset, this field is 0b00. This control bit field is write once after reset. ETBANK is used when the microcode contains entry tables not located in the default bank zero. To execute the ROM functions on this MCU, ETBANK[1:0] must be 00. Refer to **Table 5-19**. **NOTE**: This field should not be modified by the programmer unless necessary because of custom microcode.
4:2	FPSCK	Filter prescaler clock. The filter prescaler clock control bit field determines the ratio between system clock frequency and minimum detectable pulses. The reset value of these bits is zero, defining the filter clock as four system clocks. Refer to **Table 5-20**.
1	T2CF	T2CLK pin filter control. When asserted, the T2CLK input pin is filtered with the same filter clock that is supplied to the channels. This control bit is write once after reset. 0 = Uses fixed four-clock filter 1 = T2CLK input pin filtered with same filter clock that is supplied to the channels
0	DTPU	Disable TPU3 pins. When the disable TPU3 control pin is asserted, pin TP15 is configured as an input disable pin. When the TP15 pin value is zero, all TPU3 output pins are three-stated, regardless of the pins function. The input is not synchronized. This control bit is write once after reset. 0 = TP15 functions as normal TPU3 channel 1 = TP15 pin configured as output disable pin. When TP15 pin is low, all TPU3 output pins are in a high-impedance state, regardless of the pin function.

Table 5-19 Entry Table Bank Location

ETBANK	Bank
00	0
01	1
10	2
11	3

Table 5-20 System Clock Frequency/Minimum Guaranteed Detected Pulse

Filter Control	Divide By	20 MHz	33 MHz
000	4	200 ns	121 ns
001	8	400 ns	242 ns
010	16	800 ns	485 ns
011	32	1.6 µs	970 ns
100	64	3.2 µs	1.94 µs
101	128	6.4 µs	3.88 µs
110	256	12.8 µs	7.76 µs
111	512	25.6 µs	15.51 µs

5.4.12 TPU Module Configuration Register 3

TPUMCR3 — TPU Module Configuration Register 3 **0xYF F82A**
0xYF FE2A

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED							PWOD	TCR2PCK2	EP-SCKE	RESERVED	EPSCK				
RESET:					0	0	0	0	0	0	0				

Table 5-21 TPUMCR3 Bit Settings

Bit(s)	Name	Description
15:9	—	Reserved
8	PWOD	Prescaler write-once disable bit. The PWOD bit does not lock the EPSCK field and the EPSCKE bit. 0 = Prescaler fields in MCR are write-once 1 = Prescaler fields in MCR can be written anytime
7	TCR2PSCK2	TCR2 prescaler 2 0 = Prescaler clock source is divided by one 1 = Prescaler clock source is divided by two
6	EPSCKE	Enhanced pre-scaler enable 0 = Disable enhanced prescaler (use standard prescaler) 1 = Enable enhanced prescaler. System clock will be divided by the value in EPSCK field.
5	—	Reserved
4:0	EPSCK	Enhanced prescaler value that will be loaded into the enhanced prescaler counter. Prescaler value = (EPSCK + 1) x 2. Refer to **5.3.8 Prescaler Control for TCR1** for details.

5.4.13 TPU3 Parameter RAM

The channel parameter registers are organized as one hundred 16-bit words of RAM. Channels 0 to 15 have eight parameters. The parameter registers constitute a shared work space for communication between the CPU and the TPU3. The TPU3 can only access data in the parameter RAM, refer to **Table 5-22**.

Table 5-22 Parameter RAM Address Map[1]

Channel Number	Parameter							
	0	1	2	3	4	5	6	7
0	00	02	04	06	08	0A	0C	0E
1	10	12	14	16	18	1A	1C	1E
2	20	22	24	26	28	2A	2C	2E
3	30	32	34	36	38	3A	3C	3E
4	40	42	44	46	48	4A	4C	4E
5	50	52	54	56	58	5A	5C	5E
6	60	62	64	66	68	6A	6C	6E
7	70	72	74	76	78	7A	7C	7E
8	80	82	84	86	88	8A	8C	8E
9	90	92	94	96	98	9A	9C	9E
10	A0	A2	A4	A6	A8	AA	AC	AE
11	B0	B2	B4	B6	B8	BA	BC	BE
12	C0	C2	C4	C6	C8	CA	CC	CE
13	D0	D2	D4	D6	D8	DA	DC	DE
14	E0	E2	E4	E6	E8	EA	EC	EE
15	F0	F2	F4	F6	F8	FA	FC	FE

NOTES:

1. The base address of the parameter RAM is 0xYF FF00. The parameter RAM addresses should be added to the base address.