SECTION 12
STATIC RANDOM ACCESS MEMORY (SRAM)

12.1 Introduction

This SRAM module is a fast access (two clocks) general purpose 8 Kbytes (8,192 bytes) static RAM (SRAM) for the MCU and is accessed via the IMB3. In addition there is 2 Kbytes (configured as four blocks of 512 bytes each) of patch static RAM. These modules are fast access (two clocks) general purpose static RAM (SRAM) for the MCU with a patch option which provides a method to overlay the internal CMFI memory for emulation. As an additional feature, the 512-byte arrays can be used as additional SRAM. A register map showing the SRAM and overlay configuration registers and memory blocks is shown in **Figure 12-1**.

The SRAM module is powered by V_{DDL} in normal operation and may be used as standby SRAM if standby power is supplied via the V_{STBY} pin of the MCU. Switching between V_{DDL} and V_{STBY} will occur automatically.

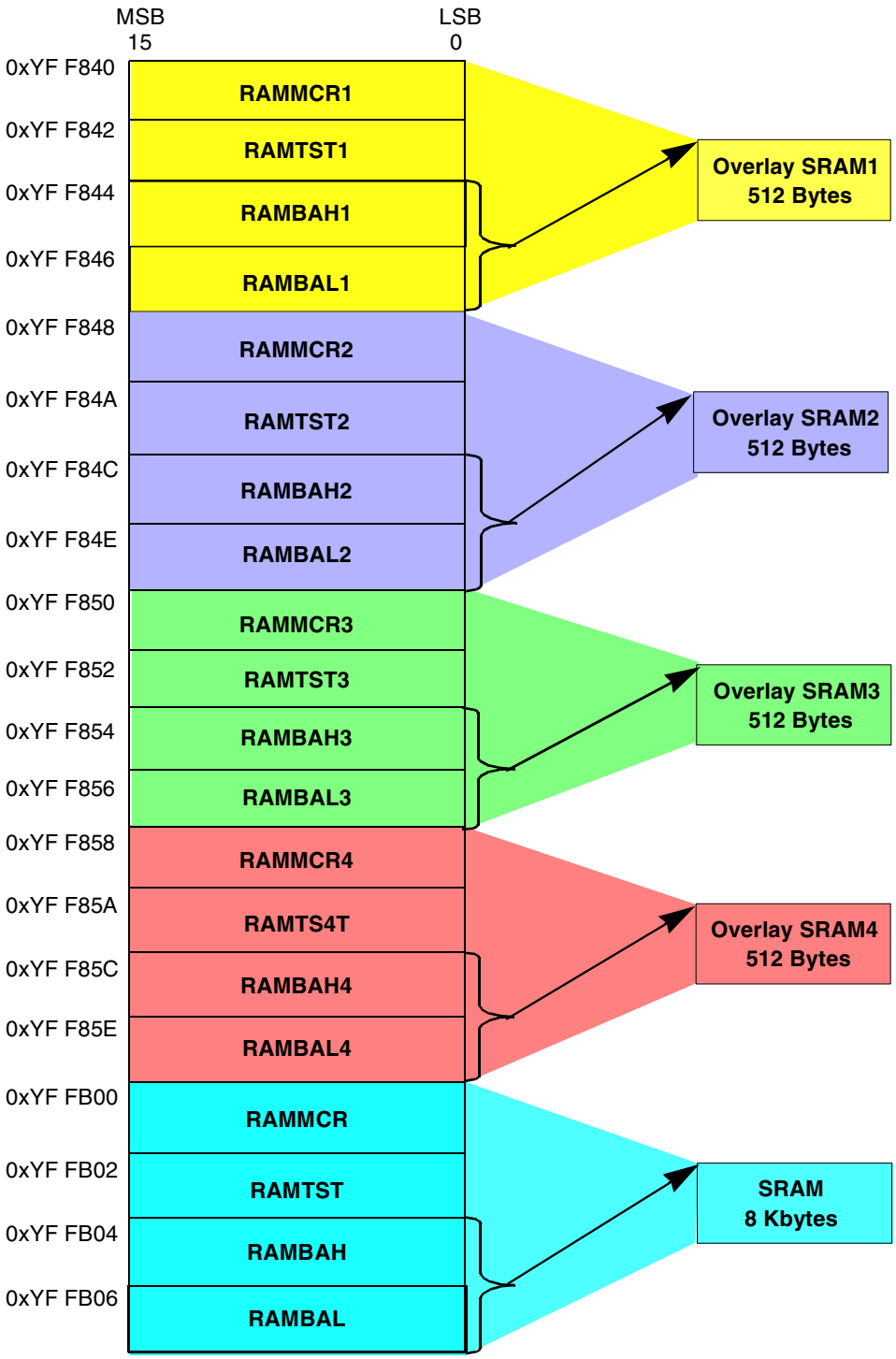
When used as general purpose SRAM, this module is accessed via the IMB3. The SRAM may be read or written as either bytes or words. Access for aligned long-word operations is supported by back-to-back IMB3 accesses (four clocks) to accommodate 32-bit operations.

12.2 Programmer's Model

Each SRAM module consists of two separately addressable sections. The first is a set of memory mapped control and status registers used for configuration and testing of the SRAM array. The second section is the array itself.

12.2.1 SRAM Control Block

There are four registers provided for configuration and control of each SRAM module: SRAM module configuration register (RAMMCR), a factory test register (RAMTST), and the array base address registers (RAMBAH, RAMBAL). In order to offer the maximum protection for the SRAM array, the SRAM module control registers are located in supervisor data space.



Y = M111, where M is the logic state of the module mapping (MM) bit in the SCIM2E configuration register (SCIMMCR).

Figure 12-1 SRAM Module Configuration

12.2.2 SRAM Array

The SRAM array itself can be placed anywhere in the address map of the MCU by means of the array base address registers. The high order address lines (IADDR[31:N] N=13 and nine for 8-Kbyte and 512-byte arrays) are compared with the value in RAMBAH and RAMBAL registers for a base address match. This value points to the lowest address that SRAM data may be located and is always on an 8-Kbyte or 512-byte boundary. The SRAM array top is on a 256-byte boundary. The only restrictions on the base address is that it must be on an address boundary greater than or equal to the array size. If the SRAM array base address is located to overlap the SRAM control block then access to the 8 bytes in the SRAM array located at the same address as the SRAM control block are ignored allowing the control block to be accessed.

NOTE

This is only the eight bytes in the SRAM control block; this mapping may have unknown results for other modules.

12.2.2.1 SRAM Array Addressing

The BIU of the SRAM module compares IADDR[31:N] (N = 13 for 8 Kbytes and 9 for 512-byte arrays) of the IMB3 with the value of the array base address registers. If they match then the low address and ISIZ[1:0] are used to access the SRAM location in the array. Addresses in the array that are not implemented will be ignored by the SRAM module allowing an external device to respond to the address. Function codes are also checked for the correct access rights. If the array is placed in supervisor space, user accesses will be ignored allowing an external device to respond to the address. If the array is placed in unrestricted space, it will respond to both user and supervisor accesses. The array may also be placed in program space, or program/data space. Program space allows the SRAM array to contain only program instructions for execution, or program counter relative addressing modes for operand fetches from the array. Program/data space allows both program and data may be stored in the SRAM array.

12.3 SRAM Module Control and Status Registers

The SRAM module control and status registers are used to control and monitor the operation of the SRAM array. The following sections describe the operation of each register in the SRAM control block. Since all the registers are in supervisor data space, the only way to change the state of the registers is through a supervisor program. Any other restrictions for making changes to the registers will be noted in the description of the register. Unless otherwise noted, any source of master reset will cause register bits to be forced to their reset state; while, system resets have no effect on the registers. Reads to unimplemented bits will return “0”; while, writes have no effect.

12.3.1 Module Configuration Register (RAMMCR)

All modules on the MCU contain a module configuration register. The RAMMCR register bits configure the SRAM module for stop operation and for proper access rights to the array.

RAMMCR1 — SRAM Module Configuration Register **0xYF F840**
RAMMCR2 **0xYF F848**
RAMMCR3 **0xYF F850**
RAMMCR4 **0xYF F858**
RAMMCR **0xYF FB00**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
STOP	RESERVED		PDS	RLCK	0	RASP[1:0]		RESERVED							
RESET:															
1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Table 12-1 RAMMCR Bit Settings

Bit(s)	Name	Description
15	STOP	Stop control. The assertion of the STOP control bit in the RAMMCR register by a bus master signals the SRAM module to enter into the STOP state. When STOP is asserted, SRAM array accesses are ignored. When the SRAM module is in normal mode of operation the array base address registers are write protected. 0 = SRAM module normal operation. 1 = Causes SRAM module to enter low power stop mode.
14:13	—	Reserved
12	PDS	Power down status. PDS is a optional status bit in the RAMMCR that enables a power monitor for the SRAM array. The power monitor circuit will clear the PDS bit (PDS = “0”) if the array standby power is lost. If the PDS bit is unimplemented reads will return “0”. 0 = Power monitor for the SRAM array is disabled. SRAM array standby power has failed. 1 = Power monitor for the SRAM array is enabled. SRAM array standby power has not failed.
11	RLCK	Base address lock. 0 = SRAM base address registers are writable from the IMB3. 1 = SRAM base address registers are write locked.
10	—	Reserved
9:8	RASP[1:0]	Array space. The RASP field limits access to the SRAM array to one of four CPU32 address spaces. Refer to. 0 = Only the module configuration register, test register, and interrupt register are designated as supervisor-only data space. Access to all other locations is unrestricted. 1 = All QADC64 registers and tables are designated as supervisor-only data space.
7:0	—	Reserved

Table 12-2 RASP Encoding

RASP[1:0]	Space
00	Unrestricted program and data
01	Unrestricted program
10	Supervisor program and data
11	Supervisor program

12.3.2 Array Base Address Registers (RAMBAH, RAMBAL)

The array base address registers are provided to allow the flexibility of placing the SRAM array anywhere in the memory map. RAMBAH and RAMBAL contains an address field used to specify the most significant bits of the lowest address value in

the SRAM array address block. The SRAM array base address is placed on a 512, 1-Kbyte, 2-Kbyte or 4-Kbyte block boundary (block size greater than or equal to the size of the array). RAMBAH and RAMBAL may only be written while the SRAM is in STOP mode STOP = “1” and the lock bit is not set RLCK = “0”. Once the RLCK bit is set, writes will have no effect on RAMBAH and RAMBAL. This will prevent runaway software from inadvertently re-mapping the array. The SRAM must be in STOP mode while RAMBAH or RAMBAL are written this prevents inadvertent intermediate array mapping to be acknowledged.

RAMBAH1, RAMBAL1 — SRAM Base Address Registers **0xYF F844, 0xYF F846**
RAMBAH2, RAMBAL2 0xYF F84C, 0xYF F84E
RAMBAH3, RAMBAL3 0xYF F854, 0xYF F856
RAMBAH4, RAMBAL4 0xYF F85C, 0xYF F85E
RAMBAH, RAM1BAL 0xYF FB04, 0xYF FB06

MSB 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	LSB 16
RAMBAH															
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RAMBAL							RESERVED								
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 12-3 RAMBAH, RAMBAL Bit Settings

Bit(s)	Name	Description
31:16	RAMBAH	Array base address high. With STOP asserted the base Address field of RAMBAH may be changed so that the array may be placed at the desired address in the memory map. This must be done by a supervisor program since the register is in supervisor data space. To lock the base address field, RLCK in the RAMMCR should be set. This will prevent the base address field from being changed until the next master reset.
15:9	RAMBAL	Array base address low. With STOP asserted the base Address field of RAMBAL may be changed so that the array may be placed at the desired address in the memory map. This must be done by a supervisor program since the register is in supervisor data space. To lock the base address field, RLCK RAMMCR should be set. This will prevent the base address field from being changed until the next master reset.
8:0	—	Reserved

12.4 Operation

The SRAM module has several modes of operation. The following sections describe SRAM module operation in each of these modes.

12.4.1 Normal Operation

Normal operation is when the SRAM may be accessed via the IMB3 by a bus master and is being powered by V_{DDL}. The array may be accessed as byte or word. Access may be either read or write.

12.4.1.1 Read/Write

The SRAM module allows a byte or aligned word read/write in one IMB3 bus cycle. Long word read/write will require an additional bus cycle. An IMB3 bus cycle requires two system clocks.

Table 12-4 SRAM Array Read/Write Minimum Access Times

TYPE	Bus Cycles Required for Read or Write	Number of System Clocks
Byte	1	2
Aligned Word	1	2
Aligned Long Word	2	4

12.4.2 Standby Operation

A separate supply pin is used by the standby SRAM module to maintain the contents of the SRAM array during a power down phase. The external supply pin of the MCU is known as V_{STBY}. Data in the standby SRAM will be retained down to the lowest supply voltage, either V_{DDL} or V_{STBY}, see **APPENDIX E ELECTRICAL AND AC CHARACTERISTICS**. Circuitry within the standby SRAM module will automatically switch between V_{DDL} and V_{STBY}. The SRAM module will switch to standby power when $V_{DDL} < V_{STBY} - V_{SWITCH}$.

When the SRAM array is powered by the V_{STBY} pin of the MCU, access to the SRAM array is blocked. Data read from the SRAM array during this condition will not be valid. Data written to the SRAM may be corrupted if switching occurs during a write operation. For the module to function correctly as general purpose SRAM, the maximum value for $V_{STBY} \leq V_{DDL}$.

12.4.2.1 Power Down

In order to guarantee valid standby SRAM data during power down, external low voltage inhibit circuitry, (external to the MCU), must be designed to force the RESET pin into the active state before V_{DDL} drops below its normal limit. This is necessary to inhibit a write cycle to the SRAM during power down.

12.4.3 RESET Operation

When a synchronous reset occurs, a bus master will be allowed, as a result of internal synchronization, to complete the current access. Thus, a write bus cycle, byte or word, that is in progress when a synchronous reset occurs will be completed without error. During the RESET state, once an in-progress write has been completed, further writes to the standby SRAM array will be inhibited.

Note that a long word write will be completed coherently only if the reset occurs during the second write bus cycle. If reset occurs during the first write bus cycle, only the first word will be written to the SRAM array and the second write will not be allowed to occur. In this case, the long word data contained in the SRAM will not be coherent. The first word will contain the most significant half of the new long word information and the second word will contain the least significant half of the old long word information.

If a reset is generated by an asynchronous reset such as the loss of clocks or software watchdog time-out, the contents of the standby SRAM array are not guaranteed.

12.4.4 STOP Operation

The assertion of the STOP control bit of the RAMMCR (see **12.3.1 Module Configuration Register (RAMMCR)**) causes the SRAM module to enter its lowest power consuming state. The register block may still be accessed to allow the STOP control bit to be cleared and the array base address registers to be updated, see **12.3.2 Array Base Address Registers (RAMBAH, RAMBAL)**.

When in stop mode, the SRAM array can not be read or written. All data in the array will be retained. Switching to V_{STBY} will occur as normal if V_{DDL} drops below its specified value when the SRAM module is in stop mode.

12.4.5 Overlay Operation

The four 512-byte SRAM blocks can be used independently of the main 8K SRAM array. The blocks can be initialized to be continuous with the main array or can be used to overlay the flash module. The overlay feature is enabled whenever an overlay SRAM module base address is mapped over the flash array address space. The 512-byte SRAM block should be placed on a 512-byte boundary and will respond to any access to the overlayed section of the flash and will disable the flash contents from being read.