PREFACE

This manual defines the functionality of the MPC555 / MPC556 for use by software and hardware developers. The MPC555 / MPC556 is based on the PowerPC processor used in the Motorola MPC500 family of microcontrollers. For further information refer to the *MPC500 Family RCPU Reference Manual*, RCPURM/AD (Motorola order number).

Boxed sections appear throughout this manual. These boxes designate optional features that are only available on the MPC556.

Audience

This manual is intended for system software and hardware developers and applications programmers who want to develop products for the MPC555 / MPC556. It is assumed that the reader understands operating systems, microprocessor and microcontroller system design, and the basic principles of RISC processing.

Additional Reading

For additional reading that provides background to or supplements the information in this manual see:

- John L. Hennessy and David A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann Publishers, Inc., San Mateo, CA
- ***PowerPC Microprocessor Family: the Programming Environments***, MPCFPE/AD (Motorola order number)
- ***MPC500 Family RCPU Reference Manual***, RCPURM/AD (Motorola order number)

Conventions

This document uses the following notational conventions:

ACTIVE_HIGH	Names for signals that are active high are shown in uppercase text without an overbar. Signals that are active high are referred to as asserted when they are high and negated when they are low.
ACTIVE_LOW	A bar over a signal name indicates that the signal is active low. Active-low signals are referred to as asserted (active) when they are low and negated when they are high.
0x0F	Hexadecimal numbers
0b0011	Binary numbers
REG[FIELD]	Abbreviations or acronyms for registers are shown in uppercase text. Specific bit fields or ranges are shown in brackets.

x	In certain contexts, such as a signal encoding, this indicates a don’t care. For example, if a field is binary encoded 0bx001, the state of the first bit is a don’t care.

NOTE:

Throughout this manual references to 3 V refer to the nominal supply voltage of 3.3 volts.

Nomenclature

Logic level one is the voltage that corresponds to Boolean true (1) state.

Logic level zero is the voltage that corresponds to Boolean false (0) state.

To **set** a bit or bits means to establish logic level one on the bit or bits.

To **clear** a bit or bits means to establish logic level zero on the bit or bits.

A signal that is **asserted** is in its active logic state. An active low signal changes from logic level one to logic level zero when asserted, and an active high signal changes from logic level zero to logic level one.

A signal that is **negated** is in its inactive logic state. An active low signal changes from logic level zero to logic level one when negated, and an active high signal changes from logic level one to logic level zero.

LSB means least significant bit or bits. **MSB** means most significant bit or bits. References to low and high bytes are spelled out.