APPENDIX E
ELECTRICAL CHARACTERISTICS

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing characteristics of the MPC565 / MPC566.

The MPC565 / MPC566 is designed to operate at 40 MHz, or optionally up to 56 MHz. The electrical characteristics are PRELIMINARY and are from previous designs, design simulations, or initial evaluation. These characteristics may not be fully tested or guaranteed at this early stage of the product life cycle, however, for production silicon these characteristics will be met. Finalized characteristics will be published after complete characterization and device qualifications have been completed.

E.1 Absolute Maximum Ratings (VSS = 0V)

Table E-1 Absolute Maximum Ratings

	Rating	Symbol	Min. Value	Max. Value	Unit
1	2.6-V Supply Voltage[1]	V_{DDL}	-0.3	3.0	V
2	Flash Supply Voltages[2]	V_{FLASH}	-0.3	5.6	V
3	Flash Core Voltage[1]	V_{DDF}	-0.3	3.0	V
4	Oscillator, keep-alive Reg. Supply Voltage[1]	KAPWR	-0.3	3.0	V
5	SRAM Supply Voltage[1]	V_{DDSRAM}[1, 2, 3]	-0.3	3.0	V
6	Clock Synthesizer Supply Voltage[1]	V_{DDSYN}	-0.3	3.0	V
7	32-KHz RTC Oscillator Supply Voltage	V_{DDRTC}	-0.3	3.0	V
8	QADC Supply Voltage[3]	V_{DDA}	-0.3	5.6	V
9	5-V Supply Voltage	V_{DDH}	-0.3	5.6	V
10	DC Input Voltages[4,5]	V_{IN}	V_{SS}-0.3	5.6	V
11	Reference V_{RH}, with reference to V_{RL}	V_{RH}	-0.3	5.6	V
12	Reference ALTREF, with reference to V_{RL}	V_{ARH}	-0.3	5.6	V
13	V_{SS} Differential Voltage	$V_{SS} – V_{SSA}$	-0.1	0.1	V
15	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	-5.6	5.6	V
16	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	-5.6	0.3	V
17	Maximum Input Current per pin [6, 7, 8]	I_{MA}	- 25	25	µA
18	QADC Maximum Input Current per Pin	I_{MAX}	-25	25	µA
19	Operating Temperature Range – Ambient (Packaged)	T_A	-40 (T_L)	+125 (T_H)	°C
20	Operating Temperature Range – Solder Ball (Packaged any perimeter solder ball)[9]	T_{SB}	-40 (T_L)	+135 (T_H)	°C
21	Operating Temperature Range (Die Form)	T_J	-40	+150	°C
22	Storage Temperature Range	T_{STG}	-55	+150	°C
23	Maximum Solder Temperature[10]	T_{SDR}	—	220	°C
24	Moisture Sensitivity Level[11]	MSL	—	3	—

NOTES:

1. For internal digital supply of V_{DDL} = 2.6-V typical.
2. During operation the value of V_{FLASH} must be 5.0 V ± 5%.
3. V_{DDA}=5.0 V ±5%.
4. All 2.6-V input-only pins are 5-V tolerant.
5. Note that long term reliability may be compromised if 2.6-V output drivers drive a node which has been previously pulled to >3.45 V by an external component.
6. Maximum continuous current on I/O pins provided the overall power dissipation is below the power dissipation of the package. Proper operation is not guaranteed at this condition.
7. Condition applies to one pin at a time.
8. Transitions within the limit do not affect device reliability or cause permanent damage. Exceeding limit may cause permanent conversion error on stressed channels and on unstressed channels.
9. Maximum operating temperature on any solder ball in outer four rows of solder balls on the package. These rows are referred to as “Perimeter Balls” to distinguish them from the thermal balls in the center of the package.
10. Solder profile per CDF-AEC-Q100, current revision.
11. Moisture sensitivity per JEDEC test method A112.

Functional operating conditions are given in **E.6 DC Electrical Characteristics**. Ab-

solute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

E.2 Package

The MPC565 / MPC566 is available in two forms, packaged and bumped die. The package is a 388-ball PBGA having a 1.0 mm ball pitch, Motorola case outline 1164-01 (See **Figure 2-5**).

E.3 EMI Characteristics

E.3.1 Reference Documents

The documents referenced for the EMC testing of MPC565 / MPC566 are listed below.

1. The SAE J1752/3 Issued 1995-03
2. The ***MPC555/MPC556UM/AD Users Manual***

E.3.2 Definitions and Acronyms

EMC – Electromagnetic Compatibility

EMI – Electromagnetic Interference

TEM Cell – Transverse Electromagnetic Mode cell

E.3.3 EMI Testing Specifications

1. Scan range: 150 KHz – 1000 MHz
2. Operating Frequency: 56 MHz
3. Operating Voltages: 2.6 V, 5.0 V
4. Max spikes: TBD dBuV
5. I/O port waveforms: Per J1752/3
6. Temperature: 25 °C

E.4 Thermal Characteristics

Table E-2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
BGA Package Thermal Resistance, Junction to Ambient – Natural Convection	$R_{\theta JA}$	TBD[1,2]	°C/W
BGA Package Thermal Resistance, Junction to Ambient – Four layer (2s2p) board, natural convection	$R_{\theta MA}$	TBD[3,4]	°C/W
BGA Package Thermal Resistance, Junction to Board	$R_{\theta JB}$	TBD[5]	°C/W
BGA Package Thermal Resistance, Junction to Case (top)	$R_{\theta JC}$	TBD[6]	°C/W
BGA Package Thermal Resistance, Junction to Package Top, Natural Convection	Ψ_{JC}	TBD[7]	°C/W

NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the board thermal resistance.
2. Per SEMI G38-87 and JESD51-2 with the board horizontal.
3. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the board thermal resistance.
4. Per JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed circuit board (Four layer (2s2p) board, natural convection).
6. Indicates the thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction to ambient resistance (°C/W)

P_D = power dissipation in package

The junction to ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. Unfortunately, the answer is only an estimate; test cases have demonstrated that errors of a factor of two are possible. As a result, more detailed thermal characterization is supplied.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta JA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the air flow can be changed around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where about 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

The simplest thermal model of a package which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction to board and a junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board. temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_B = board temperature (°C)

$R_{\theta JB}$ = package junction to board resistance (°C/W)

P_D = power dissipation in package (W)

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction to board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application (2), or a more accurate and complex model of the package can be used in the thermal simulation. Consultation on the creation of the complex model is available.

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine

the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JA} \times P_D)$$

where:

T_T = thermocouple temperature on top of package (°C)

$R_{\theta JA}$ = thermal characterization parameter

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type-T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

E.4.1 Thermal References

Semiconductor Equipment and Materials International
805 East Middlefield Road
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at ***http://www.jedec.org***

1. C.E. Triplett and B. Joiner, "*An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. B. Joiner and V. Adams, "*Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

E.5 ESD Protection

Table E-3 ESD Protection

Characteristics	Symbol	Value	Units
ESD for Human Body Model (HBM)[1]		2000	V
HBM Circuit Description	R1	1500	W
	C	100	pF
ESD for Machine Model (MM)		200	V
MM Circuit Description	R1	0	W
	C	200	pF
Number of pulses per pin[2] Positive pulses (MM) Negative pulses (MM) Positive pulses (HBM) Negative pulses (HBM)	 — — — —	 3 3 1 1	—
Interval of Pulses	—	1	S

NOTES:

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

E.6 DC Electrical Characteristics

(V_{DDL} = 2.6 V ± 0.1 V, V_{DDH} = 5.0 V ± 0.25 V, $T_A = T_L$ to T_H, $T_B = T_L$ to T_H)

Table E-4 DC Electrical Characteristics

	Characteristic	Symbol	Min	Max	Unit
1	2.6-V only Input High Voltage [1] except DATA[0:31] and EXTCLK	VIH2.6	2.0	V_{DDH} + 0.3	V
1a	2.6-V Input High Voltage EXTCLK	VIHC	1.6	V_{DDH} + 0.3	V
2	DATA[0:31] Precharge Voltage [2]	VDATAPC		3.45	V
3	5-V Input only High Voltage [3]	VIH5	0.7 * V_{DDH}	V_{DDH} + 0.3	V
4	5-V Input High Voltage (QADC PQA, PQB)	VIHA5	0.7 * V_{DDH}	V_{DDA} + 0.3	V
5	MUXed 2.6-V/ 5-V pins (GPIO muxed with Addr and Data) 2.6-V Input High Voltage Addr., Data 5-V Input High Voltage (GPIO)	 VIH2.6M VIH5M	 2.0 0.7 * V_{DDH}	 V_{DDH} + 0.3 V_{DDH} + 0.3	 V V
6	2.6-V Input Low Voltage Except EXTCLK	VIL2.6	V_{SS} – 0.3	0.8	V
7	2.6-V Input Low Voltage EXTCLK	VIL2.6C	V_{SS} – 0.3	0.4	V

Table E-4 DC Electrical Characteristics (Continued)

	Characteristic	Symbol	Min	Max	Unit
8	5-V Input Low Voltage	VIL5	V_{SS} – 0.3	0.48 * V_{DDH}	V
9	5-V Input Low Voltage (QADC PQA, PQB)	VILA5	V_{SSA} – 0.3	0.48 * V_{DDH}	V
10	MUXed 2.6-V/ 5-V pins (GPIO muxed with Addr, Data) 2.6-V Input Low Voltage (Addr., Data) 5-V Input Low Voltage (GPIO)	 VIL2.6M VIL5M	 V_{SS} – 0.3 V_{SS} – 0.3	 0.8 0.48 * V_{DDH}	 V V
11	QADC Analog Input Voltage[4] Note: Assumes $V_{DDA} \geq V_{DDH}$	VINDC	V_{SSH} – 0.3	V_{DDH} + 0.3	V
12	2.6-V Weak Pull-up/down Current [5] pull-up @ VIL2.6, pull-down @ VIH2.6	$I_{ACT2.6V}$	20	130	µA
13	5-V Weak Pull-up/down Current[4] pull-up @ VIL5, pull-down @ VIH5	I_{ACT5V}	20	130	µA
14	2.6-V Input Leakage Current[4] pull-up/down inactive – measured @rails	$I_{INACT2.6V}$	—	2.5	µA
15	5V Input Leakage Current[4] pull-up/down inactive – measured @rails	$I_{INACT5V}$	—	2.5	µA
16	QADC64 Input Current, Channel Off [6] PQA, PQB	I_{OFF}	 -200 -200	 200 200	 nA nA
17	2.6-V Output High Voltage $V_{DD} = V_{DDL}$ (IOH = -2mA)	VOH2.6	2.3	—	V
18	5-V Output High Voltage $V_{DD} = V_{DDH}$ (IOH= -2mA) All 5-V only outputs except TPU.	VOH5	V_{DDH} – 0.7	—	V
19	5-V Output High Voltage $V_{DD} = V_{DDH}$ (IOH= -5mA) For TPU pins Only	VOHTP5	V_{DDH} – 0.65	—	V
20	MUXed 2.6-V/ 5-V pins (GPIO MUXed with Addr, Data) 2.6-V Output High Voltage (IOH = -2mA) 5-V Output High Voltage (IOH = -2mA)	 VOH2.6M VOH5M	 2.3 V_{DDH} – 0.7	—	 V V
21	2.6-V Output Low voltage $V_{DD} = V_{DDL}$ (IOL = 3.2mA)	VOL2.6	—	0.5	V
22	5-V Output Low voltage $V_{DD} = V_{DDH}$ (IOL = 2mA) All 5-V only outputs except TPU	VOL5	—	0.45	V
23	5-V Output Low voltage $V_{DD} = V_{DDH}$ -TPU pins Only IOL = 2mA IOL = 10mA	VOLTP5	—	 0.45 1.0	V
24	MUXed 2.6-V/ 5-V pins (GPIO MUXed with Addr, Data) 2.6-V Output Low Voltage (IOL = 3.2mA) 5-V Output Low Voltage (IOL = 2mA)	 VOL2.6M VOL5M		 0.5 0.45	 V V
25	Output Low Current (@ VOL= 0.4 V)	IOL	2.0	—	mA
26	Output High Current (@ VOH= 2.3 V)	IOH	2.0	—	mA
27	CLKOUT Load Capacitance – SCCR COM & CQDS COM[0:1]= 0b01, CQDS = 0b1 COM[0:1]= 0b01 CQDS = 0b0 COM[0:1]= 0b00 CQDS = 0bx	C_{CLK}	—	 25 50 100	 pF pF pF
29	Capacitance for Input, Output, and Bidirectional Pins: Vin = 0 V, f = 1 MHz (except QADC)	Cin	—	7	pF
30	Load Capacitance for bus pins only [7] COM[0:1] of SCCR = 0b11 COM[0:1] of SCCR = 0b10	CL	—	 25 45	pF

Table E-4 DC Electrical Characteristics (Continued)

	Characteristic	Symbol	Min	Max	Unit
31	Total Input Capacitance PQA Not Sampling PQB Not Sampling	 C_{IN}	 — —	 15 15	pF
32	Hysteresis (Only IRQ, TPU, MIOS, GPIO, QADC (Digital inputs) and RESET) [8]	VH	0.5	—	V
33	Operating Current (2.6-V supplies) @ 40 MHz[9] V_{DDL}/V_{DDI} KAPWR (Crystal Frequency: 20 MHz) $V_{DDSRAM1}$ ($V_{DDSRAM1}$ + $V_{DDSRAM2}$) $V_{DDSRAM3}$ V_{DDSYN} V_{DDRTC} (Crystal Frequency: 32 KHz) V_{DDF} (Read, program, or erase) V_{DDF} (two-module program or erase) $V_{DDFSTOP}$ $V_{DDFDISABLED}$	 I_{DDL} I_{DDKAP} $I_{DDSRAM1}$ $I_{DDSRAM3}$ I_{DDSYN} I_{DDRTC} I_{DDF} $I_{DDFPROG2}$ $I_{DDFSTOP}$ $I_{DDFDISB}$		 200 8 10 30 8 10 60 120 10 100	mA
34	Operating Current (5-V supplies)@ 40 MHz[10] V_{DDH} V_{DDA}[11] $V_{FLASHF5}$ (Program or Erase) $V_{FLASHF5READ}$ $V_{FLASHF5}$ (Stopped) $V_{FLASHF5}$ (Disabled)	 I_{DDH5} I_{DDA} I_{DDF5} I_{DDF5R} SI_{DDF5} SI_{DDF5D}		 21 5 75 7 1 100	mA
35	Operating Current (2.6-V supplies)@ 56 MHz[12] V_{DDL}/V_{DDI} KAPWR $V_{DDSRAM1}$ ($V_{DDSRAM1}$ + $V_{DDSRAM2}$) $V_{DDSRAM3}$ V_{DDSYN} (Crystal Frequency: 20 MHz) V_{DDRTC} (Crystal Frequency: 32 KHz) V_{DDF} (Read, program, or erase) V_{DDF} (2 module program or erase) $V_{DDF\ STOP}$ $V_{DDF\ DISABLED}$	 I_{DDL} I_{DDKAP} $I_{DDSRAM1}$ $I_{DDSRAM3}$ I_{DDSYN} I_{DDRTC} I_{DDF} $I_{DDFPROG2}$ $I_{DDFSTOP}$ $I_{DDFDISB}$		 285 8 10 30 10 10 60 120 10 100	mA
36	Operating Current (5-V supplies)@ 56 MHz[13] V_{DDH} V_{DDA}[14] $V_{FLASHF5}$ (Program or Erase) $V_{FLASHF5READ}$ $V_{FLASHF5}$ (Stopped) $V_{FLASHF5}$ (Disabled)	 I_{DDH5} I_{DDA} I_{DDF5} I_{DDF5R} SI_{DDF5} SI_{DDF5D}		 25 5.0 75 10 1 100	 mA mA mA mA mA mA
37	QADC64 Low Power Stop Mode (V_{DDA})	I_{DDA}		10	µA
38	Low Power Current (V_{DDL}+V_{DDI}+V_{DDF}) @56 MHz DOZE, Active PLL and Active Clocks SLEEP, Active PLL with Clocks off DEEP SLEEP, PLL and Clocks off	 I_{DDDZ} I_{DDSLP} $I_{DDDPSLP}$		 **TBD**[15] **TBD**[15] **TBD**[15]	 mA mA µA

Table E-4 DC Electrical Characteristics (Continued)

	Characteristic	Symbol	Min	Max	Unit
39	V_{DDL}, V_{DDI}, $V_{DDF,}$ Operating Voltage	V_{DDL}, $V_{DDI,}$ $V_{DDF,}$	2.5	2.7	V
40	V_{FLASH} Flash Operating/Programming Voltage	V_{FLASH}	4.75	5.25	V
41	Oscillator, Keep-Alive Registers Operating Voltage[16,17]	KAPWR	V_{DDL}-0.2 V	V_{DDL}+0.2 V	V
42	SRAM Operating Voltage[18]	V_{DDSRAM}	V_{DDL}-0.2 V	V_{DDL}+ 0.2 V	V
43	V_{DDH} Operating Voltage	V_{DDH}	4.75	5.25	V
44	QADC Operating Voltage	V_{DDA}	4.75	5.25	V
45	Clock Synthesizer Operating Voltage[17]	V_{DDSYN}	V_{DDL} – 0.2 V	V_{DDL} + 0.2 V	V
46	Real Time Clock Operating Voltage[17]	V_{DDRTC}	V_{DDL} – 0.2 V	V_{DDL}+ 0.2 V	V
47	V_{SS} Differential Voltage	V_{SS} – V_{SSA}	-100	100	mV
48	QADC64 Reference Voltage Low[19]	V_{RL}	V_{SSA}	V_{SSA} + 0.1	V
49	QADC64 Reference Voltage High[19]	V_{RH}	3.0	V_{DDA}	V
50	QADC64 V_{REF} Differential Voltage	V_{RH} – V_{RL}	3.0	5.25	V
51	QADC64 Reference Supply Current, DC QADC64 Reference Supply Current, Transient	I_{REF} I_{REF}	— —	500 4.0	µA mA
52	QADC64 ALT Reference Voltage	V_{ARH}	.25 * V_{DDA}	.75 * V_{DDA}	V
53	Standby Supply Current[4] KAPWR only V_{DDRTC} RAM Standby Current (CALRAM) $V_{DDSRAM1}$ RAM Standby Current (CALRAM) $V_{DDSRAM2}$ RAM Standby Current (DPTRAM)$V_{DDSRAM3}$ Measured @ 2.7 V	 ISB_{KAPWR} ISB_{RTC} ISB_{SRAM1} ISB_{SRAM2} ISB_{SRAM3}		 5 50 250 100 100	 mA µA µA µA µA
53a	RAM Standby Voltage for Data Retention Applies to $V_{DDSRAM1}$ $V_{DDSRAM2}$ and $V_{DDSRAM3}$ (power-down Mode)[4] Specified V_{DD} applied (V_{DD} = V_{SS})	V_{STBY}	1.4[20, 21]	2.7	V
54	DC Injection Current per Pin GPIO, TPU, MIOS, QSM, EPEE and 5 V [4, 22]	I_{IC5}	-1.0	1.0	mA
55	DC Injection Current per Pin 2.6 V [4, 23, 24]	I_{IC3}	-1.0	1.0	mA
56	QADC64 Disruptive Input Current [25]	I_{NA}	- 3	3	mA
57	Power Dissipation – 56 MHz 40 MHz	PD		1.12 0.8	W W

NOTES:

1. This characteristic is for 2.6-V output and 5-V input friendly pins.
2. VDATAPC is the max voltage the data pins can have been precharged to by an external device when the MPC565 / MPC566 data pins turn on as outputs. The 3.45-V max for VDATAPC is to allow the data pins to be driven from an external memory running at a higher voltage. Note that if the data pins are precharged to higher than V_{DDL}, then the 50-pF max. load characteristic must be observed.
3. This characteristic is for 5-V output and 5-V input pins.
4. Within this range, no significant injection will be seen. See QADC64 Disruptive Input Current (I_{NA}).
5. After characterization this value may be improved.
6. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each eight to 12 °C, in the ambient temperature range of 50 to 125 °C.
7. All bus pins support two drive strengths capabilities, 25 pF and 50 pF. Current drive is less at the 25-pF capacitive load. Both modes achieve 40-MHz (or, optionally, 56-MHz) timing.

8. Only IRQ, TPU, MIOS, GPIO, QADC (when digital inputs) and RESET pins have hysteresis, thus there is no hysteresis specification required for all other pins
9. Values to be characterized. Current consumption values will be updated as information becomes available. Initial values are only estimates based on predicted capacitive differences between CDR1 and CDR3 as well as actual CDR1 measurements.
10. Values to be characterized. Current measured at maximum system clock frequency with QADC active.
11. Current measured at maximum system clock frequency with QADC active.
12. All power consumption specifications assume 50-pF loads and running a typical application. Of the power consumption of some modules could go up is they are exercised heavier, but the power consumption of other modules would decrease.
13. Values to be characterized. Current measured at maximum system clock frequency with QADC active.
14. Current measured at maximum system clock frequency with QADC active.
15. Pending characterization.
16. KAPWR and V_{DDSRAM} are powered-up prior to any other supply.
17. This parameter is periodically sampled rather than 100% tested
18. KAPWR and V_{DDSRAM} are powered-up prior to any other supply.
19. To obtain full-range results, $V_{SSA} \leq V_{RL} \leq V_{INDC} \leq V_{RH} \leq V_{DDA}$
20. The voltage at which the LVSRS bits in the VSRAMCR register will be set ranges from TBD to TBD volts. V_{STBY} should remain above TBD volts to prevent LVSRS bits to be set.
21. This parameter is guaranteed by design.
22. All injection current is transferred to the V_{DDH}. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
23. Total injection current for all I/O pins on the chip must not exceed 20 μA. Exceeding this limit can cause disruption of normal operation.
24. Current refers to two QADC64 modules operating simultaneously.
25. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

E.7 Oscillator and PLL Electrical Characteristics

Table E-5 Oscillator and PLL

PIN	Characteristic	Symbol	Min	Typical	Max	Unit
1	Oscillator Startup time (for typical crystal capacitive load) 4-MHz crystal 20-MHz crystal	 OSCstart4 OSCstart20			 10 10	 mS mS
2	PLL Lock Time	T_{LOCK}			500[1]	Input Clocks
3	PLL Operating Range	F_{VCOOUT}	30		112	MHz
4	Crystal Operating Range, MODCK=0b010,0b110 MODCK[1:3] = 0b001, 0b011, 0b100, 0b101, 0b111)	$F_{CRYSTAL}$	2 15		5 25	MHz MHz
5	PLL Jitter PLL Jitter (averaged over 10 µs)	F_{JIT} F_{JIT10}	-1% -0.3%		+1% +0.3%	—
6	Limp Mode Clock Out Frequency	—	**3**[2]	7	**12**[1]	MHz
7	Oscillator Bias Current (XTAL) 4 MHz 20 MHz	I_{BIAS}	**TBD**[3] **TBD**[2]		 — —	 mA mA
8	Oscillator Drive (XTAL)	Iosc	**TBD**[2]		—	mA
9	Oscillator Bias Resistor	R_{OSC}	**TBD**[2]	1	**TBD**[2]	MΩ

NOTES:
1. Assumes stable power and oscillator.
2. Estimated value, real values to be characterized and updated.
3. Values to be characterized.

E.8 Flash Electrical Characteristic

Table E-6 Array Program and Erase Characteristics

(V_{DDF} = 2.6 V ± 0.1 V, V_{FLASH} = 5.0 V ± 0.25 V, $T_A = T_L$ to T_H, $T_B = T_L$ to T_H)

Symbol	Meaning	Value		
		Minimum	Typical[1]	Maximum
T_{ERASE}	Block or Module Erase Time[2]		0.7 s	15 s
T_{PROG}	Word Programming Time[3]		15 µs	300 µs

NOTES:
1. Typical program and erase times assume nominal supply values and 25 °C.
2. Erase time specification does not include pre-programming operation
3. Word size is.32 bits.

Table E-7 CENSOR Cell Program and Erase Characteristics

(V_{DDF} = 2.6 V ± 0.1 V, V_{FLASH} = 5.0 V ± 0.25 V, T_A = T_L to T_H, T_B = T_L to T_H)

Symbol	Meaning	Value		
		Minimum	Typical[1]	Maximum
T_{CLEAR}	CENSOR Bit Clear Time[2]		TBD	
T_{SET}	CENSOR bit Set Time		TBD	

NOTES:
1. Typical set and clear times assume nominal supply values and 25C.
2. Clear time specification does not include pre-set operation.

Table E-8 Module Life

Symbol	Meaning	Value
Array P/E Cycles[1]	Maximum number of Program/Erase cycles per block to guarantee data retention.	1,000
CENSOR Set/Clear Cycles[2]	Minimum number of Program/Erase cycles per bit before failure.	100
Array and CENSOR Data Retention	Minimum data retention at 85 °C.	Min 10 years

NOTES:
1. A Program/Erase cycle is defined as switching the bits from 1 to 0 to 1.
2. A CENSOR Set/Clear cycle is defined as switching the bits from 1 to 0 to 1.

E.9 Power-Up/Down Sequencing

This section applies to only CDR3 devices such as MPC565 / MPC566.

The supply symbols used in this section are described in **Table E-9**.

Table E-9 MPC565 / MPC566 Power Supply Pin Groups

Symbol	Types of Power Pins
V_{DDHI} (High Voltage Supply Group)	Supply to the 5-V pads for output driver (V_{DDH})
	Supply to the analog (QADC64E) circuitry (V_{DDA})
	High voltage supply to the flash module (V_{FLASH})
V_{DDLO} (Low Voltage Supply Pins)	Supply to low voltage pad drivers (QVDDL, NVDDL)
	Supply to all low voltage internal logic (V_{DD})
	Supply to low voltage flash circuitry (V_{DDF})
	Supply to system PLL and other circuitry required for keep-alive functions (KAPWR, V_{DDSYN})
V_{DDKA} (Low Voltage Keep-Alive Supply Pins[1]	Supply to SRAM arrays only ($V_{DDSRAM1}$, $V_{DDSRAM2}$, $V_{DDSRAM3}$)
	Supply to low power counter and 32 KHz crystal (V_{DDRTC})

NOTES:
1. Any supply in the V_{DDKA} group can be powered with the V_{DDLO} if the function which it supplies is not required during “Keep-alive”.

There are two power-up/down options. Choosing which one is required for an application will depend upon circuitry connected to 2.6-V compliant pins and dual 2.6-V/5-V compliant pins. power-up/down option A is required if 2.6-V compliant pins and dual 2.6-V/5-V compliant pins are connected to the 5-V supply with a pull-up resistor or driven by 5-V logic during power-up/down. In applications for which this scenario is not true the power-up/down option B may be implemented. Option B is less stringent and easier to ensure over a variety of applications.

Refer to **Table 2-1** for a list of 2.6 V and dual 2.6V/5 V compliant pins.

Power consumption during power-up/down sequencing can not be specified prior to evaluation and characterization of production silicon. It is Motorola’s intention to keep the power consumption during power-up/down sequencing below the operating power consumption when following these guidelines.

E.9.1 Power-Up/Down Option A

The Option A power-up sequence (excluding V_{DDKA}) is

1. $V_{DDHI} \leftarrow V_{DDLO}$ + 3.1 V (V_{DDHI} cannot lead V_{DDLO} by more than 3.1 V)
2. $V_{DDHI} > V_{DDLO}$ - 0.5 V (V_{DDHI} cannot lag V_{DDLO} by more than 0.5 V)

Requirement ‘1’ is due to gate-to-drain stress limits for transistors in the pads of 2.6-V compliant pins and dual 2.6-V/5-V compliant pins. Damage can occur if gate-to-drain voltage potential is greater than 3.1 V. This is only a concern at power-up/down. Requirement ‘2’ is due to ESD diodes in the pad logic for dual 2.6-V/5-V compliant pins. The diodes are forward biased when V_{DDLO} is greater than V_{DDHI} and will start to conduct current.

Figure E-1 illustrates the power-up sequence if no keep-alive supply is required. **Figure E-2** illustrates the power-up sequence if a keep-alive supply is required. The keep-

alive supply should be powered-up at the same instant or before both the high voltage and low voltage supplies are powered-up.

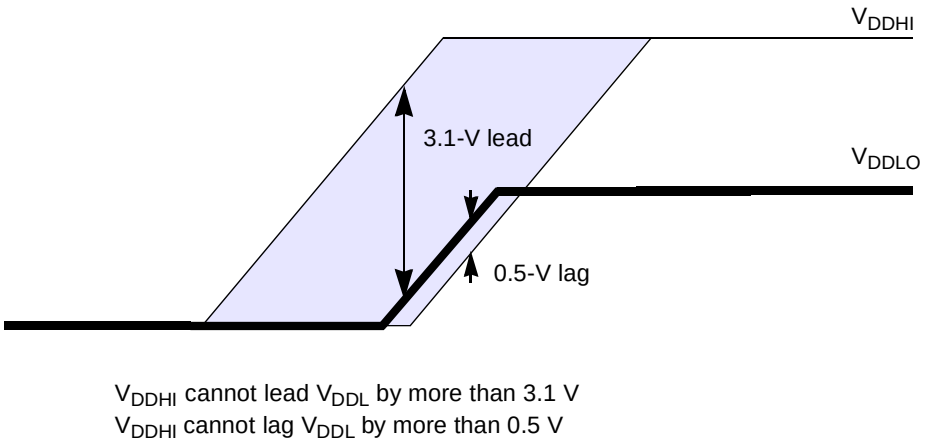


Figure E-1 Option A Power-Up Sequence Without Keep-Alive Supply

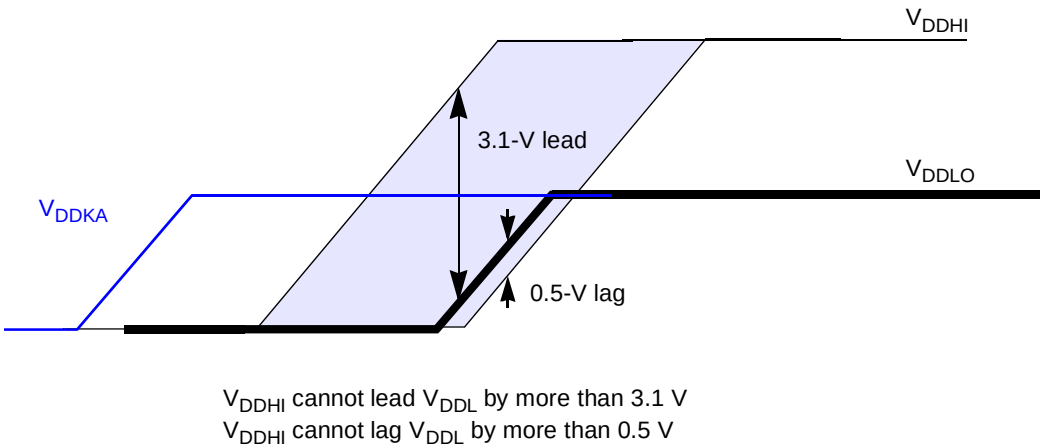


Figure E-2 Option A Power-Up Sequence With Keep-Alive Supply

The option A power-down sequence (excluding V_{DDKA}) is

1. $V_{DDHI} \leftarrow V_{DDLO}$ + 3.1 V (V_{DDHI} cannot lag V_{DDL} by more than 3.1 V)
2. V_{DDLO} crossover should occur at 0.5 V or less

Figure E-3 illustrates the power-down sequence if no keep-alive supply is required. **Figure E-4** illustrates the power-down sequence if a keep-alive supply is required.

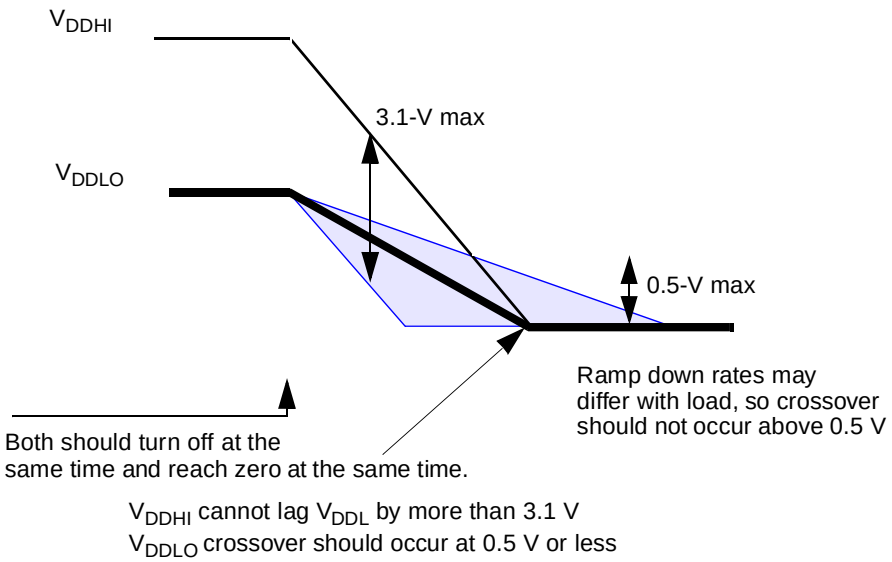


Figure E-3 Option A Power-Down Sequence Without Keep-Alive Supply

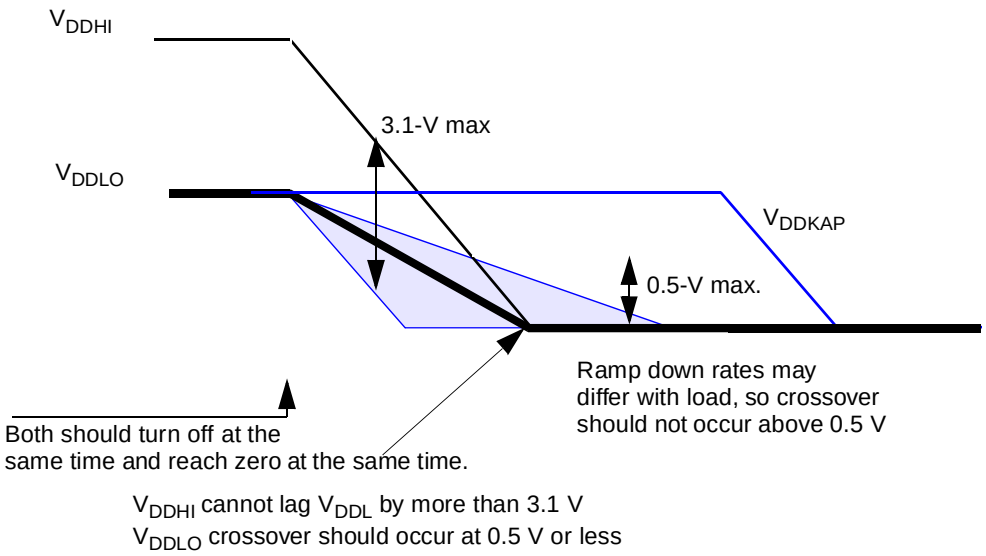


Figure E-4 Option A Power-Down Sequence With Keep-Alive Supply

E.9.2 Power-Up/Down Option B

A less stringent power-up sequence may be implemented if 2.6-V compliant pins and dual 2.6-V/5-V compliant pins are NOT connected to the 5-V supply with a pull-up resistor or driven by 5-V logic during power-up/down.

The option B power-up sequence (excluding V_{DDKA}) is:

$V_{DDHI} > V_{DDLO}$ - 0.5 V (V_{DDHI} cannot lag V_{DDLO} by more than 0.5 V)

Thus the V_{DDHI} supply group can be fully powered-up prior to power-up of the V_{DDLO} supply group, with no adverse affects to the device.

The requirement that V_{DDHI} cannot lag V_{DDLO} by more than 0.5 V is due to ESD diodes in the pad logic for dual 2.6-V/5-V compliant pins. The diodes are forward biased when V_{DDLO} is greater than V_{DDHI} and will start to conduct current.

Figure E-5 illustrates the power-up sequence if no keep-alive supply is required. **Figure E-6** illustrates the power-up sequence if a keep-alive supply is required. The keep-alive supply should be powered-up at the same instant or before both the high voltage and low voltage supplies are powered-up.

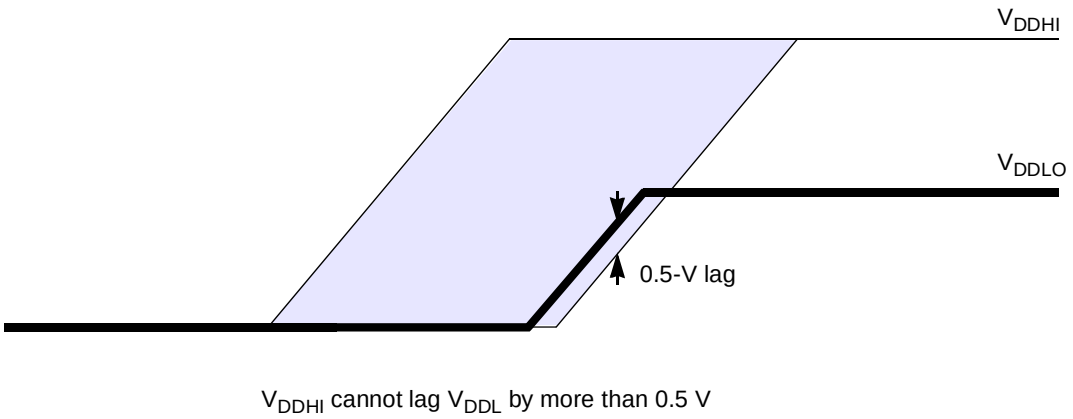


Figure E-5 Option B Power-Up Sequence Without Keep-Alive Supply

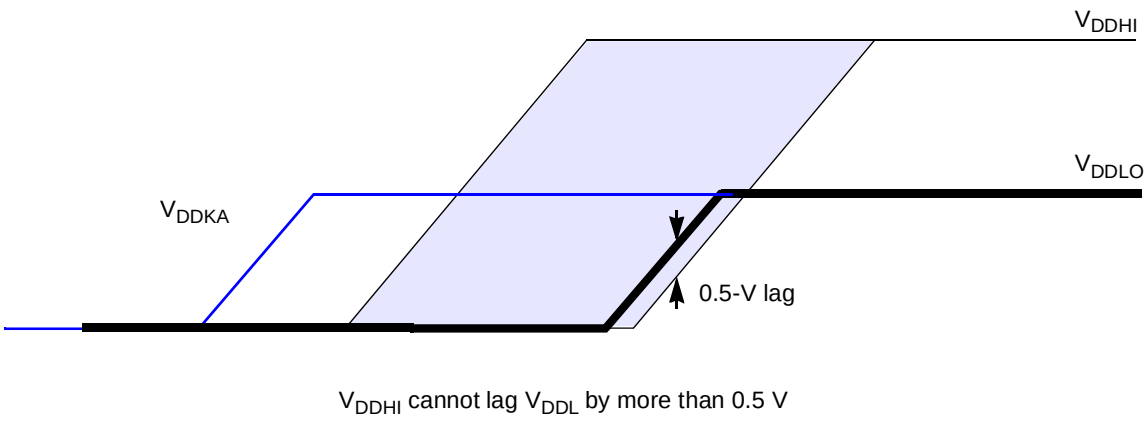


Figure E-6 Option B Power-Up Sequence With Keep-Alive Supply

The option B power-down sequence (excluding V_{DDKA}) is:

V_{DDLO} crossover should occur at 0.5 V or less

Thus the V_{DDLO} supply group can be fully powered-down prior to power-down of the V_{DDHI} supply group, with no adverse affects to the device.

For power-down, the low voltage supply should come down before the high voltage supply, although with varying loads, the high voltage may actually get ahead.

Figure E-7 illustrates the power-down sequence if no keep-alive supply is required. **Figure E-8** illustrates the power-down sequence if a keep-alive supply is required.

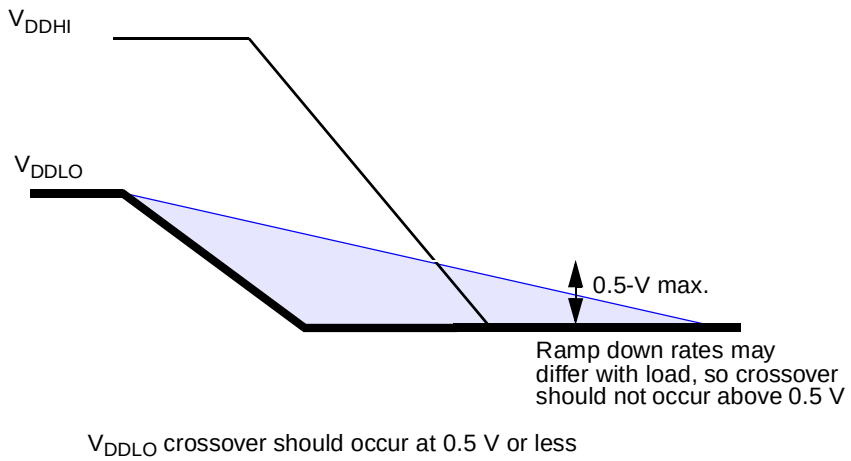


Figure E-7 Option B Power-Down Sequence Without Keep-Alive Supply

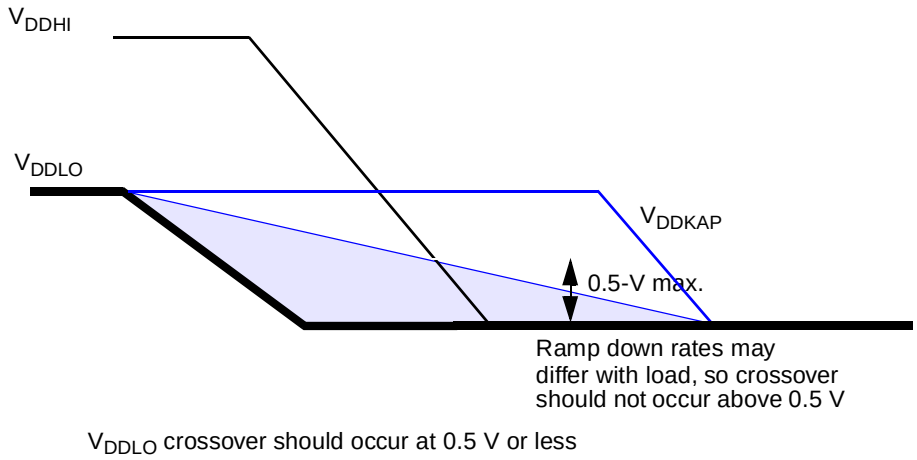


Figure E-8 Option B Power-Down Sequence with Keep-Alive Supply

E.10 Issues Regarding Power Sequence

E.10.1 Flash Issue

The $\overline{\text{PORESET}}$ signal must be asserted during power-up before the low voltage supply is above 0.5 V. If the $\overline{\text{PORESET}}$ signal is not asserted before this condition, there is a possibility of disturbing the programmed state of the flash.

E.10.2 Keep-Alive RAM

This issue should be addressed on all MPC5XX devices in both CDR1 and CDR3.

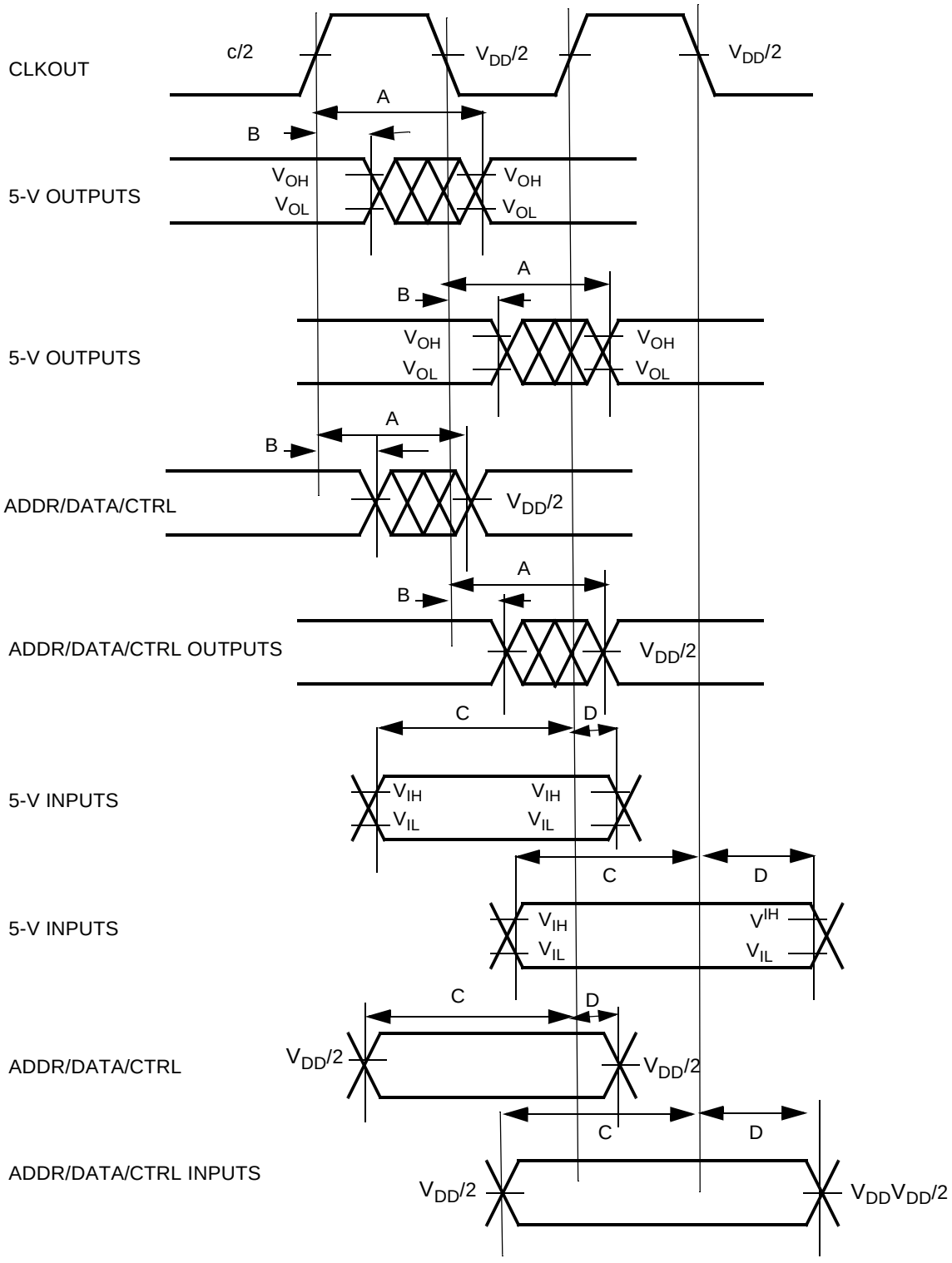
$\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ must be asserted during power-down prior to any supply dropping out of specified operating conditions.

An additional constraint is placed on $\overline{\text{PORESET}}$ assertion since it is an asynchronous input. To assure that the assertion of $\overline{\text{PORESET}}$ does not potentially cause stores to keep-alive RAM to be corrupted (store single or store multiple) or non-coherent (store multiple), either of the following solutions is recommended:

1. Assert $\overline{\text{HRESET}}$ at least 0.5 µs prior when $\overline{\text{PORESET}}$ is asserted.
2. Assert $\overline{\text{IRQ0}}$ (non-maskable interrupt) at least 0.5 µs prior when $\overline{\text{PORESET}}$ is asserted. The service routine for $\overline{\text{IRQ0}}$ should not perform any writes to keep-alive RAM.

The amount of delay which should be added to $\overline{\text{PORESET}}$ assertion is dependent upon the frequency of operation and the maximum number of store multiples executed that are required to be coherent. If store multiples of more that 28 registers are needed and if the frequency of operation is lower that 56 MHz, the delay added to $\overline{\text{PORESET}}$ assertion will need to be greater than 0.5 µs.

E.11 Timing



A. Maximum Output Delay Specification
B. Minimum Output Hold Time
C. Minimum input Setup Time Specification
D. Minimum input Hold Time Specification

Figure E-9 Generic Timing Examples

Table E-10 Bus Operation Timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
1	CLKOUT Period	TC	25		17.86		ns
1a	ENGCLK Frequency 5 V – EECLK = 01 2. 6 V – EECLK = 00			 10 40		 10 56	MHz
2	Clock pulse width low		12.5 –2%	12.5 + 2%	8.93 –2%	8.93 + 2%	ns
3	Clock pulse width high		12.5 – 2%	12.5 + 2%	8.93 – 2%	8.93 + 2%	ns
4	CLKOUT rise time ABUS/DBUS rise time			3.5 3.0		3.5 3.0	ns
5	CLKOUT fall time ABUS/DBUS rise time			3.5 3.0		3.5 3.0	ns
6	Circuit Parameter	TCC	7		5		ns
7	CLKOUT to Signal Invalid (Hold Time) A[0:31] RD/$\overline{WR}$ $\overline{BURST}$ D[0:31]	0.25TC – 1.25	5		5		ns
7a	CLKOUT to Signal Invalid: (Hold Time) TSIZ[0:1] $\overline{RSV}$ AT[0:3] $\overline{BDIP}$ PTR $\overline{RETRY}$	0.25TC – 1.25	5		5		ns
7b	CLKOUT to Signal Invalid (Hold Time)[2] $\overline{BR}$ $\overline{BG}$ FRZ VFLS[0:1] VF[0:2] IWP(0:2] LWP[0:1] $\overline{STS}$[3]	0.25TC –- 1.25	5		5		ns
7c	Slave mode CLKOUT to Signal Invalid D[0:31]	**0.25TC+TCC**	7		6.5		ns
8	CLKOUT to Signal Valid A[0:31] RD/$\overline{WR}$ BURST D[0:31][4]	0.25TC + TCC	6.25	13	4.5	10	ns

Table E-10 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
8a	CLKOUT to Signal Valid TSIZ[0:1] $\overline{RSV}$ AT[0:3] $\overline{BDIP}$ PTR $\overline{RETRY}$	0.25TC + TCC	6.25	13	4.5	9.5	ns
8b	CLKOUT to Signal Valid[2] $\overline{BR}$ $\overline{BG}$ VFLS[0:1] VF[0:2] IWP[0:2] FRZ LWP[0:1] $\overline{STS}$ valid.	0.25TC + TCC	6.25	13	4.5	9.5	ns
8c	Slave Mode CLKOUT to Signal Valid D[0:31]	0.25TC + TCC + 4		14		14	ns
9	CLKOUT to High Z A[0:31] RD/$\overline{WR}$ BURST D[0:31] TSIZ[0:1] $\overline{RSV}$ AT[0:3] PTR $\overline{RETRY}$	0.25TC + TCC	6.25	13	4.5	9.5	ns
10	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion	0.25TC + TCC	6.25	13	4.5	9.5	ns
10a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the Memory Controller)	—		10		10	ns
10b	CLKOUT to $\overline{RETRY}$ assertion (when driven by the Memory Controller)	—		10		10	ns
11	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation	0.25TC + TCC	6.25	13	4.5	9.5	ns
11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the Memory Controller)	—		11		11	ns
11b	CLKOUT to $\overline{RETRY}$ negation (when driven by the Memory Controller)	—		11		11	ns
12	CLKOUT to $\overline{TS}$, $\overline{BB}$ High Z	0.25TC +14	6.25	20	4.5	16	ns
12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High Z (when driven by the Memory Controller)			15		15	ns
13	CLKOUT to $\overline{TEA}$ assertion	—		11		11	ns
14	CLKOUT to $\overline{TEA}$ High Z			15		15	ns

Table E-10 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
15	Input Valid to CLKOUT (Setup Time) $\overline{TA}$ $\overline{TEA}$ $\overline{BI}$[3]		12		8.5		ns
15a	Input Valid to CLKOUT (Setup Time) $\overline{KR}$ $\overline{CR}$ $\overline{RETRY}$		10		7.25		ns
15b	Input Valid to CLKOUT (Setup Time) $\overline{BB}$ $\overline{BG}$ $\overline{BR}$[2]		7		5		ns
16	CLKOUT to Signal Invalid (Hold Time) $\overline{TA}$ $\overline{TEA}$ $\overline{BI}$ $\overline{BB}$ $\overline{BG}$ $\overline{BR}$[2, 3]		2		2		ns
16a	CLKOUT to Signal Invalid (Hold Time) $\overline{RETRY}$ $\overline{KR}$ $\overline{CR}$		2		2		ns
17	Signal Valid to CLKOUT Rising Edge (Setup Time) D[0:31][4]		6		6		ns
18	CLKOUT Rising Edge to Signal Invalid (Hold Time) D[0:31][4]		1		.71		ns
19	CLKOUT Rising Edge to $\overline{CS}$ asserted -GPCM- ACS = 00	0.25TC + TCC + 1	6.25	14	5.5	10.5	ns
19a	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 0 or 1	TCC + 1		8		6	ns
19b	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0 or 1	0.25TC + TCC + 1	6.25	14	5.5	10.5	ns
19c	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1	**0.375TC+TCC+1**	6.25	17	6.69	12.69	ns

Table E-10 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
20	CLKOUT Rising Edge to $\overline{CS}$ negated -GPCM- Read Access or Write access when CSNT = 0 or write access when CSNT = 1 and ACS = 00	TCC + 1	1	8	1	6	ns
21	A[0:31] to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 0		3		2.25		ns
21a	A[0:31] to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0		8		5.71		ns
22	CLKOUT Rising Edge to $\overline{OE}$, $\overline{WE[0:3]}$ asserted			8		5.71	ns
23	CLKOUT Rising Edge to $\overline{OE}$ n egated		1	8	0.71	5.71	ns
24	A[0:31] to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 1		23		16.42		ns
24a	A[0:31] to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 1		28		20		ns
25	CLKOUT Rising Edge to $\overline{WE[0:3]}$ negated -GPCM-write access CSNT = '0'			6		4.5	ns
25a	CLKOUT Falling Edge to $\overline{WE[0:3]}$ negated -GPCM-write access TRLX = '0' or '1', CSNT = '1, EBDF = 0'.	0.25TC + TCC + 1	6.25	14	5.5	10.5	ns
25b	CLKOUT Falling Edge to $\overline{CS}$ negated -GPCM-write access TRLX = '0' or '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0	0.25TC + TCC + 1	6.25	14	5.5	10.5	ns
25c	CLKOUT Falling Edge to $\overline{WE[0:3]}$ negated -GPCM-write access TRLX = '0', CSNT = '1, EBDF = 1'.	0.375TC + TCC + 1	6.25	17	5.5	12.69	ns
25d	CLKOUT Falling Edge to $\overline{CS}$ negated -GPCM-write access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	0.375TC + TCC + 1	6.25	17	6.25	17	ns

Table E-10 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
26	$\overline{WE}$[0:3] negated to D[0:31] High Z -GPCM- write access, CSNT = '0'		3		2.25		ns
26a	$\overline{WE}$[0:3] negated to D[0:31] High Z -GPCM- write access, TRLX = '0', CSNT = '1', EBDF = 0		8		5.71		ns
26b	$\overline{CS}$ negated to D[0:31], High Z -GPCM- write access, ACS = '00', TRLX = '0' & CSNT = '0'		3		2.25		ns
26c	$\overline{CS}$ negated to D[0:31], High Z -GPCM- write access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0		8		5.71		ns
26d	$\overline{WE}$[0:3] negated to D[0:31] High Z -GPCM- write access, TRLX = '1', CSNT = '1', EBDF = 0		28		20		ns
26e	$\overline{CS}$ negated to D[0:31] High Z -GPCM- write access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0		28		20		ns
26f	$\overline{WE}$[0:3] negated to D[0:31] HighZ -GPCM- write access, TRLX = '0', CSNT = '1', EBDF = 1		5		3.75		ns
26g	$\overline{CS}$ negated to D[0:31] High Z -GPCM- write access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1		5		3.75		ns
26h	$\overline{WE}$[0:3] negated to D[0:31] High Z -GPCM- write access, TRLX = '1', CSNT = '1', EBDF = 1		24		17.25		ns
26i	$\overline{CS}$ negated to D[0:31] High Z -GPCM- write access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1		24		17.25		ns
27	$\overline{CS}$, $\overline{WE}$[0:3] negated to A[0:31] invalid -GPCM- write access[5]		3		2.25		ns

Table E-10 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
27a	$\overline{WE}$[0:3] negated to A[0:31] Invalid -GPCM- write access, TRLX='0', CSNT = '1'. $\overline{CS}$ negated to A[0:31] Invalid -GPCM- write access, TRLX='0', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 0		8		5.71		ns
27b	$\overline{WE}$[0:3] negated to A[0:31] Invalid -GPCM- write access, TRLX='1', CSNT = '1'. $\overline{CS}$ negated to A[0:31] Invalid -GPCM- write access, TRLX='1', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 0		28		20		ns
27c	$\overline{WE}$[0:3] negated to A[0:31] in-valid -GPCM- write access, TRLX='0', CSNT = '1'. $\overline{CS}$ negated to A[0:31] Invalid -GPCM- write ac-cess, TRLX='0', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 1		4		3		ns
27d	$\overline{WE}$[0:3] negated to A[0:31] Invalid -GPCM- write access, TRLX='1', CSNT = '1'. CS negated to A[0:31] Invalid -GPCM- write ac-cess, TRLX='1', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 1		24		17.25		ns
28	A[0:31], TSIZ[0:1], RD/$\overline{WR}$, $\overline{BURST}$, $\overline{BDIP}$ valid to CLKOUT Rising Edge. (Slave mode Setup Time)		11		8		ns
28a	Slave Mode D[0:31] valid to CLKOUT Rising Edge		7		7		ns

Table E-10 Bus Operation Timing (Continued)

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz[1]		Unit
			Min	Max	Min	Max	
29	$\overline{TS}$ valid to CLKOUT Rising Edge (Setup Time)		7		5		ns
30	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time).		2		2		ns

NOTES:

1. 56-MHz operation is available as an option. Some parts (without the 56-MHz option) will operate at a maximum frequency of 40 MHz.
2. The timing for $\overline{BR}$ output is relevant when the MPC565 / MPC566 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC565 / MPC566 is selected to work with internal bus arbiter.
3. The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by the external device (and not the memory controller).
4. The maximum value of spec 8 for DATA[0:31] pins must be extended by 1.1 ns if the pins have been precharged to greater than V_{DDL}. This is the case if an external slave device on the bus is running at the max. value of VDATAPC. This is currently specified at 3.45 V. The 1.1 ns addition to spec 8 reflectls the expected timing degradation for 3.45 V.
5. The timing 27 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE}$[0:3] when CSNT = '0'.

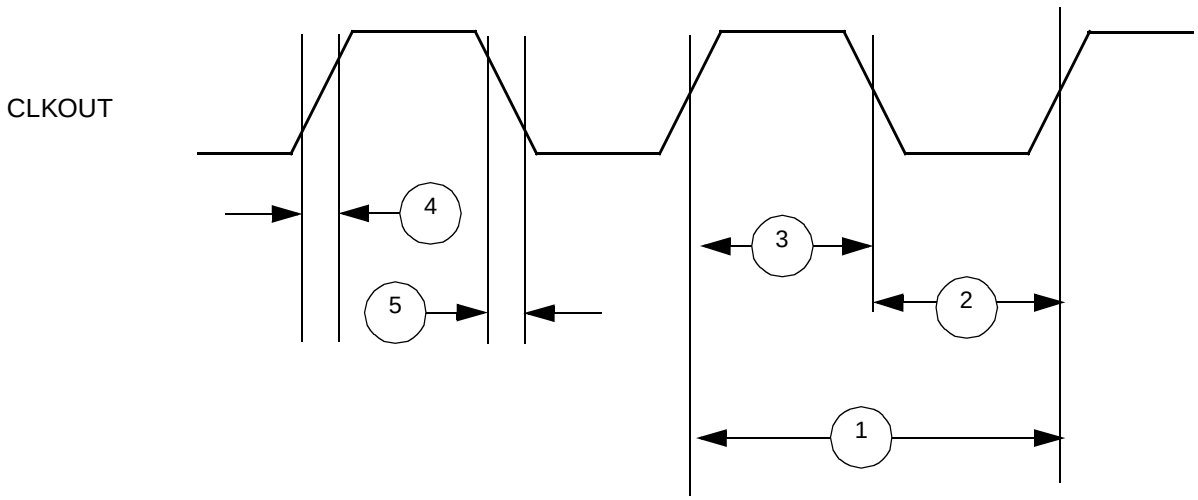


Figure E-10 CLKOUT Pin Timing

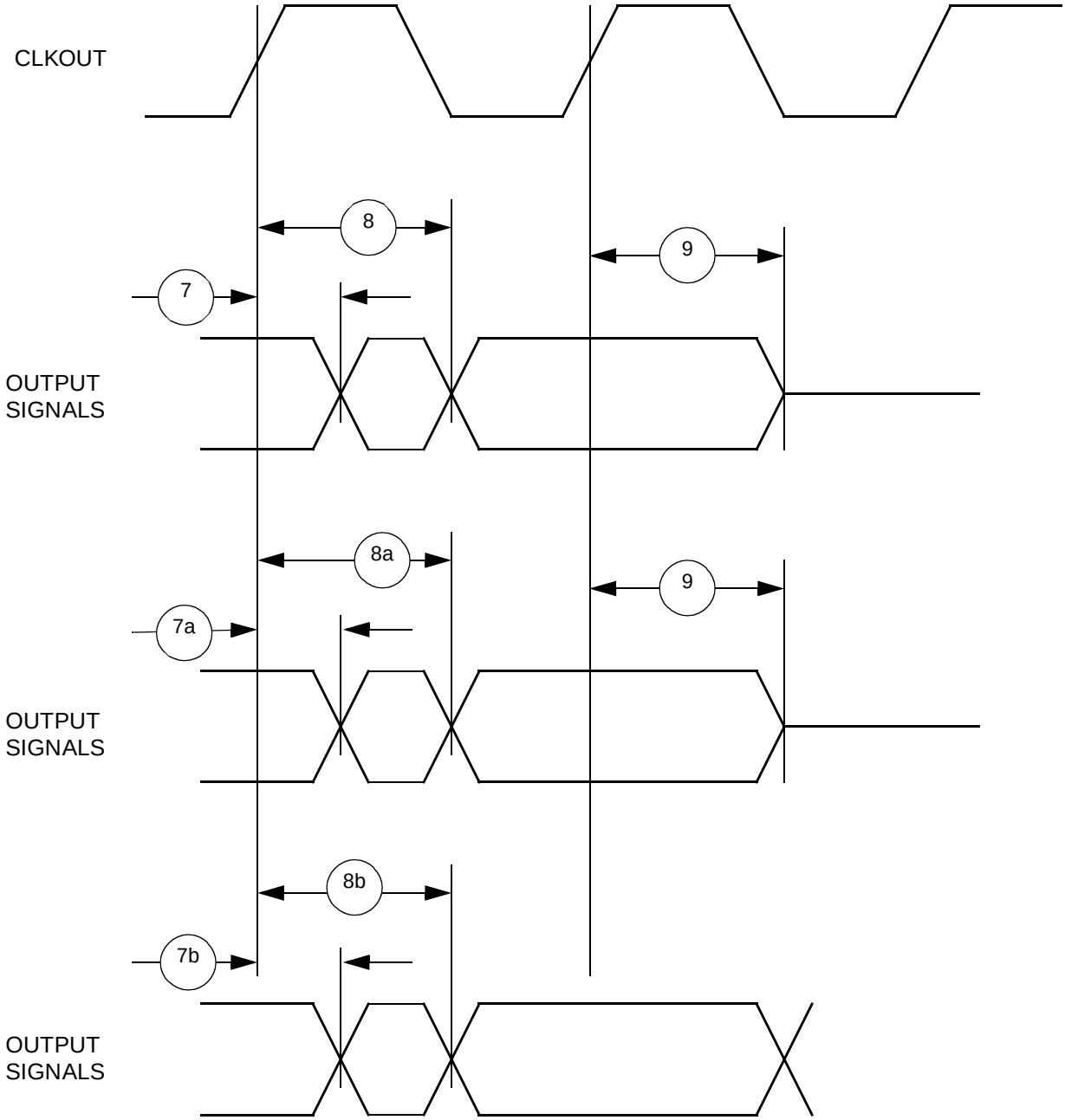


Figure E-11 Synchronous Output Signals Timing

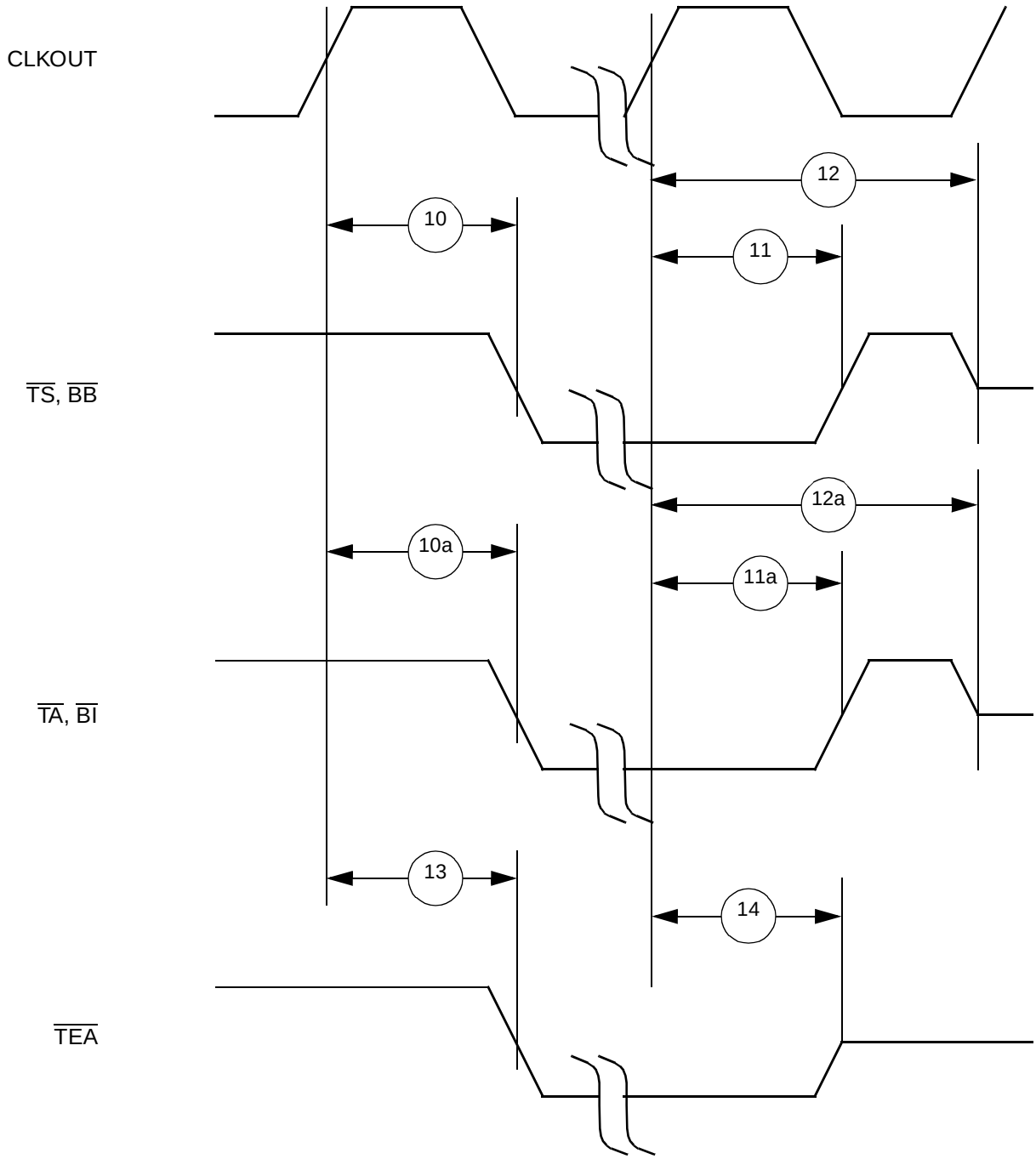


Figure E-12 Synchronous Active Pull-Up And Open Drain Outputs Signals Timing

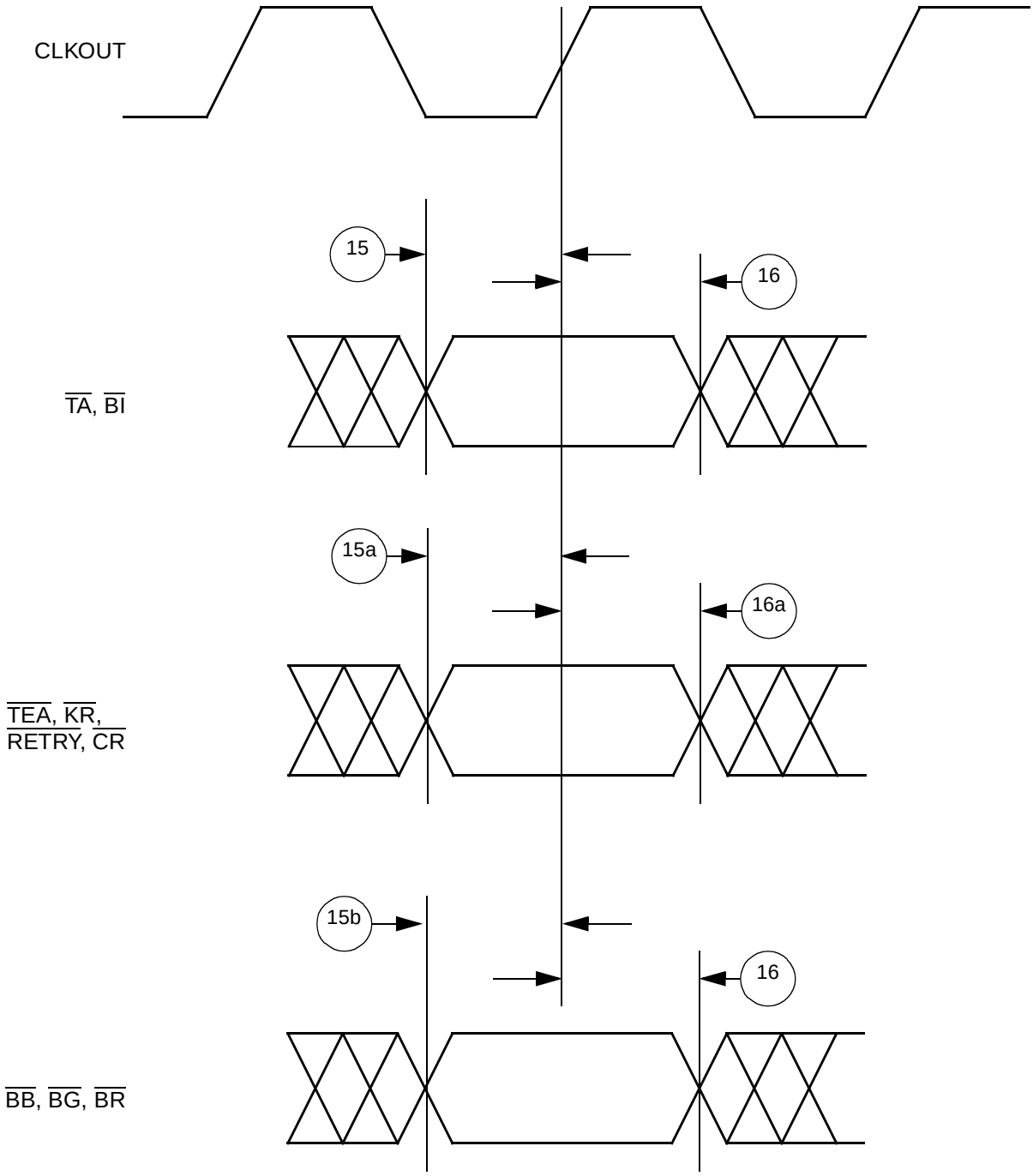


Figure E-13 Synchronous Input Signals Timing

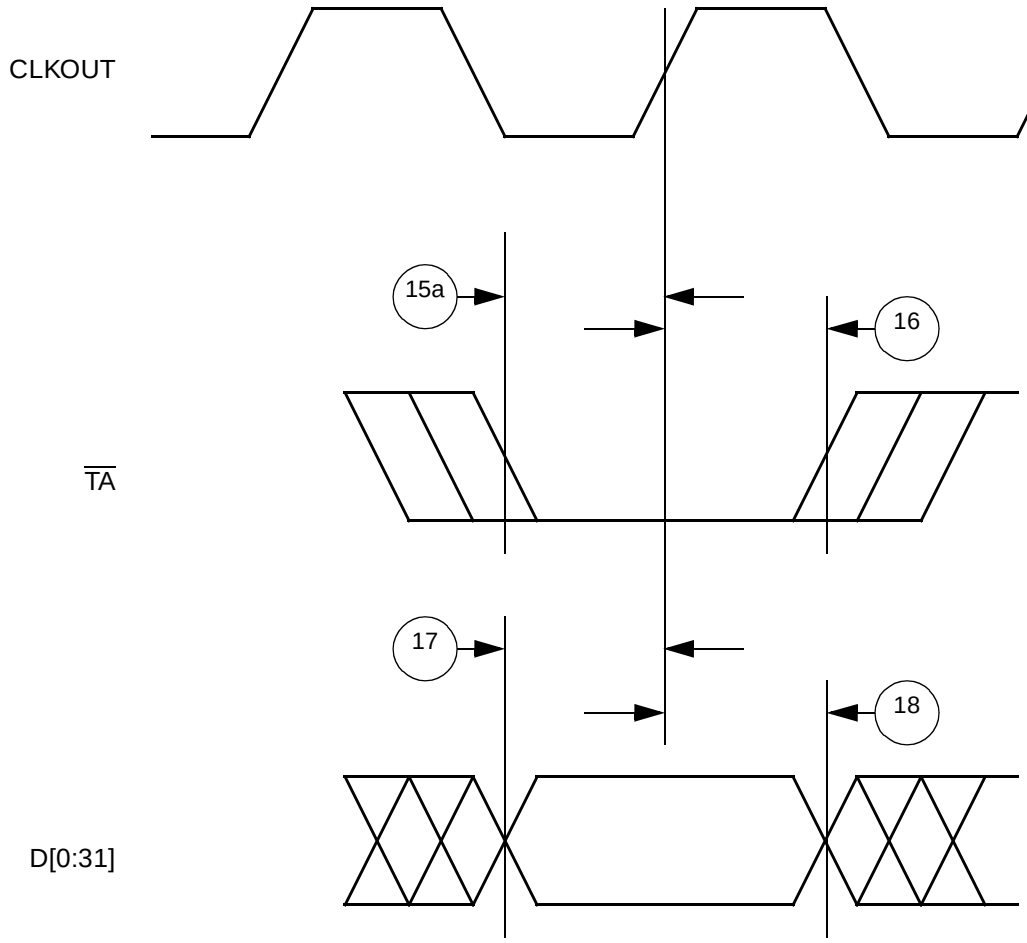


Figure E-14 Input Data Timing In Normal Case

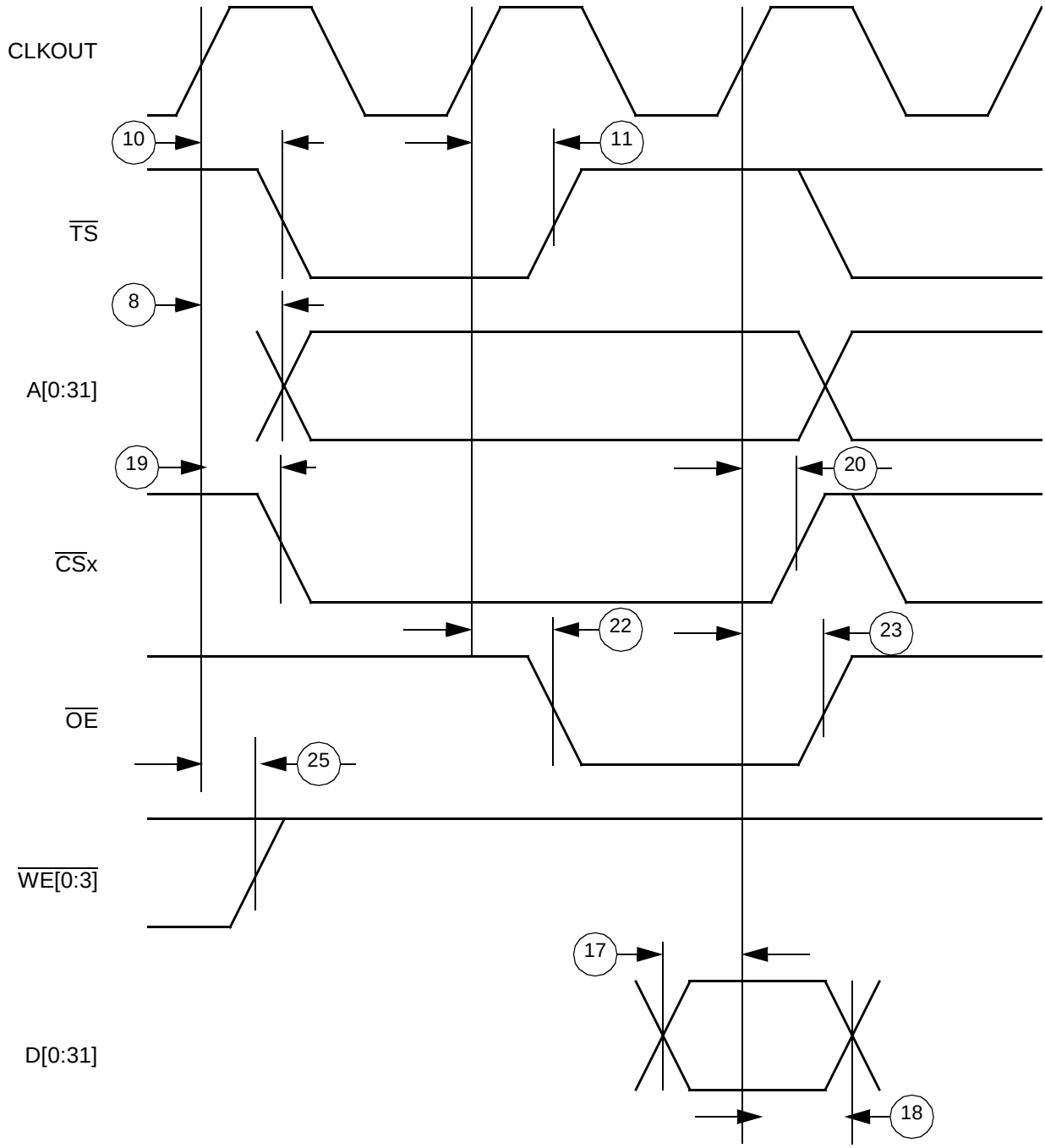


Figure E-15 External Bus Read Timing (GPCM Controlled – ACS = ‘00’)

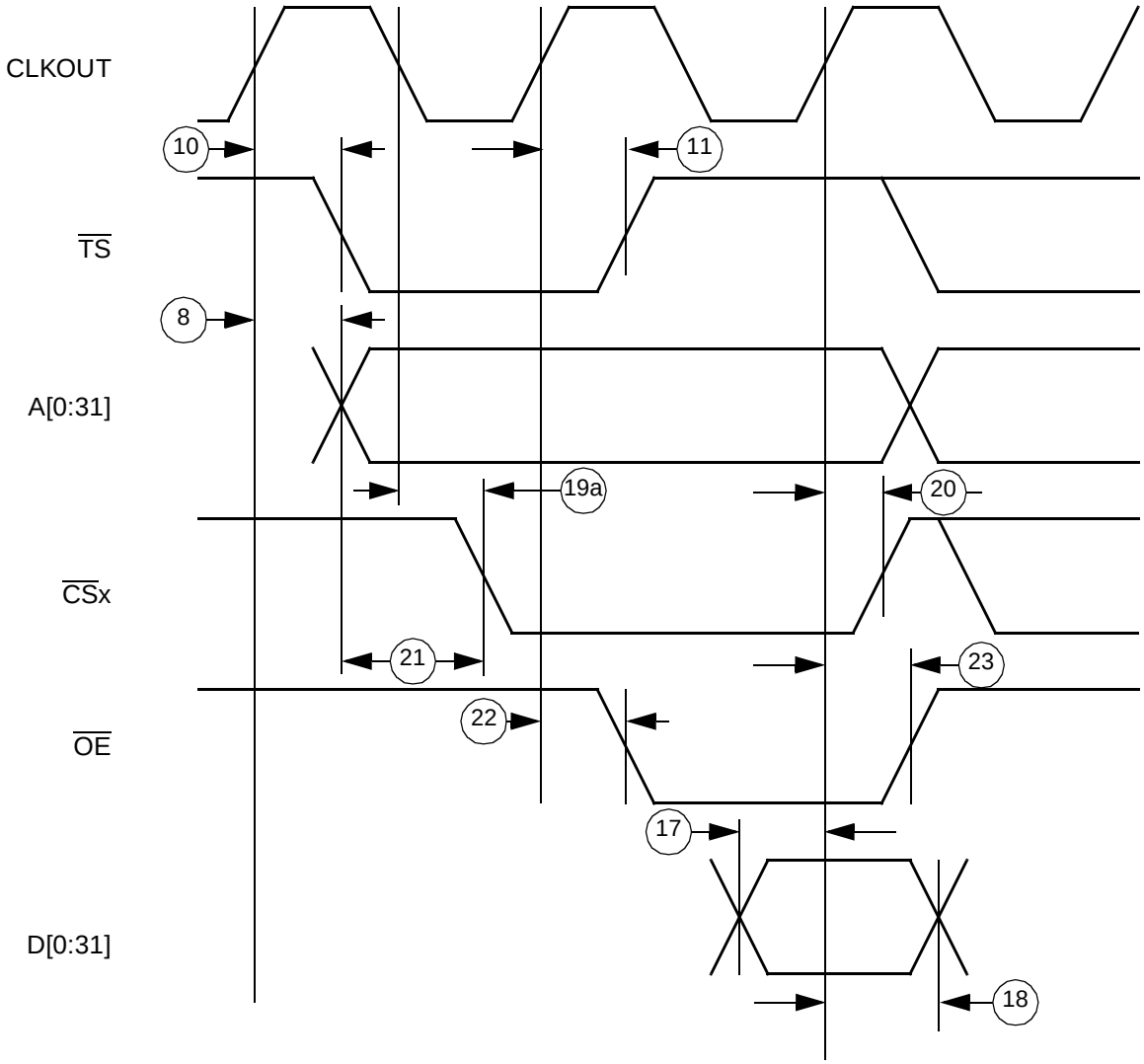


Figure E-16 External Bus Read Timing
(GPCM Controlled – TRLX = '0' ACS = '10')

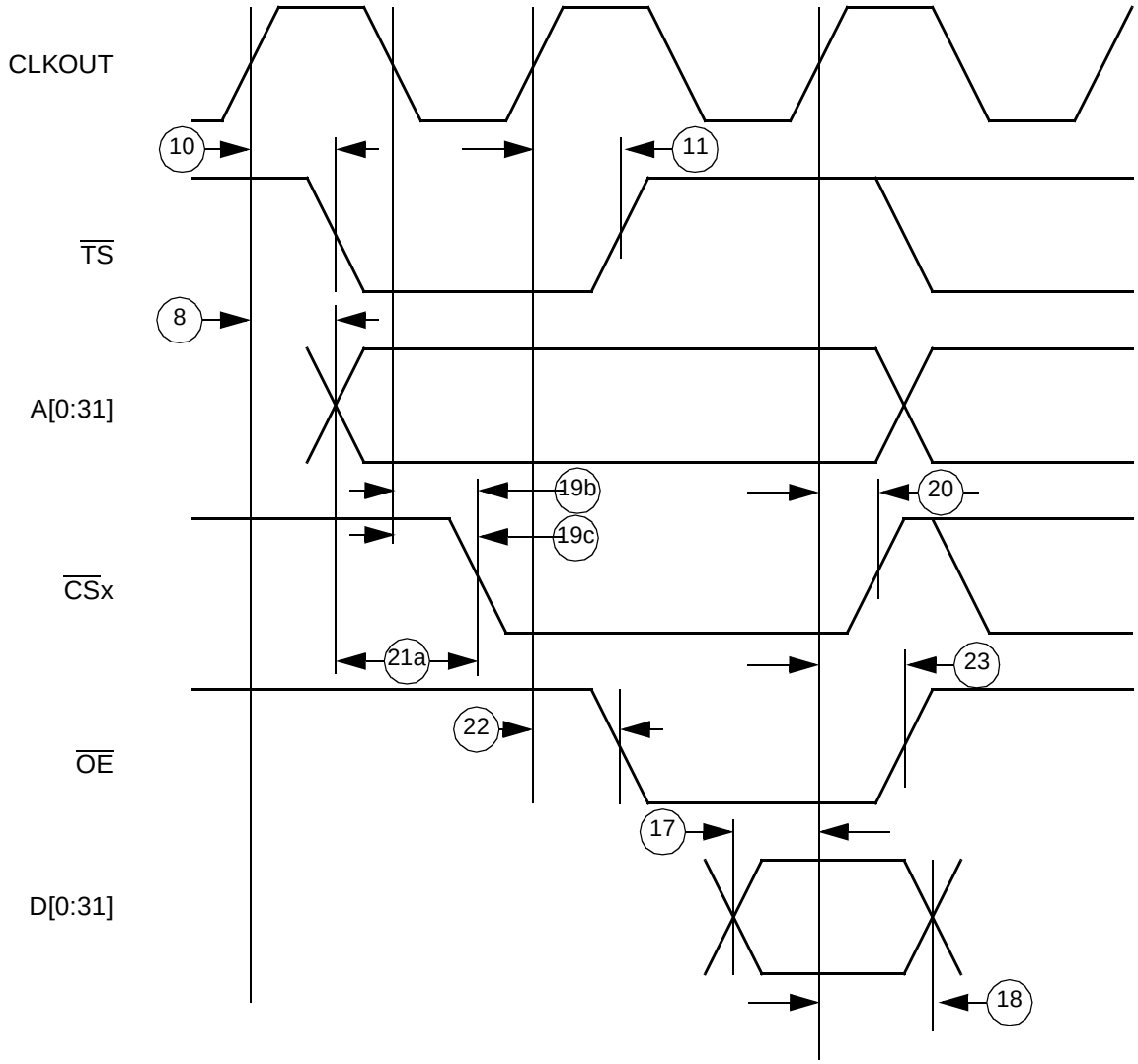


Figure E-17 External Bus Read Timing
(GPCM Controlled – TRLX = '0' ACS = '11')

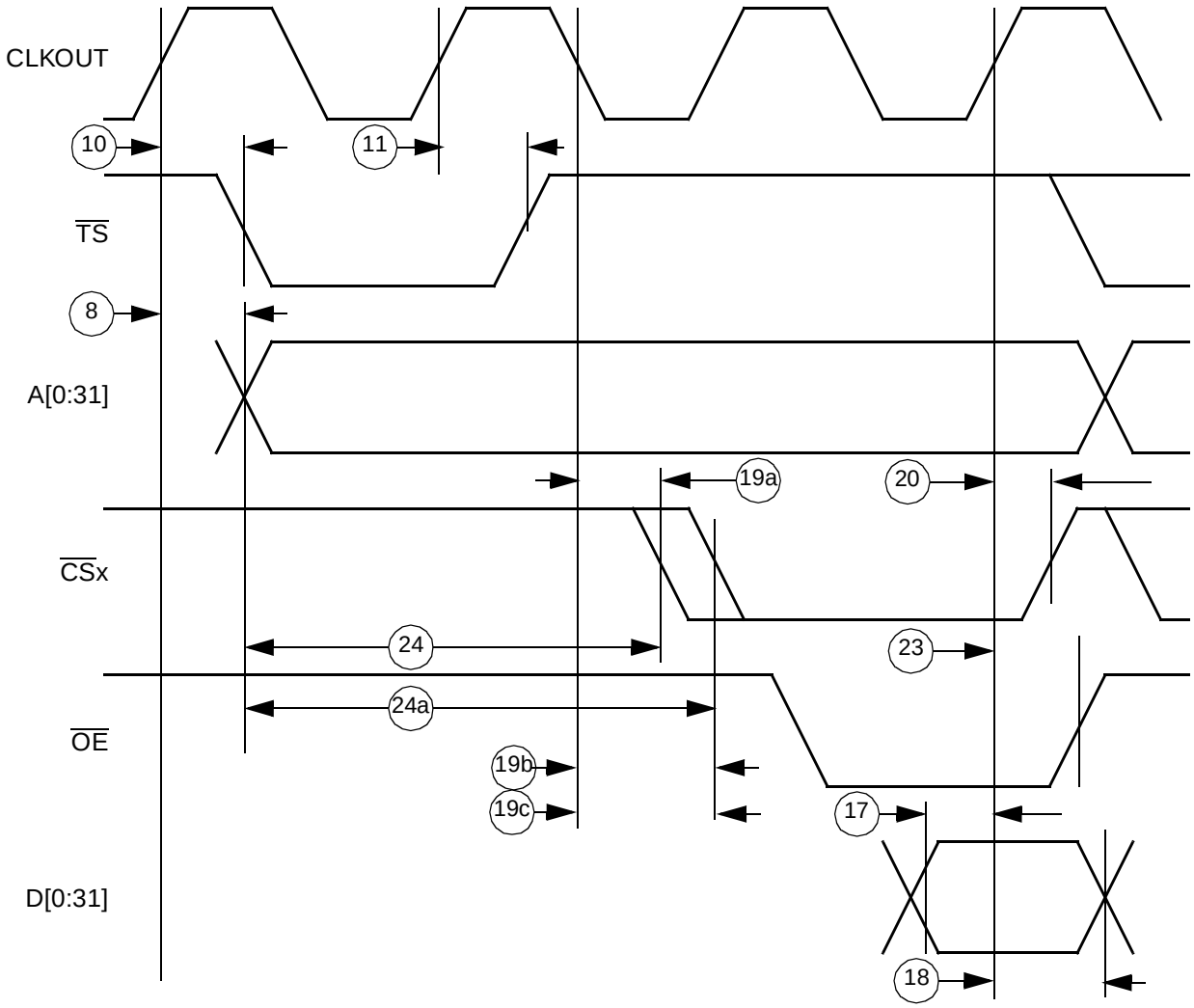


Figure E-18 External Bus Read Timing
(GPCM Controlled – TRLX = '1', ACS = '10', ACS = '11')

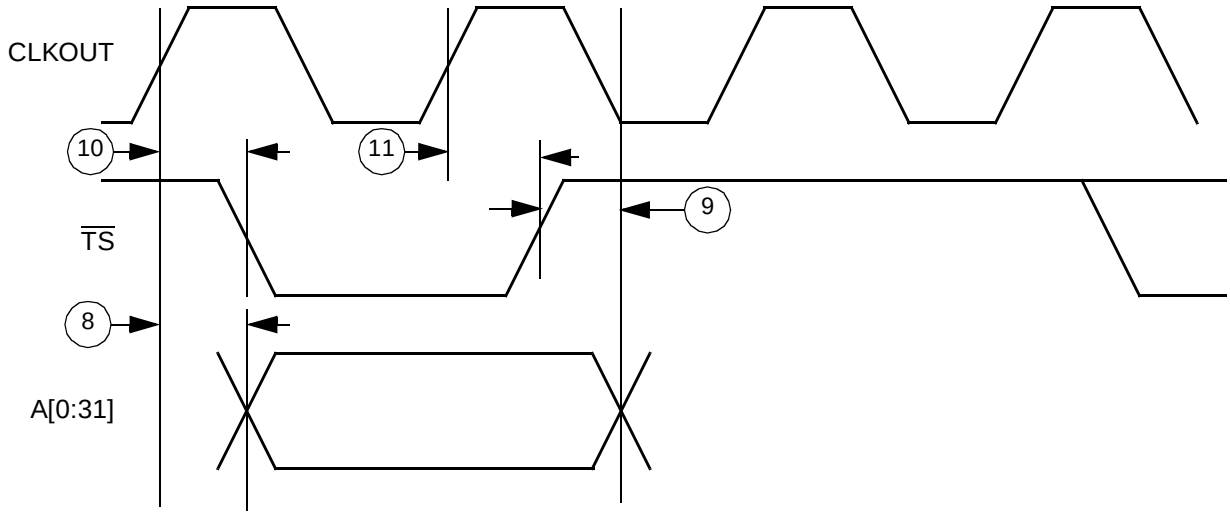


Figure E-19 Address Show Cycle Bus Timing

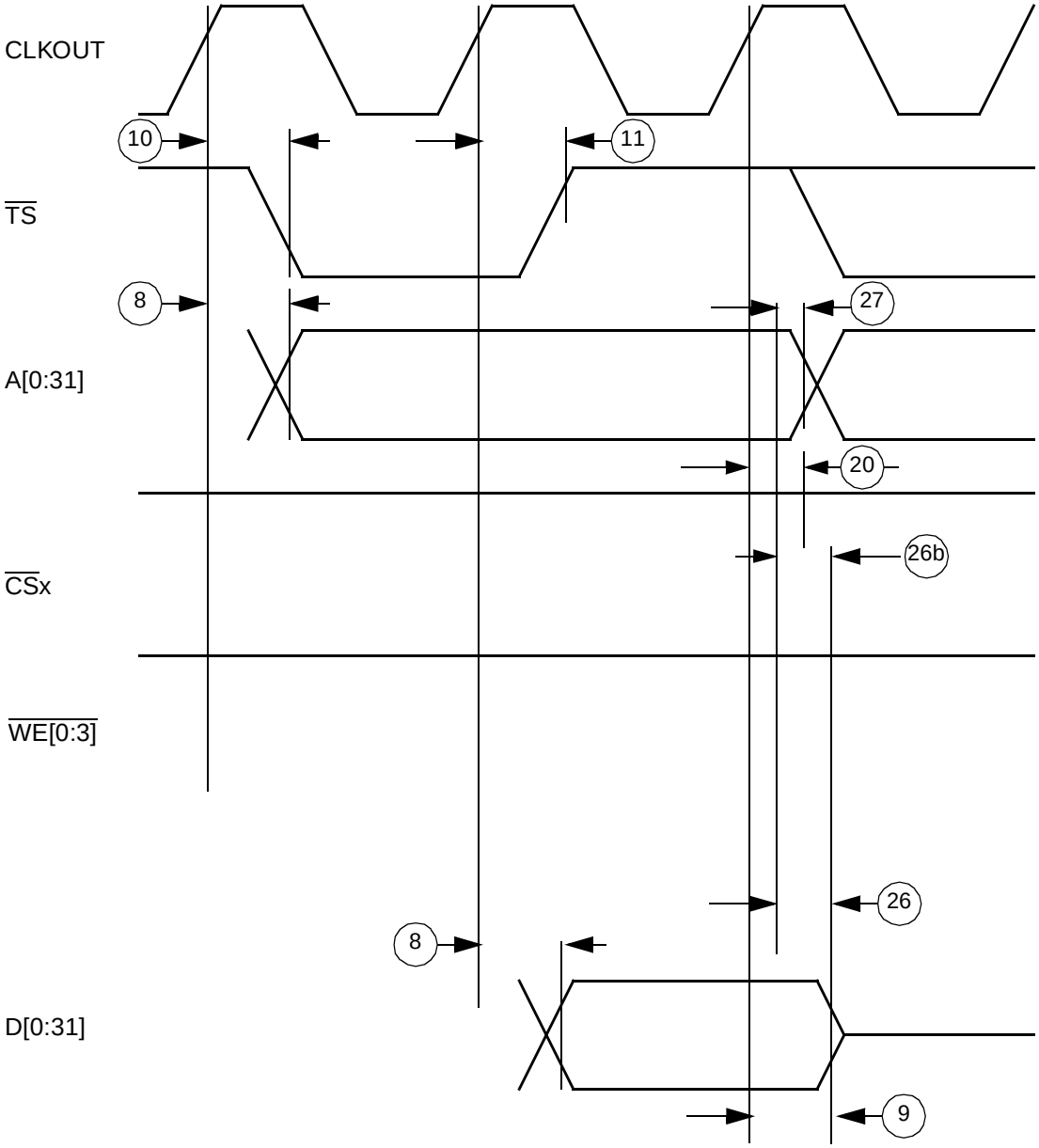


Figure E-20 Address and Data Show Cycle Bus Timing

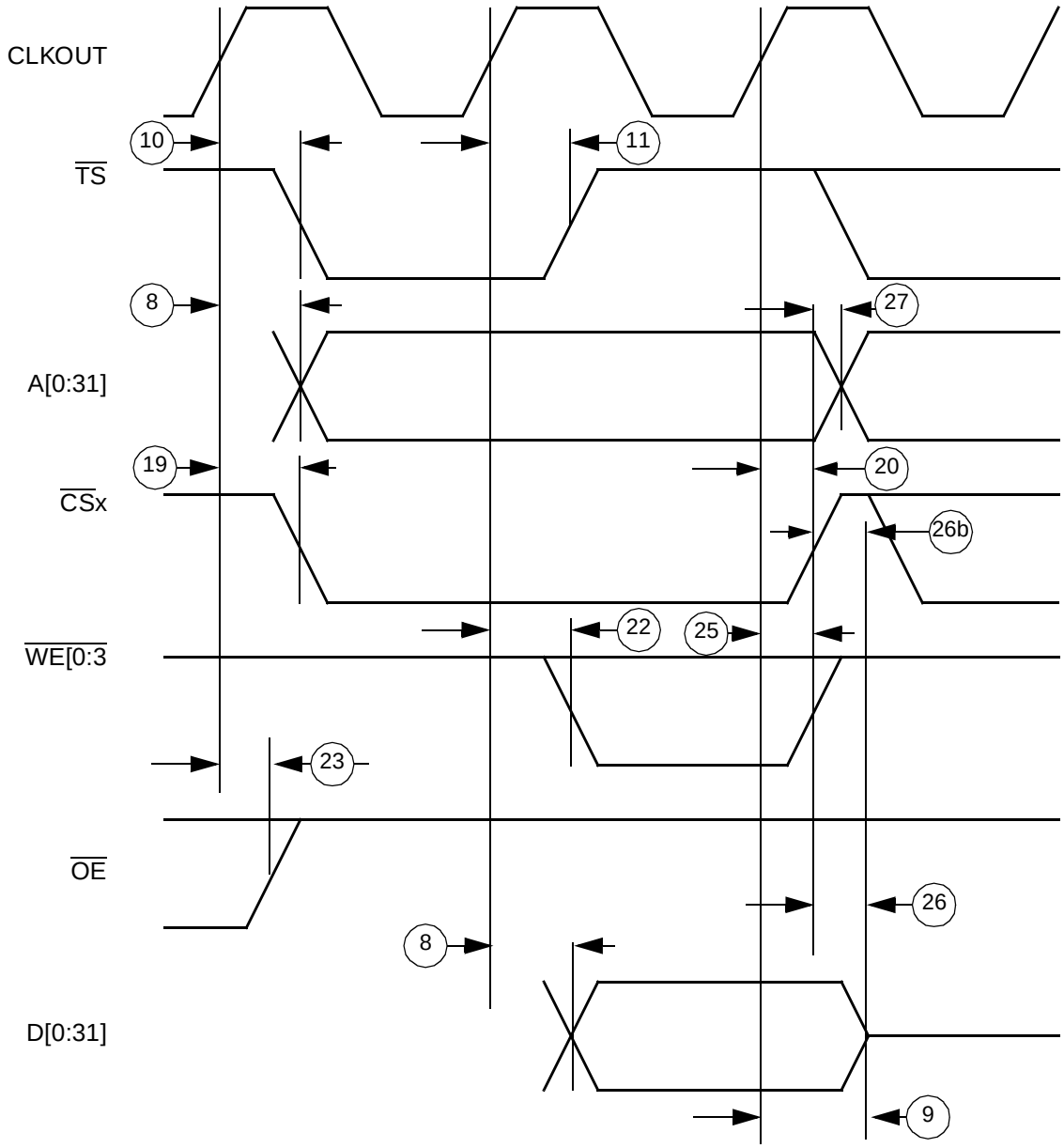


Figure E-21 External Bus Write Timing
(GPCM Controlled – TRLX = '0', CSNT = '0')

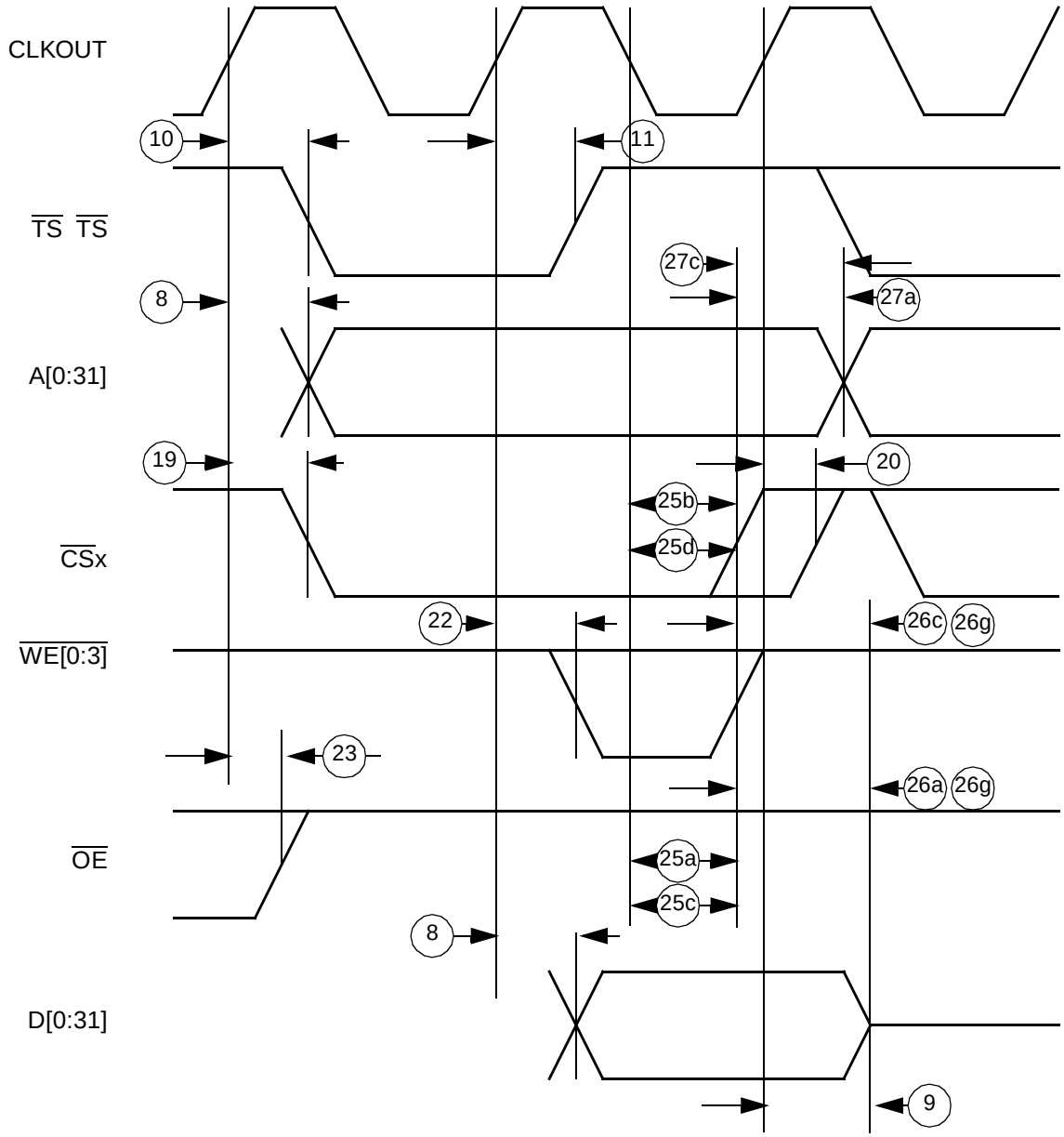


Figure E-22 External Bus Write Timing
(GPCM Controlled – TRLX = '0', CSNT = '1')

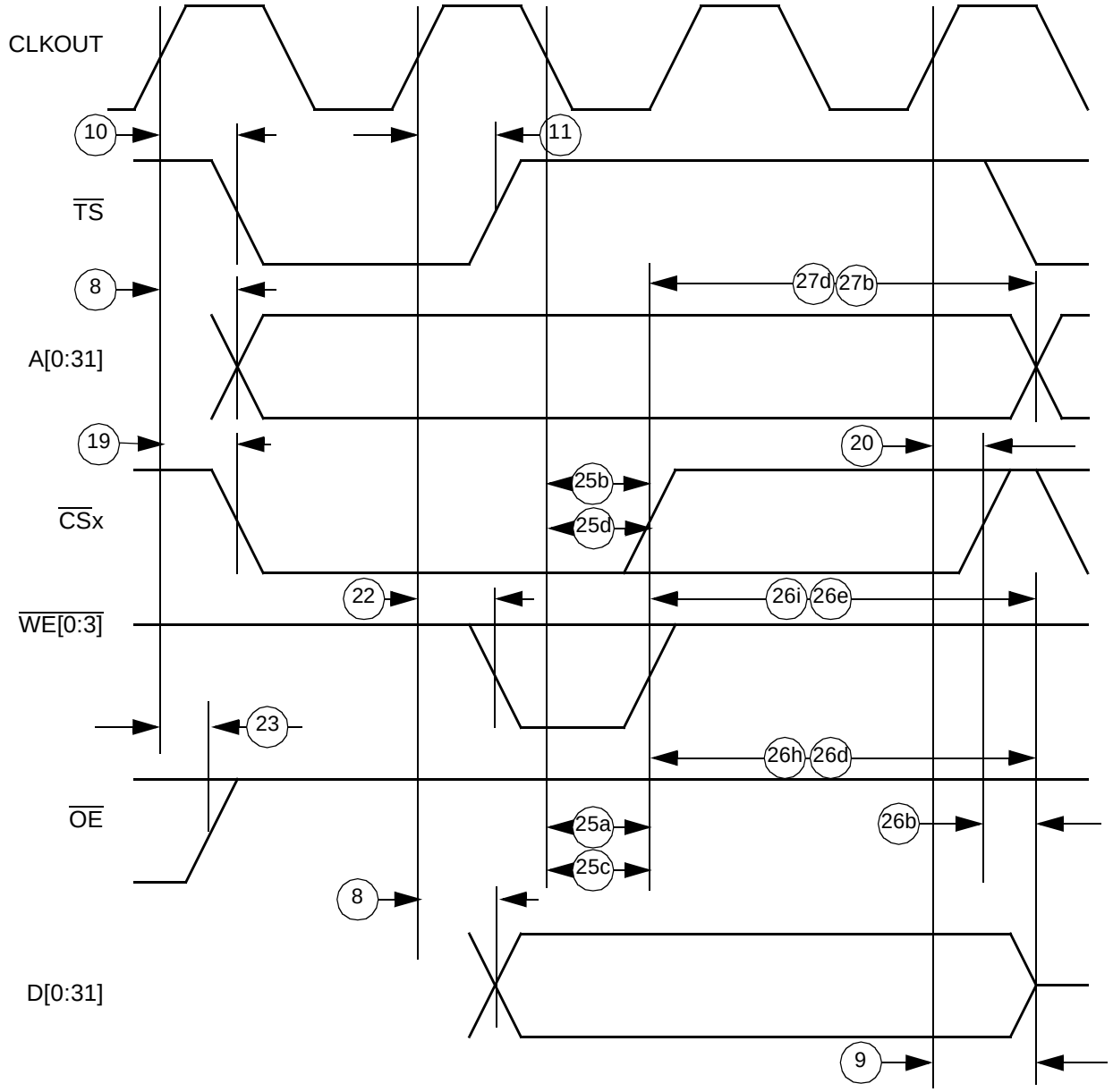


Figure E-23 External Bus Write Timing
(GPCM Controlled – TRLX = '1', CSNT = '1')

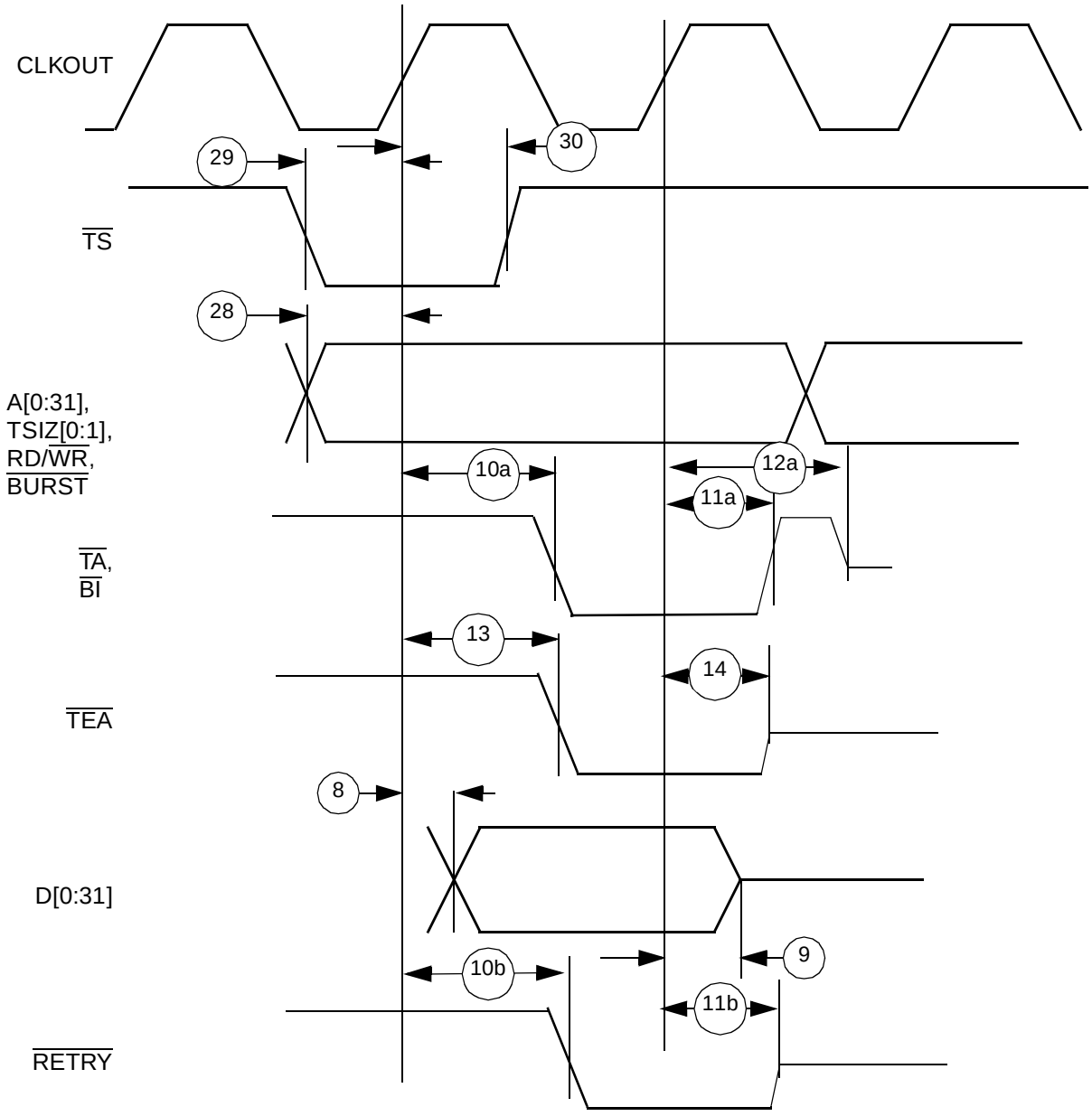


Figure E-24 External Master Read From Internal Registers Timing

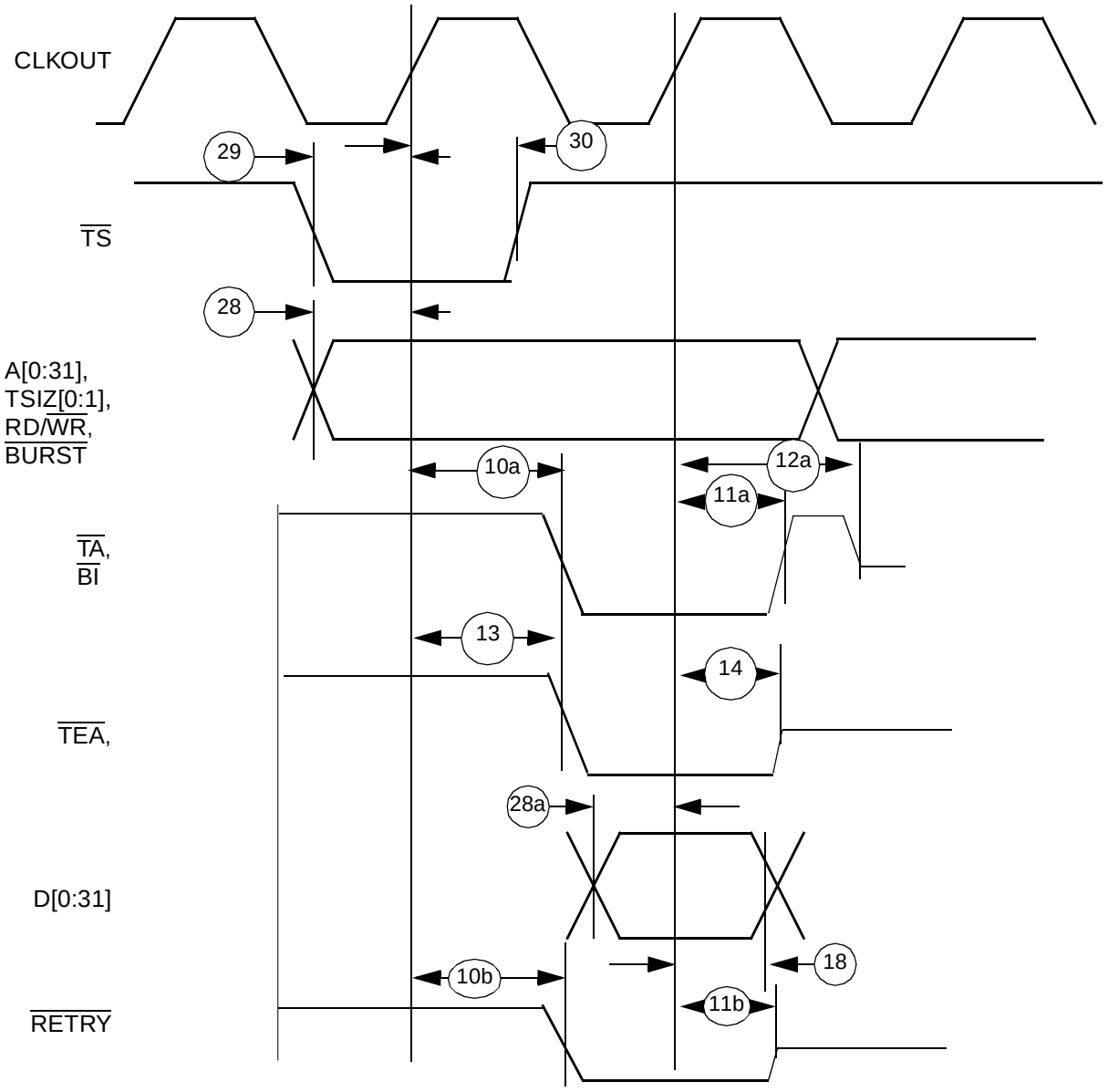


Figure E-25 External Master Write To Internal Registers Timing

Table E-11 Interrupt Timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz		Unit
			Min	Max	Min	Max	
31	$\overline{IRQ}$x valid to CLKOUT rising edge (Setup Time)[1]		10		10		ns
32	$\overline{IRQ}$x hold time after CLKOUT[1]		2		2		ns
33	$\overline{IRQ}$x Pulse width Low		3		3		ns
34	$\overline{IRQ}$x Pulse width High		3		3		ns
35	$\overline{IRQ}$x Edge to Edge time	4 * TC	100		100		ns

NOTES:

1. The timings 31 and 32 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

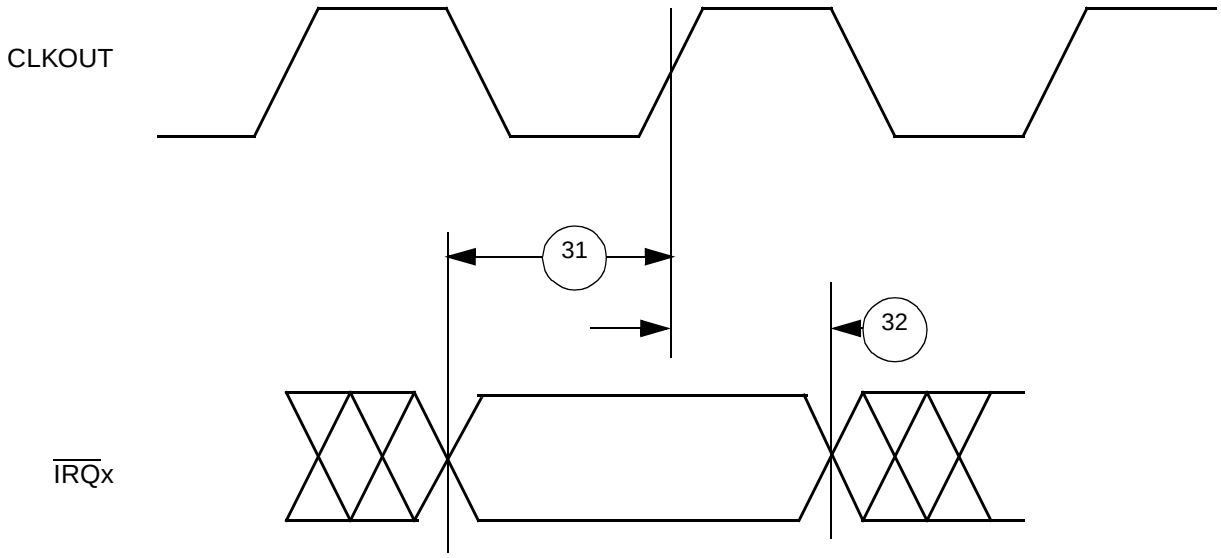


Figure E-26 Interrupt Detection Timing for External Level Sensitive Lines

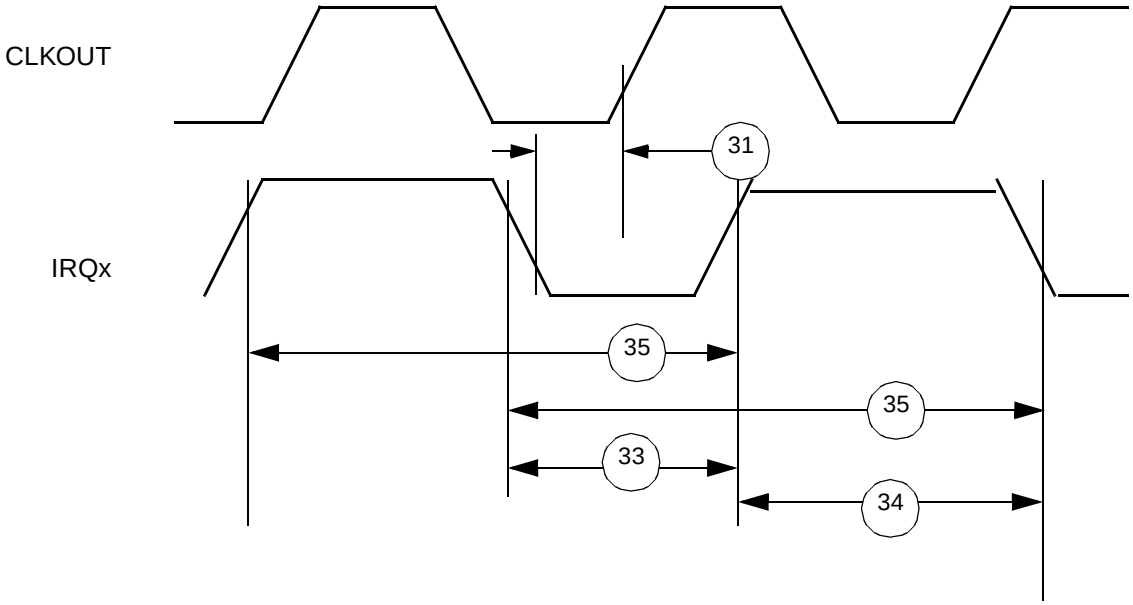


Figure E-27 Interrupt Detection Timing for External Edge Sensitive Lines

E.12 Debug Port Timing

Table E-12 Debug Port timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz		Unit
			Min	Max	Min	Max	
36	DSCK Cycle Time		60	—	TBD	—	ns
37	DSCK Clock Pulse Width		25	—	TBD	—	ns
38	DSCK Rise and Fall Times		0	3	0	3	ns
39	DSDI Input Data Setup Time		15	—	TBD	—	ns
40	DSDI Data Hold Time		5	—	TBD	—	ns
41	DSCK low to DSDO Data Valid		0	18	0	18	ns
42	DSCK low to DSDO Invalid		0	—	0	—	ns

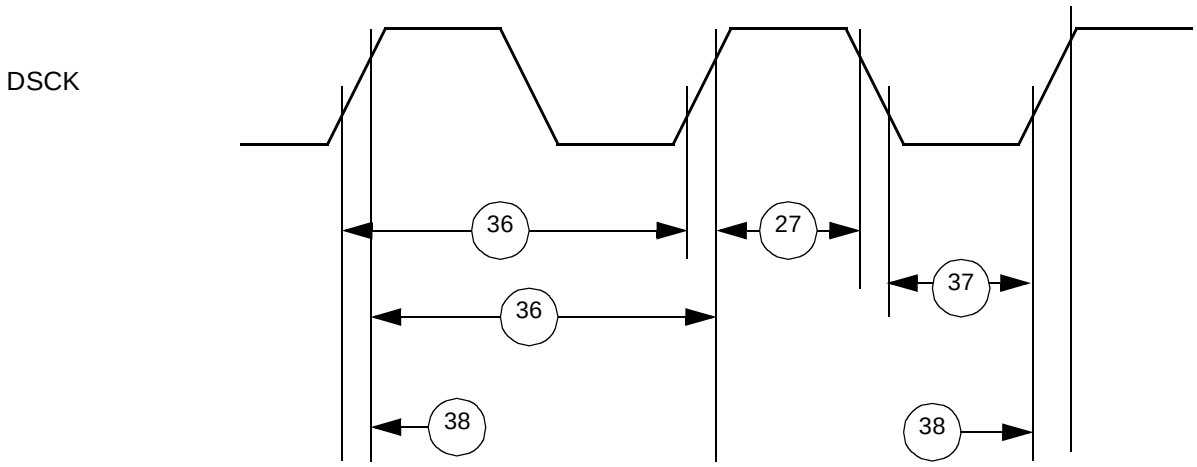


Figure E-28 Debug Port Clock Input Timing

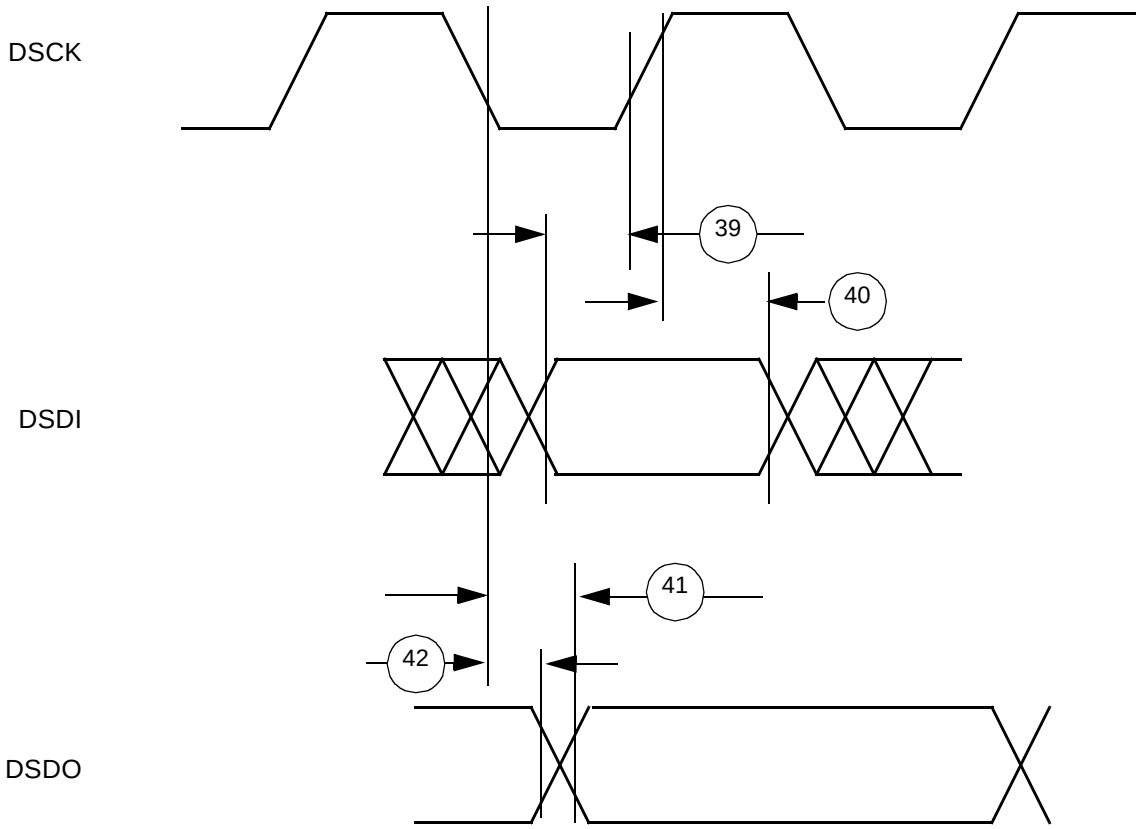


Figure E-29 Debug Port Timings

E.13 Pin Electrical Characteristics

E.13.1 AC Electrical Characteristics

The AC electrical characteristics (56 MHz) are described in the following tables and figures

Table E-13 AC Electrical Characteristics

Number	Characteristic	Min	Max	Unit
1	MCKO Cycle Time (**Tco**)	17.9	—	ns
2	MCKO Duty Cycle	40	60	%
3	Output Rise and Fall Times	0	3	ns
4	MCKO low to MDO Data Valid	(-0.10)Tco	(0.20) Tco	ns
5	MCKI Cycle Time (**Tci**)	35.6	—	ns
6	MCKI Duty Cycle	40	60	%
7	Input Rise and Fall Times	0	3	ns
8	MDI, $\overline{\text{EVTI}}$, $\overline{\text{MSEI}}$ Setup Time	(0.20)Tci	—	ns
9	MDI Hold TIme	(0.10)Tci	—	ns
10	$\overline{\text{RSTI}}$ Pulse Width	(4.0) Tco	—	ns
11	MCKO low to $\overline{\text{MSEO}}$ Valid	(-0.10)Tco	(0.20) Tco	ns
12	$\overline{\text{EVTI}}$ Pulse Width	(4.0) Tco	—	ns
13	$\overline{\text{EVTI}}$ to $\overline{\text{RSTI}}$ Setup (at reset only)	(4.0) System Clock	—	ns
14	$\overline{\text{EVTI}}$ to $\overline{\text{RSTI}}$ Hold (at reset only)	(4.0) System Clock	—	ns

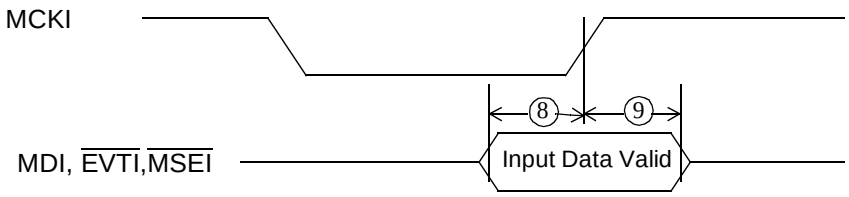


Figure E-30 Auxiliary Port Data Input Timing Diagram

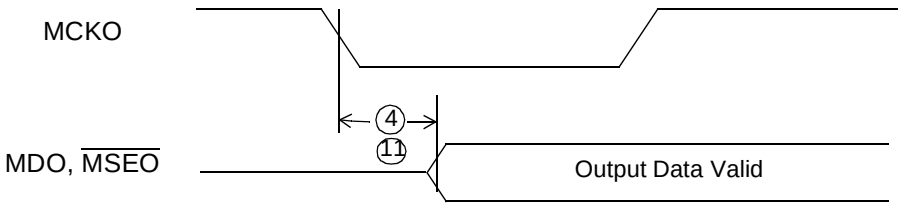


Figure E-31 Auxiliary Port Data Output Timing Diagram

MDO and $\overline{\text{MSEO}}$ data is held valid until the next MCKO low transition.

When $\overline{\text{RSTI}}$ is asserted, $\overline{\text{EVTI}}$ is used to enable or disable the auxiliary port. Because MCKO probably is not active at this point, the timing must be based on the system clock. Since the system clock is not realized on the connector, its value must be known by the tool.

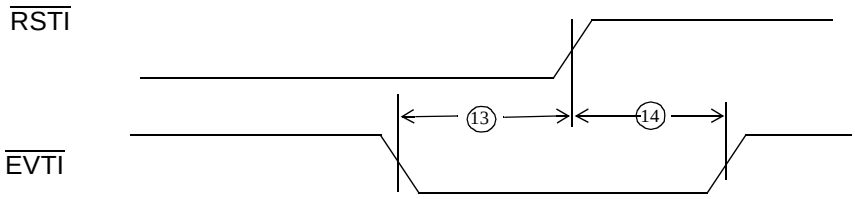


Figure E-32 Enable Auxiliary From $\overline{\text{RSTI}}$

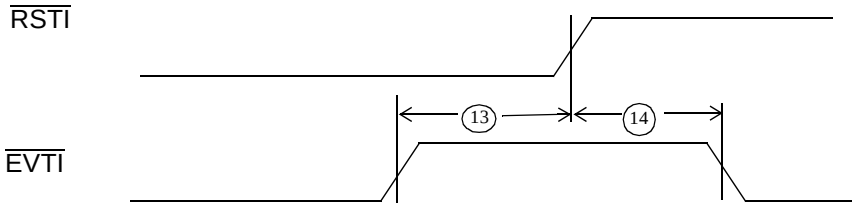


Figure E-33 Disable Auxiliary From $\overline{\text{RSTI}}$

E.14 RESET Timing

Table E-14 RESET Timing

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz		Unit
			Min	Max	Min	Max	
43	CLKOUT to $\overline{\text{HRESET}}$ high impedance			20		20	ns
44	CLKOUT to $\overline{\text{SRESET}}$ high impedance			20		20	ns
45	$\overline{\text{RSTCONF}}$ pulse width	17 * TC	425		302		ns
46	Configuration Data to $\overline{\text{HRESET}}$ rising edge Setup Time	15 * TC + TCC	382		272		ns
47	Configuration Data to $\overline{\text{RSTCONF}}$ rising edge set up time	15 * TC + TCC	382		272		ns
48	Configuration Data hold time after $\overline{\text{RSTCONF}}$ negation		0		0		ns
49	Configuration Data hold time after $\overline{\text{HRESET}}$ negation		0		0		ns
49a	$\overline{\text{RSTCONF}}$ hold time after $\overline{\text{HRESET}}$ negation[1]		50		35		
50	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to Data out drive		25		25		ns
51	$\overline{\text{RSTCONF}}$ negated to Data out high impedance		25		25		ns
52	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to Data out high impedance		25		25		ns
53	DSDI, DSCK set up	3 * TC	75		55		ns
54	DSDI, DSCK hold time		0		0		ns
55	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	8 * TC	200		142		ns
55a	$\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{PORESET}}$ pulse width [2]		100		100		ns

NOTES:

1. Weak pull-ups and pull-downs used for Reset timing will comply with the 130 µA mode select current outlined in **E.6 DC Electrical Characteristics** The system requires two clocks of hold time on $\overline{\text{RSTCONF}}$/TEXP after negation of $\overline{\text{HRESET}}$. The simplest way to insure meeting this requirement in systems that require the use of the TEXP function, is to connect $\overline{\text{RSTCONF}}$/TEXP to $\overline{\text{SRESET}}$.
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{PORESET}}$ have a glitch detector to ensure that spikes less than 20 ns are rejected. The internal $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{PORESET}}$ will assert only if these signals are asserted for more than 100 ns

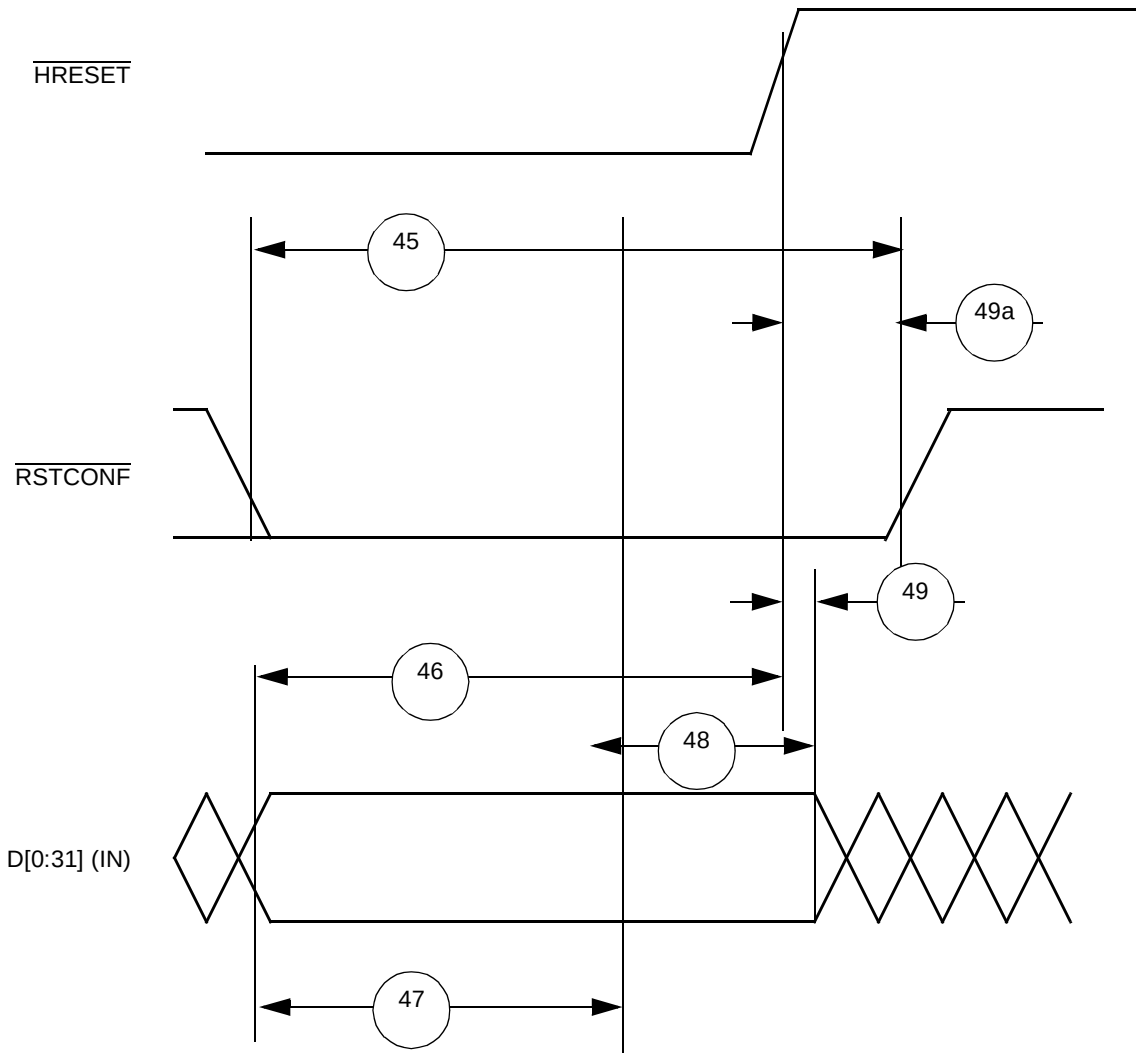


Figure E-34 Reset Timing – Configuration from Data Bus

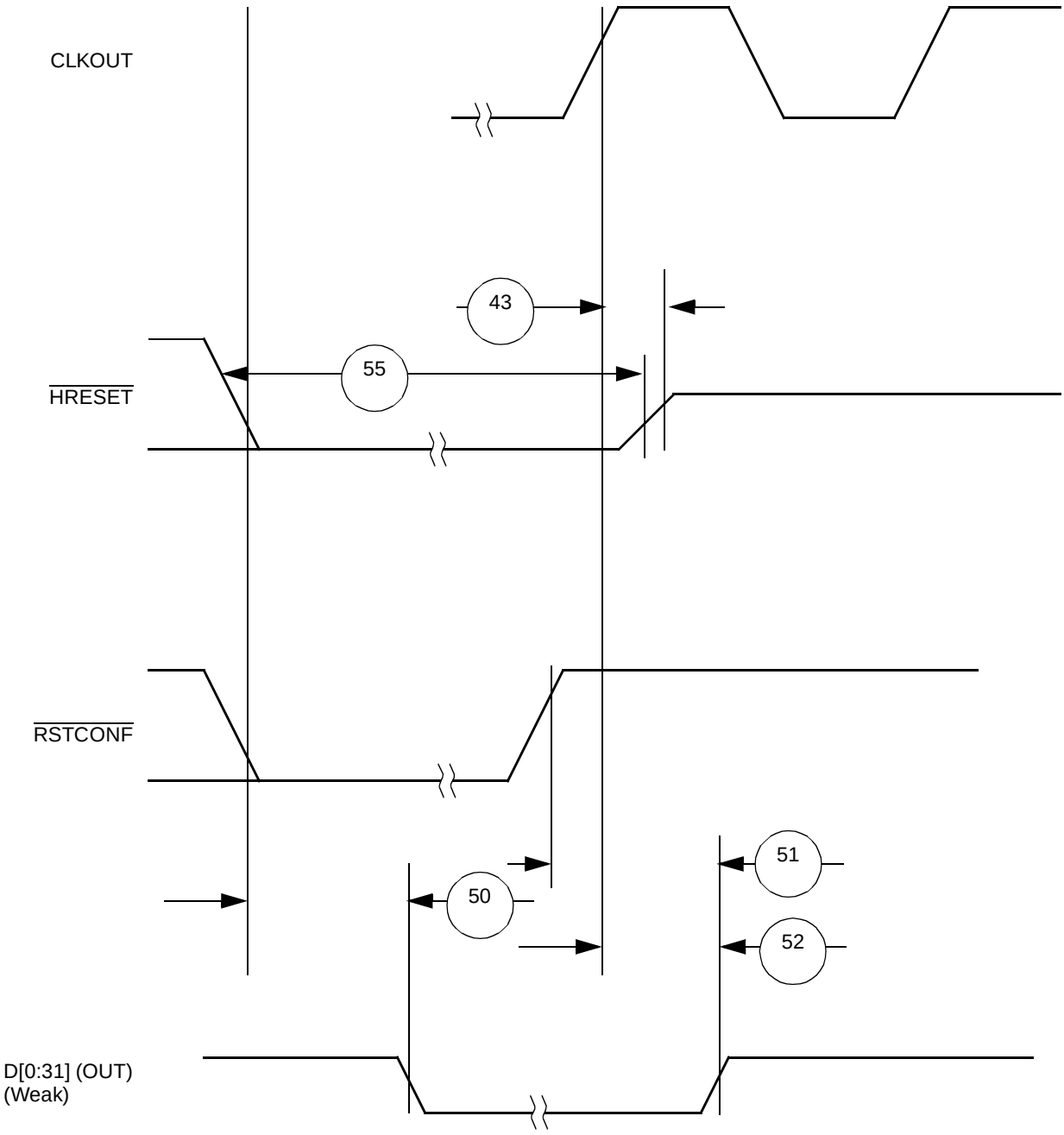


Figure E-35 Reset Timing – Data Bus Weak Drive During Configuration

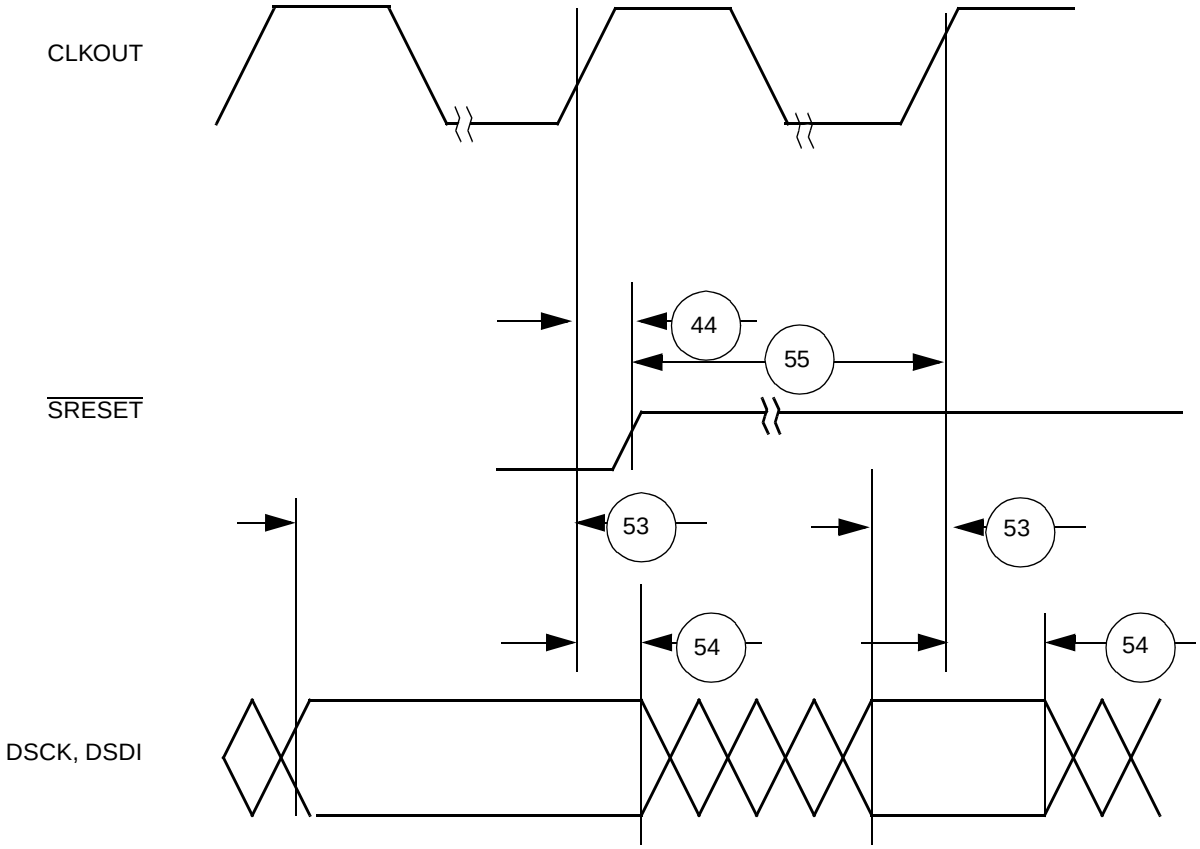


Figure E-36 Reset Timing – Debug Port Configuration

E.15 IEEE 1149.1 Electrical Characteristics

Table E-15 JTAG timing[1]

($T_A = T_L$ to T_H)

	Characteristic	Expression	40 MHz		56 MHz		Unit
			Min	Max	Min	Max	
56	TCK Cycle Time		—	100	—	100	ns
57	TCK Clock Pulse Width Measured at $V_{DD}/2$		—	40	—	40	ns
58	TCK Rise and Fall Times		0	10	0	10	ns
59	TMS, TDI Data Setup Time		5		5		ns
60	TMS, TDI Data Hold Time		25		25		ns
61	TCK Low to TDO Data Valid			20		20	ns
62	TCK Low to TDO Data Invalid		0		0		ns
63	TCK Low to TDO High Impedance			20		20	ns
64	$\overline{\text{TRST}}$ Assert Time		100		100		ns
65	$\overline{\text{TRST}}$ Setup Time to TCK Low		40		40		ns
66	TCK Falling Edge to Output Valid			50		50	ns
67	TCK Falling Edge to Output Valid out of High Impedance			50		50	ns
68	TCK Falling Edge to Output High Impedance			50		50	ns
69	Boundary Scan Input Valid to TCK Rising Edge		50		50		ns
70	TCK Rising Edge to Boundary Scan Input Invalid		50		50		ns

NOTES:
1. JTAG timing is only tested at 10 MHz

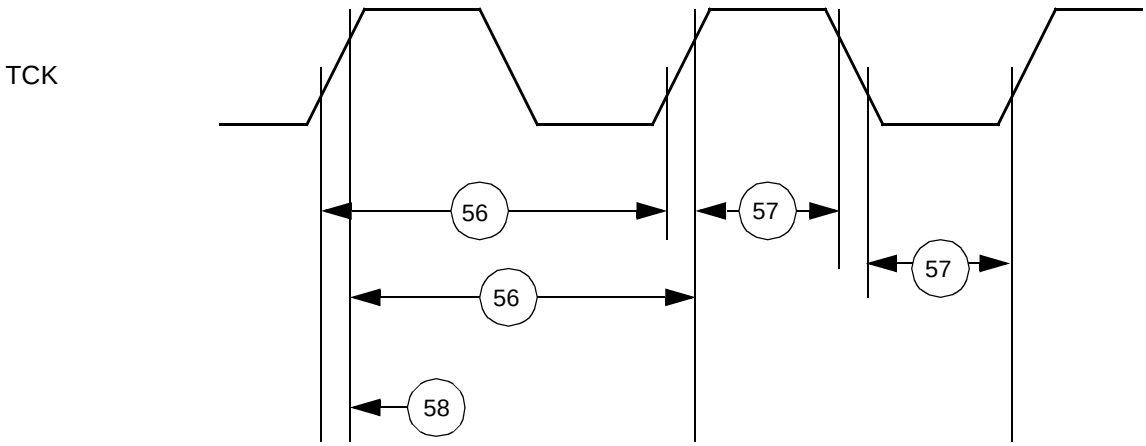


Figure E-37 JTAG Test Clock Input Timing

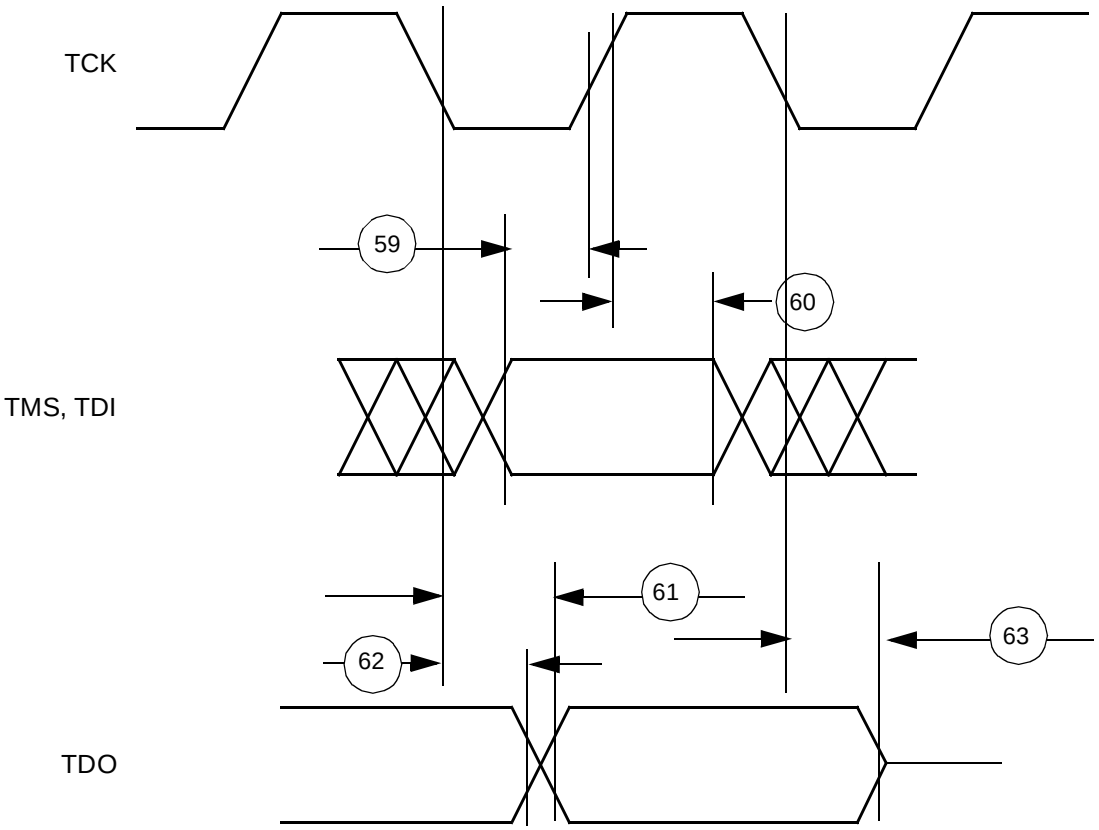


Figure E-38 JTAG Test Access Port Timing Diagram

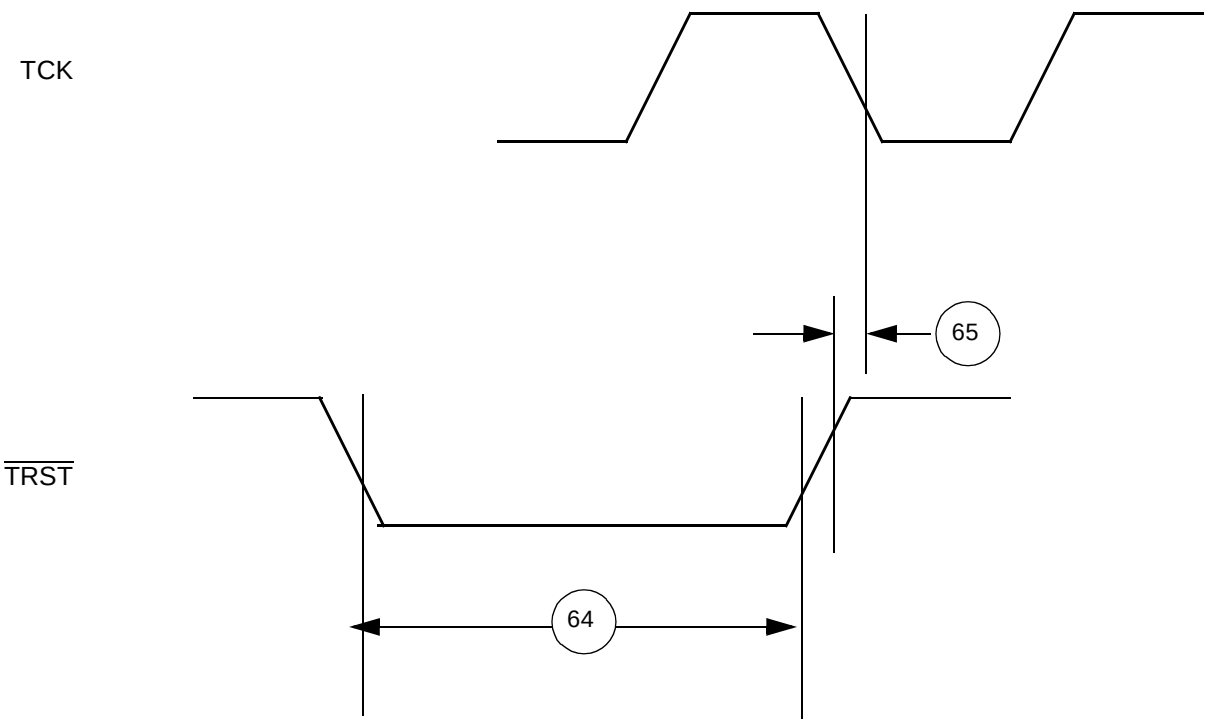


Figure E-39 JTAG $\overline{\text{TRST}}$ Timing Diagram

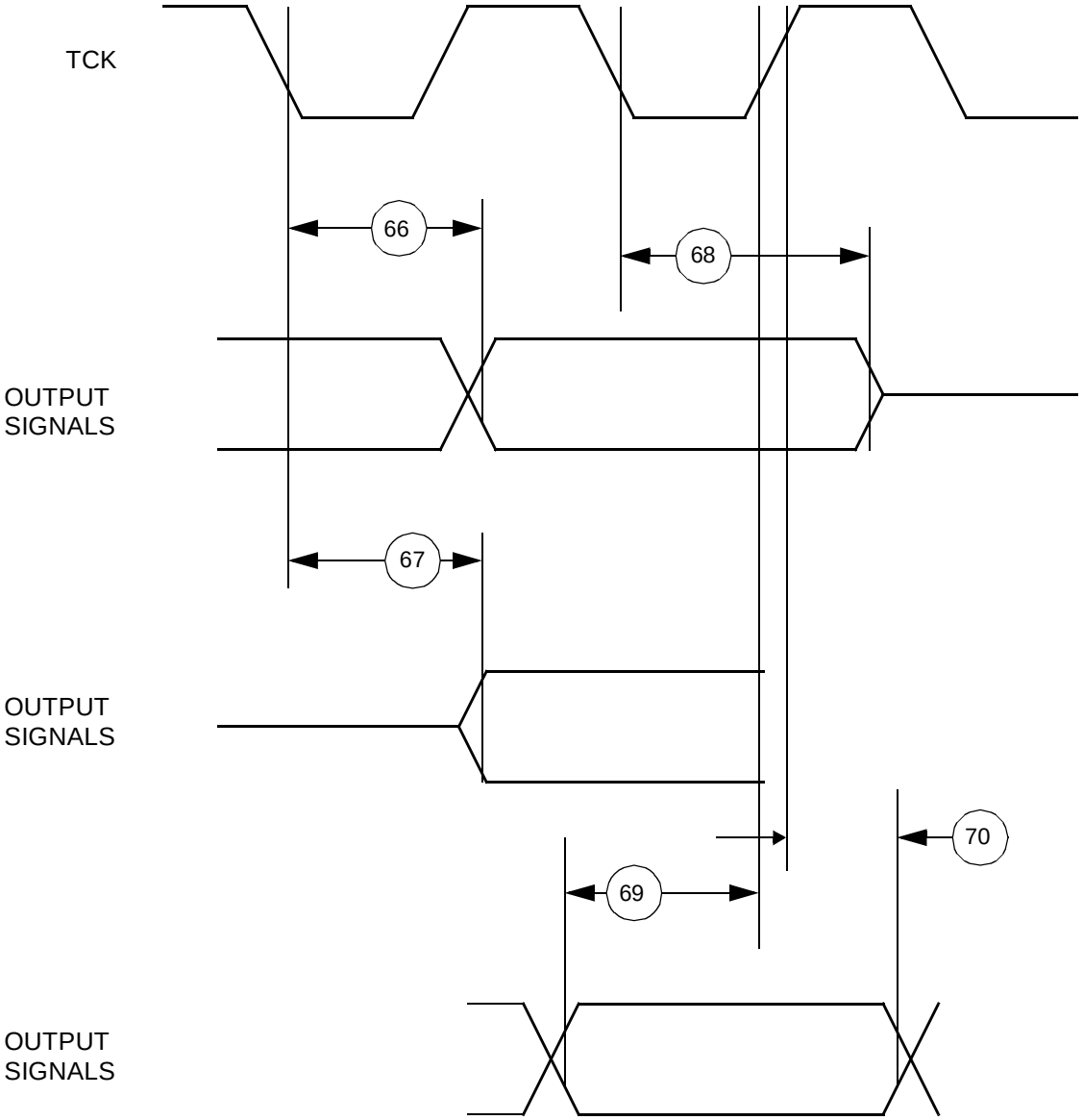


Figure E-40 Boundary Scan (JTAG) Timing Diagram

E.16 QADC64E Electrical Characteristics

Table E-16 QADC64E Conversion Characteristics (Enhanced Mode Operation)

($T_A = T_L$ to T_H)

Num	Parameter	Symbol	Min	Max	Units
97	QADC Clock (QCLK) Frequency[1]	F_{QCLK}	0.5	3.0	MHz
98	Conversion Cycles[2]	CC	14	20	QCLK cycles
99	Conversion Time[3] F_{QCLK} = 2.8MHz[1,4] Min = CCW/IST =1b0 Max = CCW/IST =1b1	T_{CONV}	7.0	 7.25	 µs µs
100	Stop Mode Recovery Time	T_{SR}	—	10	µs
101	Resolution[5]	—	5	—	mV
102	Absolute (total unadjusted) error[6, 7, 8, 9] F_{QCLK} = 3.0MHz[3], 2 clock input sample time	AE	- 2	2	Counts
103	DC Disruptive Input Injection Current[10, 11, 12, 13, 14]	I_{INJ}[15] I_{INJ}[16]	- 3 -1	3 1	mA mA
104	Current Coupling Ratio[17] PQA PQB	K	 — —	 $8x10^{-5}$ $8x10^{-5}$	
105	Incremental Error due to injection current All channels have same 10kΩ < Rs <100kΩ Channel under test has Rs=10kΩ, I_{INJ}=±3mA	E_{INJ}		 ±1.0 ±1.0	 Counts Counts
106	Source impedance at input [18]	R_S	—	100	kΩ
107	Incremental Capacitance during Sampling [19]	C_{SAMP}	—	5	pF

NOTES:

1. Conversion characteristics vary with F_{QCLK} rate. Reduced conversion accuracy occurs at max F_{QCLK} rate.
2. The number of conversion cycles is dependent on the IST bits in the CCW register.
3. Assumes that f_{SYS} = 56 MHz
4. Assumes F_{QCLK} = 2.80 MHz, with clock prescaler values of: 20 * CCW: BYP=0b0
5. At $V_{RH} - V_{RL}$ = 5.12 V, one count = 5 mV.
6. Accuracy tested and guaranteed at $V_{RH} - V_{RL}$ = 5.0 V ± 0.5 V
7. This parameter is periodically sampled rather than 100% tested.
8. Absolute error includes 1/2 count (~2.5 mV) of inherent quantization error and circuit (differential, integral, and offset) error. Specification assumes that adequate low-pass filtering is present on analog input pins — capacitive filter with 0.01 µF to 0.1 µF capacitor between analog input and analog ground, typical source isolation impedance of 10 KΩ.
9. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals may affect the conversion accuracy of other channels.
10. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leftarrow V_{DDA}$ and $V_{RL} \leftarrow V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
11. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
12. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP}$ = (the lower of V_{DDA} or V_{DDH}) + 0.3 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values. The diode drop voltage is a function of current and varies approximately 0.4 to 0.8 V over temperature
13. This parameter is periodically sampled rather 100% tested.
14. Derate linearly to 0.3 mA if VDDH - VDDA = 1 V. This specification is preliminary and may change after further characterization.

15. Condition applies to two adjacent pins.
16. Condition applies to all analog channels.
17. Current Coupling Ratio, K, is defined as the ratio of the output current, I_{OUT}, measured on the pin under test to the injection current, I_{INJ}, when both adjacent pins are overstressed with the specified injection current. $K = I_{OUT} / I_{INj}$ The input voltage error on the channel under test is calculated as $Verr = I_{INJ} * K * R_S$.
18. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance. Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{ERRJ}): $V_{ERRJ} = R_S * I_{OFF}$ where I_{OFF} is a function of operating temperature. Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the filtering capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance
19. For a maximum sampling error of the input voltage ← 1LSB, then the external filter capacitor, $C_f \geq 1024 * C_{SAMP}$. The value of C_{SAMP} in the new design may be reduced.

E.17 QSMCM Electrical Characteristics

Table E-17 QSPI Timing

($T_A = T_L$ to T_H, 50 pF load on all QSPI pins unless otherwise noted)

Num	Function	Symbol	Min	Max	Unit
108	Operating Frequency[1] Master Slave	f_{OP}	 DC DC	 $f_{SYS}/4$ $f_{SYS}/4$	 Hz Hz
109	Cycle Time Master Slave	t_{QCYC}	 4*TC 4*TC	 510 * TC[2] —	 ns ns
110	Enable Lead Time Master Slave	t_{LEAD}	 2*TC 2*TC	 128 * TC —	 ns ns
111	Enable Lag Time Master Slave	t_{LAG}	 — 2*TC	 SCK/2 —	 ns ns
112	Clock (SCK) High or Low Time Master Slave[3]	t_{SW}	 2*TC– 60 2*TC– n	 255 * TC —	 ns ns
113	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{TD}	 17*TC 13*TC	 8192 * TC -	 ns ns
114	Data Setup Time (Inputs) Master Slave	t_{SU}	 30 20	 - -	 ns ns
115	Data Hold Time (Inputs) Master Slave	t_{HI}	 0 20	 - -	 ns ns
116	Slave Access Time	t_A	—	TC	ns
117	Slave MISO Disable Time	t_{DIS}	—	2 * TC	ns
118	Data Valid (after SCK Edge) Master Slave	t_V	 — —	 50 50	 ns ns
119	Data Hold Time (Outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns

Table E-17 QSPI Timing (Continued)

($T_A = T_L$ to T_H, 50 pF load on all QSPI pins unless otherwise noted)

Num	Function	Symbol	Min	Max	Unit
	Rise Time Input	t_{rI}	— 	 1	 µs
120	Output – up to 50 pF, SLRC bit of PDMCR = “0” up to 50 pF, SLRC bit of PDMCR = “1” up to 200 pF, SLRC bit of PDMCR = “1”	t_{RO}	 — — —	 200 8 21	 ns ns ns
	Fall Time Input	t_{FI}	— 	 1	 µs
121	Output – up to 50 pF, SLRC bit of PDMCR = “0” up to 50 pF, SLRC bit of PDMCR = “1” up to 200 pF, SLRC bit of PDMCR = “1”	t_{FO}	 — — —	 200 8 21	 ns ns ns

NOTES:

1. All AC timing is tested to the 3-V levels outlined in **E.6 DC Electrical Characteristics**
2. TC is defined to be the clock period.
3. For high time, n = External SCK rise time; for low time, n = External SCK fall time.

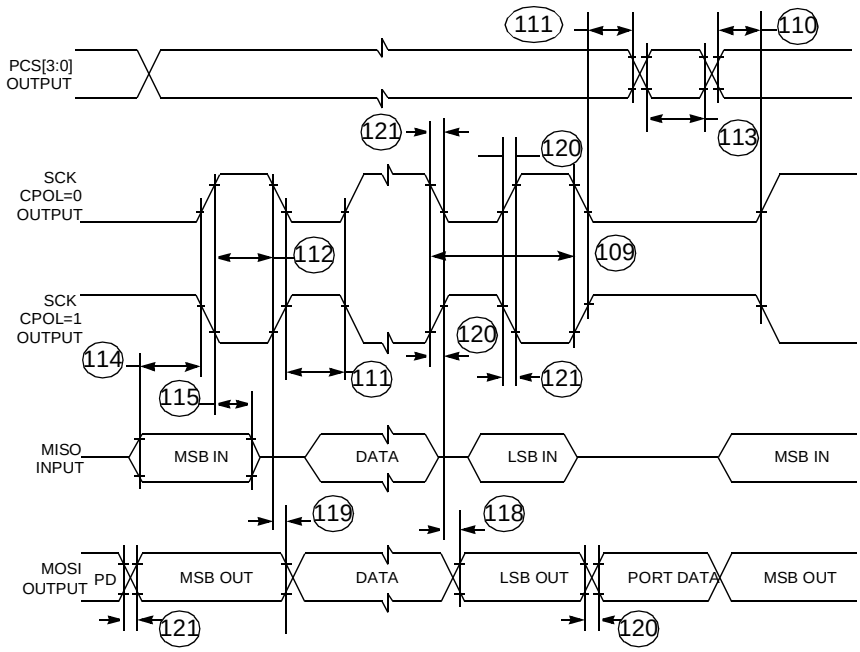
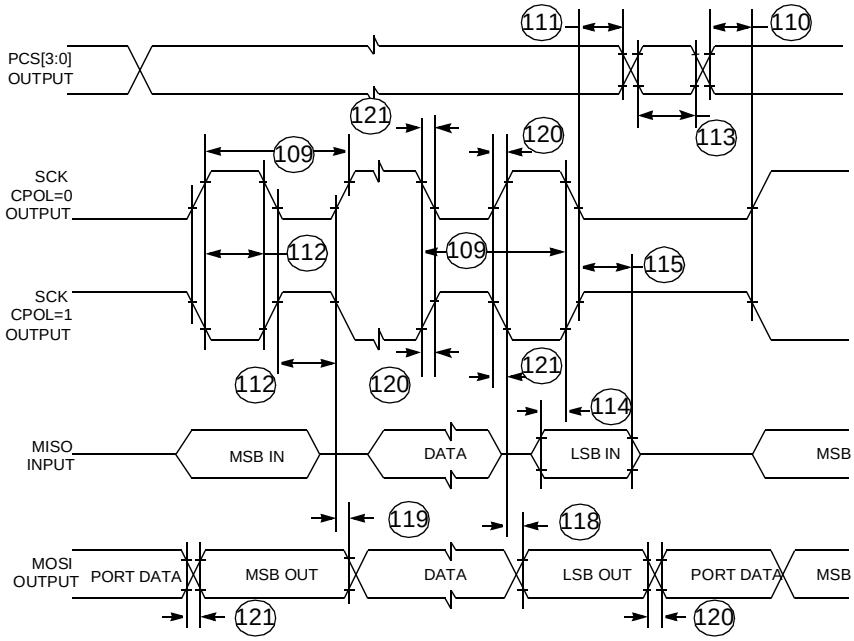
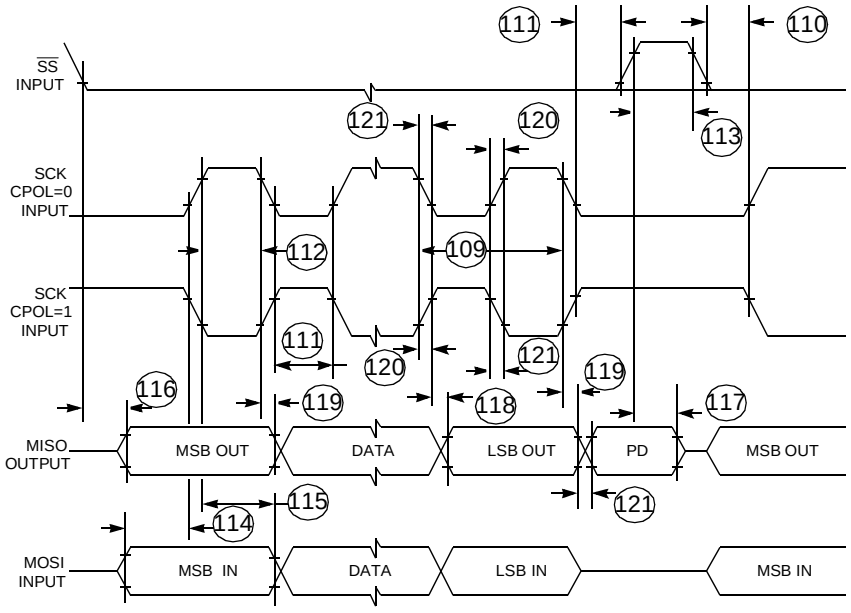


Figure E-41 QSPI Timing – Master, CPHA = 0



QSPI MAST CPHA1

Figure E-42 QSPI Timing – Master, CPHA = 1



QSPI SLV CPHA0

Figure E-43 QSPI Timing – Slave, CPHA = 0

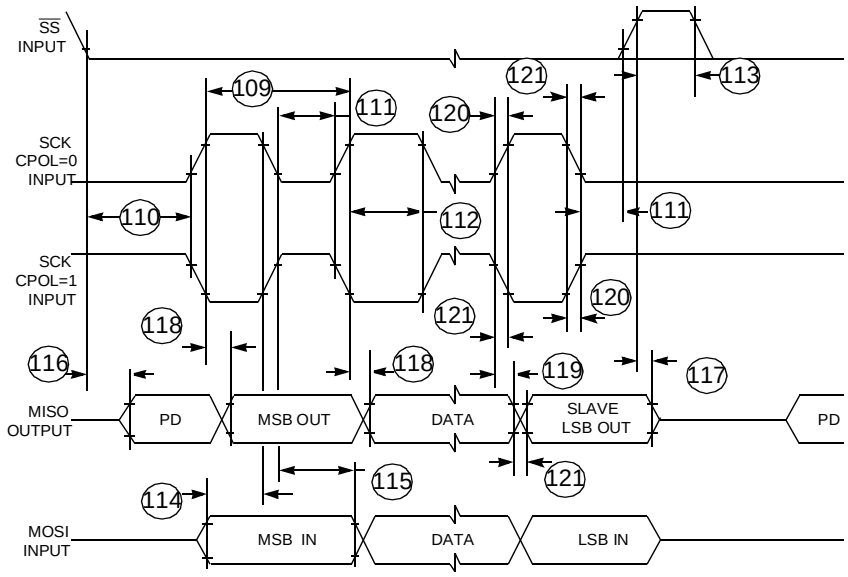


Figure E-44 QSPI Timing – Slave, CPHA = 1

E.18 GPIO Electrical Characteristics

Table E-18 GPIO Timing

($T_A = T_L$ to T_H)

GPIO applies to all pins used as GPIO: SGPIOA[8:31], SQPIOD[0:31], SGPIOC[0:7], QGPIO[0:6], QGPO[1:2], MPIO[0:15], A_PQA[0:7], B_PQA[0:7], A_PQB[0:7], B_PQB[0:7]

Num	Rating	Symbol	Min	Max	Unit
122	Rise Time Input	t_{RI}	—	1	µs
	Output[1] (SLR0 of PDMCR = 0), 50 pF to 200 pF Load	t_{RO}	90	600	ns
	Output[1] (SLR0 of PDMCR = 0), 20 nF Load[2]		2000	7500	ns
	Output (SLR0 of PDMCR = 1), 50 pF Load		3	25	ns
123	Fall Time Input	t_{FI}	—	1	µs
	Output[1] (SLR0 of PDMCR = 0), 50 pF to 200 pF Load	t_{FO}	90	600	ns
	Output[1] (SLR0 of PDMCR = 0), 20 nF Load[2]		2000	7500	ns
	Output (SLR0 of PDMCR = 1), 50 pF Load			25	ns

NOTES:

1. This parameter is tested during initial characterization and is not tested in production.
2. Care should be taken to insure that the total power dissipation of the device remain below the absolute maximum rating under this condition. See **Table E-1**.

E.19 TPU3 Electrical Characteristics

Table E-19 TPU3 Timing

($T_A = T_L$ to T_H)

Num	Rating	Symbol	Min	Max	Unit
124	Slew Rate of TPU Output Channel Valid[1,2] (SLR0 of PDMCR = 0, 50 pF to 200 pF load) (SLR0 of PDMCR = 0, 20 nF load)[3] (SLR0 of PDMCR = 1, 50 pF load)	t_{CHTOV}	 92 2000 3	 650 7550 25	 ns ns ns
125	CLKOUT High to TPU Output Channel Hold	t_{CHTOH}	0	15	ns
126	TPU Input Channel Pulse Width[4]	t_{TIPW}	4	—	t_{cyc}

NOTES:
1. AC timing is shown with respect to 10% V_{DD} & 90% V_{DD} levels.
2. Timing not valid for external T2CLK input.
3. Care should be taken to insure that the total power dissipation of the device remain below the absolute maximum rating under this condition. See **Table E-1**.
4. t_{CYC} is defined as the CLKOUT Period.

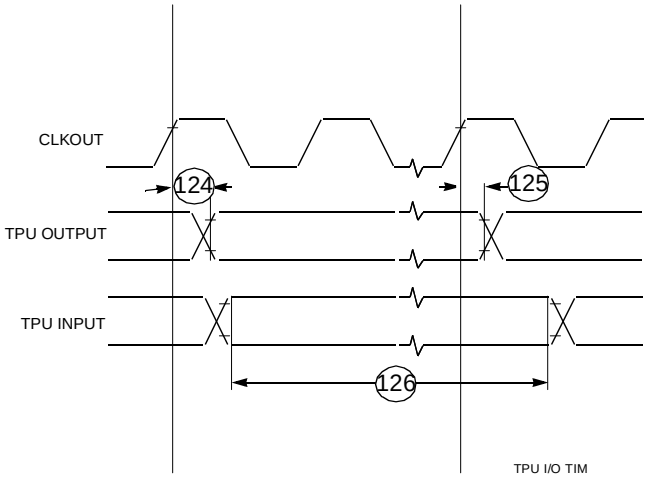


Figure E-45 TPU3 Timing

E.20 TouCAN Electrical Characteristics

Table E-20 TouCAN Timing[1]

($T_A = T_L$ to T_H)

Num	Rating	Symbol	Min	Max	Unit
127	CNTX0 (Delay from ICLOCK)	t_{CNTX0}		19	ns
128	CNRX0 (Set-Up to ICLOCK rise)	t_{CNRX0}		0	ns
	Rise Time Input	t_{RI}		1	µs
127	Output – 50 pF load, SLRC bit of PDMCR = “0” 200 pF load, SLRC bit of PDMCR = “0” 50 pF, SLRC bit of PDMCR = “1”	t_{RO}		 50 100 25	 ns ns ns
	Fall Time Input	t_{FI}		1	µs
128	Output– 50 pF load, SLRC bit of PDMCR = “0” 200 pF load, SLRC bit of PDMCR = “0” 50 pF, SLRC bit of PDMCR = “1”	t_{FO}		 50 100 25	 ns ns ns
	Serial Pins (Maximum frequency)	t_F	1	—	MHz

NOTES:
1. AC timing is shown is tested to the 3-V levels outlined in **E.6 DC Electrical Characteristics**.

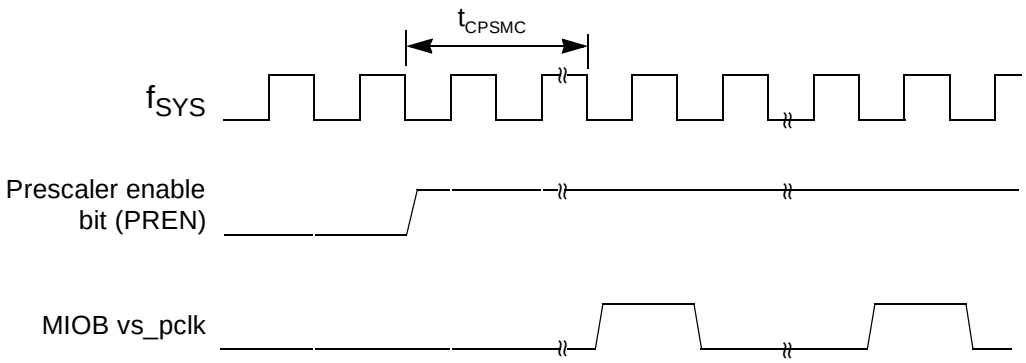
E.21 MIOS Timing Characteristics

All MIOS output pins are slew rate controlled. Slew rate control circuitry adds 90 ns as minimum to the output timing and 650 ns as a maximum. This slew rate is from 10% V_{DD} to 90% V_{DD}, an additional 100 ns should be added for total 0 to V_{DD} slew rate.

Table E-21 MCPSM Timing Characteristics

Characteristic	Symbol	Delay	Unit
MCPSM enable to vs_pclk pulse[1]	t_{CPSMC}	(MCPSMSCR_PSL[3:0]) -1	System Clock Cycles

NOTES:
1. The MCPSM clock prescaler value (MCPSMSCR_PSL[3:0]) should be written to the MCPSMSCR (MCPSM Status/Control Register) before rewriting the MCPSMSCR to set the enable bit (MCPSMSCR_PREN). If this is not done the prescaler will start with the old value in the MCPSMSCR_PSL[3:0] before reloading the new value into the counter.
   Note: after reset MCPSMSCR_PSL[3:0] is set to 0b0000.
   Note: vs_pclk is the MIOS prescaler clock which is distributed to all the counter (e.g., MPWMSM and MMCSM) submodules.



Note 1: f_{SYS} is the internal system clock for the IMB3 bus.
Note 2: The numbers associated with the f_{SYS} ticks refer to the IMB3 internal state.
Note 3: vs_pclk is the MIOS prescaler clock which is distributed around the MIOS to counter modules such as the MMCSM and MPWMSM.

Figure E-46 MCPSM Enable to vs_pclk Pulse Timing Diagram

E.21.1 MPWMSM Timing Characteristics

NOTE

All delays are in system clock periods.

Table E-22 MPWMSM Timing Characteristics

Characteristic	Symbol	Min	Max
PWMSM output resolution	t_{PWMR}	— [1]	2.0 [2]
PWM output pulse[3]	t_{PWMO}	2.0	—
MPWMI input pin to MPWMSCR_PIN status set	t_{PIN}	1	2
CPSM enable to output set[4]	t_{PWMP}	(MPWMPERR - MPWMPULR + 1) * (256 - MPWMSCR_CP) * MCPSMSCR_PSL + 1	
MPWMSM Enable to output set (MIN)[5]	t_{PWME}	(MPWMPERR - MPWMPULR) * (256 - MPWMSCR_CP) * MCPSMSCR_PSL + 3 + (255 - MPWMSCR_CP) * MCPSMSCR_PSL[6]	
MPWMSM Enable to output set (MAX)[5]	t_{PWME}	t_{PWME}(MIN) + MCPSMSCR_PSL - 1[6]	
Interrupt Flag to output pin reset (period start)[7]	t_{FLGP}	(256 - MPWMSCR_CP) * MCPSMSCR_PSL - 1[6]	

NOTES:

1. Minimum output resolution depends on MPWMSM and MCPSM prescaler settings.
2. Maximum resolution is obtained by setting CPSMPSL[3:0] =0x2 and MPWMSCR_CP[7:0] =0xFF.
3. Excluding the case where the output is always “0”.
4. With MPWMSM enabled before enabling the MCPSM. Please also see note *1 on the MCPSM timing information.
5. The exact timing from MPWMSM enable to the pin being set depends on the timing of the register write and the MCPSM vs_pclk.
6. When MCPSMSCR_PSL = 0x0000, this gives a prescale value of 16 and it is 16 which should be used in these calculations. When MCPSMSCR_PSL = 0x0001, the CPSM is inactive.
7. Note: the interrupt is set before the output pin is reset (Signifying the start of a new period).

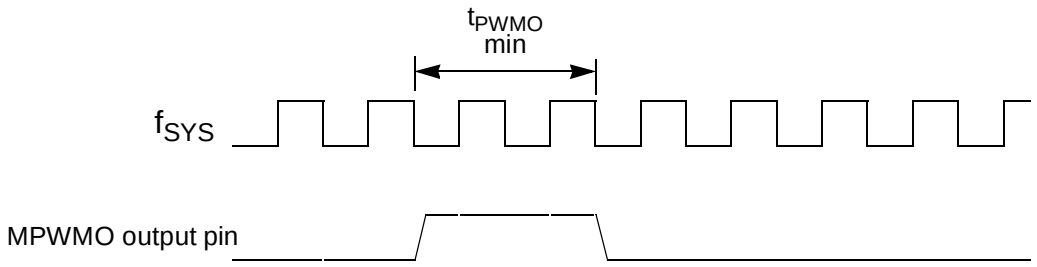


Figure E-47 MPWMSM Minimum Output Pulse Example Timing Diagram

NOTE

f_{SYS} is the internal system clock for the IMB3 bus.

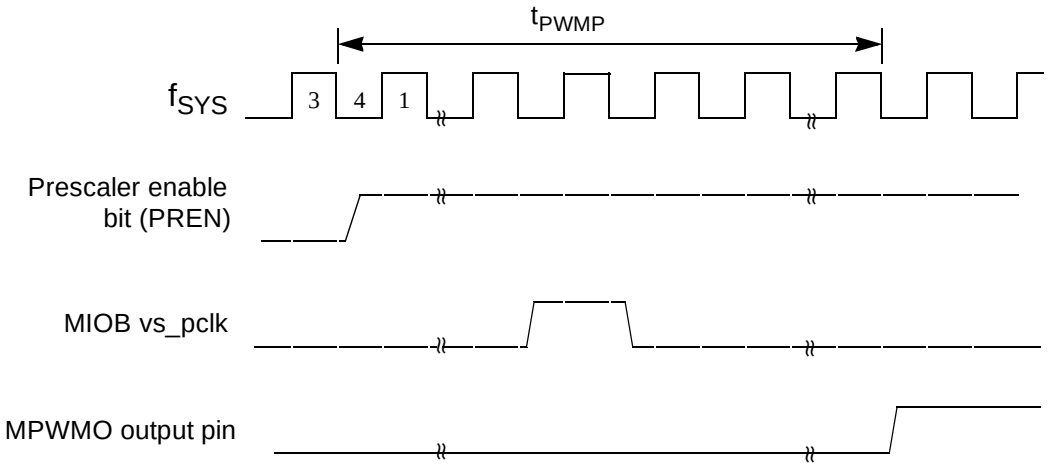


Figure E-48 MCPSM Enable To MPWMO Output Pin Rising Edge Timing Diagram

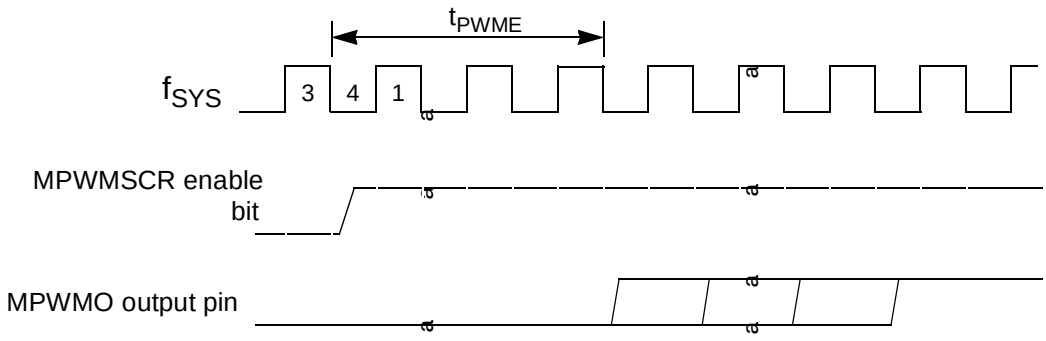


Figure E-49 MPWMSM Enable To MPWMO Output Pin Rising Edge Timing Diagram

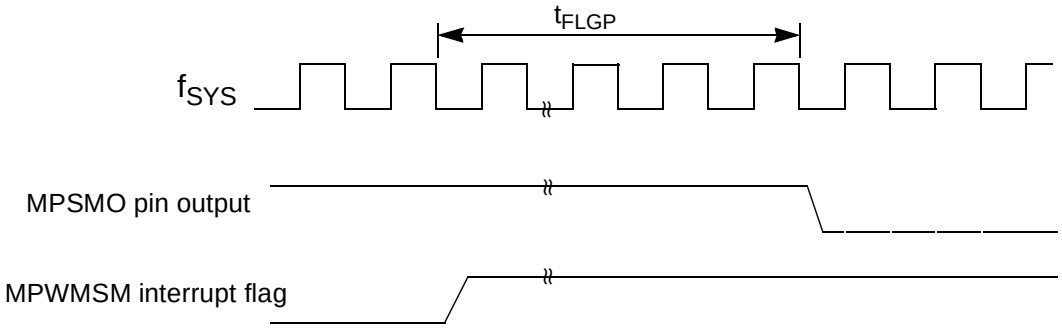


Figure E-50 MPWMSM Interrupt Flag To MPWMO Output Pin Falling Edge Timing Diagram

E.21.2 MMCSM Timing Characteristics

Table E-23 MMCSM Timing Characteristics

Note: All delays are in system clock periods.

Characteristic	Symbol	Min	Max
MMCSM input pin period	t_{PPER}	4	—
MMCSM pin low time	t_{PLO}	2	—
MMCSM pin high time	t_{PHI}	2	—
clock pin to counter bus increment.	t_{PCCB}	1	2
load pin to new counter bus value	t_{PLCB}	1	2
clock pin to PINC delay	t_{PINC}	1	2
load pin to PINL delay	t_{PINL}	1	2
Counter bus resolution	t_{CBR}	—[1]	2 [2]
Counter bus overflow reload to interrupt flag	t_{CBFLG}	1	
MCPSM enable to counter bus increment.	t_{MCMP}	(256 - MMCSMSCR_CP) * MCPSMSCR_PSL + 2	
MMCSM Enable to counter bus increment (MIN) [3]	t_{MCME}	4 + MCPSMSCR_PSL* (255 - MMCSMSCR_CP)[3]	
MMCSM Enable to counter bus increment (MAX)[3]	t_{MCME}	4 + MCPSMSCR_PSL * (255 - MMCSMSCR_CP) + (MCPSMSCR_PSL - 1)[3]	

NOTES:

1. Minimum output resolution depends on MMCSM and MCPSM prescaler settings.
2. Maximum resolution is obtained by setting CPSMPSL[3:0] =0x2 and MMCSMSCR_CP[7:0] =0xFF.
3. The exact timing from MMCSM enable to the pin being set depends on the timing of the MMCSMSCR register write and the MCPSM vs_pclk. The MMCSM enable is taken to mean the MMCSMSCR_CLS[1:0] being written to 2‘b11.

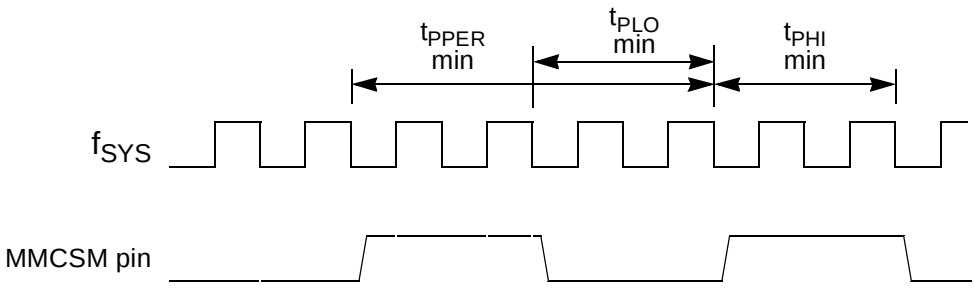


Figure E-51 MMCSM Minimum Input Pin (Either Load Or Clock) Timing Diagram

NOTE

f_{SYS} is the internal system clock for the IMB3 bus.

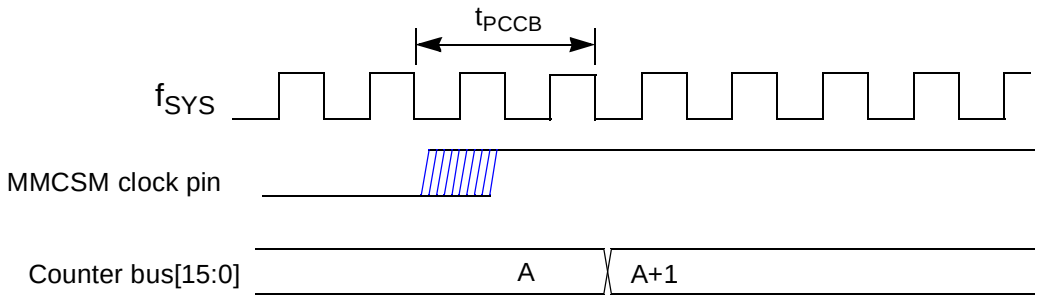


Figure E-52 MMCSM Clock Pin To Counter Bus Increment Timing Diagram

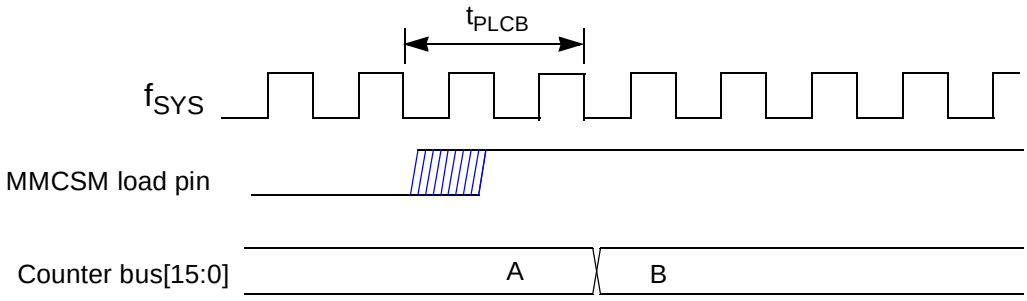


Figure E-53 MMCSM Load Pin To Counter Bus Reload Timing Diagram

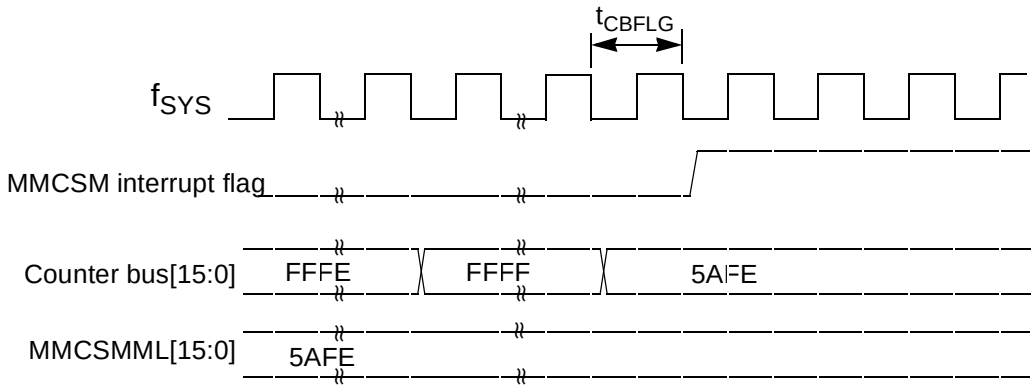


Table E-24 MMCSM Counter Bus Reload To Interrupt Flag Setting Timing Diagram

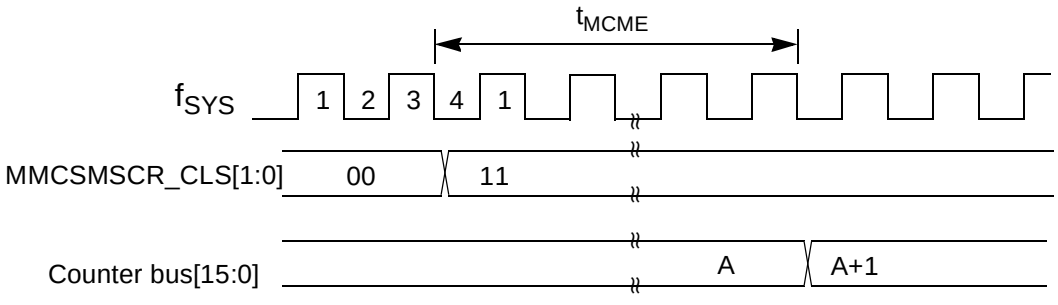


Figure E-54 MMCSM Prescaler Clock Select To Counter Bus Increment Timing Diagram

E.21.3 MDASM Timing Characteristics

Table E-25 MDASM Timing Characteristics

Note: All delays are in system clock periods.

Characteristics	Symbol	Min	Max
Input Modes: (IPWM, IPM, IC, DIS)			
MDASM input pin period	t_{PPER}	4	—
MDASM pin low time	t_{PLO}	2	—
MDASM pin high time	t_{PHI}	2	—
Input capture resolution	t_{CAPR}	—	2
Input pin to Counter Bus capture delay	t_{PCAP}	1	3[1]
Input pin to interrupt flag delay	t_{PFLG}	2	3
Input pin to PIN delay	t_{PIN}	1	2
Counter bus resolution	t_{CBR}	—	2[2]
Output Modes: (OC, OPWM)			
Output pulse width[3]	t_{PULW}	2	—
Compare resolution[3]	t_{COMR}	—	2[2]
Counter Bus to pin change	t_{CBP}	3	
Counter Bus to interrupt flag set.	t_{CBFLG}	3	

NOTES:

1. If the counter bus capture occurs when the counter bus is changing then the capture is delayed one cycle. In situations where the counter bus is stable when the input capture occurs the t_{PCAP} has a maximum delay of two cycles (the one-cycle uncertainty is due to the synchronizer).
2. Maximum resolution is obtained by setting CPSMPSL[3:0] =0x2 and MDASMSCR_CP[7:0] =0xFF.
3. Maximum output resolution and pulse width depends on counter (e.g., MMCSM) and MCPSM prescaler settings.

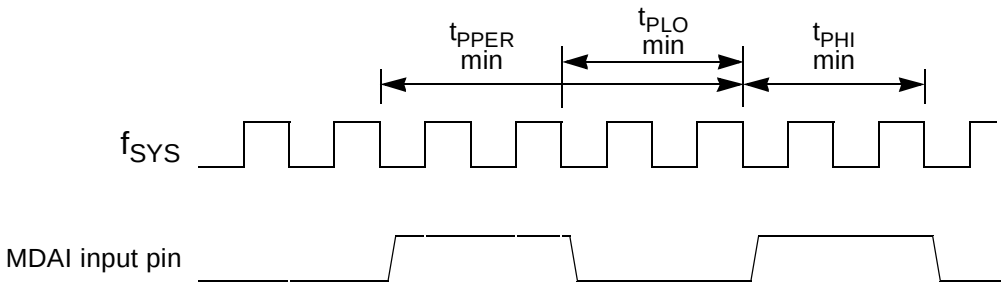


Figure E-55 MDASM Minimum Input Pin Timing Diagram

NOTE

f_{SYS} is the internal system clock for the IMB3 bus.

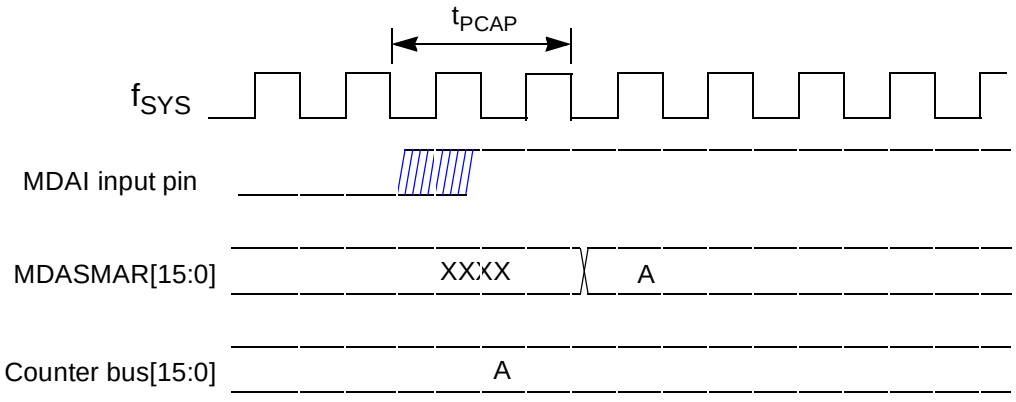


Figure E-56 MDASM Input Pin To Counter Bus Capture Timing Diagram

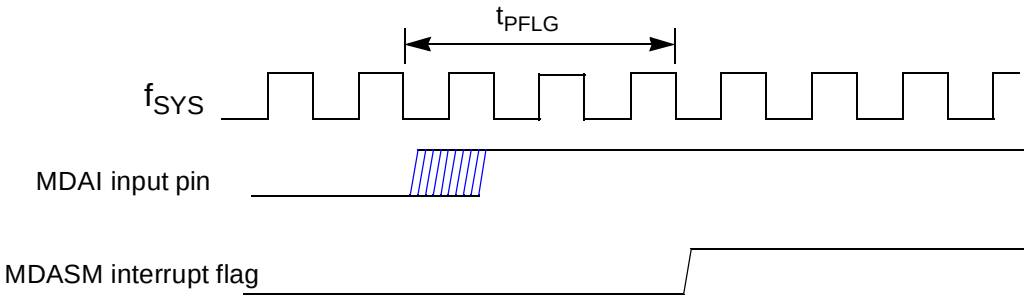


Figure E-57 MDASM Input Pin to MDASM Interrupt Flag Timing Diagram

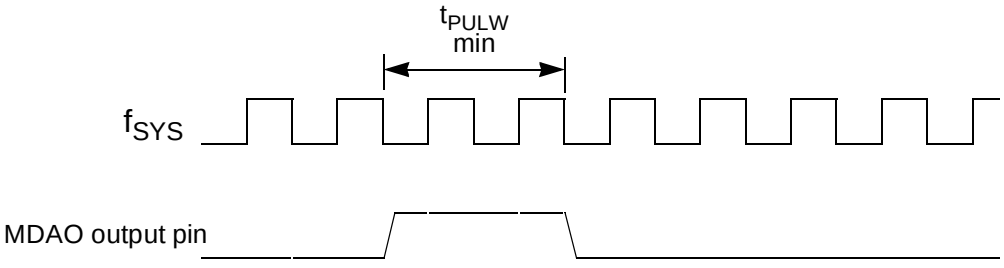


Figure E-58 MDASM Minimum Output Pulse Width Timing Diagram

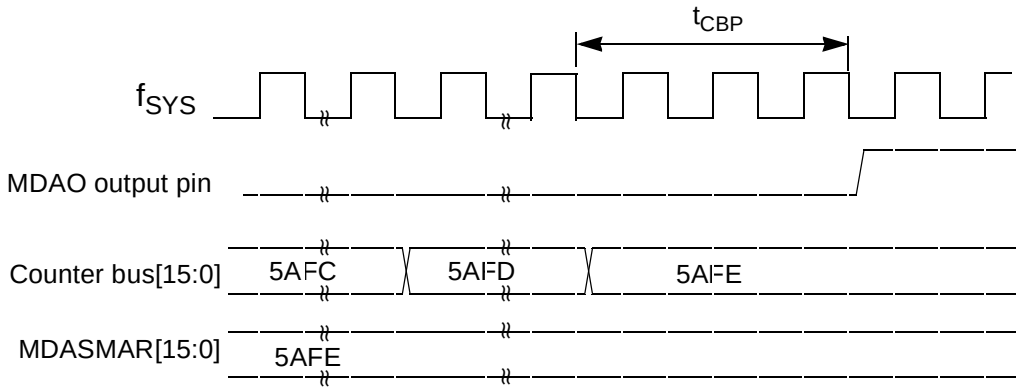


Figure E-59 Counter Bus to MDASM Output Pin Change Timing Diagram

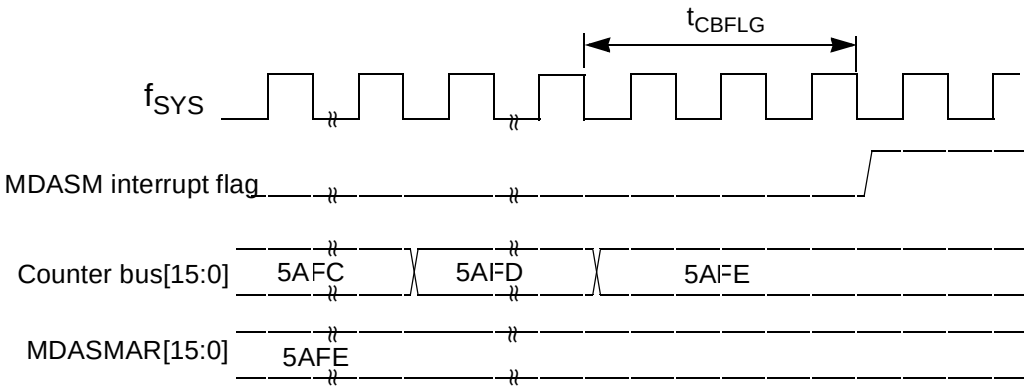


Figure E-60 Counter Bus to MDASM Interrupt Flag Setting Timing Diagram

E.22 MSASM Timing Characteristics

Table E-26 MSASM Timing Characteristics

Note: All delays are in system clock periods.

Characteristics	Symbol	Min	Max
Input Modes: (IC, IOP)			
MSASM input pin period	t_{PPER}	4[1]	—
MSASM pin low time	t_{PLO}	2	—
MSASM pin high time	t_{PHI}	2	—
Input capture resolution	t_{CAPR}	—	2
Input pin to Counter Bus capture delay	t_{PCAP}	1	3[2]
Input pin to interrupt flag delay	t_{PFLG}	3	5
Input pin to PIN delay	t_{PIN}	1	2
Counter bus resolution	t_{CBR}	—	2[3]
Output Modes: (OC, OCT)			
Output pulse width[4]	t_{PULW}	2	—
Compare resolution[4]	t_{COMR}	—	2[4]
Counter Bus to pin change	t_{CBP}	2	
Counter Bus to interrupt flag set.	t_{CBFLG}	3	

NOTES:

1. The minimum input pin period depends on how fast the CPU services the MSASM. The MSASM can respond to a pin changing every four clock periods but the CPU will miss some of the captured values.
2. If the counter bus capture occurs when the counter bus is changing then the capture is delayed one cycle. In situations where the Counter Bus is stable when the input capture occurs the t_{PCAP} has a maximum delay of two cycles (the one-cycle uncertainty is due to the synchronizer).
3. Maximum resolution is obtained by setting CPSMPSL[3:0] =%2 and MSASMSCR_CP[7:0] =%FF.
4. Maximum output resolution and pulse width depends on counter (e.g., MMCSM) and MCPSM prescaler settings.

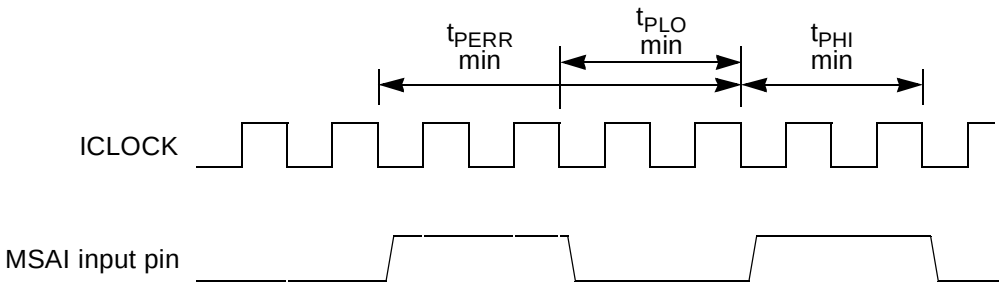


Figure E-61 MSASM Minimum Input Pin Timing Diagram

NOTE

ICLOCK is the internal system clock for the IMB3 bus.

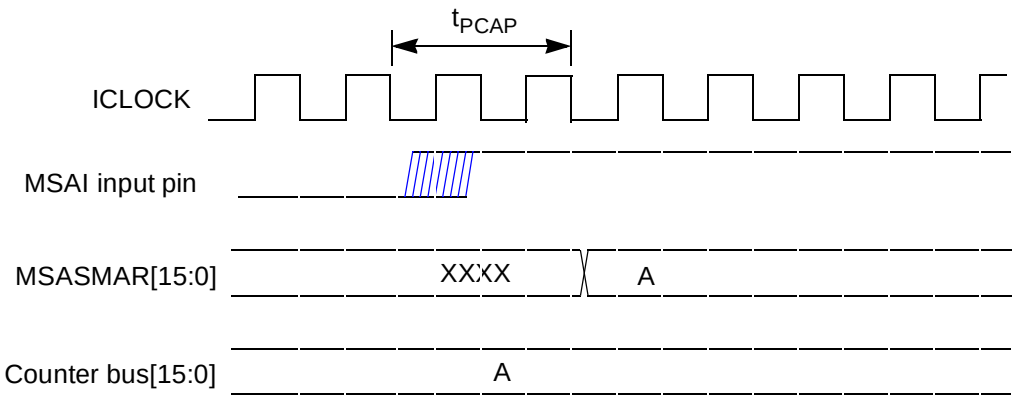


Figure E-62 MSASM Input Pin To Counter Bus Capture Timing Diagram

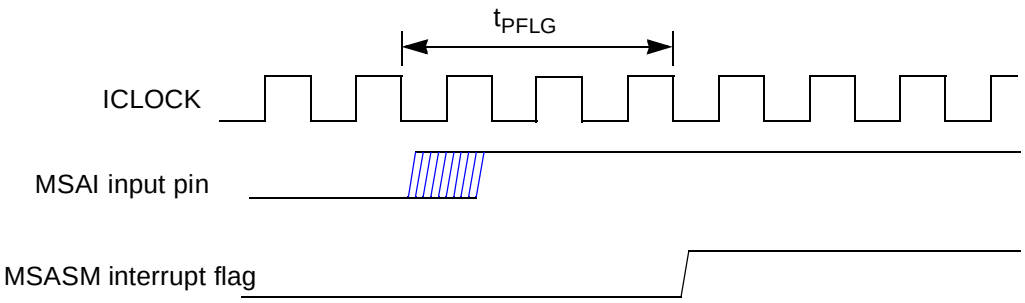


Figure E-63 MSASM Input Pin to MSASM Interrupt Flag Timing Diagram

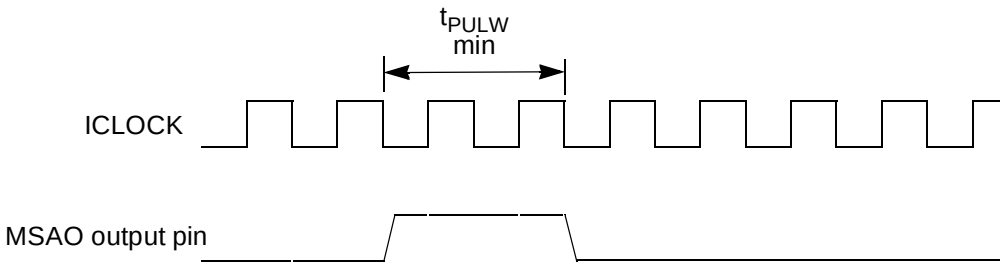


Figure E-64 MSASM Minimum Output Pulse Width Timing Diagram

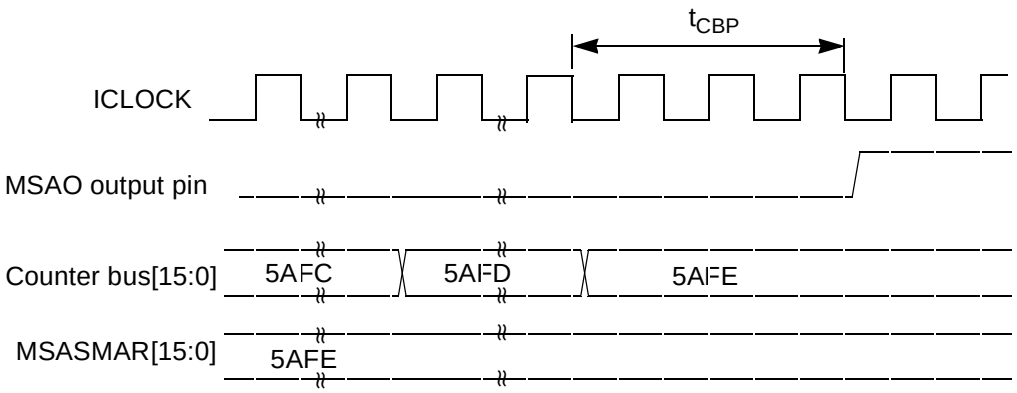


Figure E-65 Counter Bus to MSASM Output Pin Change Timing Diagram

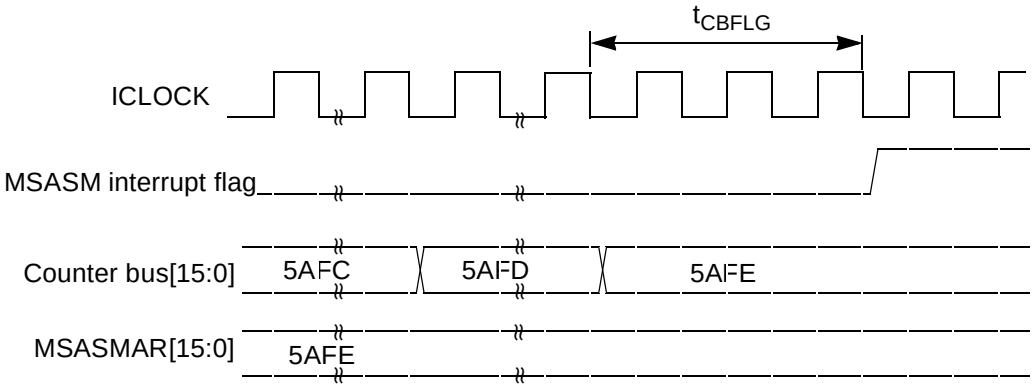


Figure E-66 Counter Bus to MSASM Interrupt Flag Setting Timing Diagram

E.22.1 MPIOSM Timing Characteristics

Table E-27 MPIOSM Timing Characteristics

Note: All delays are in system clock periods.

Characteristic	Symbol	Min	Max
Input Mode			
MPIOSM input pin period	t_{PPER}	—[1]	—
MPIOSM pin low time	t_{PLO}	—[1]	—
MPIOSM pin high time	t_{PHI}	—[1]	—
Input pin to MPIOSM_DR delay	t_{PDR}	0	1
Output mode			
Output pulse width [2]	t_{PULW}	—[2]	—

NOTES:

1. The minimum input pin period, pin low and pin high times depend on the rate at which the MPIOSM_DR register is polled.
2. The minimum output pulse width depends on how quickly the CPU updates the value inside the MIOPSM_DR register.

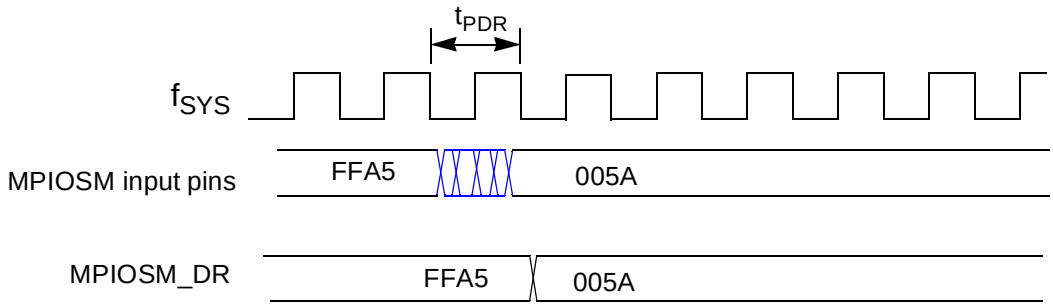


Figure E-67 MPIOSM input pin to MPIOSM_DR (Data Register) Timing Diagram

NOTE

f_{SYS} is the internal system clock for the IMB3 bus.