SECTION 10
CDR MoneT FLASH FOR THE IMB3 (CMFI)

10.1 Overview

The CDR MoneT FLASH for the IMB3 (CMFI) is designed to be used with the Inter-module Bus 3 (IMB3) and consequently any bus master capable of operating the IMB3.

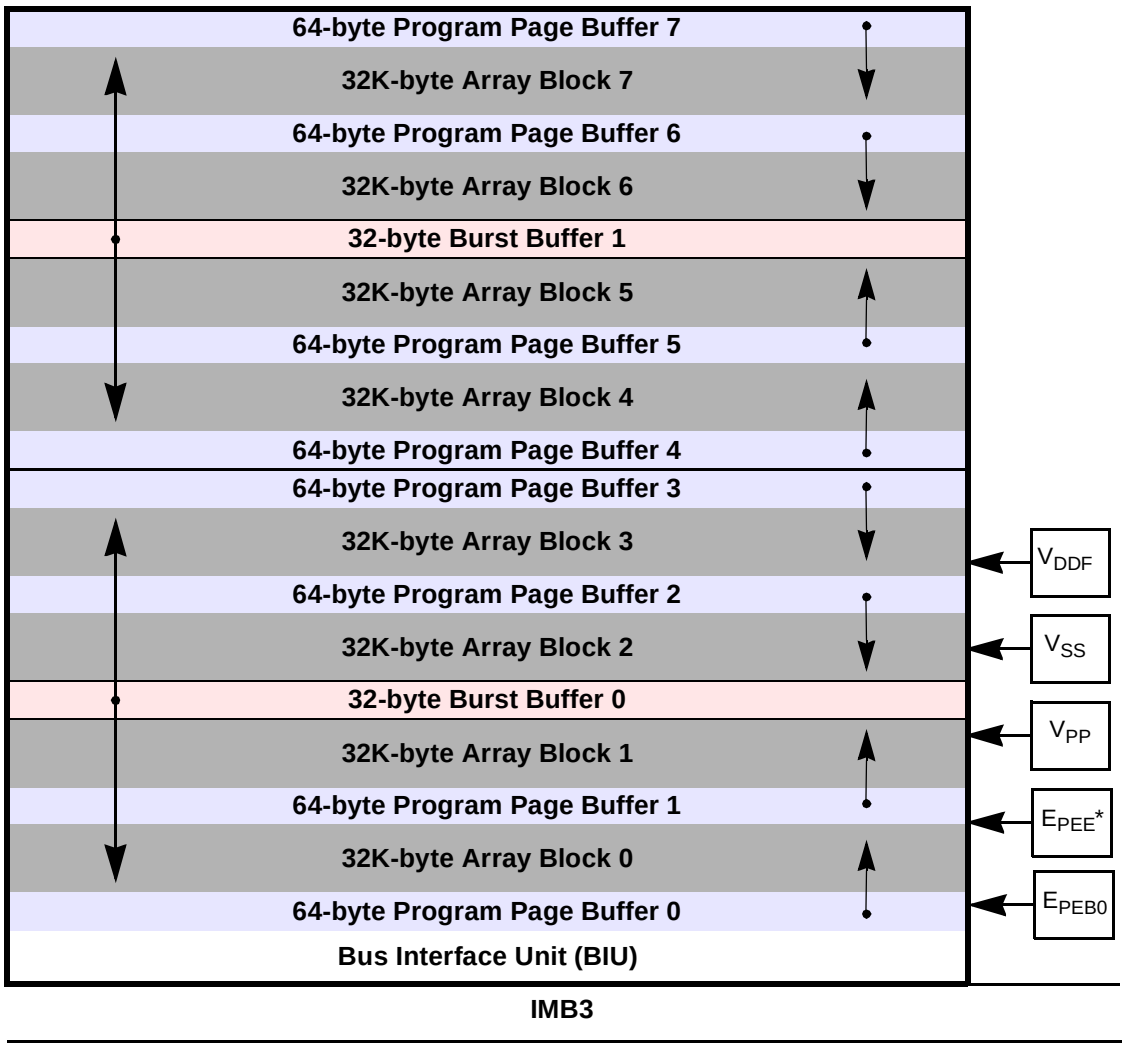
The CMFI array uses the MOTOROLA 1 transistor (MoneT) bit cell configured as 256 Kbytes (262,144 bytes) of non-volatile memory (NVM). The CMFI array is divided into eight 32-Kbyte (32,768-bytes) array blocks.

10.1.1 Overview Description

The primary function of the CMFI EEPROM module is to serve as electrically programmable and erasable NVM to store program instructions and/or data. It is a class of non-volatile solid state silicon memory devices consisting of an array of isolated elements, a means for selectively adding and removing electrical charge to the elements and a means of selectively sensing the stored charge in the elements. When power is removed from the device, the stored charge of the isolated elements will be retained.

The CMFI EEPROM module is arranged into two major sections as shown in **Figure 10-1**. The first section is the MoneT array used to store system programs and data. The second section is the bus interface unit (BIU) that controls access and operation of the CMFI array through a standard IMB3 interface and external signals for:

- E_{PEB0} – Block 0 protect signal
- E_{PEE} - Program enable (note: The EPEE pin is not available on the MC68F375 and is always enabled.)
- V_{PP} – Supplying program and erase power.
- V_{DDF} - Flash operating voltage



* The E_{PEE} pin does not exist on the MC68F375 and is always enabled.

Figure 10-1 Block Diagram for a CMFI EEPROM in the 256-Kbyte Configuration.

The CMFI EEPROM module array is divided into array blocks to allow for independent block erase and multiple block programming. The size of an array block in the CMFI module is a fixed 32 Kbytes. The total CMFI EEPROM array is distributed into 8 blocks. Information is transferred to the CMFI EEPROM through the IMB3 by a long-word (32 bits).

To improve system performance, the BIU accesses information in the array at 32 bytes per access. These 32 bytes are copied into a burst buffer aligned to the low order addresses, IADDR[4:0]. The CMFI contains two non-overlapping burst buffers. The first burst buffer is associated to the lower array blocks. The second burst buffer is associated with the higher array blocks. Read access time of the data in the current burst buffers is 1 system clock, while the time to copy new data into a burst buffer and

access the required information is 2 system clocks. Reads will always begin with a 2 clock access. If the IMB3 indicates a burst access the following access(es) will be 1 clock until the CMFI reaches the end of the burst buffer or the IMB3 terminates the burst access. During the burst reads, the CMFI increments the address by one word each access. The end of the burst buffer is indicated by the highest location within the burst buffer being read, ADDR[4:0] = 0x1F. All burst accesses are aligned to the IMB3 data bus, ignoring the byte address(es). To prevent the BIU from unnecessarily accessing the array, the CMFI EEPROM shall monitor the IMB3 address to determine if the required information is in one of the two current burst buffers and the access is valid for the module. This process is designed to reduce power consumption by the CMFI.

In normal operation write accesses to the CMFI array are not recognized.

The CMFI EEPROM module requires an external program or erase voltage, V_{PP}, to program or erase the array or any of its control register shadow bits. Special control logic is included to require a specific series of read and write accesses before program or erase operation is allowed.

To improve program performance, the CMFI programs up to eight unique 64-byte pages simultaneously in eight separate array blocks. These 64 bytes are aligned to the low order addresses, IADDR[5:0], to form a program page buffer. Each of the pages being programmed simultaneously are located at the same block offset address, IADDR[23:15|14]. Erase is performed on one or more of the selected array blocks simultaneously.

10.1.2 Features of the CMFI

- MOTOROLA's 1 transistor, MoneT, FLASH bit cell.
- -40 to 125° C operating temperature range.
- V_{DD} 3. 0 V to 3. 6 V operating range.
  - — Operational at 2. 7 V**.**
  - — Up to 40 MHz operation at V_{DD} = 3. 0 V, 150° C = T_J.
- Shadow and bootstrap information stored in special FLASH NVM locations.
- 256-Kbyte array size.
- Array distributed in 8 blocks.
  - — Erase by array block(s).
  - — Common array block size of 32 Kbytes.
  - — Array lock protection for program and erase operations.
    - Built-in margin reads for both program and erase verify reads.
    - Array access disabled while programming or erasing.
  - — Array address attributes restriction control.
    - Select between supervisor and supervisor/user spaces.
    - Select between data and instruction/data spaces.
- Program up to 512 bytes at a time.
  - — Program up to eight 64-byte pages simultaneously.
  - — Pages located at the same offset address.
- Self-timed program and erase pulses.
  - — Internal pulse width timing control using system clock frequencies from 8.0

MHz to 40.0 MHz.
  — Program pulses from 4.0 µs to 2.73 ms.
  — Erase pulses from 4.096 ms to 2.796 s.
- External 4.75 to 5.25 V V_{PP} program and erase power supply.
- Array block 0 enable is selected from one of two sources:
  — A pin external to the device (EPEB0)
  — The inverted state of the CMFI PROTECT bit.
- Data word length of 16 bits.
- Supports IMB3 burst read accesses.
  — Contains two separate non-sequential burst buffers.
  — Burst buffer size of 32 bytes.
  — Burst terminated at end of buffer or by IMB3.
- Software mapping to establish array base address.
- Emulation support
  — Support for integration modules with external emulation through a special chip select.
  — Supports internal emulation through memory overlay option.
- Low power disable via the integration module.
- Wait states for integration from slower external memory.

10.1.3 Glossary of terms used in the CMFI EEPROM Specification

Array block — CMFI array subdivision: a 32-Kbyte contiguous block of information. Each array block may be erased independently.

BIU — Bus interface unit controls access and operation of the CMFI array through a standard IMB3 interface.

Burst read — Array read operation that requires 2 clocks for the first data access and 1 clock for the following data accesses.

CMFI — The CDR MoneT FLASH EEPROM for the IMB3.

Erase interlock write — A write to any CMFI array address after initializing the erase sequence.

Erase margin read — Special burst buffer updates of the CMFI array where the CMFI EEPROM hardware adjusts the reference of the sense amplifier to check for correct erase operation. All CMFI array burst buffer updates between the erase interlock write and clearing the SES bit are erase margin reads.

IM — Integration module.

IMB3 — A motherboard-on-a-chip for embedded controller designs.

Notable features of the bus architecture include: burst data transfers, multiple bus masters, exception processing support, address space partitioning, multiple interrupt levels, vectored interrupts, and extendable bus cycles via wait state insertion.

The IMB3 provides a flexible, high performance bus capable of supporting a family of parts.

Initialize program/erase sequence — The write to the high voltage control register that changes the SES bit from a 0 to a 1.

Master reset — The hardware reset that resets the entire CMFI.

MoneT — The CMFI EEPROM's FLASH bit cell.

Over programmed — By exceeding the specified programming time and/or voltage, a CMFI bit may be over programmed. This bit causes erased bits in the same column on the same array block to read as programmed.

Programming write — A word write to a CMFI array address to transfer information into a program page buffer. The CMFI EEPROM accepts programming writes after initializing the program sequence until the EHV bit is changed from a 0 to a 1.

Program margin read — Special burst buffer updates of the CMFI array where the CMFI EEPROM hardware adjusts the reference of the sense amplifier to check for correct program operation. All CMFI burst buffer updates between the first programming write and clearing the SES bit are program margin reads.

Program page buffer — 64 bytes of information used to program the CMFI array. This information is aligned to a 64-byte boundary within the CMFI array. Each CMFI module has 1 program page buffer per block.

Read burst buffer — 32-byte block of information that is read from the CMFI array. This information is aligned to a 32-byte boundary within the CMFI array. Each CMFI module has two non-sequential burst buffers.

Reserved registers — A location within the control register block which may have one or more bits that are reserved for use by Motorola. These bits are not available for normal use.

Shadow information — An extra row (256 bytes) of the CMFI array used to provide reset configuration information. This row may be accessed by setting the SIE bit in the module configuration register and accessing the CMFI array, see **10.4.3 CMFI EEPROM Configuration Register (CMFIMCR)**. The shadow information is always in the lowest array block of the CMFI array.

System reset — A reset generated under software control that clears the high voltage enable (EHV) bit of the CMFICTL register and forces the BIU into a state ready to receive a new IMB3 access.

10.2 CMFI EEPROM Interface

The CMFI module contains a slave BIU to the IMB3. The BIU controls access and operation of the array through standard IMB3 reads and writes of the array and register blocks in the CMFI module. Additionally, the CMFI uses external signals to provide control and power to the module. These other external signals include an optional sig-

nal to externally control program or erase operations to array block 0 (E_{PEB0}). Three other pins: V_{SSF} V_{DD3F} and V_{PP} provide power to the module.

10.2.1 External Interface

The CMFI EEPROM module uses external signals to provide some external control of operations and provide power. These signals are listed in **Table 10-1**.

Table 10-1 CMFI EEPROM Module External Signals

Description	MNEMONIC	Comments
Internal memory patch signals	INTPATCHB	These signals signify that the current bus cycle will be provided by the internal patch memory instead of the CMFI. The CMFI EEPROM BIU will force an aborted access to the CMFI if any of the four patch signals = “1” to remain synchronized with the IMB3. Thus the CMFI will not assert the data, data transfer acknowledge or burst transfer acknowledge if any of the internal memory patch signals = “1”.
Master program and erase enable	E_{PEE}	This optional signal externally controls program or erase operation. To enable these operations the signal should be at the logic "1" level, while a logic "0” level disables these operations in the CMFI module. The E_{PEE} signal includes a pull down device to keep a logic "0” unless the pin is driven to a logic "1” and a digital filter to protect from external noise. On the MC68F375, this signal is connected to V_{DD} to allow program and erase operations at all times.
Block 0 program and erase enable	E_{PEB0}	This optional signal will externally control program or erase operations to array block 0. To enable these operations the signal should be at the logic “1” level, while a logic “0” level disables these operations in the CMFI Module. This signal may be generated by any desired method and must remain valid throughout the program or erase software starting their respective operation. The E_{PEB0} pin will include a pull down device to keep a logic “0” unless the pin is driven to a logic "1” and a digital filter to protect from external noise. When not connected to E_{PEB0} this signal will be connected to V_{DD} to allow program and erase operations.
CMFI ground	V_{SSF}	To reduce noise in the read path no other circuits should be connected to the CMFI V_{SSF} supply. A maximum of 2 CMFI Modules may be connected to a V_{SSF} supply pin. This V_{SSF} pin must be isolated from all other V_{SS} pins inside the device.
CMFI power supply	V_{DDF}	To reduce noise in the read path no other circuits should be connected to the CMFI V_{DDF} supply pin. A maximum of 2 CMFI Modules may be connected to a V_{DDF} supply pin. This V_{DDF} pin must be isolated from all other V_{DD} pins inside the device. The specified voltage range during operation is 3. 0 V to 3. 6 V.
Program and erase high voltage supply	V_{PP}	V_{PP} provides the high voltage (4. 75 V to 5. 25 V) used during program and erase operations of the CMFI Module. A maximum of 2 CMFI Modules may be connected to a V_{PP} supply pin. The suggested voltage at the V_{PP} pin should be equal to the V_{DD} voltage during all operations except program and erase.

10.3 Programmer's Model

The CMFI EEPROM module consists of two addressed sections. The first is the 32-byte control registers section used to configure, program, erase and test the CMFI EEPROM array, while the second is the array. **Table 10-2** represents how the IMB3 addresses correspond to the CMFI EEPROM control register and array mapping.

Table 10-2 CMFI EEPROM Memory Map with 32-Bit Word

<table>
<tr><th>Control Register</th><th colspan="3">32-Kbyte Blocks</th><th>IMB3 Address</th></tr>
<tr><td rowspan="16">Control Register Hardware Mapping Addresses</td><td colspan="3" rowspan="5">Array Mapping Addresses</td><td>23</td></tr>
<tr><td>22</td></tr>
<tr><td>21</td></tr>
<tr><td>20</td></tr>
<tr><td>19</td></tr>
<tr><td colspan="2"></td><td>18</td></tr>
<tr><td colspan="2"></td><td>Array Hardware Mapping or Block Address[1]</td><td>17</td></tr>
<tr><td>Array Hardware Mapping or Block Address[1]</td><td rowspan="2">Block Addresses</td><td rowspan="2">Block Addresses</td><td>16</td></tr>
<tr><td rowspan="2">Block Addresses</td><td>15</td></tr>
<tr><td rowspan="8">Row Addresses</td><td rowspan="8">Row Addresses</td><td>14</td></tr>
<tr><td>13</td></tr>
<tr><td>12</td></tr>
<tr><td>11</td></tr>
<tr><td>10</td></tr>
<tr><td>9</td></tr>
<tr><td>8</td></tr>
<tr><td colspan="3">Column Addresses</td><td>7</td></tr>
<tr><td>6</td></tr>
<tr><td rowspan="3">Control Register Select Addresses</td><td>32-Byte Read Page Select</td><td rowspan="3">Program Page Word Addresses</td><td>32-Byte Read Page Select</td><td>5</td></tr>
<tr><td rowspan="3">Read Burst Buffer Word Addresses</td><td rowspan="3">Read Burst Buffer Word Addresses</td><td>4</td></tr>
<tr><td>3</td></tr>
<tr><td>2</td></tr>
<tr><td colspan="4">Byte Addresses</td><td>1</td></tr>
<tr><td colspan="4"></td><td>0</td></tr>
</table>

NOTES:
1. The high order address of the block addresses selects the read burst buffer.

10.4 CMFI EEPROM Control Block

The 32-byte control block contains registers which are used to control CMFI EEPROM module operation. Configuration information is specified and programmed independently from the contents of the CMFI EEPROM array. There are three registers provided for configuration and control of the CMFI EEPROM module:

- The module configuration register (CMFIMCR)
- Array base address register (CMFIBAR)
- CMFI EEPROM high voltage control register (CMFICTLx).

Control bits in these registers are provided to control array operation, programming and erasing.

Some of the control registers have shadow information words which physically exist in a spare CMFI EEPROM row. On master reset, some of the registers and fields within certain registers are loaded with default reset information from the shadow information words. Writing to a register does not alter the contents of the corresponding shadow information word. Using the address of the corresponding control register, the shadow information word is programmed in the same manner as a location in the CMFI EEPROM array. When data is latched into the programming latches while programming a shadow information word, it will not be written to the register itself. Data which is programmed into the CMFIMCR, CMFIBAR or CMFICTL register's shadow information word will not be copied into the register until the next master reset.

The last write to a programming buffer prior to setting EHV determines the value to be programmed. The registers that are loaded from shadow information words during master reset are identified in the individual register field and control bit descriptions. The shadow information words are erased whenever the low block (block 0) of the array is erased.

10.4.1 CMFI EEPROM Module Control Block Addressing

The module control block is addressed by comparing the module control mapping (IMODMAP) to IADDR[23] while IADDR[22:5] are decoded by the CMFI EEPROM module. If the CMFI EEPROM control block address is decoded, the CMFI EEPROM module will assert the address acknowledge (IAACKB) signal. The value of IADDR[22:5] is defined for each device that has a CMFI EEPROM module. These bits are fixed for a particular device (MCU or peripheral), and are specified by Motorola. The value of the module control mapping (IMODMAP) is specified by a control bit in the module configuration register, see **10.4.3 CMFI EEPROM Configuration Register (CMFIMCR)**. The exact register addressing within the control block is determined by IADDR[4:0]. The control block is restricted to supervisor data space (IFC[2:0] = 0b101). Any other address space read or write of the registers will not assert address acknowledge. See **Table 10-3** for control register offset addresses.

Table 10-3 CMFI Control Register Addressing

Address	Control Register	
0xYF F800[1]	Module Configuration (CMFIMCR)	
0xYF F802	RESERVED	
0xYF F804	CMFITST	
0xYF F806	RESERVED	
0xYF F808	CMFIBAR	Base Address High (CMFIBAH)
0xYF F80A		Base Address Low (CMFIBAL)
0xYF F80C	CMFICTL	High Voltage Control 1 (CMFICTL1)
0xYF F80E		High Voltage Control 2 (CMFICTL2)
0xYF F810 to 0xYF F816	CMFIBS[3:0]	
0xYF F818 to 0xYF F81E	RESERVED	

Registers with shadow information word (erased bit state: 0b1).

NOTES:

1. The "Y" in the address is determined by the state of the MM bit in the SCIMMCR.

10.4.2 Reserved Register Accesses

The IMB3 does not support accesses to reserved registers. An internal BERR protocol will terminate with a bus error for all accesses to a reserved register. Also, the data returned by the BIU is undefined and a write access will have no effect for a reserved register.

10.4.3 CMFI EEPROM Configuration Register (CMFIMCR)

The CMFI EEPROM module configuration register is used to control the operation of the CMFI EEPROM array and the BIU.

CMFIMCR — CMFI EEPROM Configuration Register **0xYF F800**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STOP	PROTECT	SIE	$\overline{\text{BOOT}}$	$\overline{\text{LOCK}}$	EMUL	ASPC		WAIT		0	0	0	0	0	0
RESET:[1]															
U[2]	1	0	U[3]	1	U[4]	U[5]		U[6]		—	—	—	—	—	—

NOTES:

1. The default values of some bits in the CMFIMCR are read from the location 0 of the shadow row.
2. Reset state is defined by a shadow bit **or** the state of D15 during reset mode configuration.
3. Reset state is defined by a shadow bit.
4. Reset state is defined by D[10] or the state of D[13] during reset mode configuration.
5. Reset state is defined by a shadow bit, bit is write protected by $\overline{\text{LOCK}}$ and STOP.
6. Reset state is defined by a shadow bit, bit is write protected by $\overline{\text{LOCK}}$.

Table 10-4 CMFIMCR Bit Settings

Bit(s)	Name	Description
15	STOP	Stop control. When the STOP control bit is a 1, the CMFI EEPROM array is disabled. It will not respond to the base address stored in CMFIBAR. STOP will prevent read accesses to the array and to the shadow information words, but has no effect on accesses to the control registers. Attempts to read any shadow information word while STOP = 1 will produce indeterminate results. With STOP = 1 the CMFI may enter the lower power clock stop operation, see **4.4.9 Low Power Stop Mode**. If STOP is set during programming or erasing, the program and erase voltage will automatically be turned off by clearing the EHV bit. The state of this bit after master reset is the logical OR of the inverted state of D[15] and the STOP shadow bit, STOP = D[15] or STOP shadow bit. If STOP is set to a 1 by D[15] or the STOP shadow bit during master reset, the array may be re-enabled by clearing STOP after master reset. This bit is read/write always. 0 = The CMFI EEPROM module is in normal mode of operation. 1 = Causes the CMFI EEPROM module to enter low power STOP operation.
14	PROTECT	Prevent array program/erase. The CMFI EEPROM array and shadow information are protected from program and erase operation by setting PROTECT = 1. The CMFI BIU will perform all programming and erase interlocks except the program and erase voltages will not be applied to locations within the array if PROTECT = 1 Read always, Write when $\overline{\text{LOCK}}$ = 1 and SES = 0. 0 = All NVM bits are unprotected. 1 = All NVM bits are protected.

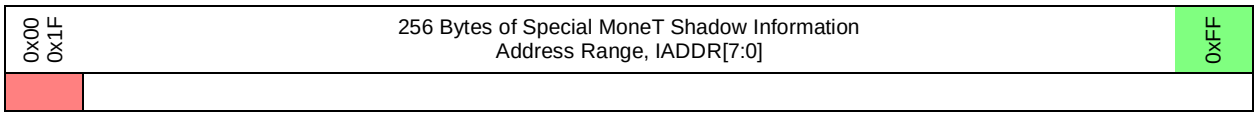
Table 10-4 CMFIMCR Bit Settings (Continued)

Bit(s)	Name	Description
13	SIE	Shadow information enable. The SIE bit is write protected by the start end sequence (SES) bit for programming operation. Writes will have no effect if SES = 1 and PE = 0. The SIE bit can be read whenever the registers are enabled. When an array location is read in this mode, the shadow information will be read from a location determined by the column, 32-byte read page select, and word addresses (IADDR[7:0]) of the access. Accessing the CMFI control block registers will access the registers and not the shadow information. The default reset state of SIE is normal array access (SIE = 0). The address range of the shadow information is the entire address range of the CMFI EEPROM array but the high order array addresses, IADDR[17|16|15:7], are not used to encode the location. The first 32 bytes (IADDR[7:0] = 0x00 to 0x1F) of the 256 bytes of shadow locations are withheld by Motorola for the register shadow information words. The remaining 224 bytes are available for general use. This is shown in **Figure 10-3**. The upper address bits (IADDR[7:6]) are forced to 0 during reset. When SIE = 1, only the program page buffer associated with the lowest block can be programmed. The other program page buffers cannot be accessed and will not apply any programming voltages to their CMFI array blocks while programming the shadow information. The shadow information is typically in block 0 except for when the 192K-byte and 96K-byte arrays are mapped high, then the shadow information is in block 2. 0 = Normal array access. 1 = Disables normal array access and selects the shadow information.
12	$\overline{\text{BOOT}}$	Boot control. After reset, the $\overline{\text{BOOT}}$ bit may be cleared or set via a write to CMFIMCR; however, it will not affect bootstrap operation. If the STOP bit is set (STOP = 1) then bootstrap operation will be terminated. While the CMFI EEPROM is configured to provide the bootstrap information and read access to the control block, the CMFI array will not provide correct data. Control block writes will not be affected by bootstrap operation. 0 = The CMFI will respond to bootstrap address after reset. 1 = The CMFI will not respond to bootstrap address after reset.
11	$\overline{\text{LOCK}}$	Lock control. In normal operation once the $\overline{\text{LOCK}}$ bit is asserted ($\overline{\text{LOCK}}$ = 0) the write-lock can only be disabled again by a master reset. The $\overline{\text{LOCK}}$ bit is writable if the device is in background debug mode (IFREEZEB = 0). When the $\overline{\text{LOCK}}$ control bit in the CMFIMCR register is asserted ($\overline{\text{LOCK}}$ = 0) the write-lock register bits ASPC, WAIT, PROTECT, EMUL and CMFIBAH are locked. Writes to these bits will have no effect. Read always, clear once unless in background debug mode. 0 = Write-locked registers are protected. 1 = Write-lock is disabled.
10	EMUL	Emulation operation. When the EMUL control bit in the CMFIMCR register is a 1, the CMFI EEPROM is placed in emulation operation. Emulation operation may be entered by writing EMUL to a 1 on devices that support emulation operation; otherwise, writes have no operational effect. The state of this bit after master reset is the logical NOR of EMULIN and EMULEN, EMUL = $\overline{\text{EMULIN}}$ and $\overline{\text{EMULEN}}$. Emulation operation allows the array to be emulated externally, with access controlled by the CMFI EEPROM.
9:8	ASPC	Array space. The array may be specified to exist in supervisor or unrestricted space. The default reset state of ASPC is programmed in a CMFI EEPROM shadow bit by the user. ASPC may be written by the bus master any time STOP = 1 and $\overline{\text{LOCK}}$ = 1. The ASPC bits govern accesses to the array, but have no effect on how control registers and shadow registers are accessed. 00 = Unrestricted data space (IFC = x01), unrestricted program space (IFC = x10) 01 = Unrestricted program space (IFC = x10) 10 = Supervisor data space (IFC = 101), supervisor program space (IFC = 110) 11 = Supervisor program space (IFC = 110)

Table 10-4 CMFIMCR Bit Settings (Continued)

Bit(s)	Name	Description
7:6	WAIT	Wait states. The WAIT field is used to specify the number of wait states inserted by the BIU during accesses. These wait states are added to the bus cycle between the IMB3 asserting data strobe (IDSB) and the CMFI EEPROM writing or reading data. For burst accesses, the wait states are inserted for the first data access only. A wait state has a duration of one system clock cycle. This feature allows the migration of storage space from a slower emulation or development system memory to the MC68F375 without the need for re-timing the system. The program and erase margin reads will extend the bus cycle to their respective timings regardless of the value of WAIT. Read always, writable if $\overline{\text{LOCK}}$ = 1. 00 = Minimum bus cycles = 3 clocks, 1 inserted wait states 01 = Minimum bus cycles = 4 clocks, 2 inserted wait states 10 = Minimum bus cycles = 5 clocks, 3 inserted wait states 11 = Minimum bus cycles = 2 clocks, 0 inserted wait states
5:0	—	Reserved

Figure 10-2



Shadow information words and locations withheld by Motorola for future applications.

General use special MoneT shadow information.

Figure 10-3 Shadow Information

WARNING

If a CMFI EEPROM enables the lock protection mechanism ($\overline{\text{LOCK}}$ = 0) before PROTECT is cleared the device must use background debug mode (IFREEZEB = 0) to program or erase the CMFI EEPROM.

10.4.4 CMFI EEPROM Test Register (CMFITST)

The CMFI EEPROM test register is used to control the test operation of the CMFI EEPROM array and BIU. Only 6 bits are read/writeable in the CMFITST register (in supervisor mode only).

CMFITST — CMFI EEPROM Test Register **0xYF F804**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RESERVED				NVR[1]	PAWS[2]			RESERVED	STE[1,3]	GDB[1]	RESERVED				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTES:
1. The NVR, STE, and GDB bits are not accessible in all revisions of the MC68F375 (prior to the J61X mask set).
2. The PAWS bits are not accessible in all revisions of the MC68F375.
3. The STE bit should always be programmed as a 0.

Table 10-5 CMFITST Bit Settings

Bit(s)	Name	Description
15:12	—	Reserved
11	NVR	Negative voltage range. This bit switches between the low and high voltage range of the negative charge pump in programming and erasing the CMF Flash module when GDB = 0b1. This bit is writeable when HVS = 0b0. 0 = High Range (more negative) 1 = Low Range
10:8	PAWS[0:2]	Program amplitude/width modulation select. The PAWS bits can be used to select the programming voltage applied to the drain of the EEPROM bitcell. These bits should be left-set to 000. For information about PAWS programming modes, see **Table 10-6**.
7	—	Reserved
6	STE	This bit is reserved for Motorola factory testing and should always be programmed to 0b0. 0 = Normal Operation 1 = Factory test mode use only. This setting could disturb contents of flash
5	GDB	Gate/drain bias select. This bit works in conjunction with the PAWS bits to select between positive and negative ramped voltages for programing and erasing. This bit is writeable when SES = 0b0. 0 = Positive voltage ramp selected on the bitcell drain 1 = Negative voltage ramp selected on the bitcell gate
4:0	—	Reserved

Table 10-6 CMF Programming Algorithm (v6 and Later)

No. of Pulses	Pulse Width	NVR	PAWs	GDB	PAWs Mode	Description
4	256 µs	1	100	1	Mode 4NL	Negative gate ramp (low range)
4	256 µs	1	101	1	Mode 5NL	
4	256 µs	1	110	1	Mode 6NL	
4	256 µs	1	111	1	Mode 7NL	
20	50 µs	0	100	1	Mode 4NL	Negative gate ramp (high range)
20	50 µs	0	101	1	Mode 5NL	
20	50 µs	0	110	1	Mode 6NL	
max. 10,000	50 µs	0	111	1	Mode 7NL	

Table 10-7 CMF Erase Algorithm (v6)

No. of Pulses	Pulse Width	NVR	PAWs	GDB	PAWs Mode	Description
1	100 ms[1]	1	100	1	Mode 4NL	Negative gate ramp (low range)
1	100 ms[1]	1	101	1	Mode 5NL	
1	100 ms[1]	1	110	1	Mode 6NL	
1	100 ms[1]	1	111	1	Mode 7NL	
1	100 ms[1]	0	100	1	Mode 4NL	Negative gate ramp (high range)
1	100 ms[1]	0	101	1	Mode 5NL	
1	100 ms[1]	0	110	1	Mode 6NL	
20	100 ms[2]	0	111	1	Mode 7NL	

NOTES:
1. No margin read after pulse.
2. Do margin read after each pulse.

10.4.5 CMFI Base Address Registers (CMFIBAR)

The CMFI base address register is used to set the base address of the CMFI flash module. It consists of two 16-bit registers, CMFIBAH and CMFIBAL. On a 256-Kbyte CMFI module, the base address of the module should be on a 256-Kbyte boundary, therefore CMFIBAH[7:16] and CMFIBAL[15:12] should be set to zero.

CMFIBAH — CMFI Base Address High Register 0xYF F808

MSB 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	LSB 16
RESERVED								**CMFIBAH[1]**							
RESET:															
0	0	0	0	0	0	0	0	U	U	U	U	U	U	U	U

NOTES:
1. Indicates bits protected by LOCK and STOP. The default state of these bits is read from address 0x000008 of the shadow row on reset.

CMFIBAL — CMFI Base Address Low Register 0xYF F80A

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CMFIBAL[1]				RESERVED											
RESET:															
U	U	U	U	0	0	0	0	0	0	0	0	0	0	0	0

NOTES:
1. Indicates bits protected by $\overline{\text{LOCK}}$ and STOP. The default state of these bits is read from address 0x000008 of the shadow row on reset.

Table 10-8 CMFIBAR (CMFIBAH, CMFIBAL) Bit Settings

Bit(s)	Name	Description
31:24	—	Reserved
23:16	CMFIBAH	The 32-bit base address of the CMFI array memory address block is contained in the CMFIBAH and CMFIBAL array base address registers. The base address register (CMFIBAR) is formed by concatenating the contents of CMFIBAH and CMFIBAL. CMFIBAH contains the high order 16 bits of the address (A[31:16]) and CMFIBAL contains the next lower order bits. The value of CMFIBAH and CMFIBAL are forced to the user defined value programmed in CMFI shadow registers on master RESET. CMFIBAH and CMFIBAL can be written to relocate the CMFI array to an alternate block of memory only when the $\overline{\text{LOCK}}$ bit is 1 and the CMFI module is in STOP mode. NOTE: For a 256K module, CMFIBAH[17:16] and CMFIBAL[15:12] should be programmed to 0.
15:12	CMFIBAL	
11:0	—	Reserved

10.4.6 High Voltage Control Register

The high voltage control register is used to control the program and erase operations of the CMFI array.

CMFICTL1 — CMFI High Voltage Control Register 1 **0xYF F80C**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
HVS	0	SCLKR[1]			0	CLKPE[1]		0	CLKPM[1]						
RESET:															
0	0	U[2]			—	U[2]		—	U[2]						

NOTES:
1. These fields are NOT locked by SES if the value of the PAWS bits (in CMFITST) is not 0b000.
2. The default state of these bits will be read from the shadow row location 0xC on reset.

Table 10-9 CMFICTL1 Bit Settings

Bit(s)	Name	Description
15	HVS	High voltage status. The HVS bit is for status only and writes will have no effect. During a program or erase pulse this bit will be a 1 while the pulse is active or during recovery. The BIU will not acknowledge (IAACKB not asserted) an access to an array location if HVS = 1. While HVS = 1 SES cannot be changed and the CMFI cannot enter low power clock stop operation. The program or erase pulse becomes active by setting the EHV bit and is terminated by clearing EHV or by the pulse width timing control. The recovery time is the time that the CMFI EEPROM requires to remove the program or erase voltage from the array or shadow information before switching to another mode of operation. The recovery time is determined by the system clock range (SCLKR[0:2]) and the PE bit. The recovery time is 48 of the scaled clock periods unless SCLKR = 0 then the recovery time is 128 clocks. Once master reset is completed HVS shall indicate no program or erase pulse (HVS = 0). 0 = Program or erase pulse is not applied to the CMFI. 1 = Program or erase pulse is applied to the CMFI.
14	—	Reserved
13:11	SCLKR	System clock range. The SCLKR bits are write protected by the SES bit. Writes to CMFICTL will not change SCLKR if SES = 1. The first term of the timing control is the clock scaling, R. The value of R is determined by the system clock range (SCLKR). SCLKR defines the pulse timer's base clock using the system clock. The following table should be used to set SCLKR based upon the system clock frequency. The system clock period is multiplied by the clock scaling value to generate a 83. 3 ns to 125 ns scaled clock. This scaled clock is used to run the charge pump submodule and the next functional block of the timing control. See **Table 10-11** for SCLKR settings.
10	—	Reserved
9:8	CLKPE	Clock period exponent. The CLKPE[1:0] bits are write protected by the SES bit. Writes to CMFICTL will not change CLKPE[1:0] if SES = 1. The second term of the timing control is the exponential clock multiplier, N. The program pulse number (pulse), clock period exponent (CLKPE[1:0]) CSC, and PE define the exponent in the 2^N multiply of the clock period. The exponent, N, is defined by the equation: $N = 5 + CLKPE[1:0] + (PE \bullet 10)$ See **Table 10-12** for the range of exponents.

Table 10-9 CMFICTL1 Bit Settings (Continued)

Bit(s)	Name	Description
7	—	Reserved
6:0	CLKPM	Clock period multiple select. The CLKPM[6:0] bits are write protected by the SES bit. Writes to CMFICTL will not change CLKPM[6:0] if SES = 1. The third term of the timing control is the linear clock multiplier, M. The clock period multiplier, CLKPM[6:0], defines a linear multiplier for the program or erase pulse. The multiplier, M, is defined by the equation: M = 1 + CLKPM[6:0] This allows for the program/erase pulse to be from 1 to 128 times the pulse set by the system clock period, SCLKR[2:0] and CLKPE[1:0].

CMFICTL2 — CMFI High Voltage Control Register 2 **0xYF F80E**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
BLOCK								0	0	PEEM	B0EM	0	PE	SES	EHV
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 10-10 CMFICTL2 Bit Settings

Bit(s)	Name	Description
15:8	BLOCK	Block program and erase select. The BLOCK[7:0] bits are write protected by the SES bit. Writes to CMFICTL will not change BLOCK[7:0] if SES = 1. BLOCK[7:0] selects the CMFI EEPROM array blocks for program and erase operation. Up to eight blocks may be selected for program or erase operation at once. The CMFI EEPROM configuration along with BLOCK[7:0] determine the blocks that will be programmed simultaneously. The CMFI EEPROM array blocks that are selected to be programmed by the program operation are the blocks where BLOCK[M] = 1. The CMFI EEPROM configuration along with BLOCK[7:0] determine the blocks that will be erased simultaneously. The CMFI EEPROM array blocks that are selected to be erased by the erase operation are the blocks where BLOCK[M] = 1. **WARNING** The block bit must be set only for the blocks currently being programed. If the block bits are set for blocks that are not being programmed, the contents of the other blocks could be disturbed. 0 = Array block M is not selected for program or erase. 1 = Array block M is selected for program or erase.
7:6	—	Reserved
5	PEEM	Program erase enable monitor. The CMFI will sample the E_{PEE} signal (always enabled on the MC68F375) when EHV is asserted and hold the E_{PEE} state until EHV is negated. The E_{PEE} signal has a digital filter that requires two consecutive samples to be equal before the output of the filter will change. 0 = High voltage operations are not possible. 1 = High voltage operations are possible.
4	B0EM	Block zero enable monitor. The CMFI will sample B0EM when EHV is asserted and hold the B0EM state until EHV is negated. The optional E_{PEB0} pin has a digital filter similar to the E_{PEE} signal. If B0EM = 1 when EHV is asserted, high voltage operations to CMFI array block 0 such as program or erase are enabled. While, if B0EM = 0 when EHV is asserted high voltage operations to CMFI array block 0 are disabled. 0 = High voltage operations in Array Block 0 are not possible. 1 = High voltage operations in Array Block 0 are possible.
3	—	Reserved

Table 10-10 CMFICTL2 Bit Settings (Continued)

Bit(s)	Name	Description
2	PE	Program or erase select. The PE bit is write protected by the SES bit. Writes to CMFICTL will not change PE if SES = 1. PE configures the CMFI EEPROM for programming or erasing. When PE = 0, the array is configured for programming and if SES = 1 the SIE bit will be write locked. When PE = 1, the array is configured for erasing and SES will not write lock the SIE bit. 0 = Configure for program operation. 1 = Configure for erase operation.
1	SES	Start-end program or erase sequence. The SES bit is write protected by the HVS and EHV bits. Writes to CMFICTL will not change SES if HVS = 1 or EHV = 1. The SES bit is used to signal the start and end of a program or erase sequence. At the start of a program or erase sequence SES is set (written to a 1). At this point the CMFI EEPROM is ready to receive either the programming writes or the erase interlock write. The following bits shall be write locked: PROTECT, BLOCK[7:0], CSC, PE. SES also write locks SCLKR[2:0], CLKPE[1:0] and CLKPM[6:0]. If PE = 0 and SES = 1, SIE will be write locked. The erase interlock write is a write to any CMFI EEPROM array location after SES is set and PE = 1. If the PE bit is a 0 the CMFI BIU will accept programming writes to the CMFI array address for programming. The first programming write shall select the program page offset address (IADDR[14|13:6]) to be programmed along with the data for the programming buffers at the location written. All programming writes after the first shall update the program buffers using the lower address (IADDR[5:2]) and the block address (IADDR[17|16:15|14]) to select the program page buffers to receive the data. For further information see **10.5.2 Program Page Buffers**. After the data has been written to the program buffers the EHV bit is set (written to a 1) to start the programming pulse and lock out further programming writes. If the PE bit is a 1 the CMFI BIU will accept writes to the CMFI array addresses for an erase interlock. An erase interlock write is required before the EHV bit can be set. At the end of the program or erase operation the SES bit must be cleared (written to a 0) to return to normal operation and release the program buffers, PROTECT, SCLKR[2:0], CLKPE[1:0], CLKPM[6:0], BLOCK[7:0], CSC and the PE bit. 0 = Not configured for program or erase operation. 1 = Configure for program or erase operation.
0	EHV	Enable high voltage. EHV can be asserted only after the SES bit has been asserted and a valid programming write(s) or erase hardware interlock write has occurred. If an attempt is made to assert EHV when SES is negated, or if a valid programming write(s) or erase hardware interlock write has not occurred since SES was asserted, EHV will remain negated. The program or erase enable monitor (PEEM) and EHV are used to control the application of the program or erase voltage to the CMFI EEPROM module. High voltage operations to the CMFI EEPROM array, special MoneT shadow locations or FLASH NVM registers can occur only if EHV = 1 and PEEM = 1. Only after the correct hardware and software interlocks have been applied to the CMFI EEPROM can EHV be set. Once EHV is set SES cannot be changed and attempts to read the array will not be acknowledged. The default reset state of EHV disables program or erase pulses (EHV = 0). A master reset while EHV = 1 will terminate the high voltage operation (reset CMFICTL). A system reset or setting the STOP bit to 1 will clear EHV to a 0 terminating the high voltage pulse. The CMFI shall generate the required sequence to disable the high voltage without damage to the high voltage circuits. 0 = Program or erase pulse disabled. 1 = Program or erase pulse enabled.

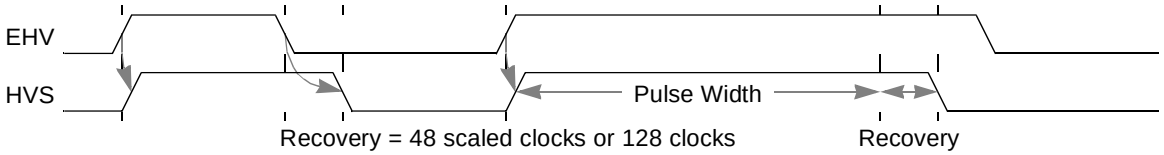


Figure 10-4 Pulse Status Timing

10.4.7 CMFIBS CMFI Bootstrap Words [3:0]

The bootstrap information for the CPU32 processor can be stored in the CMFI shadow row in the four words CMFIBS0–CMFIBS3. CMFIBS0 responds to address 0x000000, CMFIBS1 responds to 0x000002, CMFIBS2 to 0x000004 and CMFIBS3 to 0x000006 on the IMB3. See **10.6.6.3 Programming Shadow Information**.

CMFIBS0 — CMFI Bootstrap Word 0 **0xYF F810**

MSB 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	LSB 16
SP[31:16]															
RESET:															
U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]

NOTES:
1. The default state of these bits is read from the shadow row on reset.

CMFIBS1 — CMFI Bootstrap Word 1 **0xYF F812**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
SP[15:0]															
RESET:															
U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]

NOTES:
1. The default state of these bits is read from the shadow row on reset.

CMFIBS2 — CMFI Bootstrap Word 2 **0xYF F814**

MSB 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	LSB 16
PC[31:16]															
RESET:															
U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]

NOTES:
1. The default state of these bits is read from the shadow row on reset.

CMFIBS3 — CMFI Bootstrap Word 3 **0xYF F816**

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
PC[15:0]															
RESET:															
U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]	U[1]

NOTES:
1. The default state of these bits is read from the shadow row on reset.

10.4.8 Pulse Width Timing Control

To control the pulse widths for program and erase operations the CMFI EEPROM uses the system clock and the timing control in CMFICTL. The control of the program/erase pulse timing is divided into three functions. The total pulse time is defined by the following pulse width equation:

Pulse Width = System Clock Period • R • 2^N • M
Where: R = Clock Scaling, **Table 10-11**,
N = 5 + CLKPE[1:0] + (PE • 10)

Table 10-11 System Clock Range

SCLKR[2:0]	System Clock Frequency (MHz)		Clock Scaling (R)
	Minimum	Maximum	
000	NOTE: NOT FOR CUSTOMER USE Program and erase timing control not specified and pulse will not be terminated by the timer control. Recovery time will be specified to be 128 clocks.		1
001	8	12	1
010	12	18	3/2
011	18	24	2
100	24	33	3
101, 110 and 111	Reserved by Motorola for future use		

NOTE

The minimum specified system clock frequency for performing program and erase operations is 8.0 MHz. The CMFI EEPROM does not have any means to monitor the system clock frequency and will not prevent program or erase operation at frequencies below 8.0 MHz. Attempting to program or erase the CMFI EEPROM at system clock frequencies lower than 8.0 MHz will not damage the device if the maximum pulse times and total times are not exceeded. While some bits in the CMFI EEPROM array may change state if programmed or erased at system clock frequencies below 8.0 MHz, the full program or erase transition is not assured.

WARNING

Never stop or alter the IMB3 clock frequency during program or erase operation. Changing the clock frequency during program or erase will result in inaccurate pulse widths and variations in the charge transferred to the array bits.

The value of SCLKR is forced to the user defined value in the corresponding shadow information words on master reset. When SCLKR[2:0] = 000, the pulse width timer control will not terminate the program or erase pulse therefore the user must clear EHV via a software write.

All of the exponents are shown in **Table 10-12**.

Table 10-12 Clock Period Exponent and Pulse Width Range

PE	CLKPE[0:1]	Exponent (N)	Pulse Width Range for all System Clock Frequencies from 8.0 MHz to 33.0 MHz.					
			Minimum Pulse Width			Maximum Pulse Width		
			8 MHz[1] 2^N•1.25E-7	10 MHz[1] 2^N•1E-7	12 MHz[1] 2^N•0.833E-7	8 MHz[1] 2^N•1.25E-07	10 MHz[1] 2^N•1E-7	12 MHz[1] 2^N•0.833E-7
0	00	5	4 µs	3.2 µs	2.7 µs	512 µs	409.6 µs	341.3 µs
	01	6	8 µs	6.4 µs	5.3 µs	1.024 ms	819.2 µs	682.7 µs
	10	7	16 µs	12.8 µs	10.7 µs	2.048 ms	1.6384 ms	1.365 ms
	11	8	32 µs	25.6 µs	21.3 µs	4.096 ms	3.2768 ms	2.731 ms
1	00	15	4.096 ms	3.28 ms	2.73 ms	524.29 ms	419.43 ms	349.5 ms
	01	16	8.192 ms	6.55 ms	5.46 ms	1.05 s	838.86 ms	699.1 ms
	10	17	16.384 ms	13.11 ms	10.92 ms	2.10 s	1.68 s	1.398 s
	11	18	32.768 ms	26.21 ms	21.85 ms	4.19 s	3.35 s	2.796 s

NOTES:
1. CMF clock frequency after SCKLR scaling. Example: A 32 MHz system clock scaled by 3 (SCLKR[0:2] = 0b100) results in an equivalent CMF clock of 10 MHz.

The value of CLKPE[1:0] is forced to the user defined value in the corresponding shadow information words on master reset, as is the value of CLKPM[6:0].

10.4.9 A Technique to Determine SCLKR, CLKPE, and CLKPM

The following example determines the values of the SCLKR, CLKPE, and CLKPM fields for a 51.4 µS pulse program pulse, PE=0, in a system with a 33.0 MHz system clock.

In this example system clock frequency = 33.0 MHz; the system clock period is therefore 30.3 nS.

1. Determine SCLKR:
   From **Table 10-11** a 33.0 MHz system clock uses SCLKR[0:2]=100, R=3.
2. Determine CLKPE:
   From **Table 10-12** a 51.4 µS program pulse, PE=0, can be generated by expo-

nents in the range of N=6. While any of these values can be selected CLKPE[0:1]=00, N=6, will be used for the example.

3. Determine CLKPM:
   Using the selected values of N and R in the pulse width equation and solving for M yields M=8.8. Rounding M to 9 then CLKPM[0:6]=0x8 (0b0001000).
4. Check the results:
   Pulse Width=System Clock Period • R • 2^N • M
   using SCLKR[0:2]=100, CLKPE[0:1]=00, CLKPM[0:6]=0001000 and PE=0 at 33.0 MHz system clock. Pulse Width=30.3 µS • 3 • 2^6 • 9=52.4 µS program pulse.

10.5 CMFI EEPROM Array Addressing

The base address of the memory block in which the CMFI EEPROM array resides is specified in the array base address register (CMFIBAR). The default reset base address is specified in the shadow registers by the user. The only restrictions on the base address are that it must be on a 2^N byte boundary (N = 16, 17 or 18 depending on array size). If the base address is set such that the CMFI EEPROM array overlaps the control register block, accesses to the 32-bytes of the array that overlap the control registers will be ignored, allowing the control block to remain accessible. This is only true with respect to the same CMFI EEPROM module. If the control register blocks of other modules are overlapped by the CMFI EEPROM array, accesses to the overlapped addresses will be indeterminate.

The CMFI EEPROM array is divided into a shadow row and eight 32-Kbyte blocks as shown in **10.6.6.3 Programming Shadow Information**. The shadow register information is stored in shadow block. The array supports multiple-page programming.

Information in the array is accessed in 32-byte burst buffers. Two read burst buffers are aligned to the low order addresses (IADDR[4:0]). The first burst buffer is associated with the lower array blocks. The second burst buffer is associated with the higher array blocks. Read access time from the array will take 2, 3, 4 or 5 clocks as defined by WAIT[1:0] for the first data access. If a burst access the following access are 1 clock accesses from within the 32-byte burst buffer. To prevent the BIU from unnecessarily refreshing the burst buffer from the array, the CMFI EEPROM shall monitor the IMB3 address to determine if the required information is within one of the two read burst buffers and the access is valid for the module.

Write accesses to the CMFI array will not assert the address acknowledge unless they are programming or erase interlock writes.

10.5.1 Read Burst Buffers

The two 32-byte read burst buffers are fully independent and are located in two separate read sections of the array as indicated in **Figure 10-1**. Each burst buffer status and address are monitored in the BIU. The status of the read burst buffers are usually valid, but are made invalid by the following operations:

- Setting/Clearing VT

- Setting/Clearing PBR
- Reset,
- Programming write
- Erase interlock write
- Setting EHV
- Clearing SES
- Setting/Clearing SIE

Each access to the CMFI EEPROM array shall determine if the requested location is within the current burst buffers. If the requested location is not within the read burst buffers then the correct read burst buffer shall be made invalid and a new 32 byte block of information will be fetched from the array. The burst buffer address is updated and status is made valid. If the requested location is within one of the current burst buffers or has been fetched from the array the selected bytes are transferred to the IMB3 completing the access. While bursting data from the read burst buffer the address is incremented by width of the internal data bus. Upon reaching the end of the read burst buffer the CMFI EEPROM shall terminate the burst access.

10.5.2 Program Page Buffers

The CMFI EEPROM can program up to eight 64-byte pages at one time. Each program page buffer is associated with one array block as indicated in the diagrams in **Figure 10-1**. All program page buffers share the same block offset address, IADDR[14|13:6], stored in the BIU. The block offset address is extracted from the address of the first programming write. To select the CMFI EEPROM array block that will be programmed, the program page buffers use the CMFI EEPROM array configuration and BLOCK[7:0]. The data programmed in each array block is determined by the programming writes to the program buffer for each block. All program buffer data is unique whereas the program page offset address is shared by all blocks.

The array block that will be programmed is selected by the BLOCK bit that is a 1. If BLOCK[M] = 1 then program buffer[M] is active and array block[M] will program. If BLOCK[M] = 0 then program buffer[M] is inactive and array block[M] will not program.

Bits in the program page buffers shall select the non-program state if SES = 0. During a program margin read, the program buffers will update bits to the non-program state for bits that correspond to array bits that the program margin read has determined are programmed.

10.6 Operation

The following sections describe the functioning of the CMFI EEPROM during various operational modes. The primary function of the CMFI EEPROM Module is to serve as electrically erasable and programmable non-volatile memory accessed by any bus master capable of using the IMB3.

10.6.1 Power On Reset

The device signals a power on reset (IPORB = 0) to the CMFI EEPROM when a full reset is required. A power on reset is the priority operation for the CMFI EEPROM and will terminate all other operations, including resetting FRI = 0.

10.6.2 Master Reset

The device signals a master reset (IMSTRSTB = 0) to the CMFI EEPROM when a full reset is required. A master reset is the 3rd highest priority operation for the CMFI EEPROM and will terminate all other operations, unless FRI = 1. If FRI = 1 master reset is blocked to the CMFI EEPROM.

The CMFI EEPROM module uses master reset to initialize all register bits to their default reset value. If the CMFI EEPROM is in program or erase operation (EHV = 1) and a master reset is generated, the module will perform the needed interlocks to disable the high voltage without damage to the high voltage circuits. Master reset will terminate any other mode of operation and force the CMFI EEPROM BIU to a state ready to receive IMB3 accesses within 4 clocks of the end of master reset.

During master reset the CMFI EEPROM must perform several tasks to assure correct and reliable operation. In order of execution these tasks are:

1. Recover from high voltage operation.
2. Copy the shadow information into the registers.
3. Reset the BIU state machine to receive the first cycle start within 4 clocks of the final reset clock.

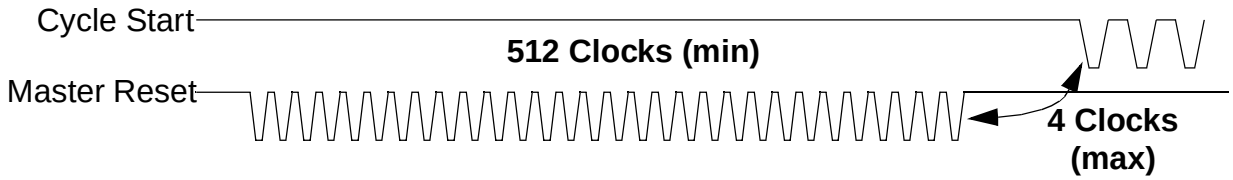


Figure 10-5 Master Reset Configuration Timing

10.6.3 System Reset

The device signals a system reset (ISYSRSTB = 0) to the CMFI EEPROM when required. A system reset is the 4th highest priority operation and forces the BIU into a state ready to receive IMB3 accesses and clears the EHV bit, unless FRI = 1. All other bits shall remain unaltered by a system reset.

10.6.4 Register Read and Write Operation

The CMFI EEPROM control registers are accessible for read or write operation at all times while the device is powered up except during master reset, or system reset.

The access time of a CMFI register is at least 2 clocks depending on the state of WAIT[1:0] for both read and write accesses. Read accesses to reserved registers shall

cause the BIU to generate either a bus error or return all zeros. Write accesses to reserved registers shall have no effect. See section **10.4.1 CMFI EEPROM Module Control Block Addressing** for more information on register accesses.

10.6.5 Array Read Operation

The CMFI EEPROM array is available for read operation under most conditions while the device is powered up. Reads of the array are not allowed during master reset, system reset, and ACCESS = 0 while high voltage is applied to the array or while the CMFI EEPROM is stopped, see section **10.6.8 Stop Operation** for more information on stopping the CMFI EEPROM. At certain points, as defined in the program or erase sequence, reading the array shall result in a margin read. These margin reads return the status of the program or erase operation and not the data in the array.

After reset, programming writes, erase interlock write, setting EHV, clearing SES or setting/clearing SIE (this affects the lower array blocks burst buffer only) the burst buffers will not contain valid information and the correct information will be fetched from the array.

Section **10.5.1 Read Burst Buffers** defines how the two burst buffers in the CMFI EEPROM are associated to array blocks. During burst read operation, the initial read will require at least 2 clocks depending on the state of WAIT[1:0]. Subsequent burst reads will take 1 clock until the end of the burst buffer is reached or the burst is terminated by the IMB3.

10.6.6 Programming

To modify the charge stored in the isolated element of the CMFI bit from a logic 1 state to a logic 0 state, a programming operation is required. This programming operation shall apply the required voltages to change the charge state of the selected bits without changing the logic state of any other bits in the CMFI array. The program operation cannot change the logic 0 state to a logic 1 state; this transition must be done by the erase operation. Programming uses a set of up to 8 program buffers of 64 bytes each to store the required data, an address offset buffer to store the starting address of the block(s) to be programmed and a block select buffer that stores information on which block(s) are to be programmed. Any number of the array blocks may be programmed at one time.

Do not program any page more than once after a successful erase operation. While this will not physically damage the array it shall cause an increased partial disturb time for the unselected bits on the row and columns that are not programmed.

A full erase of all blocks being programmed must be done before the CMFI EEPROM can be used reliably if over programming occurs.

WARNING

If the PROTECT bit is set then the CMFI EEPROM array will not be programmed. Also, if PEEM = 0, no programming voltages will be applied to the array and if B0EM = 0, no programming voltages will be applied to block 0.

10.6.6.1 Program Sequence

The CMFI EEPROM module requires a sequence of writes to the high voltage control registers (CMFICTL1 and CMFICTL2) and to the program page buffer(s) in order to enable the high voltage to the array or shadow information for program operation. The required program sequence follows.

1. Write PROTECT = 0 to disable protection on the CMFI EEPROM array.
2. Write PAWS to 0b100, write NVR = 1, write GDB = 1.
3. Set the initial pulse width bit settings per **Table 10-6**. Using section **10.4.9 A Technique to Determine SCLKR, CLKPE, and CLKPM**, write the pulse width timing control fields for a program pulse to the CMFICTL1 register. Write BLOCK[7:0] to select the array blocks to be programmed and PE = 0 in the CMFICTL2 register.

   WARNING

   Do not select the block bits of blocks not currently being programmed.

4. Write SES = 1 in the CMFICTL2 register. This step can be done with the same write in step 2 but is split out as a separate step in the sequence for looping.
5. Programming writes. Write to the 64-byte array locations to be programmed. This shall update the programming page buffer(s) with the information to be programmed. Only the last write to each word within the program page buffer shall be saved for programming. All accesses of the array after the first write shall be to the same block offset address (IADDR[14|13:6]) regardless of the address provided. Thus the locations accessed after the first programming write are limited to the page locations to be programmed. Off page read accesses of the CMFI array after the first programming write are program margin reads see section **10.6.6.2 Program Margin Reads**.

   All program page buffers share the same block offset address (IADDR[14|13:6]) stored in the BIU. The block offset address is extracted from the address of the first programming write. To select the CMFI EEPROM array block(s) that will be programmed, the program page buffers use the CMFI EEPROM array configuration and BLOCK[7:0]. Subsequent writes fill in the program page buffers using the block address to select the program page buffer and the page word address (IADDR[5:2]) to select the word in the page buffer. The array configuration and BLOCK[7:0] determine which blocks are programmed simultaneously.
6. Write EHV = 1 in the CMFICTL2 register. If a program buffer has not received

a programming write no programming voltages will be applied to the corresponding word in the array. Also, at this point writes to the program page buffers are disabled until SES has been cleared and set.

7. Read the CMFICTL1 register until HVS = 0.
8. Write EHV = 0 in CMFICTL2.
9. Program Verify. Read the words of the pages that are being programmed. These are program margin reads, see section **10.6.6.2 Program Margin Reads**. If any bit is a 1 after reading all of the locations that are being programmed go to step 5. If all the locations verify as programmed go to step 9.

WARNING

After a program pulse, read at least one location with IADDR[5] = 0 and one location with IADDR[5] = 1 on each programmed page. Failure to do so may result in the loss of information in the CMFI EEPROM array. While this will not physically damage the array it will require that a full erase of all blocks being programmed be done before the CMFI EEPROM can be used reliably.

To reduce the time for verification, read only two locations in each array block that is being programmed after reading a non-programmed bit. The first location must be a location with IADDR[5] = 0; while, the second must use IADDR[5] = 1. Also, after a location has been fully verified (all bits are programmed) it is not necessary to verify the location as no further programming voltages will be applied to the drain of the corresponding bits.

10. If the margin read is successful, then write SES = 0 in the CMFCTL register, otherwise do the following:

    a. Write new pulse width parameters (if required per **Table 10-6**) - SCLKR, CLKPE, CLKPM.

    b. Write new values for PAWS, NVR, and GDB (if required per **Table 10-6**).

    c. Go back to step 6 to apply additional programming pulses.

11. If more information needs to be programmed, go back to step 2.

CAUTION

Failure to read each page that is being programmed after each program pulse may result in the loss of information in the CMF EEPROM array. While this will not physically damage the array a full erase of all blocks being programmed must be performed before the CMF EEPROM can be used reliably.

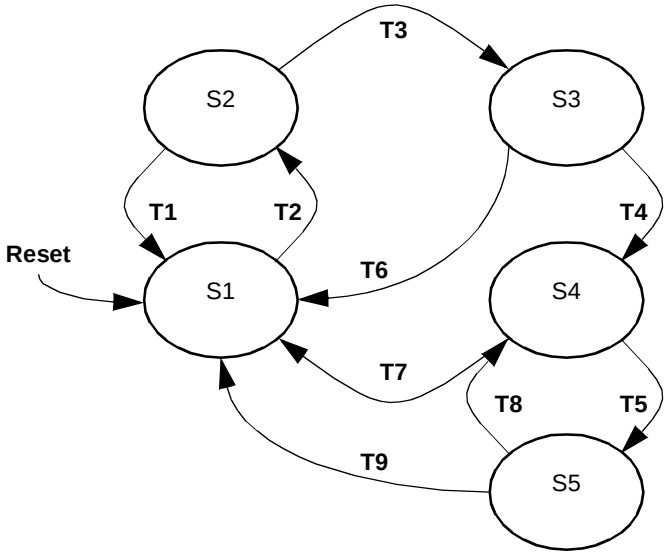


Figure 10-6 Program State Diagram

Table 10-13 Program Interlock State Descriptions

State	Mode	Next State	Transition Requirement	
S1	Normal Operation: Normal array reads and register accesses. The Block protect information and pulse width timing control can be modified.	S2	T2	Write PE = 0, SES = 1
S2	First Program Hardware Interlock Write: Normal read operation still occurs. The array will accept programming writes Accesses to the registers are normal register accesses. A write to CMFICTL2 cannot change EHV at this time. If the write is to a register no data will be stored in the program page buffers and the CMFI shall remain in state S2.	S1	T1	Write SES = 0 or master reset
		S3	T3	Hardware Interlock Write to any CMFI array location This programming write will latch the selected word of data into the programming page buffer and the address shall be latched to select the location that will be programmed. Once a bit has been written then it shall remain in the program buffer until another write to the word or a write of SES = 0 or a program margin read determines that the state of the bit needs no further modification by the program operation If the write is to a register no data will be stored in the program page buffers and the CMFI shall remain in state S2
S3	Expanded Program Hardware Interlock Operation: Program margin reads will occur. Programming writes are accepted so that all program pages may be programmed. These writes may be to any CMFI array location. The program page buffers will be updated using only the data, the lower address (IADDR[5:2]) and the block address. Accesses to the registers are normal register accesses. A write to CMFICTL2 can change EHV. If the write is to a register no data will be stored in the program page buffer.	S1	T6	Write SES = 0 or master reset
		S4	T4	Write EHV = 1.

Table 10-13 Program Interlock State Descriptions (Continued)

State	Mode	Next State	Transition Requirement	
S4	Program Operation: High voltage is applied to the array or shadow information to program the CMFI bit cells. The pulse width timer is active if SCLKR[2:0] ≠ 0 and HVS can be polled to time the program pulse. No further programming writes will be accepted. During programming the CMFI will not generate an address acknowledge for any array access. Accesses to the registers are normal register accesses. A write to CMFICTL2 can change EHV only.	S1	T7	Master reset
		S5	T5	Write EHV = 0, write STOP = 1 or system reset
S5	Program Margin Read Operation: These reads shall determine if the state of the bits on the selected page needs further modification by the program operation. Once a bit is fully programmed, the data stored in the program page shall be updated so no further programming occurs for that bit and the value read is a 0.	S4	T8	Write EHV = 1.
		S1	T9	Write SES = 0 or master reset

10.6.6.2 Program Margin Reads

The CMFI EEPROM provides a program margin read with electrical margin for the program state. Program margin reads provide sufficient margin to assure specified data retention. The program margin read is enabled when SES = 1 and a programming write has occurred. To increase the access time of the program margin read, the burst buffer access time shall be 16 clocks instead of the usual number of clocks as determined by WAIT[1:0] for the first read access. The program margin read and subsequent verify reads will return a 1 for any bit that has not completely programmed. Bits that the programming write left in the non-programmed state will read as a 0. Bits that have completed programming will read as a 0 and update the data in the programming page buffer so that no further programming of those bits will occur. The program margin read occurs whenever the burst buffer data is invalid. See section **10.6.5 Array Read Operation** for information on when the burst buffer is invalid. A program margin read must be done for all pages that are being programmed after each program pulse. This requires two program margin reads for each program buffer. The first required program margin read should be to an address in either the lower or upper 32 bytes of the program buffer while the second should be to an address in the other 32 bytes.

Table 10-14 Results of Programming Margin Read

Current Data in the Program Page Buffer[1]	Current State of Bit	Data Read During Margin Read[2]	New Data for the Program Page Buffer[1]
0	Programmed (0)	0	1
0	Erased (1)	1	0
1	Programmed (0)	0	1
1	Erased (1)	0	1

NOTES:
1. 0 = bit needs to further programming
   1 = bit does not need further programming
2. A “0” read during the margin read means that the bit does NOT need further programming. A “1” means the bit needs to be programmed further.

Failure to read each page that is being programmed after each program pulse may result in the loss of information in the CMFI EEPROM array.

While this will not physically damage the array a full erase of all blocks being programmed must be done before the CMFI EEPROM can be used reliably.

For more information see section **10.6.6.4 Over Programming**.

10.6.6.3 Programming Shadow Information

Programming the shadow information uses the same procedure as programming the array except that only the program page buffer associated with the lowest array block will be used to program the shadow information. Before starting the program sequence SIE must be a 1.

The first 32 bytes (IADDR[7:0] = 0x00 to 0x1F) of the 256 bytes of shadow locations are withheld by Motorola for the shadow information words and future applications. The remaining 224 bytes are available for general use. Programming of these 32 bytes affects the reset configuration of the CMFI EEPROM. The register shadow information word and location within the shadow row is presented in the following table. Registers not listed in this table do not require shadow information for reset configuration but their shadow locations are withheld from general use by Motorola for future applications.

Table 10-15 Register Shadow Information

Register Name	Register Address	Shadow Row Address (addr[7:0])
CMFIMCR	0x00 0000	0x00
CMFIBAR	0x00 0008	0x08
CMFICTL1	0x00 000C	0x0C
CMFIBS0	0x00 0010	0x10
CMFIBS1	0x00 0012	0x12
CMFIBS2	0x00 0014	0x14
CMFIBS3	0x00 0016	0x16

10.6.6.4 Over Programming

Programming a CMFI bit without a program margin read after each program pulse or exceeding the specified program times or voltages will result in an over programmed state. Once a CMFI bit has been over programmed, data in the array block that is located upon the same column shall be lost as the over programmed bit causes the entire column to appear programmed. To restore an array block with an over programmed bit the block must be erased and reprogrammed.

10.6.7 Erase

To modify the charge stored in the isolated element of the CMFI bit from a logic 0 state to a logic 1 state, an erase operation is required. The erase operation cannot change the logic 1 state to a logic 0 state; this transition must be done by the program operation. In the CMFI EEPROM, erase is a bulk operation that shall affect the stored charge of all the isolated elements in an array block. To make the CMFI module block-erasable, the array is divided into blocks that are physically isolated from each other. Each of the array blocks may be erased in isolation or in any combination. The CMFI array block size is fixed for all blocks in the module at 32 Kbytes and the module is comprised of 4, 6 or 8 blocks. If the CMFI EEPROM array is protected (PROTECT = 1), the array will not be erased. Also, if PEEM = 0 no erase voltages will be applied to the array and if B0EM = 0, no programming voltages will be applied to block 0.

The array blocks selected for erase operation are determined by BLOCK[7:0].

10.6.7.1 Erase Sequence

The CMFI EEPROM module requires a sequence of writes to the high voltage control registers (CMFICTL1 and CMFICTL2) and an erase interlock write in order to enable the high voltage to the array and shadow information for erase operation. The erase sequence follows.

1. Write PROTECT = 0 to disable protection on the array.
2. Set the initial pulse width bit settings per **Table 10-7**.
3. Using section **10.4.9 A Technique to Determine SCLKR, CLKPE, and CLKPM**, write the pulse width timing control fields for an erase pulse in the CMFICTL1 register. Write the BLOCK[7:0] to select the blocks to be erased, PE = 1 and SES = 1 in the CMFICTL2 register.
4. Execute an erase interlock write to any CMFI array location.
5. Write EHV = 1 in the CMFICTL2 register.
6. Read the CMFICTL1 register until HVS = 0.
7. Write EHV = 0 in the CMFICTL2 register.
8. To verify the erase operation, read all locations that are being erased, including the shadow information if the block containing it is erased. Off-page reads are erase margin reads that update the read page buffer. (See section **10.6.7.2 Erase Margin Reads**.) If all the locations read as erased, go to step 9.

NOTE

Do not perform erase margin reads until reaching the condition PAWS=0b111, NVR=0 and GDB=1.

9. To reduce the time used for erase margin reads, upon the first read of a zero, do the following:

   a. Write new pulse width parameters, SCLKR, CLKPE, and CLKPM (if required per **Table 10-7**).

   b. Write newPAWS value (if required per **Table 10-7**).

   c. Write new values for NVR and GDB (if required per **Table 10-7**).

   d. Go back to step 5 to apply additional erase pulses.

NOTE

After a location has been verified (all bits erased), it is not necessary to verify the location after subsequent erase pulses.

10. Write SES = 0 in the CMFICTL2 register. The CMFI requires 16 clocks after writing SES = 0 prior to a normal CMFI EEPROM array read. To meet this requirement the CMFI shall allow all access to start any time after writing SES = 0 but the access shall not be completed until after the 16 clock period. This time shall be extended by the number of clocks defined by WAIT[1:0].

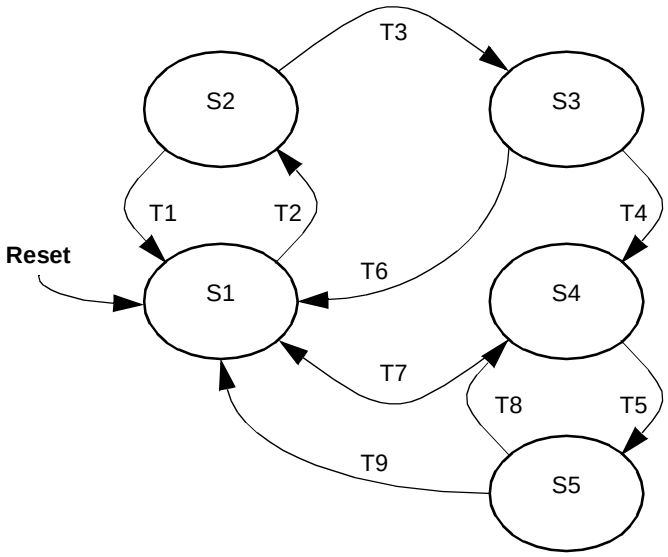


Figure 10-7 Erase State Diagram

Table 10-16 Erase Interlock State Descriptions

State	Mode	Next State	Transition Requirement	
S1	Normal Operation: Normal array reads and register accesses The Block protect information and pulse width timing control can be modified.	S2	T2	Write PE = 1, SES = 1
S2	Erase Hardware Interlock Write: Normal read operation still occurs The CMFI will accept the erase hardware interlock write. This write may be to any CMFI array location Accesses to the registers are normal register accesses. A write to CMFICTL2 cannot set EHV at this time A write to the register is not an erase hardware interlock write and the CMFI shall remain in state S2.	S1	T1	Write SES = 0 or master reset
		S3	T3	Hardware Interlock Write to any CMFI array location is the erase interlock write. If the write is to a register the erase hardware interlock write has not been done and the CMFI shall remain in state S2.
S3	High voltage write enable Erase margin reads will occur Accesses to the registers are normal register accesses. A write to CMFICTL2 can change EHV.	S1	T6	Write SES = 0 or master reset
		S4	T4	Write EHV = 1
S4	Erase Operation: High voltage is applied to the array blocks to erase the CMFI bit cells. The pulse width timer is active if SCLKR[2:0] ≠ 0 and HVS can be polled to time the erase pulse During erase the array will not respond to any address. Accesses to the registers are normal register accesses. A write to CMFICTL2 can change EHV only.	S1	T7	Master reset
		S5	T5	Write EHV = 0, write STOP = 1 or system reset
S5	Erase Margin Read Operation: These reads shall determine if the state of the bits on the selected blocks needs further modification by the erase operation. Once a bit is fully erased it shall read as a 1. All words within the blocks being erased must be read to determine if erase is completed.	S4	T8	Write EHV = 1
		S1	T9	Write SES = 0 or master reset

10.6.7.2 Erase Margin Reads

The CMFI EEPROM provides an erase margin read with electrical margin for the erase state. Erase margin reads provide sufficient margin to assure specified data retention. The erase margin read is enabled when SES = 1 and the erase write has occurred. The erase margin read and subsequent on page erase verify reads will return a 0 for any bit that has not completely erased. Bits that have completed erasing will read as a 1. To increase the access time of the erase margin read the access time shall be 16 clocks instead of the usual number of clocks as determined by WAIT[1:0] for the first read access. The erase margin read occurs while doing the transfer from the array to the burst buffer. All locations within the block(s) that are being erased must read as a 1 to determine that no more erase pulses are required.

10.6.7.3 Erasing Shadow Information Words

The shadow information words are erased with either CMFI array block 0 or block 2 depending upon the array configuration. To verify that the shadow information words are erased the SIE bit in CMFIMCR should be set to 1 during the erase margin read while the shadow information is read. For the erase operation to be completed block 0 or 2 must also be fully verified.

Setting SIE = 1 will disable normal array access and should be cleared after verifying the shadow information.

10.6.8 Stop Operation

The CMFI EEPROM goes into a low power operation, or stop operation, while STOP = 1. Setting STOP to 1 will clear EHV to a 0. When the STOP bit is set only the control registers can be accessed on the CMFI EEPROM. The CMFI EEPROM array may not be programmed, erased or read while STOP = 1. With STOP = 1 and $\overline{\text{LOCK}}$ = 1 the array may be mapped to another location in the memory map, and the array Address Space may be changed. During stop operation the CMFI may enter low power stop clock operation.

10.6.8.1 Low Power Stop Clock Operation

The low power stop clock operation is the lowest power configuration of the CMFI EEPROM, disabling the internal clock. This operation is entered when STOP = 1 and the correct system clock disable (ICLKDIS[N]) is asserted and HVS = 0. The BIU will disable the system clock to the state machine at the completion of required functions to protect the CMFI EEPROM after the STOP bit is set and ICLKDIS[N] is asserted. Once the CMFI EEPROM is in low power stop clock operation, all accesses by the IMB3 will be ignored, and AACKB will not be asserted until ICLKDIS[N] is cleared by the IM. When ICLKDIS[N] is cleared, the internal clocks will be enabled and the CMFI EEPROM register control block will respond to IMB3 accesses.

10.6.8.2 STOP Recovery

The CMFI requires 16 clocks after writing STOP = 0 prior to a normal CMFI EEPROM array read. The access time of the first CMFI array read shall be 16 clocks instead of the usual number of clocks as determined by WAIT[1:0]. To meet this requirement the

CMFI shall allow all access to start any time after writing STOP = 0 but the access shall not be completed until after the 16 clock period.

10.6.9 Background Debug Mode or Freeze Operation

While in background debug mode (IFREEZEB = 0) the CMFI should respond normally to accesses except that $\overline{\text{LOCK}}$ is writable.