GLOSSARY OF TERMS AND ABBREVIATIONS

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this book. Some of the terms and definitions included in the glossary are reprinted from *IEEE Std 754-1985, IEEE Standard for Binary Floating-Point Arithmetic*, copyright ©1985 by the Institute of Electrical and Electronics Engineers, Inc. with the permission of the IEEE.

A

Atomic. A bus access that attempts to be part of a read-write operation to the same address uninterrupted by any other access to that address (the term refers to the fact that the transactions are indivisible). The processor initiates the read and write separately, but signals the L-bus or external bus interface that it is attempting an atomic operation. If the operation fails, status is kept so that the processor can try again. The processor implements atomic accesses through the **lwarx**/**stwcx.** instruction pair.

B

Beat. A single state on the external bus interface that may extend across multiple bus cycles. An RCPU transaction can be composed of multiple address or data beats.

Biased Exponent. The sum of the exponent and a constant (bias) chosen to make the biased exponent's range non-negative.

Big-Endian. A byte-ordering method in memory where the address n of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.

Blockage. The number of clock cycles between the time an instruction begins execution and the time its execution unit is available for a subsequent instruction.

Boundedly Undefined. The results of attempting to execute a given instruction are said to be boundedly undefined if they could have been achieved by executing an arbitrary sequence of defined instructions, in valid form, starting in the state the machine was in before attempting to execute the given instruction. Boundedly undefined results for a given instruction may vary between implementations, and between execution attempts in the same implementation.

Branch Folding. A technique of removing the branch instruction from the instruction sequence.

Breakpoint. An event that, when detected, forces the machine to branch to a breakpoint exception routine.

Burst. A multiple beat data transfer.

Bus Master. The owner of the address or data bus; the device that initiates or requests the transaction.

C

Cache Coherency. Caches are coherent if a processor performing a read from its cache is supplied with data corresponding to the most recent value written to memory or to another processor's cache.

Context Synchronization. All instructions in execution complete past the point where they can produce an exception; all instructions in execution complete in the context in which they began execution; all subsequent instructions are fetched and executed in the new context.

D

Denormalized Number. A non-zero floating-point number whose exponent has a reserved value, usually the format's minimum, and whose explicit or implicit leading significand bit is zero.

E

Exception. An unusual or error condition encountered by the processor that results in special processing.

Exception Handler. A software routine that executes when an exception occurs. Normally, the exception handler corrects the condition that caused the exception, or performs some other meaningful task (such as aborting the program that caused the exception). The addresses of the exception handlers are defined by a two-word exception vector that is branched to automatically when an exception occurs.

Execution Serialization. During execution serialization, instruction issue is halted until all instructions currently in the pipeline (i.e., all instructions that have been issued but have not completed) complete execution.

Exponent. The component of a binary floating-point number that normally signifies the integer power to which two is raised in determining the value of the represented number. Occasionally the exponent is called the signed or unbiased exponent.

F

Fetch Serialization. During fetch serialization, instruction fetch is halted until all instructions currently in the processor (i.e., in the pipeline or in the pre-fetch queue) have completed. Following fetch serialization, the machine is said to be completely synchronized.

Floating-Point Unit. The functional unit in the RCPU responsible for executing all floating-point arithmetic instructions.

Flow-Control Instruction. One of the following: **b**, **br**, **bcr**, **bcc**, **rfi**, **sc**, or (in some cases) **isync**.

Fraction. The field of the significand that lies to the right of its implied binary point.

G

General-Purpose Registers. Any of the 32 registers in the MPC601 register file. These registers provide the source operands and destination results for all MPC601 data manipulation instructions. Load instructions move data from memory to registers, and store instructions move data from registers to memory.

I

IEEE 754. A standard written by the Institute of Electrical and Electronics Engineers that defines operations of binary floating-point arithmetic and representations of binary floating-point numbers.

I-Bus. Internal instruction bus connecting the processor to instruction memory.

Implementation Specific. An RCPU register, exception, or other feature is said to be implementation specific if it is not part of the PowerPC architecture.

Instruction Completion. Completion of the instruction issue, execution, and writeback stages. An instruction is ready to be retired if it completes without generating an exception and all instructions ahead of it in the history buffer have completed without generating an exception.

Instruction Execution Time. The number of clock cycles between the time an instruction is taken and the time it is completed.

Instruction Fetch. The process of reading the instruction data received from the instruction memory.

Instruction Issue. The process of driving valid instruction bits inside the processor. The instruction is decoded by each execution unit, and the appropriate execution unit prepares to execute the instruction during the next clock cycle.

Instruction Taken. An instruction is taken after it has been issued and recognized by the appropriate execution unit. All resources to perform the instruction are ready, and the processor begins to execute it.

Instruction Unit. The functional unit in the RCPU that fetches all instructions from memory and performs the initial stages of instruction decoding. The instruction unit also contains the branch processing unit and performs all instruction address calculations (including branch address calculations).

Integer Unit. The functional unit in the RCPU responsible for executing all integer arithmetic instructions.

Instruction Cache. High-speed memory containing recently accessed instructions (subset of main memory).

Interrupt. An external signal that causes the processor to suspend current execution and take a predefined exception.

L

L-Bus. Internal load/store bus connecting the processor to internal modules and data memory and to the external bus interface.

Latency. The number of clock cycles necessary to execute an instruction and make ready the results of that instruction.

Little-Endian. A byte-ordering method in memory where the address n of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.

N

NaN. Not a number; a symbolic entity encoded in floating-point format. There are two types of NaNs — signaling NaNs and quiet NaNs.

No-Op. No-operation. A single-cycle operation that does not affect registers or generate bus activity.

O

Overflow. An error condition that occurs during arithmetic operations when the result cannot be stored accurately in the destination register(s). For example, if two 32-bit numbers are added, the sum may require 33 bits due to carry. Since the 32-bit registers of the MPC601 cannot represent this sum, an overflow condition occurs.

P

Park. The act of allowing a bus master to maintain mastership of the bus without having to arbitrate.

Pipelining. A technique that breaks instruction execution into distinct steps so that multiple steps can be performed at the same time.

Precise Exceptions. The pipeline can be stopped so the instructions that preceded the faulting instruction can complete, and subsequent instructions can be executed from their beginning.

Q

Quiet NaNs. Propagate through almost every arithmetic operation without signaling exceptions. These are used to represent the results of certain invalid operations, such as invalid arithmetic operations on infinities or on NaNs, when invalid.

S

Sequential Instruction. Any instruction other than a flow-control instruction or **isync**.

Show Cycle. An internal access (e.g., to an internal memory) reflected on the external bus using a special cycle (marked with a dedicated transfer code). For an internal memory “hit,” an address-only bus cycle is generated; for an internal memory “miss,” a complete bus cycle is generated.

Signaling NaNs. Signal the invalid operation exception when they are specified as arithmetic operands.

Significand.The component of a binary floating-point number that consists of an explicit or implicit leading bit to the left of its implied binary point and a fraction field to the right.

Slave. The device addressed by a master device. The slave is identified in the address tenure and is responsible for supplying or latching the requested data for the master during the data tenure.

Snooping. Monitoring addresses driven by a bus master to detect the need for coherency actions.

Static Branch Prediction. Mechanism by which software (for example, compilers) can give a hint to the machine hardware about the direction the branch is likely to take.

Supervisor Mode. The privileged operation state of the RCPU. In supervisor mode, software can access all control registers and can access the supervisor memory space, among other privileged operations.

T

Tiny Result. A tiny result is detected before rounding when a non-zero result value, computed as though the exponent range were unbounded, would be smaller in magnitude than the smallest normalized number.

U

Underflow. An error condition that occurs during arithmetic operations when the result cannot be represented accurately in the destination register. For example, underflow can happen if two floating-point fractions are multiplied and the result is a single-precision number. The result may require a larger exponent and/or mantissa than the single-precision format makes available. In other words, the result is too small to be represented accurately.

User Mode. The unprivileged operating state of the RCPU. In user mode, software can only access certain control registers and can only access user memory space. No privileged operations can be performed.

W

Watchpoint. An event that, when detected, is reported but does not change the timing of the machine.