SECTION 1
OVERVIEW

1.1 Introduction

The MC68377 is a member of the MC68300 family of modular microcontrollers. This family includes a series of modules from which numerous microcontrollers (MCUs) are being assembled. These modules are connected on-chip via the inter-module bus (IMB).

A short description of each module used in the MC68377 appears in the following sections.

1.2 Module List

The MC68377 chip contains twelve modules. These modules are:

1. MC68000 family central processing unit **(**CPU32X)
2. Burst integration module **(**BIM)
3. 32-Kbyte (16-Kbyte x 16) fast access SRAM module (FASRAM)
4. Two time processor units (TPU3)
5. Dual-port RAM for TPU3 (DPTRAM)
6. Two queued serial modules (QSM)
7. 10-bit queued analog to digital converter module (QADC64)
8. Analog multiplexer (AMUX)
9. Configurable timer module (CTM9)
10. CAN serial communication module (TouCAN)
11. J1850 serial communication module (DLCMD2)
12. Four 512-byte SRAM modules (SRAM)

1.3 Referenced Documents

As a complement to the present document, the following Motorola documents provide an in-depth functional description of the MC68377 modules:

- MC68332 User's Manual (**MC68332UM/AD**)
- CPU32 Central Processor Unit Reference Manual (**CPU32RM/AD**)
- QSM Reference Manual (**QSMRM/AD**)
- TPU documentation (**TPULITPAK/D**, including the **TPURM/AD**)
- MC68336/376 Reference Manual with TouCAN (**MC68336/376RM/AD**)
- Configurable Timer Module Reference Manual (**CTMRM/AD**)

1.4 Feature List

The major features of the MC68377 are:

- Modular architecture:
  - — Compatible with the current modular library of peripherals
  - — Separate program bus (imb) and data bus (FAB — fast access bus)
  - — Burst mode internal bus (IMB) and external bus for instruction fetches
  - — Burst mode chip select for glueless connection to burst mode memories
  - — Fast one clock access static RAM for data accesses (FASRAM)
  - — Fully static implementation
- 32-Bit 68000 family CPU (CPU32x):
  - — Object code compatible with the CPU32
  - — Greater than 2X performance increase over CPU32 at same system frequency
  - — Clock doubled (2X system clock) operation
  - — Burst mode program fetches
  - — Six word instruction prefetch queue
  - — One-clock fast access data bus (FAB)
  - — Virtual memory implementation
  - — Loop mode of instruction execution
  - — Improved exception handling for controller applications
  - — Table lookup and interpolate instruction
  - — High level language support
  - — Hardware breakpoint signal, background debug mode
- Burst integration module (BIM):
  - — External asynchronous bus and synchronous burst mode bus support
  - — Improved memory access timing
  - — One burst mode chip select output (five pins)
  - — Seven programmable asynchronous chip select outputs
  - — Three modes of operation: master mode, single chip mode, and emulation mode
  - — System protection logic with improved loss-of-oscillator protection
  - — Automatic configuration from shadow registers
  - — System clock based on 5.50-MHz crystal
  - — Watchdog timer, clock monitor, and bus monitor
- 32-Kbyte (16-Kbyte x 16) fast access SRAM (FASRAM):
  - — Dynamic dual access on IMB and FAB
  - — Separate standby power supply pin for 32 Kbytes of standby SRAM
- Two serial I/O subsystems (queued serial module: QSM):
  - — Enhanced SCI (UART): modulus baud rate generator, parity
  - — Queued SPI: 80-byte RAM, up to 16 automatic transfers, continuous cycling, eight to 16 bits per transfer, LSB/MSB first
  - — Dual function I/O port pins
- 10-Bit queued analog to digital converter with internal analog multiplexer (QADC64/AMUX):
  - — 26 channels (with two 8-bit internal analog MUXs)
  - — Four automatic channel selection and conversion modes

- — Two channel scan queues of variable length
- — Queue pointers indicate current location for each queue
- — Automated queue modes initiated by software command, external edge trigger/level gate, or one periodic/interval timer assignable to both queue one and two
- — Sub-queues possible using pause mechanism
- — Queue complete and pause software interrupts available in both queues
- — 64 result registers and three result alignment formats
- — Programmable input sample time
- — 10-bit A/D converter with internal sample/hold
- — Typical conversion time is 10 µs (100-Kbyte samples/sec) full accuracy
- — Programmable frequency and duty cycle for A/D converter clock

• Two time processor units (TPU3) (refer to **Appendix C**):

- — 16 channels — each is associated with a pin
- — Each channel can perform any time function
- — Each time function may be assigned to more than one channel
- — Each channel has an event register comprised of: 16-bit capture register, 16-bit compare/match register, 16-bit ≥ comparator
- — Each channel can be programmed to perform match or capture operations with one, or both, of the two 16-bit free running timer count registers (TCR1 and TCR2)
- — TCR1 is clocked from the internal TPU3 system clock
- — TCR2 may be clocked or gated from the external T2CLK pin
- — All time primitives are microcoded
- — Four Kbytes of microstore program ROM space
- — All channels have eight 16-bit parameter registers
- — A hardware scheduler with three priority levels is included
- — Resolution is one system clock period
- — Modulus prescaler (DIV 2, 4, 6..... 62, 64)

• Six Kbytes dual port memory for TPU3 (DPTRAM):

• Configurable timer module #9 (CTM9):

- — One bus interface unit submodule (BIUSM)
- — One counter prescaler submodule (CPSM)
- — One free-running counter submodule (FCSM)
- — Two modulus counter submodule (MCSM)
- — Four single action submodules (SASM)
- — Four double action submodules (DASM)
- — Four dedicated PWM submodules (PWMSM)

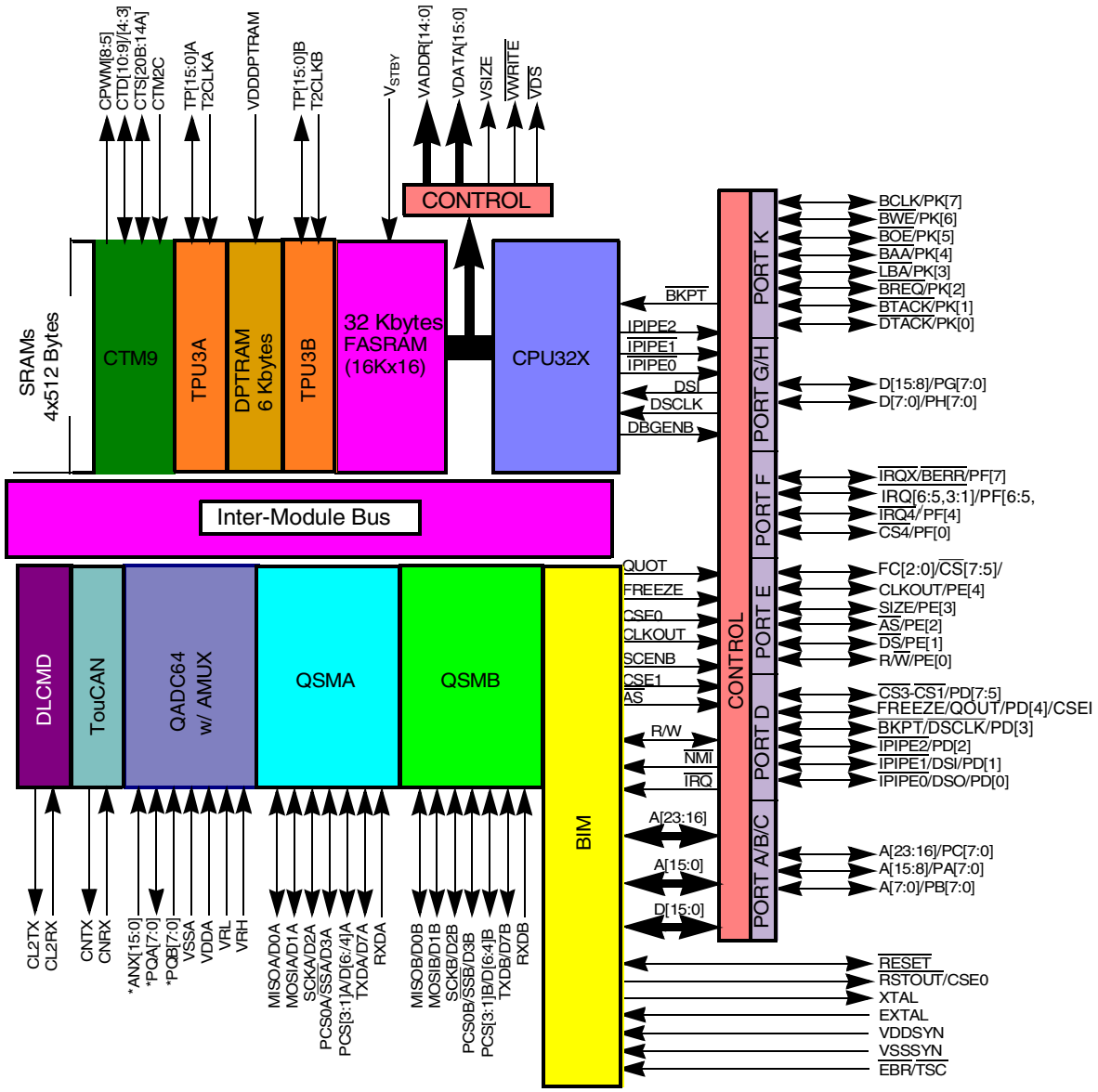
• Data link controller module digital (DLCMD)

- — Requires a 22 MHz system clock for correct bit timing
- — GM class-two compatible / SAE J1850 compatible
- — 10.4 KBps VPW bit format
- — Handles all network protocol functions
- — Message buffering on transmit (11 bytes — full message) and on receive (20 bytes)
- — Hardware CRC generation and checking
- — Transmit and receive block mode support

- CAN 2.0B controller module (TouCAN™):
  - — Full implementation of CAN protocol — version 2.0B.
  - — Standard/extended data and remote frames (up to 109/127 bits long).
  - — Programmable bit rate up to one Mbit/s, derived from system clock.
  - — 16 Rx/Tx message buffers of 0-8 bytes data length, of which two buffers are configurable to work as Rx buffers with specific programmable masks.
  - — Full implementation of CAN protocol — version 2.0B.
  - — Standard/extended data and remote frames (up to 109/127 bits long).
  - — Programmable bit rate up to one Mbit/s, derived from system clock.
  - — 16 Rx/Tx message buffers of 0-8 bytes data length, of which two buffers are configurable to work as Rx buffers with specific programmable masks.
- SRAM
  - — Two Kbytes (4 x 512 bytes) static RAM (SRAM).
- Package: 324-pin BGA
- Technology: sub-micron HCMOS
- Operating temperature: -40° C to 125° C
- Operating frequency: 22.00-MHz maximum system clock at V_{DD} = 3.3 V 5%
- 3.3-V core voltage (3.3-V external interface with 5-V tolerant inputs).
- 5-V general purpose digital I/O.

1.5 Functional Block Diagram

A functional block diagram of the MC68377 chip appears in **Figure 1-1**:



*See **Table 8-1** for breakdown of pin functions.

Figure 1-1 Block Diagram

Table 1-1 MC68377 Pin Usage/Pin Definitions

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Voltage	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Output Type
BIM	A[15:8]/PA[7:0]	8	I/O	Address[15:8]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortA[7:0]	5 V	—	sel[2]	sel[3]				
	A[7:0]/PB[7:0]	8	I/O	Address[7:0]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortB[7:0]	5 V	—	sel[2]	sel[3]				
	A[23:16]/ PC[7:0]	8	I/O	Address[23:16]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortB[7:0]	5 V	—	sel[2]	sel[3]				
	IPIPE0/DSO/ PD[0]	1	O	Pipe tracking	—	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			O	BDM serial output data	—	—	3.3 V	40 pf/80 pf				
			I/O	PortD[0]	5 V	—	sel[2]	sel[3]				
	IPIPE1/DSI/ PD[1]	1	O	Pipe tracking	—	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			I	BDM serial data input	3.3 V	—	—	—				
			I/O	PortD[1]	5 V	—	sel	sel[3]				
	IPIPE2/PD[2]	1	O	Pipe tracking	—	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			I/O	PortD[1]	5 V	—	sel[2]	sel[3]				
	$\overline{BKPT}$/$\overline{DSCLK}$/ PD[3]	1	I/O	Break point	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U	A
			I	BDM serial clock	3.3 V	—	—	—				
			I/O	PortD[3]	5 V	—	sel[2]	sel[3]				
	FREEZE/ QUOT/CSE1/ PD[4]	1	O	Freeze	—	H	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	TP	A
			O	Quotient out	—	—	3.3 V	40 pf/80 pf				
			O	Emulation mode chip select[1]	—	—	3.3 V	40 pf/80 pf				
			I/O	PortD[4]	5 V	—	sel[2]	sel[3]				
	$\overline{CS}$[3:1]/PD[7:5]	3	O	Chip selects[3:1]	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	TP	A[1]
			I/O	PortD[7:5]	5 V	—	sel[2]	sel[3]				
	R/$\overline{W}$/PE[0]	1	I/O	Read/write	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	TP	A[1]
			I/O	PortE[0]	5 V	—	sel[2]	sel[3]				
	$\overline{DS}$/PE[1]	1	I/O	Data strobe	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	TP	A[1]
			I/O	PortE[1]	5 V	—	sel[2]	sel[3]				
	$\overline{AS}$/PE[2]	1	I/O	Address strobe	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	TP	A[1]
			I/O	PortE[2]	5 V	—	sel[2]	sel[3]				
	SIZE/PE[3]	1	I/O	Transfer size	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[4]	A[1]
			I/O	PortE[3]	5 V	—	sel[2]	sel[3]				
	CLKOUT/PE[4]	1	O	Clock output	—	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			I/O	PortE[2]	5 V	—	sel[2]	sel[3]				

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
BIM	FC[2:0]/ $\overline{CS}$[7:5]/PE[7:5]	3	O	Function code[2:0]	—	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			O	Chip selects[7:5]	—	L	3.3 V	40 pf/80 pf				
			I/O	PE[7:5]	5 V	—	sel[2]	sel[3]				
	$\overline{CS}$[4]/PF[0]	1	O	Chip select[4]	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortF[0]	5 V	—	sel[2]	sel[3]				
	$\overline{IRQ}$[3:1]/ PF[3:1]	3	I/O	Interrupt request[3:1]	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			I/O	PortF[3:1]	5 V	—	sel[2]	sel[3]				
	$\overline{IRQ4}$/PF[4]	1	I/O	Interrupt request[4]	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			I/O	PortF[4]	5 V	—	sel[2]	sel[3]				
	$\overline{IRQ}$[6:5]/ PF[6:5]	2	I/O	Interrupt request[6:5]	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A
			I/O	PortF[6:5]	5 V	—	sel[2]	sel[3]				
	$\overline{IRQX}$/$\overline{BERR}$/ PF[7]	1	I/O	Interrupt request	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U	A
			I/O	Bus Error	3.3 V	L	sel[2]	3.3 V				
			I/O	PortF[7]	5 V	—	sel[2]	sel[3]				
	D[11,9,8]/ PG[3:,1,0]	3	I/O	Data bus[11,9,8]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[5]	A[1]
			I/O	PortG[3,1,0]	5 V	—	sel[2]	3.3 V				
	D[15:12,10]/ PG[7:4,]	5	I/O	Data bus[15:12,10]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U	A[1]
			I/O	PortG[7:4,2]	5 V	—	sel[2]	3.3 V				
	D[7:2,0]/ PH[7:2,0]	7	I/O	Data bus[7:0]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Sync	U/D[5]	A[1]
			I/O	PortH[7:0]	5 V	—	sel[2]	3.3 V				
	D[1]/PH[1]	1	I/O	Data bus[1]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Sync	U	A[1]
			I/O	PortH[1]	5 V	—	sel[2]	3.3 V				
	$\overline{DTACK}$/PK[0]	1	I/O	Data bus[1]	3.3 V	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[4]	A
			I/O	PortH[1]	5 V	—	sel[2]	3.3 V				
	$\overline{BTACK}$/PK[1]	1	I/O	Burst transfer acknowledge	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[4]	A
			I/O	PortK[1]	5 V	—	sel[2]	3.3 V				
	$\overline{BREQ}$/PK[2]	1	I/O	Burst request	3.3 V	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[4]	A[1]
			I/O	PortK[2]	5 V	—	sel[2]	3.3 V				
	$\overline{LBA}$/PK[3]	1	O	Burst CS load burst address	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[4]	A[1]
			I/O	PortK[3]	5 V	—	sel[2]	3.3 V				
	$\overline{BAA}$/PK[4]	1	O	Burst CS ad-dress advance	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortK[4]	5 V	—	sel[2]	3.3 V				

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
BIM	$\overline{BOE}$/PK[5]	1	O	Burst CS output enable	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	U/D[4]	A[1]
			I/O	PortK[5]	5 V	—	sel[2]	3.3 V				
	$\overline{BWE}$/PK[6]	1	O	Burst CS write enable	—	L	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortK[6]	5 V	—	sel[2]	3.3 V				
	BCLK/PK[7]	1	O	Burst CS clock	—	—	3.3 V	40 pf/80 pf	TP	Hyst/ Sync	—	A[1]
			I/O	PortK[7]	5 V	—	sel[2]	3.3 V				
	RESET	1	I/O	Reset	3.3 V	L	3.3 V	40 pf/80 pf	OD	Hyst/ Sync	U	A
	$\overline{RSTOUT}$/CSE0	1	O	Burst CS clock	—	L	3.3 V	40 pf/80 pf	TP	—	U	A[6]
			O	PortK[7]	—	—	3.3 V	40 pf/80 pf				
	XTAL	1	—	Crystal	—	L	—	—	—	—	—	—
	EXTAL	1	—	Crystal external clock	—	L	—	—	—	—	—	—
	$\overline{EBR}$/$\overline{TSC}$	1	I	External bus request	3.3 V	L	—	—	—	Hyst/ Sync	U	A
			I	Tri-state control	3.3 V	L	—	—				
	Total for Module = 77 pins											
FAS-RAM	VADDR[14:0]	15	O	Visibility ad-dress bus	—	—	3.3 V	40 pf/80 pf	TP	—	D	A
	VDATE[15:0]	16	O	Visibility data bus	—	—	3.3 V	40 pf/80 pf	TP	—	D	A
	VWRITE	1	O	Visibility bus write strobe	—	L	3.3 V	40 pf/80 pf	TP	—	D	A
	$\overline{VDS}$	1	O	Visibility bus data strobe	—	L	3.3 V	40 pf/80 pf	TP	—	D	A
	VSIZE	1	O	Visibility bus operand size	—	—	3.3 V	40 pf/80 pf	TP	—	D	A
	V_{STBY}	1	—	Standby supply voltage	3.3 V	—	—	—	—	—	—	—
	Total For Module = 35 Pins											

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
QADC64	AN[54:52]/ PQA[2:0]	3	I	Port A analog inputs[54:52]	An	—	—	—	—	—	—	B
			I/O	Port A digital I/O[2:0]	5 V	—	5 V/ sel[7]	50 pf	TP	Hyst/ Sync		
	AN55/ETRIG1/ PQA3	1	I	Port A analog input[55]	An	—	—	—	—	—	—	B
			I/O	Port A digital I/O[3]	5 V	—	5 V/ sel[7]	50 pf	TP	Hyst/ Sync		
	AN56/ETRIG2/ PQA4	1	I	Port A analog input[56]	An	—	—	—	—	—	—	B
			I	Port A external trigger[2]	5 V	L/H	—	—	—	Hyst/ Sync		
			I/O	Port A digital I/O[4]	5 V	—	5 V/ sel[7]	50 pf	TP	Hyst/ Sync		

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
QADC64	AN[59:57]/ PQA[7:5]	3	I	Port A analog inputs[59:57]	An	—	—	—	—	—	—	B
			I/O	Port A digital I/O[7:5]	5 V	—	5 V/ sel[7]	50 pf	TP	Hyst/ Sync		
	AN0/ANW/ PQB0 (For Test Pur-poses Only)	1	I	Por tB analog input[0]	An	—	—	—	—	—	—	B
			I	Port B analog input[W]	An	—	—	—	—	—		
			I	Port B digital input[0]	5 V	—	—	—	—	Hyst/ Sync		
	AN1/ANX/ PQB1 (For Test Pur-poses Only)	1	I	PortB analog input[1]	An	—	—	—	—	—	—	B
			I	Port B analog input[X]	An	—	—	—	—	—		
			I	Port B digital input[1]	5 V	—	—	—	—	Hyst/ Sync		
	AN2/ANY/ PQB2 (For Test Pur-poses Only)	1	I	Port B analog input[2]	An	—	—	—	—	—	—	B
			I	Port B analog input[Y]	An	—	—	—	—	—		
			I	Port B digital input[2]	5 V	—	—	—	—	Hyst/ Sync		
	AN3/ANZ/ PQB3	1	I	Port B analog input[3]	An	—	—	—	—	—	—	B
			I	Port B analog input[Z]	An	—	—	—	—	—		
			I	Port B digital input[3]	5 V	—	—	—	—	Hyst/ Sync		
	AN[51:48]/ PQB[7:4]	4	I	Port B analog inputs[51:48]	An	—	—	—	—	—	—	B
			I	Port B digital inputs[7:4]	5 V	—	—	—	—	Hyst/ Sync		
	ANX[15:0]	16	I	Mux'd analog inputs[15:0]	An	—	—	—	—	—		B
	V_{RH}	1	—	Voltagle reference high	5 V	—	—	—	—	—		—
	V_{RL}	1	—	Voltagle reference low	—	—	—	—	—	—		—
	V_{DDA}	1	—	Analog supply	5 V	—	—	—	—	—		—
	V_{SSA}	1	—	Analog ground	—	—	—	—	—	—		—
	Total For Module = 36 Pins											

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
QSMA	MISOA/D0A	1	I/O	Master in/slave out	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I/O	General purpose I/O D0	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	MOSIA/D1A	1	I/O	Master out/slave in	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I/O	General purpose I/O D1	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	PCS0A/$\overline{\text{SSA}}$/ D3A	1	I/O	Peripheral chip select0	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I	Slave select	5 V	L	—	—		Hys/ Sync		
			I/O	General purpose I/O D3	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	PCS[3:1]A/ D[6:4]A	3	I/O	Peripheral chip selects[3:1]	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I/O	General purpose I/O D[6:4]	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	TxDA/D7A	1	O	SCI transmit date	—	—	5 V/50 ns	200 pf	TP[8]	—	—	C
			I/O	General purpose I/O D7	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	RxDA	1	I	SCI receive data	5 V	—	—	—		Hyst		
	Total For Module = 9 pins											

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
QSMB	MISOB/D0B	1	I/O	Master in/slave out	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I/O	General purpose I/O D0	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	MOSIB/D1B	1	I/O	Master out/slave in	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I/O	General purpose I/O D1	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	PCS0B/$\overline{SSB}$/ D3B	1	I/O	Peripheral chip select0	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I	Slave select	5 V	L	—	—		Hys/ Sync		
			I/O	General purpose I/O D3	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	PCS[3:1]B/ D[6:4]B	3	I/O	Peripheral chip selects[3:1]	5 V	—	5 V/50 ns	200 pf	TP[8]	Hyst/ Sync	—	C
			I/O	General purpose I/O D[6:4]	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	TxDB/D7B	1	O	SCI transmit date	—	—	5 V/50 ns	200 pf	TP[8]	—	—	C
			I/O	General purpose I/O D7	5 V	—	5 V/ 600 ns	50 pf		Hyst		
	RxDB	1	I	SCI receive data	5 V	—	—	—		Hyst		
	Total For Module = 9 pins											
TPU3A	TP[15:0]A	16	I/O	Timer channel	5 V	L/H	5 V/ sel[7]	50 pf	TP	Hyst	—	C
	T2CLKA	1	I	External clock input	5 V	L/H	—	—	—	Hyst	U	C
	Total For Module = 17 pins											
TPU3B	TP[15:0]B	16	I/O	Timer channel	5 V	L/H	5 V/ sel[7]	50 pf	TP	Hyst	—	C
	T2CLKB	1	I	External clock input	5 V	L/H	—	—	—	Hyst	U	C
	Total For Module = 17 pins											
CTM9	CTM2C	1	I	External clock input	5 V	L/H	—	—	—	Hyst/ Sync	—	C
	CTD[4:3]	2	I/O	DASM channels[4:3]	5 V	L/H	5 V/ sel[7]	50 fp	TP	Hyst/ Sync	—	C
	CTM[8:5]	4	I/O	PWMSM channels[8:5]	5 V	L/H	5 V/ sel[7]	50 fp	TP	—	—	C
	CTD[10:9]	2	I/O	DASM Channels[10:9]	5 V	L/H	5 V/ sel[7]	50 fp	TP	Hyst/ Sync	—	C
	CTS[20B:14A]	8	I/O	SASM channels[20:14]	5 V	L/H	5 V/ sel[7]	50 fp	TP	Hyst/ Sync	—	C
	Total For Module = 17 pins											

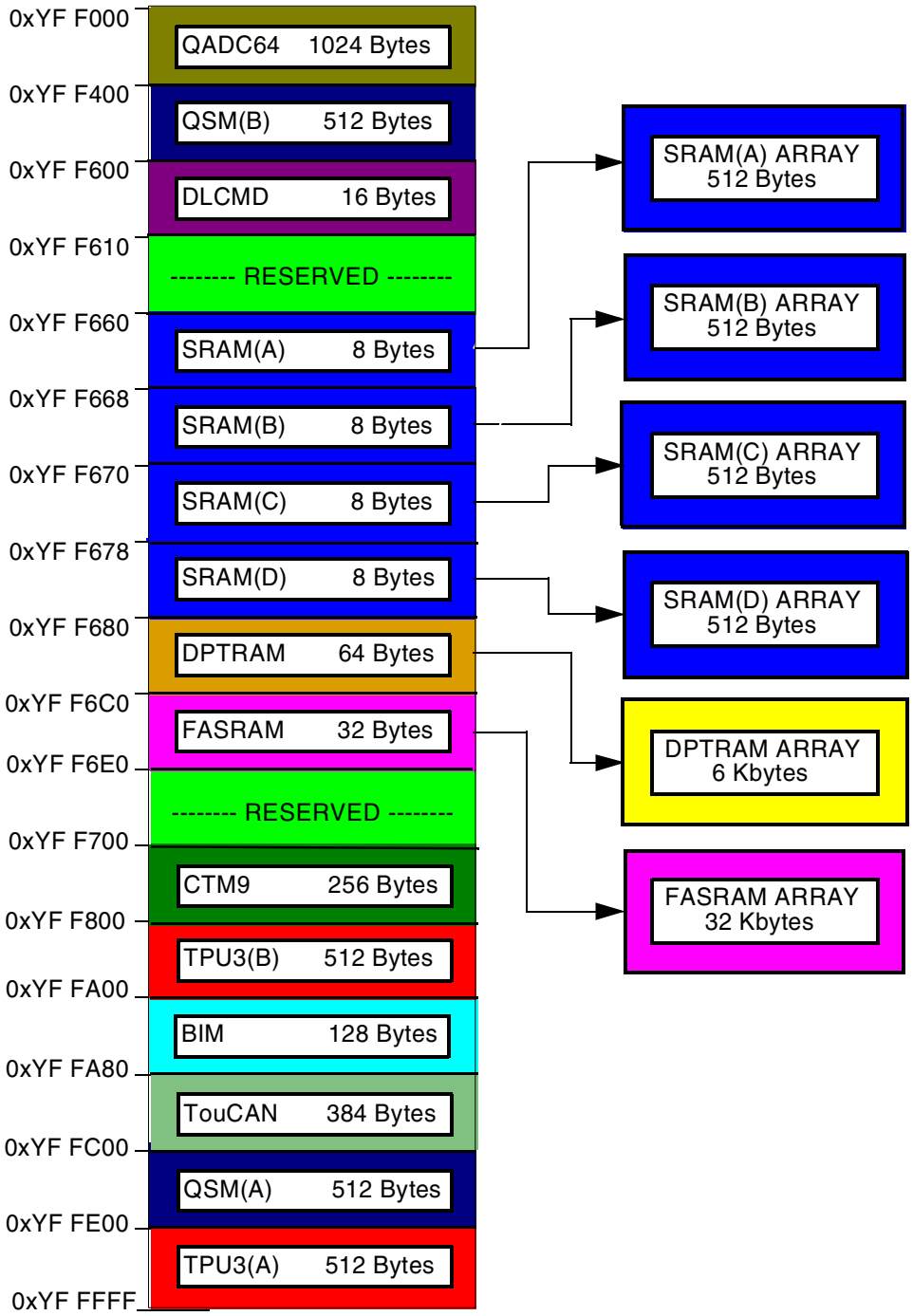
Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Volt-age	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Out-put Type
Tou-CAN	CNRX	1	I	CAN receive	5 V	—	—	—	—	—	—	C
	CNTX	1	O	CAN transmit	5 V	—	5 V/ 50ns	200 pf	TP[8]	—	—	C
	Total For Module = 2 pins											
DLMCD	CL2RX	1	I	Class 2 receive	5 V	—	—	—	—	—	—	C
	CL2TX	1	O	Class 2 transmit	5 V	—	5 V/50 ns	50 pf	TP	—	—	C
	CNRX	1	I	CAN receive	5 V	—	—	—	—	—	—	C
	Total For Module = 2 pins											

Table 1-1 MC68377 Pin Usage/Pin Definitions (Continued)

Module	Pin Name	Pins	I/O	Function	Input Voltage	Act Lvi	Output Voltage	Drive Stren.	Driver	Input Buffer	Pull Up/ Down	Output Type
POWER/ GND	V_{DDSYN}	1	—	Clock synthesizer power	3.3 V	—	—	—	—	—	—	—
	V_{SSSYN}	1	—	Clock synthesizer ground	—	—	—	—	—	—	—	—
	V_{DD3}	73	—	Supply voltage	3.3 V	—	—	—	—	—	—	—
	V_{SS}	23	—	Ground	—	—	—	—	—	—	—	—
	V_{DDS5}	10	—	Supply voltage	5 V	—	—	—	—	—	—	—
	$V_{DDPTRAM}$	1	—	DPTRAM supply	3.3 V	—	—	—	—	—	—	—
	Power/Ground = 103 pins											
Total Number of Pins for MCU = 324 Pins												
Sync = Synchronized Hyst = Hysteresis OD = Open Drain TP = Totem Pole An = Analog												

NOTES:
1. Driver three-stated on EBR.
2. Either 5-V / 600-ns slew rate or 3.3-V no slew rate control based upon state of FASTIO bit in BIM MCR.
3. Either 50 pf or 40 pf/80 pf drive strength based upon state of FASTIO bit in BIM MCR.
4. Pullup or pulldown at RESET depending upon PCON register bit. Disabled after RESET.
5. Pullup or pulldown at RESET depending upon PCON register bit. Pullup after RESET.
6. Will not three-state on TSC (required by PLL test mode).
7. Either 5-V / 600-ns or 5-V / 50-ns slew rate based upon state of FASTIO bit in BIM MCR.
8. Module will configure signals for OD operation.



Y = M111, where M is the MODMAP signal state on the IMB, which reflects the state of the MODMAP in the module configuration register of the burst integration module. (Y= 0x7 or 0xF).

Figure 1-2 MC68377 Address Map