SECTION 20
CDR3 FLASH (UC3F) EEPROM

20.1 Introduction

The U-bus CDR3 EEPROM module (UC3F) is designed for use in embedded microcontroller (MCU) applications targeted for high speed read performance and high density byte count requirements. The UC3F array uses a single transistor flash bit cell and is configured for a module of 512 Kbytes (524,288 bytes) of non-volatile memory (NVM). The UC3F array is divided into 64-Kbyte (65,536-byte) array blocks. The UC3F array size is created by using eight array blocks. Two blocks of the UC3F array memory map may be subdivided into two smaller blocks, a 16-Kbyte (16,384-byte) block and a 16-Kbyte block or a 16-Kbyte block and a 48-Kbyte (49,152-byte) block. The microcontroller's (MCU's) total flash requirements is distributed between two UC3F EEPROM modules on MPC565 / MPC566.

The primary function of the UC3F EEPROM module is to serve as electrically programmable and erasable NVM to store program instructions and/or data. It is a class of non-volatile solid state silicon memory device consisting of an array of isolated elements, an electrical means for selectively adding and removing charge to the elements, and a means of selectively sensing the stored charge in the elements. When power is removed from the device, the stored charge of the isolated elements will be retained.

The UC3F EEPROM module is arranged into two major sections as shown in **Figure 20-1**. The first section is the UC3F array used to store system program and data. The second section is the memory interface (MI) that controls operation of the UC3F array. The MI also serves as the interface between the UC3F array and a bus interface unit (BIU) which connects the UC3F array to the U-bus.

NOTE

If the flash arrays are disabled in the IMMR register (FLEN=0), then neither the UC3F array or the UC3F control registers are accessible.

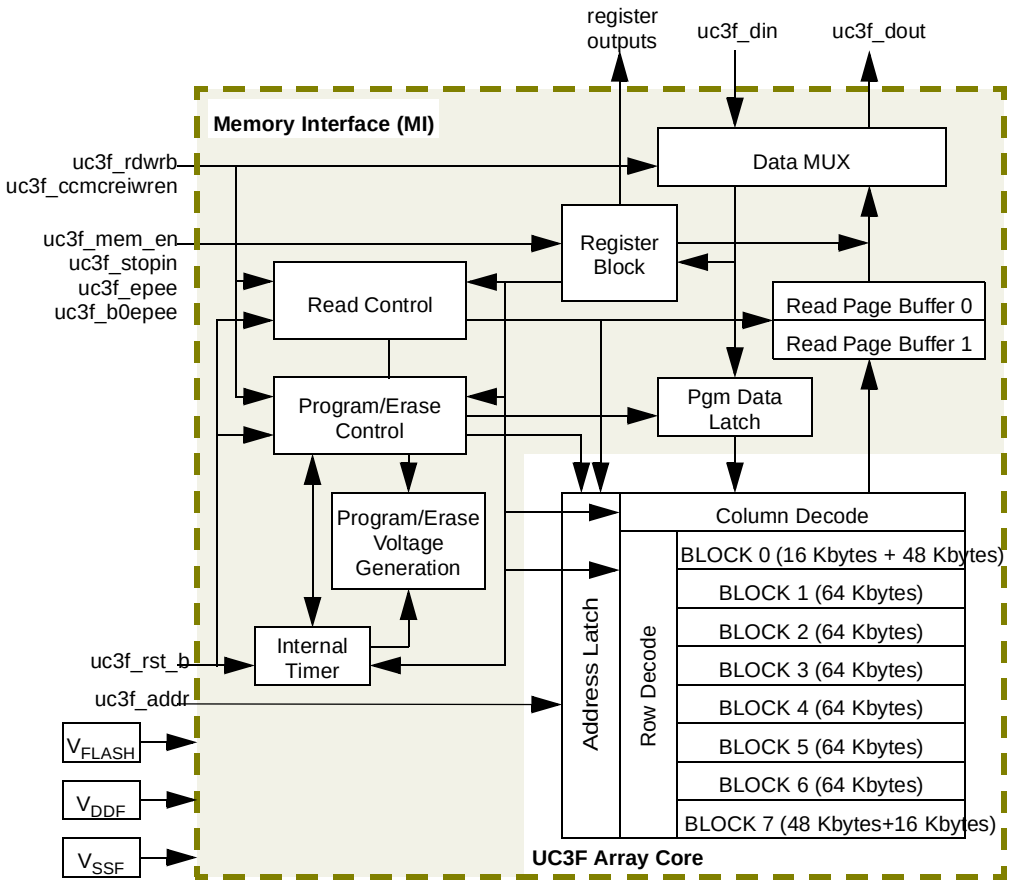

Figure 20-1 Block Diagram for a 512-Kbyte UC3F Module Configuration

The UC3F EEPROM module array is divided into array blocks to allow for independent erase, address attributes restrictions, and protection from program and erase for each array block. The size of a large array block in the UC3F module is fixed at 64 Kbytes. The size of a subdivided large block becomes the original large array block size minus 16 Kbytes, (64 Kbytes – 16 Kbytes = 48 Kbytes. The size of the small block, which is the remainder of the large block, is always 16 Kbytes. The total UC3F EEPROM array is distributed into eight large blocks, two of which contain small blocks. Information is transferred to the UC3F EEPROM by long-word (64 bits), word (32 bits), half-word (16 bits), or byte (eight bits).

To improve system performance, each array read access retrieves 32 bytes of information. These 32 bytes may be copied into one of two read page buffers aligned to the low order addresses. The two read page buffers are independently updated by page management logic contained in the BIU which interfaces to the UC3F EEPROM module.

To prevent unnecessary page accesses from the array, the UC3F memory interface (MI) shall monitor the incoming address to determine if the required information is in one of the two read page buffers. This strategy allows the UC3F array to have an off

page access and an on page access. In normal operation, write accesses to the UC3F array are not recognized except during program and erase operations.

The UC3F EEPROM uses an embedded hardware algorithm to program and erase the UC3F array. Special control logic is included to guard against accidental program or erase by requiring a specific series of read and write accesses to the UC3F control registers. Optional external inputs provide a hardware protection mechanism to prevent accidental program and erase of UC3F array blocks. The hardware algorithm automatically performs all necessary applications of high voltage pulses and verify reads of the UC3F array to ensure that all bits are programmed and erased with sufficient margin to guarantee data integrity and reliability.

20.1.1 Features of the CDR3 FLASH EEPROM (UC3F)

- High density single transistor flash bit cell
- -40 to 125° C ambient temperature operating range
- 2.5-V to 2.7-V V_{DDF} operating range and 4.75-V to 5.25-V V_{FLASH} operating range
- Shadow information stored in special flash NVM shadow locations
- Two 16-Kbyte small blocks per module
- 512 Kbytes per module using 64-Kbyte blocks
  - — One Mbyte total
- Array block restriction control for small and large blocks
  - — Erase by array block(s)
  - — Array protection for program and erase operations
  - — Array block assignment of supervisor or supervisor/user space
  - — Array block assignment of data or instruction/data space
- Internal 64-bit data path architecture
- Page mode read
  - — Retains two independent read page buffers
  - — Read page size of 32 bytes (eight words).
- Word (32-bit) programming
- Embedded hardware program and erase algorithm
  - — Uses internal oscillator to time program and erase pulses. Pulses are timed independently of system clock frequency
  - — Automatically performs margin reads
- Optional external flash program or erase enable inputs for block 0 or entire flash array
  - — Flash program or erase enables are selected from one of three sources: a pin external to the device, a register bit external to the UC3F but internal to the MCU, or always enabled
- Low power disable via an external signal or UC3F register bit
- Censor mode for flash memory array access restriction with a user bypass for unrestricted array access

20.1.2 Glossary of Terms Used

Array block — A 64-Kbyte UC3F array subdivision.

Array small block — The independently erasable 16-Kbyte subdivision of a 64-Kbyte array block.

Array host block — An array block containing a small block.

Array residual block — The 16-Kbyte or 48-Kbyte portion of a host block not contained in the small block.

BIU — Bus interface unit which controls access of the UC3F module through a standard system bus interface.

UC3F — The CDR3 flash EEPROM module.

CAM — Non-volatile content addressible memory cell used as a nonvolatile storage bit. CAMs are used for CENSOR bits.

Erase interlock write — A write to any UC3F array address after initializing the erase sequence.

IM — Integration module is a bus master which serves as the system bus arbitration unit on the microcontroller.

I**nitialize program/erase sequence** — The write to the high voltage control register that changes the SES bit from a 0 to a 1.

Mask option — A customer configurable option that is specified during the design process.

MCU — Microcontroller unit.

MI — Memory interface controls operation of the UC3F array.

Off page read — Array read operation that retrieves 32 bytes of information from the flash memory array and transfers the address selected eight bytes of the 32 bytes to the data out port.

On page read — Array read operation that accesses eight bytes of information stored in one of the read page buffers.

Programming write — A word write to a UC3F array address to transfer information into a program data latch. The UC3F EEPROM accepts programming writes after initializing the program sequence until the EHV bit is changed from a 0 to a 1.

Read page buffer — 32-byte block of information that is read from the UC3F array. This information is aligned to a 32-byte boundary within the UC3F array. Each UC3F module has two read page buffers.

Shadow information — The shadow provides 512 bytes of additional UC3F storage that is used for the reset configuration word and for additional user data. These loca-

tions may be accessed by setting the SIE bit in the module configuration register and accessing the UC3F array. The shadow information is always in the lowest numbered array block of the UC3F module.

SIU — System integration unit.

20.2 UC3F Interface

The UC3F module contains a memory interface (MI) and an array core. The MI controls access of the array core and register block in the UC3F module.

The interface signals to the UC3F module consist of address inputs, data inputs, data outputs, a simple set of control signals for read and write operations, a set of register selects, and a set of register outputs which are used by the BIU. Three required supply pins power the module: V_{DDF}, V_{SSF}, and V_{FLASH}.

The UC3F module is a fully asynchronous module and does not require a clock input for operation. All required clocks are generated internally using an internal oscillator, external test clock input, or internal delay circuits.

20.2.1 External Interface

The UC3F EEPROM module uses external pins to provide power supplies. These pins are listed in **Table 20-1**.

Table 20-1 UC3F External Interface Signals

Mnemonic	I/O Type	Description	Comments
V_{DDF}	Power Pin	UC3F power supply	To reduce noise in the read path no other circuits should be connected to the UC3F V_{DDF} supply pin.This V_{DD} pin must be isolated from all other V_{DD} pins inside the device. The specified voltage range during operation is 2.6 V ± 0.1 V.
V_{SSF}	Ground Pin	UC3F ground	To reduce noise in the read path no other circuits should be connected to the UC3F V_{SSF} supply. This V_{SS} pin must be isolated from all other V_{SS} pins inside the device.
VFLASH	Power Pin	UC3F 5-V power supply	VFLASH provides a 5-V supply to the UC3F module which is used for read, program, and erase operations. VFLASH must be in the range of 4.75 V to 5.25 V (5 V ± 5%) during operation.

Table 20-1 UC3F External Interface Signals (Continued)

Mnemonic	I/O Type	Description	Comments
EPEE	External Program/ Erase	EPEE pin status	The EPEE bit monitors the state of the external program/erase enable (EPEE) input. The UC3F module samples the EPEE input when EHV is asserted and holds that sampled state until EHV is negated.
B0EPEE	Block 0 External Program/ Erase	Block 0 EPEE pin status	The B0EM bit monitors the state of the Block 0 EPEE, B0EPEE, input. The UC3F module samples the B0EPEE input when EHV is asserted and holds that sampled value until EHV is negated.If B0EM = 1 when EHV is asserted, high voltage operations such as program or erase are enabled for either small block 0 or the lowest numbered block of the UC3F array regardless of the state of EPEE. If B0EM = 0 when EHV is asserted, high voltage operations are disabled for small block 0 or the lowest numbered block of the UC3F array regardless of the state of EPEE.

20.3 Programmer's Model

The UC3F EEPROM module consists of a control register block, an addressable shadow row implemented in flash, and an addressable main flash memory array. The control registers are used to configure, program, erase and exercise the UC3F shadow row and flash array.

20.3.0.1 UC3F EEPROM Module Control Register Addressing

The UC3F module control registers are selected with individual register selects generated from the BIU. As such, each flash module that is designed using the UC3F EEPROM module may uniquely define the addressing of the control register block.

Table 20-2 UC3F Register Programmer's Model

Address	Register
0x2F C800	Module A Configuration (UC3FMCR_A)
0x2F C804	High Voltage Control (UC3FCTL_A)
0x2F C808	Extended Module Configuration (UC3FMCRE_A)
0x2F C80C	Reserved
0x2F C840	Module A Configuration (UC3FMCR_B)
0x2F C844	High Voltage Control (UC3FCTL_B)
0x2F C848	Extended Module Configuration (UC3FMCRE_B)
0x2F C84C	Reserved

20.3.1 UC3F EEPROM Control Registers

The control registers are used to control UC3F EEPROM module operation. On reset, the registers are loaded with default reset information. Several bits of the UC3F control registers are special flash NVM registers which retain their state when power is

removed from the UC3F EEPROM. These special NVM registers are identified in the individual register field and control bit descriptions.

20.3.2 UC3F EEPROM Configuration Register (UC3FMCR)

The UC3F module configuration register is used to configure the operation and access restrictions of the UC3F array and shadow row.

UC3FMCR — UC3F EEPROM Configuration Register **0x2F C800**
0x2F C840

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
STOP	LOCK	Reserved		FIC	SIE	ACCESS	CENSOR	SUPV							
HRESET:															
0	1	0		0	0	0		1	1	1	1	1	1	1	1

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
DATA								PROTECT							
HRESET:															
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Reset State Determined by NVM Registers

Table 20-3 UC3FMCR Bit Descriptions

Bit(s)	Name	Description
0	STOP	Array stop control. When uc3f_stopin = 1 during the negation of uc3f_rst_b, the reset state of STOP is 1 and the C3F array wakes up in a disabled low power mode. Likewise, when uc3f_stopin = 0, the reset state of STOP is 0 and the UC3F array wakes up in a read mode. Writes to the STOP bit have no effect while in program or erase operation (SES = 1). The STOP bit is always readable whenever the registers are enabled. When STOP is set to 1, the UC3F array is disabled, and internal circuits are switched into a low power state. The STOP bit may be used to implement low power standby modes or power management schemes. At least the UC3FMCR remains readable and writable when STOP = 1 so that the STOP bit may be deasserted. Attempts to program or erase the array while STOP = 1 have no effect. SES cannot be set to 1 when STOP = 1. When STOP = 0, the UC3F array is enabled for accesses. In addition, all registers which were disabled with STOP = 1 are now enabled. A STOP recovery time of 1 µs is required for biases in the UC3F array to reach their appropriate levels to resume normal operation. Operations to the UC3F array should be delayed for at least 1µs after clearing the STOP bit. 0 = UC3F array is enabled 1 = UC3F array is disabled
1	LOCK[1]	Lock control. The default reset state of $\overline{\text{LOCK}}$ is 1. $\overline{\text{LOCK}}$ can be written to 0 once after reset when CSC = 0 to allow protection of the write-locked register bits after initialization. When the $\overline{\text{LOCK}}$ control bit in the UC3FMCR Register is written to a 0, the write-locked register bits: BPB, FIC, SUPV, SBSUPV[0:1], DATA, SBDATA, PROTECT, SBPROTECT, and SBEN[0:1] are locked. Writes to these bits while $\overline{\text{LOCK}}$ = 0 will have no effect. Once the $\overline{\text{LOCK}}$ bit has been asserted ($\overline{\text{LOCK}}$ = 0) in normal operating mode, the write-lock can only be disabled again by a reset. When the device is in background debug mode and CSC = 0, the $\overline{\text{LOCK}}$ bit may be written from a 0 to a 1. **WARNING**: If the lock protection mechanism is enabled ($\overline{\text{LOCK}}$ = 0) before PROTECT and SBPROTECT are cleared, the device must use background debug mode to program or erase the UC3F EEPROM.
2	—	Reserved
3	FIC	Force information censorship. The default reset state of FIC is normal censorship operation (FIC = 0). The FIC bit is write protected by the $\overline{\text{LOCK}}$ bit and the CSC bit. Writes will have no effect if $\overline{\text{LOCK}}$ = 0 or CSC = 1. Once FIC is set (FIC = 1), it can not be cleared except by a reset. The FIC bit can be read whenever the registers are enabled. The FIC bit is a censorship emulation mode used to aid in the development of custom techniques for controlling the ACCESS bit without setting CENSOR[0:1] to the information censorship state. Using FIC to force information censorship allows testing of the hardware and software for setting ACCESS without setting CENSOR[0:1] = 11 and risk permanently setting the device into an unusable information censorship state. 0 = normal uc3f censorship operation 1 = forces the uc3f into information censorship model
4	SIE	Shadow information enable. The default reset state of SIE is 0. The SIE bit is write protected in program operation (SES = 1 and PE = 0). The SIE bit can be read whenever the registers are enabled. When SIE = 1, normal array accesses are disabled, and the two shadow information rows are enabled. Array accesses are directed to the shadow row while SIE = 1. When an array location is read in this mode, only the lower 6 address bits are used to select which 64 bits of the 512-byte shadow row are read. The upper address bits are not used for shadow row decoding. The read page buffer address monitor shall be reset whenever SIE is modified making the next UC3F array access an off page access. 0 = normal array access 1 = disables normal array access and selects the shadow information rows

Table 20-3 UC3FMCR Bit Descriptions (Continued)

Bit(s)	Name	Description
5	ACCESS	Enable uncensored access. A censored access to the UC3F EEPROM is any access where the device is in the censored mode (uc3f_censor_b = 0). The default reset state is ACCESS is a 0 so that FIC and CENSOR[0:1] control the level of censorship to the UC3F EEPROM array. All accesses to the UC3F EEPROM array shall be allowed if ACCESS = 1. ACCESS can be read whenever the registers are enabled. ACCESS provides a method to bypass the UC3F EEPROM module censorship. 0 = censored uc3f array access allowed only if the c3f censorship is no censorship 1 = allows all uc3f array access
6:7	CENSOR	Censor accesses. The CENSOR[0:1] bits are implemented using nonvolatile register bits or CAM cells. The reset state of CENSOR[0:1] is user defined by the contents stored in the NVM register bits. CENSOR is not writable but the NVM register's data can be set or cleared to the desired reset state. Reading CENSOR while setting or clearing with the high voltage applied (CSC = 1 and HVS = 1) will return 0's. 00 = cleared censorship, UC3F array access allowed only if device is in uncensored mode 01 = no censorship, all UC3F array accesses allowed 10 = no censorship, all UC3F array accesses allowed 11 = information censorship, UC3F array access allowed only if device is in uncensored mode
8:15	SUPV	Supervisor space. The SUPV bits are used to assign supervisor space restrictions for each block of the UC3F array. The index for the SUPV bit field is used to determine block assignment. For example, SUPV[0] is used for the supervisor space assignment of array block 0, while SUPV[4] is used for array block 4 Supervisor space assignment. Array block M is mapped into supervisor address space when SUPV[M] = 1, and only supervisor accesses are allowed to array block M. If SUPV[M] = 0, then array block M is mapped into unrestricted address space which allows both supervisor and user accesses to array block M. The SUPV bits are not actually used in the UC3F EEPROM module but are used by the BIU to determine access restrictions to UC3F array on a blockwise basis. The block addresses are decoded in the BIU to determine which array block is selected, and the selected block's SUPV bit is compared with the address space attributes to determine validity of an array access. When the small block function is enabled, the enabled small block portion of an array block is not controlled by the SUPV bit corresponding to the array block containing that small block. This particular small block is controlled by the appropriate SBSUPV bit while the remainder of that array block is controlled by its SUPV bit. 0 = array block m is placed in unrestricted address space 1 = array block m is placed in supervisor address space

Table 20-3 UC3FMCR Bit Descriptions (Continued)

Bit(s)	Name	Description
16:23	DATA	Data space. The DATA bits are write protected by $\overline{\text{LOCK}}$ and CSC. Writes to DATA have no effect if $\overline{\text{LOCK}}$ = 0 or CSC = 1. The DATA bits may be read whenever the registers are enabled. Each array block of the UC3F EEPROM may be mapped into data or data and instruction address space. When array block M is mapped into data address space (DATA[M] = 1), only data accesses will be allowed. When array block M is mapped into both Data and Instruction address space (DATA[M] = 0), both data and instruction accesses will be allowed. The DATA bits are not actually used in the UC3F EEPROM module but are used by the BIU to determine access restrictions to UC3F array on a blockwise basis. The block addresses are decoded in the BIU to determine which array block is selected, and the selected block's DATA bit is compared with the address space attributes to determine validity of an array access. When the small block function is enabled, the enabled small block portion of an array block is not controlled by the DATA bit corresponding to the array block containing that small block. This particular small block is controlled by the appropriate SBDATA bit while the remainder of that array block is controlled by its DATA bit. 0 = array block m is placed in both data and instruction address spaces 1 = array block m is placed in data address space
24:31	PROTECT	Block protect. Each array block of the UC3F EEPROM can be individually protected from program or erase operation. The contents of array block M are protected from program or erase by setting PROTECT[M] = 1. The UC3F will perform all program and erase interlocks and complete the program or erase sequence, but the program and erase voltages are not applied to locations within the protected array block(s), blocks whose corresponding PROTECT bit is set to 1. By setting PROTECT[M] = 0, array block M is enabled for program and erase operation, and its contents may be altered by programming or erasing. When the small block function is enabled, the enabled small block portion of an array block is not controlled by the PROTECT bit corresponding to the array block containing that small block. This particular small block is controlled by the appropriate SBPROTECT bit while the remainder of that array block is controlled by its PROTECT bit. 0 = array block m is unprotected 1 = array block m is protected

NOTES:
1. Note that the LOCK bit is in a different bit location on the MPC565 / MPC566 than in the MPC555/556.

20.3.3 UC3F EEPROM Extended Configuration Register (UC3FMCRE)

The UC3FMCRE is an extended module configuration register used for configuring the small block functions. In addition, 16 bits of the UC3FMCRE are used to provide a source for module identification.

UC3FMCRE— UC3F EEPROM Extended Configuration Register **0x2F C804**
0x2F C844

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SBEN		SBSUPV		SBDATA		SBPROTECT		Reserved		BIU					
HRESET:															
0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
MEMSIZ			BLK	MAP	SBLKL		FLASHID								
HRESET:															
1	0	1	1	0	X[1]	X	0	0	0	0	0	0	0	0	0

NOTES:
1. SBLKL = 0b10 for module A and SBLKL = 0b01 for module B.

Table 20-4 UC3FMCRE Bit Descriptions

Bit(s)	Name	Description
0:1	SBEN	Small block enable. When SBEN[M]=0, the corresponding small block M behaves logically as if the small block is still part of the larger host block. In addition, the small block protect bit (SBPROTECT[M]), the small block supervisor bit (SBSUPV[M]), the small block data bit (SBDATA[M]), and the small block BLOCK bit (SBBLOCK[M]) corresponding to small block M have no effect. The corresponding small block is controlled by the same protect, supervisor, data, and block bits that control its host block. When SBEN[M] = 1, the corresponding small block M can be programmed and erased independently of its host block. The corresponding small block protect bit, the small block supervisor bit, the small block data bit, and the small block bit are enabled by SBEN. For example: when SBEN[0] = 0, Small Block 0 (16 Kbytes) and the residual block (16 Kbytes or 48 Kbytes) contained in the host block of Small Block 0 are programmed and erased as if the two blocks are one large array block (32 Kbytes or 64 Kbytes). When SBEN[0] = 1, small block 0 and the residual block contained in the host block of small block 0 behave as two separate blocks, i.e. small block 0 and the residual block in small block 0's host block can be programmed and erased independently of each other. 0 = small block M behaves as part of the host block 1 = small block M functions independent of host block
2:3	SBSUPV	Small block supervisor space. Each small array block of the UC3F EEPROM may be mapped into supervisor or unrestricted address space. When small array block M is mapped into supervisor address space, SBSUPV[M] = 1, only supervisor accesses are allowed. When small block M is mapped to unrestricted address space, SBSUPV[M] = 0, both supervisor and user accesses are allowed. If SBEN[M] = 0, the corresponding small block M is logically part of the host block and SBSUPV[M] has no effect. Instead, the corresponding SUPV[M] bit will be used to determine if the small block is mapped to Supervisor or Unrestricted address space. Like the SUPV[0:7] bits, SBSUPV are not actually used in the UC3F EEPROM module but are used by the BIU to determine access restrictions to the UC3F array. Block addresses are decoded in the BIU to determine which small array block is selected, and the selected small block's SBSUPV bit is compared with the address space attributes to determine validity of an array access. 0 = small block M is placed in unrestricted address space 1 = small block M is placed in supervisor address space

Table 20-4 UC3FMCRE Bit Descriptions (Continued)

Bit(s)	Name	Description
4:5	SBDATA	Small block data space. Each small array block of the UC3F EEPROM may be mapped into data or both data and instruction address space. When a small array block is mapped into data address space, SBDATA[M] = 1, only data accesses will be allowed. When a small array block is mapped into both data and instruction address space, SBDATA[M] = 0, both data and instruction accesses will be allowed. If SBEN[M] = 0, the corresponding small block M is logically part of the host block and SBDATA[M] has no effect. Instead, the corresponding DATA[M] bit will be used to determine if the small block is mapped to Data or to both Data and Instruction address space. Like the DATA bits, SBDATA are not actually used in the UC3F EEPROM module but are used by the BIU to determine access restrictions to the UC3F array. Block addresses are decoded in the BIU to determine which small array block is selected, and the selected small block's SBDATA bit is compared with the address space attributes to determine validity of an array access. 0 = small block M is place in both Data and Instruction address spaces 1 = small block M is place in Data address space
6:7	SBPRO-TECT	Small block protect. Each small block of the UC3F EEPROM can be individually protected from program or erase operation. The UC3F will perform all program and erase interlocks and even complete the program or erase sequence, but the program and erase voltages are not applied to locations within the protected small block(s). 0 = small block M is unprotected 1 = small block M is protected
8:9	—	Reserved
10:15	BIU	BIU configuration bits. These register bits are reserved for BIU functionality and are strictly outputs from the UC3F EEPROM.
16:18	MEMSIZ	Memory size. The MEMSIZ field is used to indicate the UC3F array size. The MEMSIZ bits are read only and writes have no effect. 0b000 = UC3F array is 64 Kbytes 0b001 = UC3F array is 128 Kbytes 0b010 = UC3F array is 192 Kbytes 0b011 = UC3F array is 256 Kbytes 0b100 = unused 0b101 = UC3F array is 512 Kbytes 0b110 = unused 0b111 = unused Both modules on the MPC565 / MPC566 are 512 Kbytes.
19	BLK	Block size. The BLK bit is used to indicate the array block size used in the UC3F array. The BLK bit is read only and writes have no effect. 0 = array block size is 32 Kbytes 1 = block size is 64 Kbytes
20	MAP	Array address mapping. The MAP bit is used to indicate the UC3F array address mapping within a 2^N address space. The MAP bit is read only and writes have no effect. The MAP bit is more useful when the UC3F array is a non-2^N size. When MAP = 0, the UC3F array is mapped to the bottom (starting at address 0) of the 2^N space in which the array resides. For modules with 2^N array sizes, the MAP bit is always set to 0. When MAP = 1, the UC3F array is mapped to the top (ending at address all $F's) of the 2^N space in which the array resides. The 192KB and 384KB modules are the only two allowed configurations of the UC3F module which have non-2^N array sizes. If MAP = 1 for a 192-Kbyte or 384-Kbyte array, the UC3F array is mapped starting at the respective 64KB offset from the beginning of a 256-Kbyte address space or 128-Kbyte offset from the beginning of a 512-Kbyte address space. 0 = UC3F array is mapped to top of 2^N address space 1 = UC3F array is mapped to bottom of 2^N address space

Table 20-4 UC3FMCRE Bit Descriptions (Continued)

Bit(s)	Name	Description
21:22	SBLKL	Small block location code. There are three possible locations for the small blocks: 1) a small block may be placed in the lowest numbered host block and the highest numbered host blocks, 2) a small block may be placed in the lowest numbered host block and the second lowest numbered host block, and 3) a small block may be placed in the second highest numbered host block and the highest numbered host block. 00 = unused 01 = small blocks are part of the two highest numbered blocks of the UC3F array 10 = small blocks are part of the two lowest numbered blocks of the UC3F array 11 = small blocks are part of the lowest and highest numbered blocks of the UC3F array
23:31	FLASHID	Flash module identification code. The FLASHID value is assigned by Motorola and used internally for tracking purposes. The FLASHID field is read only and writes have no effect.

20.3.4 UC3F EEPROM High Voltage Control Register (UC3FCTL)

The UC3F EEPROM high voltage control register is used to control the program and erase operations of the UC3F EEPROM module.

UC3FCTL— UC3F EEPROM High Voltage Control Register **0x2F C808**
0x2F C848

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HVS	PEGOOD	PEFI	EPEE	B0EM	Reserved									SBBLOCK	
HRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
BLOCK								0	CSC	Reserved		HSUS	PE	SES	EHV
HRESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 20-5 UC3FCTL Bit Descriptions

Bit(s)	Name	Description
0	HVS	High voltage status. The HVS bit is for status only, and writes to HVS have no effect. During a program or erase operation, HVS is set (HVS = 1) to indicate when high voltage operations are in progress. The HVS bit will negate itself when the program or erase operation completes successfully, EHV negates during program or erase to terminate the program/erase operation, HSUS is asserted to suspend the program/erase operation, resetting the module, or the internal hardware program/erase controller times out. 0 = no program or erase of the UC3F array or shadow information or CENSOR bits in progress 1 = program or erase of the UC3F array or shadow information or CENSOR bits in progress
1	PEGOOD	Program/erase operation result. The PEGOOD bit is for status only. At the completion of a program or erase operation using the embedded hardware algorithm, the hardware algorithm will change the state of the PEGOOD bit to reflect whether or not the program or erase operation was successful. The PEGOOD bit is only valid after the hardware program erase algorithm has cleared HVS. PEGOOD is reset when either EHV is asserted or SES is cleared. See **Figure 20-2** for a timing diagram of when PEGOOD is valid. 0 = program or erase operation failed 1 = program or erase operation was successful
2	PEFI	Program/erase fail indicator. The PEFI bit is a status qualifier for the PEGOOD bit and is valid for the same times that PEGOOD is valid. In the event of an erase failure which returns PEGOOD = 0, the PEFI bit provides diagnostic information for the cause of the erase failure. If PEFI = 0, the erase failure occurred during the preprogramming step of the erase operation. If PEFI = 1, the erase failure occurred during the actual erase or APDE steps of the erase operation. In the event of a program failure which returns PEGOOD = 0, the PEFI bit indicates a program failure by reading as a 0. The PEFI bit should never return a 1 for a program failure. NOTE: The PEFI bit is meaningful only while PEGOOD is valid and PEGOOD = 0. PEFI is valid after HVS negates and prior to the assertion of EHV or negation of SES. 0 = program operation failed if PEGOOD = 0 1 = erase operation failed if PEGOOD = 0
3	EPEE	EPEE pin status. The EPEE bit monitors the state of the external program/erase enable (EPEE) input. The UC3F module samples the EPEE input when EHV is asserted and holds that sampled state until EHV is negated. 0 = high voltage operations are not possible 1 = high voltage operations are possible
4	B0EM	Block 0 EPEE pin status. The B0EM bit monitors the state of the Block 0 EPEE, B0EPEE, input. The UC3F module samples the B0EPEE input when EHV is asserted and holds that sampled value until EHV is negated.If B0EM = 1 when EHV is asserted, high voltage operations such as program or erase are enabled for either small block 0 or the lowest numbered block of the UC3F array regardless of the state of EPEE. If B0EM = 0 when EHV is asserted, high voltage operations are disabled for small block 0 or the lowest numbered block of the UC3F array regardless of the state of EPEE. 0 = high voltage operations are not possible for block 0 or lowest numbered block 1 = high voltage operations are possible for block 0 or lowest numbered block.
5:13	—	**Reserved**
14:15	SBBLOCK	Small block block program and erase select. The SBBLOCK bits are write-protected by the SES bit. SBBLOCK selects the UC3F EEPROM small array blocks for program and erase operation. When programming, only those blocks intended to be enabled for programming should have their corresponding BLOCK[M] or SBBLOCK[M] bit set. 0 = small block M is not selected for program or erase 1 = small Block M is selected for program or erase

Table 20-5 UC3FCTL Bit Descriptions (Continued)

Bit(s)	Name	Description
16:23	BLOCK	Block program and erase select. The BLOCK bits are write protected by the SES bit. BLOCK selects the UC3F EEPROM array blocks for program and erase operation. All the blocks may be selected for program or erase operation at once. The UC3F EEPROM configuration along with BLOCK determine which array blocks that may be programmed. The UC3F EEPROM array blocks that are enabled to be programmed by the program operation are the blocks whose corresponding BLOCK bit is set to 1. For example, if array blocks 2 and 5 are enabled for programming, BLOCK[2] and BLOCK[5] must be set to 1 while BLOCK[0], BLOCK[1], BLOCK[3], BLOCK[4], BLOCK[6], and BLOCK[7] are set to 0. The UC3F EEPROM configuration along with BLOCK determine the blocks that will be erased simultaneously. All array blocks whose corresponding BLOCK bits are set will be erased during the erase operation. For example, if BLOCK = 00100111, then array blocks 2, 5, 6, and 7 get erased when an erase operation is performed. 0 = array block M is not selected for program or erase 1 = array block M is selected for program or erase
24	—	Reserved
25	CSC	Censor set or clear. The CSC bit is write protected by the SES bit. CSC configures the UC3F EEPROM for setting or clearing CENSOR. If CSC = 1 then CENSOR is configured for setting if PE = 0 or clearing if PE = 1. When the CSC bit is set, the following bits in the UC3FMCR register are write-locked: $\overline{\text{LOCK}}$, FIC, ACCESS, SUPV, DATA, and PROTECT. 0 = configure for normal operation 1 = configure to set or clear the CENSOR bits
26:27	—	Reserved
28	HSUS	Program/erase suspend. Setting the HSUS bit during an embedded hardware algorithm program or erase operation will force the UC3F EEPROM to suspend the current program or erase. The UC3F EEPROM will maintain all information necessary to resume the suspended operation. Array reads are possible while HSUS = 1. However, array reads must be done to locations that are not being affected by the program/erase operation that is currently being suspended. The UC3F EEPROM will NOT prevent read accesses to those locations. Reads to those locations will result in UNKNOWN data. Writes to the HSUS bit only have effect while EHV = 1. The HSUS bit is write locked by EHV = 0. 0 = hardware program/erase behaves normally 1 = any current hardware program/erase is suspended
29	PE	Program or erase select. The PE bit is write protected by the SES bit. PE configures the UC3F EEPROM for programming or erasing. When PE = 0, the array is configured for programming and if SES = 1 the SIE bit will be write locked. When PE = 1, the array is configured for erasing and SES will not write lock the SIE bit. 0 = configure for program operation 1 = configure for erase operation

Table 20-5 UC3FCTL Bit Descriptions (Continued)

Bit(s)	Name	Description
30	SES	Start-end program or erase sequence. The SES bit is write protected by the STOP, HVS, and EHV bits. The SES bit is used to signal the start and end of a program or erase sequence. At the start of a program or erase sequence, SES is set (written to a 1). This will lock STOP, PROTEC, SBPROTECT, BLOCK, SBBLOCK, SBEN, CSC, and PE. If PE = 0 and SES = 1, SIE will be write locked. At this point, the UC3F EEPROM is ready to receive either the programming writes or the erase interlock write. NOTE: The erase interlock write is a write to any UC3F EEPROM array location after SES is set and PE = 1. If PE = 0 and SES = 1, writes to the UC3F array are programming writes. The first programming write sets the address of the location to be programmed, and the data written is captured into the program data latch for programming into the UC3F array. All programming writes after the first programming write update the program data latch but do not change the address to be programmed. At the end of the program or erase operation, the SES bit must be cleared (written to a 0) to return to normal operation and release the STOP, PROTECT, SBPROTECT, BLOCK, SBBLOCK, CSC, SBEN, and PE bits. 0 = UC3F EEPROM not configured for program or erase operation 1 = configure UC3F EEPROM for program or erase operation
31	EHV	Enable high voltage. EHV can be asserted only after the SES bit has been asserted and a valid programming write(s) or erase hardware interlock write has occurred. If an attempt is made to assert EHV when SES is negated, or if a valid programming write or erase hardware interlock write has not occurred since SES was asserted, EHV will remain negated. The external program or erase enable pin (EPEE) and EHV are used to control the application of the program or erase voltage to the UC3F EEPROM module. High voltage operations to the UC3F EEPROM array, special shadow locations or FLASH NVM registers can occur only if EHV = 1 and EPEE = 1. Only after the correct hardware and software interlocks have been applied to the UC3F EEPROM can EHV be set. Once EHV is set, SES cannot be changed and attempts to read the array will not be acknowledged. Clearing EHV during a program or erase operation will safely terminate the high voltage operation. If EHV is cleared while using the embedded hardware program/erase algorithm, the program/erase routine will abort the operation and exit normally. 0 = program or erase pulse disabled 1 = program or erase pulse enabled

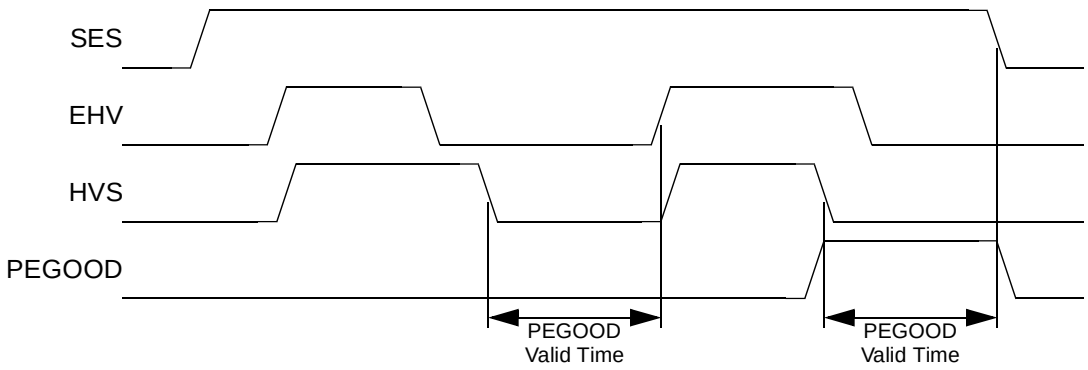

Figure 20-2 PEGOOD Valid Time

20.3.5 UC3F EEPROM Array Addressing

The mapping of the array in the MCU is determined by the address decoder in the BIU. The UC3F array is divided into a maximum of eight blocks, 64 Kbytes in size, which may be independently erased. Two blocks are host to a 16-Kbyte small block.

Seventeen bits of address are used to decode locations in the UC3F array. The read control logic in the UC3F EEPROM module decodes the upper 14 bits of that address to determine if the desired data is currently stored in one of the two read page buffers. If the data is already present in one of the two read page buffers, a read operation is not completed to the UC3F array core, and 64 bits of data are transferred from the appropriate read page buffer to the BIU. This type of array read access is an on-page read.

In the event that the read control logic determines that the desired data is not contained within one of the read page buffers, a read access to the UC3F array core is completed and 32 bytes of data are transferred from the array core. Only the addressed 64 bits of data will be transferred to the BIU. This type of array read access is an off-page read. The BIU contains logic to implement the read page buffer update and replacement scheme to transfer the 32 bytes of data into the appropriate read page buffer. If the read page update and replacement scheme contains a random access mode that does not update the read page buffers, the 32 bytes of data retrieved from the UC3F array core will not be transferred into either read page buffer. The BIU is expected to contain page update logic for controlling the updating of the read page buffers.

Write accesses to the UC3F array have no effect except during program and erase operation.

20.3.6 UC3F EEPROM Shadow Row

The UC3F EEPROM module contains a special shadow row that is used to hold reset configuration data and user data. See figure **Figure 20-3**.

The shadow row is accessed by setting SIE = 1 and performing normal array accesses. Upon transitioning SIE (a 1-to-0 or 0-to-1 transition), the read page match decode circuit is reset so that the next array access is an off-page access.

The shadow row contains 512 bytes which are addressed for read accesses using the low order row and read page addresses.

The shadow row is implemented in the lowest numbered block of the array. In the case of a UC3F array configuration which also has a small block in the lowest numbered block of the array, the shadow row is contained in the small block. If SBEN[0] = 1 in this array configuration, the shadow row is treated as part of small block 0. SBPROTECT[0] and SBBLOCK[0] are used to control program and erase operation of the shadow row. If SBEN[0] = 0 in this array configuration, the shadow row is treated as part of the host block. The corresponding PROTECT and BLOCK bits are used to control program and erase operation of the shadow row.

NOTE

A shadow row can not be read if the program code is executing from the same module of the MPC565 / MPC566. (i.e., If a program is executing from one flash module), it can only read the shadow row of the other flash module, for example a program running from module UC3F_A can read the shadow row of the UC3F_B module.

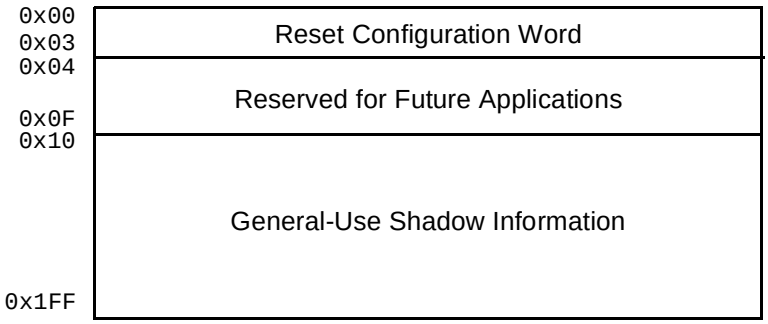

Figure 20-3 Shadow Information

20.3.6.1 Reset Configuration Word (UC3FCFIG)

The UC3F EEPROM reset configuration word is implemented in the first word (ADDR[23:29] = 0x00) of the special shadow locations. The reset configuration word along with the rest of the shadow information words is located in supervisor data address space. The purpose of the reset configuration word is to provide the system with an alternative internal source for the reset configuration.

Note that with the exception of bit 20, the bits in the UC3FCFIG are identical to those in the USIU hard reset configuration word.

UC3FCFIG — Hard Reset Configuration Word

MSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EARB	IP	BDRV	BDIS	BPS[0:1]		Reserved			DBGC[0:1]		DBPC	ATWC	EBDF[0:1]		Re-served
Reset															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LSB

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
PRPM	SC		ETRE	$\overline{HC}$	EN_COMP[1]	EXC_COMP[1]	Re-served	OERC		RESERVED		ISB			DME
Reset															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTES:
1. Available only on the MPC566.

Table 20-6 RCW Bit Descriptions

Bit(s)	Name	Description
0	EARB	External Arbitration — Refer to **9.5.6 Arbitration Phase** for a detailed description of Bus arbitration. The default value is that internal arbitration hardware is used. 0 = Internal arbitration is performed 1 = External arbitration is assumed
1	IP	Initial Interrupt Prefix — This bit defines the initial value of the MSR_{IP} immediately after reset. The MSR_{IP} bit defines the Interrupt Table location. If IP is zero then the MSR_{IP} initial value is zero, If the IP is one, then the MSR_{IP} initial value is one. Default value is zero. See **Table 3-12** for more information. 0 = MSR[IP] = 0 after reset 1 = MSR[IP] = 1 after reset
2	BDRV	Bus Pins Drive Strength — This bit determines the bus pins (address, data and control) driving capability to be either full or reduced drive. The bus default drive strength is full; Upon default, it also effects the CLKOUT drive strength to be full. See **Table 6-7** for more information. BDRV controls the default state of COM[1] in the SIUMCR. 0 = Full drive 1 = Reduced drive
3	BDIS	Boot Disable — If the BDIS bit is set, then memory controller is not activated after reset. If it is cleared then the memory controller bank 0 is active immediately after reset such that it matches any addresses. If a write to the OR0 register occurs after reset this bit definition is ignored. The default value is that the memory controller is enabled to control the boot with the $\overline{CS}0$ pin. See **10.4 Global (Boot) Chip-Select Operation** for more information. 0 = Memory controller bank 0 is active and matches all addresses immediately after reset 1 = Memory controller is not activated after reset.
4:5	BPS	Boot Port Size — This field defines the port size of the boot device on reset (BR0[PS]). If a write to the OR0 register occurs after reset this field definition is ignored. See**Table 10-3** and **Table 10-7** for more information. 00 = 32-bit port (default) 01 = 8-bit port 10 = 16-bit port 11 = Reserved
6:8	—	Reserved. This bit must not be high in the reset configuration word.
9:10	DBGC[0:1]	Debug Pins Configuration — See **6.14.1.1 SIU Module Configuration Register (SIUMCR)** for this field definition. The default value is that these pins function as: VFLS[0:1], $\overline{BI}$, $\overline{BR}$, $\overline{BG}$ and $\overline{BB}$. See **Table 6-8**.
11	DBPC	Debug Port Pins Configuration — The default value is that these pins function as the debug port pins for development support. See **Table 6-9**.
12	ATWC	Address Type Write Enable Configuration — The default value is that these pins function as $\overline{WE}$ pins. 0 = $\overline{WE}$[0:3]/$\overline{BE}$[0:3]/AT[0:3] functions as $\overline{WE}$[0:3]/$\overline{BE}$[0:3] 1 = $\overline{WE}$[0:3]/$\overline{BE}$[0:3]/AT[0:3] functions as AT[0:3] See **Table 6-7**.
13:14	EBDF	External Bus Division Factor — This field defines the initial value of the external bus frequency. The default value is that CLKOUT frequency is equal to that of the internal clock (no division). See **Table 8-9**.
15	—	Reserved. This bit must not be high in the reset configuration word.
16	PRPM	Peripheral Mode Enable — This bit determines if the chip is in peripheral mode. A detailed description is in **Table 6-14** The default value is no peripheral mode enabled.
17:18	SC	Single Chip Select — This field defines the mode of the MPC565 / MPC566. 00 = Extended chip, 32 bits data 01 = Extended chip, 16 bits data 10 = Single chip and show cycles (address) 11 = Single chip See **Table 6-11**.

Table 20-6 RCW Bit Descriptions (Continued)

Bit(s)	Name	Description
19	ETRE	Exception Table Relocation Enable — This field defines whether the Exception Table Relocation feature in the BBC is enabled or disabled; The default state for this field is disabled. For more details, see **Table 4-4**.
20	$\overline{HC}$	$\overline{Has\ Configuration}$ — During reset the $\overline{HC}$ bit ("has configuration," bit 20) and the USIU configure the UC3F EEPROM module to provide UC3FCFIG. If $\overline{HC}$ = 0 and the USIU requests internal configuration during reset the reset configuration word will be provided by UC3FCFIG Unlike the MPC555, the flash reset configuration word can come from either the UC3F_A or the UC3F_B module. See **7.5.2 Hard Reset Configuration Word** for additional information..
21	EN_COMP[1]	Enable Compression — This bit enables the operation of the MPC566 with compressed code. The default state is disabled. See **Table 4-4**.
22	EXC_COMP[1]	Exception Compression — This bit determines the operation of the MPC566 with exceptions. If this bit is set, than the MPC566 assumes that ALL the exception routines are in compressed code. The default indicates the exceptions are all non-compressed. See **Table 4-4**.
23	—	Reserved. This bit must not be high in the reset configuration word.
24:25	OERC	Other Exceptions Relocation Control — These bits effect only if ETRE was enabled. Relocation offset: 00 = Offset 0 01 = Offset 64 KB 10 = Offset 512 KB 11 = Offset to 0x003 FE000 (SRAM start address) See **Table 4-2**.
26:27	—	Reserved
28:30	ISB	Internal Space Base Select — This field defines the initial value of the ISB field in the IMMR register. A detailed description is in **Table 6-13**. The default state is that the internal memory map is mapped to start at address 0x0000_0000 hex. This bit must not be high in the reset configuration word.
31	DME	Dual Mapping Enable — This bit determines whether Dual mapping of the internal flash is enabled. For a detailed description refer to **Table 10-9**. The default state is that dual mapping is disabled. 0 = Dual mapping disabled 1 = Dual mapping enabled

NOTES:
1. This bit is available only on the MPC556.

The default reset state of the UC3FCFIG after an erase operation of the UC3F module A block 0 is no configuration word available ($\overline{HC}$ = 1).

20.3.7 UC3F EEPROM 512-Kbyte Array Configuration

The MPC565 / MPC566 contains only the 512-Kbyte array configuration of the UC3F module, as shown in **Figure 20-4**. The blue shaded blocks in the array configuration diagram indicate the location of the shadow row.

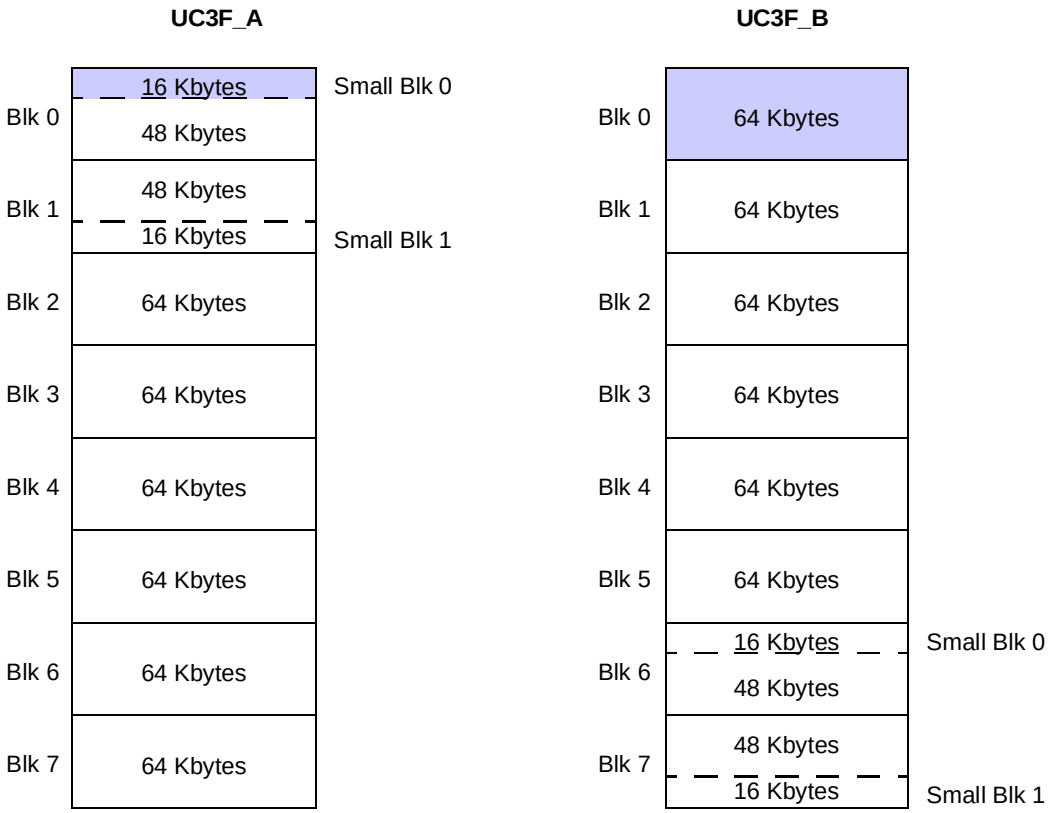

Figure 20-4 512-Kbyte Array Configurations

20.4 Operation

The following sections describe the operation of the UC3F EEPROM during various operational modes. The primary function of the UC3F EEPROM module is to serve as electrically erasable and programmable non-volatile memory for embedded application in microcontrollers.

20.4.1 Reset

The device shall signal a reset to the UC3F EEPROM by asserting the reset signal. A reset is the highest priority operation for the UC3F EEPROM and terminates all other operations. The UC3F EEPROM module uses reset to initialize register bits to their default reset value. If the UC3F EEPROM is in program or erase operation (EHV = 1 and SES = 1) and a reset is issued, the module will perform the needed interlocks to disable the high voltage without damage to the high voltage circuits. Reset terminates any other mode of operation and forces the UC3F EEPROM module to a state ready to receive accesses.

Upon power up and power down periods, it is assumed that the reset signal is asserted to prevent accidental program/erase disturb of the UC3F array.

20.4.2 Register Read and Write Operation

The UC3F EEPROM control registers are accessible for read or write operation at all times while the device is powered up and enabled except during reset.

20.4.3 Array Read Operation

The UC3F EEPROM array is available for read operation under most conditions while the device is powered up. Reads of the array are not allowed during reset, when in information or cleared censorship with ACCESS = 0, while the UC3F EEPROM is disabled (see section **20.4.10 Disabled** for more information on disabling the UC3F EEPROM), while the UC3F EEPROM is in STOP mode (see section **20.4.9 Stop Operation** for more information on STOP mode), or while high voltage is applied to the array during program and erase operation (HVS = 1 or EHV = 1 and not suspended). The UC3F array may be configured into a page mode access memory by setting the BPB bit in the UC3FMCR register, see **20.3.2 UC3F EEPROM Configuration Register (UC3FMCR)**.

When in page mode operation, the address of an incoming read access is compared to the address for which data is currently held in the read page buffers. If the data corresponding to the read address is currently held in one of the two read page buffers, the data is fetched from the appropriate read page buffer. A data fetch from a read page buffer is an on-page read operation **20.4.3.1 Array On-Page Read Operation**. If the data is not contained in one of the read page buffers, 32 bytes of information is fetched from the UC3F array, and the addressed data is driven onto the data bus. A data fetch from the UC3F array is an off-page read operation.

NOTE

After setting/clearing HSUS, reset, programming writes, erase interlock write, setting EHV, clearing SES or setting/clearing SIE, the page buffers may not contain valid information and the UC3F page match logic negates uc3f_onpage[0:1] to force an off page read before an on page read can be accomplished to ensure data coherency.

For information regarding how the two read page buffers in the UC3F EEPROM are associated to array blocks, refer to **20.3.5 UC3F EEPROM Array Addressing**.

The UC3F module is configured as a page mode memory. The UC3F module uses an internal address comparator to monitor incoming addresses to determine if the addressed information is stored in a read page buffer. When the address comparator determines that the requested information is not stored in a read page buffer, an array off-page read operation retrieves 32 bytes of data from the flash array and transfers the addressed data to the data bus.

In the MPC565 / MPC566, each UC3F module contains two 32-byte read page buffers. On module UC3F_A, these read page buffers contain the two most recently loaded off-page accessed instruction fetches. On module UC3F_B, one buffer is dedicated to the most recently accessed instruction fetches and the other read page buffer is dedicated to the most recently loaded data access.

20.4.3.1 Array On-Page Read Operation

An internal address comparator is used to determine if addressed information is stored in a read page buffer. If the address of a read access matches data contained in a read page buffer, that addressed data is transferred from the read page buffer to the data bus. An off-page read access to transfer data from the flash array to the data bus is not performed in this case.

20.4.4 Shadow Row Select Read Operation

The normal array is accessed when the SIE register bit in the UC3FMCR = 0. When SIE = 1, reads to the array access the shadow information row.

20.4.5 Array Program/Erase Interlock Write Operation

The only valid writes to the UC3F array are program or erase interlock writes. In the case of program interlock writes, the address of the write determines the location to be programmed while the data written is transferred to the program data latches to be programmed into the array. Address and data written during an erase interlock write is a “don’t care” and is not stored anywhere.

20.4.6 High Voltage Operations

There are two fundamental high voltage operations, program and erase. Program changes a UC3F array bitcell from a logic 1 state to a logic 0 state and is a selective operation performed on up to 32 bits at a time. Erase changes a UC3F array bitcell from a logic 0 state to a logic 1 state and is a bulk operation performed on one block or multiple blocks of the UC3F array.

20.4.6.1 Overview of Program/Erase Operation

The embedded hardware program/erase algorithm relies on an internal state controller to perform the program and erase sequences. The embedded hardware algorithm uses an internal oscillator to control the high voltage pulse duration and hardware control logic. The embedded hardware algorithm is also responsible for performing all margin reads and applying high voltage pulses to ensure each bit is programmed or erased with sufficient margin. Upon successful program or erase operation, the program/erase hardware control logic terminates the program or erase operation with a pass status (PEGOOD = 1). The program/erase control logic will time out in the event that the maximum program or erase time is exceeded and return a fail status (PEGOOD = 0).

20.4.7 Programming

To modify the charge stored in an isolated element of the UC3F bit from a logic 1 state to a logic 0 state, a programming operation is required. This programming operation shall apply the required voltages to change the charge state of the selected bits without changing the logic state of any other bits in the UC3F array. The program operation cannot change the logic 0 state to a logic 1 state; this transition must be done by the erase operation. Programming uses a program data latch to store the data to be pro-

grammed and an address latch to store the word address to be programmed. The UC3F Array may be programmed by byte (8 bits), half-word (16 bits), or word (32 bits).

Blocks of the UC3F EEPROM that are protected (PROTECT[M] = 1, SBEN[N] = 1 and SBPROTECT[N] = 1) will not be programmed. Also, if EPEE = 0, no programming voltages will be applied to the array. If B0EPEE = 0, no programming voltages will be applied to block 0 or small block 0 depending on the state of SBEN[0] and the configuration of the array.

In the event of UC3F module configurations which do not contain a block 0, the lowest numbered block is protected by B0EPEE. Also, if the lowest numbered block does not host small block 0, then no small blocks can be protected by B0EPEE.

20.4.7.1 Program Sequence

The UC3F EEPROM module requires a sequence of writes to the high voltage control register (UC3FCTL) and to the program data latch in order to enable the high voltage to the array or shadow information for program operation. The required hardware program sequence follows.

1. Write PROTECT[0:7] and SBPROTECT[0:1] to disable protection on blocks to be programmed.
2. Write BLOCK[0:7] and SBBLOCK[0:1] to select the array blocks to be programmed, SES = 1 and PE = 0 in the UC3FCTL register.

NOTE

BLOCK[0:7] and SBBLOCK[0:1] in conjunction with SBEN[0:1] determine which blocks/small blocks in the array are enabled for programming operation. Just because a BLOCK or SBBLOCK bit is enabled (set to 1), no programming can occur in the corresponding block/small block unless the programming operation specifically targets an address location within that block/small block to program. If BLOCK or SBBLOCK is not set to 1, no address locations in that corresponding block or small block can be programmed.

3. Programming write — A successful write to the array location to be programmed. This write shall update the program data latch with the information to be programmed. In addition, the address, uc3f_addr[0:16], of the first programming write is latched in the UC3F memory interface block. All access of the array after the first write shall be to the same address regardless of the address provided. Thus the locations accessed after the first programming write are limited to the location to be programmed. The last write to the program data latch shall be saved for programming.

NOTE

If a byte of the program data latch has not received a programming write, no programming voltages will be applied to the corresponding byte in the array. Once EHV has been set, writes to the program data latch are disabled until EHV is cleared to 0.

4. Write EHV = 1 in the UC3FCTL register.

NOTE

The values of the EPEE and B0EPEE inputs are latched with the assertion of EHV to determine the array protection state for the program operation. It is assumed that the EPEE and B0EPEE inputs are setup prior to the assertion of EHV.

5. Read the UC3FCTL register until HVS = 0.
6. Read the UC3FCTL, confirm PEGOOD = 1.
7. Write EHV = 0.

WARNING

Writing EHV = 0 before HVS = 0 causes the current program sequence to ABORT. The location for which the program sequence was aborted may not have been programmed with sufficient margins. The block containing that location must be erased and reprogrammed before that block of the UC3F array may be used reliably.

8. If more information needs to be programmed go to step 3.
9. Write SES = 0 in the UC3FCTL register.

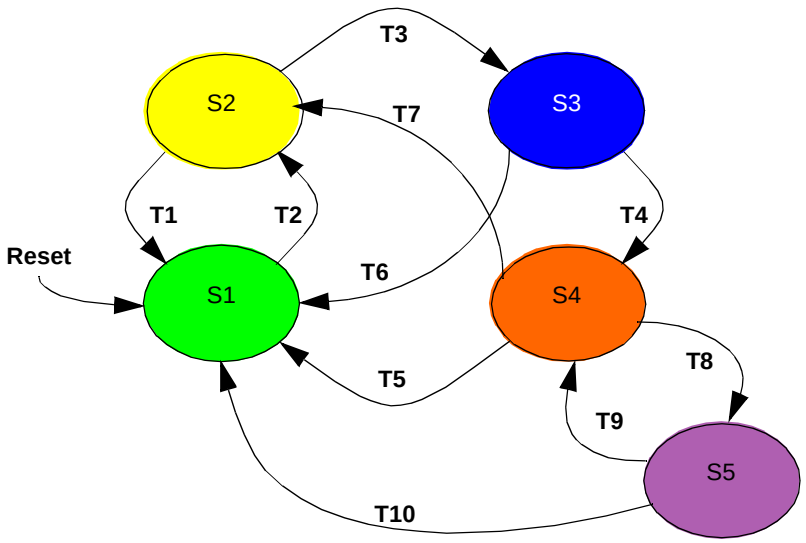

Figure 20-5 Program State Diagram

Table 20-7 Program Interlock State Descriptions

State	Mode	Next State	Transition Requirement	
S1	Normal Operation: Normal array reads and register accesses. The block protect information can be modified.	S2	T2	Write PE = 0, SES = 1.
S2	First Program Hardware Interlock Write: Normal read operation still occurs. The array will accept programming writes. Accesses to the registers are normal register accesses. A write to UC3FCTL can not change EHV at this time. If the write is to a register no data will be stored in the program data latch and the UC3F shall remain in state S2.	S1	T1	Write SES = 0 or a reset.
		S3	T3	Hardware Interlock A successful write to any UC3F array location. This programming write will latch the selected word of data into the program data latch and the address shall be latched to select the location that will be programmed. Once a bit has been written then it shall remain in the program data latch until another write over-writes that data or a write of SES = 0. If the write is to a register no data will be stored in the program data latch and the UC3F shall remain in state S2.
S3	Expanded Program Hardware Interlock Operation: Programming writes are accepted so that data may be programmed. These writes may be to any UC3F array location. The location to be programmed is determined from the address initially written to on the first program interlock write. The program data latch may be updated on any program interlock writes which occur in this state. Accesses to the registers are normal register accesses. A write to UC3FCTL can change EHV. If the write is to a register no data will be stored in the program data latch.	S1	T6	Write SES = 0 or a reset.
		S4	T4	Write EHV = 1.
S4	Program Operation: High voltage is applied to the array or shadow information to program the UC3F bit cells, and program margin reads are automatically performed by the internal program control logic. No further programming writes will be accepted. During programming, the array will not respond to any access. Accesses to the registers are allowed. A write to UC3FCTL can change EHV or HSUS only.	S1	T5	Reset.
		S2	T7	Write EHV = 0.
		S5	T8	Write HSUS = 1 or disable the UC3F module.
S5	Program Suspend Operation: The program operation is suspended to either read the array or disable the module. Once HVS reads as a 0, the program operation is suspended. Normal reads to the array can be performed if the module is enabled; read accesses to the location being programmed returns indeterminate data.	S1	T10	Reset.
		S4	T9	Write HSUS = 0 or re-enable the UC3F module.

20.4.7.2 Program Shadow Information

Programming the shadow information uses the same procedure as programming the array except that SIE must be set to a 1 prior to initiating the programming sequence. Only the lower most addresses are used to encode which words get programmed in the shadow row. the shadow information is physically located in lowest numbered block and will also be located in small block 0 if the lowest numbered block hosts a small block in the implemented configuration.

20.4.7.3 Program Suspend

The program operation may be suspended to allow read accesses to the array. Setting the HSUS bit in the UC3FCTL to a 1 while PE = 0, EHV = 1, and HVS = 1 forces the array into a program suspend state. The deassertion of the HVS bit (HVS = 0) signifies that the program operation has been successfully suspended. The HVS bit should negate within 10µs of asserting the HSUS bit.

While in program suspend mode, normal read accesses may be performed to the UC3F array or shadow information words. Reads to the array location targeted for program return indeterminate data since only a partial programming operation may have been performed.

The program operation may be resumed by setting HSUS = 0.

NOTE

Repeated suspending of a program operation to fetch array contents may extend the program operation. The internal program hardware may only resume the program operation at predefined steps of the internal program hardware sequence; interrupting the program operation on a high frequency basis may cause the internal program hardware to delay completion of the current step and delay advancement to the next step of the internal program hardware sequence.

20.4.8 Erasing

To modify the charge stored in an isolated element of the UC3F bit from a logic 0 state to a logic 1 state, an erase operation is required. In the UC3F EEPROM, erase is a bulk operation that shall affect the stored charge of all the isolated elements in an array block. To make the UC3F module block-erasable, the array is divided into blocks that are physically isolated from each other. Each of the array blocks may be erased in isolation or in any combination. The UC3F array block size is fixed for all blocks in the module at 64 Kbytes and the module is comprised of eight blocks. Two of these blocks may be further subdivided into two small blocks. Array blocks of the UC3F EEPROM that are protected (PROTECT[M] = 1 or (SBEN[M] = 1 & SBPROTECT[M] = 1)) will not be erased. Also, if EPEE = 0 or B0EPEE = 0, no erase voltages will be applied to the array or the block corresponding to block 0 (or lowest numbered block if no block 0 exists) or small block 0 (assuming that the lowest numbered block contains small block 0) if SBEN[0] = 1.

The embedded program/erase algorithm first preprograms all bits in blocks selected for erase prior to actually erasing the selected blocks.

The array blocks selected for erase operation are determined by BLOCK[0:7], SBBLOCK[0:1] in conjunction with SBEN[0:1], and the array configuration. If multiple blocks are selected for erase, the embedded erase hardware algorithm serially erases each array block until all of the selected blocks are erased. For instance, if BLOCK[0:7] = 0x78 and SBEN[0:1] = 0b00, then blocks 1, 2, 3, and 4 are selected for erase. The embedded erase hardware algorithm first erases block 1 and then erases block 2 followed by blocks 3 and 4. The total erase time for this example is the block erase time, T_{ERASE}, multiplied by four since four blocks are erased. In addition, the preprogramming time to program all locations in blocks 1, 2, 3, and 4 to a “0” state needs to be considered when determining the total erase time. The preprogramming time is dependent on the data already stored in the flash array before beginning the erase operation.

20.4.8.1 Erase Sequence

The UC3F EEPROM module requires a sequence of writes to the high voltage control register (UC3FCTL) and an erase interlock write in order to enable high voltage to the array and shadow information for erase operation. The required hardware algorithm erase sequence follows.

1. Write PROTECT[0:7] and SBPROTECT[0:1] to disable protect for the blocks to be erased.
2. Write BLOCK[0:7] and SBBLOCK[0:1] to select the blocks to be erased, PE = 1 and SES = 1 in the UC3FCTL register.

NOTE

BLOCK[0:7] and SBBLOCK[0:1] in conjunction with SBEN[0:1] determine which blocks are selected for erase. Blocks whose BLOCK bits or enabled small blocks whose SBBLOCK bits are set (equal to 1) get erased when an erase operation is performed.

3. Execute an erase interlock write to any UC3F array location.
4. Write EHV = 1 in the UC3FCTL register.

NOTE

The values of the EPEE and B0EPEE inputs are latched with the assertion of EHV to determine the array protection state for the erase operation. It is assumed that the EPEE and B0EPEE inputs are setup prior to the assertion of EHV.

5. Read the UC3FCTL register until HVS = 0.

WARNING

Writing EHV = 0 before HVS = 0 causes the current erase sequence to ABORT. All blocks being erased must go through another erase sequence before the UC3F EEPROM can be used reliably.

6. Read the UC3FCTL register. Confirm PEGOOD =1.
7. Write EHV = 0 in the UC3FCTL register.
8. Write SES =0 in the UC3FCTL register.

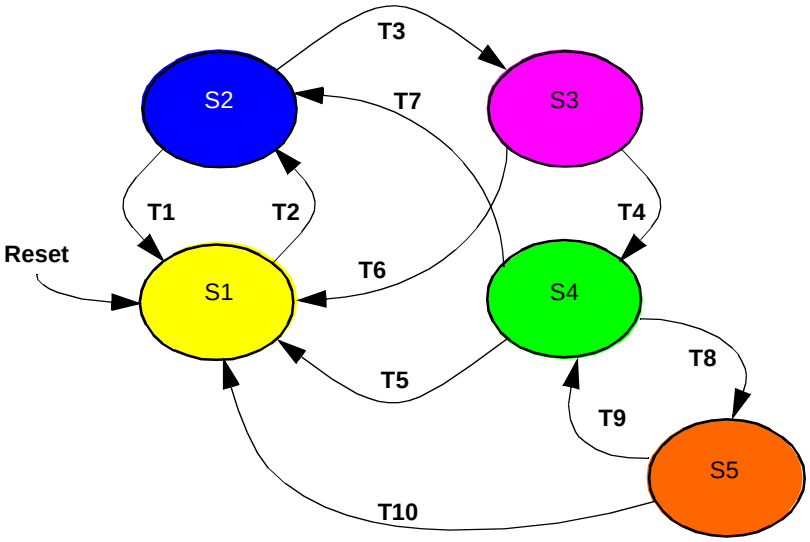

Figure 20-6 Erase State Diagram

Table 20-8 Erase Interlock State Descriptions

State	Mode	Next State	Transition Requirement	
S1	Normal Operation: Normal array reads and register accesses. The Block protect information can be modified.	S2	T2	Write PE = 1, SES = 1.
S2	Erase Hardware Interlock Write: Normal read operation still occurs. The UC3F will accept the erase hardware interlock write. This write may be to any UC3F array location. Accesses to the registers are normal register accesses. A write to UC3FCTL can not set EHV at this time. A write to the register is not an erase hardware interlock write and the UC3F shall remain in state S2.	S1	T1	Write SES = 0 or a reset.
		S3	T3	Hardware Interlock A successful write to any UC3F array location is the erase interlock write. If the write is to a register the erase hardware interlock write has not been done and the UC3F shall remain in state S2.
S3	High voltage write enable Accesses to the registers are normal register accesses. A write to UC3FCTL can change SES or EHV.	S1	T6	Write SES = 0 or a reset.
		S4	T4	Write EHV = 1.

Table 20-8 Erase Interlock State Descriptions (Continued)

State	Mode	Next State	Transition Requirement	
S4	Erase Operation: High voltage is applied to the array blocks to erase the UC3F bit cells, and erase margin reads are automatically performed by the embedded erase control logic. During erase the array will not respond to any address. Accesses to the registers are allowed. A write to UC3FCTL can change EHV or HSUS only.	S1	T5	Reset.
		S2	T7	Write EHV = 0.
		S5	T8	Write HSUS = 1 or disable the UC3F module.
S5	Erase Suspend Operation: The erase operation is suspended to either read the array or disable the module. Once HVS reads as a 0, the erase operation is suspended. Normal reads to the array can be performed if the module is enabled; read accesses to locations in blocks being erased return indeterminate data.	S1	T10	Reset.
		S4	T9	Write HSUS = 0 or re-enable the UC3F module.

20.4.8.2 Erasing Shadow Information Words

The shadow information words are erased with either the lowest numbered block or small block 0, depending on the array configuration and the state of SBEN[0]. If the lowest numbered block in the array does not host a small block, then the shadow information words are erased with the lowest numbered block. If the lowest numbered block hosts a small block, then the shadow information words may get erased with small block 0. If SBEN[0] = 0 for this array configuration, then the shadow information words get erased with the lowest numbered block. If SBEN[0] = 1 for this same array configuration, then the shadow information words get erased with small block 0 only.

20.4.8.3 Erase Suspend

The erase operation may be suspended to allow read accesses to the array. Setting the HSUS bit in the UC3FCTL to a 1 while EHV=1 and HVS=1 forces the array into an erase suspend state. The deassertion of the HVS bit (HVS = 0) signifies that the erase operation has been successfully suspended. The HVS bit should negate within 10 ms of asserting the HSUS bit.

While in erase suspend mode, normal read accesses may be performed to the UC3F array or shadow information words. Reads to the array block or blocks targeted for erase return indeterminate data since only a partial erase operation has been performed.

The erase operation may be resumed by setting HSUS = 0.

NOTE

Repeated suspending of an erase operation to fetch array contents may severely extend the erase operation. The internal erase hardware may only resume the erase operation at predefined steps of the internal erase hardware sequence; interrupting the erase operation on a high frequency basis may cause the internal erase hardware to delay completion of the current step and delay advancement to the next step of the internal erase hardware sequence.

20.4.9 Stop Operation

The UC3F EEPROM goes into a low power operation, or stop operation, while STOP = 1. When the STOP bit is set, only the control registers can be accessed on the UC3F EEPROM module. The UC3F EEPROM array may not be programmed, erased or read while STOP = 1.

With STOP = 1, the UC3F module enters a low power state by shutting down internal timers and bias generators. A stop recovery time of 1 µs is required when clearing the STOP bit to exit stop operation. The BIU should allow 1 µs following the negation of the STOP bit so that internal bias generators used by the array may recover to normal levels prior to initiating any UC3F array accesses.

NOTE

The UC3F cannot be stopped while the array is being programmed or erased since the STOP bit is write locked by SES = 1.

20.4.10 Disabled

Both UC3F modules can be disabled by clearing the FLEN bit in the IMMR register (see **6.14 System Configuration and Protection Registers**). While disabled, the UC3F module is completely shut down. The register block and array are not accessible in this mode, and all circuits which draw any DC power are disabled to eliminate power consumption. In addition, each individual module can be disabled by setting the STOP bit in the UC3FMCR register (see **20.3.2 UC3F EEPROM Configuration Register (UC3FMCR)**).

If the UC3F module is disabled while programming or erasing, the HSUS bit in the UC3FCTL register is asserted (HSUS = 1) to suspend the current program or erase operation. When the UC3F module is re-enabled, the suspended program or erase operation may be resumed by writing the HSUS bit to a 0.

NOTE

While there should be no harmful side effects resulting from disabling the UC3F module while in program or erase operation, it is not recommended that program or erase operation be suspended in this manner.

When disabled, the power used by the UC3F is reduced to leakage levels, see Power Supplies Section.

When not disabled, the UC3F module is enabled for accesses. Like recovering from stop operation (STOP = 1), there is a recovery time of one µs for internal biases to recover to operating levels.

20.4.11 Censored Accesses and Non-Censored Accesses

The UC3F EEPROM has a censorship mechanism which provides for several censorship levels. The censorship mechanism is used to increase restrictions in accessing flash data. Four bits in UC3FMCR are used to configure the UC3F censorship level. These bits are:

ACCESS — Enables a UC3F EEPROM to bypass the censorship.

FIC — Overrides CENSOR[0:1] to force information censorship.

CENSOR[0:1] — Determine the censorship level of the UC3F.

The device has two relevant modes used by the UC3F EEPROM to select the type of censorship. The first mode, which is uncensored mode, provides no censorship. In uncensored mode the ACCESS and CENSOR[0:1] bits are irrelevant. The second mode, censored mode, enables the UC3F EEPROM to exercise censorship based on the state of ACCESS, FIC, and CENSOR[0:1]. The device shall authenticate between uncensored mode and censored mode. In censored mode, a UC3F EEPROM may disallow accesses to the array. If censored mode is entered by any means then the UC3F EEPROM will exercise censorship according to the following.

ACCESS	FIC	CENSOR[0:1]	
0	0	11	Information censorship, No UC3F array accesses allowed.
0	0	01 or 10	No censorship, UC3F array accesses allowed.
0	0	00	Cleared censorship, No UC3F array accesses allowed.
0	1	XX	Emulated censorship, UC3F array accesses not allowed.
1	X	XX	No censorship, UC3F array accesses allowed.

While the device remains in the uncensored mode, ACCESS may be set to allow the device to enter censored mode and still access the UC3F array. ACCESS may not be set while the device is in censored mode but may be cleared.

Device Mode	Censored					Uncensored					
ACCESS	0					1		0		1	
FIC	0			1		0	1	0	1	0	1
CENSOR[0:1]	00	01 or 10	11	00, 01 or 10	11	00, 01, 10 or 11					
UC3F EEPROM Status	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11

Indicates that the UC3F array can not be accessed.

1.	ACCESS can not be changed. FIC can be set. UC3F array can not be accessed. CENSOR[0:1] can be set. CENSOR[0:1] can not be cleared.
2.	ACCESS can not be changed. FIC can be set. UC3F array can be accessed. CENSOR[0:1] can be set. CENSOR[0:1] can be cleared.
3.	ACCESS can not be changed. FIC can be set. UC3F array can not be accessed. CENSOR[0:1] can not be cleared unless uc3f_ccmcreiwren = 1.
4.	ACCESS can not be changed. FIC can not be changed. UC3F array can not be accessed. CENSOR[0:1] can be set. CENSOR[0:1] can not be cleared unless uc3f_ccmcreiwren = 1.
5.	ACCESS can not be changed. FIC can not be changed. UC3F array can not be accessed. CENSOR[0:1] can not be cleared unless uc3f_ccmcreiwren = 1.
6.	ACCESS can be cleared. FIC can be set. UC3F array can be accessed. CENSOR[0:1] can be changed.
7.	ACCESS can be cleared. FIC can not be changed. UC3F array can be accessed. CENSOR[0:1] can be changed.
8.	ACCESS can be changed. FIC can be set. UC3F array can be accessed. CENSOR[0:1] can be changed.
9.	ACCESS can be changed. FIC can not be changed. UC3F array can be accessed. CENSOR[0:1] can not be changed unless uc3f_ccmcreiwren = 1.
10.	ACCESS can be changed. FIC can be set. UC3F array can be accessed. CENSOR[0:1] can be changed.
11.	ACCESS can be changed. FIC can not be changed. UC3F array can be accessed. CENSOR[0:1] can be changed.

The only way CENSOR[0:1] can be changed is by setting or clearing the FLASH NVM fuses. In the information censorship state, CENSOR[0:1] must be cleared to the cleared censorship state before CENSOR[0:1] can be put into the no censorship state. While clearing CENSOR[0:1] the entire UC3F array is erased. Thus the information stored in the UC3F array is made invalid while clearing CENSOR[0:1].

20.4.11.1 Setting and Clearing Censor

The value of each bit in CENSOR[0:1] is determined by the state of an NVM CAM cell. The NVM CAM cell is not writable but instead may be set or cleared. Reading CENSOR[0:1] while setting or clearing with the high voltage applied (CSC = 1 and EHV = 1) will return 0's.

20.4.11.2 Setting Censor

The set operation changes the state in an NVM CAM cell from a zero to a one. This set operation can be done without changing the contents of the UC3F array. The required sequence to set one or both of the bits in CENSOR[0:1] follows.

1. Write CSC = 1, PE = 0 and SES = 1 in the UC3FCTL register
2. Write a 1 to the CENSOR bit(s) to be set
3. Write EHV = 1 in the UC3FCTL register
4. Read the UC3FCTL register until HVS = 0
5. Read the UC3FCTL register. Confirm PEGOOD = 1
6. Write EHV = 0 in the UC3FCTL register
7. Write SES = 0 and CSC = 0

20.4.11.3 Clearing Censor

The clear operation changes the state of the CENSOR[0:1] bits from a one to a zero by erasing the CAM cells. This clear operation can be done only while erasing the entire UC3F array and shadow information. The required sequence to clear CENSOR follows.

Clear CENSOR[0:1]

1. Write PROTECT[0:7] = 0x00 to enable the entire array for erase. If SBEN[M] = 1, then SBPROTECT[M] must also be set to 0.
2. Write BLOCK[0:7] = 0xFF, CSC = 1, PE = 1 and SES = 1 in the UC3FCTL register. If SBEN[M] = 1, then SBBLOCK[M] must also be set to 1.
3. Do an erase interlock write.

The erase interlock write is normally defined as a write to any valid array location and is subject to any censorship conditions which might apply.

When the UC3F module interface signal, uc3f_ccmcreiwren, is maintained in a logic 1 state, a write to the UC3FMCR also serves as an erase interlock write for the clear CENSOR operation, in addition to a write to any valid array location. When uc3f_ccmcreiwren = 1, the CENSOR[0:1] bits may always be cleared in the UC3F EEPROM status states #3, #4, #5, #9, and #11, from the above table, in addition to those states (state #1 is already cleared) where writes to the array are valid interlock writes.

When uc3f_ccmcreiwren = 0, only a write to any valid array location serves as the erase interlock write for the clear CENSOR operation.

The erase interlock write is only valid if all blocks of the array are selected for erase and not protected. BLOCK[0:7] and SBBLOCK[0:1] set to 1 in addition to PROTECT[0:7] and SBPROTECT[0:1] set to 0 are required to validate the erase interlock write during the clear censor operation.

4. Write EHV = 1 in the UC3FCTL register.

NOTE

The values of the EPEE and B0EPEE inputs are latched with the assertion of EHV to determine the array protection state for the clear censor operation. It is assumed that the EPEE and B0EPEE inputs are setup prior to the assertion of EHV. If EPEE and B0EPEE are not enabled for erase, the CENSOR[0:1] bits may not be cleared.

5. Read the UC3FCTL register until HVS = 0.
6. Read the UC3FCTL register. Confirm PEGOOD = 1.
7. Write EHV = 0 in the UC3FCTL register.
8. Write SES = 0 and CSC = 0.

20.4.11.4 Switching The UC3F EEPROM Censorship

There are three levels of censorship that CENSOR[0:1] can select. These are: cleared censorship, no censorship (two states) and information censorship. These three levels, state values, transitions and level of censorship are shown in the following diagram.

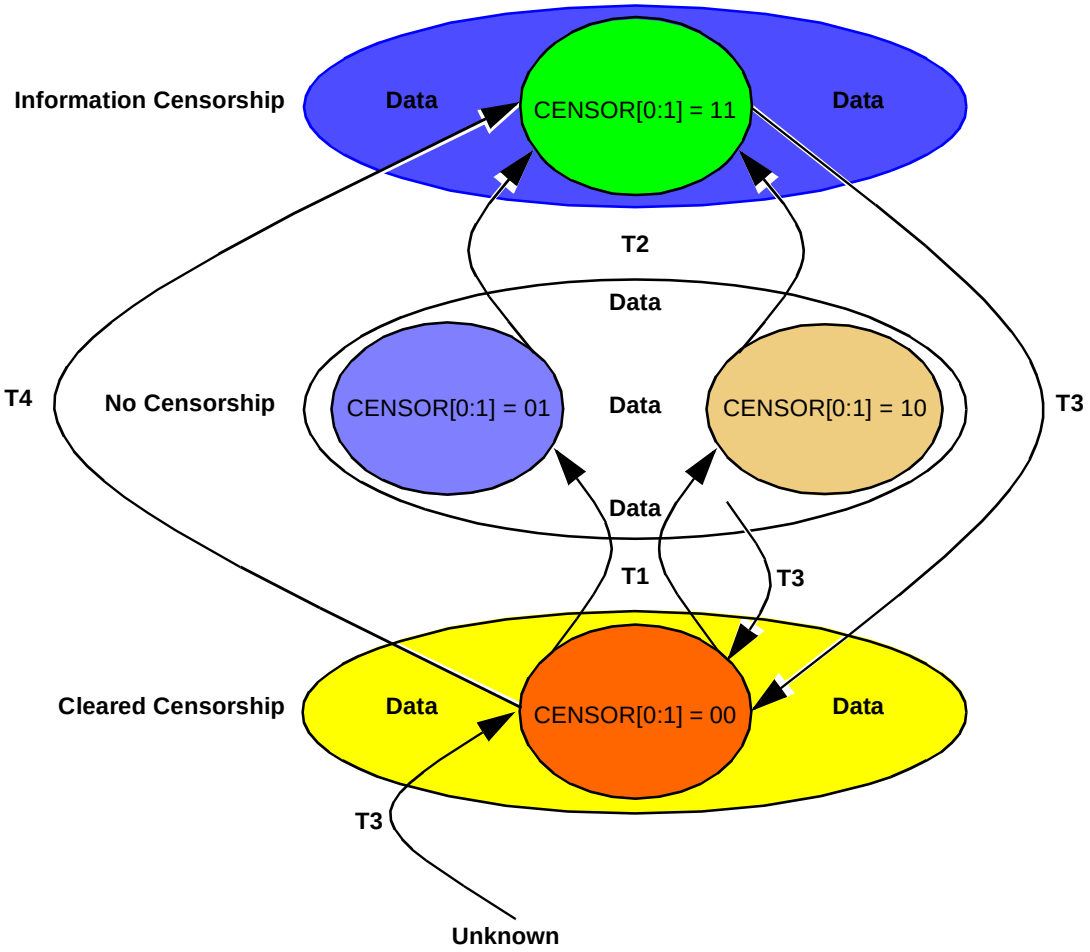

Figure 20-7 Censorship States and Transitions

CENSOR[0:1] transitions are listed as follows:

1. Cleared censorship to no censorship, T1
   Set CENSOR[0] or CENSOR[1].
2. No censorship to information censorship, T2
   Set CENSOR[0] and CENSOR[1].
3. Information censorship, no censorship or unknown to cleared censorship, T3
   Clear CENSOR[0:1]. This is done only while the entire UC3F array is erased.
4. Cleared censorship to information censorship, T4
   Set both CENSOR[0] and CENSOR[1].

20.4.12 Background Debug Mode or Freeze Operation

While in background debug mode, the UC3F should respond normally to accesses except that $\overline{\text{LOCK}}$ is writable.