SECTION 5
UNIFIED SYSTEM INTERFACE UNIT (USIU)

5.1 USIU Introduction

The unified system interface unit (USIU) of the MPC565 / MPC566 consists of several functional modules that control system start-up, system initialization and operation, system protection, and the external system bus. The MPC565 / MPC566 USIU functions include the following:

- System configuration and protection
- Enhanced interrupt controller
- System reset monitoring and generation
- Clock synthesizer
- Power management
- External bus interface (EBI)
- Memory controller supports four memory banks
- Debug support

5.2 USIU Module Overview

The system configuration and protection features control the overall system configuration and provides various monitors and timers, including the bus monitor, software watchdog timer, periodic interrupt timer, PPC decrementer, time base, and real-time clock. The interrupt controller supports up to eight external interrupts, eight levels for all internal USIU interrupt sources and 32 levels for internal peripheral modules reside on IMB bus. It has an enhanced mode of operation, which simplifies the MPC565 / MPC566 interrupt structure and speeding up interrupt processing.

The USIU provides several pinout configurations that allow up to 64 general-purpose I/O, external 32-bit port that supports internal and external masters, and various debug functions. Refer to **SECTION 6 SYSTEM CONFIGURATION AND PROTECTION** for details.

The USIU supports the internal flash censorship mechanism. Any attempt to operate the MPC565 / MPC566 from the external world, while the internal flash is in censor mode, locks the internal flash. The flash is blocked after following events:

- Booting from external memory;
- External master access into the MPC565 / MPC566;
- Debug port/READI accesses are performed.

The clock synthesizer generates the clock signals used by the USIU as well as the other modules and external devices. This circuitry can generate the system clock from a 4-MHz or 20-MHz crystal.

The USIU supports various low-power modes. Each one supplies a different range of power consumption, functionality and wake-up time. The clock scheme supports low power modes for applications that use the baud rate generators and/or serial ports during the standby mode. The main system clock can be changed dynamically while the baud rate generators and serial ports work with a fixed frequency. Refer to **SECTION 8 CLOCKS AND POWER CONTROL** for details.

The EBI handles the transfer of information between the internal busses and the memory or peripherals in the external address space. The MPC565 / MPC566 is designed to allow external bus masters to request and obtain mastership of the system bus, and if required access the on-chip memory and registers. Refer to **SECTION 9 EXTERNAL BUS INTERFACE** for details.

The memory controller module provides glueless interface to many types of memory devices and peripherals. It supports up to four memory banks.Refer to **SECTION 10 MEMORY CONTROLLER** for details.

Figure 5-1 shows the USIU block diagram.

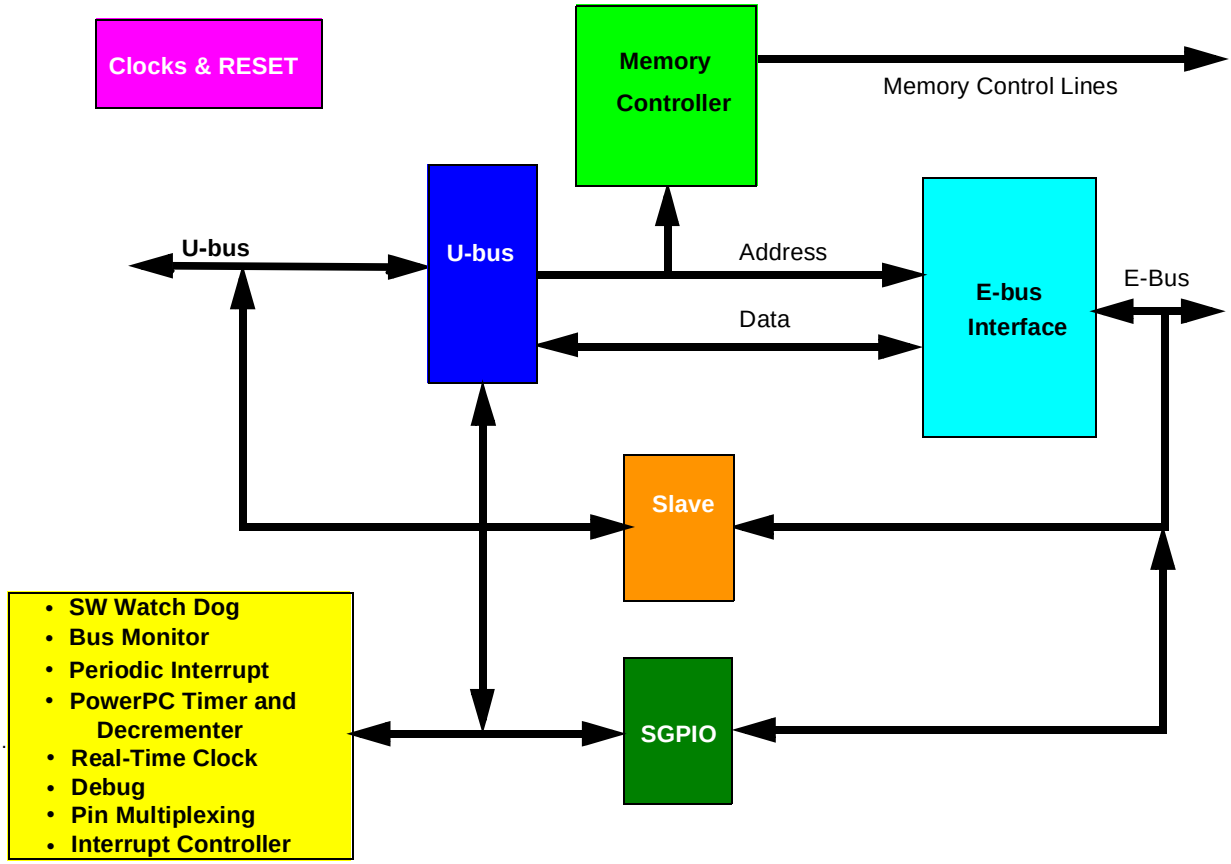

Figure 5-1 USIU Block Diagram

5.2.1 USIU Address Map

Table 5-1 is an address map of the SIU registers. Where not otherwise noted, registers are 32 bits wide. The address shown for each register is relative to the base address of the MPC565 / MPC566 internal memory map. The internal memory block can reside in one of eight possible four-Mbyte memory spaces. See Figure 1-3 for details.

Table 5-1 USIU Address Map

Address	Register
0x2F C000	SIU Module Configuration Register (SIUMCR) See Table 6-7 for bit descriptions.
0x2F C004	System Protection Control Register (SYPCR) See Table 6-15 for bit descriptions.
0x2F C008	Reserved
0x2F C00E[1]	Software Service Register (SWSR) See Table 6-16 for bit descriptions.
0x2F C010	Interrupt Pending Register (SIPEND).

Table 5-1 USIU Address Map (Continued)

Address	Register
0x2F C014	Interrupt Mask Register (SIMASK) See **SIMASK is a 32 bit read/write register. Each bit in the register corresponds to an interrupt request bit in the SIPEND register.** for bit descriptions.
0x2F C018	Interrupt Edge Level Mask (SIEL) See **6.14.2.7 SIU Interrupt Edge Level Register (SIEL)** for bit descriptions.
0x2F C01C	Interrupt Vector (SIVEC) See **6.14.2.8 SIU Interrupt Vector Register** for bit descriptions.
0x2F C020	Transfer Error Status Register (TESR) See **Table 6-17** for bit descriptions.
0x2F C024	USIU General-Purpose I/O Data Register (SGPIODT1) See **Table 6-23** for bit descriptions.
0x2F C028	USIU General-Purpose I/O Data Register 2 (SGPIODT2) See **Table 6-24** for bit descriptions.
0x2F C02C	USIU General-Purpose I/O Control Register (SGPIOCR) See **Table 6-25** for bit descriptions.
0x2F C030	External Master Mode Control Register (EMCR) See **Table 6-14** for bit descriptions.
0x2F C03C[1]	Pads Module Configuration Register (PDMCR) See **Table 2-3** for bit descriptions.
0x2F C040	Interrupt Pend2 Register (SIPEND2) See **6.14.2.2 SIU Interrupt Pending Register 2** for bit descriptions.
0x2F C044	Interrupt Pend3 Register (SIPEND3) See **6.14.2.3 SIU Interrupt Pending Register 3** for bit descriptions.
0x2F C048	Interrupt Mask2 Register (SIMASK2) See **6.14.2.5 SIU Interrupt Mask Register 2** for details.
0x2F C04C	Interrupt Mask3 Register (SIMASK3) See **6.14.2.6 SIU Interrupt Mask Register 3** for details.
0x2F C050	Interrupt In-Service2 Register (SISR2) See **6.14.2.9 Interrupt In-Service Registers** for details.
0x2F C054	Interrupt In-Service3 Register (SISR3) See **6.14.2.9 Interrupt In-Service Registers** for details.
0x2F C0FC — 0x2F C0FF	Reserved
Memory Controller Registers	
0x2F C100	Base Register 0 (BR0) See **Table 10-7** for bit descriptions.
0x2F C104	Option Register 0 (OR0) See **Table 10-8** for bit descriptions.
0x2F C108	Base Register 1 (BR1) See **Table 10-7** for bit descriptions.
0x2F C10C	Option Register 1 (OR1) See **Table 10-8** for bit descriptions.
0x2F C110	Base Register 2 (BR2) See **Table 10-7** for bit descriptions.
0x2F C114	Option Register 2 (OR2) See **Table 10-8** for bit descriptions.

Table 5-1 USIU Address Map (Continued)

Address	Register
0x2F C118	Base Register 3 (BR3) See **Table 10-7** for bit descriptions.
0x2F C11C	Option Register 3 (OR3) See **Table 10-8** for bit descriptions.
0x2F C120 — 0x2F C13C	Reserved
0x2F C140	Dual-Mapping Base Register (DMBR) See **Table 10-9** for bit descriptions.
0x2F C144	Dual-Mapping Option Register (DMOR) See **Table 10-10** for bit descriptions.
0x2F C148 — 0x2F C174	Reserved
0x2F C178[1]	Memory Status (MSTAT) See **Table 10-6** for bit descriptions.
0x2F C17A — 0x2F C1FC	Reserved
System Integration Timers	
0x2F C200	Time Base Status and Control (TBSCR) See **Table 6-18** for bit descriptions.
0x2F C204	Time Base Reference 0 (TBREF0) See **6.14.4.3 Time Base Reference Registers** for bit descriptions.
0x2F C208	Time Base Reference 1 (TBREF1) See **6.14.4.3 Time Base Reference Registers** for bit descriptions.
0x2F C20C — 0x2F C21C	Reserved
0x2F C220	Real-Time Clock Status and Control (RTCSC) See **Table 6-19** for bit descriptions.
0x2F C224	Real-Time Clock (RTC) See **6.14.4.6 Real-Time Clock Register (RTC)** for bit descriptions.
0x2F C228	Real-Time Alarm Seconds (RTSEC) — Reserved
0x2F C22C	Real-Time Alarm (RTCAL) See **6.14.4.7 Real-Time Clock Alarm Register (RTCAL)** for bit descriptions.
0x2F C230 — 0x2F C23C	Reserved
0x2F C240	PIT Status and Control (PISCR) See **Table 6-20** for bit descriptions.
0x2F C244	PIT Count (PITC) See **Table 6-21** for bit descriptions.
0x2F C248	PIT Register (PITR) See **Table 6-22** for bit descriptions.
0x2F C24C — 0x2F C27C	Reserved
Clocks and Reset	
0x2F C280	System Clock Control Register (SCCR) See **Table 8-9** for bit descriptions.
0x2F C284	PLL Low-Power and Reset Control Register (PLPRCR) See **Table 8-11** for bit descriptions.

Table 5-1 USIU Address Map (Continued)

Address	Register
0x2F C288[1]	Reset Status Register (RSR) See **Table 7-3** for bit descriptions.
0x2F C28C[1]	Change of Lock Interrupt Register (COLIR) See **Table 8-12** for bit descriptions.
0x2F C290[1]	VDDSRAM1 Control Register (VSRCR) See **Table 8-13** for bit descriptions.
0x2F C294 — 0x2F C2FC	Reserved
System Integration Timer Keys	
0x2F C300	Time Base Status and Control Key (TBSCRK) See **Table 8-8** for bit descriptions.
0x2F C304	Time Base Reference 0 Key (TBREF0K) See **Table 8-8** for bit descriptions.
0x2F C308	Time Base Reference 1 Key (TBREF1K) See **Table 8-8** for bit descriptions.
0x2F C30C	Time Base and Decrementor Key (TBK) See **Table 8-8** for bit descriptions.
0x2F C310 — 0x2F C31C	Reserved
0x2F C320	Real-Time Clock Status and Control Key (RTCSCK) See **Table 8-8** for bit descriptions.
0x2F C324	Real-Time Clock Key (RTCK) See **Table 8-8** for bit descriptions.
0x2F C328	Real-Time Alarm Seconds Key (RTSECK) See **Table 8-8** for bit descriptions.
0x2F C32C	Real-Time Alarm Key (RTCALK) See **Table 8-8** for bit descriptions.
0x2F C330 — 0x2F C33C	Reserved
0x2F C340	PIT Status and Control Key (PISCRIK) See **Table 8-8** for bit descriptions.
0x2F C344	PIT Count Key (PITCK) See **Table 8-8** for bit descriptions.
0x2F C348 — 0x2F C37C	Reserved
Clocks and Reset Keys	
0x2F C380	System Clock Control Key (SCCRK) See **Table 8-8** for bit descriptions.
0x2F C384	PLL Low-Power and Reset Control Register Key (PLPRCRK) See **Table 8-8** for bit descriptions.
0x2F C388	Reset Status Register Key (RSRK) See **Table 8-8** for bit descriptions.
0x2F C38C — 0x2F C3FC	Reserved

NOTES:
1. 16-bit register.

5.2.2 USIU Special Purpose Registers

Table 5-2 lists the MPC565 / MPC566 special purpose registers (SPR). These registers can be accessed with the PowerPC™ **mtspr** and **mfspr** instructions, or from an external master (refer to **6.2 External Master Modes** for details). All registers are 32 bits wide.

NOTE

RCPU special purpose registers can not be accessed by external master.

Table 5-2 USIU Special Purpose Registers

Internal Address[0:31]	Register	Decimal Address spr[5:9]:spr[0:4][1]
0x2C00	Decrementer (DEC). See **3.9.5 Decrementer Register (DEC)** for more information.	22
0x1880	Time Base — Read (TB). See **Table 3-11** for bit descriptions	268
0x1A80	Time Base Upper — Read (TBU). See **6.14.4.2 Time Base SPRs** for bit descriptions	269
0x3880	Time Base — Write (TB). See **Table 3-14** for bit descriptions	284
0x3A80	Time Base Upper — Write (TBU). See **6.14.4.2 Time Base SPRs** for bit descriptions	285
0x3B30	Internal Memory Mapping Register (IMMR). See **Table 6-13** for bit descriptions.	638

NOTES:
1. Bits [0:17] and [28:31] are all 0.

Table 5-3 shows the MPC565 / MPC566 address format for special purpose registers access. For an external master, accessing a PowerPC SPR, address bits [0:17] and [28:31] are compared to zeros to confirm that an SPR access is valid. See **6.2.1 Operation in External Master Modes** for more details.

Table 5-3 MPC565 / MPC566 Address Format for SPR Access From External Bus

0:17	18:27	28:31
0..0	spr[0:9]	0000