SECTION 18
TIME PROCESSOR UNIT 3

The time processor unit 3 (TPU3), an enhanced version of the original TPU, is an intelligent, semi-autonomous microcontroller designed for timing control. The TPU3 is fully compatible to the TPU2. Operating simultaneously with the CPU, the three TPU3 modules process micro-instructions, schedules and processes real-time hardware events, performs input and output, and accesses shared data without CPU intervention. Consequently, for each timer event, the CPU setup and service times are minimized or eliminated.

The MPC565 / MPC566 contains three independent TPU3s. **Figure 18-1** is a simplified block diagram of a single TPU3.

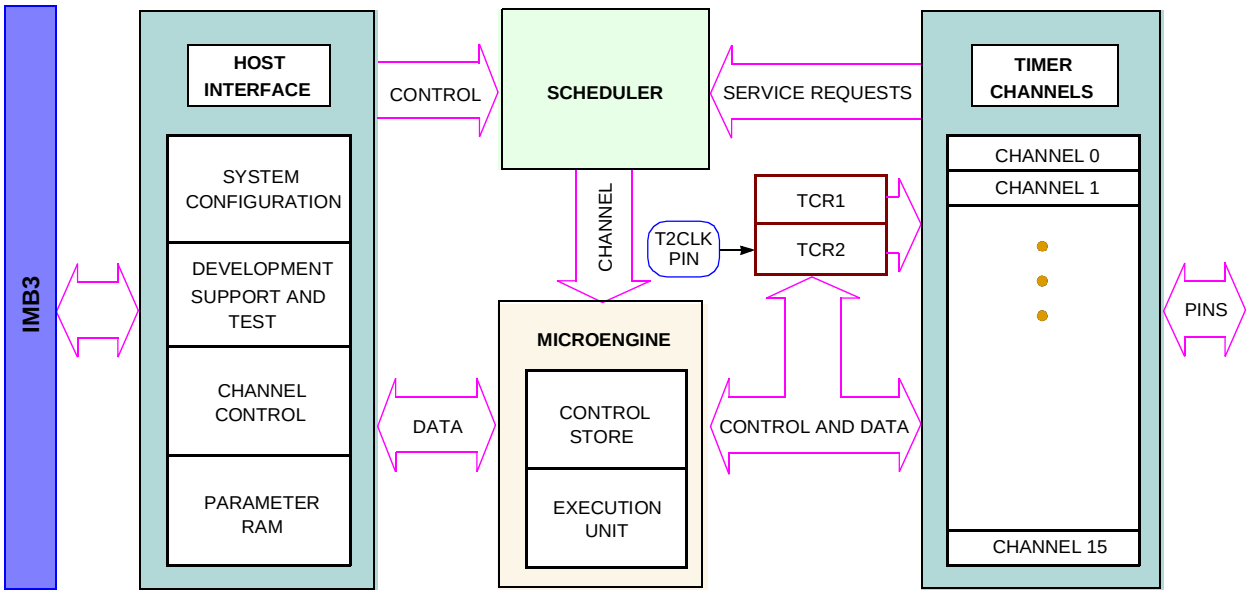

Figure 18-1 TPU3 Block Diagram

18.1 Overview

The TPU3 can be viewed as a special-purpose microcomputer that performs a programmable series of two operations, match and capture. Each occurrence of either operation is called an event. A programmed series of events is called a function. TPU functions replace software functions that would require CPU interrupt service.

The microcode ROM TPU3 functions that are available in the MPC565 / MPC566 are described in **APPENDIX D TPU ROM FUNCTIONS**.

18.2 TPU3 Components

The TPU3 consists of two 16-bit time bases, 16 independent timer channels, a task scheduler, a microengine, and a host interface. In addition, a dual-ported parameter RAM is used to pass parameters between the module and the CPU.

18.2.1 Time Bases

Two 16-bit counters provide reference time bases for all output compare and input capture events. Prescalers for both time bases are controlled by the CPU via bit fields in the TPU3 module configuration register (TPUMCR) and TPU module configuration register two (TPUMCR2). Timer count registers TCR1 and TCR2 provide access to the current counter values. TCR1 and TCR2 can be read by TPU microcode but are not directly available to the CPU. The TCR1 clock is always derived from the system clock. The TCR2 clock can be derived from the system clock or from an external input via theT2CLK clock pin. The duration between active edges on the T2CLK clock pin must be at least nine system clocks.

18.2.2 Timer Channels

The TPU3 has 16 independent channels, each connected to an MCU pin. The channels have identical hardware and are functionally equivalent in operation. Each channel consists of an event register and pin control logic. The event register contains a 16-bit capture register, a 16-bit compare/match register, and a 16-bit greater-than-or-equal-to comparator. The direction of each pin, either output or input, is determined by the TPU microengine. Each channel can either use the same time base for match and capture, or can use one time base for match and the other for capture.

18.2.3 Scheduler

When a service request is received, the scheduler determines which TPU3 channel is serviced by the microengine. A channel can request service for one of four reasons: for host service, for a link to another channel, for a match event, or for a capture event. The host system assigns each active channel one of three priorities: high, middle, or low. When multiple service requests are received simultaneously, a priority-scheduling mechanism grants service based on channel number and assigned priority.

18.2.4 Microengine

The microengine is composed of a control store and an execution unit. Control-store ROM holds the microcode for each factory-masked time function. When assigned to a channel by the scheduler, the execution unit executes microcode for a function assigned to that channel by the CPU. Microcode can also be executed from the dual-port RAM (DPTRAM) module instead of the control store. The DPTRAM allows emulation and development of custom TPU microcode without the generation of a microcode ROM mask. Refer to **18.3.6 Emulation Support** for more information.

18.2.5 Host Interface

The host interface registers allow communication between the CPU and the TPU3, both before and during execution of a time function. The registers are accessible from the IMB through the TPU3 bus interface unit. Refer to **18.4 Programming Model** for register bit/field definitions and address mapping.

18.2.6 Parameter RAM

Parameter RAM occupies 256 bytes at the top of the system address map. Channel parameters are organized as 128 16-bit words. Channels zero through 15 each have eight parameters. The parameter RAM address map in **18.4.18 TPU3 Parameter RAM** shows how parameter words are organized in memory.

The CPU specifies function parameters by writing to the appropriate RAM address. The TPU3 reads the RAM to determine channel operation. The TPU3 can also store information to be read by the CPU in the parameter RAM. Detailed descriptions of the parameters required by each time function are beyond the scope of this manual. Refer to the ***TPU Reference Manual*** **(TPURM/AD)**, included in the ***TPU Literature Package*** **(TPULITPAK/D)** for more information.

18.3 TPU Operation

All TPU3 functions are related to one of the two 16-bit time bases. Functions are synthesized by combining sequences of match events and capture events. Because the primitives are implemented in hardware, the TPU3 can determine precisely when a match or capture event occurs, and respond rapidly. An event register for each channel provides for simultaneous match/capture event occurrences on all channels.

When a match or input capture event requiring service occurs, the affected channel generates a service request to the scheduler. The scheduler determines the priority of the request and assigns the channel to the microengine at the first available time. The microengine performs the function defined by the content of the control store or emulation RAM, using parameters from the parameter RAM.

18.3.1 Event Timing

Match and capture events are handled by independent channel hardware. This provides an event accuracy of one time-base clock period, regardless of the number of channels that are active. An event normally causes a channel to request service. The time needed to respond to and service an event is determined by which channels and the number of channels requesting service, the relative priorities of the channels requesting service, and the microcode execution time of the active functions. Worst-case event service time (latency) determines TPU3 performance in a given application. Latency can be closely estimated. For more information, refer to the ***TPU Reference Manual*** **(TPURM/AD)**.

18.3.2 Channel Orthogonality

Most timer systems are limited by the fixed number of functions assigned to each pin. All TPU3 channels contain identical hardware and are functionally equivalent in oper-

ation, so that any channel can be configured to perform any time function. Any function can operate on the calling channel, and, under program control, on another channel determined by the program or by a parameter. The user controls the combination of time functions.

18.3.3 Interchannel Communication

The autonomy of the TPU3 is enhanced by the ability of a channel to affect the operation of one or more other channels without CPU intervention. Interchannel communication can be accomplished by issuing a link service request to another channel, by controlling another channel directly, or by accessing the parameter RAM of another channel.

18.3.4 Programmable Channel Service Priority

The TPU3 provides a programmable service priority level to each channel. Three priority levels are available. When more than one channel of a given priority requests service at the same time, arbitration is accomplished according to channel number. To prevent a single high-priority channel from permanently blocking other functions, other service requests of the same priority are performed in channel order after the lowest-numbered, highest-priority channel is serviced.

18.3.5 Coherency

For data to be coherent, all available portions of the data must be identical in age, or must be logically related. As an example, consider a 32-bit counter value that is read and written as two 16-bit words. The 32-bit value is read-coherent only if both 16-bit portions are updated at the same time, and write-coherent only if both portions take effect at the same time. Parameter RAM hardware supports coherent access of two adjacent 16-bit parameters. The host CPU must use a long-word operation to guarantee coherency.

18.3.6 Emulation Support

Although factory-programmed time functions can perform a wide variety of control tasks, they may not be ideal for all applications. The TPU3 provides emulation capability that allows the development of new time functions. Emulation mode is entered by setting the EMU bit in TPUMCR. In emulation mode, an auxiliary bus connection is made between the DPTRAM and the TPU3, and access to DPTRAM via the intermodule bus is disabled. A 9-bit address bus, a 32-bit data bus, and control lines transfer information between the modules. To ensure exact emulation, DPTFLASH module access timing remains consistent with access timing of the TPU microcode ROM control store.

To support changing TPU application requirements, Motorola has established a TPU function library. The function library is a collection of TPU functions written for easy assembly in combination with each other or with custom functions. Refer to Motorola Programming Note**,** ***Using the TPU Function Library and TPU Emulation Mode*** (**TPUPN00/D)** for information about developing custom functions and accessing the

TPU function library. Refer to the Motorola ***TPU Literature Package*** **(TPULITPAK/D)** for more information about specific functions.

18.3.7 TPU3 Interrupts

Each of the TPU3 channels can generate an interrupt service request. Interrupts for each channel must be enabled by writing to the appropriate control bit in the channel interrupt enable register (CIER). The channel interrupt status register (CISR) contains one interrupt status flag per channel. Time functions set the flags. Setting a flag bit causes the TPU3 to make an interrupt service request if the corresponding channel interrupt enable bit is set.

The TPU3 can generate one of 32 possible interrupt request levels on the IMB3. The value driven onto $\overline{\text{IRQ}}$[7:0] represents the interrupt level programmed in the IRL field of the TPU interrupt configuration register (TICR). Under the control of the ILBS bits in the ICR, each interrupt request level is driven during the time multiplexed bus during one of four different time slots, with eight levels communicated per time slot. No hardware priority is assigned to interrupts. Furthermore, if more than one source on a module requests an interrupt at the same level, the system software must assign a priority to each source requesting at that level. **Figure 18-2** displays the interrupt level scheme.

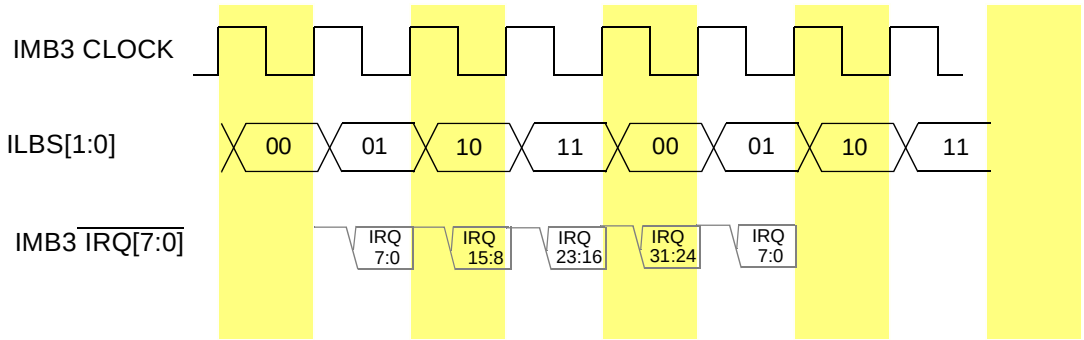

Figure 18-2 TPU3 Interrupt Levels

18.3.8 Prescaler Control for TCR1

Timer count register 1 (TCR1) is clocked from the output of a prescaler. The following fields control TCR1:

- The PSCK and TCR1P fields in TPUMCR
- The DIV2 field in TPUMCR2
- The EPSCKE and EPSCK fields in TPUMCR3.

The rate at which TCR1 is incremented is determined as follows:

- The user selects either the standard prescaler (by clearing the enhanced prescaler enable bit, EPSCKE, in TPUMCR3) or the enhanced prescaler (by setting EPSCKE).

— If the standard prescaler is selected (EPSCKE = 0), the the PSCK bit determines whether the standard prescaler divides the system clock input by 32 (PSCK = 0) or four (PSCK = 1)

— If the enhanced prescaler is selected (EPSCKE = 1), the EPSCK bits select a value by which the system clock is divided. The lowest frequency for TCR1 clock is system clock divided by 64x8. The highest frequency for TCR1 clock is system clock divided by two (2x1). See **Table 18-1**.

Table 18-1 Enhanced TCR1 Prescaler Divide Values

EPSCK Value	Divide System Clock By
0x00	2
0x01	4
0x02	6
0x03	8
0x04, 0x05,...0x1d	10,12,...60
0x1e	62
0x1f	64

— The output of either the standard prescaler or the enhanced prescaler is then divided by 1, 2, 4, or 8, depending on the value of the TCR1P field in the TPUMCR.

Table 18-2 TCR1 Prescaler Values

TCR1P Value	Divide by
0b00	1
0b01	2
0b10	4
0b11	8

— If the DIV2 bit is one, the TCR1 counter increments at a rate of the internal clock divided by two. If DIV2 is zero, the TCR1 increment rate is defined by the output of the TCR1 prescaler (which, in turn, takes as input the output of either the standard or enhanced prescaler).

Figure 18-3 shows a diagram of the TCR1 prescaler control block.

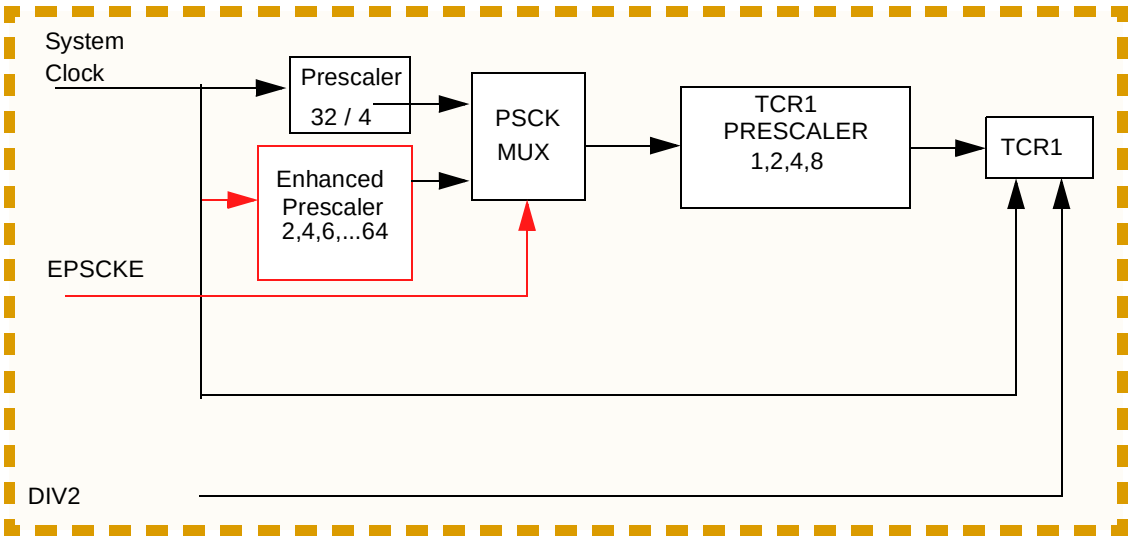

Figure 18-3 TCR1 Prescaler Control

18.3.9 Prescaler Control for TCR2

Timer count register 2 (TCR2), like TCR1, is clocked from the output of a prescaler. The T2CG (TCR2 clock/gate control) bit and the T2CSL (TCR2 counter clock edge) bit in TPUMCR determine T2CR2 pin functions. Refer to **Table 18-3**.

Table 18-3 TCR2 Counter Clock Source

T2CSL	T2CG	TCR2 Clock
0	0	Rise transition T2CLK
0	1	Gated system clock
1	0	Fall transition T2CLK
1	1	Rise and fall transition T2CLK

The function of the T2CG bit is shown in **Figure 18-4**.

When T2CG is set, the external T2CLK pin functions as a gate of the DIV8 clock (the TPU3 system clock divided by eight). In this case, when the external TCR2 pin is low, the DIV8 clock is blocked, preventing it from incrementing TCR2. When the external TCR2 pin is high, TCR2 is incremented at the frequency of the DIV8 clock. When T2CG is cleared, an external clock from the TCR2 pin, which has been synchronized and fed through a digital filter, increments TCR2. The duration between active edges on the T2CLK clock pin must be at least nine system clocks.

The TCR2PSCK2 bit in TPUMCR3 determines whether the clock source is divided by two before it is fed into the TCR2 prescaler. The TCR2 field in TPUMCR specifies the value of the prescaler: 1, 2, 4, or 8. Channels using TCR2 have the capability to

resolve down to the TPU3 system clock divided by eight. **Figure 18-4** illustrates the TCR2 pre-divider and pre-scaler control.

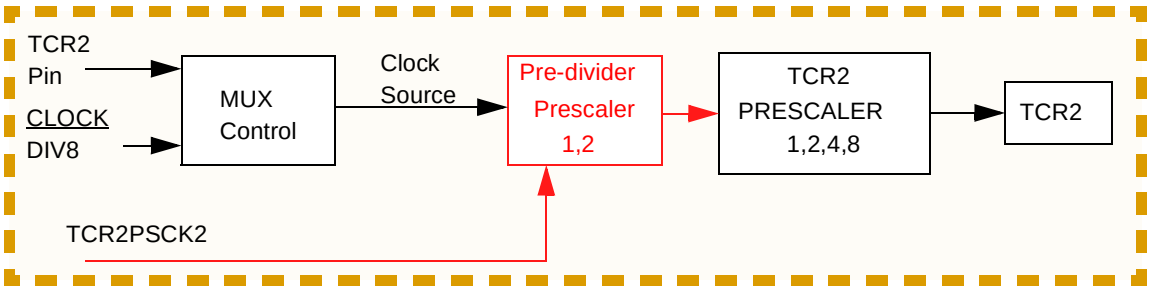

Figure 18-4 TCR2 Prescaler Control

Table 18-4 is a summary of prescaler output (assuming a divide-by-one value for the pre-divider prescaler.

Table 18-4 TCR2 Prescaler Control

TCR2 Value	Internal Clock Divide Ratio		External Clock Divide Ratio	
	TCR2PSCK2 = 0	TCR2PSCK2 = 1	TCR2PSCK2 = 0	TCR2PSCK2 = 1
0b00	8	8	1	1
0b01	16	24	2	3
0b10	32	56	4	7
0b11	64	120	8	15

18.4 Programming Model

The TPU3 memory map contains three groups of registers:

- System configuration registers
- Channel control and status registers
- Development support and test verification registers

All registers except the channel interrupt status register (CISR) must be read or written by means of half-word (16-bit) or word (32-bit) accesses. The address space of the TPU3 memory map occupies 512 bytes. Unused registers within the 512-byte address space return zeros when read.

Table 18-5 shows the TPU3 address map.

Table 18-5 TPU3 Register Map

	MSB 0 LSB 15
Address	**Register**
0x30 4000(A) 0x30 4400(B) 0x30 5C00(C)	TPU3 Module Configuration Register (TPUMCR) See **Table 18-6** for bit descriptions.
0x30 4002(A) 0x30 4402(B) 0x30 5C02(C)	TPU3 Test Configuration Register (TCR)
0x30 4004(A) 0x30 4404(B) 0x30 5C04(C)	Development Support Control Register (DSCR) See **Table 18-7** for bit descriptions.
0x30 4006(A) 0x30 4406(B) 0x30 5C06(C)	Development Support Status Register (DSSR) See **Table 18-8** for bit descriptions.
0x30 4008(A) 0x30 4408(B) 0x30 5C08(C)	TPU3 Interrupt Configuration Register (TICR) See **Table 18-9** for bit descriptions.
0x30 400A(A) 0x30 440A(B) 0x30 5C0A(C)	Channel Interrupt Enable Register (CIER) See **Table 18-10** for bit descriptions.
0x30 400C(A) 0x30 440C(B) 0x30 5C0C(C)	Channel Function Selection Register 0 (CFSR0) See **Table 18-11** for bit descriptions.
0x30 400E(A) 0x30 440E(B) 0x30 5C0E(C)	Channel Function Selection Register 1 (CFSR1) See **Table 18-11** for bit descriptions.
0x30 4010(A) 0x30 4410(B) 0x30 5C10(C)	Channel Function Selection Register 2 (CFSR2) See **Table 18-11** for bit descriptions.
0x30 4012(A) 0x30 4412(B) 0x30 5C12(C)	Channel Function Selection Register 3 (CFSR3) See **Table 18-11** for bit descriptions.
0x30 4014(A) 0x30 4414(B) 0x30 5C14(C)	Host Sequence Register 0 (HSQR0) See **Table 18-12** for bit descriptions.
0x30 4016(A) 0x30 4416(B) 0x30 4416(C)	Host Sequence Register 1 (HSQR1) See **Table 18-12** for bit descriptions.
0x30 4018(A) 0x30 4418(B) 0x30 5C18(C)	Host Service Request Register 0 (HSRR0) See **Table 18-13** for bit descriptions.
0x30 401A(A) 0x30 441A(B) 0x30 5C1A(C)	Host Service Request Register 1 (HSRR1) See **Table 18-13** for bit descriptions.
0x30 401C(A) 0x30 441C(B) 0x30 5C1C(C)	Channel Priority Register 0 (CPR0) See **Table 18-14** for bit descriptions.
0x30 401E(A) 0x30 441E(B) 0x30 5C1E(C)	Channel Priority Register 1 (CPR1) See **Table 18-14** for bit descriptions.

Table 18-5 TPU3 Register Map (Continued)

	MSB 0
Address	**Register**
0x30 4020(A) 0x30 4420(B) 0x30 5C20(C)	Channel Interrupt Status Register (CISR) See **Table 18-16** for bit descriptions.
0x30 4022(A) 0x30 4422(B) 0x30 5C22(C)	Link Register (LR)
0x30 4024(A) 0x30 4424(B) 0x30 5C24(C)	Service Grant Latch Register (SGLR)
0x30 4026(A) 0x30 4426(B) 0x30 5C26(C)	Decoded Channel Number Register (DCNR)
0x30 4028(A) 0x30 4428(B) 0x30 5C28(C)	TPU Module Configuration Register 2 (TPUMCR2) See **Table 18-17** for bit descriptions.
0x30 402A(A) 0x30 442A(B) 0x30 5C2A(C)	TPU Module Configuration 3 (TPUMCR3) See **Table 18-20** for bit descriptions.
0x30 402C(A) 0x30 442C(B) 0x30 5C2C(C)	Internal Scan Data Register (ISDR)
0x30 402E(A) 0x30 442E(B) 0x30 5C2E(C)	Internal Scan Control Register (ISCR)
0x30 4100 – 0x30 410F(A) 0x30 4500 – 0x30 450F(B) 0x30 5D00– 0x30 5D0F(C)	Channel 0 Parameter Registers
0x30 4110 – 0x30 411F(A) 0x30 4510 – 0x30 451F(B) 0x30 5D10 – 0x30 5D1F(C)	Channel 1 Parameter Registers
0x30 4120 – 0x30 412F(A) 0x30 4520 – 0x30 452F(B) 0x30 5D20 – 0x30 5D2F(C)	Channel 2 Parameter Registers
0x30 4130 – 0x30 413F(A) 0x30 4530 – 0x30 453F(B) 0x30 5D30 – 0x30 5D3F(C)	Channel 3 Parameter Registers
0x30 4140 – 0x30 414F(A) 0x30 4540 – 0x30 454F(B) 0x30 5D40 – 0x30 5D4F(C)	Channel 4 Parameter Registers
0x30 4150 – 0x30 415F(A) 0x30 4550 – 0x30 455F(B) 0x30 5D50 – 0x30 5D5F(C)	Channel 5 Parameter Registers
0x30 4160 – 0x30 416F(A) 0x30 4560 – 0x30 456F(B) 0x30 5D60 – 0x30 5D6F(C)	Channel 6 Parameter Registers
0x30 4170 – 0x30 417F(A) 0x30 4570 – 0x30 457F(B) 0x30 5D70 – 0x30 5D7F(C)	Channel 7 Parameter Registers

Table 18-5 TPU3 Register Map (Continued)

	MSB 0
Address	**Register**
0x30 4180 – 0x30 418F(A) 0x30 4580 – 0x30 458F(B) 0x30 5D80 – 0x30 5D8F(C)	Channel 8 Parameter Registers
0x30 4190 – 0x30 419F(A) 0x30 4590 – 0x30 459F(B) 0x30 5D90 – 0x30 5D9F(C)	Channel 9 Parameter Registers
0x30 41A0 – 0x30 41AF(A) 0x30 45A0 – 0x30 45AF(B) 0x30 5DA0 – 0x30 5DAF(C)	Channel 10 Parameter Registers
0x30 41B0 – 0x30 41BF(A) 0x30 45B0 – 0x30 45BF(B) 0x30 5DB0 – 0x30 5DBF(C)	Channel 11 Parameter Registers
0x30 41C0 – 0x30 41CF(A) 0x30 45C0 – 0x30 45CF(B) 0x30 5CC0 – 0x30 5CCF(C)	Channel 12 Parameter Registers
0x30 41D0 – 0x30 41DF(A) 0x30 45D0 – 0x30 45DF(B) 0x30 5DD0 – 0x30 5DDF(C)	Channel 13 Parameter Registers
0x30 41E0 – 0x30 41EF(A) 0x30 45E0 – 0x30 45EF(B) 0x30 5CD0 – 0x30 5DEF(C)	Channel 14 Parameter Registers
0x30 41F0 – 0x30 41FF(A) 0x30 45F0 – 0x30 45FF(B) 0x30 5DF0 – 0x30 5DFF(C)	Channel 15 Parameter Registers

18.4.1 TPU Module Configuration Register

TPUMCR — TPU Module Configuration Register **0x30 4000**
0x30 4400
0x30 5C00

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
STOP	TCR1P		TCR2P		EMU	T2CG	STF	SUPV	PSCK	TPU3	T2CSL	RESERVED			
RESET:															
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 18-6 TPUMCR Bit Descriptions

Bit(s)	Name	Description
0	STOP	Low-power stop mode enable. If the STOP bit in TPUMCR is set, the TPU3 shuts down its internal clocks, shutting down the internal microengine. TCR1 and TCR2 cease to increment and retain the last value before the stop condition was entered. The TPU3 asserts the stop flag (STF) in TPUMCR to indicate that it has stopped. 0 = Enable TPU3 clocks 1 = Disable TPU3 clocks
1:2	TCR1P	Timer count register 1 prescaler control. TCR1 is clocked from the output of a prescaler. The prescaler divides its input by 1, 2, 4, or 8. This is a write-once field unless the PWOD bit in TPUMCR3 is set. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 Refer to **18.3.8 Prescaler Control for TCR1** for more information.
3:4	TCR2P	Timer count register 2 prescaler control. TCR2 is clocked from the output of a prescaler. The prescaler divides this input by 1, 2, 4, or 8. This is a write-once field unless the PWOD bit in TPUMCR3 is set. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 Refer to **18.3.9 Prescaler Control for TCR2** for more information.
5	EMU	Emulation control. In emulation mode, the TPU3 executes microinstructions from DPTRAM exclusively. Access to the DPTRAM via the IMB3 is blocked, and the DPTRAM is dedicated for use by the TPU3. After reset, this bit can be written only once. 0 = TPU3 and DPTRAM operate normally 1 = TPU3 and DPTRAM operate in emulation mode
6	T2CG	TCR2 clock/gate control 0 = TCR2 pin used as clock source for TCR2 1 = TCR2 pin used as gate of DIV8 clock for TCR2 Refer to **18.3.9 Prescaler Control for TCR2** for more information.
7	STF	Stop flag. 0 = TPU3 is operating normally 1 = TPU3 is stopped (STOP bit has been set)
8	SUPV	Supervisor data space 0 = Assignable registers are accessible from user or supervisor privilege level 1 = Assignable registers are accessible from supervisor privilege level only
9	PSCK	Standard prescaler clock. Note that this bit has no effect if the extended prescaler is selected (EPSCKE = 1). 0 = $f_{SYS} \div 32$ is input to TCR1 prescaler, if standard prescaler is selected 1 = $f_{SYS} \div 4$ is input to TCR1 prescaler, if standard prescaler is selected
10	TPU3	TPU3 enable. The TPU3 enable bit provides compatibility with the TPU. If running TPU code on the TPU3, the microcode size should not be greater than 2 Kbytes and the TPU3 enable bit should be cleared to zero. The TPU3 enable bit is write-once after reset. The reset value is one, meaning that the TPU3 will operate in TPU3 mode. 0 = TPU mode; zero is the TPU reset value 1 = TPU3 mode; one is the TPU3 reset value **NOTE**: The programmer should not change this value unless necessary when developing custom TPU microcode.
11	T2CSL	TCR2 counter clock edge. This bit and the T2CG control bit determine the clock source for TCR2. Refer to **18.3.9 Prescaler Control for TCR2** for details.
12:15	—	Reserved. These bits are used for the IARB (interrupt arbitration ID) field in TPU3 implementations that use hardware interrupt arbitration.

18.4.2 TPU3 Test Configuration Register

TCR — TPU3 Test Configuration Register **0x30 4002, 0x30 4402, 0x30 5C02**

Used for factory test only.

18.4.3 Development Support Control Register

DSCR — Development Support Control Register **0x30 4004 0x30 4404 0x30 5C04**

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HOT4	RESERVED				BLC	CLKS	FRZ		CCL	BP	BC	BH	BL	BM	BT
RESET:															
0					0	0	0	0	0	0	0	0	0	0	0

Table 18-7 DSCR Bit Descriptions

Bit(s)	Name	Description
0	HOT4	Hang on T4 0 = Exit wait on T4 state caused by assertion of HOT4 1 = Enter wait on T4 state
1:4	—	Reserved
5	BLC	Branch latch control 0 = Latch conditions into branch condition register before exiting halted state 1 = Do not latch conditions into branch condition register before exiting the halted state or during the time-slot transition period
6	CLKS	Stop clocks (to TCRs) 0 = Do not stop TCRs 1 = Stop TCRs during the halted state
7:8	FRZ	FREEZE assertion response. The FRZ bits specify the TPU microengine response to the IMB3 FREEZE signal 00 = Ignore freeze 01 = Reserved 10 = Freeze at end of current microcycle 11 = Freeze at next time-slot boundary
9	CCL	Channel conditions latch. CCL controls the latching of channel conditions (MRL and TDL) when the CHAN register is written. 0 = Only the pin state condition of the new channel is latched as a result of the write CHAN register microinstruction 1 = Pin state, MRL, and TDL conditions of the new channel are latched as a result of a write CHAN register microinstruction
10	BP	µPC breakpoint enable 0 = Breakpoint not enabled 1 = Break if µPC equals µPC breakpoint register
11	BC	Channel breakpoint enable 0 = Breakpoint not enabled 1 = Break if CHAN register equals channel breakpoint register at beginning of state or when CHAN is changed through microcode
12	BH	Host service breakpoint enable 0 = Breakpoint not enabled 1 = Break if host service latch is asserted at beginning of state
13	BL	Link service breakpoint enable 0 = Breakpoint not enabled 1 = Break if link service latch is asserted at beginning of state
14	BM	MRL breakpoint enable 0 = Breakpoint not enabled 1 = Break if MRL is asserted at beginning of state
15	BT	TDL breakpoint enable 0 = Breakpoint not enabled 1 = Break if TDL is asserted at beginning of state

18.4.4 Development Support Status Register

DSSR — Development Support Status Register

0x30 4006
0x30 4406
0x30 5C04

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RESERVED								BKPT	PCBK	CHBK	SRBK	TPUF	RESERVED		
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-8 DSSR Bit Descriptions

Bit(s)	Name	Description
0:7	—	Reserved
8	BKPT	Breakpoint asserted flag. If an internal breakpoint caused the TPU3 to enter the halted state, the TPU3 asserts the BKPT signal on the IMB and sets the BKPT flag. BKPT remains set until the TPU3 recognizes a breakpoint acknowledge cycle, or until the IMB FREEZE signal is asserted.
9	PCBK	µPC breakpoint flag. PCBK is asserted if a breakpoint occurs because of a µPC (microprogram counter) register match with the µPC breakpoint register. PCBK is negated when the BKPT flag is cleared.
10	CHBK	Channel register breakpoint flag. CHBK is asserted if a breakpoint occurs because of a CHAN register match with the CHAN register breakpoint register. CHBK is negated when the BKPT flag is cleared.
11	SRBK	Service request breakpoint flag. SRBK is asserted if a breakpoint occurs because of any of the service request latches being asserted along with their corresponding enable flag in the development support control register. SRBK is negated when the BKPT flag is cleared.
12	TPUF	TPU3 FREEZE flag. TPUF is set whenever the TPU3 is in a halted state as a result of FREEZE being asserted. This flag is automatically negated when the TPU3 exits the halted state because of FREEZE being negated.
13:15	—	Reserved

18.4.5 TPU3 Interrupt Configuration Register

TICR — TPU3 Interrupt Configuration Register

0x30 4008
0x30 4408
0x30 5C08

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RESERVED					CIRL			ILBS		RESERVED					
RESET:															
					0	0	0	0	0	0	0				

Table 18-9 TICR Bit Descriptions

Bit(s)	Name	Description
0:4	—	Reserved
5:7	CIRL	Channel interrupt request level. This three-bit field specifies the interrupt request level for all channels. This field is used in conjunction with the ILBS field to determine the request level of TPU3 interrupts.
8:9	ILBS	Interrupt level byte select. This field and the CIRL field determine the level of TPU3 interrupt requests. 00 = $\overline{IRQ}$[0:7] selected 01 = $\overline{IRQ}$[8:15] selected 10 = $\overline{IRQ}$[16:23] selected 11 = $\overline{IRQ}$[24:31] selected
10:15	—	Reserved. Note that bits 10:11 represent channel interrupt base vector (CIBV) bits in some TPU3 implementations.

18.4.6 Channel Interrupt Enable Register

The channel interrupt enable register (CIER) allows the CPU to enable or disable the ability of individual TPU3 channels to request interrupt service. Setting the appropriate bit in the register enables a channel to make an interrupt service request; clearing a bit disables the interrupt.

CIER — Channel Interrupt Enable Register **0x30 400A**
0x30 440A
0x30 5C0A

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-10 CIER Bit Descriptions

Bit(s)	Name	Description
0:15	CH[15:0]	Channel interrupt enable/disable 0 = Channel interrupts disabled 1 = Channel interrupts enabled **NOTE:** The MSB (bit 0 in big-endian mode) represents CH15, and the LSB (bit 15 in big-endian mode) represents CH0.

18.4.7 Channel Function Select Registers

Encoded 4-bit fields within the channel function select registers specify one of 16 time functions to be executed on the corresponding channel. Encodings for predefined functions will be provided in a subsequent draft of this document.

CFSR0 — Channel Function Select Register 0

0x30 400C
0x30 440C
0x30 5C0C

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 15				CH 14				CH 13				CH 12			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CFSR1 — Channel Function Select Register 1

0x30 400E
0x30 440E
0x30 5C0E

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 11				CH 10				CH 9				CH 8			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CFSR2 — Channel Function Select Register 2

0x30 4010
0x30 4410
0x30 5C10

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 7				CH 6				CH 5				CH 4			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CFSR3 — Channel Function Select Register 3

0x30 4012
0x30 4412
0x30 5C12

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 3				CH 2				CH 1				CH 0			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-11 CFSRx Bit Descriptions

Name	Description
CH[15:0]	Encoded time function for each channel. Encoded four-bit fields in the channel function select registers specify one of 16 time functions to be executed on the corresponding channel.

18.4.8 Host Sequence Registers

The host sequence field selects the mode of operation for the time function selected on a given channel. The meaning of the host sequence bits depends on the time function specified. Meanings of host sequence bits and host service request bits for predefined time functions will be provided in a subsequent draft of this document.

HSQR0 — Host Sequence Register 0

0x30 4014
0x30 4414
0x30 5C14

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 15		CH 14		CH 13		CH 12		CH 11		CH 10		CH 9		CH 8	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HSQR1 — Host Sequence Register 1

0x30 4016
0x30 4416
0x30 5C16

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 7		CH 6		CH 5		CH 4		CH 3		CH 2		CH 1		CH 0	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-12 HSQRx Bit Descriptions

Name	Description
CH[15:0]	Encoded host sequence. The host sequence field selects the mode of operation for the time function selected on a given channel. The meaning of the host sequence bits depends on the time function specified.

18.4.9 Host Service Request Registers

The host service request field selects the type of host service request for the time function selected on a given channel. The meaning of the host service request bits is determined by time function microcode. Refer to the ***TPU Reference Manual* (TPURM/AD**) and the Motorola ***TPU Literature Package* (TPULITPAK/D)** for more information.

HSRR0 — Host Service Request Register 0

0x30 4018
0x30 4418
0x30 5C18

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 15		CH 14		CH 13		CH 12		CH 11		CH 10		CH 9		CH 8	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HSRR1 — Host Service Request Register 1

0x30 401A
0x30 441A
0x30 5C1A

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 7		CH 6		CH 5		CH 4		CH 3		CH 2		CH 1		CH 0	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-13 HSSRx Bit Descriptions

Name	Description
CH[15:0]	Encoded type of host service. The host service request field selects the type of host service request for the time function selected on a given channel. The meaning of the host service request bits depends on the time function specified. A host service request field cleared to 0b00 signals the host that service is completed by the microengine on that channel. The host can request service on a channel by writing the corresponding host service request field to one of three non-zero states. The CPU must monitor the host service request register until the TPU3 clears the service request to 0b00 before any parameters are changed or a new service request is issued to the channel.

18.4.10 Channel Priority Registers

The channel priority registers (CPR1, CPR2) assign one of three priority levels to a channel or disable the channel.

CPR0 — Channel Priority Register 0

0x30 401C
0x30 441C
0x30 5C1C

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 15		CH 14		CH 13		CH 12		CH 11		CH 10		CH 9		CH 8	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CPR1 — Channel Priority Register 1

0x30 401E
0x30 441E
0x30 5C1E

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 7		CH 6		CH 5		CH 4		CH 3		CH 2		CH 1		CH 0	
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-14 CPRx Bit Descriptions

Name	Description
CH[15:0]	Encoded channel priority levels. **Table 18-15** indicates the number of time slots guaranteed for each channel priority encoding.

Table 18-15 Channel Priorities

CHx[1:0]	Service	Guaranteed Time Slots
00	Disabled	—
01	Low	1 out of 7
10	Middle	2 out of 7
11	High	4 out of 7

18.4.11 Channel Interrupt Status Register

The channel interrupt status register (CISR) contains one interrupt status flag per channel. Time functions specify via microcode when an interrupt flag is set. Setting a flag causes the TPU3 to make an interrupt service request if the corresponding CIER bit is set. To clear a status flag, read CISR, then write a zero to the appropriate bit. CISR is the only TPU3 register that can be accessed on a byte basis.

CISR — Channel Interrupt Status Register

0x30 4020
0x30 4420
0x30 5C20

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-16 CISR Bit Descriptions

Bit(s)	Name	Description
0:15	CH[15:0]	Channel interrupt status 0 = Channel interrupt not asserted 1 = Channel interrupt asserted

18.4.12 Link Register

LR — Link Register **0x30 4022, 0x30 4422, 0x30 5C22**

Used for factory test only.

18.4.13 Service Grant Latch Register

SGLR — Service Grant Latch Register **0x30 4024, 0x30 4424, 0x30 5C24**

Used for factory test only.

18.4.14 Decoded Channel Number Register

DCNR — Decoded Channel Number Register **0x30 4026, 0x30 4426, 0x30 5C26**

Used for factory test only.

18.4.15 TPU3 Module Configuration Register 2

TPUMCR2 — TPU Module Configuration Register 2 **0x30 4028**
0x30 4428
0x30 5C28

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RESERVED							DIV2	SOFT RST	ETBANK		FPSCK			T2CF	DTPU
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18-17 TPUMCR2 Bit Descriptions

Bit(s)	Name	Description
0:6	—	Reserved
7	DIV2	Divide by 2 control. When asserted, the DIV2 bit, along with the TCR1P bit and the PSCK bit in the TPUMCR, determines the rate of the TCR1 counter in the TPU3. If set, the TCR1 counter increments at a rate of two system clocks. If negated, TCR1 increments at the rate determined by control bits in the TCR1P and PSCK fields. 0 = TCR1 increments at rate determined by control bits in the TCR1P and PSCK fields of the TPUMCR register 1 = Causes TCR1 counter to increment at a rate of the system clock divided by two
8	SOFT RST	Soft reset. The TPU3 performs an internal reset when both the SOFT RST bit in the TPUMCR2 and the STOP bit in TPUMCR are set. The CPU must write zero to the SOFT RST bit to bring the TPU3 out of reset. The SOFT RST bit must be asserted for at least nine clocks. 0 = Normal operation 1 = Puts TPU3 in reset until bit is cleared **NOTE**: Do not attempt to access any other TPU3 registers when this bit is asserted. When this bit is asserted, it is the only accessible bit in the register.

Table 18-17 TPUMCR2 Bit Descriptions (Continued)

Bit(s)	Name	Description
9:10	ETBANK	Entry table bank select. This field determines the bank where the microcoded entry table is situated. After reset, this field is 0b00. This control bit field is write once after reset. ETBANK is used when the microcode contains entry tables not located in the default bank 0. To execute the ROM functions on this MCU, ETBANK[1:0] must be 00. Refer to **Table 18-18**. **NOTE**: This field should not be modified by the programmer unless necessary because of custom microcode.
11:13	FPSCK	Filter prescaler clock. The filter prescaler clock control bit field determines the ratio between system clock frequency and minimum detectable pulses. The reset value of these bits is zero, defining the filter clock as four system clocks. Refer to **Table 18-19**.
14	T2CF	T2CLK pin filter control. When asserted, the T2CLK input pin is filtered with the same filter clock that is supplied to the channels. This control bit is write once after reset. 0 = Uses fixed four-clock filter 1 = T2CLK input pin filtered with same filter clock that is supplied to the channels
15	DTPU	Disable TPU3 pins. When the disable TPU3 control pin is asserted, pin TP15 is configured as an input disable pin. When the TP15 pin value is zero, all TPU3 output pins are three-stated, regardless of the pins function. The input is not synchronized. This control bit is write once after reset. 0 = TP15 functions as normal TPU3 channel 1 = TP15 pin configured as output disable pin. When TP15 pin is low, all TPU3 output pins are in a high-impedance state, regardless of the pin function.

Table 18-18 Entry Table Bank Location

ETBANK	Bank
00	0
01	1
10	2
11	3

Table 18-19 System Clock Frequency/Minimum Guaranteed Detected Pulse

Filter Control	Divide By	20 MHz	33 MHz	40 MHz
000	4	200 ns	121 ns	100 ns
001	8	400 ns	242 ns	200 ns
010	16	800 ns	485 ns	400 ns
011	32	1.6 µs	970 ns	800 ns
100	64	3.2 µs	1.94 µs	1.60 µs
101	128	6.4 µs	3.88 µs	3.20 µs
110	256	12.8 µs	7.76 µs	6.40 µs
111	512	25.6 µs	15.51 µs	12.80 µs

18.4.16 TPU Module Configuration Register 3

TPUMCR3 — TPU Module Configuration Register 3

0x30 402A
0x30 442A
0x30 5C2A

MSB LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RESERVED							PWOD	TCR2 PCK2	EPSCKE	RSVD	EPSCK				
RESET:					0	0	0	0	0	0	0				

Table 18-20 TPUMCR3 Bit Descriptions

Bit(s)	Name	Description
0:6	—	Reserved
7	PWOD	Prescaler write-once disable bit. The PWOD bit does not lock the EPSCK field and the EPSCKE bit. 0 = Prescaler fields in MCR are write-once 1 = Prescaler fields in MCR can be written anytime
8	TCR2PSCK2	TCR2 prescaler 2 0 = Prescaler clock source is divided by one. 1 = Prescaler clock is divided. See divider definitions in **Table 18-4**.
9	EPSCKE	Enhanced pre-scaler enable 0 = Disable enhanced prescaler (use standard prescaler) 1 = Enable enhanced prescaler. System clock will be divided by the value in EPSCK field.
10	—	Reserved
11:15	EPSCK	Enhanced prescaler value that will be loaded into the enhanced prescaler counter. Prescaler value = (EPSCK + 1) x 2. Refer to **18.3.8 Prescaler Control for TCR1** for details.

18.4.17 TPU3 Test Registers

The following TPU3 registers are used for factory test only:

- Internal scan data register (ISDR, address offset 0x30 402C, 0x30 442C, and 0x30 5C2C)
- Internal scan control register (ISCR, address offset 0x30 402E, 0x30 442E, 0x30 5C2E)

18.4.18 TPU3 Parameter RAM

The channel parameter registers are organized as one hundred 16-bit words of RAM. Channels 0 to 15 have eight parameters. The parameter registers constitute a shared work space for communication between the CPU and the TPU3. The TPU3 can only access data in the parameter RAM. Refer to **Table 18-21**.

Table 18-21 Parameter RAM Address Offset Map

Channel Number	Parameter							
	0	1	2	3	4	5	6	7
0	0x30 4100(A) 0x30 4500(B) 0x30 5D00(C)	0x30 4102A(A) 0x30 4502(B) 0x30 5D02(C)	0x30 4104(A) 0x30 4504(B) 0x30 5D04(C)	0x30 4106(A) 0x30 4506(B) 0x30 5D06(C)	0x30 4108(A) 0x30 4508(B) 0x30 5D08(C)	0x30 410A(A) 0x30 450A(B) 0x30 5D0A(C)	0x30 410C(A) 0x30 450C(B) 0x30 5D0C(C)	0x30 410E(A) 0x30 450E(B) 0x30 5D03(C)
1	0x30 4110(A) 0x30 4510(B) 0x30 5D10(C)	0x30 4112(A) 0x30 4512(B) 0x30 5D12(C)	0x30 4114(A) 0x30 4514(B) 0x30 5D14(C)	0x30 4116(A) 0x30 4516(B) 0x30 5D16(C)	0x30 4118(A) 0x30 4518(B) 0x30 5D18(C)	0x30 411A(A) 0x30 451A(B) 0x30 5D1A(C)	0x30 411C(A) 0x30 451C(B) 0x30 5D1C(C)	0x30 411E(A) 0x30 451E(B) 0x30 5D1E(C)
2	0x30 4120(A) 0x30 4520(B) 0x30 5D20(C)	0x30 4122(A) 0x30 4522(B) 0x30 5D23(C)	0x30 4124(A) 0x30 4524(B) 0x30 5D24(C)	0x30 4126(A) 0x30 4526(B) 0x30 5D26(C)	0x30 4128(A) 0x30 4528(B) 0x30 5D28(C)	0x30 412A(A) 0x30 452A(B) 0x30 5D2A(C)	0x30 412C(A) 0x30 452C(B) 0x30 5D2C(C)	0x30 412E(A) 0x30 452E(B) 0x30 5D2E(C)
3	0x30 4130(A) 0x30 4530(B) 0x30 5D30(C)	0x30 4132(A) 0x30 4532(B) 0x30 5D32(C)	0x30 4134(A) 0x30 4534(B) 0x30 5D34(C)	0x30 4136(A) 0x30 4536(B) 0x30 5D36(C)	0x30 4138(A) 0x30 4538(B) 0x30 5D38(C)	0x30 413A(A) 0x30 453A(B) 0x30 5D3A(C)	0x30 413C(A) 0x30 453C(B) 0x30 5D3C(C)	0x30 413E(A) 0x30 453E(B) 0x30 5D3E(C)
4	0x30 4140(A) 0x30 4540(B) 0x30 5D40(C)	0x30 4142(A) 0x30 4542(B) 0x30 5D42(C)	0x30 4144(A) 0x30 4544(B) 0x30 5D44(C)	0x30 4146(A) 0x30 4546(B) 0x30 5D46(C)	0x30 4148(A) 0x30 4548(B) 0x30 5D48(C)	0x30 414A(A) 0x30 454A(B) 0x30 5D4A(C)	0x30 414C(A) 0x30 454C(B) 0x30 5D4C(C)	0x30 414E(A) 0x30 454E(B) 0x30 5D4E(C)
5	0x30 4150(A) 0x30 4550(B) 0x30 5D50(C)	0x30 4152(A) 0x30 4552(B) 0x30 5D52(C)	0x30 4154(A) 0x30 4554(B) 0x30 5D54(C)	0x30 4156(A) 0x30 4556(B) 0x30 5D56(C)	0x30 4158(A) 0x30 4558(B) 0x30 5D58(C)	0x30 415A(A) 0x30 455A(B) 0x30 5D5A(C)	0x30 415C(A) 0x30 455C(B) 0x30 5D5C(C)	0x30 415E(A) 0x30 455E(B) 0x30 5D5E(C)
6	0x30 4160(A) 0x30 4560(B) 0x30 5D60(C)	0x30 4162(A) 0x30 4562(B) 0x30 5D62(C)	0x30 4164(A) 0x30 4564(B) 0x30 5D64(C)	0x30 4166(A) 0x30 4566(B) 0x30 5D66(C)	0x30 4168(A) 0x30 4568(B) 0x30 5D68(C)	0x30 416A(A) 0x30 456A(B) 0x30 5D6A(C)	0x30 416C(A) 0x30 456C(B) 0x30 5D6C(C)	0x30 416E(A) 0x30 456E(B) 0x30 5D6E(C)
7	0x30 4170(A) 0x30 4570(B) 0x30 5D70(C)	0x30 4172(A) 0x30 4572(B) 0x30 5D72(C)	0x30 4174(A) 0x30 4574(B) 0x30 5D74(C)	0x30 4176(A) 0x30 4576(B) 0x30 5D76(C)	0x30 4178(A) 0x30 4578(B) 0x30 5D78(C)	0x30 417A(A) 0x30 457A(B) 0x30 5D7A(C)	0x30 417C(A) 0x30 457C(B) 0x30 5D7C(C)	0x30 417E(A) 0x30 457E(B) 0x30 5D7E(C)
8	0x30 4180(A) 0x30 4580(B) 0x30 5D80(C)	0x30 4182(A) 0x30 4582(B) 0x30 5D82(C)	0x30 4184(A) 0x30 4585(B) 0x30 5D84(C)	0x30 4186(A) 0x30 4586(B) 0x30 5D86(C)	0x30 4188(A) 0x30 4588(B) 0x30 5D88(C)	0x30 418A(A) 0x30 458A(B) 0x30 5D8A(C)	0x30 418C(A) 0x30 458C(B) 0x30 5D8C(C)	0x30 418E(A) 0x30 458E(B) 0x30 5D8E(C)
9	0x30 4190(A) 0x30 4590(B) 0x30 5D90(C)	0x30 4192(A) 0x30 4592(B) 0x30 5D92(C)	0x30 4194(A) 0x30 4594(B) 0x30 5D94(C)	0x30 4196(A) 0x30 4596(B) 0x30 5D96(C)	0x30 4198(A) 0x30 4598(B) 0x30 5D98(C)	0x30 419A(A) 0x30 459A(B) 0x30 5D9A(C)	0x30 419C(A) 0x30 459C(B) 0x30 5D9C(C)	0x30 419E(A) 0x30 459E(B) 0x30 5D9E(C)
10	0x30 41A0(A) 0x30 45A0(B) 0x30 5DA0(C)	0x30 41A2(A) 0x30 45A2(B) 0x30 5DA2(C)	0x30 41A4(A) 0x30 45A4(B) 0x30 5DA4(C)	0x30 41A6(A) 0x30 45A6(B) 0x30 5DA6(C)	0x30 41A8(A) 0x30 45A8(B) 0x30 5DA8(C)	0x30 41AA(A) 0x30 45AA(B) 0x30 5DAA(C)	0x30 41AC(A) 0x30 45AC(B) 0x30 5DAC(C)	0x30 41AE(A) 0x30 45AE(B) 0x30 5DAE(C)
11	0x30 41B0(A) 0x30 45B0(B) 0x30 5DB0(C)	0x30 41B2(A) 0x30 45B2(B) 0x30 5DB2(C)	0x30 41B4(A) 0x30 45B4(B) 0x30 5DB4(C)	0x30 41B6(A) 0x30 45B6(B) 0x30 5DB6(C)	0x30 41B8(A) 0x30 45B8(B) 0x30 5DB8(C)	0x30 41BA(A) 0x30 45BA(B) 0x30 5DBA(C)	0x30 41BC(A) 0x30 45BC(B) 0x30 5DBC(C)	0x30 41BE(A) 0x30 45BE(B) 0x30 5DBE(C)
12	0x30 41C0(A) 0x30 45C0(B) 0x30 5DC0(C)	0x30 41C2(A) 0x30 45C2(B) 0x30 5DC2(C)	0x30 41C4(A) 0x30 45C4(B) 0x30 5DC4(C)	0x30 41C6(A) 0x30 45C6(B) 0x30 5DC6(C)	0x30 41C8(A) 0x30 45C8(B) 0x30 5DC8(C)	0x30 41CA(A) 0x30 45CA(B) 0x30 5DCA(C)	0x30 41CC(A) 0x30 45CC(B) 0x30 5DCC(C)	0x30 41CE(A) 0x30 45CE(B) 0x30 5DCE(C)
13	0x30 41D0(A) 0x30 45D0(B) 0x30 5DD0(C)	0x30 41D2(A) 0x30 45D2(B) 0x30 5DD2(C)	0x30 41D4(A) 0x30 45D4(B) 0x30 5DD4(C)	0x30 41D6(A) 0x30 45D6(B) 0x30 5DD6(C)	0x30 41D8(A) 0x30 45D8(B) 0x30 5DD8(C)	0x30 41DA(A) 0x30 45DA(B) 0x30 5DDA(C)	0x30 41DC(A) 0x30 45DC(B) 0x30 5DDC(C)	0x30 41DE(A) 0x30 45DE(B) 0x30 5DDE(C)
14	0x30 41E0(A) 0x30 45E0(B) 0x30 5DE0(C)	0x30 41E2(A) 0x30 45E2(B) 0x30 5DE2(C)	0x30 41E4(A) 0x30 45E4(B) 0x30 5DE4(C)	0x30 41E6(A) 0x30 45E6(B) 0x30 5DE6(C)	0x30 41E8(A) 0x30 45E8(B) 0x30 5DE8(C)	0x30 41EA(A) 0x30 45EA(B) 0x30 5DEA(C)	0x30 41EC(A) 0x30 45EC(B) 0x30 5DEC(C)	0x30 41EE(A) 0x30 45EE(B) 0x30 5DEE(C)
15	0x30 41F0(A) 0x30 45F0(B) 0x30 5DF0(C)	0x30 41F2(A) 0x30 45F2(B) 0x30 5DF2(C)	0x30 41F4(A) 0x30 45F4(B) 0x30 5DF4(C)	0x30 41F6(A) 0x30 45F6(B) 0x30 5DF6(C)	0x30 41F8(A) 0x30 45F8(B) 0x30 5DF8(C)	0x30 41FA(A) 0x30 45FA(B) 0x30 5DFA(C)	0x30 41FC(A) 0x30 45FC(B) 0x30 5DFC(C)	0x30 41FE(A) 0x30 45FE(B) 0x30 5DFE(C)

18.5 Time Functions

Descriptions of the MPC565 / MPC566 pre-programmed time functions are shown in **APPENDIX D TPU ROM FUNCTIONS**.