APPENDIX A
INTERNAL MEMORY MAP

The tables below use the following notations.

In the Access column: S = Supervisor Access Only, U = User Access, T = Test Access

In the Reset column: S = $\overline{\text{SRESET}}$, H = $\overline{\text{HRESET}}$, M = $\overline{\text{Module Reset}}$,
POR = $\overline{\text{Power-On Reset}}$, U = Unchanged, X = Unknown

The codes in the Reset column indicate which reset has an effect on register values.

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Table A-1 SPR (Special Purpose Registers)

Address	Access	Symbol	Register	Size	Reset
CR	U	CR	Condition State Register See **3.7.4 Condition Register (CR)** for bit descriptions	32	—
FPSCR	U	FPSCR	Floating-Point Status and Control Register See **Table 3-5** for bit descriptions	32	—
MSR	U	MSR	Machine State Register See **Table 3-12** for bit descriptions	32	—
SPR 1	U	XER	Integer Exception Register See **Table 3-10** for bit descriptions	32	—
SPR 8	U	LR	Link Register See **3.7.6 Link Register (LR)** for bit descrip-tions	32	—
SPR 9	U	CTR	Count Register See **3.7.7 Count Register (CTR)** for bit de-scriptions	32	—
SPR 18	U	DSISR	DAE/Source Instruction Service Register See **3.9.2 DAE/Source Instruction Service Register (DSISR)** for bit descriptions	32	—
SPR 19	U	DAR	Data Address Register See **3.9.3 Data Address Register (DAR)** for bit descriptions	32	—
SPR 22	S	DEC	Decrementer Register. See **3.9.5 Decrementer Register (DEC)** for more information.	32	POR, H
SPR 26	U	SRR0	Machine Status Save/Restore Register 0 See **3.9.6 Machine Status Save/Restore Register 0 (SRR0)** for bit descriptions	32	—
SPR 27	U	SRR1	Machine Status Save/Restore Register1 See **3.9.7 Machine Status Save/Restore Register 1 (SRR1)** for bit descriptions	32	—
SPR 80	U	EIE	External Interrupt Enable See **3.9.10.1 EIE, EID, and NRI Special-Pur-pose Registers** for bit descriptions.	32	—
SPR 81	U	EID	External Interrupt Disable See **3.9.10.1 EIE, EID, and NRI Special-Pur-pose Registers** for bit descriptions.	32	—
SPR 82	U	NRI	Non-Recoverable Interrupt Register See **3.9.10.1 EIE, EID, and NRI Special-Pur-pose Registers** for bit descriptions	32	—
SPR 144 — SPR 147	—	CMPA — CMPD	Comparator A-D Value Register. See **Table 22-17** for bit descriptions.	32	—
SPR 148	—	ECR	Exception Cause Regiser. See **Table 22-27** for bit descriptions.	32	—
SPR 149	—	DER	Debug Enable Regiser. See **Table 22-28** for bit descriptions.	32	—
SPR 150	—	COUNTA	Breakpoint Counter A Value and Control Regiser. See **Table 22-25** for bit descriptions.	32	—
SPR 151	—	COUNTB	Breakpoint Counter B Value and Control Regiser. See **Table 22-26** for bit descriptions.	32	—

Table A-1 SPR (Special Purpose Registers) (Continued)

Address	Access	Symbol	Register	Size	Reset
SPR 152 — SPR 153	—	CMPE — CMPF	Comparator E-F Value Register. See **Table 22-18** for bit descriptions.	32	—
SPR 154 — SPR 155	—	CMPG — CMPH	Comparator G-H Value Register. See **Table 22-20** for bit descriptions.	32	—
SPR 156	—	LCTRL1	L-bus Support Control Regiser 1. See **Table 22-23** for bit descriptions.	32	—
SPR 157	—	LCTRL2	L-bus Support Control Regiser 2. See **Table 22-24** for bit descriptions.	32	—
SPR 158	—	ICTRL	I-bus Support Control Regiser. See **Table 22-21** for bit descriptions.	32	—
SPR 159	—	BAR	Breakpoint Address Register. See **Table 22-19** for bit descriptions.	32	—
SPR 268, 269	U	TBL/TBU	Time Base Register See **Table 3-11** and **6.14.4.2 Time Base SPRs** for bit descriptions	32	POR, H
SPR 272 — SPR 275	U	SPRG0 — SPRG3	General Special-Purpose Registers 0-3 See **Table 3-15** for bit descriptions	32	—
SPR 284, 285	U	TBL/TBU	Time Base (Write Only) Register See **Table 3-14** and **6.14.4.2 Time Base SPRs** for bit descriptions	32	POR, H
SPR 287	U	PVR	Processor Version Register See **Table 3-14** for bit descriptions	32	—
SPR 1022	U	FPECR	Floating-Point Exception Cause Register See **Table 3-18** for bit descriptions	32	—
SPR 528	S	MI_GRA	MI Global Region Attribute Register. See **Table 4-8** for bit descriptions.	32	—
SPR 529	S	EIBADR	External Interrupt Relocation Table Base Address Register. See **Table 4-9** for bit descriptions.	32	—
SPR 536	S	L2U_GRA	L2U Global Region Attribute Register. See **Table 11-10** for bit descriptions.	32	—
SPR 560	S	BBCMCR	BBC Module Configuration Register. See **Table 4-4** for bit descriptions.	32	—
SPR 568	S	L2U_MCR	L2U Module Configuration Register. See **Table 11-7** for bit descriptions.	32	—
SPR 630	S	DPDR	Development Port Data Register See **22.5.6 Development Port Registers** for bit descriptions.	32	—
SPR 638	S	IMMR	Internal Memory Mapping Register. See **Table 6-13** for bit descriptions.	32	POR, H
SPR 784 – 787	S	MI_RBAx	MI Region x Base Address Register. See **Table 4-5** for bit descriptions.	32	—
SPR 792 – 795	S	L2U_RBAx	L2U Region x Base Address Register. See **Table 11-8** for bit descriptions.	32	—
SPR 816 – 819	S	MI_RAx	MI Region x Attribute Register. See **Table 4-6** for bit descriptions.	32	—
SPR 824 – 827	S	L2U_RAx	L2U Region x Attribute Register. See **Table 11-9** for bit descriptions.	32	—
SPR 1022	S	FPECR	Floating-Point Exception Cause Register See **3.9.10.2 Floating-Point Exception Cause Register (FPECR)** for bit descriptions.	32	—

Table A-2 UC3F Flash Array

Address	Access	Symbol	Register	Size	Reset
C3F_A					
0x00 0000 — 0x07 FFFF	U,S	UC3F_A	UC3F Flash Array A.	32	—
C3F_B					
0x08 0000 — 0x0F FFFF	U,S	UC3F_B	UC3F Flash Array B.	32	—

Table A-3 DECRAM SRAM Array

Address	Access	Symbol	Register	Size	Reset
0x2F 8000 — 0x2F 8FFF	U,S	DECRAM	DECRAM SRAM	32	—

Table A-4 BBC (Burst Buffer Controller Module)

Address	Access	Symbol	Register	Size	Reset
0x2F A004	U	DCCR1	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A008	U	DCCR2	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A00C	U	DCCR3	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	—	—
0x2F A010	U	DCCR4	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	16	S
0x2F A014	U	DCCR5	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	S
0x2F A018	U	DCCR6	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	S
0x2F A01C	U	DCCR7	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A020	U	DCCR8	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A024	U	DCCR9	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A028	U	DCCR10	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A02C	U	DCCR11	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A030	U	DCCR12	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A034	U	DCCR13	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A038	U	DCCR14	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H
0x2F A03C	U	DCCR15	Decompressor Class Configuration Register. See **Table 4-10** for bit descriptions.	32	H

Table A-5 USIU (Unified System Interface Unit)

Address	Access	Symbol	Register	Size	Reset
0x2F C000	U[1]	SIUMCR	SIU Module Configuration Register. See **Table 6-7** for bit descriptions.	32	H
0x2F C004	U[2]	SYPCR	System Protection Control Register. See **Table 6-15** for bit descriptions.	32	H
0x2F C008	—	—	Reserved	—	—
0x2F C00E	U, write only	SWSR	Software Service Register. See **Table 6-16** for bit descriptions.	16	S
0x2F C010	U	SIPEND	Interrupt Pending Register. See **6.14.2.1 SIU Interrupt Pending Register** for bit descriptions.	32	S
0x2F C014	U	SIMASK	Interrupt Mask Register. See **SIMASK is a 32 bit read/write register. Each bit in the register corresponds to an interrupt request bit in the SIPEND register.** for bit descriptions.	32	S
0x2F C018	U	SIEL	Interrupt Edge Level Mask. See **6.14.2.7 SIU Interrupt Edge Level Register (SIEL)** for bit descriptions.	32	H
0x2F C01C	U, read only	SIVEC	Interrupt Vector. See **6.14.2.8 SIU Interrupt Vector Register** for bit descriptions.	32	—
0x2F C020	U	TESR	Transfer Error Status Register. See **Table 6-17** for bit descriptions.	32	S
0x2F C024	U	SGPIODT1	USIU General-Purpose I/O Data Register 1. See **Table 6-23** for bit descriptions.	32	H
0x2F C028	U	SGPIODT2	USIU General-Purpose I/O Data Register 2. See **Table 6-24** for bit descriptions.	32	H
0x2F C02C	U	SGPIOCR	USIU General-Purpose I/O Control Register. See **Table 6-25** for bit descriptions.	32	H
0x2F C030	U	EMCR	External Master Mode Control Register. See **Table 6-14** for bit descriptions.	32	H
0x2F C03C	U	PDMCR	Pads Module Configuration Register. See **Table 2-3** for bit descriptions.	32	H
0x2F C040 — 0x2F C044	U	SIPEND2 — SIPEND3	Interrupt Pending Registers 2 and 3. See **6.14.2.1 SIU Interrupt Pending Register** for bit descriptions.	32	S
0x2F C048 — 0x2F C04C	U	SIMASK2 — SIMASK3	Interrupt Mask Register and Interrupt Mask Registers 2 and 3. See **6.14.2.9 Interrupt In-Service Registers** for bit descriptions.	32	S
0x2F C050 — 0x2F C054	U	SISR2 — SISR3	SISR2and SISR3 Registers. See **6.14.2.9 Interrupt In-Service Registers** for bit descriptions.	32	S
0x2F C0FC — 0x2F C0FF	—	—	Reserved	—	—
Memory Controller Registers					
0x2F C100	U	BR0	Base Register 0. See **Table 10-7** for bit descriptions.	32	H
0x2F C104	U	OR0	Option Register 0. See **Table 10-8** for bit descriptions.	32	H

Table A-5 USIU (Unified System Interface Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x2F C108	U	BR1	Base Register 1. See **Table 10-7** for bit descriptions.	32	H
0x2F C10C	U	OR1	Option Register 1. See **Table 10-8** for bit descriptions.	32	H
0x2F C110	U	BR2	Base Register 2. See **Table 10-7** for bit descriptions.	32	H
0x2F C114	U	OR2	Option Register 2. See **Table 10-8** for bit descriptions.	32	H
0x2F C118	U	BR3	Base Register 3. See **Table 10-7** for bit descriptions.	32	H
0x2F C11C	U	OR3	Option Register 3. See **Table 10-8** for bit descriptions.	32	H
0x2F C120 – 0x2F C13C	—	—	Reserved	—	—
0x2F C140	U	DMBR	Dual-Mapping Base Register. See **Table 10-9** for bit descriptions.	32	H
0x2F C144	U	DMOR	Dual-Mapping Option Register. See **Table 10-10** for bit descriptions.	32	H
0x2F C148 – 0x2F C174	—	—	Reserved	—	—
0x2F C178	U	MSTAT	Memory Status. See **Table 10-6** for bit descriptions.	16	H
System Integration Timers					
0x2F C200	U[3]	TBSCR	Time Base Status and Control. See **Table 6-18** for bit descriptions.	16	H
0x2F C204	U[3]	TBREF0	Time Base Reference 0. See **6.14.4.3 Time Base Reference Registers** for bit descriptions.	32	U
0x2F C208	U[3]	TBREF1	Time Base Reference 1. See **6.14.4.3 Time Base Reference Registers** for bit descriptions.	32	U
0x2F C20C – 0x2F C21C	—	—	Reserved	—	—
0x2F C220	U[4]	RTCSC	Real-Time Clock Status and Control. See **Table 6-19** for bit descriptions.	16	H
0x2F C224	U[4]	RTC	Real-Time Clock. See **6.14.4.6 Real-Time Clock Register (RTC)** for bit descriptions.	32	U
0x2F C228	T[4]	RTSEC	Real-Time Alarm Seconds, Reserved.	32	—
0x2F C22C	U[4]	RTCAL	Real-Time Alarm. See **6.14.4.7 Real-Time Clock Alarm Register (RTCAL)** for bit descriptions.	32	U
0x2F C230 – 0x2F C23C	—	—	Reserved	—	—
0x2F C240	U[3]	PISCR	PIT Status and Control. See **Table 6-20** for bit descriptions.	16	H
0x2F C244	U[3]	PITC	PIT Count. See **Table 6-21** for bit descriptions.	32 (half reserved)	U

Table A-5 USIU (Unified System Interface Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x2F C248	U, read only	PITR	PIT Register. See **Table 6-22** for bit descriptions.	32 (half reserved)	U
0x2F C24C – 0x2F C27C	—	—	Reserved	—	—
Clocks and Reset					
0x2F C280	U[2]	SCCR	System Clock Control Register. See **Table 8-9** for bit descriptions.	32	H
0x2F C284	U[3,5,6]	PLPRCR	PLL Low Power and Reset Control Register. See **Table 8-11** for bit descriptions.	32	H
0x2F C288	U[3]	RSR	Reset Status Register. See **Table 7-3** for bit descriptions.	16	POR
0x2F C28C	U	COLIR	Change of Lock Interrupt Register. See **Table 8-12** for bit descriptions.	16	U
0x2F C290	U	VSRCR	VDDSRAM1 Control Register. See **Table 8-13** for bit descriptions.	16	U
0x2F C294 – 0x2F C2FC	—	—	Reserved	—	—
System Integration Timer Keys					
0x2F C300	U	TBSCRK	Time Base Status and Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C304	U	TBREF0K	Time Base Reference 0 Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C308	U	TBREF1K	Time Base Reference 1 Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C30C	U	TBK	Time Base and Decrementer Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C310 – 0x2F C31C	—	—	Reserved	—	—
0x2F C320	U	RTCSCK	Real-Time Clock Status and Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C324	U	RTCK	Real-Time Clock Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C328	U	RTSECK	Real-Time Alarm Seconds Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C32C	U	RTCALK	Real-Time Alarm Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C330 – 0x2F C33C	—	—	Reserved	—	—
0x2F C340	U	PISCRIK	PIT Status and Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C344	U	PITCK	PIT Count Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C348 – 0x2F C37C	—	—	Reserved	—	—
Clocks and Reset Keys					
0x2F C380	U	SCCRK	System Clock Control Key. See **Table 8-8** for bit descriptions.	32	POR

Table A-5 USIU (Unified System Interface Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x2F C384	U	PLPRCRK	PLL Low-Power and Reset Control Register Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C388	U	RSRK	Reset Status Register Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C38C – 0x2F C3FC	—	—	Reserved	—	—

NOTES:

1. Entire register is locked if bit 15 (DLK) is set.
2. Write once after power on reset (POR).
3. Must use the key register to unlock if it has been locked by a key register, see **8.9.3.2 Keep-Alive Power Registers Lock Mechanism**.
4. Locked after Power on Reset (POR). A write of 0x55CCAA33 must performed to the key register to unlock. See **8.9.3.2 Keep-Alive Power Registers Lock Mechanism**.
5. Can have bits 0:11 (MF bits) write-protected by setting bit 4 (MFPDL) in the SCCR register to 1. Bit 21 (CSRC) and bits 22:23 (LPM) can be locked by setting bit 5 (LPML) of the SCCR register to 1.
6. Bit 24 (CSR) is write-once after soft reset.

Table A-6 CDR3 Flash Control Registers EEPROM (UC3F)

Address	Access	Symbol	Register	Size	Reset
C3F_A					
0x2F C800	U, S	C3FMCR_A	C3F EEPROM Configuration Register. See **Table 20-3** for bit descriptions.	32	POR, H
0x2F C804	U, S	C3FMCRE_A	C3F EEPROM Extended Configuration Register. See **Table 20-4** for bit descriptions.	32	POR, H
0x2F C808	U, S	C3FCTL_A	C3F EEPROM High Voltage Control Register. See **Table 20-5** for bit descriptions.	32	POR, H
C3F_B					
0x2F C840	U, S	C3FMCR_B	C3F EEPROM Configuration Register	32	POR, H
0x2F C844	U, S	C3FMCRE_B	C3F EEPROM Extended Configuration Register	32	POR, H
0x2F C848	U, S	C3FCTL_B	C3F EEPROM High Voltage Control Register	32	POR, H

Table A-7 DPTRAM AB and C Control Registers

Address	Access	Symbol	Register	Size	Reset
DPTRAM_AB Control					
0x30 0000	U, S[1]	DPTMCR_AB	DPTRAM Module Configuration Register. See **Table 19-2** for bit descriptions.	16	S
0x30 0002	S	DPTTCR_AB	Test Configuration Register.	16	S
0x30 0004	S	RAMBAR_AB	RAM Array Base Address Register. See **Table 19-3** for bit descriptions.	16	S
0x30 0006	S	MISRH_AB	Multiple Input Signature Register High.	16	S
0x30 0008	S	MISRL_AB	Multiple Input Signature Register Low.	16	S
0x30 000A	S	MISCNT_AB	MISC Counter Register.	16	S
DPTRAM_C Control					
0x30 0040	U, S[2]	DPTMCR_C	DPTRAM Module Configuration Register. See **Table 19-2** for bit descriptions.	16	S
0x30 0042	S	DPTTCR_C	Test Configuration Register.	16	S
0x30 0044	S	RAMBAR_C	RAM Array Base Address Register. See **Table 19-3** for bit descriptions.	16	S
0x30 0046	S	MISRH_C	Multiple Input Signature Register High.	16	S
0x30 0048	S	MISRL_C	Multiple Input Signature Register Low.	16	S
0x30 004A	S	MISCNT_C	MISC Counter Register.	16	S

NOTES:
1. Access to the DPTRAM_AB array through the IMB3 bus is disabled once bit 5 (EMU) of either TPUMCR_A or TPUMCR_B is set.
2. Access to the DPTRAM_C array through the IMB3 bus is disabled once bit 5 (EMU) of TPUMCR_C is set.

Table A-8 DLCMD2 (Data Link Controller Module)

Address	Access	Symbol	Register	Size	Reset
0x30 0080	S	MCR	Module Configuration Register. See **Table 15-7** for bit descriptions.	16	S, M
0x30 0084	S	IPR	Interrupt Pending Register. See **Table 15-9** for bit descriptions.	16	S, M
0x30 0086 — 0x30 0087	S	ILR — IVR	Interrupt Level Register and Interrupt Vector Register. See **Table 15-10** and **Table 15-12** for bit descriptions.	16	S, M
0x30 0088	S/U	SCTL	Symbol Timing Control and Pre-Scaler Register. See **Table 15-13** for bit descriptions.	16	S, M
0x30 008A	S/U	SDATA	Symbol Timing Control and Pre-Scaler Register. See **Table 15-15** for bit descriptions.	16	S, M
0x30 008C — 0x30 008D	S/U	CMD — TDATA	Command Register and Transmit Data Register. See **Table 15-17** and **Table 15-22** for bit descriptions.	16	S, M
0x30 008E — 0x30 008F	S/U	STAT — RDATA	Status Register and Receive Data Register. See **Table 15-23** and **Table 15-29** for bit descriptions.	16	S, M

Table A-9 DPTRAM Memory Arrays

DPTRAM_C Memory Array					
0x30 1000 — 0x30 1FFF	U, S[1]	DPRAM_C	DPTRAM Module Configuration Register. See **Table 19-2** for bit descriptions.	16	—
DPTRAM_AB Memory Array					
0x30 2000 — 0x30 37FF	U, S[2]	DPTRAM_AB	DPTRAM Module Configuration Register. See **Table 19-2** for bit descriptions.	16	—

NOTES:
1. Access to the DPTRAM_C array through the IMB3 bus is disabled once bit 5 (EMU) of TPUMCR_C is set.
2. Access to the DPTRAM_AB array through the IMB3 bus is disabled once bit 5 (EMU) of either TPUMCR_A or TPUMCR_B is set.

Table A-10 Time Processor Unit 3 A and B (TPU3 A and B)

Address	Access	Symbol	Register	Size	Reset
TPU_A (Note: Bit descriptions apply to TPU_B and TPU_C as well)					
0x30 4000	S[1]	TPUMCR_A	TPU3_A Module Configuration Register. See **Table 18-6** for bit descriptions.	16 only	S, M
0x30 4002	T	TCR_A	TPU3_A Test Configuration Register.	16	S, M
0x30 4004	S	DSCR_A	TPU3_A Development Support Control Register. See **Table 18-7** for bit descriptions.	16[2]	S, M
0x30 4006	S	DSSR_A	TPU3_A Development Support Status Register. See **Table 18-8** for bit descriptions.	16[2]	S, M
0x30 4008	S	TICR_A	TPU3_A Interrupt Configuration Register. See **Table 18-9** for bit descriptions.	16[2]	S, M
0x30 400A	S	CIER_A	TPU3_A Channel Interrupt Enable Register. See **Table 18-10** for bit descriptions.	16[2]	S, M
0x30 400C	S	CFSR0_A	TPU3_A Channel Function Selection Register 0. See **Table 18-11** for bit descriptions.	16[2]	S, M
0x30 400E	S	CFSR1_A	TPU3_A Channel Function Selection Register 1. See **Table 18-11** for bit descriptions.	16[2]	S, M
0x30 4010	S	CFSR2_A	TPU3_A Channel Function Selection Register 2. See **Table 18-11** for bit descriptions.	16[2]	S, M
0x30 4012	S	CFSR3_A	TPU_A Channel Function Selection Register 3. See **Table 18-11** for bit descriptions.	16[2]	S, M
0x30 4014	S/U[3]	HSQR0_A	TPU_A Host Sequence Register 0. See **Table 18-12** for bit descriptions.	16[2]	S, M
0x30 4016	S/U[3]	HSQR1_A	TPU_A Host Sequence Register 1. See **Table 18-12** for bit descriptions.	16[2]	S, M
0x30 4018	S/U[3]	HSRR0_A	TPU_A Host Service Request Register 0. See **Table 18-13** for bit descriptions.	16[2]	S, M
0x30 401A	S/U[3]	HSRR1_A	TPU_A Host Service Request Register 1. See **Table 18-13** for bit descriptions.	16[2]	S, M
0x30 401C	S	CPR0_A	TPU_A Channel Priority Register 0. See **Table 18-14** for bit descriptions.	16[2]	S, M
0x30 401E	S	CPR1_A	TPU_A Channel Priority Register 1. See **Table 18-14** for bit descriptions.	16[2]	S, M
0x30 4020	S	CISR_A	TPU_A Channel Interrupt Status Register. See **Table 18-16** for bit descriptions.	16	S, M

Table A-10 Time Processor Unit 3 A and B (TPU3 A and B) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4022	T	LR_A	TPU_A Link Register[4]	16[2]	S, M
0x30 4024	T	SGLR_A	TPU_A Service Grant Latch Register[4]	16[2]	S, M
0x30 4026	T	DCNR_A	TPU_A Decoded Channel Number Register[4]	16[2]	S, M
0x30 4028	S[5]	TPUMCR2_A	TPU_A Module Configuration Register 2. See **Table 18-17** for bit descriptions.	16[2]	S, M
0x30 402A	S	TPUMCR3_A	TPU_A Module Configuration Register 3. See **Table 18-20** for bit descriptions.	16[2]	S, M
0x30 402C	T	ISDR_A	TPU_A Internal Scan Data Register	16, 32[2]	—
0x30 402E	T	ISCR_A	TPU_A Internal Scan Control Register	16, 32[2]	—
0x30 4100 – 0x30 410F	S/U[3]	—	TPU_A Channel 0 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4110 – 0x30 411F	S/U[3]	—	TPU_A Channel 1 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4120 – 0x30 412F	S/U[3]	—	TPU_A Channel 2 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4130 – 0x30 413F	S/U[3]	—	TPU_A Channel 3 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4140 – 0x30 414F	S/U[3]	—	TPU_A Channel 4 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4150 – 0x30 415F	S/U[3]	—	TPU_A Channel 5 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4160 – 0x30 416F	S/U[3]	—	TPU_A Channel 6 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4170 – 0x30 417F	S/U[3]	—	TPU_A Channel 7 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4180 – 0x30 418F	S/U[3]	—	TPU_A Channel 8 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 4190 – 0x30 419F	S/U[3]	—	TPU_A Channel 9 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 41A0 – 0x30 41AF	S/U[3]	—	TPU_A Channel 10 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 41B0 – 0x30 41BF	S/U[3]	—	TPU_A Channel 11 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 41C0 – 0x30 41CF	S/U[3]	—	TPU_A Channel 11 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—

Table A-10 Time Processor Unit 3 A and B (TPU3 A and B) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 41D0 – 0x30 41DF	S/U[3]	—	TPU_A Channel 11 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 41E0 – 0x30 41EF	S/U[3]	—	TPU_A Channel 14 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
0x30 41F0 – 0x30 41FF	S/U[3]	—	TPU_A Channel 15 Parameter Registers. See **18.4.18 TPU3 Parameter RAM** for more information.	16, 32[2]	—
TPU_B					
0x30 4400[1]	S[1]	TPUMCR_B	TPU3_B Module Configuration Register	16 only	S, M
0x30 4402	T	TCR_B	TPU3_B Test Configuration Register	16	S, M
0x30 4404	S	DSCR_B	TPU3_B Development Support Control Register	16[2]	S, M
0x30 4406	S	DSSR_B	TPU3_B Development Support Status Register	16[2]	S, M
0x30 4408	S	TICR_B	TPU3_B Interrupt Configuration Register	16[2]	S, M
0x30 440A	S	CIER_B	TPU3_B Channel Interrupt Enable Register	16[2]	S, M
0x30 440C	S	CFSR0_B	TPU3_B Channel Function Selection Register 0	16[2]	S, M
0x30 440E	S	CFSR1_B	TPU3_B Channel Function Selection Register 1	16[2]	S, M
0x30 4410	S	CFSR2_B	TPU3_B Channel Function Selection Register 2	16[2]	S, M
0x30 4412	S	CFSR3_B	TPU_B Channel Function Selection Register 3	16[2]	S, M
0x30 4414	S/U[3]	HSQR0_B	TPU_B Host Sequence Register 0	16[2]	S, M
0x30 4416	S/U[3]	HSQR1_B	TPU_B Host Sequence Register 1	16[2]	S, M
0x30 4418	S/U[3]	HSRR0_B	TPU_B Host Service Request Register 0	16[2]	S, M
0x30 441A	S/U[3]	HSRR1_B	TPU_B Host Service Request Register 1	16[2]	S, M
0x30 441C	S	CPR0_B	TPU_B Channel Priority Register 0	16[2]	S, M
0x30 441E	S	CPR1_B	TPU_B Channel Priority Register 1	16[2]	S, M
0x30 4420	S	CISR_B	TPU_B Channel Interrupt Status Register	16	S, M
0x30 4422	T	LR_B	TPU_B Link Register	16[2]	S, M
0x30 4424	T	SGLR_B	TPU_B Service Grant Latch Register	16[2]	S, M
0x30 4426	T	DCNR_B	TPU_B Decoded Channel Number Register	16[2]	S, M
0x30 4428	S[4]	TPUMCR2_B	TPU_B Module Configuration Register 2	16[2]	S, M
0x30 442A	S	TPUMCR3_B	TPU_B Module Configuration Register 3	16, 32[2]	S, M
0x30 442C	T	ISDR_B	TPU_B Internal Scan Data Register	16, 32[2]	—
0x30 442E	T	ISCR_B	TPU_B Internal Scan Control Register	16, 32[2]	—
0x30 4500 – 0x30 450E	S/U[3]	—	TPU_B Channel 0 Parameter Registers	16, 32[2]	—
0x30 4510 – 0x30 451E	S/U[3]	—	TPU_B Channel 1 Parameter Registers	16, 32[2]	—
0x30 4520 – 0x30 452E	S/U[3]	—	TPU_B Channel 2 Parameter Registers	16, 32[2]	—

Table A-10 Time Processor Unit 3 A and B (TPU3 A and B) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4530 – 0x30 453E	S/U[3]	—	TPU_B Channel 3 Parameter Registers	16, 32[2]	—
0x30 4540 – 0x30 454E	S/U[3]	—	TPU_B Channel 4 Parameter Registers	16, 32[2]	—
0x30 4550 – 0x30 455E	S/U[3]	—	TPU_B Channel 5 Parameter Registers	16, 32[2]	—
0x30 4560 – 0x30 456E	S/U[3]	—	TPU_B Channel 6 Parameter Registers	16, 32[2]	—
0x30 4570 – 0x30 457E	S/U[3]	—	TPU_B Channel 7 Parameter Registers	16, 32[2]	—
0x30 4580 – 0x30 458E	S/U[3]	—	TPU_B Channel 8 Parameter Registers	16, 32[2]	—
0x30 4590 – 0x30 459E	S/U[3]	—	TPU_B Channel 9 Parameter Registers	16, 32[2]	—
0x30 45A0 – 0x30 45AE	S/U[3]	—	TPU_B Channel 10 Parameter Registers	16, 32[2]	—
0x30 45B0 – 0x30 45BF	S/U[3]	—	TPU_B Channel 11 Parameter Registers	16, 32[2]	—
0x30 45C0 – 0x30 45CF	S/U[3]	—	TPU_B Channel 11 Parameter Registers	16, 32[2]	—
0x30 45D0 – 0x30 45DF	S/U[3]	—	TPU_B Channel 11 Parameter Registers	16, 32[2]	—
0x30 45E0 – 0x30 45EF	S/U[3]	—	TPU_B Channel 14 Parameter Registers	16, 32[2]	—
0x30 45F0 – 0x30 45FF	S/U[3]	—	TPU_B Channel 15 Parameter Registers	16[2]	—

NOTES:
1. Bit 10 (TPU3) and bit 11 (T2CSL) are write-once. Bits 1:2 (TCR1P) and bits 3:4 (TCR2P) are write-once if PWOD is not set in the TPUMCR3 register. This register cannot be accessed with a 32-bit read. It can only be accessed with an 8- or 16-bit read.
2. Some TPU registers can only be read or written with 16- or 32-bit accesses. 8-bit accesses are not allowed.
3. S/U = Supervisor accessible only if SUPV = 1 or unrestricted if SUPV = 0. Unrestricted registers allow both user and supervisor access. The SUPV bit is in the TPUMCR register.
4. TPU code development (Debug) register
5. Bits 9:10 (ETBANK), 14 (T2CF), and 15 (DTPU) are write-once.

Table A-11 QADC64E A and B (Queued Analog-to-Digital Converter)

Address	Access	Symbol	Register	Size	Reset
QADC_A (Note: Bit descriptions apply to QADC_B as well)					
0x30 4800	S	QADC64MCR_A	QADC64 Module Configuration Register. See **Table 13-5** for bit descriptions.	16	S
0x30 4802	S	QADC64TST	QADC64 Test Register.	16	S
0x30 4804	S	QADC64INT_A	Interrupt Register. See **13.2.2 QADC64E Interrupt Register** for bit descriptions.	16	S
0x30 4806	S/U	PORTQA_A/ PORTQB_A	Port A and Port B Data. See **Table 13-21** for bit descriptions.	16	U

Table A-11 QADC64E A and B (Queued Analog-to-Digital Converter) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4808	S/U	DDRQA_A/ DDRQB_A	Port A Data and Port B Direction Register. See **Table 13-21** for bit descriptions.	16	S
0x30 480A	S/U	QACR0_A	QADC64 Control Register 0. See **Table 13-8** for bit descriptions.	16	S
0x30 480C	S/U[1]	QACR1_A	QADC64 Control Register 1. See **Table 13-10** for bit descriptions.	16	S
0x30 480E	S/U[1]	QACR2_A	QADC64 Control Register 2. See **Table 13-12** for bit descriptions.	16	S
0x30 4810	S/U	QASR0_A	QADC64 Status Register 0. See **Table 13-8** for bit descriptions.	16	S
0x30 4812	S/U	QASR1_A	QADC64 Status Register 1. See **Table 13-16** for bit descriptions.	16	S
0x30 4814 – 0x30 49FE	—	—	Reserved	—	—
0x30 4A00 – 0x30 4A7E	S/U	CCW_A	Conversion Command Word Table. See **Table 13-18** for bit descriptions.	16	U
0x30 4A80 – 0x30 4AFE	S/U	RJURR_A	Result Word Table Right-Justified, Unsigned Result Register. See **13.2.10 Result Word Table** for bit descriptions.	16	X
0x30 4B00 – 0x30 4B7E	S/U	LJSRR_A	Result Word Table Left-Justified, Signed Result Register. See **13.2.10 Result Word Table** for bit descriptions.	16	X
0x30 4B80 – 0x30 4BFE	S/U	LJURR_A	Result Word Table Left-Justified, Unsigned Result Register. See **13.2.10 Result Word Table** for bit descriptions.	16	X
QADC_B					
0x30 4C00	S	QADC64MCR_B	QADC64 Module Configuration Register	16	S
0x30 4C02	T	QADC64TEST_ B	QADC64 Test Register	16	—
0x30 4C04	S	QADC64INT_B	Interrupt Register	16	S
0x30 4C06	S/U	PORTQA_B/ PORTQB_B	Port A and Port B Data	16	U
0x30 4C08	S/U	DDRQA_B/ DDRQB_B	Port A Data and Port B Direction Register	16	S
0x30 4C0A	S/U	QACR0_B	QADC64 Control Register 0	16	S
0x30 4C0C	S/U[1]	QACR1_B	QADC64 Control Register 1	16	S
0x30 4C0E	S/U[1]	QACR2_B	QADC64 Control Register 2	16	S
0x30 4C10	S/U	QASR0_B	QADC64 Status Register 0	16	S
0x30 4C12	S/U	QASR1_B	QADC64 Status Register 1	16	S
0x30 4C14 – 0x30 4DFE	—	—	Reserved	—	—
0x30 4E00 – 0x30 4E7E	S/U	CCW_B	Conversion Command Word Table	16	U
0x30 4E80 – 0x30 4EFE	S/U	RJURR_B	Result Word Table. Right-Justified, Unsigned Result Register.	16	X

Table A-11 QADC64E A and B (Queued Analog-to-Digital Converter) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4F00 – 0x30 4F7E	S/U	LJSRR_B	Result Word Table. Left-Justified, Signed Result Register.	16	X
0x30 4F80 – 0x30 4FFE	S/U	LJURR_B	Result Word Table. Left-Justified, Unsigned Result Register.	16	X

NOTES:
1. Bit 3 (SSEx) is readable in test mode only.

Table A-12 QSMCM A and B (Queued Serial Multi-Channel Module)

Address	Access	Symbol	Register	Size	Reset
QSMCM_A **(Note: Bit descriptions apply to QSMCM_B as well)**					
0x30 5000	S	QSMCMMCR_A	QSMCM Module Configuration Register. See **Table 14-7** for bit descriptions.	16	S
0x30 5002	T	QTEST_A	QSMCM Test Register	16	S
0x30 5004	S	QDSCI_IL_A	Dual SCI Interrupt Level. See **Table 14-8** for bit descriptions.	16	S
0x30 5006	S	QSPI_IL_A	Queued SPI Interrupt Level. See **Table 14-9** for bit descriptions.	16	S
0x30 5008	S/U	SCC1R0_A	SCI1Control Register 0. See **Table 14-27** for bit descriptions.	16	S
0x30 500A	S/U	SCC1R1_A	SCI1Control Register 1. See **Table 14-28** for bit descriptions.	16	S
0x30 500C	S/U	SC1SR_A	SCI1 Status Register. See **Table 14-29** for bit descriptions.	16	S
0x30 500E	S/U	SC1DR_A	SCI1 Data Register. See **Table 14-30** for bit descriptions.	16	S
0x30 5010 — 0x30 5012	—	—	Reserved	—	—
0x30 5014	S/U	PORTQS_A	QSMCM Port QS Data Register. See **14.6.1 Port QS Data Register (PORTQS)** for bit descriptions.	16	S
0x30 5016	S/U	PQSPAR/ DDRQST_A	QSMCM Port QS PIn Assignment Register/ QSMCM Port QS Data Direction Register. See **Table 14-14** for bit descriptions.	16	S
0x30 5018	S/U	SPCR0_A	QSPI Control Register 0. See **Table 14-17** for bit descriptions.	16	S
0x30 501A	S/U	SPCR1_A	QSPI Control Register 1. See **Table 14-19** for bit descriptions.	16	S
0x30 501C	S/U	SPCR2_A	QSPI Control Register 2. See **Table 14-20** for bit descriptions.	16	S
0x30 501E	S/U	SPCR3_A	QSPI Control Register 3. See **Table 14-21** for bit descriptions.	8	S
0x30 501F	S/U	SPSR_A	QSPI Status Register 3. See **Table 14-22** for bit descriptions.	8	S
0x30 5020	S/U	SCC2R0_A	SCI2 Control Register 0. See **Table 14-27** for bit descriptions.	16	S
0x30 5022	S/U	SCC2R1_A	SCI2 Control Register 1. See **Table 14-28** for bit descriptions.	16	S

Table A-12 QSMCM A and B (Queued Serial Multi-Channel Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 5024	S/U	SC2SR_A	SCI2 Status Register. See **Table 14-29** for bit descriptions.	16	S
0x30 5026	S/U	SC2DR_A	SCI2 Data Register. See **Table 14-30** for bit descriptions.	16	S
0x30 5028	S/U[1]	QSCI1CR_A	QSCI1 Control Register. See **Table 14-35** for bit descriptions.	16	S
0x30 502A	S/U[2]	QSCI1SR_A	QSCI1 Status Register. See **Table 14-36** for bit descriptions.	16	S
0x30 502C – 0x30 504A	S/U	SCTQ_A	Transmit Queue Locations	16	S
0x30 504C – 0x30 506A	S/U	SCRQ_A	Receive Queue Locations	16	S
0x30 506C – 0x30 513F	—	—	Reserved	—	—
0x30 5140 – 0x30 517F	S/U	RECRAM_A	Receive Data RAM	16	S
0x30 5180 – 0x30 51BF	S/U	TRAN.RAM_A	Transmit Data RAM	16	S
0x30 51C0 – 0x30 51DF	S/U	COMD.RAM_A	Command RAM	16	S
QSMCM_B					
0x30 5400	S	QSMCMMCR_B	QSMCM Module Configuration Register. See **Table 14-7** for bit descriptions.	16	S
0x30 5402	T	QTEST_B	QSMCM Test Register	16	S
0x30 5404	S	QDSCI_IL_B	Dual SCI Interrupt Level. See **Table 14-8** for bit descriptions.	16	S
0x30 5406	S	QSPI_IL_B	Queued SPI Interrupt Level. See **Table 14-9** for bit descriptions.	16	S
0x30 5408	S/U	SCC1R0_B	SCI1Control Register 0. See **Table 14-27** for bit descriptions.	16	S
0x30 540A	S/U	SCC1R1_B	SCI1Control Register 1. See **Table 14-28** for bit descriptions.	16	S
0x30 540C	S/U	SC1SR_B	SCI1 Status Register. See **Table 14-29** for bit descriptions.	16	S
0x30 540E	S/U	SC1DR_B	SCI1 Data Register. See **Table 14-30** for bit descriptions.	16	S
0x30 5410 — 0x30 5412	—	—	Reserved	—	—
0x30 5414	S/U	PORTQS_B	QSMCM Port QS Data Register. See **14.6.1 Port QS Data Register (PORTQS)** for bit descriptions.	16	S
0x30 5416	S/U	PQSPAR/ DDRQST_B	QSMCM Port QS PIn Assignment Register/ QSMCM Port QS Data Direction Register. See **Table 14-14** for bit descriptions.	16	S
0x30 5418	S/U	SPCR0_B	QSPI Control Register 0. See **Table 14-17** for bit descriptions.	16	S
0x30 541A	S/U	SPCR1_B	QSPI Control Register 1. See **Table 14-19** for bit descriptions.	16	S

Table A-12 QSMCM A and B (Queued Serial Multi-Channel Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 541C	S/U	SPCR2_B	QSPI Control Register 2. See **Table 14-20** for bit descriptions.	16	S
0x30 541E	S/U	SPCR3_B	QSPI Control Register 3. See **Table 14-21** for bit descriptions.	8	S
0x30 541F	S/U	SPSR_B	QSPI Status Register 3. See **Table 14-22** for bit descriptions.	8	S
0x30 5420	S/U	SCC2R0_B	SCI2 Control Register 0	16	S
0x30 5422	S/U	SCC2R1_B	SCI2 Control Register 1	16	S
0x30 5424	S/U	SC2SR_B	SCI2 Status Register	16	S
0x30 5426	S/U	SC2DR_B	SCI2 Data Register	16	S
0x30 5428	S/U[3]	QSCI1CR_B	QSCI1 Control Register. See **Table 14-35** for bit descriptions.	16	S
0x30 542A	S/U[4]	QSCI1SR_B	QSCI1 Status Register. See **Table 14-36** for bit descriptions.	16	S
0x30 542C – 0x30 544A	S/U	SCTQ_B	Transmit Queue Locations	16	S
0x30 544C – 0x30 546A	S/U	SCRQ_B	Receive Queue Locations	16	S
0x30 546C – 0x30 553F	—	—	Reserved	—	—
0x30 5540 – 0x30 557F	S/U	RECRAM_B	Receive Data RAM	16	S
0x30 5580 – 0x30 55BF	S/U	TRAN.RAM_B	Transmit Data RAM	16	S
0x30 55C0 – 0x30 55DF	S/U	COMD.RAM_B	Command RAM	16	S

NOTES:
1. Bits 0–3 writeable only in test mode, otherwise read only.
2. Bits 3–11 writeable only in test mode, otherwise read only.
3. Bits 0–3 writeable only in test mode, otherwise read only.
4. Bits 3–11 writeable only in test mode, otherwise read only.

Table A-13 Time Processor Unit 3 C (TPU3_C)
(See Table A-10 for Bit Descriptions)

Address	Access	Symbol	Register	Size	Reset
TPU_C					
0x30 5C00[1]	S[1]	TPUMCR_C	TPU3_C Module Configuration Register	16 only	S, M
0x30 5C02	T	TCR_C	TPU3_C Test Configuration Register	16	S, M
0x30 5C04	S	DSCR_C	TPU3_C Development Support Control Register	16[2]	S, M
0x30 5C06	S	DSSR_C	TPU3_C Development Support Status Register	16[2]	S, M
0x30 5C08	S	TICR_C	TPU3_C Interrupt Configuration Register	16[2]	S, M
0x30 5C0A	S	CIER_C	TPU3_C Channel Interrupt Enable Register	16[2]	S, M

Table A-13 Time Processor Unit 3 C (TPU3_C) (Continued)
(See Table A-10 for Bit Descriptions) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 5C0C	S	CFSR0_C	TPU3_C Channel Function Selection Register 0	16[2]	S, M
0x30 5C0E	S	CFSR1_C	TPU3_C Channel Function Selection Register 1	16[2]	S, M
0x30 5C10	S	CFSR2_C	TPU3_C Channel Function Selection Register 2	16[2]	S, M
0x30 5C12	S	CFSR3_C	TPU_C Channel Function Selection Register 3	16[2]	S, M
0x30 5C14	S/U[3]	HSQR0_C	TPU_C Host Sequence Register 0	16[2]	S, M
0x30 5C16	S/U[3]	HSQR1_C	TPU_C Host Sequence Register 1	16[2]	S, M
0x30 5C18	S/U[3]	HSRR0_C	TPU_C Host Service Request Register 0	16[2]	S, M
0x30 5C1A	S/U[3]	HSRR1_C	TPU_C Host Service Request Register 1	16[2]	S, M
0x30 5CC	S	CPR0_C	TPU_C Channel Priority Register 0	16[2]	S, M
0x30 5C1E	S	CPR1_C	TPU_C Channel Priority Register 1	16[2]	S, M
0x30 5C20	S	CISR_C	TPU_C Channel Interrupt Status Register	16	S, M
0x30 5C22	T	LR_C	TPU_C Link Register	16[2]	S, M
0x30 5C24	T	SGLR_C	TPU_C Service Grant Latch Register	16[2]	S, M
0x30 5C26	T	DCNR_C	TPU_C Decoded Channel Number Register	16[2]	S, M
0x30 5C28	S[4]	TPUMCR2_C	TPU_C Module Configuration Register 2	16[2]	S, M
0x30 5C2A	S	TPUMCR3_C	TPU_C Module Configuration Register 3	16, 32[2]	S, M
0x30 5C2C	T	ISDR_C	TPU_C Internal Scan Data Register	16, 32[2]	
0x30 5C2E	T	ISCR_C	TPU_C Internal Scan Control Register	16, 32[2]	
0x30 5C00 – 0x30 5C0E	S/U[3]	—	TPU_C Channel 0 Parameter Registers	16, 32[2]	
0x30 5C10 – 0x30 5C1E	S/U[3]	—	TPU_C Channel 1 Parameter Registers	16, 32[2]	
0x30 5C20 – 0x30 5C2E	S/U[3]	—	TPU_C Channel 2 Parameter Registers	16, 32[2]	
0x30 5C30 – 0x30 5C3E	S/U[3]	—	TPU_C Channel 3 Parameter Registers	16, 32[2]	
0x30 5C40 – 0x30 5C4E	S/U[3]	—	TPU_C Channel 4 Parameter Registers	16, 32[2]	
0x30 5C50 – 0x30 5C5E	S/U[3]	—	TPU_C Channel 5 Parameter Registers	16, 32[2]	

Table A-13 Time Processor Unit 3 C (TPU3_C) (Continued)
(See Table A-10 for Bit Descriptions) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 5C60 – 0x30 5C6E	S/U[3]	—	TPU_C Channel 6 Parameter Registers	16, 32[2]	
0x30 5C70 – 0x30 5C7E	S/U[3]	—	TPU_C Channel 7 Parameter Registers	16, 32[2]	
0x30 5C80 – 0x30 5C8E	S/U[3]	—	TPU_C Channel 8 Parameter Registers	16, 32[2]	
0x30 5C90 – 0x30 5C9E	S/U[3]	—	TPU_C Channel 9 Parameter Registers	16, 32[2]	
0x30 5CA0 – 0x30 5CAE	S/U[3]	—	TPU_C Channel 10 Parameter Registers	16, 32[2]	
0x30 5CB0 – 0x30 5CBF	S/U[3]	—	TPU_C Channel 11 Parameter Registers	16, 32[2]	
0x30 5CC0 – 0x30 5CCF	S/U[3]	—	TPU_C Channel 11 Parameter Registers	16, 32[2]	
0x30 5CD0 – 0x30 5CDF	S/U[3]	—	TPU_C Channel 11 Parameter Registers	16, 32[2]	
0x30 5CE0 – 0x30 5CEF	S/U[3]	—	TPU_C Channel 14 Parameter Registers	16, 32[2]	
0x30 5CF0 – 0x30 5CFF	S/U[3]	—	TPU_C Channel 15 Parameter Registers	16[2]	

NOTES:
1. Bit 10 (TPU3) and bit 11 (T2CSL) are write-once. Bits 1:2 (TCR1P) and bits 3:4 (TCR2P) are write-once if PWOD is not set in the TPUMCR3 register. This register cannot be accessed with a 32-bit read. It can only be accessed with an 8- or 16-bit read.
2. Some TPU registers can only be read or written with 16- or 32-bit accesses. 8-bit accesses are not allowed.
3. S/U = Supervisor accessible only if SUPV = 1 or unrestricted if SUPV = 0. Unrestricted registers allow both user and supervisor access. The SUPV bit is in the TPUMCR register.
4. Bits 9:10 (ETBANK), 14 (T2CF), and 15 (DTPU) are write-once.

Table A-14 MIOS14 (Modular Input/Output Subsystem)

Address	Access	Symbol	Register	Size	Reset
0x30 6000	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S[1]
0x30 6002	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 6004	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 6006	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6008	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 600A	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 600C	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S

Table A-14 MIOS14 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 600E	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6010	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 6012	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 6014	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 6016	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6018	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 601A	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 601C	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 601E	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6020	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 6022	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 6024	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 6026	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6028	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 602A	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 602C	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 602E	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6030	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 17-18** for bit descriptions.	16	X
0x30 6032	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 17-19** for bit descriptions.	16	S
0x30 6034	S/U	MMCSMSCRD	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 6036	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 6038	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 17-18** for bit descriptions.	16	X
0x30 603A	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 17-19** for bit descriptions.	16	S
0x30 603E	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 6040	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 17-18** for bit descriptions.	16	X

Table A-14 MIOS14 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 6042	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 17-19** for bit descriptions.	16	S
0x30 6046	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 6050	S/U	MRTCSMFRCH	MRTCSM 32-Bit Counter High Buffer Register. See **Table 17-42** for bit descriptions.	16	U
0x30 6052	S/U	MRTCSMFRCL	MRTCSM 32-Bit Counter Low Buffer Register. See **Table 17-43** for bit descriptions.	16	U
0x30 6054	S/U	MRTCPR	MRTCSM Prescaler Counter Buffer Register. See **Table 17-44** for bit descriptions.	16	U
0x30 6056	S/U	MRTCSM	MRTCSM Status/Control Register. See **Table 17-45** for bit descriptions.	16	S
0x30 6058	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 605A	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6060	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6062	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6062	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6066	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 6068	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 606A	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 606E	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 6070	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6072	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6076	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 6078	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 607A	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 607E	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 6080	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 6082	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 6084	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S

Table A-14 MIOS14 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 6086	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6088	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 608A	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 608C	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 608E	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6090	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 6092	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 6094	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 6096	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 6098	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 609A	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 609C	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 609E	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 60A0	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 60A2	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 60A4	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 60A6	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 60A8	S/U	MPWMPERR	MPWMSM Period Register. See **Table 17-33** for bit descriptions.	16	S
0x30 60AA	S/U	MPWMPULR	MPWMSM Pulse Width Register. See **Table 17-34** for bit descriptions.	16	S
0x30 60AC	S/U	MPWMCNTR	MPWMSM Counter Register. See **Table 17-35** for bit descriptions.	16	S
0x30 60AE	S/U	MPWMSCR	MPWMSM Status/Control Register. See **Table 17-36** for bit descriptions.	16	S
0x30 60B0	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 17-18** for bit descriptions.	16	X
0x30 60B2	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 17-19** for bit descriptions.	16	S
0x30 60B6	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 60B8	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 17-18** for bit descriptions.	16	X

Table A-14 MIOS14 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 60BA	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 17-19** for bit descriptions.	16	S
0x30 60BE	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 60C0	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 17-18** for bit descriptions.	16	X
0x30 60C2	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 17-19** for bit descriptions.	16	S
0x30 60C6	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 17-20** for bit descriptions.	16	S
0x30 60DA	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60D8	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60DE	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 60E0	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60E2	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60E6	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 60E8	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60EA	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60EE	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 60F0	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 6F2	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60F6	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 60F8	S/U	MDASMAR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60FA	S/U	MDASMBR	MDASM DataA Register. See **Table 17-27** for bit descriptions.	16	S
0x30 60FE	S/U	MDASMSCR	MDASM Status/Control Register. See **Table 17-29** for bit descriptions.	16	S
0x30 6100	S/U	MPIOSMDR	MPIOSM Data Register. See **Table 17-40** for bit descriptions.	16	S
0x30 6102	S/U	MPIOSMDDR	MPIOSM Data Direction Register. See **Table 17-41** for bit descriptions.	16	S
0x30 6800	S/U	MIOS14TPCR	MIOS14 Test and Pin Control Register. See **Table 17-11** for bit descriptions.	16	X
0x30 6802	S/U	MIOS14VECT	MIOS14 Vector Register. See **Table 17-12** for bit descriptions.	16	X
0x30 6804	S/U	MIOS14VNR	MIOS14 Vector Register. See **Table 17-13** for bit descriptions.	16	S

Table A-14 MIOS14 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 6806	S/U	MIOS14MCR	MIOS14 Module Configuration Register. See **Table 17-14** for bit descriptions.	16	X
0x30 6816	S/U	MCPSMSCR	MCPSM Status/Control Register. See **Table 17-15** for bit descriptions.	16	X
0x30 6C00	S/U	MIOS14SR0	MIOS14 Interrupt Statis Register. See **Table 17-2** for bit descriptions.	16	X
0x30 6C04	S/U	MIOS14ER0	MIOS14 Interrupt Enable Register. See **Table 17-3** for bit descriptions.	16	X
0x30 6C06	S/U	MIOS14RPR0	MIOS14 Request Pending Register. See **Table 17-4** for bit descriptions.	16	S
0x30 6C30	S/U	MIOS14LVL0	MIOS14 Interrupt Level 0 Register. See **Table 17-8** for bit descriptions.	16	S
0x30 6C40	S/U	MIOS14SR1	MIOS14 Interrupt Status Register. See **Table 17-5** for bit descriptions.	16	X
0x30 6C44	S/U	MIOSER1	MIOS14 Interrupt Enable Register. See **Table 17-6** for bit descriptions.	16	X
0x30 6C46	S/U	MIOS14RPR1	MIOS14 Request Pending Register. See **Table 17-7** for bit descriptions.	16	X
0x30 6C70	S/U	MIOS14LVL1	MIOS14 Interrupt Level 1 Register. See **Table 17-9** for bit descriptions.	16	X

NOTES:
1. Only bits WEN, TEST, STB, and WIP affected by reset.

Table A-15 TouCAN A, B and C (CAN 2.0B Controller)

Address	Access	Symbol	Register	Size	Reset
TouCAN_A (Note: Bit descriptions apply to TouCAN_B and TouCAN_C as well)					
0x30 7080	S	TCNMCR_A	TouCAN_A Module Configuration Register. See **Table 16-11** for bit descriptions.	16	S
0x30 7082	T	TTR_A	TouCAN_A Test Register	16	S
0x30 7084	S	CANICR_A	TouCAN_A Interrupt Configuration Register. See **Table 16-12** for bit descriptions.	16	S
0x30 7086	S/U	CANCTRL0_A/ CANCTRL1_A	TouCAN_A Control Register 0/ TouCAN_A Control Register 1. See **Table 16-13** and **Table 16-16** for bit descriptions.	16	S
0x30 7088	S/U	PRESDIV_A/ CTRL2_A	TouCAN_A Control and Prescaler Divider Register/ TouCAN_A Control Register 2. See **Table 16-17** and **Table 16-18** for bit descriptions.	16	S
0x30 708A	S/U	TIMER_A	TouCAN_A Free-Running Timer Register. See **Table 16-19** for bit descriptions.	16	S
0x30 708C — 0x30 708E	—	—	Reserved	—	—
0x30 7090	S/U	RXGMASKHI_A	TouCAN_A Receive Global Mask High. See **Table 16-20** for bit descriptions.	32	S
0x30 7092	S/U	RXGMASKLO_A	TouCAN_A Receive Global Mask Low. See **Table 16-20** for bit descriptions.	32	S

Table A-15 TouCAN A, B and C (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 7094	S/U	RX14MASKHI_A	TouCAN_A Receive Buffer 14 Mask High. See **16.7.10 Receive Buffer 14 Mask Registers** for bit descriptions.	32	S
0x30 7096	S/U	RX14MASKLO_A	TouCAN_A Receive Buffer 14 Mask Low. See **16.7.10 Receive Buffer 14 Mask Registers** for bit descriptions.	32	S
0x30 7098	S/U	RX15MASKHI_A	TouCAN_A Receive Buffer 15 Mask High. See **16.7.11 Receive Buffer 15 Mask Registers** for bit descriptions.	32	S
0x30 709A	S/U	RX15MASKLO_A	TouCAN_A Receive Buffer 15 Mask Low. See **16.7.11 Receive Buffer 15 Mask Registers** for bit descriptions.	32	S
0x30 709C — 0x30 709E	—	—	Reserved	—	—
0x30 70A0	S/U	ESTAT_A	TouCAN_A Error and Status Register. See **Table 16-21** for bit descriptions.	16	S
0x30 70A2	S/U	IMASK_A	TouCAN_A Interrupt Masks. See **Table 16-24** for bit descriptions.	16	S
0x30 70A4	S/U	IFLAG_A	TouCAN_A Interrupt Flags. See **Table 16-25** for bit descriptions.	16	S
0x30 70A6	S/U	RXECTR_A/ TXECTR_A	TouCAN_A Receive Error Counter/ TouCAN_A Transmit Error Counter. See **Table 16-26** for bit descriptions.	16	S
0x30 7100 — 0x30 710F	S/U	MBUFF0_A[1]	TouCAN_A Message Buffer 0. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 7110 — 0x30 711F	S/U	MBUFF1_A[1]	TouCAN_A Message Buffer 1. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 7120 — 0x30 712F	S/U	MBUFF2_A[1]	TouCAN_A Message Buffer 2. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 7130 — 0x30 713F	S/U	MBUFF3_A[1]	TouCAN_A Message Buffer 3. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 7140 — 0x30 714F	S/U	MBUFF4_A[1]	TouCAN_A Message Buffer 4. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 7150 — 0x30 715F	S/U	MBUFF5_A[1]	TouCAN_A Message Buffer 5. See **Figure 16-3** and **Figure 16-3** for message buffer definitions.	—	U
0x30 7160 — 0x30 716F	S/U	MBUFF6_A[1]	TouCAN_A Message Buffer 6. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307170 — 0x30717F	S/U	MBUFF7_A[1]	TouCAN_A Message Buffer 7. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 7180 — 0x30 718F	S/U	MBUFF8_A[1]	TouCAN_A Message Buffer 8. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U

Table A-15 TouCAN A, B and C (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 7190 — 0x30 719F	S/U	MBUFF9_A[1]	TouCAN_A Message Buffer 9. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 71A0 — 0x30 71AF	S/U	MBUFF10_A[1]	TouCAN_A Message Buffer 10. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 71B0 — 0x30 71BF	S/U	MBUFF11_A[1]	TouCAN_A Message Buffer 11. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 71C0 — 0x30 71CF	S/U	MBUFF12_A[1]	TouCAN_A Message Buffer 12. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 71D0 — 0x30 71DF	S/U	MBUFF13_A[1]	TouCAN_A Message Buffer 13. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 71E0 — 0x30 71EF	S/U	MBUFF14_A[1]	TouCAN_A Message Buffer 14. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x30 71F0 — 0x30 71FF	S/U	MBUFF15_A[1]	TouCAN_A Message Buffer 15. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
TouCAN_B					
0x30 7480	S	TCNMCR_B	TouCAN_B Module Configuration Register	16	S
0x30 7482	T	TTR_B	TouCAN_B Test Register	16	S
0x30 7484	S	CANICR_B	TouCAN_B Interrupt Configuration Register	16	S
0x30 7486	S/U	CANCTRL0_B/ CANCTRL1_B	TouCAN_B Control Register 0/ TouCAN_B Control Register 1	16	S
0x30 7488	S/U	PRESDIV_B/ CTRL2_B	TouCAN_B Control and Prescaler Divider Register/ TouCAN_B Control Register 2	16	S
0x30 748A	S/U	TIMER_B	TouCAN_B Free-Running Timer Register		S
0x30 748C — 0x30 748E	—	—	Reserved	—	—
0x30 7490	S/U	RXGMASKHI_B	TouCAN_B Receive Global Mask High	32	S
0x30 7492	S/U	RXGMASKLO_B	TouCAN_B Receive Global Mask Low	32	S
0x30 7494	S/U	RX14MASKHI_B	TouCAN_B Receive Buffer 14 Mask High	32	S
0x30 7496	S/U	RX14MASKLO_B	TouCAN_B Receive Buffer 14 Mask Low	3	S
0x30 7498	S/U	RX15MASKHI_B	TouCAN_B Receive Buffer 15 Mask High	32	S
0x30 749A	S/U	RX15MASKLO_B	TouCAN_B Receive Buffer 15 Mask Low	32	S
0x30 749C — 0x30 749E	—	—	Reserved	—	—
0x30 74A0	S/U	ESTAT_B	TouCAN_B Error and Status Register	16	S
0x30 74A2	S/U	IMASK_B	TouCAN_B Interrupt Masks	16	S
0x30 74A4	S/U	IFLAG_B	TouCAN_B Interrupt Flags	16	S
0x30 74A6	S/U	RXECTR_B/ TXECTR_B	TouCAN_B Receive Error Counter/ TouCAN_B Transmit Error Counter	16	S
0x30 7500 — 0x30 750F	S/U	MBUFF0_B[1]	TouCAN_B Message Buffer 0.	—	U
0x30 7510 — 0x30 751F	S/U	MBUFF1_B[1]	TouCAN_B Message Buffer 1.	—	U

Table A-15 TouCAN A, B and C (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 7520 — 0x30 752F	S/U	MBUFF2_B[1]	TouCAN_B Message Buffer 2.	—	U
0x30 7530 — 0x30 753F	S/U	MBUFF3_B[1]	TouCAN_B Message Buffer 3.	—	U
0x30 7540 — 0x30 754F	S/U	MBUFF4_B[1]	TouCAN_B Message Buffer 4.	—	U
0x30 7550 — 0x30 755F	S/U	MBUFF5_B[1]	TouCAN_B Message Buffer 5.	—	U
0x30 7560 — 0x30 756F	S/U	MBUFF6_B[1]	TouCAN_B Message Buffer 6.	—	U
0x30 7570 — 0x30 757F	S/U	MBUFF7_B[1]	TouCAN_B Message Buffer 7.	—	U
0x30 7580 — 0x30 758F	S/U	MBUFF8_B[1]	TouCAN_B Message Buffer 8.	—	U
0x30 7590 — 0x30 759F	S/U	MBUFF9_B[1]	TouCAN_B Message Buffer 9.	—	U
0x30 75A0 — 0x30 75AF	S/U	MBUFF10_B[1]	TouCAN_B Message Buffer 10.	—	U
0x30 75B0 — 0x30 75BF	S/U	MBUFF11_B[1]	TouCAN_B Message Buffer 11.	—	U
0x30 75C0 — 0x30 75CF	S/U	MBUFF12_B[1]	TouCAN_B Message Buffer 12.	—	U
0x30 75D0 — 0x30 75DF	S/U	MBUFF13_B[1]	TouCAN_B Message Buffer 13.	—	U
0x30 75E0 — 0x30 75EF	S/U	MBUFF14_B[1]	TouCAN_B Message Buffer 14.	—	U
0x30 75F0 — 0x30 75FF	S/U	MBUFF15_B[1]	TouCAN_B Message Buffer 15.	—	U
TouCAN_C					
0x30 7880	S	TCNMCR_C	TouCAN_C Module Configuration Register	16	S
0x30 7882	T	TTR_C	TouCAN_C Test Register	16	S
0x30 7884	S	CANICR_C	TouCAN_C Interrupt Configuration Register	16	S
0x30 7886	S/U	CANCTRL0_C/ CANCTRL1_C	TouCAN_C Control Register 0/ TouCAN_C Control Register 1	16	S
0x30 7888	S/U	PRESDIV_C/ CTRL2_C	TouCAN_C Control and Prescaler Divider Register/ TouCAN_C Control Register 2	16	S
0x30 788A	S/U	TIMER_C	TouCAN_C Free-Running Timer Register		S
0x30 788C — 0x30 788E	—	—	Reserved	—	—
0x30 7890	S/U	RXGMASKHI_C	TouCAN_C Receive Global Mask High	32	S
0x30 7892	S/U	RXGMASKLO_C	TouCAN_C Receive Global Mask Low	32	S
0x30 7894	S/U	RX14MASKHI_C	TouCAN_C Receive Buffer 14 Mask High	32	S
0x30 7896	S/U	RX14MASKLO_C	TouCAN_C Receive Buffer 14 Mask Low	32	S
0x30 7898	S/U	RX15MASKHI_C	TouCAN_C Receive Buffer 15 Mask High	32	S
0x30 789A	S/U	RX15MASKLO_C	TouCAN_C Receive Buffer 15 Mask Low	32	S
0x30 789C — 0x30 789E	—	—	Reserved	—	—
0x30 78A0	S/U	ESTAT_C	TouCAN_C Error and Status Register	16	S

Table A-15 TouCAN A, B and C (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 78A2	S/U	IMASK_C	TouCAN_C Interrupt Masks	16	S
0x30 78A4	S/U	IFLAG_C	TouCAN_C Interrupt Flags	16	S
0x30 78A6	S/U	RXECTR_C/ TXECTR_C	TouCAN_C Receive Error Counter/ TouCAN_C Transmit Error Counter	16	S
0x30 7500 — 0x30 750F	S/U	MBUFF0_C[1]	TouCAN_C Message Buffer 0.	—	U
0x30 7510 — 0x30 751F	S/U	MBUFF1_C[1]	TouCAN_B Message Buffer 1.	—	U
0x30 7520 — 0x30 752F	S/U	MBUFF2_C[1]	TouCAN_C Message Buffer 2.	—	U
0x30 7530 — 0x30 753F	S/U	MBUFF3_C[1]	TouCAN_C Message Buffer 3.	—	U
0x30 7540 — 0x30 754F	S/U	MBUFF4_C[1]	TouCAN_C Message Buffer 4.	—	U
0x30 7550 — 0x30 755F	S/U	MBUFF5_C[1]	TouCAN_C Message Buffer 5.	—	U
0x30 7560 — 0x30 756F	S/U	MBUFF6_C[1]	TouCAN_C Message Buffer 6.	—	U
0x30 7570 — 0x30 757F	S/U	MBUFF7_C[1]	TouCAN_C Message Buffer 7.	—	U
0x30 7580 — 0x30 758F	S/U	MBUFF8_C[1]	TouCAN_C Message Buffer 8.	—	U
0x30 7590 — 0x30 759F	S/U	MBUFF9_C[1]	TouCAN_C Message Buffer 9.	—	U
0x30 75A0 — 0x30 75AF	S/U	MBUFF10_C[1]	TouCAN_C Message Buffer 10.	—	U
0x30 75B0 — 0x30 75BF	S/U	MBUFF11_C[1]	TouCAN_C Message Buffer 11.	—	U
0x30 75C0 — 0x30 75CF	S/U	MBUFF12_C[1]	TouCAN_C Message Buffer 12.	—	U
0x30 75D0 — 0x30 75DF	S/U	MBUFF13_C[1]	TouCAN_C Message Buffer 13.	—	U
0x30 75E0 — 0x30 75EF	S/U	MBUFF14_C[1]	TouCAN_C Message Buffer 14.	—	U
0x30 75F0 — 0x30 75FF	S/U	MBUFF15_C[1]	TouCAN_C Message Buffer 15.	—	U

NOTES:

1. The last word of each of the the MBUFF arrays (address 0x....E) is reserved and may cause a RCPU exception if read.

Table A-16 UIMB (U-Bus to IMB Bus Interface)

Address	Access	Symbol	Register	Size	Reset
0x30 7F80	S[1]	UMCR	UIMB Module Configuration Register. See **Table 12-6** for bit descriptions.	32	H
0x30 7F84 — 0x30 7F8C	—	—	Reserved	32	H
0x30 7F90	S/T	UTSTCREG	UIMB Test Control Register. Reserved	32	H
0x30 7F94 — 0x30 7F9C	—	—	Reserved	32	H
0x30 7FA0	S	UIPEND	Pending Interrupt Request Register. See **12.5.3 Pending Interrupt Request Register (UIPEND)** and **Table 12-7** for bit descriptions.	32	H

NOTES:
1. S = Supervisor mode only, T = Test mode only

Table A-17 CALRAM_A and CALRAM_B Control Registers

Address	Access	Symbol	Register	Size	Reset
CALRAM_A					
0x38 0000	S	CRAMMCR_A	CALRAM_A Module Configuration Register. See **Table 21-3** for bit descriptions.	32	S
0x38 0004	S	CRAMTST_A	CALRAM_A Test Register.	32	S
0x38 0008	S	CRAM_RBA0_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 000C	S	CRAM_RBA1_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0010	S	CRAM_RBA2_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0014	S	CRAM_RBA3_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0018	S	CRAM_RBA4_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 001C	S	CRAM_RBA5_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0020	S	CRAM_RBA6_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S

Table A-17 CALRAM_A and CALRAM_B Control Registers (Continued)

Address	Access	Symbol	Register	Size	Reset
0x38 0024	S	CRAM_RBA7_A	CALRAM_A Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0028	S	CRAM_OLVCR_A	CALRAM_A Overlay Configuration Register. See **Table 21-7** for bit descriptions.	32	S
0x38 002C	S[1]	READI_OTR	READI Ownership Trace Register. See **23.2.1.1 User Mapped Register** for more information.	32	S
CALRAM_B					
0x38 0040	S	CRAMMCR_B	CALRAM_B Module Configuration Register. See **Table 21-3** for bit descriptions.	32	S
0x38 0044	S	CRAMTST_B	CALRAM_B Test Register. See **Table 21-3** for bit descriptions.	32	S
0x38 0048	S	CRAM_RBA0_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 004C	S	CRAM_RBA1_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0050	S	CRAM_RBA2_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0054	S	CRAM_RBA3_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0058	S	CRAM_RBA4_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 005C	S	CRAM_RBA5_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0060	S	CRAM_RBA6_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	15	S
0x38 0064	S	CRAM_RBA7_B	CALRAM_B Region Base Address Register. See **21.4.2 CALRAM Region Base Address Registers (CRAM_RBAx)** for more information.	32	S
0x38 0068	S	CRAM_OLVCR_B	CALRAM_A Overlay Configuration Register. See **Table 21-7** for bit descriptions.	32	S

Table A-17 CALRAM_A and CALRAM_B Control Registers (Continued)

Address	Access	Symbol	Register	Size	Reset
0x38 006C	S[1, 2]	CRAM_OTR_B	CALRAM_B Ownership Trace Register. See **21.4.4 CALRAM Ownership Trace Register (CRAMOTR)** for more information.	32	S

NOTES:
1. This register is write only.
2. This register is not used on the MPC565.

Table A-18 CALRAM_B and CALRAM_A Array

Address	Access	Symbol	Register	Size	Reset
CALRAM_B					
0x3F 7000 — 0x3F 7FFF	U,S	CRAM_B	CALRAM Array B.	4 Kbytes	—
CALRAM_A					
0x3F 8000 — 0x3F FFFF	U,S	CRAM_A	CALRAM Array A.	32 Kbytes	—