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EB274/D

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By Sharon Darley

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Motorola Semiconductor Engineering Bulletin

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General Information

Several steps must be followed to generate interrupts on a time processor unit (TPU) channel.

1. The first step is to store the starting address of the interrupt routine in an address in the CPU vector table.

   To calculate the appropriate address in the table, first choose a base vector number and write it to bits 7– 4 in the TPU interrupt configuration register (TICR). A base vector number is a hexadecimal number such as $6, $7, or $8. The base vector number is concatenated with the channel number to yield an interrupt vector number. For example, choosing a base vector number of $8 would assign interrupt vector $80 to channel 0, interrupt vector $81 to channel 1, interrupt vector $82 to channel 2, and so on through interrupt vector $8f to channel 15. Since this example uses channel 4, the interrupt vector is $84.

   The vector address is where the starting address of the interrupt routine is stored. It is determined from the vector number. For the MC68332, the vector address is calculated as four times the vector number plus the value in the vector base register. If the vector base register already has been initialized to $400 by CPU32Bug, then in this example the vector address is (4 x $84) +