SECTION 1
INTRODUCTION

The MPC509 is a member of the PowerPC Family of reduced instruction set computer (RISC) microcontrollers (MCUs). The MPC509 implements the 32-bit portion of the PowerPC™ architecture, which provides 32-bit effective addresses, integer data types of eight, 16, and 32 bits, and floating-point data types of 32 and 64 bits.

The RISC MCU processor (RCPU) integrates four execution units: an integer unit (IU), a load/store unit (LSU), a branch processing unit (BPU), and a floating-point unit (FPU). The RCPU is capable of issuing one sequential (non-branch) instruction per clock. In addition, branch instructions are evaluated ahead of time when possible, resulting in zero-cycle execution time for many branch instructions. Instructions can complete out of order for increased performance; however, the MPC509 makes them appear sequential.

The MPC509 includes an on-chip, 4-Kbyte, two-way set associative, physically addressed instruction cache, chip-select logic to reduce or eliminate external decoding logic, 28 Kbytes of static RAM, and extensive processor debugging functionality.

The MPC509 has a high-bandwidth, 32-bit data bus and a 32-bit address bus. The MCU supports 16-bit and 32-bit memories and both single-beat and burst data memory accesses.

The MPC509 is available in two TTL-compatible 5-V-friendly I/O configurations:

1. Operating temperature range -40°C to +85°C (part number MPC509L3C25).
2. Operating temperature range -40°C to +125°C (part number MPC509L3M25).

Reference **APPENDIX A MPC509 ELECTRICAL CHARACTERISTICS** for links to the electrical characteristics of these two configurations, described here in two separate documents.

1.1 Features

- Fully-integrated single-chip microcontroller
- RISC MCU central processing unit (RCPU)
  - — 32-bit PowerPC architecture
  - — Single-issue processor
  - — Integrated floating-point unit
  - — Branch prediction for prefetch
  - — 32 bit x 32 bit general-purpose register file
  - — 32 bit x 64 bit floating-point register file
  - — Precise exception model
  - — Internal Harvard architecture: load/store bus (L-Bus), instruction bus (I-Bus)
  - — PowerPC time base and decrementer
- System interface unit (SIU)

  - — Chip-select logic to reduce or eliminate external decoding logic
  - — External bus interface (EBI) that supports synchronous, asynchronous, burst transfer, and pipeline transfer memory types
  - — System protection features including bus monitor and periodic interrupt timer
  - — On-chip phase-locked loop (PLL), 16 MHz to 44 MHz
  - — Five dual-purpose I/O ports, two dual-purpose output ports
- Peripheral control unit (PCU)
  - — Software watchdog
  - — Interrupt controller to manage external and internal interrupts to the CPU
  - — Dual-purpose I/O port
  - — L-bus IMB interface (LIMB) connecting L-bus to intermodule bus 2 (IMB2)
- 4-Kbyte on-chip instruction cache (I-Cache)
- 28-Kbyte on-chip static data RAM (SRAM)
- 4.0-V supply voltage
- Tolerates input signals from 5-V peripherals

1.2 Block Diagram

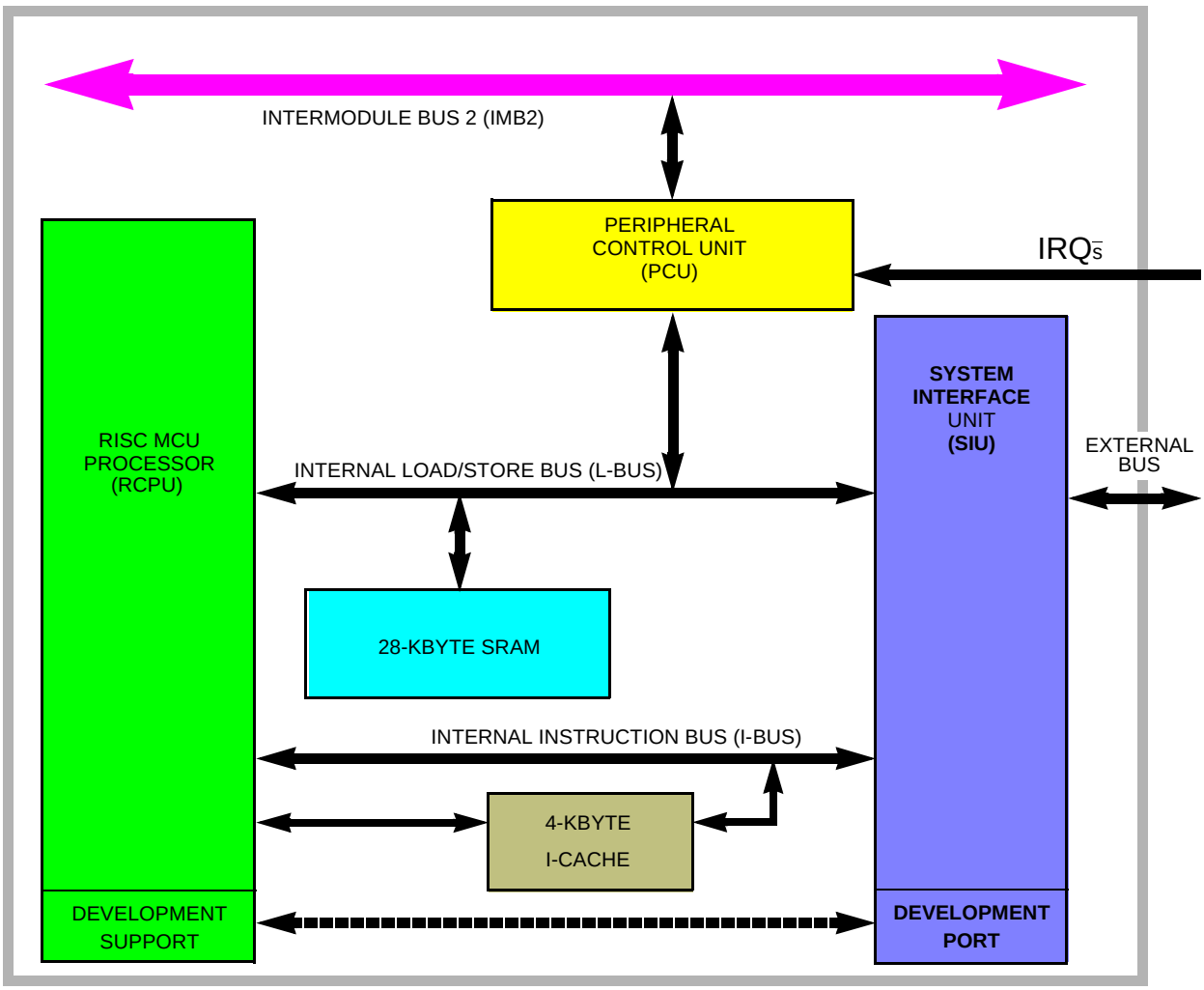

Figure 1-1 MPC509 Block Diagram

Notice in **Figure 1-1** that the IMB2 connects the processor to any on-chip peripherals. No such peripherals are present on the MPC509.

1.3 Pin Connections

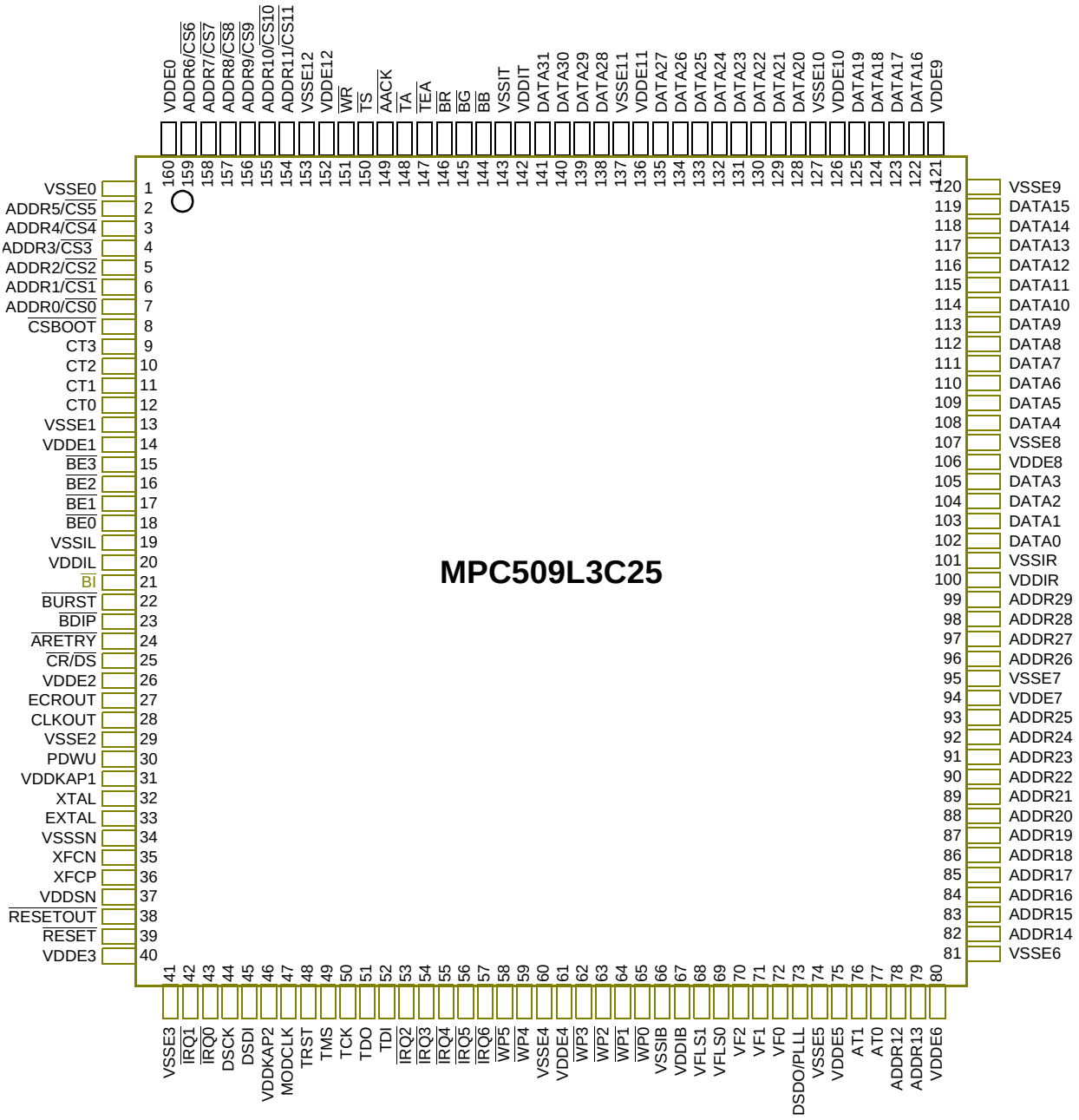

Figure 1-2 MPC509 Pin Assignments

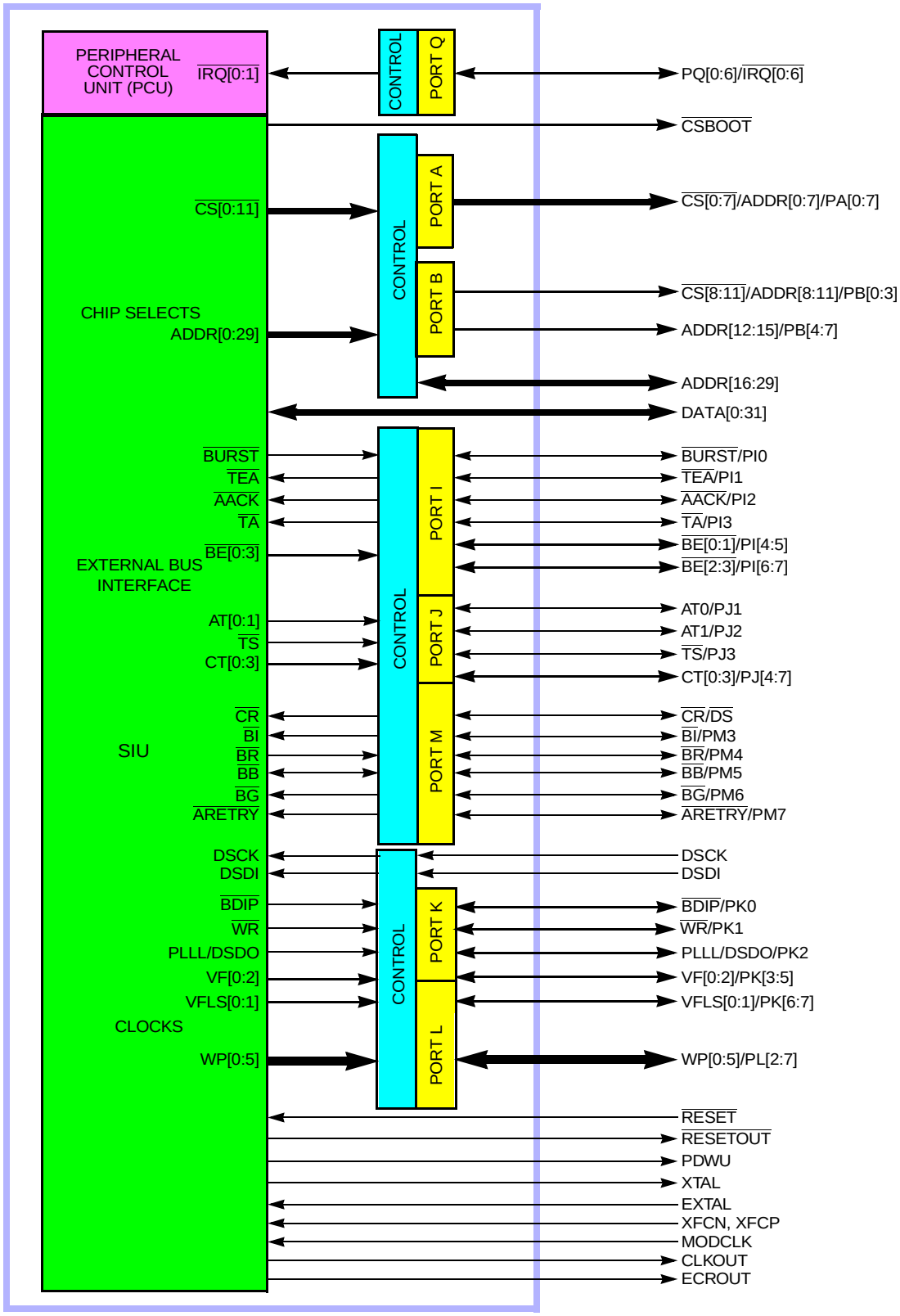

Figure 1-3 MPC509 Signals

1.4 Memory Map

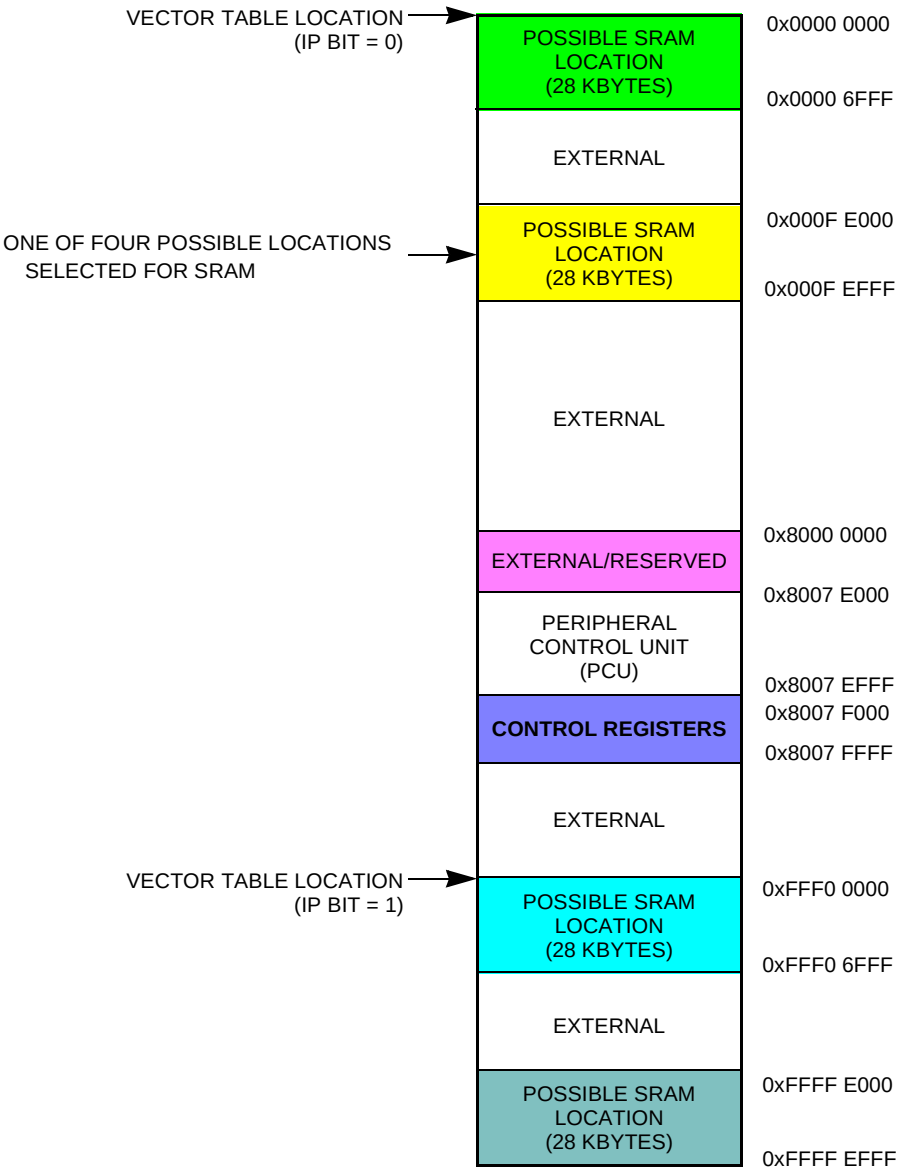

Figure 1-4 MPC509 Memory Map

The MPC family has a unified memory map including instruction memory (I-Mem), load/store memory (L-Mem), and all memory-mapped registers. I-Mem resides on the instruction bus; L-Mem resides on the load/store bus. The locations of I-Mem and L-Mem are selected in the MEMMAP register located in the SIU. In the MPC509, the SRAM module serves as L-Mem. The MPC509 has no I-Mem module.