SECTION 3
OVERVIEW

This section provides general information on the MC68332 MCU. It lists features of each of the modules, shows device functional divisions and pinouts, summarizes signal and pin functions, discusses the intermodule bus, and provides system memory maps. Timing and electrical specifications for the entire microcontroller and for individual modules are provided in **APPENDIX A ELECTRICAL CHARACTERISTICS**. Comprehensive module register descriptions and memory maps are provided in **APPENDIX D REGISTER SUMMARY**.

3.1 MCU Features

The following paragraphs highlight capabilities of each of the MCU modules. Each module is discussed separately in a subsequent section of this manual.

3.1.1 Central Processor Unit (CPU32)

- 32-bit architecture
- Virtual memory implementation
- Table look-up and interpolate instruction
- Improved exception handling for controller applications
- High level language support
- Background debug mode
- Fully static operation

3.1.2 System Integration Module(SIM)

- External bus support
- Programmable chip select outputs
- System protection logic
- Watchdog timer, clock monitor and bus monitor
- Two 8-bit dual function input/output ports
- One 7-bit dual function output port
- Phase-locked loop (PLL) clock system

3.1.3 Queued Serial Module (QSM)

- Enhanced serial communications interface (SCI)
- Modulus baud rate generator
- Parity detection
- Queued serial peripheral interface (QSPI)
- 80-byte static RAM to perform queued operations
- Up to 16 automatic transfers
- Continuous cycling, 8 to 16 bits per transfer, LSB or MSB first
- Dual function I/O pins

3.1.4 Time Processor Unit (TPU)

- Dedicated micro-engine operating independently of the CPU32
- 16 independent programmable channels and pins
- Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
- Any channel can perform any time function
- Each channel has six or eight 16-bit parameter registers
- Each timer function may be assigned to more than one channel
- Two timer counter registers with programmable prescalers
- Each channel can be synchronized to one or both counters
- Selectable channel priority levels

3.1.5 Static RAM Module with TPU Emulation Capability (TPURAM)

- 2 Kbytes of static RAM
- External V_{STBY} pin for separate standby supply
- May be used as normal RAM or TPU microcode emulation RAM

3.2 Intermodule Bus

The intermodule bus (IMB) is a standardized bus developed to facilitate both design and operation of modular microcontrollers. It contains circuitry to support exception processing, address space partitioning, multiple interrupt levels, and vectored interrupts. The standardized modules in the MCU communicate with one another through the IMB. The IMB in the MCU uses 24 address and 16 data lines.

3.3 System Block Diagram and Pin Assignment Diagrams

Figure 3-1 shows the functional block diagram of the MC68332. Although diagram blocks represent the relative size of the physical modules, there is not a one-to-one correspondence between location and size of blocks in the diagram and location and size of integrated-circuit modules.

Figures 3-2 and **3-3** show MC68332 pin assignments based on 132- and 144-pin plastic surface-mount packages. Refer to **APPENDIX B MECHANICAL DATA AND ORDERING INFORMATION** for information on obtaining package dimensions. Refer to subsequent paragraphs in this section for pin and signal descriptions.

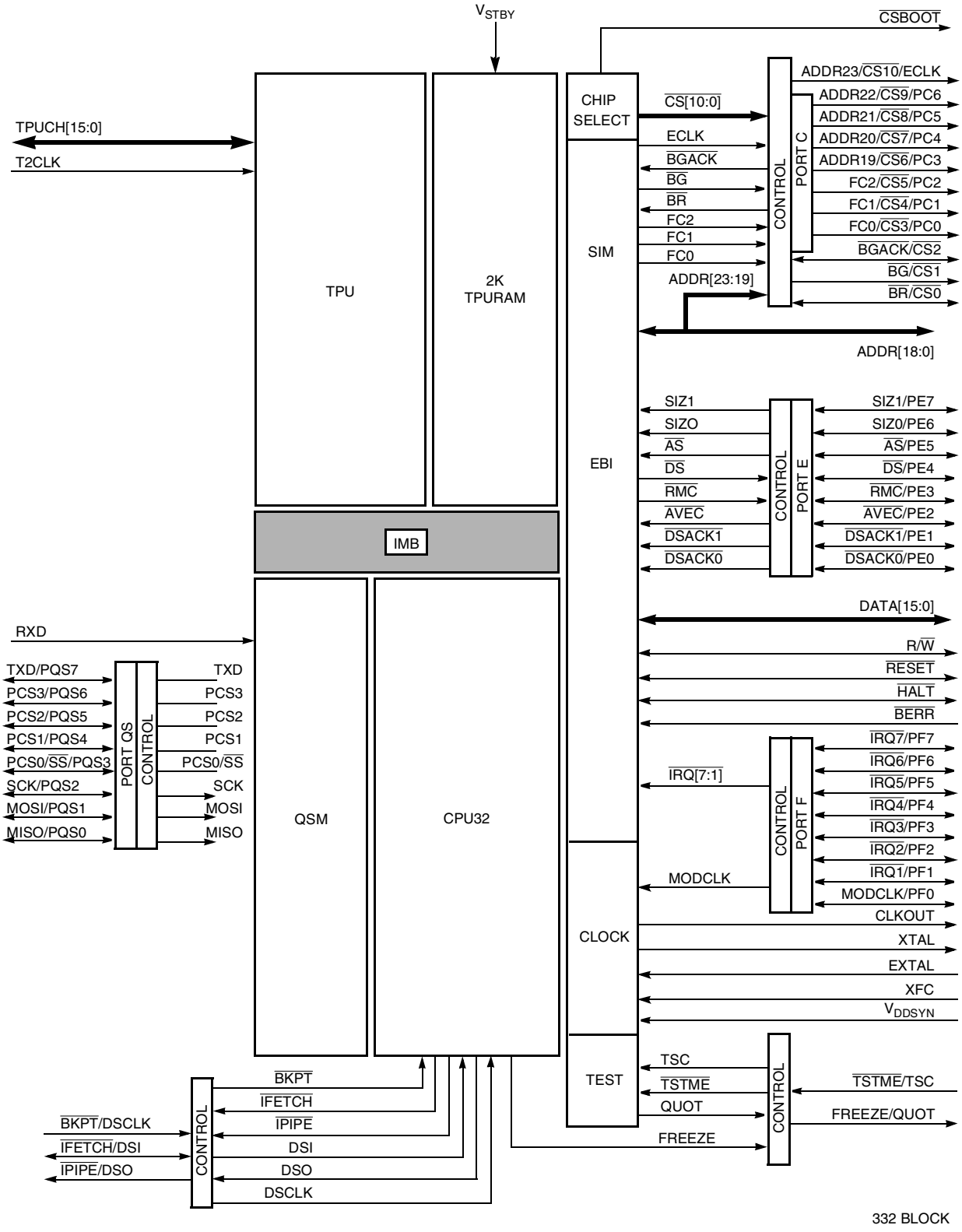
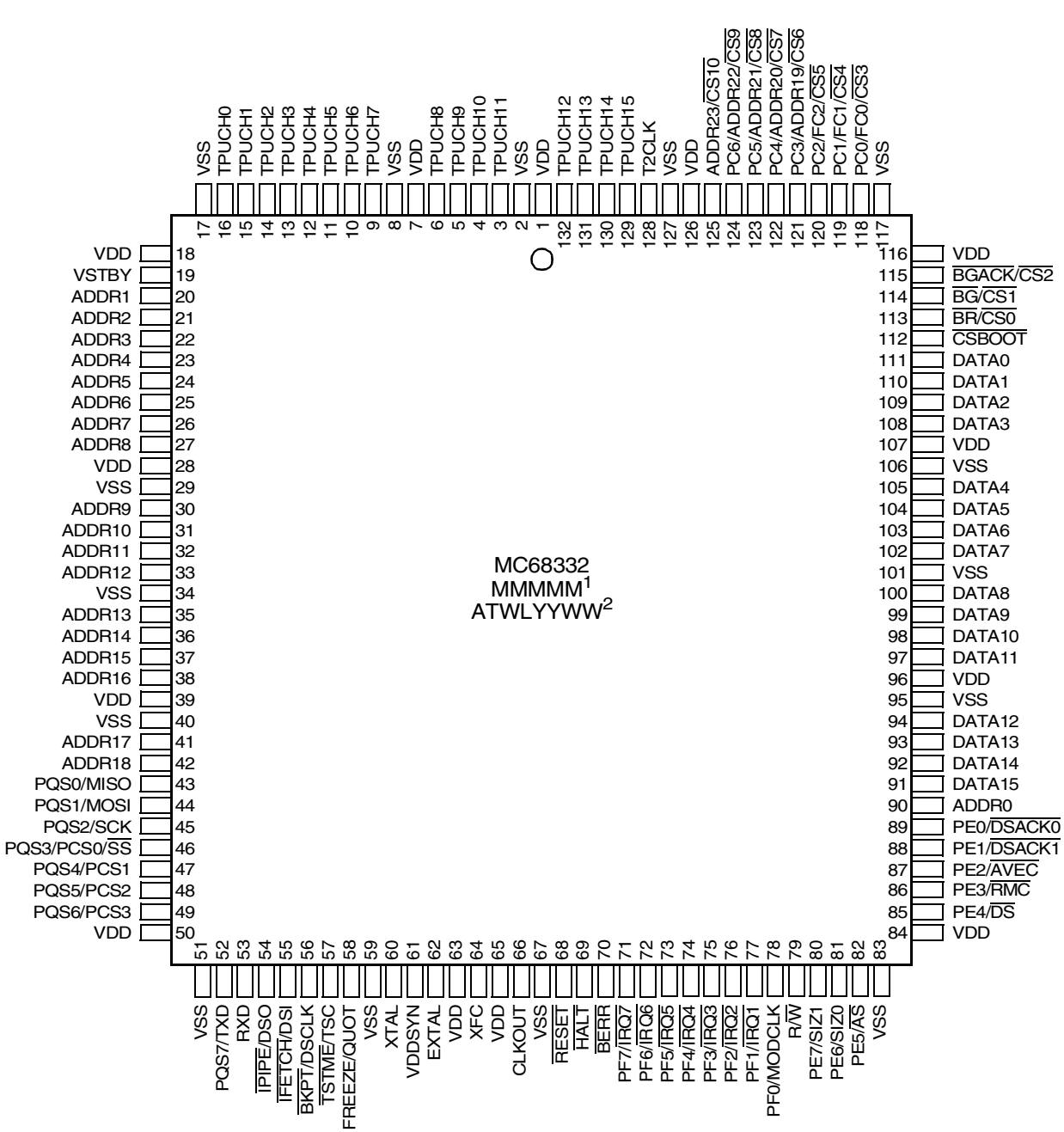


Figure 3-1 MC68332 Block Diagram



NOTES:
1. MMMMM = MASK OPTION NUMBER
2. ATWLYYWW = ASSEMBLY TEST LOCATION/YEAR, WEEK

332 132-PIN QFP

Figure 3-2 MC68332 Pin Assignments for 132-Pin Package

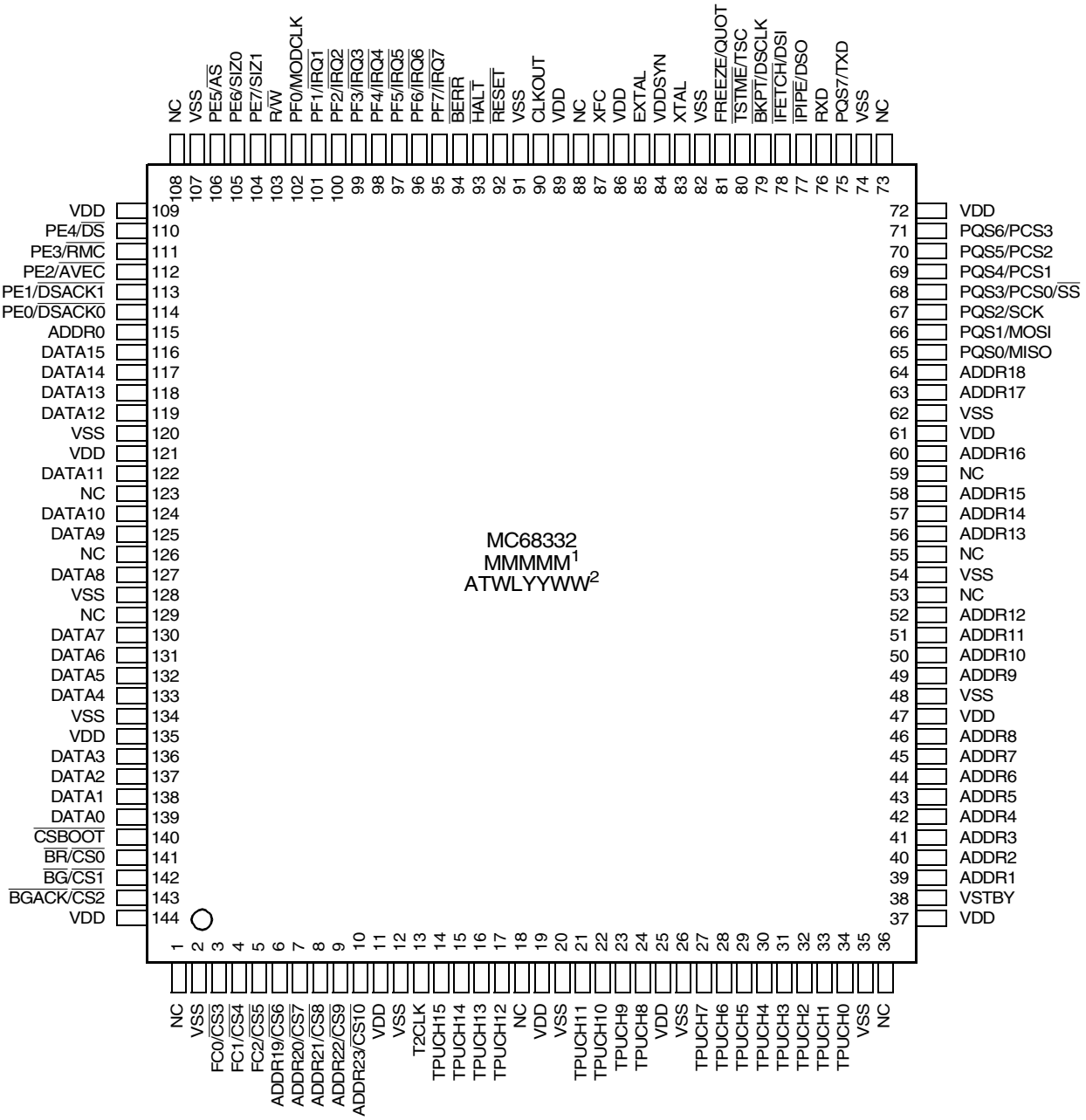


Figure 3-3 MC68332 Pin Assignments for 144-Pin Package

3.4 Pin Descriptions

Table 3-1 summarizes the pin characteristics of the MC68332 MCU. Entries in the "Associated Module" column indicate to which module individual pins belong. For MCU pins that can be outputs, the "Driver Type" column lists which output driver type is used. Table 3-2 briefly describes the four primary driver types. A "—" in the "Driver Type" column indicates either that the pin is an input only, and thus does not have a driver, or that the pin has a special driver, like the XTAL pin. Entries in the "Synchronized Input" and "Input Hysteresis" columns denote whether MCU pins that can be inputs are synchronized to the system clock and if they have hysteresis. Pins that are outputs only or that have special characteristics, like the EXTAL pin, have a "—" in these columns.

Table 3-1 MC68332 Pin Characteristics

Pin Mnemonic(s)	Pin Number(s)		Associated Module	Driver Type	Synchronized Input	Input Hysteresis
	132-Pin	144-Pin				
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15 ADDR16 ADDR17 ADDR18	90 20 21 22 23 24 25 26 27 30 31 32 33 35 36 37 38 41 42	115 39 40 41 42 43 44 45 46 49 50 51 52 56 57 58 60 63 64	SIM	A	—	—
ADDR19/$\overline{CS6}$/PC3 ADDR20/$\overline{CS7}$/PC4 ADDR21/$\overline{CS8}$/PC5 ADDR22/$\overline{CS9}$/PC6	121 122 123 124	6 7 8 9	SIM	A	—	—
ADDR23/$\overline{CS10}$/ECLK	125	10	SIM	A	—	—
$\overline{AS}$/PE5	82	106	SIM	B	Y	Y
$\overline{AVEC}$/PE2	87	112	SIM	B	Y	N
$\overline{BERR}$	70	94	SIM	—	Y[1]	N
$\overline{BG}$/$\overline{CS1}$	114	142	SIM	B	—	—
$\overline{BGACK}$/$\overline{CS2}$	115	143	SIM	B	Y	N
$\overline{BKPT}$/DSCLK	56	79	CPU32	—	Y	Y
$\overline{BR}$/$\overline{CS0}$	113	141	SIM	B	Y	N
CLKOUT	66	90	SIM	A	—	—
$\overline{CSBOOT}$	112	140	SIM	B	—	—

Table 3-1 MC68332 Pin Characteristics (Continued)

Pin Mnemonic(s)	Pin Number(s)		Associated Module	Driver Type	Synchronized Input	Input Hysteresis
	132-Pin	144-Pin				
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 DATA8 DATA9 DATA10 DATA11 DATA12 DATA13 DATA14 DATA15	111 110 109 108 105 104 103 102 100 99 98 97 94 93 92 91	139 138 137 136 133 132 131 130 127 125 124 122 119 118 117 116	SIM	Aw	Y[2]	Y
$\overline{DS}$/PE4	85	110	SIM	B	Y	Y
$\overline{DSACK0}$/PE0 $\overline{DSACK1}$/PE1	89 88	114 113	SIM	B	Y	N
EXTAL[3]	62	85	SIM	—	—	—
FC0/$\overline{CS3}$/PC0	118	3	SIM	A	—	—
FC1/$\overline{CS4}$/PC1	119	4	SIM	A	—	—
FC2/$\overline{CS5}$/PC2	120	5	SIM	A	—	—
FREEZE/QUOT	58	81	SIM	A	—	—
$\overline{HALT}$	69	93	SIM	Bo	Y[1]	N
$\overline{IPIPE}$/DSO	54	77	CPU32	A	—	—
$\overline{IFETCH}$/DSI	55	78	CPU32	A	Y	Y
$\overline{IRQ1}$/PF1 $\overline{IRQ2}$/PF2 $\overline{IRQ3}$/PF3 $\overline{IRQ4}$/PF4 $\overline{IRQ5}$/PF5 $\overline{IRQ6}$/PF6 $\overline{IRQ7}$/PF7	77 76 75 74 73 72 71	101 100 99 98 97 96 95	SIM	B	Y	Y
MISO/PQS0	43	65	QSM	Bo	Y[4]	Y
MODCLK/PF0	78	102	SIM	B	Y[2]	Y
MOSI/PQS1	44	66	QSM	Bo	Y[4]	Y
PCS3/PQS6 PCS2/PQS5 PCS1/PQS4	49 48 47	71 70 69	QSM	—	Y	Y
R/$\overline{W}$	79	103	SIM	A	—	—
$\overline{RESET}$	68	92	SIM	Bo	Y	Y
RMC/PE3	86	111	SIM	B	Y	N
RXD	53	76	QSM	—	N	N
SCK/PQS2	45	67	QSM	Bo	Y[4]	Y

Table 3-1 MC68332 Pin Characteristics (Continued)

Pin Mnemonic(s)	Pin Number(s)		Associated Module	Driver Type	Synchronized Input	Input Hysteresis
	132-Pin	144-Pin				
SIZ0/PE6 SIZ1/PE7	81 80	105 104	SIM	B	Y	Y
$\overline{SS}$/PCS0/PQS3	46	68	QSM	Bo	Y[4]	Y
TSC	57	80	SIM	—	Y	Y
TXD/PQS7	52	75	QSM	Bo	Y	Y
V_{DD}	1 7 18 28 39 50 63 65 84 96 107 116 126	11 19 25 37 47 61 72 86 89 109 121 135 144	—	—	—	—
V_{DDSYN}	61	84	SIM	—	—	—
V_{SS}	2 8 17 29 34 40 51 59 67 83 95 101 106 117 127	2 12 20 26 35 48 54 62 74 82 91 107 120 128 134	—	—	—	—
XFC[3]	64	87	SIM	—	—	—
XTAL[3]	60	83	SIM	—	—	—

NOTES:

1. $\overline{BERR}$ is only synchronized when executing retry or late bus cycle operations. $\overline{HALT}$ is only synchronized when executing retry or single-step bus cycle operations.
2. DATA[15:0] are only synchronized during reset. MODCLK is only synchronized when used as an input port pin.
3. EXTAL, XFC, and XTAL are clock connections.
4. MISO/PQS0, MOSI/PQS1, SCK/PQS2, and $\overline{SS}$/PQS3 inputs are only synchronized when used as discrete general-purpose inputs.

Table 3-2 MC68332 Driver Types

Type	I/O	Description
A	O	Three-state capable output signals
Aw	O	Type A output with weak p-channel pullup during reset
B	O	Three-state output that includes circuitry to pull up output before high impedance is established, to ensure rapid rise time
Bo	O	Type B output that can be operated in an open-drain mode

3.5 Signal Descriptions

Table 3-3 summarizes pin functions of the MC68332 MCU. Entries in the "Active State(s)" column denote the polarity of each MCU pin in its active state. Some MCU pins have multiple functions and thus have multiple entries in the "Active State(s)" column. For example, the ADDR23/$\overline{\text{CS10}}$/ECLK pin can be programmed to be either address line 23 (ADDR23), chip-select output 10 ($\overline{\text{CS10}}$), or the M6800 bus clock (ECLK). Its entry in the "Active State(s)" column is "—/0/—" which indicates the following:

- When programmed as ADDR23, the pin has no active state ("—"); it conveys information when driven by the MCU to logic 0 or logic 1.
- When programmed as $\overline{\text{CS10}}$, the pin is active when driven to logic 0 ("0") by the MCU. When driven to logic 1, the chip-select function is inactive.
- When programmed as ECLK, the pin has no active state ("—"). M6800 bus devices drive or prepare to latch an address when ECLK is logic 0 and drive or prepare to latch data when ECLK is logic 1.

The "Discrete I/O Use" column indicates whether each pin can be used as a general purpose input, output, or both. Those pins that cannot be used for general purpose I/O will have a "—" in this column.

Table 3-3 MC68332 Pin Functions

Pin Mnemonic(s)	Pin Number(s)		Active State(s)	Associated Module	Description	Discrete I/O Use
	132-Pin	144-Pin				
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15 ADDR16 ADDR17 ADDR18	90 20 21 22 23 24 25 26 27 30 31 32 33 35 36 37 38 41 42	115 39 40 41 42 43 44 45 46 49 50 51 52 56 57 58 60 63 64	—	SIM	Address lines [18:0]	—
ADDR19/$\overline{CS6}$/PC3 ADDR20/$\overline{CS7}$/PC4 ADDR21/$\overline{CS8}$/PC5 ADDR22/$\overline{CS9}$/PC6	121 122 123 124	6 7 8 9	—/0/—	SIM	Address lines [22:19], chip-select outputs [9:6], or digital output port C [6:3].	O
ADDR23/$\overline{CS10}$/ECLK	125	10	—/0/—	SIM	Address line 23, chip-select output 10, or E clock output for M6800 bus devices.	—
$\overline{AS}$/PE5	82	106	0/—	SIM	Indicates that a valid address is on the address bus or digital I/O port E5.	I/O
$\overline{AVEC}$/PE2	87	112	0/—	SIM	Requests an automatic vector during interrupt acknowledge or port E 2.	I
$\overline{BERR}$	70	94	0	SIM	Requests a bus error exception.	—
$\overline{BG}$/$\overline{CS1}$	114	142	0/0	SIM	Bus granted output or chip-select output 1.	—
$\overline{BGACK}$/$\overline{CS2}$	115	143	0/0	SIM	Bus grant acknowledge input or chip-select output 2.	—
$\overline{BKPT}$/DSCLK	56	79	0/—	CPU32	Hardware breakpoint input or background debug mode serial data clock input.	—
$\overline{BR}$/$\overline{CS0}$	113	141	0/0	SIM	Bus request input or chip-select output 0.	—
CLKOUT	66	90	—	SIM	System clock output.	—
$\overline{CSBOOT}$	112	140	0	SIM	Boot memory device chip-select output.	—

Table 3-3 MC68332 Pin Functions (Continued)

Pin Mnemonic(s)	Pin Number(s)		Active State(s)	Associated Module	Description	Discrete I/O Use
	132-Pin	144-Pin				
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 DATA8 DATA9 DATA10 DATA11 DATA12 DATA13 DATA14 DATA15	111 110 109 108 105 104 103 102 100 99 98 97 94 93 92 91	139 138 137 136 133 132 131 130 127 125 124 122 119 118 117 116	—	SIM	Data bus lines [15:0]	—
$\overline{DS}$/PE4	85	110	0/—	SIM	Indicates that an external device should place valid data on the bus during a read cycle, that valid data has been placed on the bus during a write cycle, or the pin is digital I/O port E4.	I/O
$\overline{DSACK0}$/PE0 $\overline{DSACK1}$/PE1	89 88	114 113	0/—	SIM	Data size and acknowledge inputs or digital I/O ports E [1:0].	I/O
EXTAL	62	85	—	SIM	Crystal oscillator or external clock input.	—
FC0/$\overline{CS3}$/PC0	118	3	—/0/—	SIM	Function code output 0, chip-select output 3, or digital output port C0.	O
FC1/$\overline{CS4}$/PC1	119	4	—/—	SIM	Function code output 1, chip-select output 4 (MC68HC16Y3 only), or digital output port C1.	O
FC2/$\overline{CS5}$/PC2	120	5	—/0/—	SIM	Function code output 2, chip-select output 5, or digital output port C2.	O
FREEZE/QUOT	58	81	1/—	SIM	Indicates that the CPU32 has entered background debug mode or provides the quotient bit of the polynomial divider in test mode.	—
$\overline{HALT}$	69	93	0	SIM	Suspends bus activity.	—
$\overline{IPIPE}$/DSO	54	77	—/—	CPU32	Instruction pipeline state output or background debug mode serial data output.	—
$\overline{IFETCH}$/DSI	55	78	—/—	CPU32	Instruction pipeline state output or background debug mode serial data input.	—

Table 3-3 MC68332 Pin Functions (Continued)

Pin Mnemonic(s)	Pin Number(s)		Active State(s)	Associated Module	Description	Discrete I/O Use
	132-Pin	144-Pin				
$\overline{IRQ1}$/PF1 $\overline{IRQ2}$/PF2 $\overline{IRQ3}$/PF3 $\overline{IRQ4}$/PF4 $\overline{IRQ5}$/PF5 $\overline{IRQ6}$/PF6 $\overline{IRQ7}$/PF7	77 76 75 74 73 72 71	101 100 99 98 97 96 95	0/—	SIM	External interrupt request inputs [7:1] or digital I/O port F [7:1].	I/O
MISO/PQS0	43	65	—	QSM	Serial input to QSPI in master mode and serial output from QSPI in slave mode or port QS 0.	I/O
MODCLK/PF0	78	102	1/—	SIM	Phase-locked loop reference select input or digital I/O port F0.	I/O
MOSI/PQS1	44	66	—	QSM	Serial output from QSPI in master mode and serial input from QSPI in slave mode or port QS 1.	I/O
PCS3/PQS6 PCS2/PQS5 PCS1/PQS4	49 48 47	71 70 69	—	QSM	Peripheral chip selects [3:1], or port QS [6:4].	I/O
R/$\overline{W}$	79	103	1/0	SIM	Indicates a data bus read when high and a data bus write when low.	—
$\overline{RESET}$	68	92	0	SIM	System reset.	—
RMC/PE3	86	111	0/—	SIM	Indicates an indivisible read-modify-write instruction or port E 3.	O
RXD	53	76	—	QSM	Serial input to the SCI.	I
SCK/PQS2	45	67	—	QSM	Clock output from QSPI in master mode and clock input to the QSPI in slave mode or port QS 2.	I/O
SIZ0/PE6 SIZ1/PE7	81 80	105 104	—/—	SIM	Data transfer size outputs or digital I/O ports E [7:6].	I/O
$\overline{SS}$/PCS0/PQS3	46	68	0/—	QSM	SPI slave select input or digital I/O port QS3.	I/O
TSC	57	80	1	SIM	Three-state control	—
TXD/PQS7	52	75	—	QSM	Serial output from the SCI or port QS 7.	O

Table 3-3 MC68332 Pin Functions (Continued)

Pin Mnemonic(s)	Pin Number(s)		Active State(s)	Associated Module	Description	Discrete I/O Use
	132-Pin	144-Pin				
V_{DD}	1 7 18 28 39 50 63 65 84 96 107 116 126	11 19 25 37 47 61 72 86 89 109 121 135 144	—	—	Digital supply voltage inputs.	—
V_{DDSYN}	61	84	—/1	SIM	Clock synthesizer power supply input.	—
V_{SS}	2 8 17 29 34 40 51 59 67 83 95 101 106 117 127	2 12 20 26 35 48 54 62 74 82 91 107 120 128 134	—	—	Digital ground reference.	—
XFC	64	87	—	SIM	Clock synthesizer filter connection.	—
XTAL	60	83	—	SIM	Crystal oscillator output.	—

3.6 Internal Register Maps

In **Figure 3-4**, IMB ADDR[23:20] are represented by the letter Y. The value represented by Y determines the base address of MCU module control registers. Y is equal to M111, where M is the logic state of the module mapping (MM) bit in the system integration module configuration register (SIMCR).

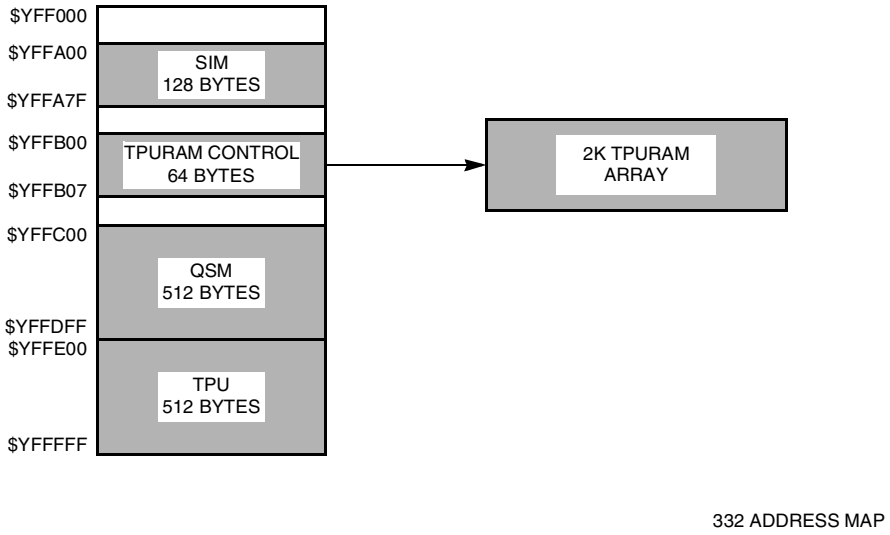
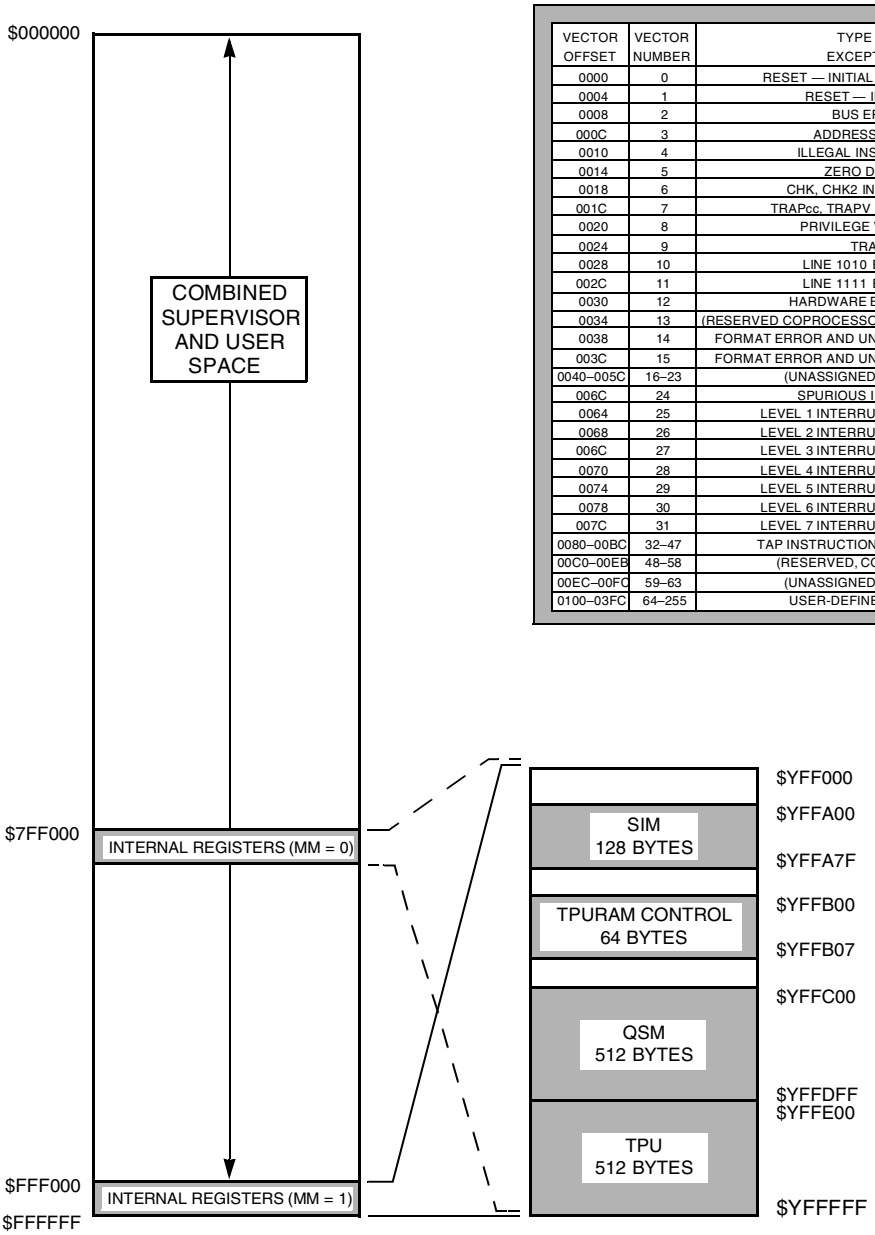


Figure 3-4 MC68332 Address Map

3.7 Address Space Maps

Figure 3-5 shows a single memory space. Function codes FC[2:0] are not decoded externally so that separate user/supervisor or program/data spaces are not provided. In **Figure 3-6**, FC2 is decoded, resulting in separate supervisor and user spaces. FC[1:0] are not decoded, so that separate program and data spaces are not provided. In **Figure 3-7** and **Figure 3-8**, FC[2:0] are decoded, resulting in four separate memory spaces: supervisor/program, supervisor/data, user/program and user/data.

All exception vectors are located in supervisor data space, except the reset vector, which is located in supervisor program space. Only the initial reset vector is fixed in the processor's memory map. Once initialization is complete, there are no fixed assignments. Since the vector base register (VBR) provides the base address of the vector table, the vector table can be located anywhere in memory. Refer to **SECTION 4 CENTRAL PROCESSOR UNIT** for more information concerning memory management, extended addressing, and exception processing. Refer to **SECTION 5 SYSTEM INTEGRATION MODULE** for more information concerning function codes and address space types.



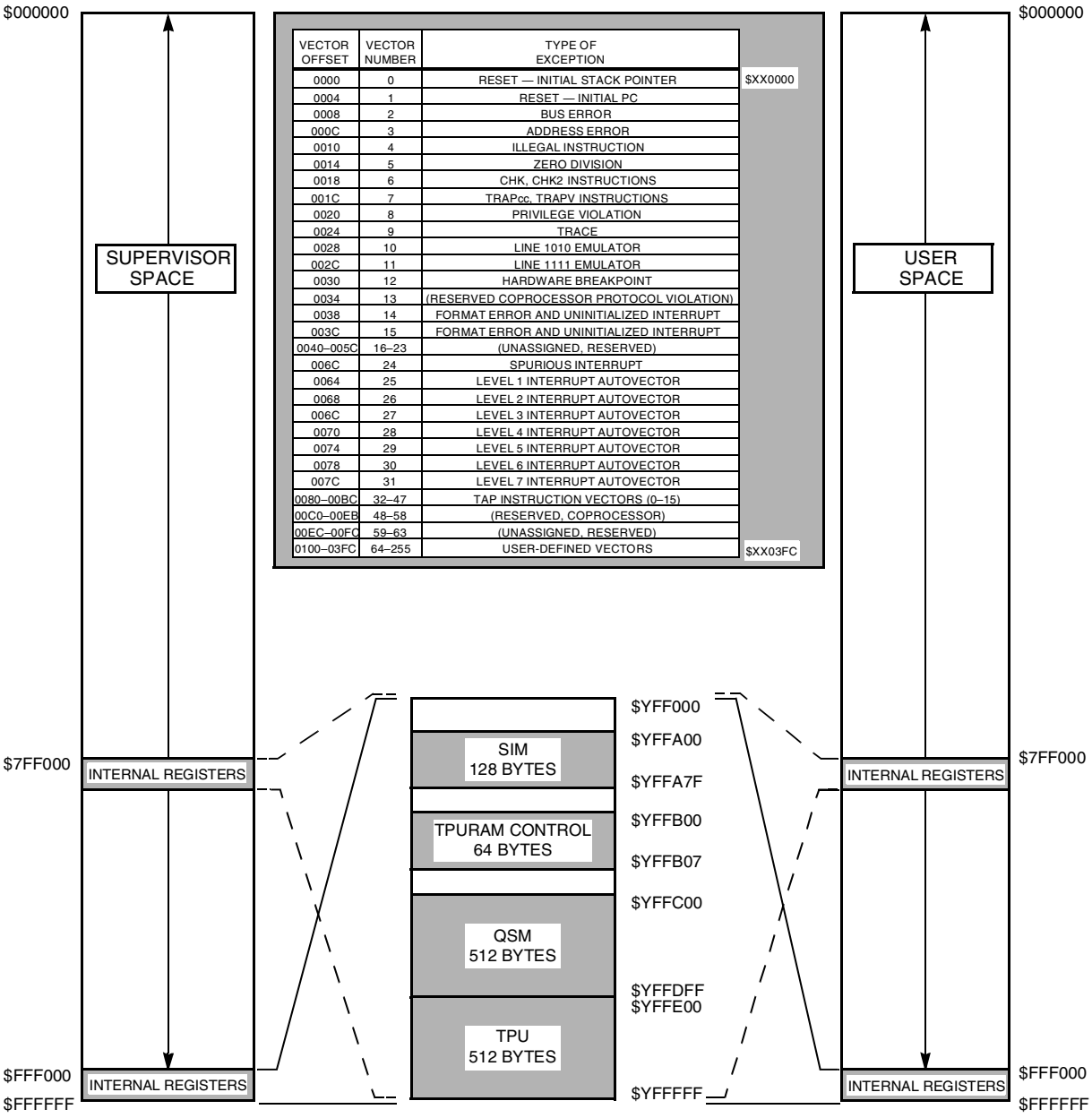
VECTOR OFFSET	VECTOR NUMBER	TYPE OF EXCEPTION	
0000	0	RESET — INITIAL STACK POINTER	$XX0000
0004	1	RESET — INITIAL PC	
0008	2	BUS ERROR	
000C	3	ADDRESS ERROR	
0010	4	ILLEGAL INSTRUCTION	
0014	5	ZERO DIVISION	
0018	6	CHK, CHK2 INSTRUCTIONS	
001C	7	TRAPcc, TRAPV INSTRUCTIONS	
0020	8	PRIVILEGE VIOLATION	
0024	9	TRACE	
0028	10	LINE 1010 EMULATOR	
002C	11	LINE 1111 EMULATOR	
0030	12	HARDWARE BREAKPOINT	
0034	13	(RESERVED COPROCESSOR PROTOCOL VIOLATION)	
0038	14	FORMAT ERROR AND UNINITIALIZED INTERRUPT	
003C	15	FORMAT ERROR AND UNINITIALIZED INTERRUPT	
0040–005C	16–23	(UNASSIGNED, RESERVED)	
006C	24	SPURIOUS INTERRUPT	
0064	25	LEVEL 1 INTERRUPT AUTOVECTOR	
0068	26	LEVEL 2 INTERRUPT AUTOVECTOR	
006C	27	LEVEL 3 INTERRUPT AUTOVECTOR	
0070	28	LEVEL 4 INTERRUPT AUTOVECTOR	
0074	29	LEVEL 5 INTERRUPT AUTOVECTOR	
0078	30	LEVEL 6 INTERRUPT AUTOVECTOR	
007C	31	LEVEL 7 INTERRUPT AUTOVECTOR	
0080–00BC	32–47	TAP INSTRUCTION VECTORS (0–15)	
00C0–00EB	48–58	(RESERVED, COPROCESSOR)	
00EC–00FC	59–63	(UNASSIGNED, RESERVED)	
0100–03FC	64–255	USER-DEFINED VECTORS	$XX03FC

NOTES:

1. LOCATION OF THE EXCEPTION VECTOR TABLE IS DETERMINED BY THE VECTOR BASE REGISTER. THE VECTOR ADDRESS IS THE CONCATENATION OF THE UPPER 22 BITS OF THE VBR WITH THE 8-BIT VECTOR NUMBER OF THE INTERRUPTING MODULE. THE RESULT IS LEFT JUSTIFIED TO FORCE LONG WORD ALIGNMENT.
2. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111 WHERE M IS THE STATE OF THE MM BIT.
3. SOME UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. REFER TO THE APPROPRIATE MODULE REFERENCE MANUAL FOR INFORMATION ON MAPPING OF UNUSED ADDRESSES WITHIN INTERNAL REGISTER BLOCKS.

332 S/U COMB MAP

Figure 3-5 Overall Memory Map

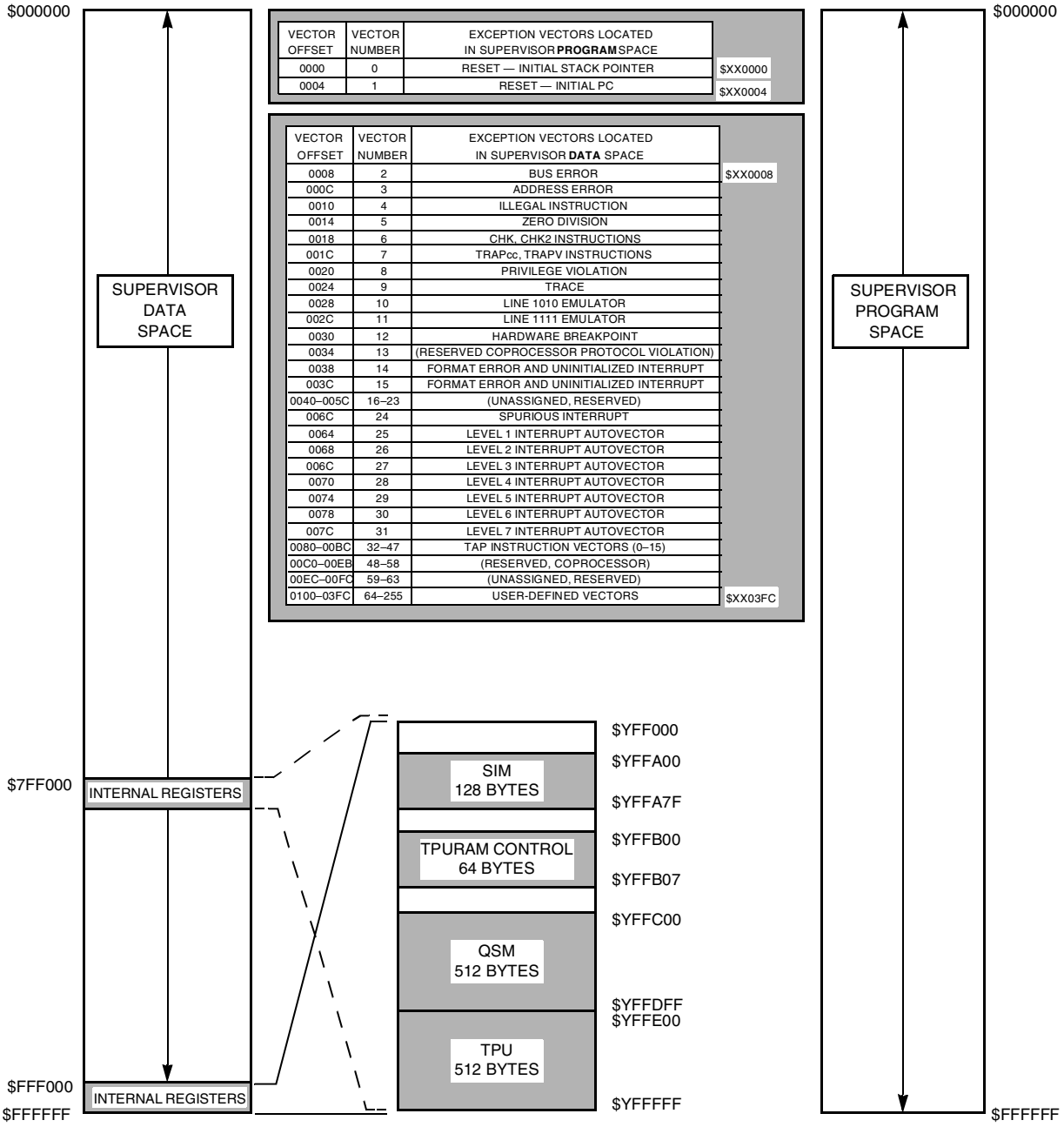


NOTES:

1. LOCATION OF THE EXCEPTION VECTOR TABLE IS DETERMINED BY THE VECTOR BASE REGISTER. THE VECTOR ADDRESS IS THE CONCATENATION OFTHE UPPER 22 BITS OF THE VBR WITH THE 8-BIT VECTOR NUMBER OF THE INTERRUPTING MODULE. THE RESULT IS LEFT JUSTIFIED TO FORCE LONG WORD ALIGNMENT.
2. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111 WHERE M IS THE STATE OF THE MM BIT.
3. SOME UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. REFER TO THE APPROPRIATE MODULE REFERENCE MANUAL FOR INFORMATION ON MAPPING OF UNUSED ADDRESSES WITHIN INTERNAL REGISTER BLOCKS.
4. SOME INTERNAL REGISTERS ARE NOT AVAILABLE IN USER SPACE.

332 S/U SEP MAP

Figure 3-6 Separate Supervisor and User Space Map

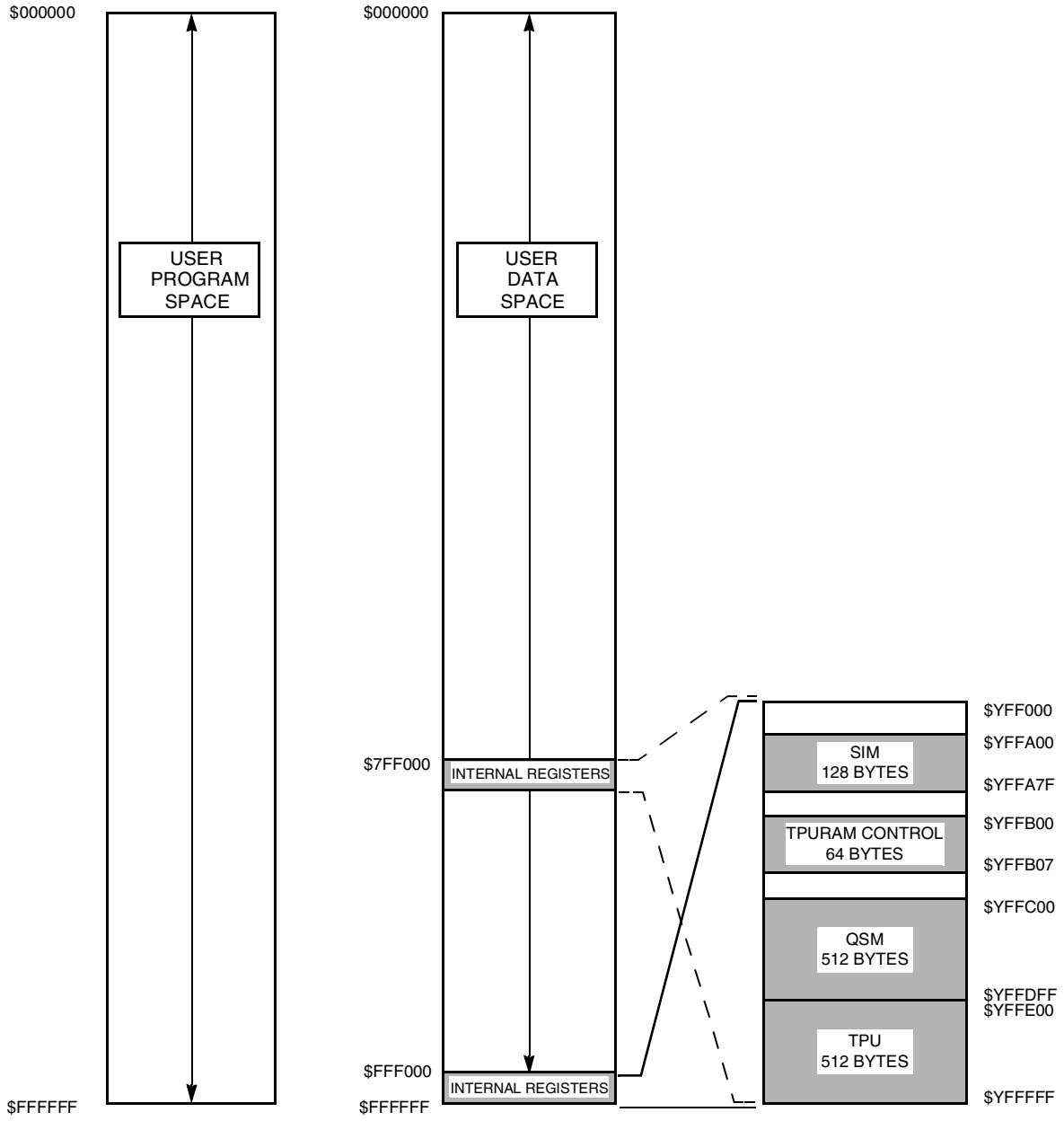


NOTES:

1. LOCATION OF THE EXCEPTION VECTOR TABLE IS DETERMINED BY THE VECTOR BASE REGISTER. THE VECTOR ADDRESS IS THE CONCATENATION OF THE UPPER 22 BITS OF THE VBR WITH THE 8-BIT VECTOR NUMBER OF THE INTERRUPTING MODULE. THE RESULT IS LEFT JUSTIFIED TO FORCE LONG WORD ALIGNMENT.
2. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111 WHERE M IS THE STATE OF THE MM BIT.
3. SOME UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. REFER TO THE APPROPRIATE MODULE REFERENCE MANUAL FOR INFORMATION ON MAPPING OF UNUSED ADDRESSES WITHIN INTERNAL REGISTER BLOCKS.
4. SOME INTERNAL REGISTERS ARE NOT AVAILABLE IN USER SPACE.

332 SUPER P/D MAP

Figure 3-7 Supervisor Space (Separate Program/Data Space) Map



NOTES:

1. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111, WHERE M IS THE STATE OF THE MM BIT.
2. UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. "RESERVED" BLOCKS ARE NOT MAPPED EXTERNALLY.
3. SOME INTERNAL REGISTERS ARE NOT AVAILABLE IN USER SPACE.

332 USER P/D MAP

Figure 3-8 User Space (Separate Program/Data Space) Map