# SECTION 7
# STATIC RAM MODULE

The static RAM (SRAM) module consists of a 28-Kbyte block of static RAM. The primary function of this module is to serve as fast (one-cycle access), general-purpose RAM for the MCU. The SRAM can be read or written as either bytes, half-words or words.

The bus interface and control logic for the SRAM module are powered by $V_{DD}$. A separate pin, VDDKAP2, supplies power to the memory arrays. If main power is shut off, VDDKAP2 can be maintained in order to retain the data in the SRAM array. When the main power is off, access to the SRAM array is blocked.

## 7.1 Features

- Fast, one-cycle access
- Low-power mode
  - — Two-cycle access
  - — Pipelined for back-to-back accesses
- Programmable attributes (supervisor only, data only, read only)

## 7.2 Placement of SRAM in Memory Map

The SRAM module consists of two separately addressable sections. The first is the array itself. The second section is a set of registers used for configuration and testing of the SRAM array.

The SRAM array is assigned to one of four locations in the MCU address map by programming the LMEMBASE field in the SIU internal memory mapping register (MEMMAP).

**NOTE**

The user must reserve the entire 32-Kbyte block containing the selected 28-Kbyte block of SRAM. **Table 7-1** indicates the location of the SRAM array and the associated reserved locations for each value of LMEMBASE.

**Table 7-1 MPC509 SRAM Module Addresses**

| LMEMBASE | SRAM Location | Reserved Location |
|---|---|---|
| 00 | 0x0000 0000 – 0x0000 6FFF | 0x0000 7FFF – 0x0000 7FFF |
| 01 | 0x000F 8000 – 0x000F EFFF | 0x000F F000 – 0x000F FFFF |
| 10 | 0xFFF0 0000 – 0xFFF0 6FFF | 0xFFF0 7FFC – 0xFFF0 7FFF |
| 11 | 0xFFFF 8000 – 0xFFFF EFFF | 0xFFFF F000 – 0xFFFF FFFF |

Refer to **5.3 SIU Module Configuration** for a diagram of the MEMMAP register.

**Figure 7-1**, a memory map of the MPC509, shows the possible locations of the SRAM array.

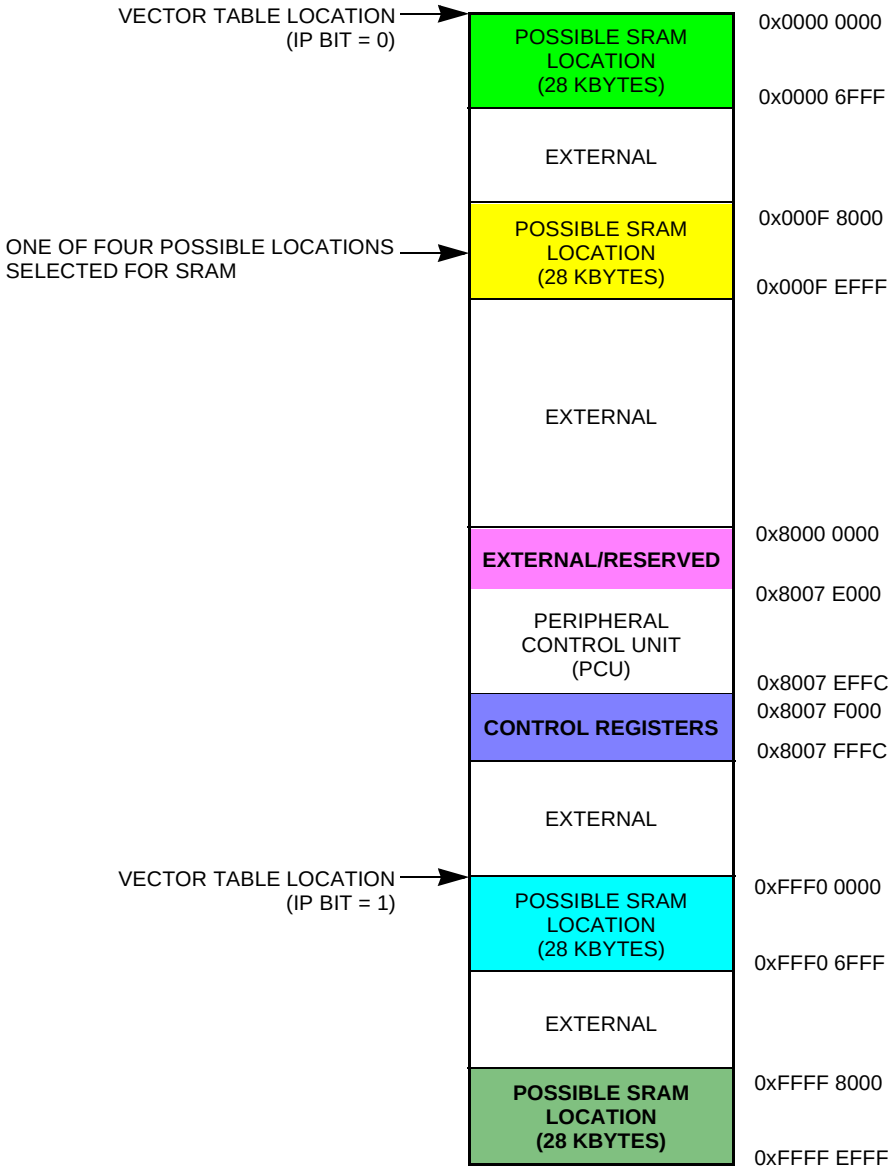


**Figure 7-1 Placement of Internal SRAM in Memory Map**

## 7.3 SRAM Registers

The control block for the SRAM module contains one control register for configuring the array and one control register for use in testing.

**SRAMMCR —** SRAM Module Configuration Register **0x8007 F000**

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LCK | DIS | 2CY | RESERVED | | | | | | | | | | | | |
| RESET: | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | R0 | D0 | S0 | RESERVED | | | | | | | | |
| RESET: | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Each SRAM module configuration register contains bits for setting access rights to the array. **Table 7-2** provides definitions for the bits.

**Table 7-2 SRAMMCR Bit Settings**

| Bit(s) | Name | Description |
|---|---|---|
| 0 | LCK | Lock bit<br>0 = Writes to the SRAMMCR are accepted.<br>1 = Writes to the SRAMMCR are ignored. |
| 1 | DIS | Module disable<br>0 = SRAM module is enabled.<br>1 = SRAM module is disabled. Module can be subsequently re-enabled by software setting this bit or by reset. Attempts to read SRAM array when it is disabled result in internal $\overline{\text{TEA}}$ assertion. |
| 2 | 2CY | Two-cycle mode<br>0 = SRAM module is in single-cycle mode (normal operation).<br>1 = SRAM module is in two-cycle mode. In this mode, the first cycle is used for decoding the address, and the second cycle is used for accepting or providing data. This mode provides some power savings while keeping the memory active. |
| 3:19 | — | Reserved |
| 20 | R0 | Read only<br>0 = 4-Kbyte block is readable and writable.<br>1 = 4-Kbyte block is read only. Attempts to write to this space result in internal $\overline{\text{TEA}}$ assertion. |
| 21 | D0 | Data only<br>0 = 4-Kbyte block can contain data or instructions.<br>1 = 4-Kbyte block contains data only. Attempts to load instructions from this space result in internal $\overline{\text{TEA}}$ assertion. |
| 22 | S0 | Supervisor only<br>0 = 4-Kbyte block is placed in unrestricted space.<br>1 = 4-Kbyte block is placed in supervisor space. Attempts to access this space from the user privilege level result in internal $\overline{\text{TEA}}$ assertion. |
| 23:31 | — | Reserved |

## SRAMTST — SRAM Test Register 0x8007 F004

The SRAM test register is used for factory testing only.