SECTION 2
SIGNAL DESCRIPTIONS

2.1 Pin Characteristics

Table 2-1 shows MCU pins and their characteristics. All inputs detect CMOS logic levels. All inputs can be put in a high impedance state, but the method of doing this differs depending upon pin function. Refer to **Table 2-3** for a description of output drivers. An entry in the discrete I/O column of the MC68F375 pin characteristics table indicates that a pin has an alternate I/O function. The port designation is given when it applies. Refer to the MC68F375 block diagram for information about port organization.

Table 2-1 Pin Characteristics

Pin Mnemonic	Module	Output Driver	Input Type			Port Designation
			Sync	Hyst Sync	Hyst/Other	
ADDR[23]/ CS[10]/ECLK	SCIM2E	A	no	yes	no	—
ADDR[22:19]/ CS[9:6]/PC[6:3]	SCIM2E	A	no	yes	no	PC[6:3]
ADDR[18:11]/PA[7:0]	SCIM2E	A	no	yes	no	PA[7:0]
ADDR[10:3]/PB[7:0]	SCIM2E	A	no	yes	no	PB[7:0]
ADDR[2:0]	SCIM2E	A	no	yes	no	—
AN[59:57]/PQA[7:5]	QADC64	Aqa	no	yes[1]	no	PQA[7:5]
AN[56:55]/ETRIG[2:1]/ PQA[4:3]	QADC64	Aqa	no	yes[2]	no	PQA[4:3]
AN[54:52]/MA[2:0]/ PQA[2:0]	QADC64	Aqa	no	yes[3]	no	PQA[2:0]
AN[51:48]/PQB[7:4]	QADC64	—	no	yes	no	PQB[7:4]
AN[3:0]/AN[z,y,x,w]/ PQB[3:0]	QADC64	—	no	yes[1]	no	PQB[3:0]
ANX[15:0]	QADC64	—	no	yes[1]	no	—
AS/PE[5]	SCIM2E	B	no	yes	no	PE[5]
AVEC/PE[2]	SCIM2E	B	yes	no	no	PE[2]
$\overline{\text{BERR}}$	SCIM2E	B	yes	no	no	—
BG/CSM	SCIM2E	B	no	no	no	—
BGACK/CSE	SCIM2E	B	yes	no	no	—
BKPT/DSCLK	CPU	—	no	yes	no	—
BR/CS[0]	SCIM2E	B	yes	no	no	—
CLKOUT	SCIM2E	A	no	no	no	—
CNRX	TOUCAN	—	no	yes	no	—
CNTX	TOUCAN	Bo	no	yes	no	—
CSBOOT	SCIM2E	B	no	no	no	—

Table 2-1 Pin Characteristics (Continued)

Pin Mnemonic	Module	Output Driver	Input Type			Port Designation
			Sync	Hyst Sync	Hyst/Other	
CPWM[8:5]	CTM9	A	no	yes	no	—
CTD[10:9]	CTM9	A	no	yes	no	—
CTM2C	CTM9	A	no	yes	no	—
CTS[20B-14A]	CTM9	A	no	yes	no	—
DATA[15:8]/PG[7:0]	SCIM2E	DB	no	yes[1]	no	PG[7:0]
DATA[7:0]/PH[7:0]	SCIM2E	DB	no	yes	no	PH[7:0]
DS/PE[4]	SCIM2E	B	no	yes	no	PE[4]
DSACK[1:0]/PE[1:0]	SCIM2E	B	yes	no	no	PE[1:0]
ETRIG[2:1]/PQA[4:3]	QADC64	Aqa	no	yes[1]	no	PQA[4:3]
EXTAL[4,5]	PLLWXY	—	no	no	Special	—
FASTREF/PF[0]	SCIM2E	Bp	no	yes[1]	no	PF[0]
FC[2]/CS[5]/PC[2] FC[1]/PC[1] FC[0]/CS[3]/PC[0]	SCIM2E	A	yes	no	no	PC[2:0]
FREEZE /QOUT	SCIM2E	A	no	no	no	—
HALT	SCIM2E	Bop	yes	no	no	—
$\overline{\text{IFETCH}}$/DSI	CPU	A	no	yes	no	—
IPIPE/DSO	CPU	A	no	no	no	—
IRQ[7]/PF[7]	SCIM2E	Bp	no	yes	no	PF[7]
IRQ[6]/PF[6]	SCIM2E	B	no	yes	no	PF[6]
IRQ[5:1]/PF[5:1]	SCIM2E	B	no	yes	no	PF[5:1]
MA[2:0]/PQA[2:0]	QADC64	Aqa	no	yes[1]	no	PQA[2:0]
MISO/PQS[0]	QSMCM	Bo	no	yes[1]	no	PQS[0]
MOSI/PQS[1]	QSMCM	Bo	no	yes[1]	no	PQS[1]
PCS[0]/SS/PQS[3]	QSMCM	Bo	no	yes[1]	no	PQS[3]
PCS[3:1]/PQS[6:4]	QSMCM	Bo	no	yes[1]	no	PQS[6:4]
R/$\overline{\text{W}}$	SCIM2E	A	yes	yes	no	—
RESET	SCIM2E	Bo	no	yes	no	—
RMC(BLOCK)/PE[3]	SCIM2E	B	no	yes	no	PE[3]
RXD[1,2]/PQS[8,10]	QSMCM	—	no	no	yes	PQS[8,10]
SCK/PQS[2]	QSMCM	Bo	no	yes[1]	no	PQS[2]
SIZ[1:0]/PE[7:6]	SCIM2E	B	no	yes	no	PE[7:6]
T2CLK	TPU3	A	no	yes	no	—
TP[15:0]	TPU3	A	no	yes	no	—
$\overline{\text{TSC}}$	SCIM2E	—	no	yes	no	—
TXD[1,2]/PQS[7,9]	QSMCM	Bo	no	yes[1]	no	PQS[7,9]
VDDSYN /MODCLK	SCIM2E	—	no	yes[1]	no	—
EPEB0[3]	CMFI	—	yes	—	—	—

Table 2-1 Pin Characteristics (Continued)

Pin Mnemonic	Module	Output Driver	Input Type			Port Designation
			Sync	Hyst Sync	Hyst/Other	
XFC[4]	PLLWXY	—	no	no	Special	—
XTAL[4,3]	PLLWXY	—	no	no	Special	—

NOTES:
1. DATA[15:0]
2. DATA[15:0]
3. DATA[15:0]
4. EXTAL, XFC and XTAL are clock reference connections.
5. These pins are 3 V level only.

Table 2-2 Power Connections

Pin	Voltage	Description
V_{STBY}	3.3 V[1]	Standby RAM power
$V_{DDDPTRAM}$	3.3 V	DPTRAM power (connect to V_{DDL})
V_{DDSYN} V_{SSSYN}	3.3 V[2] 0 V	Clock synthesizer power
V_{DDA} V_{SSA}	5 V 0 V	QADC64 converter power
V_{RH} V_{RL}	5 V 0 V	QADC64 reference voltage
V_{SS} V_{DDH}	0 V 5 V	Pad output driver power (Source and Drain)
V_{SS} V_{DDL}	0 V 3.3 V	Module power (Source and Drain)
V_{PP}	3.3 V/5 V	CMFI program/erase voltage

NOTES:
1. Throughout this manual 3 V = 3.3 volts ±0.3 volts.
   5 V = 5 volts ±10%, except V_{PP} 5 V = 5 volts ±5%.
2. V_{DDSYN}/MODCLK = 3.3 V for V_{DDSYN} function.
   V_{DDSYN}/MODCLK = 0 V for MODCLK function.

Table 2-3 Output Driver Types

Type	I/O	Description
A	O	Output that is always driven. No external pull-up required.
Aqa	O	Type A output open drain on a QADC64 pin
B	O	Three-state output that includes circuitry to assert output before high impedance is established, to ensure rapid rise time. An external holding resistor is required to maintain logic level while in the high-impedance state.
Bo	O	Type B output that can be operated in an open-drain mode.
Bop	O	Type B output that can be operated in an open-drain mode with weak pull-up.
Bp	O	Type B output with weak pull-up.
DB	O	Data bus driver with weak pull-up which pulls data bus high during reset.

Table 2-4 Signal Characteristics

Signal Name	MCU Module	Signal Type	Active State
ADDR[23:0]	SCIM2E	Bus	—
AN[59:48]/[3:0]	QADC64	Input	—
AN[z, y, x, w]	QADC64	Input	—
ANX[15:0]	Analog MUX	Input	—
AS	SCIM2E	Output	0
AVEC	SCIM2E	Input	0
BERR	SCIM2E	Input	0
BG	SCIM2E	Output	0
BGACK	SCIM2E	Input	0
BKPT	CPU32	Input	0
BR	SCIM2E	Input	0
CLKOUT	SCIM2E	Output	—
CNRX	TOUCAN	Input	---
CNTX	TOUCAN	Output	---
CS[10:5], CS[3], CS[0]	SCIM2E	Output	0
CSBOOT	SCIM2E	Output	0
CSE	SCIM2E	Output	0
CSM	SCIM2E	Output	0
CPWM[8:5]	CTM9	Output	1/0
CTD[10:9]	CTM9	Input/Output	—
CTM2C	CTM9	Input	1/0
CTS[20B - 14A]	CTM9	Input/Output	—
DATA[15:0]	SCIM2E	Bus	—
DS	SCIM2E	Output	0
DSACK[1:0]	SCIM2E	Input	0
DSCLK	CPU32	Input	Serial Clock
DSI	CPU32	Input	Serial Data
DSO	CPU32	Output	Serial Data
ECLK	SCIM2E	Output	—

Table 2-4 Signal Characteristics (Continued)

Signal Name	MCU Module	Signal Type	Active State
ETRIG[2:1]	QADC64	Input	1/0
EXTAL[1]	SCIM2E	Input	—
FASTREF	SCIM2E	Input/Output	1
FC[2]/CS[5]/PC[2] FC[1]/PC[1] FC[0]/CS[3]/PC[0]	SCIM2E	Output	1/0
FREEZE	SCIM2E	Output	1
HALT	SCIM2E	Input/Output	0
IPIPE	CPU32	Output	0
IFETCH	CPU32	Output	0
IRQ[7:1]	SCIM2E	Input	0
MA[2:0]	QADC64	Output	1
MISO	QSMCM	Input/Output	—
MOSI	QSMCM	Input/Output	—
PCS[3:0]	QSMCM	Input/Output	—
PQA[7:0]	QADC64	Input/Output	—
PQB[7:0]	QADC64	Input	—
QUOT	SCIM2E	Output	—
R/$\overline{W}$	SCIM2E	Output	1/0
RESET	SCIM2E	Input/Output	0
RMC	SCIM2E	Output	0
RXD1, RXD2	QSMCM	Input	—
SCK	QSMCM	Input/Output	—
SIZ[1:0]	SCIM2E	Output	1
SS	QSMCM	Input	0
T2CLK	TPU3	Input	—
TP[15:0]	TPU3	Input/Output	—
TSC	SCIM2E	Input	0/1
TXD1, TXD2	QSMCM	Output	—
VDDSYN/MODCLK	SCIM2E	Input	—
EPEB0[1]	CMFI	Input	—
XFC	SCIM2E	Input	—
XTAL[1]	SCIM2E	Output	—

NOTES:
1. These pins are 3 V level only.

Table 2-5 Signal Functions

Signal Name	Mnemonic	Function
Address Bus	ADDR[23:0]	24-bit address bus used by CPU32
QADC64 Analog Input	AN[59:48]/[3:0]	Sixteen channel A/D converter analog input pins
QADC64 Analog Input	AN[z, y, x, w]	Four input channels utilized when operating in multiplexed mode
Analog MUX Inputs	ANX[15:0]	Analog signal inputs multiplexed to the analog converters
Address Strobe	AS	Indicates that a valid address is on the address bus
Autovector	AVEC	Requests an automatic vector during interrupt acknowledge
Bus Error	BERR	Indicates that a bus error has occurred
Bus Grant	BG	Indicates that the MCU has relinquished the bus
Bus Grant Acknowledge	BGACK	Indicates that an external device has assumed bus mastership
Breakpoint	BKPT	Signals a hardware breakpoint to the CPU
Bus Request	BR	Indicates that an external device requires bus mastership
System Clock Out	CLKOUT	Internal system clock
TOUCAN Receive Data	CNRX	CAN 2.0B Serial Data Input
TOUCAN Transmit Data	CNTX	CAN 2.0B Serial Data Output
Chip Selects	CS[10:5], CS[3], CS[0]	Select external devices at programmed addresses
Boot Chip Select	CSBOOT	Chip select for external boot start-up ROM
Emulator Chip Select	CSE	Chip select for external port emulator
Module Chip Select	CSM	Chip select for external ROM emulator
CTM PWM	CPWM[8:5]	PWM channels which can also be used as general-purpose output pins
CTM9 Double Action Channel	CTD[10:9]	Bidirectional CTM9 double action timer channels
CTM9 Modulus Clock	CTM2C	CTM9 modulus counter clock input
CTM9 Single Action Channels	CTS[20B - 14A]	Bidirectional CTM9 single action timer channels
Data Bus	DATA[15:0]	16-bit data bus
Data Strobe	DS	Read cycle — indicates that an external device should place valid data on the data bus. Write cycle — indicates that valid data is on the data bus.
Data and Size Acknowledge	DSACK[1:0]	Provides asynchronous data transfers and dynamic bus sizing
Development Serial In, Out, Clock	DSI, DSO, DSCLK	Serial I/O and clock for background debug mode
QADC64 External Trigger	ETRIG[2:1]	When a scan queue is in external trigger mode, the corresponding ETRIG pin is configured as a digital input and the software programmed I/O direction in the DDR is ignored.
Crystal Oscillator	EXTAL, XTAL	Connections for clock synthesizer circuit reference; a crystal or an external oscillator can be used
VCO Reference Mode Select	FASTREF	Selects between FAST or SLOW reference modes
Function Codes	FC[2:0]	Identify processor state and current address space
Freeze	FREEZE	Indicates that the CPU has acknowledged a breakpoint
Halt	HALT	Suspend external bus activity
Instruction Pipeline	IPIPE	Indicates instruction pipeline activity

Table 2-5 Signal Functions (Continued)

Signal Name	Mnemonic	Function
Instruction Pipeline	IFETCH	Indicates instruction pipeline activity
Interrupt Request Level	IRQ[7:1]	Provides an interrupt priority level to the CPU
QADC64 Multiplexed Address	MA[2:0]	When external multiplexing is used, these pins provide the addresses to the external multiplexer
Master-In Slave-Out	MISO	Serial input to QSPI in master mode; serial output from QSPI in slave mode
Master-Out Slave-In	MOSI	Serial output from QSPI in master mode; serial input to QSPI in slave mode
Peripheral Chip Select	PCS[3:0]	QSPI Peripheral Chip Select
QADC64 Port A	PQA[7:0]	QADC64 port A analog inputs and I/O port PQA[7:0]
QADC64 Port B	PQB[7:0]	QADC64 port B analog inputs and input-only port PQB[7:0]
Quotient Out	QUOT	Provides the quotient bit of the polynomial divider (test mode only)
Read/Write	R/$\overline{W}$	Indicates the direction of data transfer on the bus
Reset	RESET	System reset
Read-Modify-Write Cycle	RMC	Indicates an indivisible read-modify-write instruction
SCI Receive Data	RXD1, RXD2	Serial input to the SCI
QSPI Serial Clock	SCK	Clock output from QSPI in master mode; clock input from QSPI in slave mode
Size	SIZ[1:0]	Indicates the number of bytes remaining to be transferred during a bus cycle
Slave Select	SS	Causes serial transmission when QSPI is in slave mode; chip-select in master mode
TPU3 Clock	T2CLK	TPU3 clock input
TPU3 I/O Channels	TP[15:0]	Bidirectional TPU3 channels
Three-State Control	TSC	Places all output drivers in a high impedance state
SCI Transmit Data	TXD1, TXD2	Serial output from the SCI
Clock Mode Select	VDDSYN/MODCLK	Selects the source of the internal system clock
CMFI Block 0 Program/ Erase Enable	EPEB0	When asserted, allows CMFI block 0 to be programmed or erased.
External Filter Capacitor	XFC	Connection for external phase-locked loop filter capacitor

2.2 Pinout

The production MC68F375 will be bumped flip-chip and PBGA.

2.2.1 Pinout Diagram

The pad numbers for each pad/signal on the die are shown in **Figure 2-1**. Note that the numbers and names correspond to the pad names and order on the die. The pin/bump numbers on the PBGA and Bumped die may be different. The chip layout plan is also shown in **Figure 2-1**.

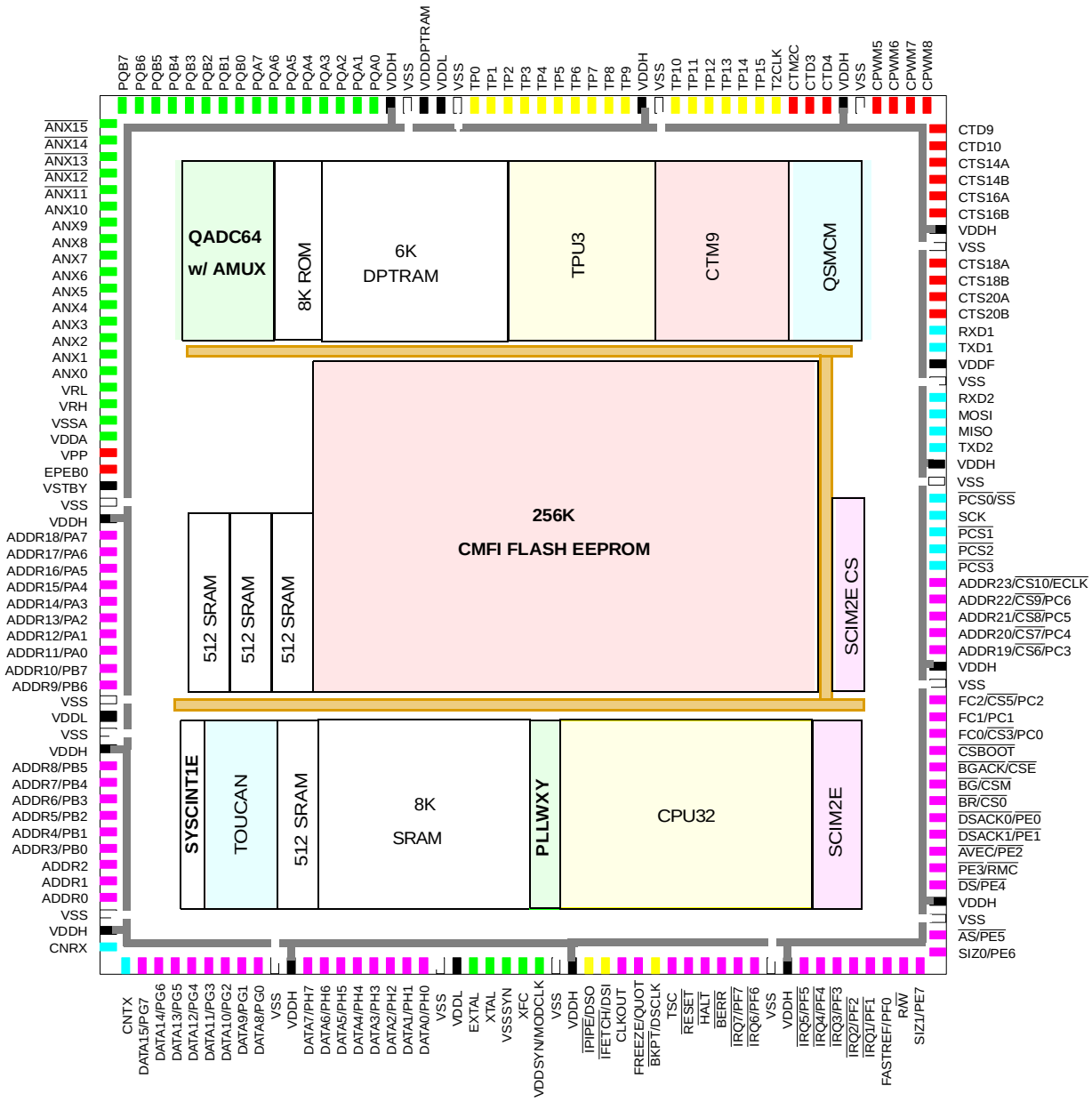
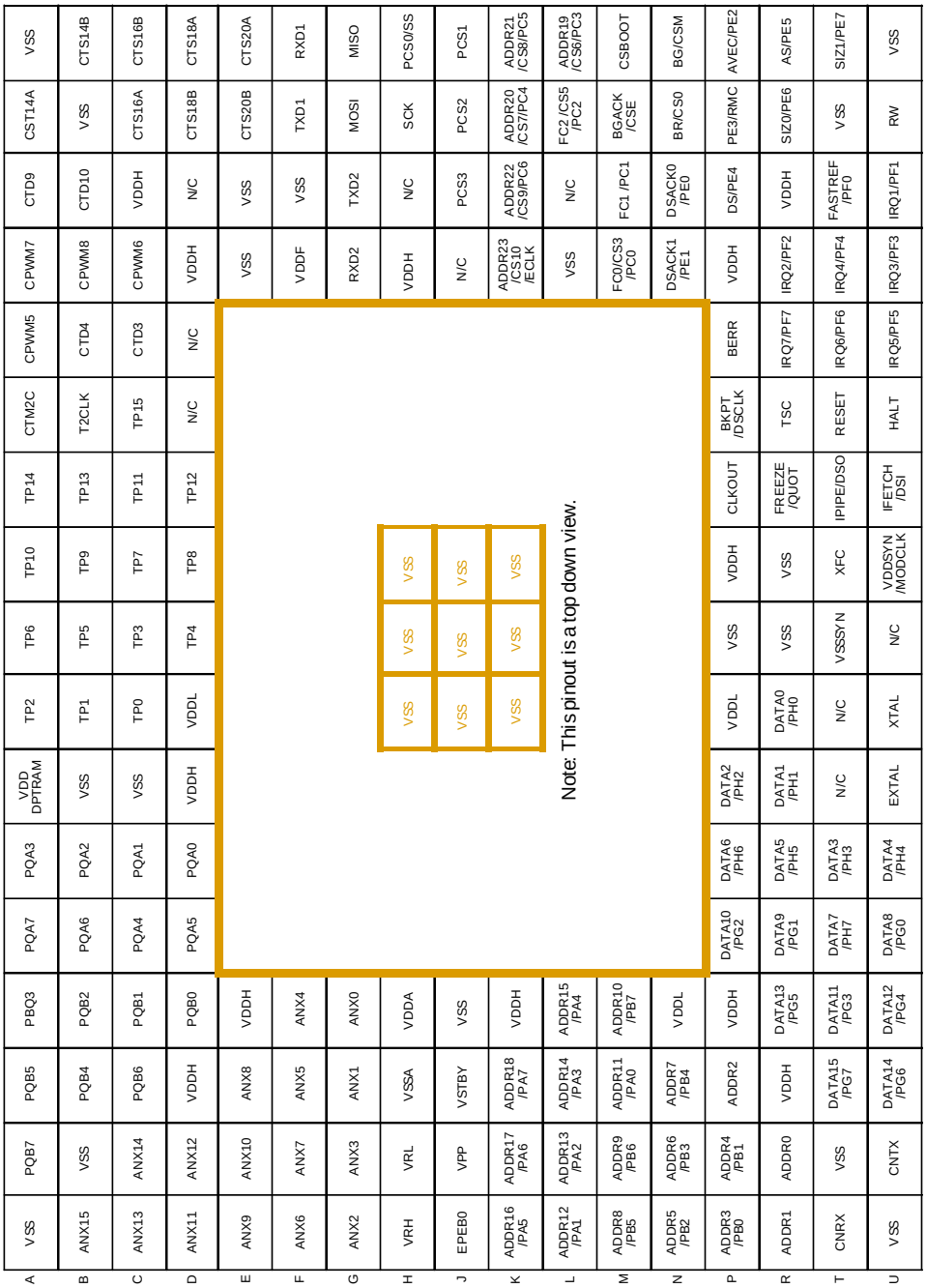


Figure 2-1 MC68F375 Pad Map



Note:
N/C = NO CONNECTION — these balls have no electrical connection inside the package.

Figure 2-2 MC68F375 Ball Map