



APPENDIX H

FLASH ELECTRICAL CHARACTERISTICS FOR ALL J76N MASK SETS AND 0K02A AND 1K02A ONLY

H.1 Electrical Characteristics

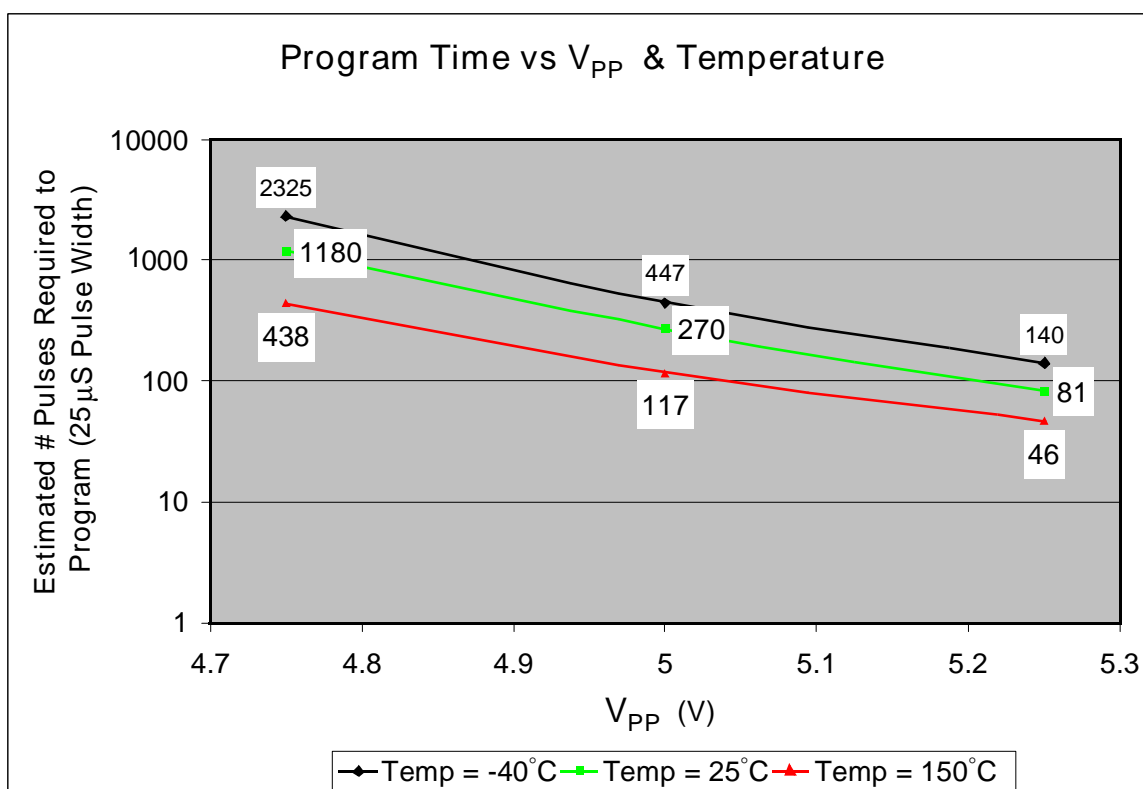
Table H-1 Program and Erase Characteristics

($V_{DDF} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{PP} = 4.75 \text{ V to } 5.25 \text{ V}$, $T_A = T_L \text{ to } T_H$)

Symbol	Meaning	Value			Units
		Minimum	Typical	Maximum	
E_{PULSE}	Number of Erase Pulses	1	1	1	
T_{ERASE}	Erase Pulse Time	0.9	1	1.1	S
$P_{PULSE(4.75 \text{ V}_{PP})}$	Number of Program Pulses @ $V_{PP} = 4.75$	—	1200 ¹	3500 ^{2,3,5}	Pulses
$P_{PULSE(5.0 \text{ V}_{PP})}$	Number of Program Pulses @ $V_{PP} = 5.00$	—	300 ⁴	1000 ⁵	Pulses
$P_{PULSE(5.25 \text{ V}_{PP})}$	Number of Program Pulses ⁶ @ $V_{PP} = 5.25$	—	125 ⁷	500 ⁵	Pulses
T_{PROG}	Program Pulse Time	21.2	25.6	32.0	μS
$C_{PULSE(4.75 \text{ V}_{PP})}$	Number of CENSOR Clear Pulses @ $V_{PP} = 4.75$	1	1	3 ⁸	Pulses
$C_{PULSE(5.0 \text{ V}_{PP})}$	Number of CENSOR Clear Pulses @ $V_{PP} = 5.00$	1	1	3 ⁸	Pulses
$C_{PULSE(5.25 \text{ V}_{PP})}$	Number of CENSOR Clear Pulses @ $V_{PP} = 5.25$	1	1	3 ⁸	Pulses
T_{CLEAR}	CENSOR Clear Pulse Time	0.9 ⁸	1 ⁸	1.1 ⁸	S
$S_{PULSE(4.75 \text{ V}_{PP})}$	Number of CENSOR Set Pulses @ $V_{PP} = 4.75$	1	1	3 ⁸	Pulses
$S_{PULSE(5.0 \text{ V}_{PP})}$	Number of CENSOR Set Pulses @ $V_{PP} = 5.00$	1	1	3 ⁸	Pulses
$S_{PULSE(5.25 \text{ V}_{PP})}$	Number of CENSOR Set Pulses @ $V_{PP} = 5.25$	1	1	3 ⁸	Pulses
T_{SET}	CENSOR Set Pulse Time	0.9 ⁸	1 ⁸	1.1 ⁸	S

NOTES:

1. The typical number of pulses at $V_{PP} = 4.75 \text{ V}$ and $T_A = 25^\circ\text{C}$.
2. The worst case programming time occurs at $V_{PP} = 4.75 \text{ V}$ and $T_A = -40^\circ\text{C}$.
3. This value is based on initial device characterization and is not tested in production.
4. The typical number of pulses is at $V_{PP} = 5.00 \text{ V}$ and $T_A = 25^\circ\text{C}$.
5. Assumes pulse width = 25.6 μs .
6. The best case (fastest) programming time of < 50 pulses is at $V_{PP} = 5.25 \text{ V}$ and $T_A = 125^\circ\text{C}$.
7. The typical number of pulses is at $V_{PP} = 5.25 \text{ V}$ and $T_A = 25^\circ\text{C}$.
8. After characterization this value may be improved.



**Figure H-1 Typical Program Time vs. V_{PP} and Temperature
(for CDR1 “Target” Process)**

Table H-2 CMF AC and DC Power Supply Characteristics

Symbol	Meaning	Min. Value	Max Value	Unit
V_{DDF}	Operating Voltage Read, Program or Erase	3.0	3.6 V	V
I_{DDF}	Operating Current at 40.0MHz, $V_{DDF} = 3.3$ V for a 256K-byte Module Read, Program or Erase Operation Disabled	— —	22 5	mA
V_{PP}	External Program or Erase voltage Read Program or Erase	$V_{DDF} - 0.35$ 4.75	5.5 5.25	V
I_{DDPP}	External Program and Erase Current ¹ Read, $V_{PP} = 5$ V Program, $V_{PP} = 5.25$ V Erase, $V_{PP} = 5.25$ V		<100 ¹ 30 ¹ 30 ¹	μA^1 mA ¹ mA ¹

NOTES:

1. Average current is less than 30 mA when programming both modules simultaneously.

H.1.1 Flash Module Life



Table H-3 Flash Module Life

Symbol	Meaning	Value
P/E Cycles ¹	Maximum Number of Program/ Erase cycles ² to Guarantee Data Retention	100 ^{3,4}
Retention	Data Retention at Average Operating Temperature of 85 °C	Minimum 10 years

NOTES:

1. Target failure rate at specified number of program/erase cycles of 2ppm pending characterization of production silicon.
2. A program/erase cycle is defined as switching the bits from 1 → 0 → 1.
3. Reprogramming of a CMF array block prior to erase is not required.
4. Number of program/erase cycles to be adjusted pending characterization of production silicon.

H.2 Programming and Erase Algorithm

Table H-4 CMF Programming Algorithm (v5)

No. of Pulses (Maximum)	Pulse Width	NVR	PAWs	GDB	PAWs Mode	Description
3500	25.6 μs	X	000	X	Normal	

Table H-5 CMF Erase Algorithm (v5)

No. of Pulses (Maximum)	Pulse Width	NVR	PAWs	GDB	PAWs Mode	Description
10	1 s	X	111	X	Mode 7P	Positive drain ramp

