



SECTION 4

BURST BUFFER CONTROLLER MODULE

4.1 Overview and General Description

The burst buffer controller module (BBC) consists of three main functional parts: bus interface unit (BIU), instruction memory protection unit (IMPU) and instruction code decompressor unit (ICDU) See [Figure 4-1](#).

The BBC master BIU interfaces between the RCPU instruction port and internal U-bus and can support burstable and non-burstable accesses on U-bus.

The IMPU allows the instruction memory to be divided into four regions with different protection attributes. The IMPU compares the attributes of the RCPU memory access request with the attributes of the appropriate region. If the access is allowed, the proper signals are sent to the BIU. If the memory region is protected, an interrupt is sent to the RCPU and master BIU cancels U-bus access.

The IMPU is able to relocate the RCPU exception vectors. The IMPU always maps the exception vectors into the internal memory space of the MPC565 / MPC566. This feature is important for multi-MPC565 / MPC566 system, where although the internal memories of some of controllers are shifted not to be on the lower four Mbytes, they can still have their own internal exception vector tables with the same exception addresses issued by their RCPU cores.

The IMPU also supports MPC565 / MPC566 enhanced interrupt controller by extending exception vectors relocation mechanism to translate the RCPU External Interrupt exception vector separately and splitting it to up to 48 different vectors, corresponding to the code, generated by the interrupt controller. See also [6.4.4 Enhanced Interrupt Controller](#)

ICDU is responsible for on-line (previously compressed) instruction code decompression in the “Decompression ON” mode.

NOTE

The code compression features of the MPC566 are slightly different than the code compression of the MPC556.

The ICDU contains a four-Kbyte RAM (DECRAM). DECRAM is used for decompressor vocabulary tables storage of the general-purpose memory.

The DECRAM can also serve as general purpose RAM memory on U-bus.

The ICDU includes special branch target buffer (BTB) that improves the MPC565 performance by holding previously fetch instructions to RCPU core.

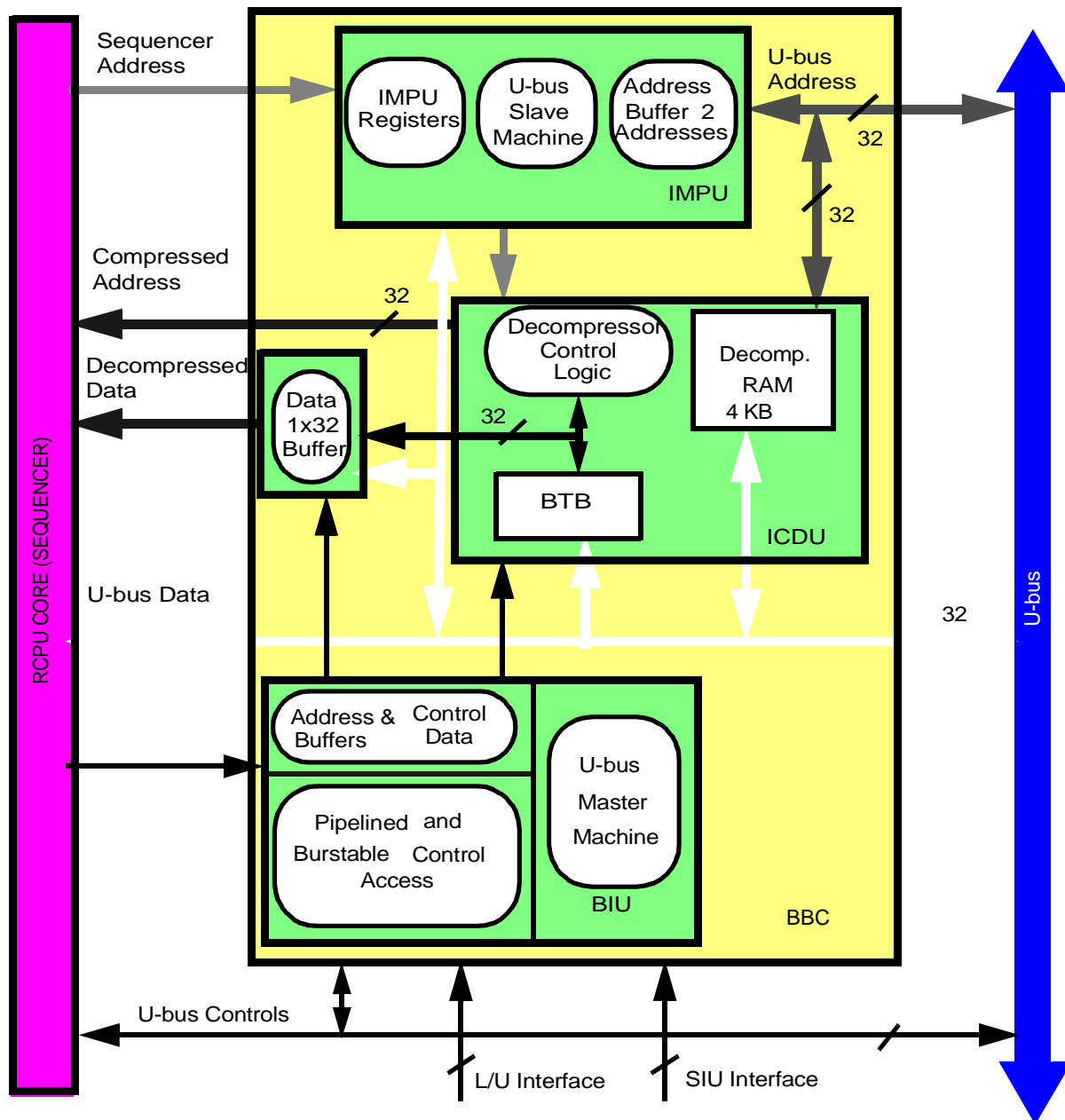


Figure 4-1 BBC Module Block Diagram

4.2 Feature List

4.2.1 BIU Key Features

- Supports pipelined and burstable accesses to internal and external memories
- Supports the de-coupled interface with the RCPU instruction unit
- Parked master on the U-bus, resulting with zero clocks delay for RCPU fetch access to the U-bus



- Full utilization of the U-bus pipeline for fetch accesses
- Tight interface with L2U module, taking advantage of full U-bus bandwidth and back-to-back accesses avoiding undesirable bubbles
- Supports program trace and show cycles

4.2.2 IMPU Key Features

- Four regions in which the base address and size can be programmed
- Available region sizes are: four Kbytes, eight Kbytes, 16 Kbytes, 32 Kbytes, 64 Kbytes, 128 Kbytes, 256 Kbytes, 512 Kbytes, one Mbyte, two Mbytes, four Mbytes, eight Mbytes, 16 Mbytes....four Gbytes
- Overlap between regions is allowed
- Each of the four regions supports the following attributes:
 - user/supervisor
 - Guard attribute (causes an interrupt in case of speculative fetch attempt)
 - compressed/non-compressed
- can be enabled or disabled by software
- Global region entry declares the default access attributes for all memory areas not covered by the four regions:
- RCPU gets the instruction storage protection exception generated upon:
 - Access violation of protection attributes
 - Fetch from guarded region
- RCPU **MSR[IR]** bit controls IMPU protection
- Programming is done using PowerPC's **mtspr/mfspr** instructions to/from implementation specific special purpose registers.
- Compressed/non-compressed region with enable/disable option
- Exception table relocation: the IMPU supplies relocation address of all exceptions within the internal memory space
- External interrupt vector splitting to reduce the external interrupt latency
- Special reset exception vector for "Decompression ON" mode

4.2.3 ICDU Key Features

- Instruction code on-line decompression based on "instruction classes" algorithm.
- No need for address translation between compressed and non-compressed address spaces — ICDU provides "next instruction address" to the RCPU
- Instruction decompression takes one clock mostly
- Code decompression is pipelined:
 - No performance penalty during sequential program flow execution
 - Minimal performance penalty due to change of program flow execution
- Two operation modes are available: "Decompression ON" and "Decompression

OFF". Switch between compressed and non-compressed user application software parts is possible.

- adaptive vocabularies scheme is supported; each user application can have its own optimum vocabularies.
- Special branch target buffer (BTB) to improve system performance



4.2.3.1 DEGRAM Key Features

- Four Kbytes RAM for decompression vocabulary tables
- Two clock read/write access U-bus general purpose RAM
- Four clock load/store access from the L-bus
- Byte, half-word (16-bit) or word (32-bit) read/write accesses and fetches
- Special access protection functions
- Low power standby operation for data retention

4.3 Class Based Compression Model Main Principles

4.3.1 Compression Model Features

- Implemented for PowerPC architecture
- Up to 50% code size reduction
- No need for address translation tables
- No changes in the CPU architecture
- Compression is done off line by a special “compressor” tool, using Instruction classes based algorithm optimized for PowerPC instructions set
- Decompression is done at run-time by special hardware
- Optimized for cache-less systems:
 - Highly effective in system solutions for low cache-hit ratio environment and for systems with fast embedded program memory
 - Deterministic program execution time
 - No performance penalty during sequential program flow execution
 - Minimal performance penalty due to change of program flow execution
- Switch between compressed and non-compressed user application sections is possible. (Compressed subroutine can call non-compressed one and be called from non-compressed portion of user application)
- Adaptive vocabularies, generated for particular application
- Slight changes in the core and existing RISC development tools — compilers, simulators, manually coded libraries
- Compressed address space is up to one Gbyte
- Branch displacement from its target:

- Conditional branch displacement is up to four Kbytes
- Unconditional branch displacement is up to four Mbytes

NOTE

Branch displacement is hardware limited. The compiler can enlarge the branch scope by creating branch chains.

4.3.2 Model Limitations

No address arithmetic is allowed, because the address map changes during compression and no software tool can identify address arithmetic structures in the code.

4.3.3 Instruction Classes Based Compression Algorithm

The code compression algorithm is based on creating vocabularies of frequently appearing PowerPC RISC instructions or instructions halves and replacing these instructions with pointers to the vocabularies. The system contains several sets of vocabularies for different groups of instructions. These groups are referred to as *classes*.

Every instruction belongs to exactly one class. Compression of the instructions in a class may be in one of the following modes. Refer to [Figure 4-2](#).

1. Compression of the whole instruction into one vocabulary pointer
2. Compression of each half of the instruction into a different vocabulary
3. Compression of one of the instruction's halves into a vocabulary pointer and bypass of the other half. Bypass is the placing of the field's data in the compressed code, sometimes after compaction defined in the class.
4. Bypass of the whole instruction. No compaction permitted.



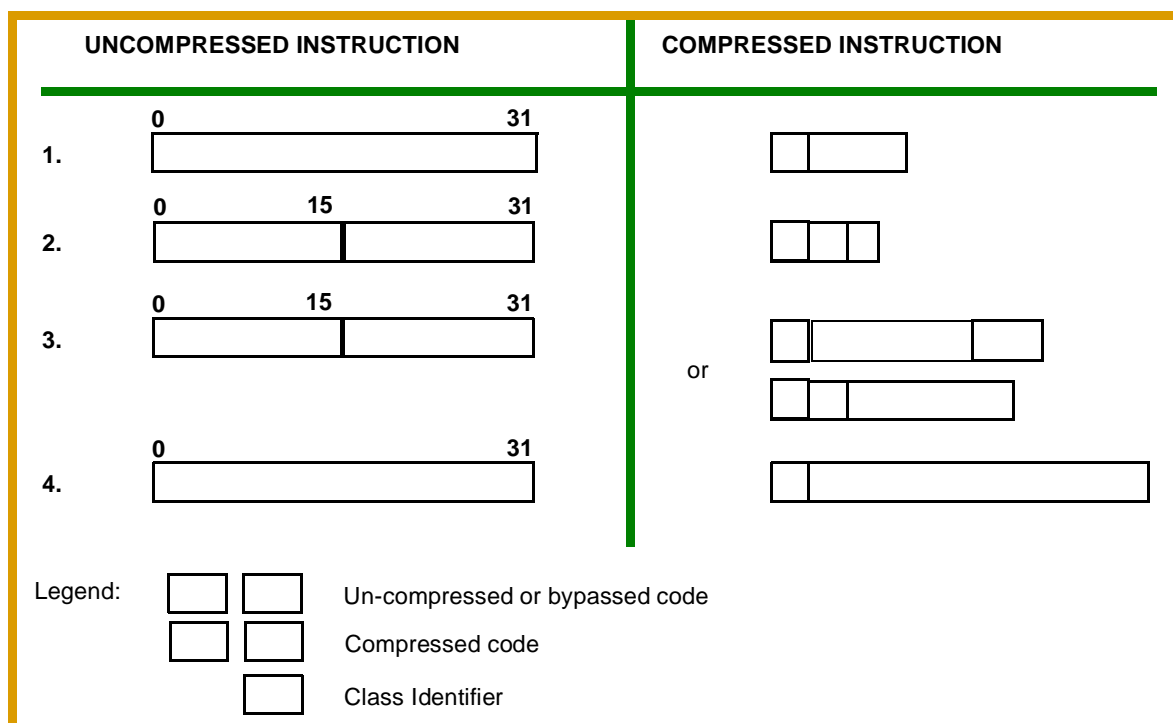


Figure 4-2 Instruction Compression Alternatives

A 4-bit class identifier is added to the head of each compressed instruction in order to enable class identification during decompression. Compressed and bypass fields' length may vary.

The compressed instruction is guaranteed to be of even length of bits. Thus, four bits are needed to locate such instruction inside a memory word. The instruction address in "Decompression ON" mode consists of a 28-bit word address and a 4-bit instruction pointer (IP). See [Figure 4-3](#).

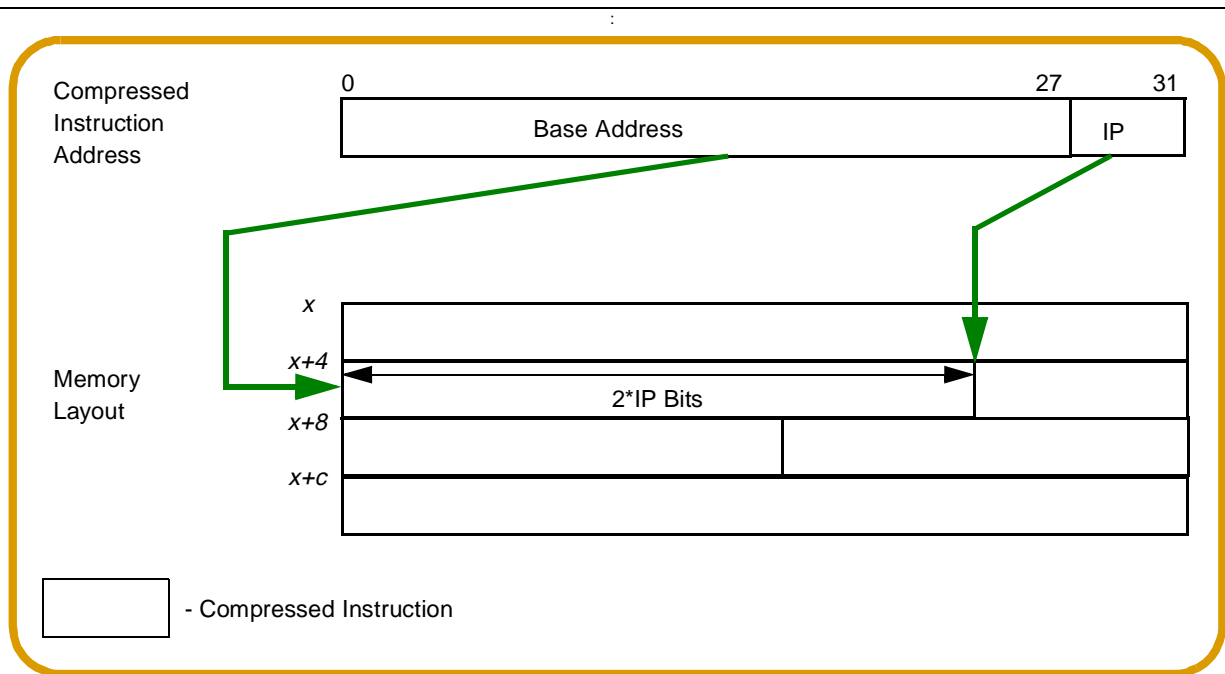


Figure 4-3 Compressed Address Format

4.3.4 Compression Process

Compression process is implemented by the following steps: (See [Figure 4-4.](#))

- User code compilation/linking
- Vocabulary and classes generation
- User application code compression by software compression tool.

The vocabularies and classes configuration are generated by profiling the static code, based on instruction classes algorithm.

The code compression can be done by using either default or specific for particular application vocabularies, generated at previous step. In case of default vocabularies, the previous step can be omitted, but compression efficiency is reduced.

Compression tool replaces regular PowerPC instruction by their “compressed” representation containing less data bits. The tool also updates offset fields in direct branch instructions to include compressed formatted offset (four bits IP and word offset). Thus maximum branch offsets in “Decompression On” mode are reduced. The RCPU uses the word offset for direct branch target address computation. The RCPU provides IP portion of the branch offset field to the decompression unit as it is represented in the branch instruction.

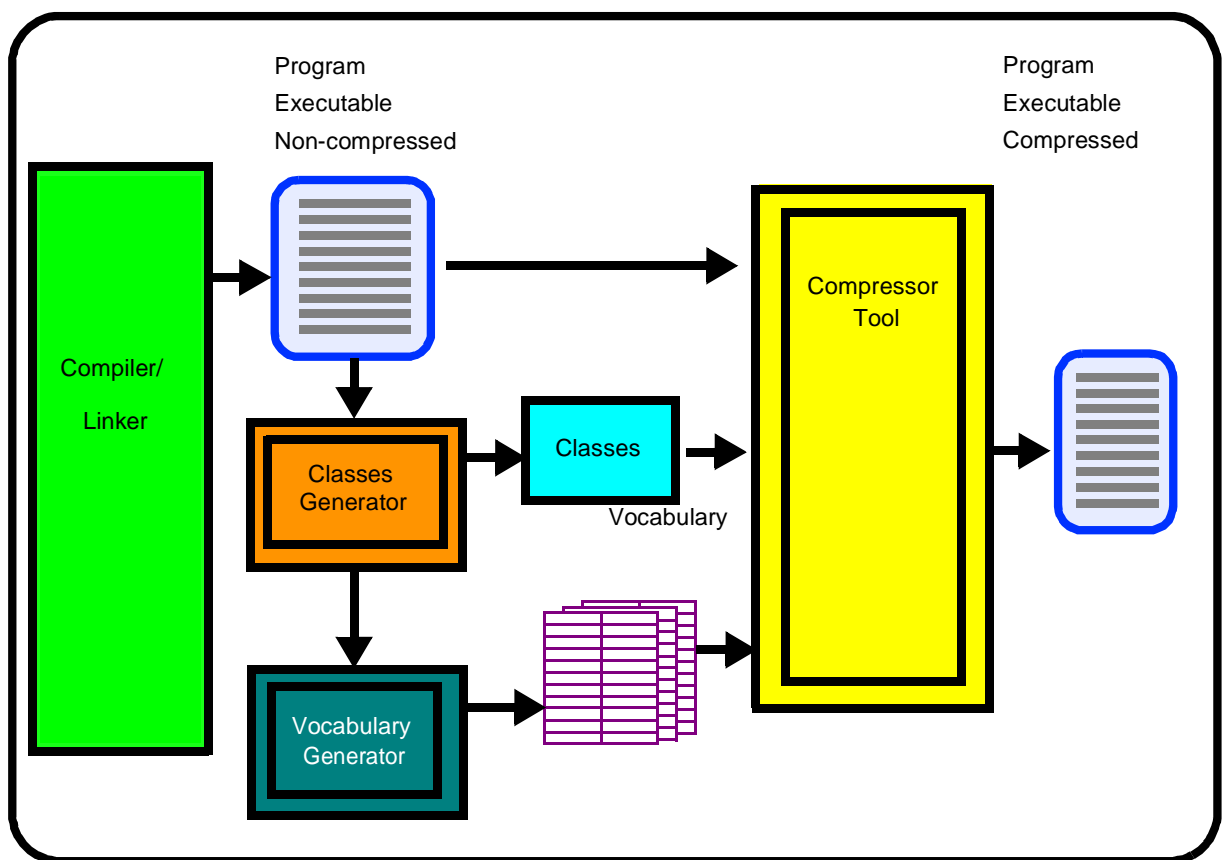


Figure 4-4 Code Compression Process

4.3.5 Decompression

- The instruction code is stored in the memory in the compressed form
- The vocabularies are stored in a dedicated ICDU RAM (DECRAM)
- The classes configuration is stored in a dedicated ICDU registers (DCCRs)
- The decompression is done on-line by the dedicated decompressor unit
- Decompression flow: (See [Figure 4-5](#))
 - RCPU provides to the BBC “**2-bit aligned COF¹ address**”
 - ICDU:
 - Converts COF address to “**word aligned physical address**” to access the memory
 - Fetches the compressed instruction code data from the memory, decompresses it and delivers “**non-compressed instruction code**” together with the bit aligned “**next instruction address**” to the RCPU, which uses it for sub-routine and exceptions handling.

¹. COF = Change of Flow

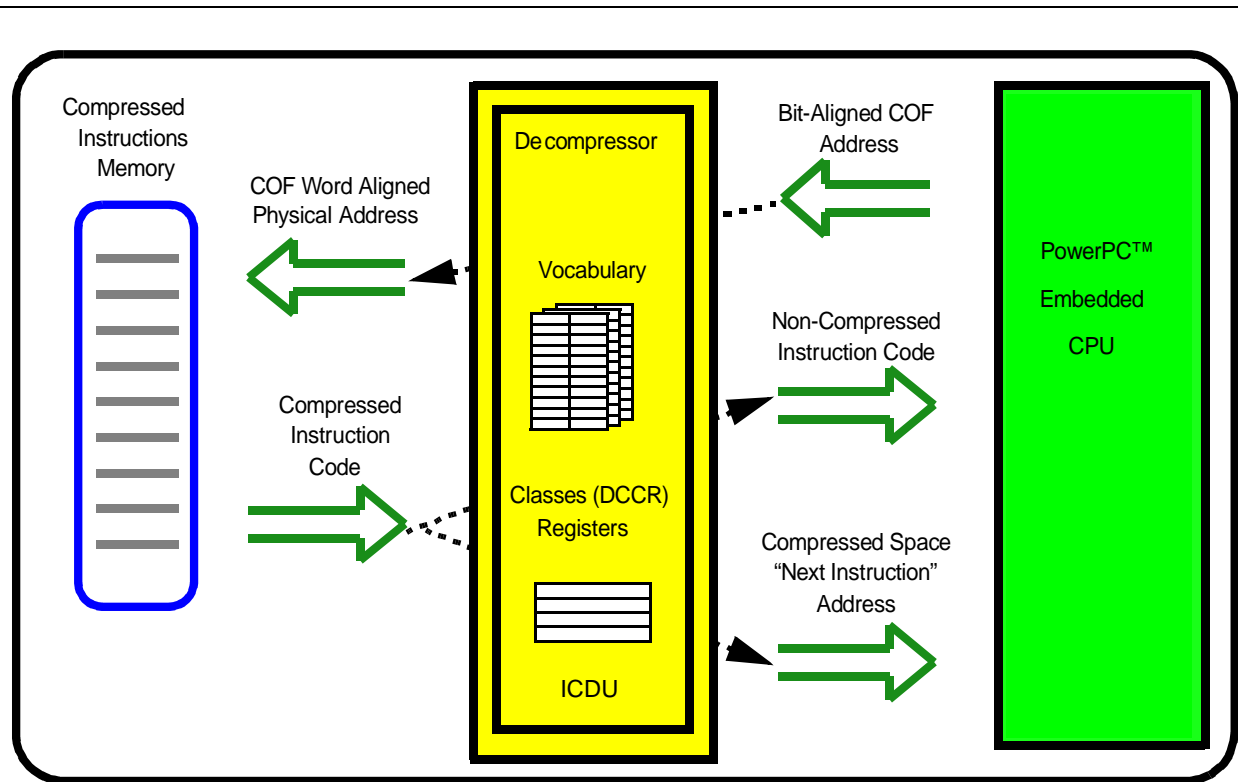


Figure 4-5 Code Decompression Process

4.3.6 Compression Environment Initialization

In order to commence execution of compressed code, the DECRAM and the classes information (in DCCR registers) should be programmed. The data to be programmed is supplied by the compressor tool and the vocabulary generator. There are two initialization scenarios:

1. Wake up in "Decompression OFF" mode — If the chip wakes up with decompression disabled, the initialization routine can be executed at any time before entering "Decompression ON" mode. After the compression environment is initialized, the operational mode would be changed to "Decompression ON".
2. Wake up in "Decompression ON" mode — If the chip wakes up in "Decompression ON" mode, it has to perform compressed instruction without the vocabularies and class parameters. Thus, all instructions executed until the end of the initialization routine will be compressed in the global bypass format. Perform the routine as close as possible to the wake up.

4.4 Operation Modes

4.4.1 Instruction Fetch

BBC provides two instruction fetch modes: "Decompression OFF" and "Decompression ON". The operational mode is defined by the RCPU **MSR[DCMPEN]** bit. If the bit

is set, the mode is “Decompression ON”. If it is not set, the mode is “Decompression OFF”.



4.4.1.1 “Decompression OFF” Mode

In this mode the BIU module transfers fetch accesses from the RCPU to the U-bus. When a new access is issued by the RCPU, it is transferred in parallel to both IMPU and BIU. The IMPU compares the address of the access to its region programming. The BIU checks if the access can be immediately transferred to the U-bus, otherwise it requests the U-bus for the next clock.

The BIU may be programmed for burstable or non-burstable access. If the BIU is programmed for burstable access, U-bus address phase transaction is accompanied by the burst request attribute. If burstable access is allowed by the U-bus slave, the BIU continues current access as burstable, otherwise current access is executed as a single access. If any protection violation is detected by the IMPU, the current U-bus access is aborted by the BIU and exception is signaled to the RCPU.

Show cycle, program trace and debug port access attributes accompanying the RCPU access are forwarded by the BIU along with the U-bus access.

4.4.1.2 “Decompression ON” Mode

In this mode the RCPU sends the two-bit aligned change of flow address to the BBC. The BIU transfers word portion of the address to the U-bus. The BBC continues to pre-fetch the data from the consequent memory addresses regardless RCPU requests in order to supply data to the ICDU.

The data coming from the instruction memory is not provided directly to the RCPU, but loaded into the ICDU for decompression. Decompressed instruction code together with “next instruction address” are provided to the RCPU whenever it requires another instruction fetch.

All addresses issued by the BIU to the U-bus are transferred in parallel to the IMPU. The IMPU compares the address of the access to its region programming. If any protection violation is detected by the IMPU, the current U-bus access is aborted by the BIU and an exception is signaled to the RCPU.

Show cycle and program trace access attributes accompanying the COF RCPU access only are forwarded by the BIU along with the U-bus access. Additional information about “IP” part of compressed instruction address is provided on U-bus data bus. Refer to [4.4.1.3 Show Cycles in “Decompression ON” Mode](#) for more details.

In this mode the ICDU DEGRAM is used as decompressor vocabulary storage and may not be used as a general purpose RAM.

4.4.1.3 Show Cycles in “Decompression ON” Mode

In the case of “Decompression ON” mode the instruction address consists of instruction “base address” and four bits of the “instruction bit pointer”. In order to provide the capability to show full instruction address, including instruction bit pointer, on the exter-

nal bus, show cycles information is presented not only on the address bus, but also on some bits of the data bus:

- **ADDR[0:29]** - show the value of the base address of compressed instruction (word pointer into the memory)
- **DATA[0]** - shows in which mode the MPC565 / MPC566 is operating
 - 0 = “Decompression OFF” mode.
 - 1 = “Decompression ON” mode.
- **DATA[1:4]** - represent an instruction bit pointer within the word.

NOTE

The **BBCMCR[DECOMP_SC_EN]** bit determines if the data portion (**DATA[0:4]**) of the instruction show cycle is driven or not, regardless of decompression mode (**BBCMCR[EN_COMP]** bit)

If the **BBCMCR[DECOMP_SC_EN]** bit is set the show cycle may be delayed by one clock by the USIU. This happens if the show cycle occurs after external device read cycle.

4.4.2 Burst Operation of the BBC

The BBC may initiate and handle burst accesses on the U-bus. The **BBCMCR[BE]** bit determines whether the BBC operates burst cycles or not. Burst requests are enabled when the BE bit is set. BBC handles non wrap-around bursts with up to 4 data beats on internal U-bus. Refer to **4.8.2.1 BBC Module Configuration Register BBCMCR**.

NOTES

The burst operation in the MPC565 / MPC566 is useful if a user system implements burstable memory devices on external bus. Otherwise the mode will cause the MPC565 / MPC566 performance degradation.

When the RCPU runs in serialized mode it's recommended to disable bursts by the BBC to speed up MPC565 / MPC566 operation

Burst operation in “Decompression ON” and “Debug” mode is disabled regardless of **BBCMCR[BE]** bit setting.

4.4.3 Access Violation Detection

Instruction memory protection is assigned on a regional basis. Default operation of IMPU is done on a global region. The IMPU has control registers which contain the following information: region protection on/off, region base address, size and access permissions.

Protection logic is activated only if RCPU **MSR[IR]** is set.

During each fetch request from the RCPU core to instruction memory, the address is compared to value in region base address of enabled regions. Any address, matching



the specific region within its appropriate size as defined in the region attribute register, sets a match indication.



When more than one match indication occurs, the effective region is the region with the highest priority. Priority is determined by region number. The lowest region number has highest priority. The global region has lowest priority.

When no match happens, the effective region is the global region.

The region attribute registers contain the region protection fields (**PP, G, CMPR**). The protection fields are compared to address attributes issued by the RCPU. If the access is permitted the address is passed to BIU and further to U-bus.

Whenever IMPU detects access violation, the following actions are taken:

1. The request, forwarded to the BIU is canceled
2. The RCPU is informed that the requested address caused an access violation by exception request.

However, if the required address contains show cycle attribute, the BIU delivers the access onto the U-bus to obtain program tracking

The exception vector (address) that the RCPU issues for this exception has a 0x1300 offset in PowerPC exception vector table. The access violation status is provided in RCPU **SRR1** special purpose register. The encoding of the status bits is as follows:

- **SRR1** [1] = 0
- **SRR1** [3] = Guarded storage
- **SRR1** [4] = Protected storage or Compression violation
- **SRR1** [10] = 0

Only one bit is set at a time.

4.4.4 Slave Operation

The BBC is operating as a U-bus slave when the IMPU registers, decompressor RAM (DECRAM) or ICDU registers are accessed from the U-bus. The IMPU registers programming is done using PowerPC **mtspr/mfspr** instructions. The ICDU configuration registers (DCCRs) (see **Table 4-10**) and DECRAM are mapped into the chip memory space and accessed by PowerPC load/store instructions. DCCR and DECRAM accesses may be disabled by **BBCMCR[DCAE]** bit. Refer to **4.8.2.1 BBC Module Configuration Register BBCMCR**.

4.4.5 Reset Behavior

Upon “soft” reset the BBC switches to an idle state and all pending U-bus accesses are ignored, ICDU internal queue is flushed and IMPU switches to a disabled state where all memory space is accessible for both user and supervisor.

“Hard” reset sets some of the fields and bits in the BBC configuration registers to their default reset state. Some bits in **BBCMCR** register get their values from the Reset Configuration Word.



4.4.6 Debug Operation Mode

When the MPC565 / MPC566 RCPU core is under debug (in debug mode) the BBC initiates not-burstable access to the debug port and ICDU is bypassed, (i.e., instructions, transmitted to debug port must be non-compressed, regardless of operational mode).

4.5 Exception Table Relocation (ETR)

4.5.1 ETR Overview

The BBC is able to relocate the exception addresses of the RCPU. The relocation feature always maps the exception addresses into the internal memory space of the MPC565 / MPC566 (See **Figure 4-6**). This feature is important in multi MPC565 / MPC566 system, where although the memory map of some of them was shifted not to be on the lower 4 MB, their RCPU cores can still access their own exception handlers in their internal flash in spite of RCPU issues the same exception addresses.

The relocation also saves the wasted space between the exception table entries in the case where each exception entry contained only a branch instruction to the exception routine, which is located elsewhere.

Exception vector table may be programmed to be located in four places in MPC565 / MPC566 internal memory space.

The exception table relocation is supported in both operation modes “Decompression ON” and “Decompression OFF”.

The RESET routine vector is relocated differently in “Decompression ON” and in “Decompression OFF” modes. This feature may be used by software code compression tool to guarantee that a vocabulary table initialization routine always executed before application code running.

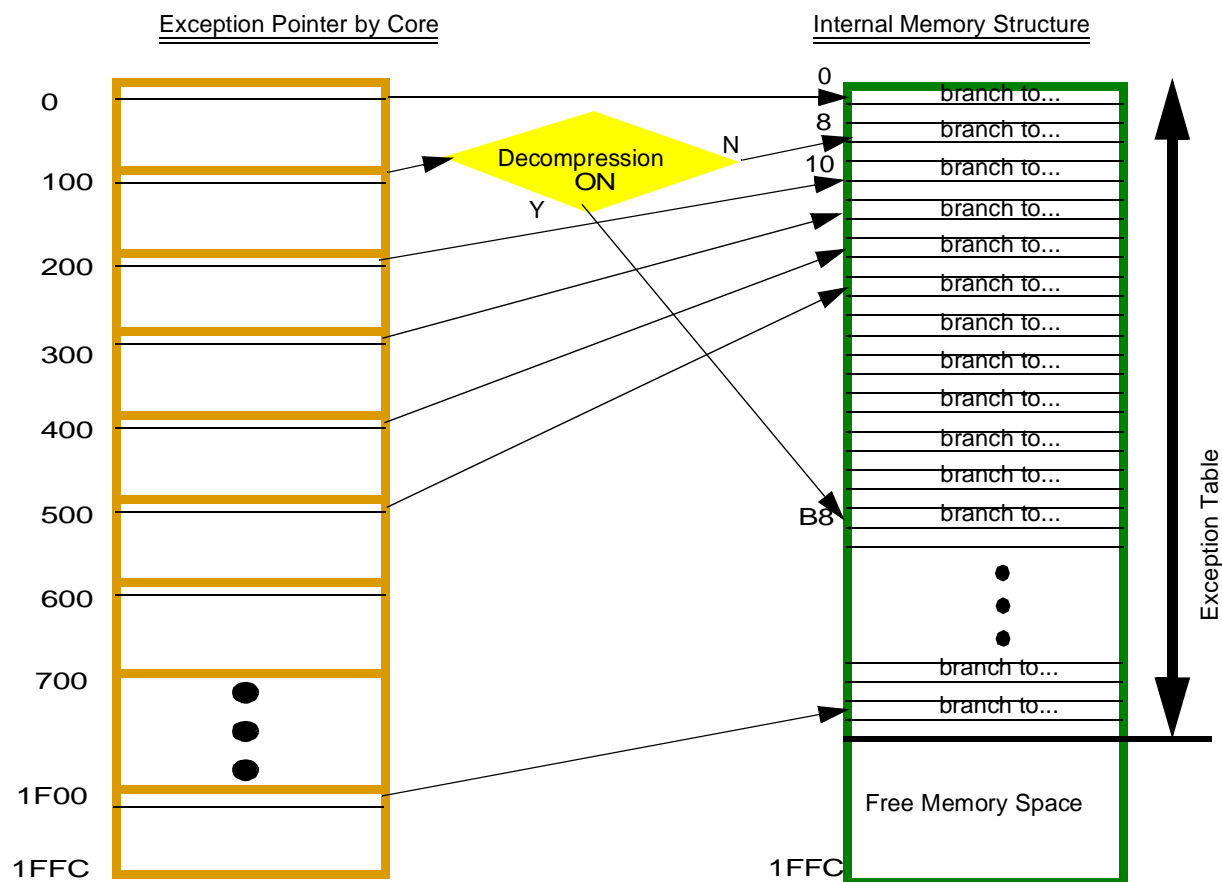


Figure 4-6 Exception Table Entries Mapping

4.5.2 ETR Operation

The exception vectors are 0x100 bytes apart from each other, starting at address 0x0000 0100 or 0xFFFF 0100, depending on the value of **MSR[IP]** bit in the RCPUR.

If the ETR is disabled, the BBC transfers the exception fetch address to the U-bus of the MPC565 / MPC566 with no interference. In this case, normal PowerPC exception addressing is implementing.

If the relocation feature is enabled, the BBC translates the exception vector into the exception relocation address. At that location, a branch instruction with absolute addressing must be placed. Each instruction branches to the required exception routine. These branch instructions should be successive in that region of the memory; that way, a table of branch instructions is implemented. Executing the branch instruction causes the core to branch twice until it gets to the exception routine.

Each exception relocation table entry occupies two words to support “Decompression ON” mode, where a branch instruction can be more than 32 bits long.

NOTES



The eight Kbytes allocated for the original PowerPC exception table can be almost fully utilized. This is possible if the MPC565 / MPC566 system memory is NOT mapped to the exception address space, (i.e., the addresses 0xFFF0_0000 to 0xFFF0_1FFF are not used).

In such case, these eight Kbytes can fully be utilized by the compiler, except for the lower 64 words (256 bytes) which are dedicated for the branch instructions.

If the RCPU, while executing an exception, issues any address between two successive exception entries (e.g., 0xFFF0_0104), then the operation of the MPC565 / MPC566 is not guaranteed if the ETR is enabled.

In order to activate the exception table relocation feature, the following steps are required:

1. Set the RCPU **MSR[IP]** bit
2. Set the **BBCMCR[ETRE]** bit. See **4.8.2.1 BBC Module Configuration Register BBCMCR** for programming details.
3. Program the **BBCMCR[OERC]** bits to determine the exception branch table location in the memory, according the description in **Table 4-2**.

The ETR feature can be activated from reset, by setting corresponded bits in the reset configuration word.

Table 4-1 Exception Addresses Mapping



Name of Exception	Original Address Issues by Core	Mapped Address by Exception Table Relocation Logic	
		EN_COMP= 0	EN_COMP= 1
System Reset	0xFFFF0_0100	Page_Offset+0x08 ¹	Page_Offset+0x0B8
Machine Check	0xFFFF0 0200	Page_Offset+0x010	
Data Storage	0xFFFF0 0300	Page_Offset+0x018	
Alignment	0xFFFF0 0600	Page_Offset+0x030	
Program	0xFFFF0 0700	Page_Offset+0x038	
Floating Point unavailable	0xFFFF0 0800	Page_Offset+0x040	
Decrementer	0xFFFF0 0900	Page_Offset+0x048	
System Call	0xFFFF0 0C00	Page_Offset+0x060	
Trace	0xFFFF0 0D00	Page_Offset+0x068	
Floating Point Assist	0xFFFF0 0E00	Page_Offset+0x070	
Implementation Dependent Software Emulation	0xFFFF0 1000	Page_Offset+0x080	
Implementation Dependent Instruction Storage Protection Error	0xFFFF0 1300	Page_Offset+0x098	
Implementation Dependent Data Storage Protection Error	0xFFFF0 1400	Page_Offset+0x0A0	
Implementation Dependent Data Breakpoint	0xFFFF0 1C00	Page_Offset+0x0E0	
Implementation Dependent Instruction Breakpoint	0x0FFF 1D00	Page_Offset+0x0E8	
Implementation Dependent Maskable External Breakpoint	0xFFFF0 1E00	Page_Offset+0x0F0	
Non-Maskable External Breakpoint	0xFFFF0 1F00	Page_Offset+0x0F8	

NOTES:

1. Refer to [Table 4-2](#).

**Table 4-2 Exception Relocation Page Offset**

BBCMCR(OERC[0:1])		Page Offset	Comments
0	0	0x0 + ISB offset ¹	0
0	1	0x1 0000 + ISB offset	64 Kbytes ²
1	0	0x8 0000 + ISB offset	512 Kbytes
1	1	0x3F E000 + ISB offset	L-bus (CALRAM) Address

NOTES:

1. ISB offset is equal $4M * ISB$ ($0x400000 * ISB$), where ISB is value of bit field in USIU IMMR register.
2. Note that this offset was 32 Kbytes on the MPC555 due to the smaller flash block size (32 Kbytes) than the MPC565 (64 Kbytes).

4.5.3 Enhanced External Interrupt Relocation (EEIR)

The BBC also supports the enhanced external interrupt model of the MPC565 / MPC566 which allows the removal of the interrupt requesting source detection stage from the interrupt routine. When the RCPU receives an external interrupt, it provides its' sole PowerPC external interrupt vector. BBC logic detects this address and replaces it with another address corresponding to the module which initiated the interrupt. See [Figure 4-7](#). Precise information about the interrupt source module is provided by the interrupt controller of USIU.

The external interrupt relocation table should start at physical address defined in the external interrupt relocation table base address register. See [4.8.2.5 External Interrupt Relocation Table Base Address Register — EIBADR](#).

Each table entry must contain a branch absolute (**ba**) instruction to the first instruction of interrupt service routine. Each table entry occupies two words (eight bytes) to support “Decompression ON” mode, where branch instruction can be more than 32 bits long.

The memory space allocated for the external interrupt relocation table is up to two Kbytes. If part of the external interrupt relocation table entries are not used, it may be utilized for another purpose as either instruction code or data.

In order to activate the external interrupt relocation feature, the following steps are required:

1. Program the [EIBADR](#) register to the external interrupt branch table base address. See [4.8.2.5 External Interrupt Relocation Table Base Address Register — EIBADR](#)
2. Set the [MSR\[IP\]](#) bit
3. Set the [BBCMCR\[EIR\]](#) bit. See [4.8.2.1 BBC Module Configuration Register BBCMCR](#) for programming details.
4. Set [SIUMCR\[EIC\]](#) bit. See [6.4.4 Enhanced Interrupt Controller](#).

NOTES

If both the enhanced external interrupt relocation and exception table relocation functions are activated simultaneously, the final external interrupt vector is defined by EEIR mechanism.

When the EEIR function is activated, any branch instruction execution with the 0xFFFF0_0500 target address may cause unpredictable program execution.

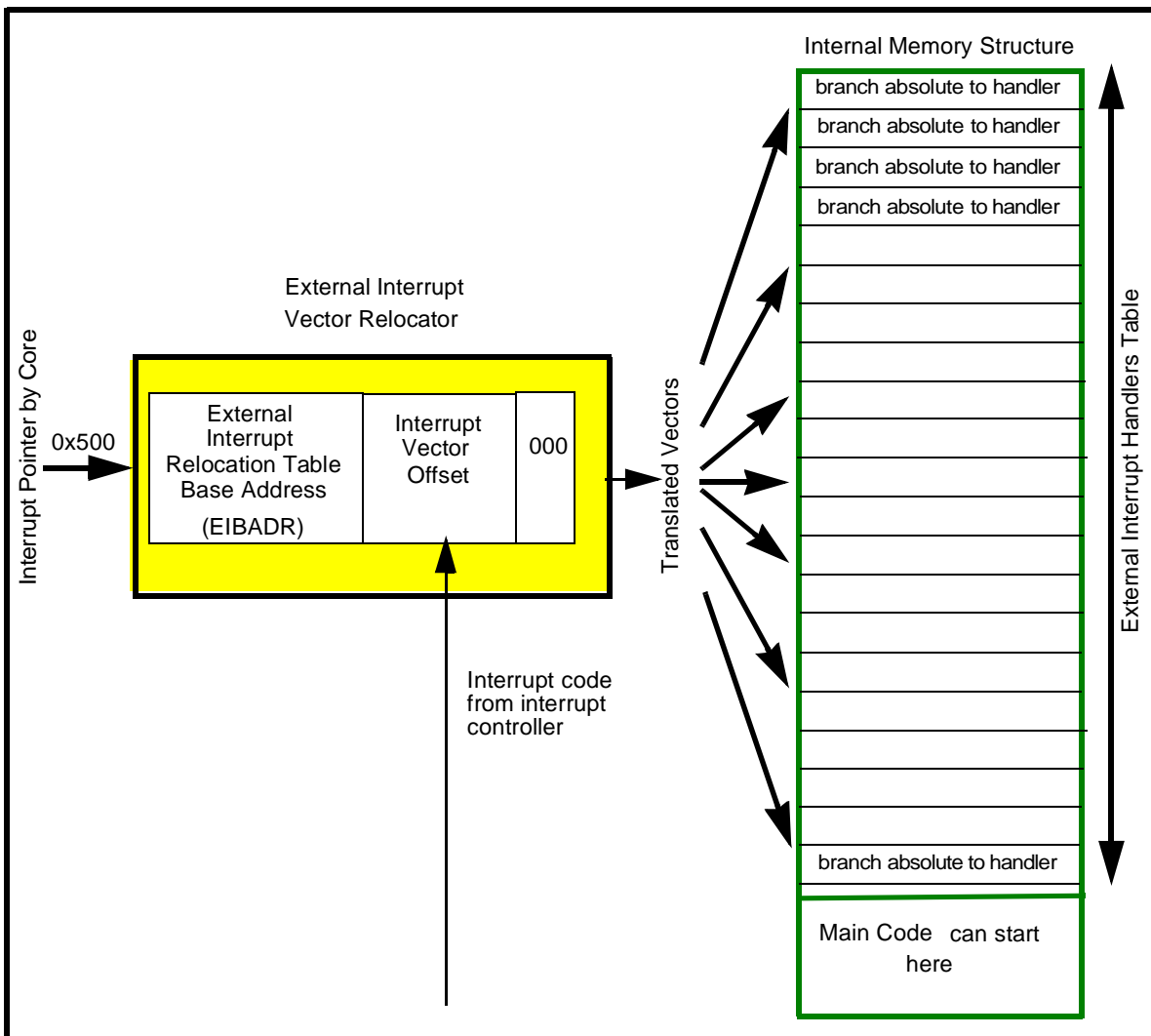


Figure 4-7 External Interrupt Vectors Splitting

4.6 Decompressor RAM (DECRAM) Functionality

Decompressor RAM (DECRAM) is a part of the ICDU. It occupies a 4-Kbyte physical RAM array block. It is mapped both in ICDU internal address space and chip memory address space. It is a single port memory and may not be accessed simultaneously from the ICDU and U-bus.

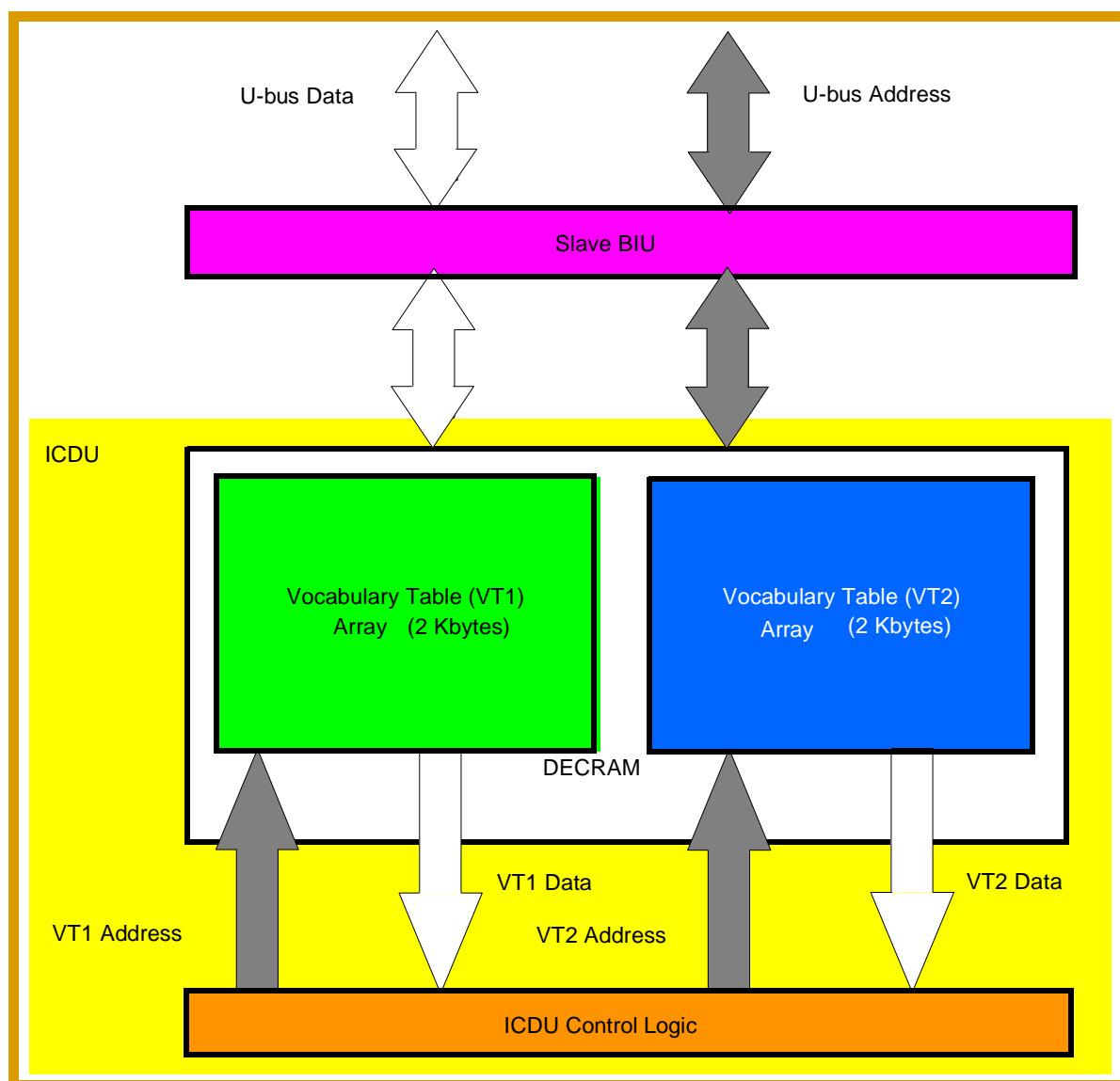


Figure 4-8 DECRAM Interfaces Block Diagram

4.6.1 Vocabulary Table Storage Operation

DECRAM is used for decompressor vocabulary tables (VT1 and VT2) storage in “Decompression ON” mode. The ICDU utilizes DECRAM as two separately accessed 2-Kbyte RAM arrays (16 bits wide) which are accessed via internal ICDU buses. The VTs should be loaded before the decompression process starts. In order to allow decompression, the DECRAM must be disabled for U-bus accesses after VTs and decompressor class configuration registers (DCCRs) are initialized.

4.6.2 General Purpose Memory Operation

In the case when “Decompression ON” mode is not activated in the chip, the DECRAM can serve as a two-clock access general purpose RAM for U-bus instruction fetches

or read/write data operations. The base address of the DECRAM is 0x2F 8000. The proper access rights to the DECRAM array may be defined by programming the R, D, and S bits of **BBCMCR** register:



- Read/write or read only
- Instruction/data or data only
- Supervisor/user or supervisor only

External access mode of the RAM is activated by the **BBCMCR[DCAE]** bit setting (see **4.8.2.1 BBC Module Configuration Register BBCMCR**). In this mode the DECRAM can be accessed from U-bus and cannot be accessed by the ICDU logic.

In this mode:

- The DECRAM supports word, half-word and byte operations.
- The DECRAM is emulated to be 32 bit wide. For example: load access from offset 0 in the DECRAM will deliver the concatenation of the first word in each of the DECRAM banks when RAM 1 contains the 16 LSB of the word and RAM 2 contains the 16 MSB.
- Load accesses at any width are supplied with 32 bits of valid data.
- The DECRAM can be accessed while the MPC565 / MPC566 is in “Decompression ON” mode, but all fetched instructions should be in the global bypass format.
- The DECRAM communicates with the U-bus pipeline but does not support pipelined accesses to itself. If a store operation is second in the U-bus pipe, the store is carried out immediately and the U-bus acknowledgment is performed when the previous transaction in the pipe completes.
- Burst access is not supported.

4.6.2.1 Memory Protection Violations

The DECRAM module does not acknowledge U-bus accesses that violate the configuration defined in the **BBCMCR**. This causes the “machine check” exception for internal RCPU or error condition for MPC565 / MPC566 external master.

4.6.2.2 DECRAM StandBy Operation Mode

The bus interface and DECRAM control logic are powered by VDD. The memory array(s) is supplied by a separate power pin (VDDSRAM3). If main power is shut off, VDDSRAM3 may subsequently be lowered for purposes of low voltage data retention.

When the DECRAM array is powered by the VDDSRAM3 pin, access to the RAM array is blocked. The application software may use **VSRMCR[LVDRS]** bit value to determine if the content of DECRAM is valid (See **8.12.4 VDDSRAM Control Register (VSRMCR)** for details).

4.7 Branch Target Buffer

In order to reduce branch impact on performance, the branch target buffer (BTB) is implemented as an optional part of the ICDU.



Following is a summary of the BTB features:

- Software controlled BTB enable/disable, lock/unlock and invalidate
- User transparent — no user management required

BTB compensates the branch and branch miss-prediction impact on system performance. It consists of eight “branch target entries” (BTE) and one “branch conditional miss-predicted entry” (BCME). Refer to [Figure 4-9](#).

All entries are managed as a fully associative cache. Each entry contains a *tag* and several data buffers related to this tag

4.7.1 BTB Operation

When the RCPU generates a Change Of Flow (COF) address for instruction fetch, the BTB control logic compares it to the tag values currently stored in the tag register file and following events can happen:

- **BTE Miss** — The target address and instruction code data will be stored in one of the BTE entries defined by its control logic. Up to four instructions and their corresponding addresses subsequent to COF target instruction may be saved in each BTE entry. The number of valid instructions currently stored in the BTE entry is written into VDC field of the current BTE entry. The “Valid” flag is set in the end of this process. The entry to be replaced upon miss is chosen based on FIFO replacement method. Thus the BTB can support up to eight different branch target addresses in a program loop.
- **BCME Miss** — Whenever the BTB logic detects that a conditional branch instruction has been transferred to the RCPU, the instructions that follow the branch conditional instruction are stored in the BCME entry. Up to four instruction codes and their adjacent addresses are saved in the BCME entry. The number of valid instructions currently stored in the BCME is written into the VDC field of BCME. The “Valid” flag is set in the end of this process.
- **BTE/BCME Hit** — When the target address of a branch matches one of the valid BTE entries or the BCME entry, two activities take place in parallel:
 - The BTB supplies all the valid instructions in the matched entry to the RCPU.
 - The ICDU (which is flushed due to the COF) starts to prefetch compressed instructions (and decompress them) from the address following the last instruction which is stored in the matched BTB entry; It will supply these instructions to the RCPU after the all stored instruction in the matched BTB entry were delivered.

Thus in case of BTB hit the impact of instruction decompression latency is eliminated as well as a latency of instruction storage memory device.

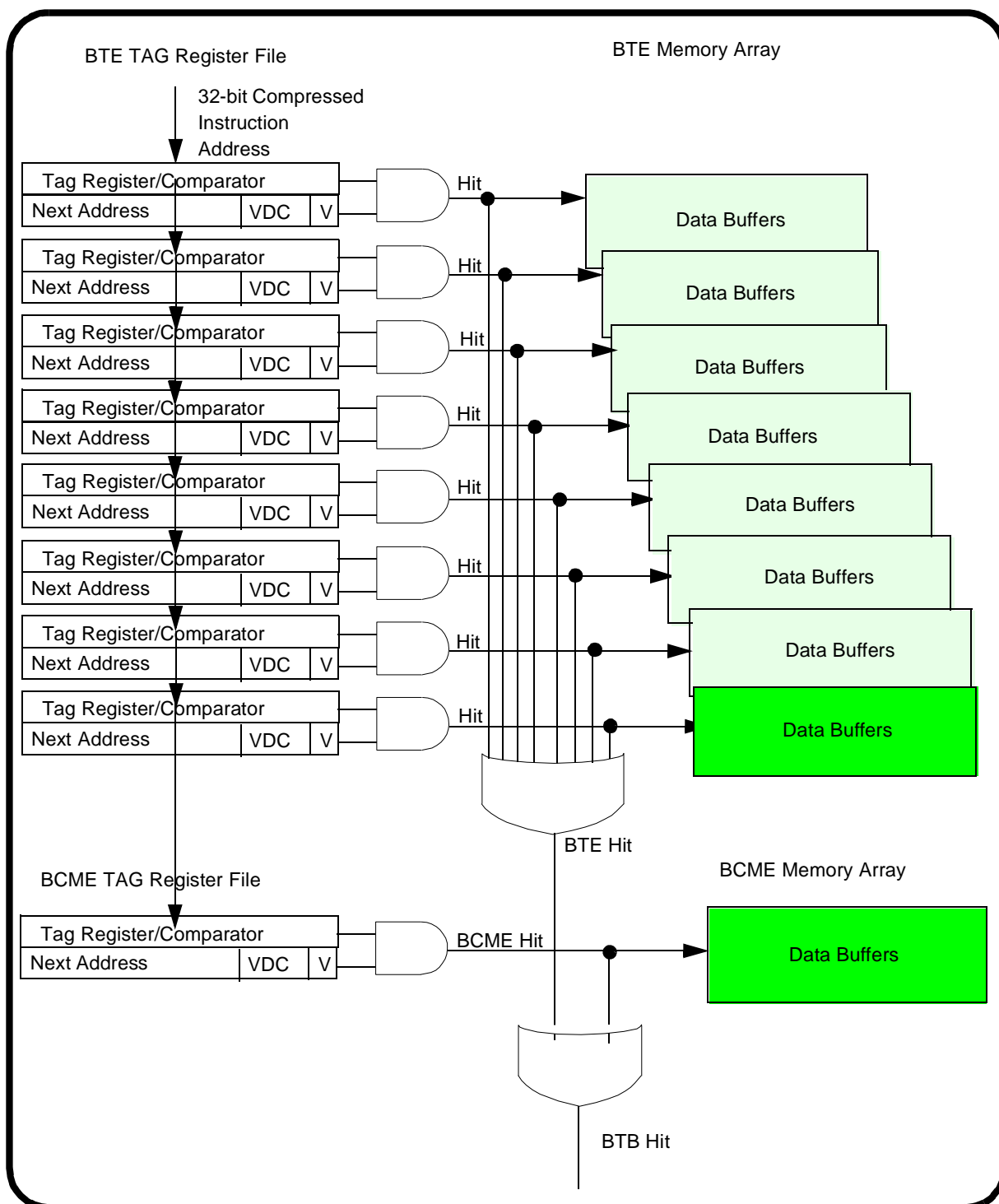


Figure 4-9 BTB Block Diagram

4.7.1.1 BTB Invalidation

Write access to any BBC special purpose register invalidates all BTB entries.

4.7.1.2 BTB Enabling/Disabling

The BTE and BCME operation may be enabled/disabled by programming **BTEE** and **BCMEE** bits in **BBCMCR** register.



4.7.1.3 BTB Inhibit Regions

The BTB operation may be inhibited for some memory regions. The BTB caching is inhibited for a region if the **BTBINH** bit set in the region attribute register (or global region attribute register). See **4.8.2.3 Region Attribute Registers MI_RA[1:3]** and **4.8.2.4 Global Region Attribute Register MI_GRA** for details.

4.8 BBC Programming Model

4.8.1 Address Map

The BBC consists of three separately addressable sections within the internal chip address space.

1. BBC and IMPU control registers. These are mapped in the SPR registers area and may be programmed by using PowerPC's **mtspr/mfspr** instructions.
2. DECompressor vocabulary RAM (DEGRAM). DEGRAM array occupies the four-Kbyte physical memory (eight-Kbyte MPC565 / MPC566 address space is allocated for DEGRAM).
3. Decompressor class configuration registers (DCCR) block. It consists of 15 de-compression class configuration registers. These registers are available for word wide read/write accesses through U-bus. The registers occupy a 64-byte physical block (eight-Kbyte chip address space is allocated for the register block).

4.8.1.1 BBC Special Purpose Registers (SPRs)



Table 4-3 BBC SPRs

SPR Number (Decimal)	Address for External Master Access (Hex)	Register Name
528	0x2100	IMPU Global Region Attribute Register (MI_GRA). See Table 4-8 for bits descriptions.
529	0x2300	External Interrupt Relocation Table Base Address Register (EIBADR). See Table 4-9 for bits descriptions.
560	0x2110	BBC Module Configuration Register (BBCMCR). See Table 4-4 for bits descriptions.
784	0x2180	IMPU Region Base Address Register 0 (MI_RBA0). See Table 4-5 for bits descriptions.
785	0x2380	IMPU Region Base Address Register 1 (MI_RBA1). See Table 4-5 for bits descriptions.
786	0x2580	IMPU Region Base Address Register 2 (MI_RBA2). See Table 4-5 for bits descriptions.
787	0x2780	IMPU Region Base Address Register 3 (MI_RBA3). See Table 4-5 for bits descriptions.
816	0x2190	IMPU Region Attribute Register 0 (MI_RA0). See Table 4-6 for bits descriptions.
817	0x2390	IMPU Region Attribute Register 1 (MI_RA1). See Table 4-6 for bits descriptions.
818	0x2590	IMPU Region Attribute Register 2 (MI_RA2). See Table 4-6 for bits descriptions.
819	0x2790	IMPU Region Attribute Register 3 (MI_RA3). See Table 4-6 for bits descriptions.

All the above registers may be accessed in the supervisor mode only. An exception is internally generated by the RCPU if there is an attempt to access them in user mode. An external master receives a transfer error acknowledge when attempting to access a register in user mode.

All the registers are reset using $\overline{\text{HRESET}}$. $\overline{\text{SRESET}}$ alone has no effect on them.

4.8.1.2 DECRAM and DCCR Block

The DECRAM occupies addresses from **0x2F8000** to **0x2F8FFF**. The DCCR block occupies addresses from **0x2FA004** to **0x2FA03F**.

Address for non-implemented memory blocks is not acknowledged, and causes an error condition.

4.8.2 BBC Registers Description



4.8.2.1 BBC Module Configuration Register BBCMCR

BBCMCR — BBC Module Configuration Register

SPR 560

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	D	S	TEST					RESERVED							
HRESET															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RE-SERVED	BE	ETRE	EIR	EN_COMP ²	EXC_COMP ²	DECOMP_SC_EN ²	OERC[0:1]	BTEE	BCMEE	RESERVED	DCAE	TST			
HRESET															
0	0	0	ID ¹ (19)	0	ID(21)	ID(22)	ID(21)	ID(24:25)	0	0	0	0	0	0	0

NOTES:

1. ID - gets value of corresponding bit of Reset Configuration Word
2. Available only on the MPC566.

Table 4-4 BBCMCR BBC Module Configuration Register Bit Description s

Bit(s)	Name	Description
0	R	Read Only — For any attempt to write to the DECRAM array while R is set, is terminated with an error. This causes a machine check exception for RCPUR. 0 = DECRAM array is Readable and Writable. 1 = DECRAM array is Read only.
1	D	Data Only — The DECRAM array may be used for Instructions and Data or for Data storage only. Any attempt to load instructions from the DCRAM array, while D is set, is terminated with an error This causes a machine check exception for the RCPUR. 0 = DECRAM array holds Data and/or Instruction. 1 = DECRAM array holds Data only.
2	S	Supervisor Only. When the bit set (S = 1), only a Supervisor program may access the DECRAM. If a Supervisor program is accessing the array, normal read/write operation will occur. If a User program is attempting to access the array, the access will be terminated with an error This causes a machine check exception for the RCPUR. If S = 0, the RAM array is placed in Unrestricted Space and access by both Supervisor and User programs is allowed.
3:7	TEST	The bits can be set in Factory test mode only, User should treat the bits as reserved
8:17	—	Reserved
18	BE	Burst Enable 0 = Burst access is disabled. 1 = Burst access is enabled.
19	ETRE	Exception Table Relocation Enable 0 = Exception Table Relocation is off: BBC does NOT map exception addresses. 1 = Exception Table Relocation is on: BBC maps exception addresses to a table holding branch instructions two memory words apart from each other. The reset value is taken from the reset configuration word bit #19.

Table 4-4 BBCMCR BBC Module Configuration Register Bit Descriptions



Bit(s)	Name	Description
20 ¹	EIR	Enhanced External Interrupt Relocation Enable— This bit activates the external interrupt relocation table mechanism. This bit is independent from the value of ETR bit, but if EIR and ETR are enabled, the mapping of external interrupt will be via EIR. 0 = EIR function is disabled. 1 = EIR function is active.
21	EN_COMP ²	Enable COMPression — This bit enables the operation of the MPC565 / MPC566 in “Compression ON” mode. The default state is disabled. This bit is read only. 0 = “Decompression ON” mode is disabled. The MPC565 / MPC566 operates only in “Decompression OFF” mode. 1 = “Decompression ON” mode is enabled. The MPC565 / MPC566 may operates with both “Decompression ON” and “Decompression OFF” modes. The bit value is determined by reset configuration word, bit #21.
22	EXC_COMP ²	Exception Compression — This bit determines the operation of the MPC565 / MPC566 with exceptions. If this bit is set, the MPC565 / MPC566 assumes that the all exception routines code is compressed; otherwise it is assumed that all exception routines code is not compressed. The reset value is determined by reset configuration word bit #22. 0 = The MPC565 / MPC566 assumes that exception routines are non-compressed 1 = The MPC565 / MPC566 assumes that ALL exception routines are compressed. This bit effects only when EN_COMP bit is set.
23	DECOMP_SC_EN ²	DECOMPRESSION Show Cycle ENable — This bit determines the way the MPC565 / MPC566 executes instruction show-cycle. The reset value is determined by configuration word bit #21. For further details regarding show cycles execution in “Decompression ON” mode see 4.4.1.2 “Decompression ON” Mode . 0 = Decompression Show Cycle does not include the bit pointer. 1 = Decompression Show Cycles includes the bit pointer information on the data bus.
24:25	OERC[0:1]	Other Exceptions Relocation Control — These bits effect only if ETRE was enabled; See details in 4.5.2 ETR Operation . 00: offset 0 01: offset 64 Kbytes 10: offset 512 Kbytes. 11: offset to 0x003FE000 (SRAM start address) The reset value is determined by reset configuration word bits #24, #25
26	BTEE ²	Branch Target Entries Enable — This bit enables Branch Target Entries of BTB operation 0 = BTE operation is disable 1 = BTE operation is enable.
27	BCMEE ²	Branch Conditional Miss-predicted Entry Enable — This bit enables Branch Conditional miss-predicted Entry of BTB operation 0 = BCME operation is disable. 1 = BCME operation is enable.
28:29	—	Reserved
30	DCAE	Decompressor Configuration Access Enable — This bit enables DECRAM and DCCR registers accesses from U-bus master (i.e. RCPU, external master). 0 = DECRAM and DCCR registers are locked. 1 = DECRAM allows accesses from the U-bus only. DCAE bit should be set before vocabulary tables loading via U-bus.
31	—	Reserved for BBC Test Operations.

NOTES:

1. Bit 20 of the BBCMCR on the MPC555/556 was OERC. The OERC bits are now bits 24:25.
2. This bit is only available on the MPC566.

BBCMCR PROGRAMMING NOTE

When writing to the **BBCMCR** register, the following instruction after **mtspr BBCMCR, Rx** should be **ISYNC**, to make sure that the programmed value will come into effect before any further action.



4.8.2.2 Region Base Address Registers MI_RBA0-3

The following registers contain 32 bits and define the starting address of the protected regions. There is one register for each of four regions.

MI_RBA[0:3] — Region Base Address Register

SPR 784 – 787

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RA															
HRESET															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RA				RESERVED											
HRESET															
U	U	U	U	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-5 MI_RBA[0:3] Registers Bit Descriptions

Bit(s)	Name	Description
0:19	RA	Region Base address. The RA field provides the base address of the region. The region base address should start on the memory block boundary for the corresponded region size, specified in the region attribute register MI_RA.
20-31	—	Reserved

NOTE

When the MPC565 / MPC566 operates “Decompression ON” mode, a minimum four unused words **MUST** be left after the last instruction in any region.

4.8.2.3 Region Attribute Registers MI_RA[1:3]

The following registers define protection attributes and size for four memory regions.

MI_RA[0:3] — Region Attribute Register

SPR 816 – 819

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RS															
HRESET															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RS				PP		RESERVED			G	CMPR'		BTBINH	RESERVED		
HRESET															
U	U	U	U	U	U	0	0	0	U	U	U	U	0	0	0



Table 4-6 MI_RA[0:3] Registers Bits Description

Bit(s)	Name	Description
0:19	RS	Region size. For byte size by region, see Table 4-7 .
20:31	PP ¹	Protection bits: 00: Supervisor — No Access, User — No Access. 01: Supervisor — Fetch, User — No Access. 1x: Supervisor — Fetch, User — Fetch.
22:24	—	Reserved
25	G	Guard attribute for region 0 = Speculative fetch is not prohibited from region. Region is not guarded. 1 = Speculative fetch is prohibited from guarded region. An exception will occur under such attempt.
26:27	CMPR ²	Compressed Region. x0 = The region is not restricted 01 = Region is considered a non-compressed code region. Access to the region is allowed only in “Decompression Off” mode 11 = Region is considered a compressed code region. Access to the region is allowed only in “Decompression On” mode
28	BTBINH ²	BTB Inhibit region 0 = BTB operation is not prohibited for current memory region 1 = BTB operation is prohibited for current memory region.
29:30	—	Reserved

NOTES:

1. G and PP attributes perform similar protection activities on a region. The more protective attribute will be implied on the region if the attributes programming oppose each other.
2. This bit is available only on MPC566.



Table 4-7 Region Size Programming Possible Values

RS field value (Binary)	Size
0000_0000_0000_0000_0000	4 Kbytes
0000_0000_0000_0000_0001	8 Kbytes
0000_0000_0000_0000_0011	16 Kbytes
0000_0000_0000_0000_0111	32 Kbytes
0000_0000_0000_0000_1111	64 Kbytes
0000_0000_0000_0001_1111	128 Kbytes
0000_0000_0000_0011_1111	256 Kbytes
0000_0000_0000_0111_1111	512 Kbytes
0000_0000_0000_1111_1111	1 Mbyte
0000_0000_0001_1111_1111	2 Mbytes
0000_0000_0011_1111_1111	4 Mbytes
0000_0000_0111_1111_1111	8 Mbytes
0000_0000_1111_1111_1111	16 Mbytes
0000_0001_1111_1111_1111	32 Mbytes
0000_0011_1111_1111_1111	64 Mbytes
0000_0111_1111_1111_1111	128 Mbytes
0000_1111_1111_1111_1111	256 Mbytes
0001_1111_1111_1111_1111	512 Mbytes
0011_1111_1111_1111_1111	1 Gbyte
0111_1111_1111_1111_1111	2 Gbytes
1111_1111_1111_1111_1111	4 Gbytes

4.8.2.4 Global Region Attribute Register MI_GRA

MI_GRA register defines protection attributes for memory region, not covered by MI_RB0-3/MI_RBA0-3 registers. It also contains protection regions 0-4 enable bits.

MI_GRA — Global Region Attribute Register

SPR 528

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ENR 0	ENR1	ENR2	ENR3	RESERVED											
HRESET															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RESERVED				PP		RESERVED			G	CMPR		BTBINH	RESERVED		
HRESET															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-8 MI_GRA Global Region Attribute Register Bits Description



Bit(s)	Name	Description
0	ENR0	Enable IMPU Region 0 0 = Region 0 is off. 1 = Region 0 is on.
1	ENR1	Enable IMPU Region 1 0 = Region 1 is off. 1 = Region 1 is on.
2	ENR2	Enable IMPU Region 2 0 = Region 2 is off. 1 = Region 2 is on.
3	ENR3	Enable IMPU Region 3 0 = Region 3 is off. 1 = Region 3 is on.
4:19	—	Reserved
20:21	PP	Protection Bits 00: Supervisor – No Access, User – No Access. 01: Supervisor – Fetch, User – No Access. 1x: Supervisor – Fetch, User – Fetch.
22:24	—	Reserved
25	G	Guard attribute for region 0 = Fetch is not prohibited from region. Region is not guarded. 1 = Fetch is prohibited from guarded region. An exception will occur under such attempt.
26:27	CMPR ¹	Compressed Region. x0 = The region is not restricted. 01 = Region is considered a non-compressed code region. Access to the region is allowed only in “Decompression Off” mode. 11 = Region is considered a compressed code region. Access to the region is allowed only in “Decompression On” mode.
28	BTBINH ²	BTB Inhibit region 0 = BTB operation is not prohibited for current memory region. 1 = BTB operation is prohibited for current memory region.
29:31	—	Reserved

NOTES:

1. This bit is only available on the MPC566.

NOTE

The MI_GRA register should be programmed to enable fetch access (PP and G bits) before RCPUR MSR[IR] bit is set.

4.8.2.5 External Interrupt Relocation Table Base Address Register — EIBADR



EIBADR — External Interrupt Relocation Table Base Address Register

SPR 529

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Base Address															
HRESET															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
Base Address					RESERVED										
HRESET															
U	U	U	U	0	0	0	0	0	0	0	0	0	0	0	0

**Table 4-9 EIBADR External Interrupt Relocation Table
Base Address Register Bit Descriptions**

Bit(s)	Name	Description
0:20	BA	External Interrupt Relocation Table Base Address bits [0:20]
21:31	—	Reserved

4.8.2.6 Decompressor Class Configuration Registers (DCCR1-15)

The DCCR fields are programmed to achieve maximum flexibility in the vocabulary tables placement into the two DECRAM banks under constraints, implied by hardware, which are:

- a bypass field must always be the second field in the compressed instruction;
- when fetching 32 bits of de-compressed instruction from the DECRAM, each 16 bits will be read from different RAM banks.

The DCCR registers should be programmed with data supplied by the code compression tool, in order to be correlated with the compressed code.

4.8.2.7 Decompressor Class Configuration Registers (DCCR1-DCCR15)

DCCR1 — Decompressor Class Configuration Registers	0x2F A004
DCCR2	0x2F A008
DCCR3	0x2F A00C
DCCR4	0x2F A010
DCCR5	0x2F A014
DCCR6	0x2F A018
DCCR7	0x2F A01C
DCCR8	0x2F A020
DCCR9	0x2F A024
DCCR10	0x2F A028
DCCR11	0x2F A02C
DCCR12	0x2F A030
DCCR13	0x2F A034
DCCR14	0x2F A038
DCCR15	0x2F A03C

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
TP1LEN				TP2LEN				TP1BA							TP2BA	
HRESET																
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31	
TP2BA						AS		DS		RESERVED						
HRESET																
U	U	U	U	0	U	U	U	0	0	0	0	0	0	0	0	



**Table 4-10 DCCR0-DCCR15 Decompressor Class
Configuration Registers Bit Descriptions**

Bit(s)	Name	Description
0:3	TP1LEN	Length and Type of Table Pointer 1 — This field's value defines the length of the field that contains a pointer to the first vocabulary table allocated for the class. 0x0 - Empty field 0x1 - Reserved 0x2 - TP1 length is 2 bits 0x3 - TP1 length is 3 bits 0x4 - TP1 length is 4 bits 0x5 - TP1 length is 5 bits 0x6 - TP1 length is 6 bits 0x7 - TP1 length is 7 bits 0x8 - TP1 length is 8 bits 0x9 - TP1 length is 9 bits 0xA to 0xF - Reserved
4:7	TP2LEN	Length and Type of Table Pointer 2 — This field's value defines the length of the field that contains either a pointer to the second vocabulary table allocated for the class or a bypass field. 0x0 - Empty field 0x1 - Reserved 0x2 - TP2 length is 2 bits 0x3 - TP2 length is 3 bits 0x4 - TP2 length is 4 bits 0x5 - TP2 length is 5 bits 0x6 - TP2 length is 6 bits 0x7 - TP2 length is 7 bits 0x8 - TP2 length is 8 bits 0x9 - TP2 length is 9 bits 0xA - Reserved 0xB - Reserved 0xC - TP2 field is a 10 bits compact bypass field 0xD - TP2 field is a 15 bits compact bypass field 0xE - TP2 field is a 16 bits bypass field 0xF - Reserved.
8:14	TP1BA	Base address for vocabulary table in RAM Bank 1 — This field specifies the base page address of the class' vocabulary table that resides in RAM Bank 1.
15:21	TP2BA	Base address for vocabulary table in RAM Bank 2 — This field specifies the base page address of the class' vocabulary table that resides in RAM Bank 2.
22	AS	Address Swap specification 0 = Address swap operation will not be performed for the class. 1 = Address swap operation will be performed for the class For further details concerning AS operation refer to Table 4-11 .
23	DS	Data swap specification 0 = Data swap operation will not be performed for the class. 1 = Data swap operation will be performed for the class. For further details concerning DS operation refer to Table 4-11 .
24:31	—	Reserved



Table 4-11 Instruction Layout Encoding

Configuration	Configuration Code	TP1 Points To RAM #	TP2 Points To RAM #	TP1BA Points To		TP2BA Points To		AS	DS	Compressed Instruction Layout
				RAM #	Vocab.	RAM #	Vocab.			
Single Segment Full Compression	CLASS 1	1 and 2	—	1	V1	2	V2	—	—	X1 ¹
Twin Segments Full Compression	CLASS 2a	1	2	1	V1	2	V2	—	0	X1 X2
Twin Segments Full Compression With Swapped Vocabularies (Vocabulary In RAM #2 For MSB Segment)	CLASS 2b				V2		V1		1	X2 X1
Left Segment Compression, Right Segment Bypassed, Vocabulary In RAM #1	CLASS 3a	1	Bypass	1	V1	—	—	0	0	X1 BP ²
Left Segment Compression, Right Segment Bypassed, Vocabulary In RAM #2	CLASS 3b	2		—	-	2	V1	1		X1 BP
Left Segment Bypassed, Right Segment Compression, Vocabulary In RAM #1	CLASS 4b	1		1	V2	—	—	0	1	X2 BP
Left Segment Bypassed, Right Segment Compression, Vocabulary In RAM #2	CLASS 4a	2		—	—	2	V2	1		X2 BP

NOTES:

1. X1,X2 - pointers to vocabularies
2. BP - the bypassed data