

Freescale Semiconductor Advance Information

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MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410RX*nnn*PC Series

This document describes part number specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7410 Hardware Specifications* (Document No. MPC7410EC).

Specifications provided in this Part Number Specification supersede those in the *MPC7410 Hardware Specifications*, for the part numbers listed in Table A only, specifications not addressed herein are unchanged. This document is frequently updated. Therefore, contact your Freescale sales office for the latest version.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Table 17.

Freescale Part Numbers Affected:

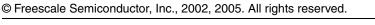
XPC7410RX400PC

XPC7410RX450PC

XPC7410RX500PC

XPC7410RX550PC

This document contains information on a new product. Specifications and information herein are subject to change without notice.







Features

Table A. Part Numbers Addressed by this Data Sheet

Freescale Part	Operat	ing Condition	s	Cinnificant Differences from Hardway
Number	CPU Frequency	Vdd	T _J (°C)	Significant Differences from Hardware Specification
XPC7410RX400PC	400 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 400Mhz frequency
XPC7410RX450PC	450 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 450Mhz frequency
XPC7410RX500PC	500 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 500Mhz frequency
XPC7410RX550PC	550 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 550Mhz frequency

Notes:

The X prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

2 Features

There are no changes to the features of the MPC7410 described in the MPC7410 Hardware Specifications (MPC7410EC).

4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7410 part numbers described herein.

Table 3. Recommended Operating Conditions

Charact	eristic	Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.0V±50mV	V
PLL supply voltage		AVdd	2.0V±50mV	V
L2 DLL supply voltage		L2AVdd	2.0V±50mV	V
Processor bus supply voltage	BVSEL = 1 or BVSEL = HRESET	OVdd	2.5V±125mV	V
	BVSEL = GND	Symbol Value U Vdd 2.0V±50mV AVdd 2.0V±50mV L2AVdd 2.0V±50mV or OVdd 2.5V±125mV RESET ND OVdd 1.8V±90mV or L2OVdd 2.5V±125mV	V	
L2 bus supply voltage	L2VSEL = 1 or L2VSEL = HRESET	L2OVdd	2.5V±125mV	V
	L2VSEL = GND	L2OVdd	1.8V±90mV	V

MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410RXnnnPC Series, Rev. 1.1



Table 3. Recommended Operating Conditions (continued)

Charac	teristic	Symbol	Recommended Value	Unit	
Input voltage	Processor bus	V _{in}	GND to OVdd	V	
	L2 Bus				
	JTAG Signals	V _{in}	GND to OVdd	V	
Die-junction temperature	9	Tj	0-65	°C	

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 6 provides the power consumption for the MPC7410 part at the frequencies described herein.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	500Mhz		
Full-On Mode				
Typical	6	7	W	1, 3,
Maximum	12	14	W	1, 2, 4
Doze Mode				
Maximum	4	5	W	1, 2
Nap Mode				
Maximum	2.0	2.25	W	1, 2
Sleep Mode				
Maximum	2.0	2.25	W	1, 2
Sleep Mode—PLL and DL	L Disabled			
Typical	0.5	0.5	W	1, 3



Table 6. Power Consumption for MPC7410 (continued)

	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	500Mhz		
Maximum	2.0	2.0	W	1, 2

Notes:

- These values apply for all valid processor bus and L2 bus ratios. The values
 do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply
 power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent,
 but is typically <10% of Vdd power. Worst case power consumption for AVdd
 = 15 mw and L2AVdd = 15 mW.
- 2. Maximum power is measured at Vdd = 2.2V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
- Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.15V, OVdd = L2OVdd = 2.5V in a system while running a codec application that is AltiVec intensive.
- These values include the use of Altivec. Without Altivec operation, estimate a 25% decrease.

4.2.1 Clock AC Specifications

Table 7 provides the additional clock AC timing specifications described in this Part Number Specification. Refer to the *MPC7410 Hardware Specification* for the remaining frequencies.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (See Table 3)

Characteristic	Symbol	400	MHz	450	MHz	500	MHz	550	MHz	Unit	Notes
Onaracteristic	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Oiiii	Notes
Processor frequency	f _{core}	300	400	300	450	300	500	300	550	MHz	
VCO frequency	f _{VCO}	600	800	600	900	600	1000	600	1100	MHz	
SYSCLK frequency	f _{SYSCLK}	33	100	33	100	33	100	33	100	MHz	1
SYSCLK cycle time	t _{SYSCLK}	10	30	10	30	10	30	10	30	ns	
SYSCLK rise and	t _{KR} & t _{KF}	_	1.0	_	1.0	_	1.0	_	1.0	ns	2
fall time		_	0.5	_	0.5	_	0.5	_	0.5	ns	3
SYSCLK duty cycle measured at OVdd/2	t _{KHKL} /t _{SYS} CLK	40	60	40	60	40	60	40	60	%	4
SYSCLK jitter		_	±150	_	±150	_	±150	_	±150	ps	5



Table 7. Clock AC Timing Specifications (continued)

At recommended operating conditions (See Table 3)

Characteristic	Symbol	400 MHz		450	450 MHz		500 MHz		550 MHz		Notes
	Cymbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	110.63
Internal PLL relock time		_	100	_	100	_	100	_	100	μS	6

Note:

See general hardware specification.

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 part described in this Part Number Specification.

Table 8. Processor Bus AC Timing Specifications

 $At \ Vdd = AVdd = 2.0V \pm 50mV; \ 0 \le Tj \le 65^{\circ}C, \ OVdd = 2.5V \pm 0.125V \ and \ OVdd = 1.8V \pm 0.090V, \ 60X \ bus \ at \ 100MHz \ bus \ at \ 1$

Parameter	Symbol		60, 500, Mhz	Unit	Notes
		Min	Max		
Mode select input setup to HRESET	t _{MVRH}	8	_	t sysclk	2,3,4,5
HRESET to mode select input hold	t _{MXRH}	0	_	ns	2,3,5
Setup Times: Address/Transfer Attribute Transfer Start (TS) Data/Data Parity ARTRY/SHD0/SHD1 All Other Inputs	t _{AVKH} t _{TSVKH} t _{DVKH} t _{ARVKH} t _{IVKH}	1.4 1.4 1.4 1.4 1.4	_ _ _ _	ns	10 6 7 8
Input Hold Times: Address/Transfer Attribute Transfer Start (TS) Data/Data Parity ARTRY/SHD0/SHD1 All Other Inputs	t _{AXKH} t _{TSXKH} t _{DXKH} t _{ARXKH} t _{IXKH}	0 0 0 0	_ _ _ _	ns	11 6 7 8
Valid Times: Address/Transfer Attribute TS, ABB, DBB Data Data Parity ARTRY/SHD0/SHD1 All Other Outputs	tkhav tkhtsv tkhdv tkhdpv tkharv tkhov	_ _ _ _ _	3.0 3.0 3.5 3.5 2.3 3.0	ns	12 6 7 7 9



DC Electrical Characteristics

Table 8. Processor Bus AC Timing Specifications (continued)

 $At \ Vdd = AVdd = 2.0 \\ V \pm 50 \\ mV; \ 0 \le T_j \le 65 \\ ^{\circ}C, \ OVdd = 2.5 \\ V \pm 0.125 \\ V \ and \ OVdd = 1.8 \\ V \pm 0.090 \\ V, \ 60X \ bus \ at \ 100 \\ MHz \ b$

Parameter	Symbol	-	60, 500, Mhz	Unit	Notes
		Min	Max		
Output Hold Times: Address/Transfer Attribute TS, ABB, DBB Data/Data Parity ARTRY/SHD0/SHD1 All Other Outputs	[†] KHAX [†] KHTSX [†] KHDX [†] KHARX [†] KHOX	0.75 0.75 0.6 0.75 0.75		ns	13 6 7 9
SYSCLK to Output Enable	t _{KHOE}	0.5	_	ns	14
SYSCLK to Output High Impedance (all except TS, ABB/AMON(0), ARTRY/SHD, DBB/DMON(0)	t _{KHOZ}	_	3.5	ns	15
SYSCLK to TS, ABB/AMON(0), DBB/DMON(0) High Impedance after precharge	t _{KHABPZ}	_	1.0	t _{sysclk}	4,15, 16,17
Maximum Delay to ARTRY/SHD0/SHD1 Precharge	t _{KHARP}	_	1	t sysclk	4,17
SYSCLK to ARTRY/SHD0/SHD1 High Impedance After Precharge	t _{KHARPZ}	_	2	tsysclk	4,17

Note:

See general hardware specification.

4.2.3 L2 Clock AC Specifications

Table 9 provides the L2CLK Output AC Timing Specifications for the MPC7410 part described in this Part Number Specification

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		Unit	Notes
Farameter		Min	Max	Min	Max	Min	Max	Min	Max	J	Notes
L2CLK frequency	f _{L2CLK}	150	200	150	225	150	250	150	275	MHz	1
L2CLK cycle time	t _{L2CLK}	5	6.67	4.4	6.67	4	6.67	3.6	6.67	ns	
L2CLK duty cycle	t _{CHCL} / t _{L2CLK}	5	50	5	50	5	50	5	50	%	2
Internal DLL-relock time		640		640	_	640	_	640	_	L2CLK	4

MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410RXnnnPC Series, Rev. 1.1



Table 9. L2CLK Output AC Timing Specifications (continued)

At recommended operating conditions (See Table 3)

Parameter	Symbol	400 MHz		450	450 MHz		500 MHz		550 MHz		Notes
	Cymbol	Min	Max	Min	Max	Min	Max	Min	Max	- Unit	110103
DLL capture window			±200		±200		±200		±200	ns	5

Note:

See general hardware specification.

4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this Part Number Specification.

Table 10. L2 Bus Interface AC Timing Specifications

Parameter	Symbol	400	MHz	450	MHz	500 I	ИНz	550	MHz	Unit	No
Faranielei	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	n <u>i</u>	Notes
L2SYNC_IN rise and fall time	t _{L2CR} & t _{L2CF}	_	1.0	_	1.0	_	1.0	_	1.0	ns	1
Setup Times: Data and parity	t _{DVL2CH}	1.5	_	1.375	_	1.250	_	1.125		ns	2
Input Hold Times: Data and parity	t _{DXL2CH}	_	0.0	_	0.0	_	0.0	_	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t _{L2CHOV}		2.5 TBD TBD TBD		2.375 TBD TBD TBD	- - -	2.25 TBD TBD TBD	- - -	2.05 TBD TBD TBD	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	^t L2CHOX	0.6 TBD TBD TBD	- - -	0.55 TBD TBD TBD	- - -	0.5 TBD TBD TBD	- - -	0.45 TBD TBD TBD		ns	3
L2SYNC_IN to high impedance All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	^t L2CHOZ	- - -	2.0 2.5 3.0 3.5	- - -	2.0 2.5 3.0 3.5	- - -	2.0 2.5 3.0 3.5	- - -	2.0 2.5 3.0 3.5	ns	

Note:

See general hardware specification.



Document Revision History

9 Document Revision History

Table 16. provides a revision history for this Part Number Specification.

Table 16. Document Revision History

Revision	Date	Substantive Changes	
1.1	4/19/2005	Document template update	
		Document ID change from MPC7410RXPCPNS for Part Number Specification to MPC7410ECS03AD for Hardware Specification Addendum.	
1	9/2002	Minor reformatting	
		Section 1.10.1 - added Table 17, Part Marking Nomenclature	
0		Initial Release	

10 Ordering Information

MPC 7410

10.1 Part Numbers Addressed by this Specification

RX

Table 17 provides the ordering information for the MPC7410 part described in this document.

YYY

Table 17. Part Marking Nomenclature

Y

•			717171	24	71
Product Code	Part Identifier	Package	Processor Frequency ¹	Application Modifier	Revision Level
XPC	7410	RX = CBGA	450 500 550	P: 2.0 V ± 50 mV 0 to 65 °C	C: 1.2; PVR = 800C 1102

Notes:

MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410RXnnnPC Series, Rev. 1.1

^{1.} Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.

^{2.} The X prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.



10.3 Part Marking

Parts are marked as the example shown in Figure 26.



Notes:

nnn is the speed grade of the part MMMMMM is the 6-digit mask number ATWLYYWWA is the traceability code BGA

CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

Figure 26. Freescale Part Marking for BGA Device



Ordering Information

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MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410RXnnnPC Series, Rev. 1.1





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Rev. 1.1 04/2005

