Pressure

NP

Freescale Semiconductor

Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXV4006 series piezoresistive transducers are state-of-the-art monolithic silicon pressure sensors designed for the appliance, consumer, health care and industrial market. The analog output can be read directly into the A/D input of Freescale microcontrollers. This transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure. The axial port has been modified to accommodate industrial grade tubing.

Features

- 2.5% Maximum Error over +10°C to +60°C with Auto Zero
- 5% Maximum Error over +10°C to +60°C without Auto Zero
- Durable Thermoplastic (PPS) Package
- Available in Surface Mount (SMT) or Through-Hole (DIP) Configurations
- Available with Standard Fluorosilicone Gel or Media Resistant Gel

MPXV4006 Series Integrated Pressure Sensor

0 to 6 kPa (0 to 0.87 psi) 0.2 to 4.8 V Output

Application Examples

- Washing Machine Water Level Measurement (Reference AN1950)
- Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Appliance Liquid Level and Pressure Measurement
- Respiratory Equipment

				ORD	ERING	G INFOF	RMATION				
	Package		#	t of Ports	;		Pressure Type		Option		Device
Device Name	Options		None	Single	Dual	Gauge	Differential	Absolute	Surface Mount	Through- Hole	Device Marking
Small Outline Pac	kage (Media	Resistant	Gel) (M	PVZ4006	Serie	s)	•	•			
MPVZ4006GW6U	Rail	1735		•		•			•		MZ4006GW
MPVZ4006GW7U	Rail	1560		•		•				•	MZ4006GW
MPVZ4006G6U	Rail	482	•				•		•		MPVZ4006G
MPVZ4006G6T1	Tape and Reel	482	•				•		•		MPVZ4006G
MPVZ4006G7U	Rail	482B	•				•			•	MPVZ4006G
Small Outline Pac	kage (MPXV	4006 Serie	s)	1			ı				
MPXV4006GC6U	Rail	482A		•		•			•		MPXV4006G
MPXV4006GC6T1	Tape and Reel	482A		•		•			•		MPXV4006G
MPXV4006GC7U	Rail	482C		•		•				٠	MPXV4006G
MPXV4006GP	Tray	1369		•		•			•		MPXV4006GP
MPXV4006DP	Tray	1351			•		•		•		MPXV4006DP



MPXV4006 Rev 3, 1/2009



SMALL OUTLINE PACKAGE SURFACE MOUNT









MPVZ4006G6U/T1

CASE 482-01



MPXV4006DP

MPXV4006GC6U/C6T1 CASE 482A-01

SMALL OUTLINE PACKAGE THROUGH-HOLE

MPVZ4006G7U

CASE 482B-03

CASE 1351-01



MPXV4006GC7U CASE 482C-03



MPVZ4006GW7U CASE 1560-02

Operating Characteristics

Table 1. Operating Characteristics ($V_S = 5.0 \text{ Vdc}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted, P1 > P2)

Characteristic	Symbol	Min	Тур	Max	Unit
Pressure Range	P _{OP}	0	_	6.0 612	kPa mm H ₂ O
Supply Voltage ⁽¹⁾	V _S	4.75	5.0	5.25	Vdc
Supply Current	۱ _S	_	—	10	mAdc
Full Scale Span ⁽²⁾	V _{FSS}	_	4.6	_	V
Offset ⁽³⁾⁽⁵⁾	V _{off}	0.152	0.265	0.378	V
Sensitivity	V/P	—	766 7.511	_	mV/kPa mV/mm H ₂ O
Accuracy ⁽⁴⁾⁽⁵⁾ (10 to 6		_	_	±2.46	%V _{FSS} with auto zero
	_	-	_	±5.0	%V _{FSS} without auto zero

1. Device is ratiometric within this specified excitation range.

2. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.

3. Offset (Voff) is defined as the output voltage at the minimum rated pressure.

4. Accuracy (error budget) consists of the following:

Linearity:	Output deviation from a straight line relationship with pressure over the specified pressure range.
Temperature Hysteresis:	Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
Pressure Hysteresis:	Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum or maximum rated pressure, at 25°C.
Offset Stability:	Output deviation, after 1000 temperature cycles, -30 to 100°C, and 1.5 million pressure cycles, with minimum rated pressure applied.
TcSpan:	Output deviation over the temperature range of 10° to 60° C, relative to 25° C.
TcOffset:	Output deviation with minimum pressure applied, over the temperature range of 10° to 60°C, relative to 25°C.

5. Auto Zero at Factory Installation: Due to the sensitivity of the MPXV4006, external mechanical stresses and mounting position can affect the zero pressure output reading. To obtain the 2.46% FSS accuracy, the device output must be "autozeroed" after installation. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. The specified accuracy assumes a maximum temperature change of ±5°C between autozero and measurement.



Maximum Ratings

Table 2. Maximum Ratings⁽¹⁾

Parametrics	Symbol	Value	Units
Maximum Pressure (P1 > P2)	P _{max}	24	kPa
Storage Temperature	T _{stg}	-30° to +100°	°C
Operating Temperature	T _A	+10° to +60°	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

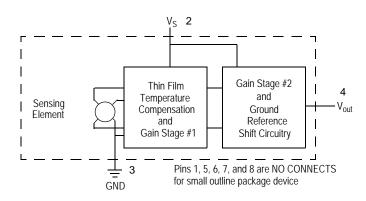


Figure 1. Fully Integrated Pressure Sensor Schematic

On-Chip Temperature Compensation and Calibration

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the Differential or Gauge configuration in the basic chip carrier (Case 482). A gel die coat isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPXV4006/MPVZ4006 series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and

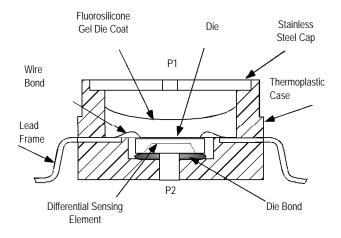


Figure 2. Cross Sectional Diagram SOP (not to scale)

gualification test for dry air, and other media, are available from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the output of the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 and Figure 5 shows the sensor output signal relative to pressure input. Typical, minimum and maximum output curves are shown for operation over a temperature range of 10°C to 60°C using the decoupling circuit shown in Figure 3. The output will saturate outside of the specified pressure range.

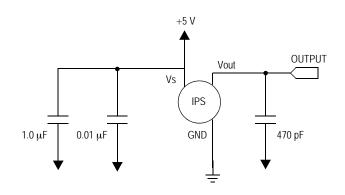
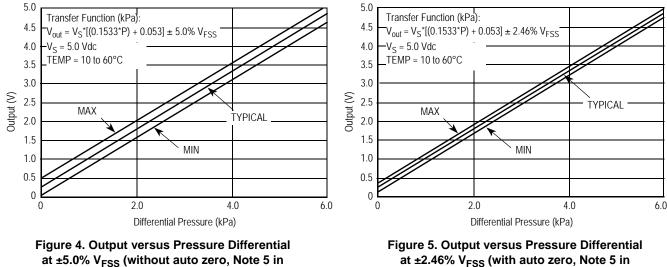
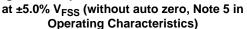


Figure 3. Recommended Power Supply Decoupling and Output Filtering Recommendations (For additional output filtering, please refer to Application Note AN1646.)

Operating Characteristics)





MPXV4006



PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing a gel die coat which isolates the die from the environment. The pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below:

Table 3. Pressure (P1)/Vacuum (P2) Side Identification Table

Part Number	Case Type	Pressure (P1) Side Identifier
MPVZ4006GW6U	1735-01	Vertical Port Attached
MPVZ4006GW7U	1560-02	Vertical Port Attached
MPVZ4006G6U/T1	482-01	Stainless Steel Cap
MPVZ4006G7U	482B-03	Stainless Steel Cap
MPXV4006GC6U/T1	482A	Vertical Port Attached
MPXV4006GC7U	482C-03	Vertical Port Attached
MPXV4006GP	1369-01	Side with Port Attached
MPXV4006DP	1351-01	Side with Part Marking

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct

footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

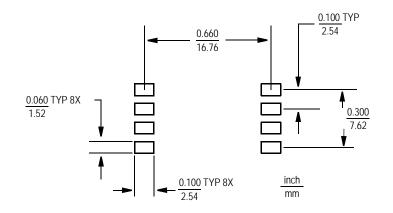
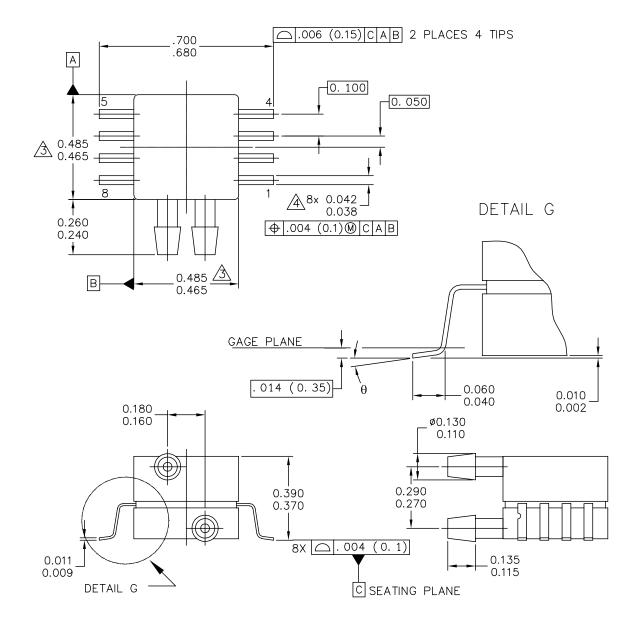


Figure 6. SOP Footprint (Case 482)





© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NO	DT TO SCALE
TITLE:	DOCUMENT NO): 98ASA99255D	REV: A
8 LD SNSR. DUAL P	PORT CASE NUMBER	R: 1351–01	27 JUL 2005
	STANDARD: NO	DN-JEDEC	

CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE



NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

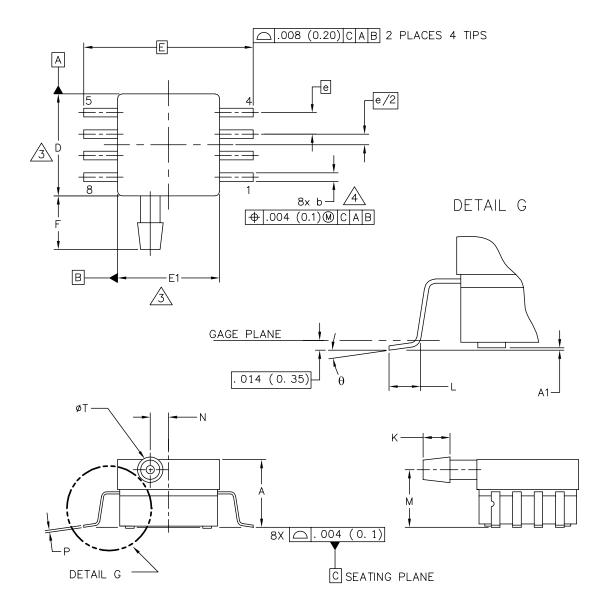
A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

STYLE 1:		STYLE 2:	
PIN 1:	GND	PIN 1:	N/C
PIN 2:	+Vout	PIN 2:	Vs
PIN 3:	Vs	PIN 3:	GND
PIN 4:	-Vout	PIN 4:	Vout
PIN 5:	N/C	PIN 5:	N/C
PIN 6:	N/C	PIN 6:	N/C
PIN 7:	N/C	PIN 7:	N/C
PIN 8:	N/C	PIN 8:	N/C

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICA	LOUTLINE	PRINT VERSION NOT TO SCALE	
TITLE:		DOCUMENT NO): 98ASA99255D	REV: A
8 LD SNSR, DUAL	PORT	CASE NUMBER	8: 1351-01	27 JUL 2005
		STANDARD: NO	N-JEDEC	

CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE





© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NO	DT TO SCALE
TITLE:	DOCUMENT NO): 98ASA99303D	REV: B
8 LD SOP, SIDE POF	RT CASE NUMBER	8: 1369–01	24 MAY 2005
	STANDARD: NO	N-JEDEC	

CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE



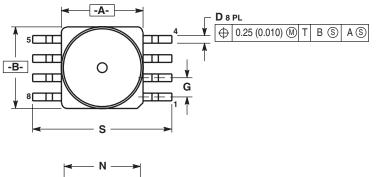
NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- △ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.
- A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

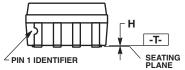
	INC	HES	MIL	LIMETERS		I	NCHES	MILLIMETERS	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	. 300	. 330	7.11	7.62	θ	0°	7 °	0°	7°
A 1	. 002	. 010	0. 05	0. 25	-				
b	. 038	. 042	0.96	1.07	-				
D	. 465	. 485	11.81	12.32	-				
E	. 717	BSC	18	.21 BSC	-				
E1	. 465	. 485	11.81	12.32	-				
e	. 100	BSC	2.	2.54 BSC					
F	. 245	. 255	6. 22	6.47	-				
к	. 120	. 130	3. 05	3. 30	-				
L	. 061	. 071	1. 55	1.80	-				
м	. 270	. 290	6.86	7.36	-				
N	. 080	. 090	2. 03	2. 28	-				
Р	. 009	. 011	0. 23	0. 28	-				
Т	. 115	. 125	2. 92	3. 17	-				
©	FREESCALE SEN ALL RIGH	ICONDUCTOR, TS RESERVED.	INC.	MECHANICA	LOU	TLINE	PRINT VER	L SION NO	DT TO SCALE
ΤΙΤΙ	TITLE:				DOCI	JMENT NO): 98ASA9930	3D	REV: B
	8 LD SOP, SIDE PORT				CASE	E NUMBER	8: 1369–01		24 MAY 2005
	,				STA	NDARD: NO	N-JEDEC		

CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE





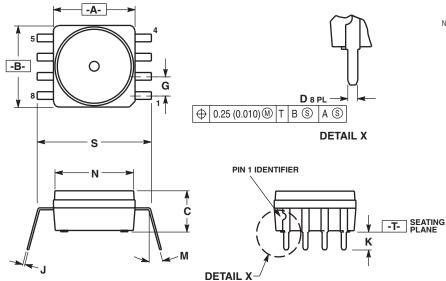




NOTES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.212	0.230	5.38	5.84
D	0.038	0.042	0.96	1.07
G	0.100	BSC	2.54 BSC	
Н	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
Κ	0.061	0.071	1.55	1.80
Μ	0°	7°	0°	7°
Ν	0.405	0.415	10.29	10.54
S	0.709	0.725	18.01	18.41

CASE 482-01 **ISSUE O** SMALL OUTLINE PACKAGE



NOTES:

DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 1.

2. CONTROLLING DIMENSION: INCH.

DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

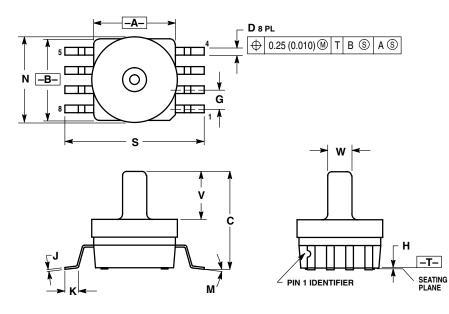
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).

- ALL VERTICAL SURFACES 5" TYPICAL DRAFT.
 DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.415	0.425	10.54	10.79	
В	0.415	0.425	10.54	10.79	
С	0.210	0.220	5.33	5.59	
D	0.026	0.034	0.66	0.864	
G	0.100	BSC	2.54 BSC		
J	0.009	0.011	0.23	0.28	
κ	0.100	0.120	2.54	3.05	
Μ	0°	15°	0°	15°	
Ν	0.405	0.415	10.29	10.54	
S	0.540	0.560	13.72	14.22	

CASE 482B-03 ISSUE B SMALL OUTLINE PACKAGE





NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006). 5. ALL VERTICAL SUBFACES 5° TYPICAL DRAFT

5.	ALL VERTICAL SURFACES 5° TYPICAL DRAFT									
		INCHES MILLIMETERS								
	DIM	MIN	MAX	MIN	MAX					
	Α	0.415	0.425	10.54	10.79					
	В	0.415	0.425	10.54	10.79					

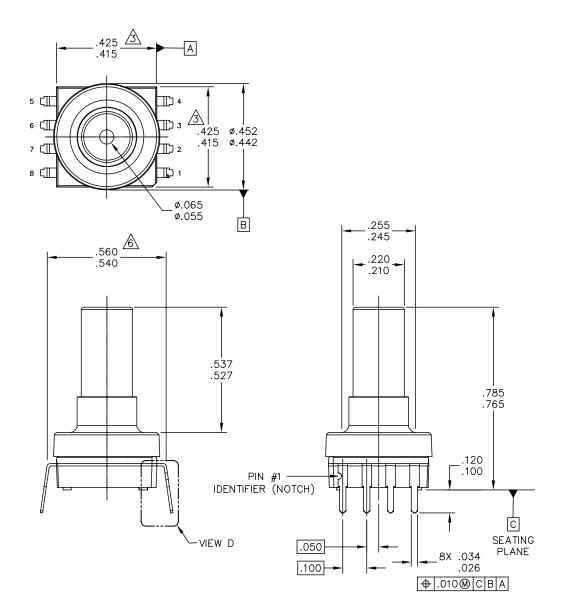
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100	BSC	2.54	BSC
н	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
К	0.061	0.071	1.55	1.80
Μ	0 °	7 °	0 °	7 °
Ν	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A-01 **ISSUE A** SMALL OUTLINE PACKAGE

MPXV4006



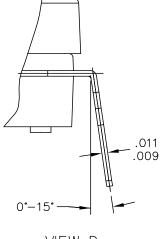




© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		L OUTLINE	PRINT VERSION NO	T TO SCALE
TITLE:		DOCUMENT NO): 98ASA10611D	REV: C
SO, 8 1/0, .420 X .4	CASE NUMBER	2: 1560–02	26 MAY 2005	
.100 IN PITCH	STANDARD: NO	N-JEDEC		

CASE 1560-02 ISSUE C SMALL OUTLINE PACKAGE





VIEW D

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICA	LOUTLINE	PRINT VERSION NC	T TO SCALE
TITLE:		DOCUMENT NO): 98ASA10611D	REV: C
SO, 8 1/0, .420 X .4	CASE NUMBER	2: 1560–02	26 MAY 2005	
.100 IN PITCH		STANDARD: NO	N-JEDEC	

CASE 1560-02 ISSUE C SMALL OUTLINE PACKAGE



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- 2. CONTROLLING DIMENSION: INCH.

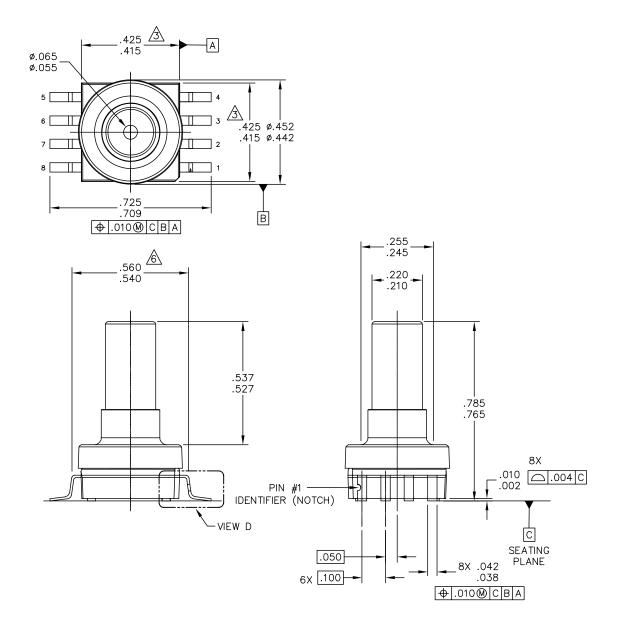
A DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.

- 4. MAXIMUM MOLD PROTRUSION IS .006.
- 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.
- 6 DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

© FREESCALE SEMICONDUCTOR, INC. All RIGHTS RESERVED.		L OUTLINE	PRINT VERSION NO	T TO SCALE
TITLE:	DOCUMENT NO): 98ASA10611D	REV: C	
SO, 8 1/0, .420 X .4	CASE NUMBER	: 1560–02	26 MAY 2005	
.100 IN PITCH	STANDARD: NO	N-JEDEC		

CASE 1560-02 ISSUE C SMALL OUTLINE PACKAGE



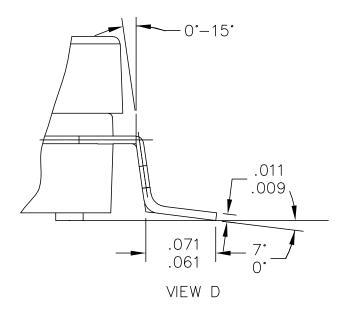


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		LOUTLINE	PRINT VERSION NO	T TO SCALE
TITLE:		DOCUMENT NO): 98ASA10686D	REV: A
SO, 8 1/0, .420 X .4	CASE NUMBER	: 1735–01	16 AUG 2005	
.100 IN PITCH	STANDARD: NO	N-JEDEC		

CASE 1735-01 ISSUE A SMALL OUTLINE PACKAGE







© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		LOUTLINE	PRINT VERSION NO	T TO SCALE
TITLE:		DOCUMENT NO): 98ASA10686D	REV: A
SO, 8 1/0, .420 X .4	CASE NUMBER	: 1735–01	18 AUG 2005	
.100 IN PITCI	STANDARD: NO	N-JEDEC		

CASE 1735-01 ISSUE A SMALL OUTLINE PACKAGE



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- 2. CONTROLLING DIMENSION: INCH.

A DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.

- 4. MAXIMUM MOLD PROTRUSION IS .006.
- 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.
- 6 DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

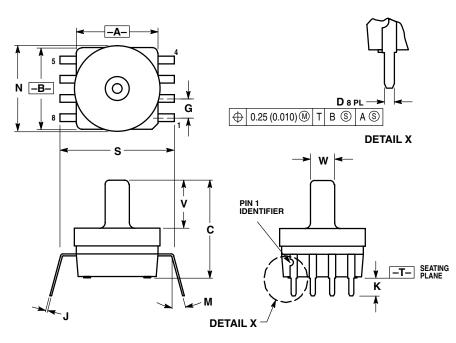
© FREESCALE SEMICONDUCTOR, INC. All RIGHTS RESERVED.		LOUTLINE	PRINT VERSION NO	T TO SCALE
TITLE:		DOCUMENT NO): 98ASA10686D	REV: A
SO, 8 1/0, .420 X .4	CASE NUMBER	8: 1735–01	18 AUG 2005	
.100 IN PITCH		STANDARD: NO	DN-JEDEC	

CASE 1735-01 ISSUE A SMALL OUTLINE PACKAGE

MPXV4006

Sensors Freescale Semiconductor





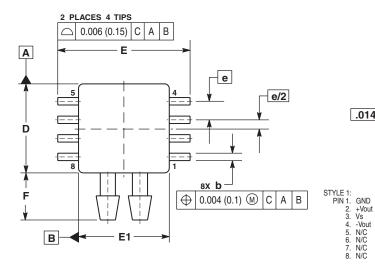
NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006). 5. ALL VENTICAL SURFACES 5° TYPICAL DRAFT. 6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

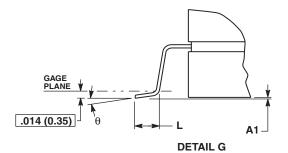
Pressure

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.026	0.034	0.66	0.864
G	0.100	BSC	2.54	BSC
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
М	0 °	15 °	0 °	15 °
Ν	0.444	0.448	11.28	11.38
S	0.540	0.560	13.72	14.22
٧	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482C-03 **ISSUE A** SMALL OUTLINE PACKAGE





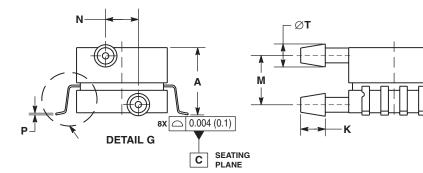


NOTES:

STYLE 2: PIN 1. N/C 2. Vs 3. GND 4. Vout 5. N/C 6. N/C 7. N/C 8. N/C

TES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 (0.152) PER SIDE

PROTRUSIONS SHALL NOT EXCEED 0.006 (0.152) PER SIDE. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.008 (0.203) MAXIMUM.

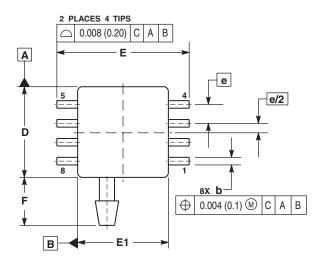


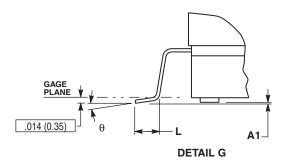
	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.370	0.390	9.39	9.91
A1	0.002	0.010	0.05	0.25
b	0.038	0.042	0.96	1.07
D	0.465	0.485	11.81	12.32
Е	0.680	0.700	17.27	17.78
E1	0.465	0.485	11.81	12.32
е	0.100	BSC	2.54 BSC	
F	0.240	0.260	6.10	6.60
Κ	0.115	0.135	2.92	3.43
L	0.040	0.060	1.02	1.52
Μ	0.270	0.290	6.86	7.37
Ν	0.160	0.180	4.06	4.57
Р	0.009	0.011	0.23	0.28
Т	0.110	0.130	2.79	3.30
θ	0°	7°	0°	7°

CASE 1351-01 **ISSUE O** SMALL OUTLINE PACKAGE

MPXV4006

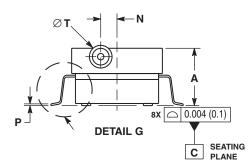


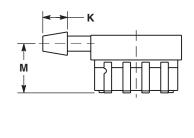




- NOTES: 1. CONTROLLING DIMENSION: INCH. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994. 3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 (0.152) PER SIDE.
 - DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
 - PROTRUSION SHALL BE 0.008 (0.203) MAXIMUM.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.300	0.330	7.11	7.62	
A1	0.002	0.010	0.05	0.25	
b	0.038	0.042	0.96	1.07	
D	0.465	0.485	11.81	12.32	
Е	0.717	BSC	18.21 BSC		
E1	0.465	0.485	11.81	12.32	
е	0.100	BSC	2.54	4 BSC	
F	0.245	0.255	6.22	6.47	
Κ	0.120	0.130	3.05	3.30	
L	0.061	0.071	1.55	1.80	
М	0.270	0.290	6.86	7.36	
Ν	0.080	0.090	2.03	2.28	
Р	0.009	0.011	0.23	0.28	
Т	0.115	0.125	2.92	3.17	
θ	0°	7°	0°	7°	





CASE 1369-01 **ISSUE O** SMALL OUTLINE PACKAGE



How to Reach Us:

Home Page: www.freescale.com

Web Support: http://www.freescale.com/support

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc. Technical Information Center, EL516 2100 East Elliot Road Tempe, Arizona 85284 1-800-521-6274 or +1-480-768-2130 www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd. Exchange Building 23F No. 118 Jianguo Road Chaoyang District Beijing 100022 China +86 010 5879 8000 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 1-800-441-2447 or +1-303-675-2140 Fax: +1-303-675-2150 LDCForFreescaleSemiconductor@hibbertgroup.com Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale[™] and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2009. All rights reserved.



MPXV4006 Rev. 3 1/2009