RF Power Field Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
  - Output Power — 8 Watts
  - Power Gain — 13 dB
  - Efficiency — 60%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive

Features
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 inch Reel.

### Table 1. Maximum Ratings

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage</td>
<td>V_{DSS}</td>
<td>-0.5, +40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Gate-Source Voltage</td>
<td>V_{GS}</td>
<td>±20</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain Current — Continuous</td>
<td>I_D</td>
<td>4</td>
<td>Adc</td>
</tr>
<tr>
<td>Total Device Dissipation @ T_C = 25°C (1)</td>
<td>P_D</td>
<td>62.5, 0.50</td>
<td>W, W/°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_{SLG}</td>
<td>- 65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>T_J</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Table 2. Thermal Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value (2)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>R_{JUC}</td>
<td>2</td>
<td>°C/W</td>
</tr>
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</table>

### Table 3. Moisture Sensitivity Level

<table>
<thead>
<tr>
<th>Test Methodology</th>
<th>Rating</th>
<th>Package Peak Temperature</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Per JESD22-A113, IPC/JEDEC J-STD-020</td>
<td>3</td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

1. Calculated based on the formula P_D = \( \frac{T_J - T_C}{R_{JUC}} \)

**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.
<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Off Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current (V&lt;sub&gt;DS&lt;/sub&gt; = 40 Vdc, V&lt;sub&gt;GS&lt;/sub&gt; = 0 Vdc)</td>
<td>I&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>μAdc</td>
</tr>
<tr>
<td>Gate-Source Leakage Current (V&lt;sub&gt;GS&lt;/sub&gt; = 10 Vdc, V&lt;sub&gt;DS&lt;/sub&gt; = 0 Vdc)</td>
<td>I&lt;sub&gt;GSS&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>μAdc</td>
</tr>
<tr>
<td><strong>On Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage (V&lt;sub&gt;DS&lt;/sub&gt; = 12.5 Vdc, I&lt;sub&gt;D&lt;/sub&gt; = 100 μA)</td>
<td>V&lt;sub&gt;GS(th)&lt;/sub&gt;</td>
<td>1</td>
<td>1.6</td>
<td>2.1</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain-Source On-Voltage (V&lt;sub&gt;GS&lt;/sub&gt; = 10 Vdc, I&lt;sub&gt;D&lt;/sub&gt; = 1 Adc)</td>
<td>V&lt;sub&gt;DS(on)&lt;/sub&gt;</td>
<td>—</td>
<td>0.4</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td><strong>Dynamic Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance (V&lt;sub&gt;DS&lt;/sub&gt; = 12.5 Vdc, V&lt;sub&gt;GS&lt;/sub&gt; = 0, f = 1 MHz)</td>
<td>C&lt;sub&gt;iss&lt;/sub&gt;</td>
<td>—</td>
<td>66</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance (V&lt;sub&gt;DS&lt;/sub&gt; = 12.5 Vdc, V&lt;sub&gt;GS&lt;/sub&gt; = 0, f = 1 MHz)</td>
<td>C&lt;sub&gt;oss&lt;/sub&gt;</td>
<td>—</td>
<td>33</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance (V&lt;sub&gt;DS&lt;/sub&gt; = 12.5 Vdc, V&lt;sub&gt;GS&lt;/sub&gt; = 0, f = 1 MHz)</td>
<td>C&lt;sub&gt;rss&lt;/sub&gt;</td>
<td>—</td>
<td>4.5</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td><strong>Functional Tests</strong> (In Freescale Test Fixture)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Source Amplifier Power Gain (V&lt;sub&gt;DD&lt;/sub&gt; = 12.5 Vdc, P&lt;sub&gt;out&lt;/sub&gt; = 8 Watts, I&lt;sub&gt;DQ&lt;/sub&gt; = 150 mA, f = 520 MHz)</td>
<td>G&lt;sub&gt;ps&lt;/sub&gt;</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Drain Efficiency (V&lt;sub&gt;DD&lt;/sub&gt; = 12.5 Vdc, P&lt;sub&gt;out&lt;/sub&gt; = 8 Watts, I&lt;sub&gt;DQ&lt;/sub&gt; = 150 mA, f = 520 MHz)</td>
<td>η</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>%</td>
</tr>
</tbody>
</table>
B1, B2  Short Ferrite Beads, Fair Rite Products (2743021446)
C1, C12 240 pF, 100 mil Chip Capacitors
C2, C3, C10, C11 0 to 20 pF Trimmer Capacitors
C4 82 pF, 100 mil Chip Capacitor
C5, C16 120 pF, 100 mil Chip Capacitors
C6, C13 10 μF, 50 V Electrolytic Capacitors
C7, C14 1,200 pF, 100 mil Chip Capacitors
C8, C15 0.1 μF, 100 mil Chip Capacitors
C9 30 pF, 100 mil Chip Capacitor
L1 55.5 nH, 5 Turn, Coilcraft
N1, N2 Type N Flange Mounts
R1 15 Ω Chip Resistor (0805)
R2 51 Ω, 1/2 W Resistor
R3 10 Ω Chip Resistor (0805)

Figure 1. 450 - 520 MHz Broadband Test Circuit

**TYPICAL CHARACTERISTICS, 450 - 520 MHz**

![Graph showing typical characteristics](image)

**Figure 2. Output Power versus Input Power**

**Figure 3. Input Return Loss versus Output Power**
TYPICAL CHARACTERISTICS, 450 - 520 MHz

![Gain versus Output Power](image)

*Figure 4. Gain versus Output Power*

![Drain Efficiency versus Output Power](image)

*Figure 5. Drain Efficiency versus Output Power*

![Output Power versus Biasing Current](image)

*Figure 6. Output Power versus Biasing Current*

![Drain Efficiency versus Biasing Current](image)

*Figure 7. Drain Efficiency versus Biasing Current*

![Output Power versus Supply Voltage](image)

*Figure 8. Output Power versus Supply Voltage*

![Drain Efficiency versus Supply Voltage](image)

*Figure 9. Drain Efficiency versus Supply Voltage*
**TYPICAL CHARACTERISTICS, 820 - 850 MHz**

![TYPICAL CHARACTERISTICS, 820 - 850 MHz](image)

**Figure 10. 820 - 850 MHz Broadband Test Circuit**

**Figure 11. Output Power versus Input Power**

![Figure 11. Output Power versus Input Power](image)

**Figure 12. Input Return Loss versus Output Power**

![Figure 12. Input Return Loss versus Output Power](image)
TYPICAL CHARACTERISTICS, 820 - 850 MHz

Figure 13. Gain versus Output Power

Figure 14. Drain Efficiency versus Output Power

Figure 15. Output Power versus Biasing Current

Figure 16. Drain Efficiency versus Biasing Current

Figure 17. Output Power versus Supply Voltage

Figure 18. Drain Efficiency versus Supply Voltage

MRF1518NT1
Figure 19. 400 - 470 MHz Broadband Test Circuit

B1, B2  Short Ferrite Beads, Fair Rite Products (2743021446)
C1, C14 240 pF, 100 mil Chip Capacitors
C2, C3, C4, C11, C12, C13 0 to 20 pF Trimmer Capacitors
C5 30 pF, 100 mil Chip Capacitor
C6 47 pF, 100 mil Chip Capacitor
C7, C18 120 pF, 100 mil Chip Capacitors
C8, C15 10 μF, 50 V Electrolytic Capacitors
C9, C16 1.200 pF, 100 mil Chip Capacitors
C10, C17 0.1 μF, 100 mil Chip Capacitors
L1 55.5 nH, 5 Turn, Coilcraft
N1, N2 Type N Flange Mounts
R1 15 Ω Chip Resistor (0805)
R2 51 Ω, 1/2 W Resistor

R3 10 Ω Chip Resistor (0805)
R4 33 kΩ, 1/8 W Resistor
Z1 0.476" x 0.080" Microstrip
Z2 0.724" x 0.080" Microstrip
Z3 0.348" x 0.080" Microstrip
Z4 0.048" x 0.080" Microstrip
Z5 0.175" x 0.080" Microstrip
Z6, Z7 0.260" x 0.223" Microstrip
Z8 0.239" x 0.080" Microstrip
Z9 0.286" x 0.080" Microstrip
Z10 0.806" x 0.080" Microstrip
Z11 0.553" x 0.080" Microstrip
Z12 Board Glass Teflon®, 31 mils, 2 oz. Copper

Figure 20. Output Power versus Input Power

Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 - 470 MHz
TYPICAL CHARACTERISTICS, 400 - 470 MHz

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**Figure 22.** Gain versus Output Power

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**Figure 23.** Drain Efficiency versus Output Power

---

**Figure 24.** Output Power versus Biasing Current

---

**Figure 25.** Drain Efficiency versus Biasing Current

---

**Figure 26.** Output Power versus Supply Voltage

---

**Figure 27.** Drain Efficiency versus Supply Voltage
Figure 28. 135 - 175 MHz Broadband Test Circuit

B1, B2  Short Ferrite Beads, Fair Rite Products  (2743021446)
C1, C13 330 pF, 100 mil Chip Capacitors
C2, C4, C11 0 to 20 pF Trimmer Capacitors
C3 12 pF, 100 mil Chip Capacitor
C5 43 pF, 100 mil Chip Capacitor
C6, C17 75 pF, 100 mil Chip Capacitors
C7, C14 10 μF, 50 V Electrolytic Capacitors
C8, C15 1,200 pF, 100 mil Chip Capacitors
C9, C16 0.1 μF, 100 mil Chip Capacitors
C10 75 pF, 100 mil Chip Capacitor
C12 13 pF, 100 mil Chip Capacitor
L1 26 nH, 4 Turn, Coilcraft
L2 5 nH, 2 Turn, Coilcraft
L3 33 nH, 5 Turn, Coilcraft
L4 55.5 nH, 5 Turn, Coilcraft
N1, N2 Type N Flange Mounts
R1 15 Ω Chip Resistor (0805)
R2 56 Ω, 1/4 W Carbon Resistor
R3 100 Ω Chip Resistor (0805)
R4 33 kΩ, 1/8 W Carbon Resistor
Z1 0.115" x 0.080" Microstrip
Z2 0.255" x 0.080" Microstrip
Z3 0.125" x 0.080" Microstrip
Z4 0.192" x 0.080" Microstrip
Z5 0.260" x 0.223" Microstrip
Z6 0.305" x 0.080" Microstrip
Z7 0.155" x 0.080" Microstrip
Z8 0.962" x 0.080" Microstrip
Z9 0.305" x 0.080" Microstrip
Z10 0.305" x 0.080" Microstrip
Board Glass Teflon®, 31 mils, 2 oz. Copper

Figure 29. Output Power versus Input Power

Figure 30. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 - 175 MHz

VDD = 12.5 Vdc
TYPICAL CHARACTERISTICS, 135 - 175 MHz

Figure 31. Gain versus Output Power

Figure 32. Drain Efficiency versus Output Power

Figure 33. Output Power versus Biasing Current

Figure 34. Drain Efficiency versus Biasing Current

Figure 35. Output Power versus Supply Voltage

Figure 36. Drain Efficiency versus Supply Voltage
TYPICAL CHARACTERISTICS

This graph displays the calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_d^2 for MTTF in a particular application.

Figure 37. MTTF Factor versus Junction Temperature
Note: $Z_{OL}^*$ was chosen based on tradeoffs between gain, drain efficiency, and device stability.

**Table 1:** Complex conjugate of source impedance with parallel 15 Ω resistor and 82 pF capacitor in series with gate. (See Figure 1).

<table>
<thead>
<tr>
<th>$f$ (MHz)</th>
<th>Z(_{in}) (Ω)</th>
<th>Z(_{OL}^*) (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>450</td>
<td>4.9 +j2.85</td>
<td>6.42 +j3.23</td>
</tr>
<tr>
<td>470</td>
<td>4.85 +j3.71</td>
<td>4.59 +j3.61</td>
</tr>
<tr>
<td>500</td>
<td>4.63 +j3.84</td>
<td>4.72 +j3.12</td>
</tr>
<tr>
<td>520</td>
<td>3.52 +j3.92</td>
<td>3.81 +j3.27</td>
</tr>
</tbody>
</table>

$Z_{in}$ = Complex conjugate of source impedance.

$Z_{OL}^*$ = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50\%$.

**Figure 38. Series Equivalent Input and Output Impedance**
Zin = Complex conjugate of source impedance with parallel 15 Ω resistor and 47 pF capacitor in series with gate. (See Figure 19).

ZOL* = Complex conjugate of load impedance at given output power, voltage, frequency, and ηD > 50%.

Note: ZOL* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>Zin (Ω)</th>
<th>ZOL* (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>4.28 +j2.36</td>
<td>4.41 +j0.67</td>
</tr>
<tr>
<td>440</td>
<td>6.45 +j5.13</td>
<td>4.14 +j2.53</td>
</tr>
<tr>
<td>470</td>
<td>5.91 +j3.34</td>
<td>3.92 +j4.02</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>Zin (Ω)</th>
<th>ZOL* (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>135</td>
<td>18.31 -j0.76</td>
<td>8.97 +j2.62</td>
</tr>
<tr>
<td>155</td>
<td>17.72 +j1.85</td>
<td>9.69 +j2.81</td>
</tr>
<tr>
<td>175</td>
<td>18.06 +j5.23</td>
<td>7.94 +j1.14</td>
</tr>
</tbody>
</table>

Figure 38. Series Equivalent Input and Output Impedance (continued)
<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>S_{11}</th>
<th>S_{12}</th>
<th>S_{21}</th>
<th>S_{22}</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.88</td>
<td>-148</td>
<td>18.91</td>
<td>99</td>
</tr>
<tr>
<td>100</td>
<td>0.85</td>
<td>-163</td>
<td>9.40</td>
<td>86</td>
</tr>
<tr>
<td>200</td>
<td>0.85</td>
<td>-170</td>
<td>4.47</td>
<td>73</td>
</tr>
<tr>
<td>300</td>
<td>0.87</td>
<td>-171</td>
<td>2.72</td>
<td>64</td>
</tr>
<tr>
<td>400</td>
<td>0.88</td>
<td>-172</td>
<td>1.85</td>
<td>56</td>
</tr>
<tr>
<td>500</td>
<td>0.90</td>
<td>-173</td>
<td>1.35</td>
<td>52</td>
</tr>
<tr>
<td>600</td>
<td>0.92</td>
<td>-173</td>
<td>1.04</td>
<td>47</td>
</tr>
<tr>
<td>700</td>
<td>0.93</td>
<td>-174</td>
<td>0.83</td>
<td>44</td>
</tr>
<tr>
<td>800</td>
<td>0.94</td>
<td>-175</td>
<td>0.68</td>
<td>39</td>
</tr>
<tr>
<td>900</td>
<td>0.94</td>
<td>-175</td>
<td>0.55</td>
<td>36</td>
</tr>
<tr>
<td>1000</td>
<td>0.96</td>
<td>-176</td>
<td>0.46</td>
<td>30</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>S_{11}</th>
<th>S_{12}</th>
<th>S_{21}</th>
<th>S_{22}</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.90</td>
<td>-159</td>
<td>20.80</td>
<td>97</td>
</tr>
<tr>
<td>100</td>
<td>0.88</td>
<td>-169</td>
<td>10.35</td>
<td>88</td>
</tr>
<tr>
<td>200</td>
<td>0.88</td>
<td>-174</td>
<td>5.09</td>
<td>79</td>
</tr>
<tr>
<td>300</td>
<td>0.89</td>
<td>-175</td>
<td>3.23</td>
<td>73</td>
</tr>
<tr>
<td>400</td>
<td>0.89</td>
<td>-175</td>
<td>2.30</td>
<td>67</td>
</tr>
<tr>
<td>500</td>
<td>0.90</td>
<td>-176</td>
<td>1.74</td>
<td>63</td>
</tr>
<tr>
<td>600</td>
<td>0.91</td>
<td>-176</td>
<td>1.39</td>
<td>59</td>
</tr>
<tr>
<td>700</td>
<td>0.92</td>
<td>-176</td>
<td>1.16</td>
<td>55</td>
</tr>
<tr>
<td>800</td>
<td>0.93</td>
<td>-176</td>
<td>0.96</td>
<td>50</td>
</tr>
<tr>
<td>900</td>
<td>0.94</td>
<td>-177</td>
<td>0.80</td>
<td>46</td>
</tr>
<tr>
<td>1000</td>
<td>0.94</td>
<td>-177</td>
<td>0.67</td>
<td>41</td>
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</table>

<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>S_{11}</th>
<th>S_{12}</th>
<th>S_{21}</th>
<th>S_{22}</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.91</td>
<td>-159</td>
<td>20.18</td>
<td>97</td>
</tr>
<tr>
<td>100</td>
<td>0.89</td>
<td>-169</td>
<td>10.05</td>
<td>89</td>
</tr>
<tr>
<td>200</td>
<td>0.88</td>
<td>-174</td>
<td>4.93</td>
<td>80</td>
</tr>
<tr>
<td>300</td>
<td>0.89</td>
<td>-175</td>
<td>3.14</td>
<td>73</td>
</tr>
<tr>
<td>400</td>
<td>0.89</td>
<td>-176</td>
<td>2.24</td>
<td>67</td>
</tr>
<tr>
<td>500</td>
<td>0.90</td>
<td>-176</td>
<td>1.70</td>
<td>64</td>
</tr>
<tr>
<td>600</td>
<td>0.92</td>
<td>-176</td>
<td>1.36</td>
<td>59</td>
</tr>
<tr>
<td>700</td>
<td>0.92</td>
<td>-176</td>
<td>1.13</td>
<td>55</td>
</tr>
<tr>
<td>800</td>
<td>0.93</td>
<td>-177</td>
<td>0.94</td>
<td>50</td>
</tr>
<tr>
<td>900</td>
<td>0.94</td>
<td>-177</td>
<td>0.78</td>
<td>46</td>
</tr>
<tr>
<td>1000</td>
<td>0.94</td>
<td>-178</td>
<td>0.65</td>
<td>41</td>
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</table>
APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Freescale Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (Cgd), and gate-to-source (Cgs). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (Cds). These capacitances are characterized as input (Ciss), output (Coss) and reverse transfer (Crss) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The Ciss can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

$BV_{DSS}$ values for this device are higher than normally required for typical applications. Measurement of $BV_{DSS}$ is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high - on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated $V_{GS}$ can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current ($I_{DQ}$), whose value is application dependent. This device was characterized at $I_{DQ} = 150$ mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, $I_{DQ}$ may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.
MOUNTING
The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065" x 0.180" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Freescale Application Note AN4005/D, “Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package,” and Engineering Bulletin EB209/D, “Mounting Method for RF Power Leadless Surface Mount Transistor” for additional information.

AMPLIFIER DESIGN
Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Freescale Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors.” Large-signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device’s S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Freescale Application Note AN215A, “RF Small-Signal Design Using Two-Port Parameters” for a discussion of two port network theory and stability.
PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents to aid your design process.

**Application Notes**
- AN211A: Field Effect Transistors in Theory and Practice
- AN215A: RF Small-Signal Design Using Two-Port Parameters
- AN721: Impedance Matching Networks Applied to RF Power Transistors
- AN4005: Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package

**Engineering Bulletins**
- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**Software**
- Electromigration MTTF Calculator

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

**REVISION HISTORY**

The following table summarizes revisions to this document.

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
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| 10       | June 2008| • Changed Power Gain from 13.5 dB to 13 dB in Functional Tests table on p. 2 and corrected specified performance values for power gain and efficiency on p. 1 to match typical performance values in the functional test. Past two years of production data shows Power Gain typical value at 13 dB.  
• Added Product Documentation and Revision History, p. 18 |
| 11       | June 2009| • Modified data sheet to reflect MSL rating change from 1 to 3 as a result of the standardization of packing process as described in Product and Process Change Notification number, PCN13516, p. 1  
• Added Electromigration MTTF Calculator availability to Product Documentation, Tools and Software, p. 18 |