NAFE33350

Software Configurable Universal Low-Power AO-AFE

Rev. 1.0 — 14 January 2026 **Product data sheet**

Document information

Information	Content
Keywords	NAFE33350, industrial, software-configurable, low-power, Universal Analog Output (UAO), Analog Front End (AFE), 18-bit DAC
Abstract	The NAFE33350 is a software-configurable universal output AFE that meets high-precision control requirements of industrial applications, such as programmable logic controllers (PLC), distributed control systems (DCS), industrial HMI, factory automation, and building automation.

1 General description

The NAFE33350 is a software-configurable universal analog output (AO) analog front-end (AFE) that meets high-precision control requirements of industrial-grade applications. The AO-AFE integrates the following components.

- A precision 18-bit digital-to-analog converter (DAC)
- A low-drift voltage reference
- Low-offset drift buffers
- A 70 V input-protection circuit for EMC and miswiring scenarios

For open circuit and short-circuit detection, the output stage includes built-in diagnostic and protection circuitry.

The AO AFE is suitable for programmable logic controllers (PLC), analog output modules, isolated industrial control systems, and process control.

2 Features and benefits

- High-precision pin-to-pin and firmware compatible AO-AFE family
- Software configurable voltage and current analog output with multiple ranges
- Integrated voltage references
- Factory calibrated voltage and current output
- Precise and fast response AO-AFE architecture provides
  - 18-bit DAC
  - DAC 0 ksps to 100 ksps data rate
  - ±12.5 V, ±25 mA
  - ±0.01 % accuracy at room
  - ±0.08 % accuracy over temperature (Voltage mode after room calibration)
  - INL and 2 LSB max @ 18-bit
- Robust and flexible
  - ±36 V protected I/O (external transient voltage suppressor (TVS), required)
  - ±7 V to ±28 V wide supply range, HVDD-HVSS = 14 V to 48 V
- -40 °C to 125 °C temperature range
- 6 mm x 6 mm small HVQFN-40 package

2.1 IEC EMC ratings

- IEC61004-2 ESD
- IEC61004-4 Electrical Fast Transient/Burst Test (EFT)
- IEC61004-5 2 kV Surge Immunity Test

2.2 ESD stress rating and latch-up

Section 2.2 describes the ESD stress rating and latch-up for NAFE33350.

Table 1. ESD stress rating and latch-up

Description	Max	Units
Human body model (HBM) on all pins	±4500	V
Charged device model (CDM) on all pins	±750	V
Latch-up at 150 ºC	±200	mA

Note: *Section 2.2 describes only the stress ratings. Functional operation of the product at conditions at or above its ratings is not implied.*

3 Applications

- Precise voltage and current source systems
- PLC, DCS I/O modules
- Industrial automation and process control

4 Ordering information

The NAFE33350 is part of a software-compatible family of products that can be used to design a flexible and scalable analog output module.

Table 2. Part family

NAFE33350 DS[1]					
NAFE	3	3	3	5	0
NXP analog front-end	Power 3 = Low power 9 = High speed	3	Reference 3 = Factory calibrated 1 = Non-factory calibrated	Resolution (DAC) 5 = 18 4 = 16 3 = 14	Channels 0: 1 AO

[1] Contact your NXP sales representative for further information and available part numbers.part variants with different resolution, number of I/Os, and calibration.

Table 3. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NAFE33350 B40BS	FE33350	HVQFN40	Plastic thermal enhanced thin quad flat package; no leads; 40 terminals; body 6 mm x 6 mm x 0.85 mm	SOT618-20(D)

Table 4. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NAFE33350 B40BS	NAFE33350 B40BSMP	HVQFN40	Reel 13" Q2 DP	4000	T_{amb} = -40 °C to 125 °C
	NAFE33350B40BSZ		Reel 7" Q1 DP	1000	

5 Block diagram

Figure 1 shows the labeled block diagram of NAFE33350.

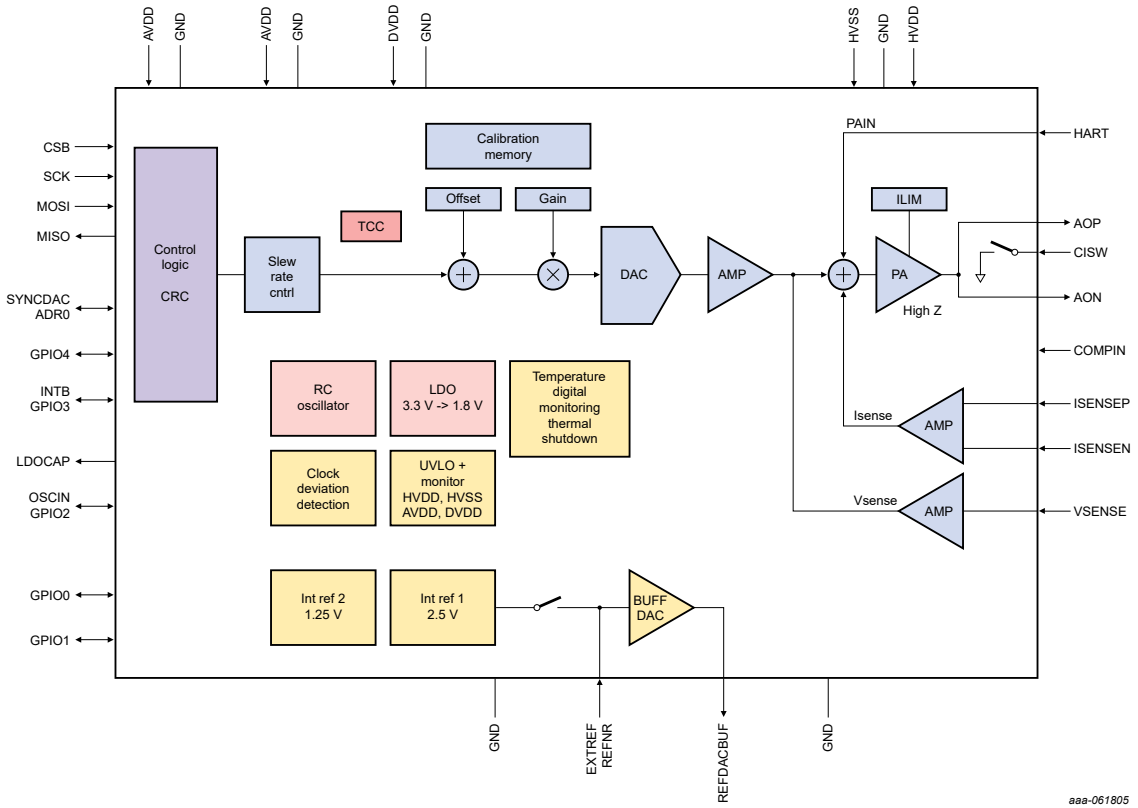


Figure 1. Block diagram

6 Pinning information

This chapter explains the configuration and assignment of pins on NAFE33350.

6.1 Pinning

Figure 2 shows the pinning for NAFE33350.

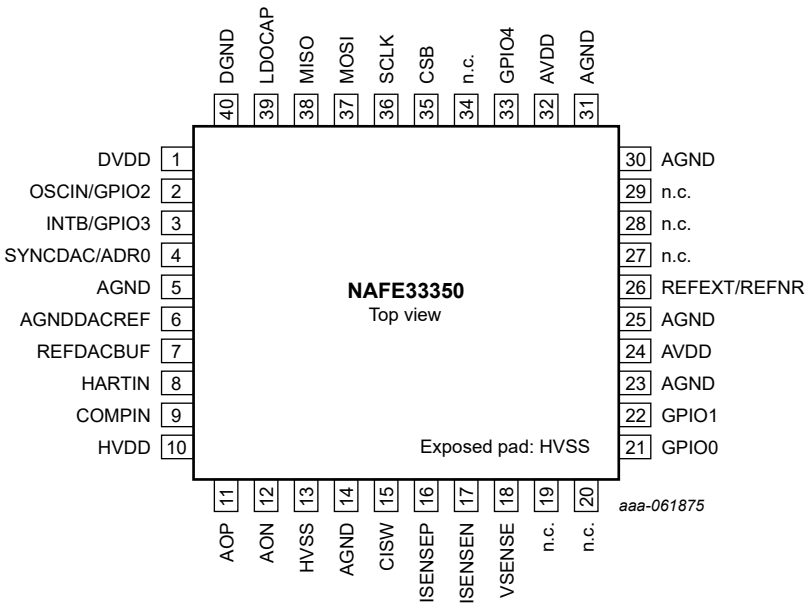


Figure 2. Top-down view, 40 pins package: 6 mm x 6 mm (HVQFN)

6.2 Pin description

Table 5 provides detailed description of various pins on NAFE33350.

Table 5. Pin number and pin description

Number	Name	I/O	Functional description
1	DVDD		3.3 V digital power supply.
2	OSCIN/GPIO2	DI	External clock input and GPIO2 multifunction pin. The default is an external clock input pin. If the external clock function is not used, it f can be left floating. When it is configured as GPIO functionality, it functions as a GPIO. Also refer to auto clock source selection for further details.
3	INTB/GPIO3	DO	Interrupt flag output (active-low) and GPIO3 multifunction pin. The default is INTB and it can be configured as GPIO3.
4	SYNCDAC/ADR0	DI	DAC synchronized input and ADR0 multifunction pin. The default is SYNCDAC and it can be configured as ADR0. It can be grounded if SYNCDAC is not used.
5	AGND		Analog ground.
6	AGNDDACREF	AI	DAC voltage reference GND sense.
7	REFDACBUF	AO	DAC voltage reference output bypass. Connect a 0.1 µF bypass capacitor close to the pin.
8	HARTIN	AI	HART signal input. A coupling capacitor is required.
9	COMPIN	AO	External compensation for the output driver amplifier. External passive compensation network can be connected between AO and COMP_IN pins.

Table 5. Pin number and pin description*...continued*

Number	Name	I/O	Functional description
10	HVDD		High-voltage positive supply.
11	AOP	AO	High-side analog output. This pin is connected to the anode of an off-chip Schottky diode. The cathode of the Schottky diode is connected to the AO onboard terminal through an off-chip current sensing resistor (50 Ω TYP).
12	AON	AO	Low-side analog output. This pin is connected to the cathode of an off-chip Schottky diode. The anode of the Schottky diode is connected to the AO onboard terminal through an off-chip current sensing resistor (50 Ω TYP).
13	HVSS		High-voltage negative supply.
14	AGND		Analog ground.
15	CISW	AI	Current input switch pin (CISW). This pin is connected to the AO onboard terminal through the current sensing resistor connected to the AOP and AON pins.
16	ISENSEP	AI	Positive input for an external current sense resistor. Must have an RC filter (5 kΩ and 100 pF).
17	ISENSEN	AI	Negative input for an external current sense resistor. Must have an RC filter (5 kΩ and 100 pF).
18	VSENSE	AI	Voltage sense input must have an RC filter (5 kΩ and 100 pF).
19	RES		Reserved. Connect to AGND.
20	RES		Reserved. Connect to AGND.
21	GPIO0	DI, DO	General-purpose digital I/O. Connect to AGND if not used.
22	GPIO1	DI, DO	General-purpose digital I/O. Connect to AGND if not used.
23	AGND		Analog ground.
24	AVDD		3.3 V analog power supply.
25	AGND		Analog ground.
26	REFEXT/REFNR	AI	External reference voltage input/internal reference output bypass.
27	Not Connected		
28	Not Connected		
29	Not Connected		
30	AGNDREF	AI	Voltage reference GND sense.
31	AGND		Analog ground.
32	AVDD		3.3 V analog power supply.
33	GPIO4	DI, DO	General-purpose digital I/O. Connect to AGND if not used.
34	RES	DO	Reserved. Leave floating.
35	CSB	DI	Chip select input, active-low.
36	SCLK	DI	SPI clock input.
37	COTI	DI	SPI data input.
38	CITO	DO	SPI data output.
39	LDOCAP		1.8 V regulator output bypass.
40	DGND		Digital ground.
	EP		Exposed pad (HVSS).

7 Functional description

The NAFE33350 is a universal AO software-configurable AFE for high-precision and high-accuracy measurements. Both the voltage output and the current output have the full range (or the overload range) of 1.25 times the linear range.

The maximum voltage overload is ±12.5 V and the correspondent max linear range is ±10 V.

The maximum current overload is ±25 mA and the correspondent max linear range is ±20 mA.

Linear voltage ranges:

- ±10 V; ±5 V.
- Load resistance > 1 kΩ.

In addition, the NAFE33350 fits the most common output current ranges and load resistance.

- ±20 mA; 0 mA to +20 mA; 4 mA-20 mA
- Load resistance from 0 Ω; 1 kΩ

The NAFE33350 includes a feedback path for the voltage and current output (Vsense, Isense).

7.1 Digital factory calibration

To save time and the cost of calibration, select the parts that are already digitally calibrated and do not require further and long calibration procedures. The NAFE33350 integrates a non-volatile memory (NVM). NVM allows digital calibration of the AFE in the factory and stores the coefficient values for offset and gain in the NVM memory.

7.2 Precise and fast analog output

The NAFE33350 integrates a high-precision DAC, low-drift voltage reference, and a precise high-voltage amplifier to generate small and wide output signals. In addition, the DAC and the amplifier have been designed to provide fast-output response with 10 µs settling time.

The total error of an end-to-end acquisition system is:

- ±0.01 % of full-scale range at 25 °C with factory calibration
- ±10 ppm of full scale/°C temperature coefficient (Voltage mode)
- ±0.05 % of full-scale range over I/O module temperature range from 0 °C to 60 °C

The NAFE33350 provides a wide range of programmable data rate. The fast data rate fits systems with fast response time requirements.

The host processor update rate determines the DAC output data rate.

The update rate is 0 ksps to 100 ksps.

To provide a fast response, the precise high-voltage (HV) amplifiers are designed with a wide GBW product and a fast slew rate for short settling time. The DAC is designed with a fast update rate and low propagation delay.

Figure 3 shows the main delay sources of the output settling time.

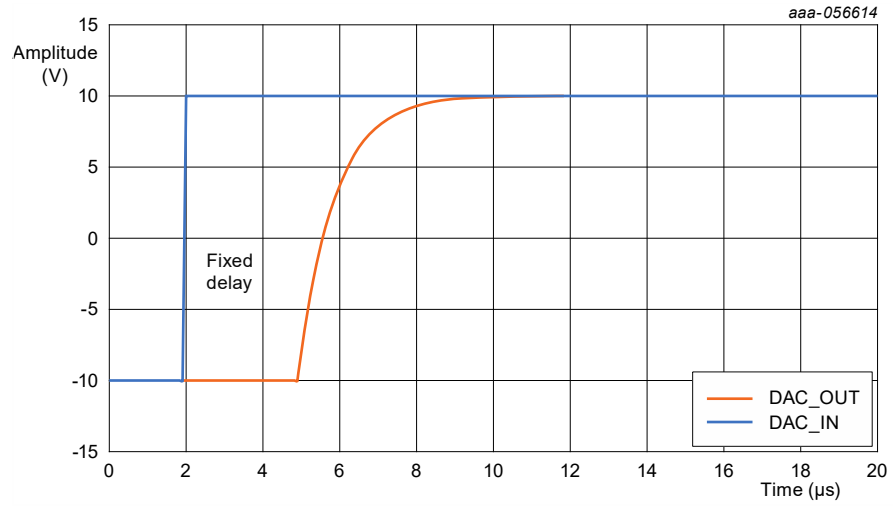


Figure 3. Main delay sources of output settling time

7.3 AO signal path

The analog output can be configured as Voltage-output mode and Current-output mode.

As shown in Figure 4, an on-chip precise DAC is used as output signal source followed by a gain stage and Power Amplifier, which can be configured for voltage output, current output, or high-impedance (Hi-Z state).

7.3.1 Power amplifier output

As shown in Figure 4, there are several switches in the output stage, which allow different modes of operation. For example, AO pin - high-Z, voltage output (VO), and current output (CO).

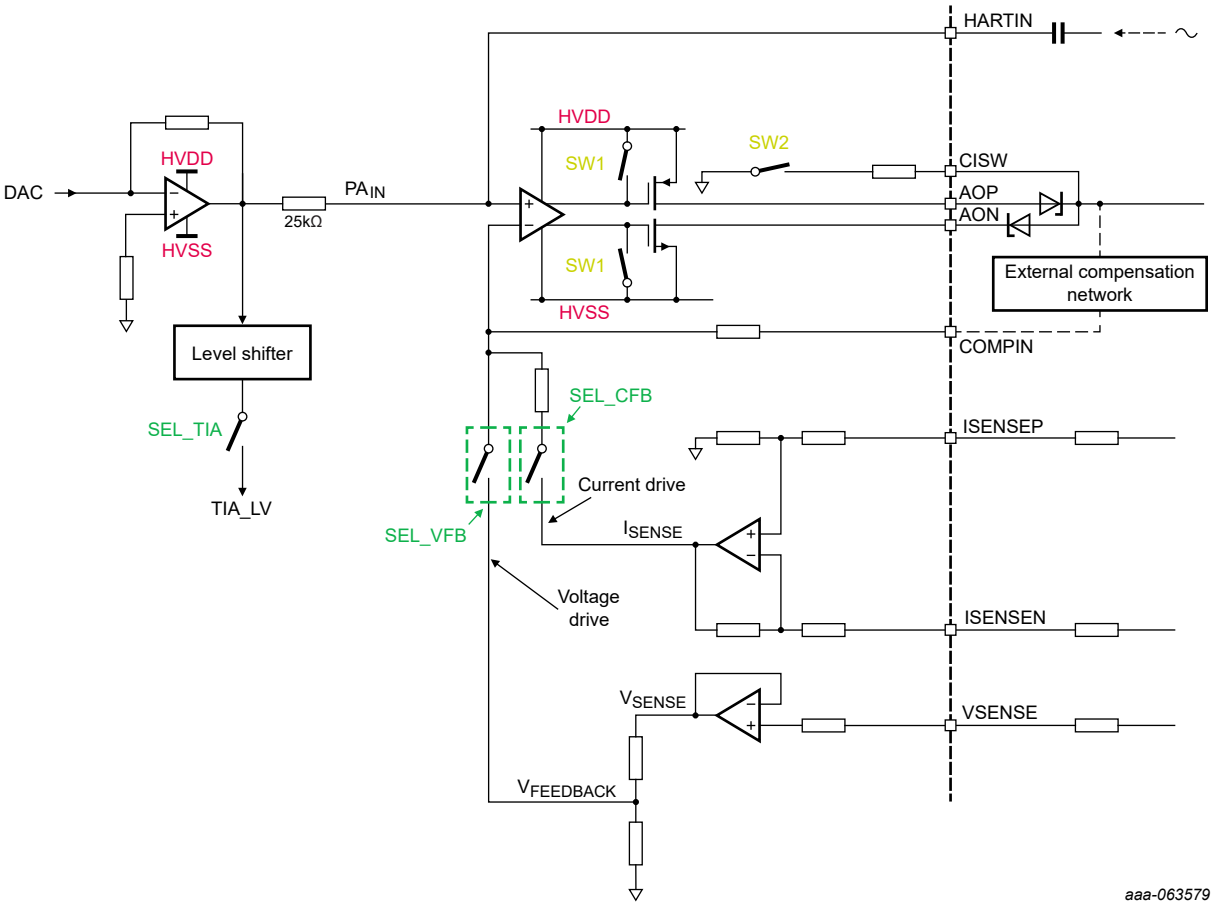


Figure 4. AO block diagram

Two switches are connected at the analog-output pin. The High-Z switch SW1 connects or disconnects the PA out to analog output pin while the ShortGND switch SW2 connect the output pin to GND.

To configure the device in Output mode, SW1 must be closed and SW2 open. The appropriate power amplifier (PA) feedback path (VFB or CFB) must be enabled using SEL_VFB or SEL_CFB respectively. PA input feedback path can be floated for high-Z mode at the AO.

Analog Output Mode (AO_MODE)

Pre-configured AO modes.

1. 00\b: high-Z mode, PA_ON = 0, VSA_ON = x, CSA_ON = x
2. 10\b: Voltage-output mode, PA_ON = 1, VSA_ON = 1, CSA_ON = x
3. 11\b: Current-output mode, PA_ON = 1, VSA_ON = x, CSA_ON = 1
4. VSA ON = 1 turn ON VSA.
5. Exception: AO_MODE = 10\b
6. Voltage-output mode force VSA ON = 1, this bit cannot be overwritten.
7. CSA ON = 1 turn ON CSA.
8. Exception: AO_mode = 11\b
9. Current-output mode force CSA ON = 1, this bit cannot be overwritten.
10. CISW_ON = 1 turn on the current input switch connected to the ground.
11. CISW is used with external Rsense for Current-input mode configuration.

Note: *To avoid short-circuit, CSIW_ON must be 0\h when the PA_ON = 1 if the CISW pin is connected to the AOP/AON path.*

7.3.2 Output modes

NAFE33350 supports both Voltage Output and Current Output modes with programmable FS ranges of 12.5 V and ±25 mA, respectively.

7.3.2.1 Voltage output

NAFE33350 voltage output can drive the maximum Rload of 10 MΩ and maximum Cload of 2 µF. The output settling time depends on the combined RC loading at the AO pin.

The voltage output settles to 0.1 % accuracy for 10 V output swing with no Rload as below:

- 50 µs with Rload = open and Cload = 20 nF
- 0.5 ms with Rload = open and Cload = 2 µF

The NAFE33350 settles to 0.1 % of 10 V swing within 10 µs for Cload in the range of 1 nF - 10 nF. If Cload > 20 nF, the system hits the current limit and overcurrent drives the device into high-Z protection mode. To avoid it, use the slew rate control to ramp up the DAC softly. Alternatively, use the current limiter to clamp the current to a specified level within the current limiter duration. The current limiter response time depends on the load capacitance. An external component can also be used to dampen the overvoltage and overcurrent condition at the device input pins. For overcurrent protection details, see Section 7.3.6.

7.3.2.2 Current output

NAFE33350 current output can drive the maximum Rload of 10 kΩ and maximum Lload of 1 mH.

The current output settles to 0.1 % accuracy for a 25 mA output swing with no Rload as below:

- 50 µs with Rload = open and Lload = 47 µH
- 0.5 ms with Rload = open and Lload = 1 mH

The user can achieve fast settling and limit the maximum current during the step response by keeping load inductance below 10 µH. If Lload > 10 µH, avoid overcurrent triggered High-Z protection mode by using the slew rate control to ramp up the DAC softly. Alternatively, place an RC filter at the HART input pin. For details, see Overcurrent protection in Current input mode. If required, an external component (such as a TVS diode) can be used to mitigate the current surge at the AO pin.

7.3.3 DAC output slew rate control

The slew rate control feature of the NAFE33350 controls the rate at which the output value changes. This feature is available on both the current and voltage outputs. You can program the slew rate control parameters in register AO_SLR_CTRL defined in Table 12. With the slew rate control feature disabled, the output value changes at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, enable the slew rate control feature. With the feature enabled via the SLREN bit of the slew rate control register (see Table 7), the output steps digitally instead of slewing directly between two values. The slew rate control register digitally defines the rate of these steps through two accessible parameters, as shown in Table 6 and Table 7.

You can program the slew rate control parameters in register AO_SLR_CTRL defined in Table 12. The parameters are SLR_CLOCK and SR_STEP. SR_CLOCK defines the rate at which the digital slew is updated. For example, if the selected update rate is 8 kHz, the output updates every 125 µs. The SLR_STEP defines by how much the output value changes at each update. Together, both parameters define the rate of change of the output value. Table 6 and Table 7 outline the range of values for both the SLR_CLOCK and SLR_STEP parameters.

Table 6. Slew rate update clock selection

SLR_CLOCK [2:0]	Update clock frequency in Hz
0 0 0	4000
0 0 1	6000
0 1 0	9000
0 1 1	12000
1 0 0	40000
1 0 1	60000
1 1 0	90000
1 1 1	150000

Table 7. Slew rate steps

DAC's resolution	SLR_STEP							
	0	1	2	3	4	5	6	7
Step_size: 18-bit	1024	2048	4096	8192	16384	32768	65536	131072
Step_size: 16-bit	256	512	1024	2048	4096	8192	16384	32768
Step_size: 14-bit	64	128	256	512	1024	2048	4096	8192
Step_size: 12-bit	16	32	64	128	256	512	1024	2048

When the slew rate control feature is enabled, SLREN = 1, all output changes occur at the programmed slew rate. For example, when you assert the RESET command, the output slews to the clear value at the programmed slew rate. It is assumed that the clear channel is enabled for clearing. The update clock frequency for any given value is the same for all output ranges. However, the step size varies across output ranges for a given value of step size because the LSB size is different for each output range.

The following equation describes the slew rate as a function of the step size, the update clock frequency, and the LSB size:

$$Slew\ time\ =\ Output\ change \Big/ \left(Step\ size{*}Update\ clock\ freq.{*}LSB\ size\right)$$

Where: Slew time is expressed in seconds.

Output change is expressed in amps for IOUT or volts for VOUT.

7.3.3.1 DAC conversion during digital slew active

When the DAC slew is active, new DAC codes sent from the SPI host is ignored. The host must wait for the completion of the current DAC conversion. Figure 5 shows that the DAC code sent from the SPI host during the DAC output slewing active.

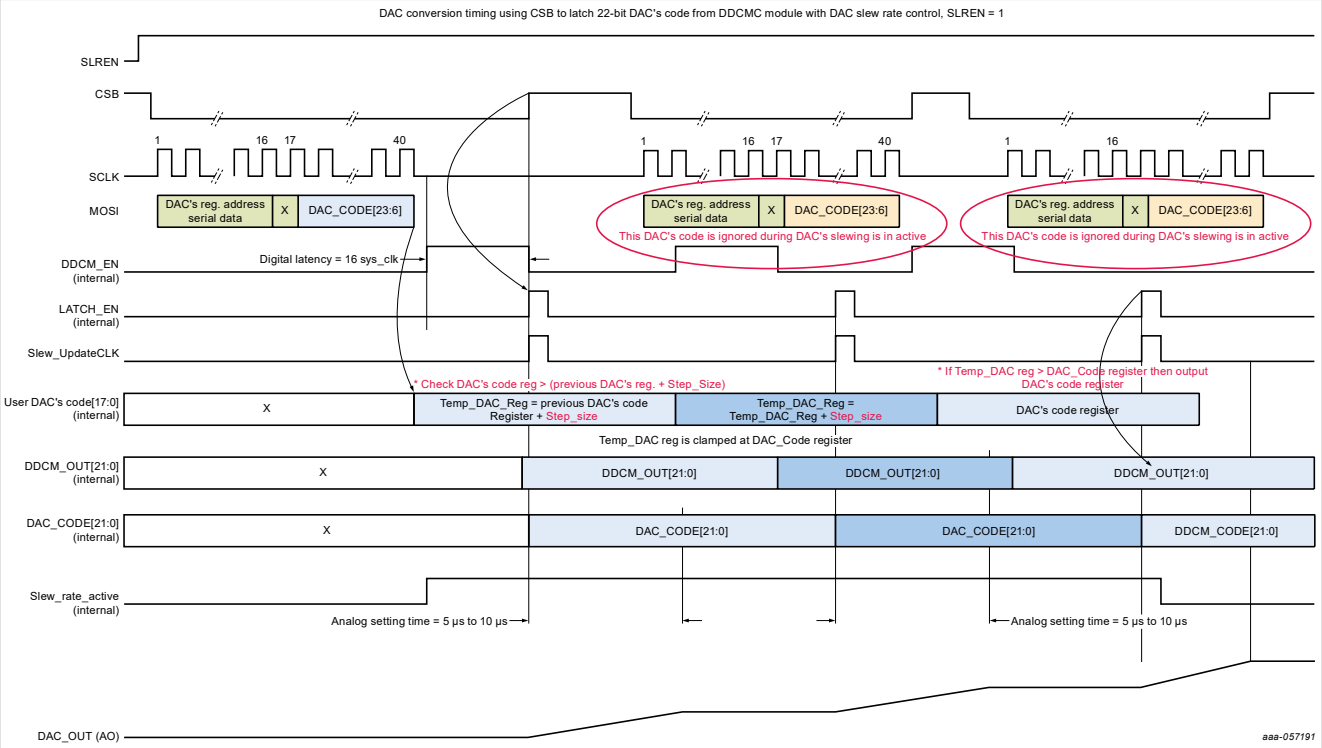


Figure 5. DAC output slewing timing

7.3.4 Auto-DAC waveform generator

The SPI host sending the DAC command CMD_WGEN can trigger the Auto-DAC waveform generator. Before issuing this command, all the waveform parameters in AWG_AMP_MAX[23:0], AWG_AMP_MIN[23:0], STEP_AMP[2:0], and STEP_FREQ[2:0] registers are programmed to get the desired output waveform. See Table 12 and Table 13 for the register address of these AWG parameters. CMD_WGEN_START continuously executes until CMD_WGEN_STOP is told to stop. When the waveform generator is enabled, AIO_CHOP is ignored. The chopping feature is not supported for auto-waveform generator.

Table 8. Step frequency selection

STEP_FREQ[2:0]	Update clock frequency in Hz
0 0 0	4000
0 0 1	6000
0 1 0	9000
0 1 1	12000
1 0 0	40000
1 0 1	60000
1 1 0	90000
1 1 1	150000

Table 9. Auto-DAC waveform generator step size

DAC' resolution	STEP_AMP[2:0]							
	0	1	2	3	4	5	6	7
Step_size: 18-bit	1024	2048	4096	8192	16384	32768	65536	131072
Step_size: 16-bit	256	512	1024	2048	4096	8192	16384	32768
Step_size: 14-bit	64	128	256	512	1024	2048	4096	8192

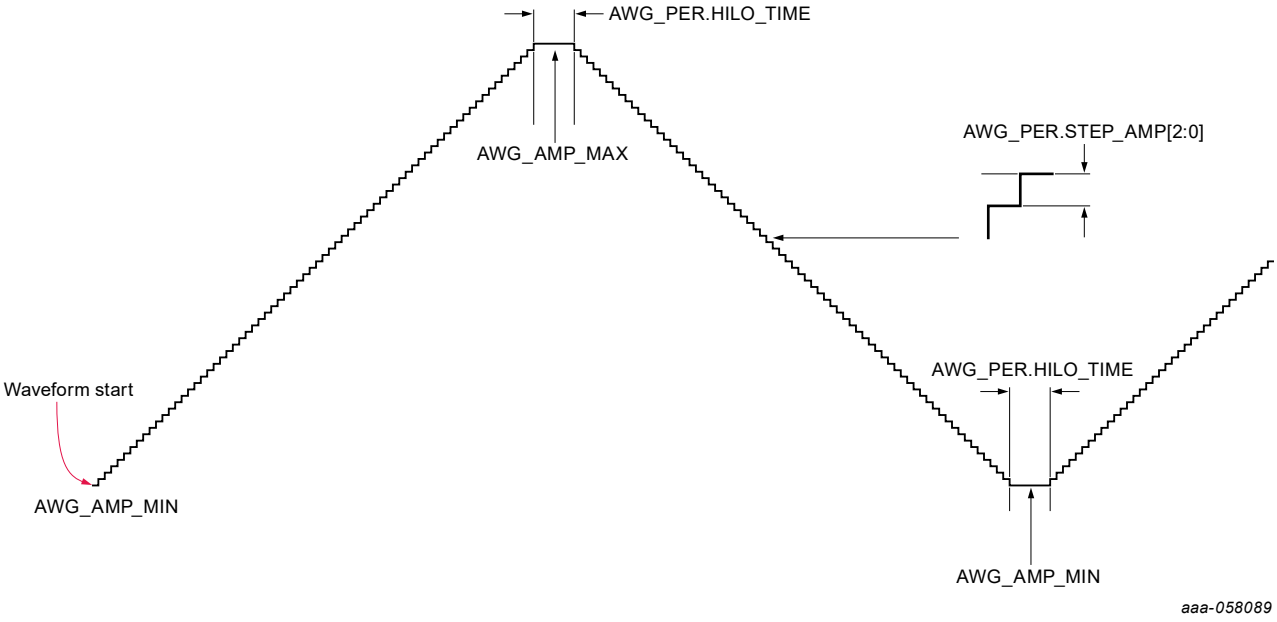


Figure 6. Auto-waveform generator timing

Note: *For some instances with different programming STEP_AMP value, AWG_AMP_MAX, or AWG_AMP_MIN value it is not possible to reach exactly. In these cases, the maximum, minimum code must be clamped to AWG_AMP_MAX, AWG_AMP_MIN value respectively.*

$$AMPmintomax\_steps = (Amp\_max - Amp\_min)/(step\_size * LSB)$$

$$AMPmintomax\_time = (AMPmintomax\_steps)/step\_freq$$

$$Waveform\_period = 2*(AMPmintomax\_time + HILO\_time)$$

$$Waveform\_freq = 1/Waveform\_period$$

For example:

For 18 bits

$$LSB = (25)/2\text{^}18 = 95.367\,\mu V$$

If Step_size(Code = 0) = 1024, Amp_max = 12.5 V, Amp_min = -12.5 V, then AMPmintomax_steps = 256.

If Step_period(Code = 0) = 4000, then AMPmintomax_time = 0.064 s.

If HILO_time = 0, then WF_freq = 7.8125 Hz.

Table 10. Generated waveform frequency with HILO time = 0

Generated waveform frequency (Hz)		STEP_Amp (18-bit)							
		0	1	2	3	4	5	6	7
Code	Step_period (Hz)	1024	2048	4096	8192	16384	32768	65536	131072
0	4000	7.8125	15.6250	31.2500	62.5000	125.0000	250.0000	500.0000	1000.0000
1	6000	11.7188	23.4375	46.8750	93.7500	187.5000	375.0000	750.0000	1500.0000
2	9000	17.5781	35.1563	70.3125	140.6250	281.2500	562.5000	1125.0000	2250.0000
3	12000	23.4375	46.8750	93.7500	187.5000	375.0000	750.0000	1500.0000	3000.0000
4	40000	78.1250	156.2500	312.5000	625.0000	1250.0000	2500.0000	5000.0000	10000.0000
5	60000	117.1875	234.3750	468.7500	937.5000	1875.0000	3750.0000	7500.0000	15000.0000
6	90000	175.7813	351.5625	703.1250	1406.2500	2812.5000	5625.0000	11250.0000	22500.0000
7	150000	292.9688	585.9375	1171.8750	2343.7500	4687.5000	9375.0000	18750.0000	37500.0000

7.3.5 ±36 V at the screw terminal AO pin

The IO module is protected at the AO screw terminal pin for voltage surge (IEC61004-5), with the help of TVS mounted on the board. The TVS must clamp the voltage within ±36 V.

The device must sustain ±36 V DC protection at the AO screw terminal pin with the help of a Schottky diode and series resistor, see Figure 25.

When the device is in the High-Z mode, the device must not load the AO pin at the screw terminal up to ±36 V.

7.3.6 Overcurrent protection in Voltage-output mode

The NAFE33350 is protected against overload and short-circuit.

Since the AO-AFE can operate in Voltage mode with different load, the current limit must be smart and configurable to adapt to different scenarios.

A typical scenario is the Voltage mode with capacitive load. In this case, during a voltage transient a surge current happens to charge the capacitor. The slew rate, voltage-step amplitude, and load capacitor determine the surge current. The overcurrent protection must be able to manage the short surge current to satisfy the settling time of the system. At the same time, the device must be protected from a real short.

For this reason, dual protection mechanisms are considered with a different current threshold and reaction time. The fast-reaction and high-current threshold (red area in Figure 7 and Figure 8) protects against severe short-circuit, while the slow-reaction and low-current threshold (green area in Figure 7 and Figure 8) protect against long-period overload.

The figures below report the time-dependent threshold profile and the current surge. When the surge current is below the current protection profile, see Figure 7, the protection circuit is not activated and the AO-AFE can charge the capacitor without interruption.

If the surge exceeds the short-circuit limit of 70 mA or lasts longer than the reaction time of 5 µA, the protection circuit activates and the part goes in High-Z mode. For details, see Figure 8. The following section explains how to handle such situations by using a device-programmable current limiter.

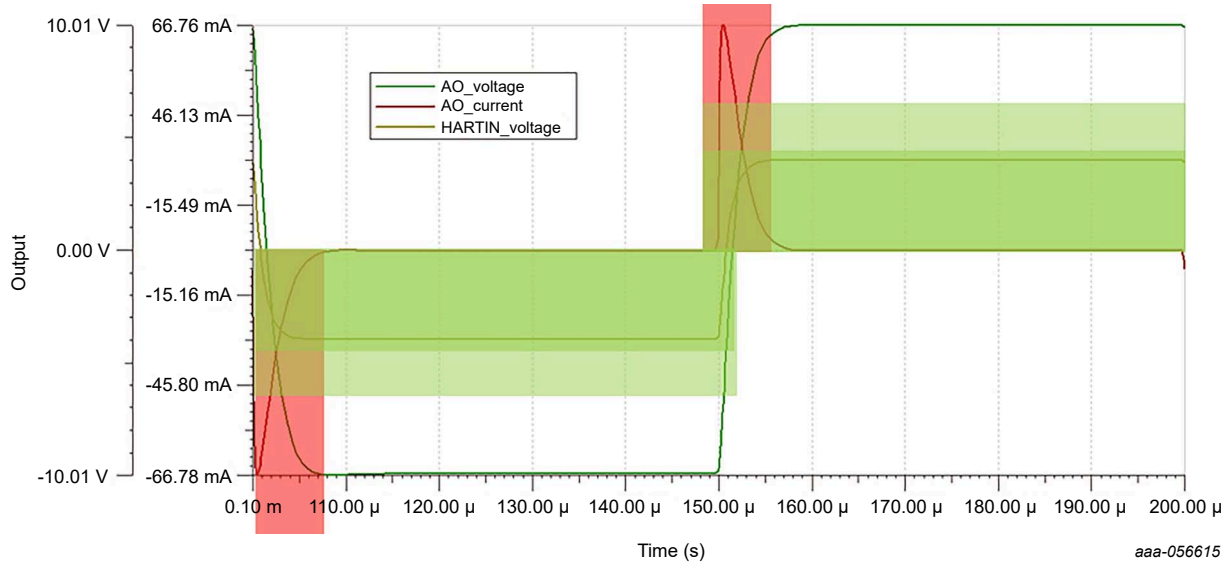


Figure 7. Current output profile in Vout mode with small Cload < 10 nF

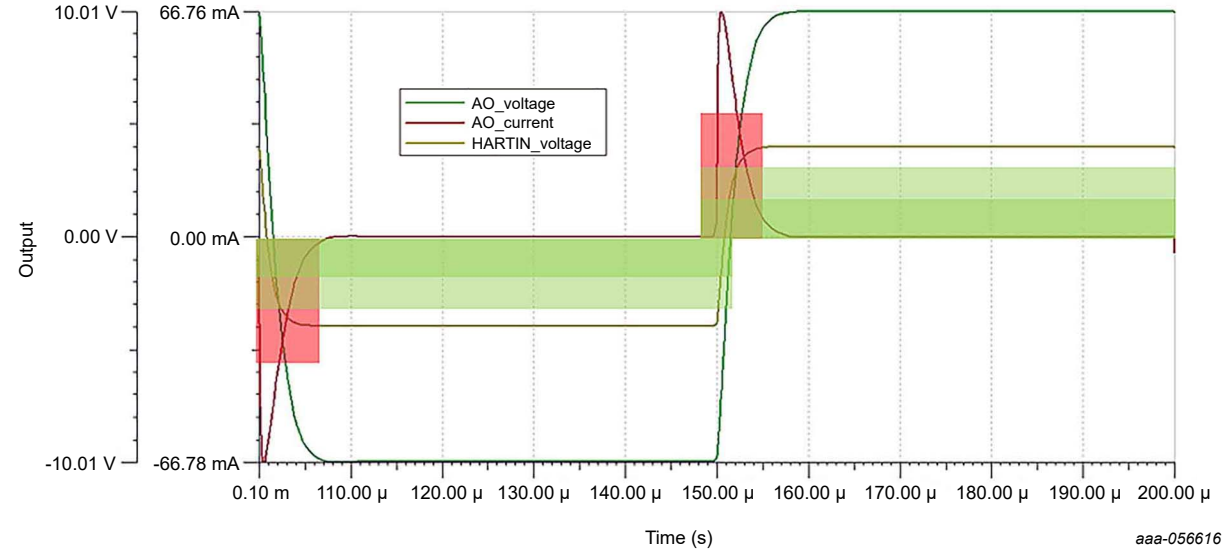


Figure 8. Current output profile in Vout mode with large Cload < 100 nF

Once a short-circuit is detected, the fast-current limiter limits the current to a max value of ~150 mA.

7.3.6.1 Overcurrent limits

This section describes short-circuit and overload circuit limits.

7.3.6.1.1 Short-circuit limits

- Short current threshold ~ ±70 mA (output stage coarse current limiter)
- Reaction time < 5 µs (faster)
- The current limiter limits the maximum current at ~ ±70 mA
- Overload is detected in approximately 1 µs - 2 µs, but not activated if the overload lasts < programmable 10 µs / 20 µs / 50 µs / 100 µs

7.3.6.1.2 Overload circuit limits

- Overload current threshold can be programmed to 5 mA, ±10 mA, ±20 mA, or ±25 mA.
  - If the overload condition happens, even after the deglitch timer, you can trigger the High-Z protection mode or initiate the programmable current limiter.
- Reaction time (for the current limit to settle) can be programmed to 25 µs, 50 µs, 100 µs, 200 µs with the default being 25 µs.
  - After the reaction time expires and if the overload (comparator output) is still active high, the output stage does the following:
    - Switch to Current-input mode and set a configured current limit output (< abs (±25) mA).
    - Set to High-Z (default safe state).
  - You can write the programmed overload threshold on the shadow register. The default value is ± 25 mA.
  - If, after a defined reaction time (current settling time), the current output is still over the current threshold, then the output stage is set in High-Z. An alarm is issued and the output stage status register is updated accordingly.
  - If, after a defined reaction time (current settling time), the current output is under the current threshold, then the output stage maintains the current output for a defined period as below:
    - Current limiter period:
      - Infinite.
      - Finite = 1 ms, 2 ms, 5 ms, 10 ms.
    - After the current limiter period, the digital control logic switches from Current mode to Voltage mode.

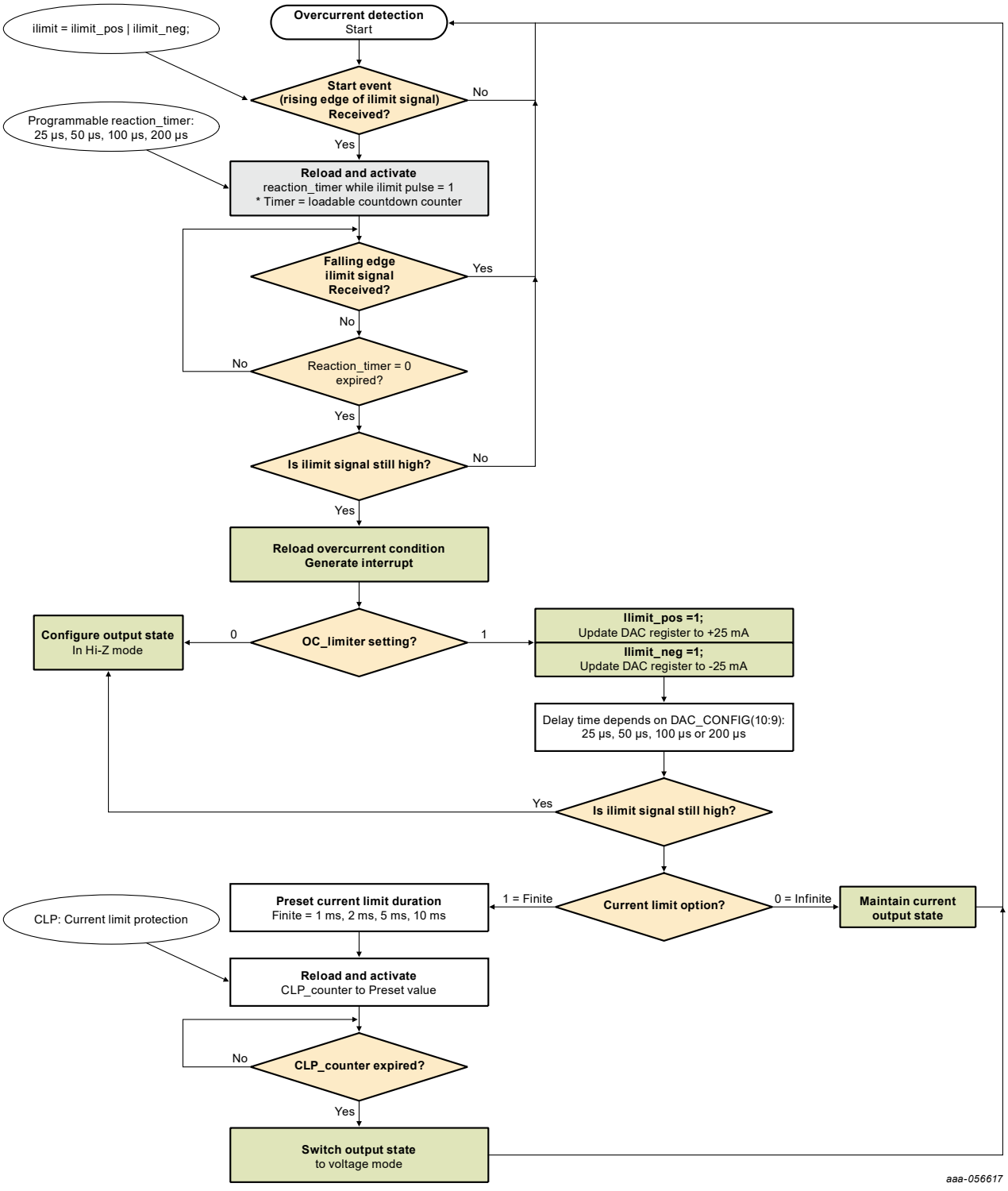


Figure 9. Overcurrent detection start

7.4 Transimpedance amplifier

A transimpedance amplifier (TRIAMP) is used to readback the voltage output as feedback for the output power amplifier.

7.5 Common system

The common system of the NAFE33350 device comprises selectable voltage reference source, clock source, and GPIOs.

7.5.1 Voltage reference sources

This section describes the voltage reference selector, low-draft internal voltage reference, external-voltage reference, and internally buffered reference for DAC.

7.5.1.1 Voltage reference selector

The voltage reference selector enables the selection of internal or external reference. The device uses an internal reference by default on power up and the user can assert SYS_CONFIG.REF_SEL to use an external 2.5 V reference.

7.5.1.2 Low-drift internal voltage reference

The AO-AFE integrates a precise voltage reference with a low-temperature coefficient to reduce the drift error overtemperature.

7.5.1.3 External-voltage reference input

The AO-AFE features a dedicated input pin to allow the connection to an external voltage reference.

7.5.1.4 Internally buffered reference for DAC

The AO-AFE has an independent internal buffer (sourced by either internal or external reference) to provide individual reference sources to the DAC block. To activate the DAC reference buffer, ensure that AO_SYSCFG.AO_ON is set as either 0x10 or 0x11. See, see Table 12.

7.5.2 General-purpose input/output

The AO-AFE has five pins (2, 3, 21, 22, 33) that serve dual purposes and can be configured as GPIO. The operating input and output voltage ranges are 0 V to VDD when these pins are configured as GPIO.

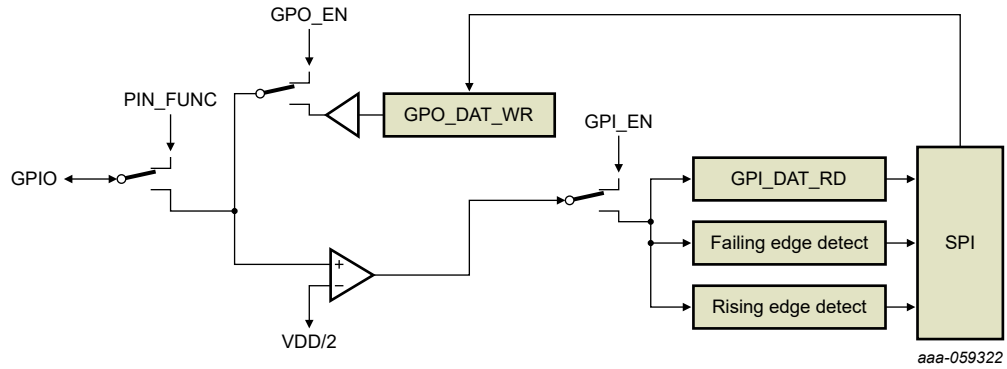


Figure 10. General-purpose input/output

The GPIO control and data registers are organized by 4x5 bits register.

1. GPI_DATA (0x23\h): Read (R) only register and it detects a level logic from the pad.
2. GPO_ENABLE (0x24\h): Read/write (R/W) GPO_EN register. It enables an output path.

3. GPIO_FUNCTION(0X25\h): R/W PIN_FUNC register.
4. GPI_ENABLE (0x26\h): R/W GPI_ENABLE. It enables the input path to allow reading data from the pad, looping back from the GPO_DATA register and/or GPIO edges detection.

GPIO both edges detection results in 2x5-bit register 0x27 for positive and 0x28 for negative respectively are implemented as follows.

While GPI_EN = 1 and GPIO_CON =1, during any transition from 0 ≥ 1 (positive edge) or 1 ≥ 0 (negative edge), the edge detection register is set to 1. This edge detection register is defined as sticky by nature and requires the host to clear it by writing 1 to the bit that is set to 1 (W1C).

7.5.3 Clock sources

The NAFE33350 provides flexible and configurable operating modes that can function with two different clock sources: internal RC oscillator and external oscillator.

Figure 11 shows the clock architecture.

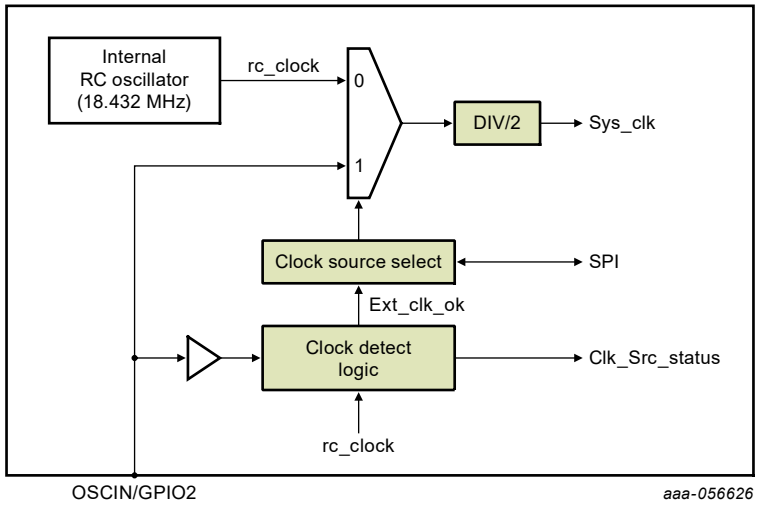


Figure 11. Clock source selector

7.5.3.1 Internal RC oscillator

The AO-AFE integrates an internal oscillator to allow autonomous and cost-effective operation without support of any external clock source.

The internal oscillator nominal frequency is 18.432 MHz.

7.5.3.2 External oscillator

The AFE can also operate with an external oscillator to enable applications that require synchronization between the AFE and the host. It also allows coherent sampling of the input signal.

Ensure that the external oscillator is applied to pin OSCIN. If not used, OSCIN can be left floating.

7.5.3.3 Clock selection

At power on, the AFE starts with the internal RC oscillator.

The NAFE33350 provides the following mechanisms for system clock selection:

- User selection via system register configuration
  - The AO-AFE detects the presence of the external oscillator before activating the external oscillator input.
  - If the external oscillator is not detected, the AFE continues to operate with the internal clock and provides an error message via the error status register.

For details, see Table 14.

7.5.3.4 User selection of clock sources

The user selection option allows the user to select the desired clock after power on. The clock source can be selected by writing to the clock source system configuration register.

Check the presence of the external clock while making external clock selection in the system configuration register to ensure proper functioning of the NAFE33350. If the external clock is detected and the NAFE33350 switches to the external clock, the system status register is updated accordingly. If the external clock is not detected, the NAFE33350 maintains the previous clock configuration.

7.5.3.5 Clock frequency drift detection

Whenever clock_src_sel [1:0] is set to 2'b11 or 2'b10, the clock period monitoring is activated. This circuit continuously measures the clock frequency difference between the external clock and the internal RC oscillator INTOSC.

The default value of the clock frequency difference is set to 20 % at power-on reset (POR). The clock comparison logic issues an alarm when the running average clock count difference is greater than 20 %. The alarm status bit for clock variation is user accessible via SPI register. The average time window is ~64 ms. If the external clock is selected as the system clock source and the EXTCLK_FREQ_ALRM bit is enabled, the external clock alarm interrupt is triggered. The trigger occurs when (EXTCLK_FREQ_INT = 1) and the EXTCLK is not within the 20 % period difference.

7.6 User register map

The user register maps are categorized into the following:

1. Output channel configuration, status, and data registers
2. System configuration, status, and alarm registers
3. Calibration coefficients, PN, and SN

Table 11. 24-bit user registers - AI channel data

24-bit user registers - AI channel data					
AI_DATA0..7 0x30\h - 0x37\h	23:0	DATA0 … DATA7	R	0x000000	Channel output data. Each channel has a corresponding data register. DATA0[23:0] is converted data output of CH0...DATA7[23:0] is converted output of CH7.
AI_CH_OVR_THR 0x38\h - 0x3F\h	23:0	OVR_THRS0 ... OVR_ THRS7	RW	0x000000	Overrange threshold setting for each logical data channel.
AI_CH_UDR_THR 0x40\h - 0x47\h	23:0	UDR_THRS0 ... UDR_ THRS7	RW	0x000000	Underrange threshold setting for each logical data channel.

Table 12. 16-bit user registers - output channel configuration registers

16-bit user registers - output channel configuration registers					
AIO_CONFIG 0x20\h	15	Reserved	R	0x0	
	14	VSA ON	RW	0x0	VSA ON = 1 turn ON VSA. Exception: AO_MODE = 10\b Voltage output mode force VSA ON = 1, this bit cannot be overwritten.

Table 12. 16-bit user registers - output channel configuration registers...*continued*

16-bit user registers - output channel configuration registers					
	13	CSA ON	RW	0x0	CSA ON = 1 turn ON CSA. Exception: AO_mode = 11\b Current output mode force CSA ON = 1, this bit cannot be overwritten.
	12	CISW_ON	RW	0x0	CISW_ON = 1 turn ON the current input switch connected to the ground. CISW is used with external Rsense for Current input mode configuration. ***Note:*** *To avoid short-circuit, CSIW_ON must be 0\h when the PA_ON = 1, if the CISW pin is connected to the AOP/AON path.*
	11:7	Reserved	R	0x0	Reserved
	6:5	AO_MODE	RW	0x0	AO_MODE Pre-configured AO modes. 00\b: Hi-Z mode, PA_ON = 0, VSA_ON = x, CSA_ON = x 10\b: Voltage output mode, PA_ON = 1, VSA_ON = 1, CSA_ON = x 11\b: Current output mode, PA_ON = 1, VSA_ON = x, CSA_ON = 1
	4	UNIPOLAR_AO_MODE	RW	0x0	Select AO mode: 0\h = Bipolar AO mode 1\h = Unipolar AO mode. See Section 7.14.
	3:2	Reserved	R	0x0	Reserved
	1:0	AO_TCC	RW	0x00	Proprietary AO temperature coefficient correction: 00\b = select AO_TCC for VO mode 01\b = select AO_TCC for CO mode 1x\b = Disable
AO_CAL_COEF 0x21\h	15	Reserved	R	0x0	Reserved
	14:12	DAC_CAL_COEF	RW	0x0	Pointer to select DAC gain and offset calibration coefficients [3-BITS]
	11:0	Reserved	R	0x0	Reserved
AIO_PROT_CFG 0x22\h	15:13	AO_CLIM_PER	RW	0x0	Select the output current limit duration at AOP, AON: 0\h = 1 ms, 1\h = 2 ms, 2\h = 5 ms, 3\h = 10 ms; 4\h = 20 ms; 5\h = 50 ms; 6\h = 20 ms; 7\h = infinite. When the timer expires, if the AO_CLIM_PER timer duration is finite, the AO mode is changed back to VO mode. If the AO_CLIM_PER timer duration is infinite, it remains in limited current mode.
	12:11	AO_OVRLOAD_CUR_THR	RW	0x0	Select the output overload current thresholds at AOP, AON pin: 0\h = ±25 mA; 1\h = ±20 mA; 2\h = ±10 mA; 3\h = ±5 mA.
	10:9	AO_OVRCUR_DEG	RW	0x0	Set the output overcurrent deglitch timer duration. AO_OVRCUR_DEG is re-armed whenever DAC code or AO mode change. Then, the timer is triggered upon an AO_SHRT_L or AO_OVRLOAD_L alarm and lasts for a duration of 0\h = 10 µs; 1\h = 20 µs; 2\h = 50 µs; 3\h = 100 µs. When the timer expires, if AO_SHRT_L = 1 persists, the AO is put into High-Z mode and the AO_STATUS is set to 01\b if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 0) and (AO_OVRLAOD_PROT = 0), the AO is put into High-Z mode and the AO_STATUS is set to 01\b if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 1) and (AO_OVRLAOD_PROT = 1), the AO is put into limited current mode and the AO_STATUS is set to 11\h. A_CLIM_SD controls the initial duration.
	8	AO_OVRLOAD_PROT	RW	0x0	Set the overload protection behavior and post the AO_OVR_CUR_RT reaction timer: In the event of a programmable overload condition (set by AO_OVRLOAD_CUR_THR), if 0\h = configure AO in High-Z mode and set AO_STATUS = 3\h 1\h = configure AO in current limiter mode and set AO_STATUS = 2\h during AO_CLIM_SD.
	7:6	AO_CLIM_SD	RW	0x0	Configure the output current limiter settling delay timer to allow the current limiter to settle. 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs. When the timer expires, if (AO_SHRT_L = 1), the AO is put into High-Z mode, and AO_STATUS alarm is set to 01\b; if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 0), the AO stays in limited current mode during AO_CLIM_PER, and the AO_STATUS alarm is set to 11\b. During the AO_CLIM_PER period, (AO_SHRT_L = 1) | (AO_OVRLOAD_L = 1) puts the AO into High-Z mode and AO_STATUS alarm is set to 01\b.
	5:4	CISW_OVRCUR_DEG	RW	0x0	CISW input overcurrent deglitch timer duration 0\h = 10 µs; 1\h = 20 µs; 2\h = 50 µs; 3\h = 100 µs; When the timer expires, if CISW_SHRT_L = 1, the CISW is turned OFF, and the CISW_STATUS bit is reset. If (CISW_SHRT_L = 0) and (CISW_OVRLOAD_L = 1), the CISW current limiter mode is activated, and the CISW_STATUS bit is set. If (CISW_SHRT_L = 0) and (CISW_OVRLOAD_L = 0), the CISW remains turned ON.

Table 12. 16-bit user registers - output channel configuration registers...*continued*

16-bit user registers - output channel configuration registers					
	3:2	CISW_CLIM_PER	RW	0x0	CISW input over the current limit period: 0\h = 1 ms; 1\h = 2 ms; 2\h = 5 ms; 3\h = 10 ms
	1:0	CISW_CLIM_SD	RW	0x0	CISW input current limiter settling delay timer 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs; After the timer expires, if CISW_SHRT_L = 1 or CISW_OVRLOAD_L = 1 persists, the AO is set in High-Z mode. If AO_SHRT_L = 0 and AO_OVRLOAD = 0, the AO stays in current limiter mode during AO_CLIM_PER. During the CISW_CLIM_PER, if CISW_SHRT_L = 1 or CISW_OVRLOAD = 1, the CISW is opened.
AO_SLR_CTRL 0x23\h	15	SLREN	RW	0x0	Slew rate enabled = 1; default 0: disabled.
	14:12	SLR_STEP	RW	0x0	Slew rate step. See Table 7.
	11:9	SLR_CLOCK	RW	0x0	Slew rate update clock. See Table 6.
	8	Reserved	R	0x0	Reserved
	7:0	Reserved	R	0x0	Reserved
AWG_PER 0x24\h	15:13	STEP_AMP	RW	0x0	Programmable step size: eight-step sizes, amplitude step. See Section 7.3.4.
	12:10	STEP_freq	RW	0x0	Programmable frequency update: eight freq. update. See Table 8.
	9:0	HILO_TIME	RW	0x000	Programmable high/low time in term of number of STEP_PERIOD(= 1/STEP_FREQ). See Table 10.
AO_SYSCFG 0x25\h	15	SYNCDAC_EN	RW	0x0	If SYNCDAC_EN = 0\b, the DAC code is latched by the rising edge of CSB. If SYNCDAC_EN = 1\b, the DAC code is latched by the rising edge of the External SYNCDAC pulse. ***Note:*** *The SYNCDAC pin serves as the device address (ADR0) at POR. During POR, if the ADR0 is at logic level HIGH, the address is set to 1, otherwise it is set to 0. After POR the pin functions as SYNCDAC.*
	14	DAC_DATA_16BIT	RW	0x0	0\h = NUMBER OF SPI DAC DATA = 3 BYTE [24-BIT] 1\h= NUMBER OF SPI DAC DATA = 2 BYTE [16-BIT]
	13	STATUS_STICKY_AO	RW	0x0	Prepended status bits behavior when reporting AO_OC or CI_OC status while STATUS_EN = 1. 1\h = sticky; 0\h = live.
	12	Reserved	R	0x0	Reserved
	11:10	AO_ON	RW	0x0	(AO_ON[1:0]) / DAC_en / DACREFBUF_en 0 0 / 0 / 0 0 1 / 0 / 1 1 0 / 1 / 1 1 1 / 1 / 1 ***Note:*** *Set AO_ON = 11 along with AO_MODE = 10\b or 11\b if an internal DAC is used for generating voltage and current output.*
	9:0	Reserved	R		Reserved
AIO_STATUS 0x26\h	15	CISW_STATUS	R	0x0	CISW live status. CISW status to compare against CISW_ON configuration.
	14	CSA_STATUS	R	0x0	CSA live status
	13	VSA_STATUS	R	0x0	VSA live status
	12:11	AO_STATUS	R	0x0	AO status to check against the AO configuration. The AO status can differ from the configuration as the protection circuits, if triggered, puts the AO into a Safe state. 00\b: High-Z mode, PA_ON = 0. 01\b: High-Z mode, set by the protection circuit. 10\b: Voltage output mode, PA_ON = 1, VSA_ON = 1. VFB mode 11\b: Current output mode, PA_ON = 1, CSA_ON = 1. CFB mode
	10:9	Reserved	R		Reserved
	8	Slew Rate_ON	R	0x0	Live detection 0\h: Slew rate control inactive 1\h: Slew rate control active

Table 12. 16-bit user registers - output channel configuration registers...*continued*

16-bit user registers - output channel configuration registers					
	7	AO_SHRT_L	R	0x0	Live detection 0\h: Current output short-circuit detection non-active 1\h: Current output short-circuit detection active
	6	AO_OVRLOAD_L	R	0x0	Live detection 0\h: Current output overload detection ON = 0 1\h: Current output overload detection ON = 1
	5	CISW_SHRT_L	R	0x0	Live detection 0\h: Current input short-circuit detection ON = 0 1\h: Current input short-circuit detection ON = 1
	4	CISW_OVRLOAD_L	R	0x0	Live detection 0\h: Current input overload detection ON = 0 1\h: Current input overload detection ON = 1
	3	CISW_SHRT_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_CISW_ABORT/CMS_CISW_ABORT_HIZ to clear 0\h: Current input short-circuit detection ON = 0 1\h: Current input short-circuit detection ON = 1
	2	CISW_OVRLOAD_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_CISW_ABORT/CMS_CISW_ABORT_HIZ to clear 0\h: Current input overload detection ON = 0 1\h: Current input overload detection ON = 1
	1	AO_SHRT_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_AO_ABORT/CMS_AO_ABORT_HIZ to clear 0\h: Current output short-circuit detection ON = 0 1\h: Current output short-circuit detection ON = 0
	0	AO_OVRLOAD_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_AO_ABORT/CMS_AO_ABORT_HIZ to clear 0\h: Current output overload detection ON = 0 1\h: Current output overload detection ON = 1

Table 13. 24-bit user registers - AO channel data

24-bit user registers - AO channel data					
AO_DATA 0x28\h	23:0	DAC_DATA	RW	0x000000	[23:6] 18-bit DAC code: Analog_trim0[1:0] = 0; Range: -131072 to +131071 [23:8] 16-bit DAC code: Analog_trim0[1:0] = 1; Range: -32768 to +32767 [23:10] 14-bit DAC code: Analog_trim0[1:0] = 2; Range: -8192 to +8191 [23:12] 12-bit DAC code: Analog_trim0[1:0] = 3; Range: -2048 to +2047
AO_OC_POS_LIMIT 0x29\h	23:0	OUT_OC_POS_LIMIT	RW	0x000000	Output overcurrent limit – positive [23:6] 18-bit - CSA
AO_OC_NEG_LIMIT 0x2A\h	23:0	OUT_OC_NEG_LIMIT	RW	0x000000	Output overcurrent limit – negative [23:6] 18-bit - CSA
AWG_AMP_MAX 0x2B \h	23:06	AMP_WMAX	RW	0x000000	[23:6] 18-bit MAX code range: -131072 to 131071. See Section 7.3.4.
	5:0	Reserved	R	0x0	Unused
AWG_AMP_MIN 0x2C\h	23:06	AMP_WMIN	RW	0x000000	[23:6] 18-bit MAX code range: -131072 to 131071. See Section 7.3.4.
	5:0	Reserved	R	0x0	Unused

Table 14. 16-bit user registers - common system configuration and status

16-bit user registers - common system configuration and status					
CRC_CONF_REGS 0x20\h	15:0	CRC_CONF_REGS	R	0x0000	Calculated CRC results of the current user configuration registers (RW) except the status and data output register (R).
CRC_COEF_REGS 0x21\h	15:0	CRC_COEF_REGS	R	0x0000	Calculated CRC results of the current user 24-bit coefficient registers (RW).
CRC_TRIM_REGS 0x22\h	15:0	CRC_TRIM_REGS	R	0x0000	Calculated CRC output result of all the current internal trim registers (R internal)
CRC_TRIM_REF 0x3F\h	15:0	CRC_TRIM_REF	R	0x0	Stored reference result of precalculated CRC at production of internal trim registers, to be used for comparison against CRC_TRIM_REGS. (R internal)
GPI_DATA 0x23\h	15:11	GPI_DATA	R	0x00	GPI data detected: 0 = Logic 0 (DGND), 1 = Logic 1 (DVDD). GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0x00	Reserved
GPO_ENABLE 0x24\h	15:11	GPO_ENABLE	RW	0x00	GPO driving enable: 0 = disabled driving, 1 = enabled driving. GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0x00	Reserved
GPIO_FUNCTION 0x25\h	15:11	PIN_FUNC	RW	0x00	0 = Normal pin function, 1= GPIO function. GPIO4 is mapped to bit15. GPIO0 is mapped to bit11.
	10:0	Reserved	R	0x0000	Reserved
GPI_ENABLE 0x26\h	15:11	GPI_ENABLE	RW	0x00	GPI read enable: 0 = disabled read, 1 = enabled read. GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0X00	Reserved
GPI_EDGE_POS 0x27\h	15:11	GPI_EDGE_POS	R	0x00	GPI positive edges data: 0\h = none, 1\h = positive edge detected. Cleared after readback or CMD_CLEAR_ALRM.
	10:0	Reserved	R	0x0000	Reserved
GPI_EDGE_NEG 0x28\h	15:11	GPI_EDGE_NEG	R	0x00	GPI negative edges data: 0\h = none, 1\h = negative edge detected. Cleared after readback or CMD_CLEAR_ALRM.
	10:0	Reserved	R	0x0000	Reserved
GPO_DATA 0x29\h	15:11	GPO_DATA	RW	0x00	Set GPO output data: 0\h = output logic 0, 1\h = output logic 1. GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0x0000	Reserved
SYS_CONFIG 0x2A\h	15:9	Reserved	R	0x0	Reserved
	8	REF_SEL	RW	0x0	Select internal or external 2.5 V voltage references for DACREFBUF: 0\h = selects internal 2.5 V (REF_INT). 1\h = selects external 2.5 V (REF_EXT). ***Note:*** *Internal reference is always powered on.*
	7	GLOBAL_ALRM_STICKY	RW	0x0	Global alarm interrupt behavior is: 0\h= non-sticky, read to clear and it is live status. 1\h= sticky, write 1 to clear a specific bit.
	6	SPI_DOUT_DRIVE	RW	0x0	Increase DOUT output drive if high capacitance loading.
	5	INTB_DRIVER_TYPE	RW	0x0	INTB pin driver type:

Table 14. 16-bit user registers - common system configuration and status*...continued*

16-bit user registers - common system configuration and status					
					0 = 100 kΩ pullup with open-drain. 1 = CMOS push-pull.
	4	CRC_EN	RW	0x0	Enable CRC: 0\h = disable, 1\h = enable.
	3:0	Reserved	R	0x0	Reserved
SYS_STATUS 0x2B\h	15:14	Reserved	R	0x0	Reserved
	13	CHIP_READY	R	0x0	Chip status indicator. Upon power up, the INTB pin goes LOW (active low) to indicate the chip is ready. The user must read this register to clear the INTB pin. This bit stays HIGH when the chip is operational. 0\h = Chip is not yet ready, 1\h = Chip is ready.
	12	Reserved	R	0x0	Reserved
	11:10	CK_SRC_SEL_STAT	R	0x0	Status indicating the system clock in use: 0x\b: Internal clock in use. 1x\b: External clock in use.
	9	CRC_ERROR_S	W1C	0x0	CRC error encountered on the COTI line before the last transmission. ***Note:*** *Write 1 to clear.*
	8	CRC_ERROR_L	R	0x0	CRC error encountered on COTI line on last transmission.
	7:0	Reserved	R	0x0	Reserved
CK_SRC_SEL_CONFIG 0x30\h	15:12	Reserved	R	0x0	Reserved

	11:10	CK_SRC_SEL	RW	0x0	If (GPIO_FUNCTION[13] = 0\b) and (CK_SRC_SEL = 0x\b), select the internal clock;
					If (GPIO_FUNCTION[13] = 0\b) and (CK_SRC_SEL = 1x\b), select the applied external clock at OSCIN/GPIO2;
					Note: *Switch time ~ 5 µs.*
					If (GPIO_FUNCTION[13] = 1\b), the OSCIN/GPIO2 pin operates as GPIO, and the internal clock is selected;
					Note: *Only during POR, an internal auto-selection logic selects the external clock source at OSCIN/GPIO2 pin if a clock signal is detected.*
					Before CHIP_READY is set to logic 1, the internal or external clock has already been selected and the auto-selection logic is disabled.
					Note: *~ 2 ms*

	9:0	Reserved	R	0x0	Reserved

Table 15. 16-bit user registers - global alarm configuration and status

16-bit user registers - global alarm configuration and status					
GLOBAL ALARM ENABLE 0x2C\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 ºC.
	14	HVDD_ALRM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13				
	12				
	11	CRC_ALRM	RW	0x0	Enable an alarm for CRC error detection on COTI line.
	10	GPI_POS_ALRM	RW	0x0	Enable an alarm for rising edge detected at any of the GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enable an alarm for falling edge detected at any of the GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enable alarm for register configuration error.
	7	Reserved			
	6	Reserved			
	5	Reserved			

Table 15. 16-bit user registers - global alarm configuration and status...*continued*

16-bit user registers - global alarm configuration and status					
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enable the alarm when the EXTCLK frequency varies with the internal CLK by XX.
	3	AO_OC_ALRM	RW	0x0	Enable alarm for analog output overcurrent.
	2	Reserved	RW	0x0	Enable alarm for analog input overcurrent.
	1	AO_SHRT_ALRM	RW	0x0	Enable a short alarm.
	0	TEMP_ALRM	RW	0x0	Enable a programmable temperature alarm. The threshold is set in THRS_TEMP register bits.
GLOBAL ALARM INT 0x2D\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	14	HVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	13	HVSS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	12	ADVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	11	CRC_ERR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	10	GPI_POS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	7	Reserved			
	6	Reserved			
	5	Reserved			
	4	EXTCLK_FREQ_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	3	AO_OC_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	2	CI_OC_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	1	AO_SHRT_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	0	TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
DIE_TEMP 0x2E\h	15:0	DIE_TEMP	R	0x00	16-bit die temperature readout in two's complement. Temperature = DIE_TEMP value/64 °C
TEMP_THRS 0x2F\h	15:0	TEMP_THRS	RW	0x00	Temperature threshold in two's complement for setting a custom temperature warning alarm.

Table 16. 16-bit user registers - part number

16-bit user registers - part number					
PN2 0x40\h	15:0	PN2	R	0x00	Part number (MSB). Example, 3335 for NAFE33350 B40BS part number
PN1 0x41\h	15:0	PN1	R	0x00	Part number (Mid-LSB). Example, 2B40 for NAFE33350 B40BS
PN0_REV 0x42\h	15:8	PN0	R	0x00	Part number (LSB). Example, 00 for NAFE33350 B40BS
	7:0	REVISION_ID	R	0xB0	Revision

Table 17. 24-bit user registers - serial number

24-bit user registers - serial number					
REGISTER(24-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
SERIAL1 0x43\h	23:0	SN1	R	0x	[23:0] Unique serial number (MSB)
SERIAL0 0x44\h	23:0	SN0	R	0x	[23:0] Unique serial number (LSB)

7.7 SPI and controls

This section describes the SPI signal pins, communication protocols, commands, and byte-wise write command. Also, it describes the register write with CRC enabled, DAC conversion timing, and CRC generator.

7.7.1 SPI signal pins

The SPI-compatible serial interface reads the conversion data and internal register content, and configures the device to control the DAC. The serial interface consists of four signals: CSB, SCLK, COTI, and CITO. One external pin is used as a SPI address, such that the host can address two devices without using a separate CSB pin. In addition, the DRDY and SYNC signals allow handshaking and data synchronization between the host and the device. The conversion data are provided with an optional CRC code to improve data integrity. The DAC word can be written with and without an 8-bit CRC appended at the end of data.

CSB (active low) is an input pin that enables the communication between the host and the chip. CSB must remain low entire data transaction. When CSB is set to high, the serial interface is reset, SCLK input and command inputs are ignored.

SPI_ADDR is an additional SPI address pin, in addition to CSB.

SCLK is a serial interface clock that can operate up to 32 MHz. It is a noise-filtered, Schmitt-triggered input used to clock data in/out of the chip. Serial input data is latched in the falling edge of SCLK and serial data outputs from the chip are updated on the rising edge of SCLK.

COTI is the serial data input to the chip. COTI is used to input commands and register data to the chip.

CITO is the serial data output from the chip. CITO is contained in the internal registers data, status byte, and/or 8-bit CRC if CRC_EN and/or STATUS_EN set to 1, respectively. When CSB is high, CITO is in high-impedance, tri-state mode. CITO is updated on the rising edge of the SCLK.

DRDY (active low to high) is an output pin that displays the conversion status. DRDY is driven from low-to-high when the conversion result is ready for reading. It stays high for a finite duration.

SYNCDAC is used to synchronize the DAC operation to the rising edge of an external signal rather than CSB rising edge.

INTB (active low) is an output pin that notifies the occurrence of a global alarm interrupt.

7.7.2 SPI communication protocols

The SPI user communication protocol is described in the following section. To initiate communication, the SPI host must always start with DEV_AD bit either 0 or 1 to match the pin of the ADDR0 device.

The following bits are:

- RW bit (read or write transaction)
- SYS_L
- 2-bit Dev_IO
- 2-bit Ch
- 8 RA bits (addressable up to 8192 location)
- D is data from host to device (or device to host depending on write or read operation, respectively)

SYS_L and Dev_IO are used to access different subsystem registers of the chip, for example, DAC and common.

Bit	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22		1	0
	DEV_AD	RW_L	SYS_L	DEV_IO1	DEV_IO0	CH1	CH0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	D23	D22		D1	D0
	RA12	RA11	RA10	RA9	RA8																

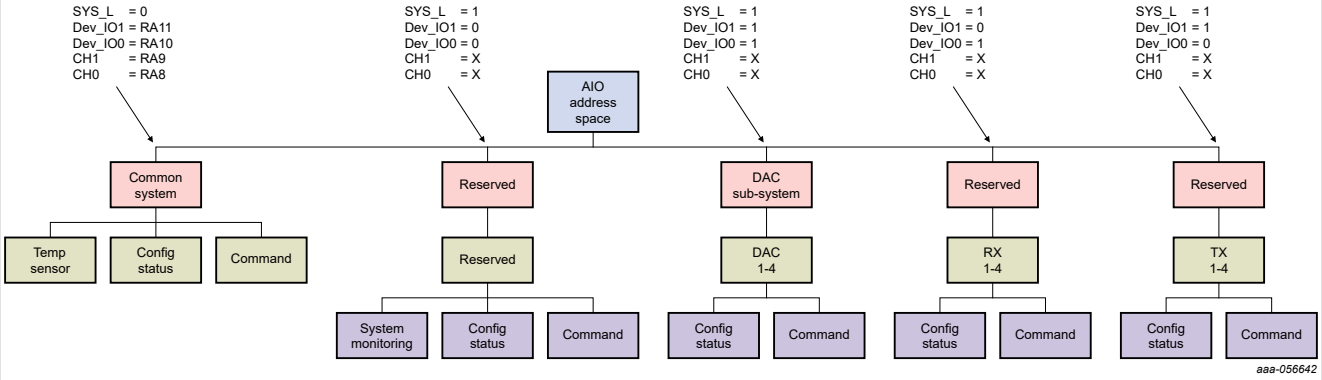


Figure 12. SPI framework

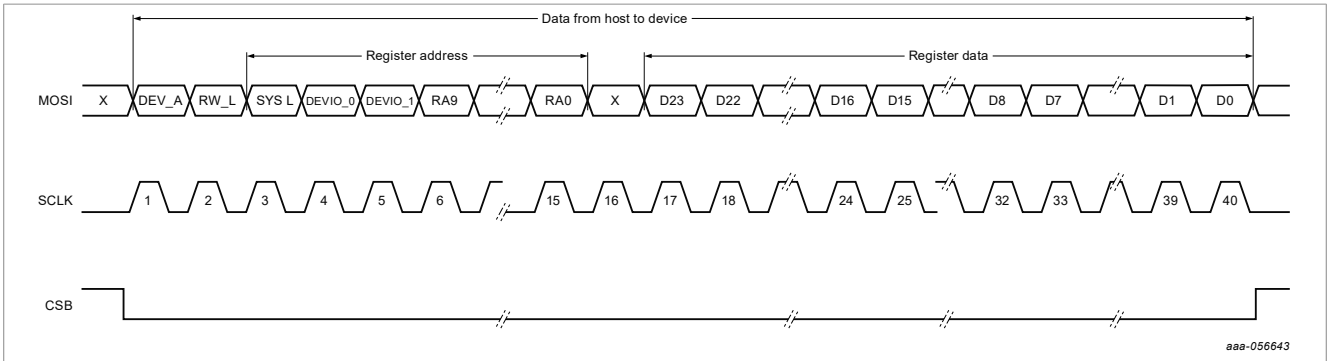


Figure 13. SPI register write timing diagram

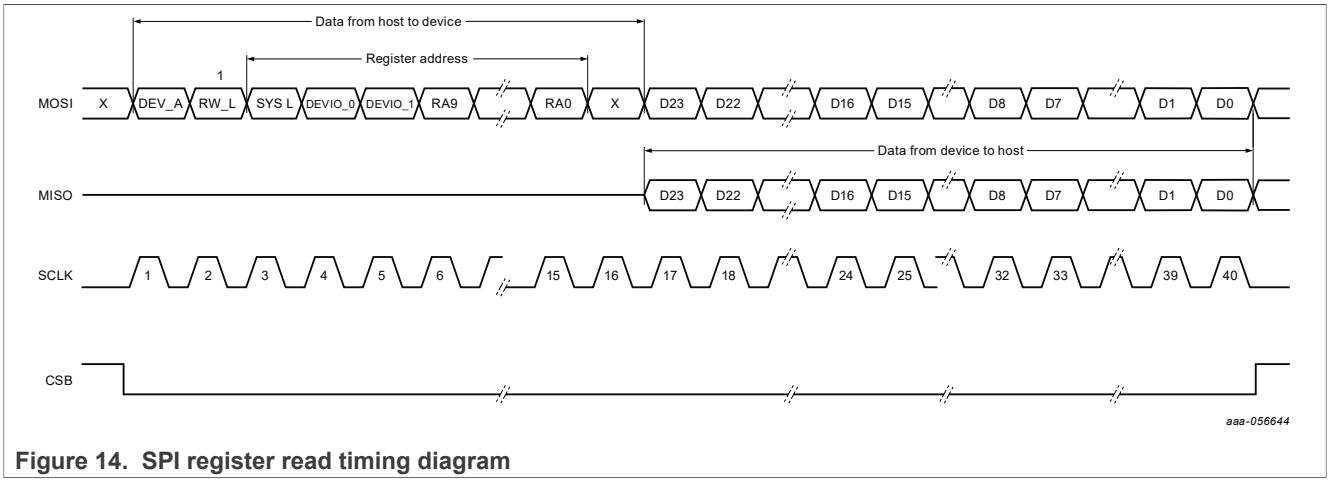


Figure 14. SPI register read timing diagram

7.7.3 SPI command

SPI commands are dedicated SPI address with predefined functions that reduce SPI transactions on frequent data accesses and controls.

CMD_RELOAD: Only reload OTP contents to shadow registers. OTP contents consist of NAFE33350 trims parameters and offset and gain calibration coefficients. This command does not reset user registers.

CMD_CLEAR_REG: Only clear user-accessible registers except the clock source select.

CK_SRC_SEL[1:0] does not get clear even if they are part of user registers. User can change this register after PORB while any conversion is in active state. For instance, CK_SRC_SEL was held other value than 0 before the command was issued, it stays the same after this command was issued.

Table 18. Common system commands

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Common system commands	*Mnemonic*
DEV_AD	RW_L	SYS_L = 0	Dev_IO1	DEV_IO0	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	Command description	
X	0	0	0	0	0	0	0	0	0	1	0	0	1	0	X	CMD_CLEAR_ALRM: Clear global alarm	***CMD_ CLEAR_ ALARM***
X	0	0	0	0	0	0	0	0	0	1	0	1	0	0	X	CMD_RESET: (HW reset, same as RSTB pulled low)	***CMD_RESET***
X	0	0	0	0	0	0	0	0	0	1	0	1	0	1	X	CMD_CLEAR_REG: (SW clears all user registers to default values except SYS_ CONFIG0 register).	***CMD_ CLEAR_REG***
X	0	0	0	0	0	0	0	0	0	1	0	1	1	0	X	CMD_RELOAD: Reload stored contents from on-chip non-volatile memory.	***CMD_ RELOAD***
X	0	0	0	0	0	0	0	0	0	1	0	1	1	1	X	Reserved	***Reserved***
X	1	0	0	0	0	0	0	0	0	0	0	1	1	0	X	CMD_CALC_CRC_CONFG: Calculate the CRC sum for all 16-bit user configuration registers and save the result to CONF_REGS_CRC register.	***CMD_CALC_ CRC_CONFG***
X	1	0	0	0	0	0	0	0	0	0	0	1	1	1	X	CMD_CALC_CRC_COEF: Calculate the CRC sum for all 24-bit CAL coefficient and threshold registers and save the result to COEF_REGS_ CRC register.	***CMD_CALC_ CRC_COEF***
X	1	0	0	0	0	0	0	0	0	0	1	0	0	0	X	CMD_CALC_CRC_FAC: Calculate all factory OTP trim registers and save the result to TRIM_REGS_CRC register (save factory sum in memory somewhere: OTP's PA: TDB).	***CMD_CALC_ CRC_FAC***
X	X	0	0	0	0	0	0	0	0	X	X	X	X	X	X	TBA	
X	1	0	0x200-0xFFF												X	Common system's register read via SPI	
X	0	0	0x200-0xFFF												X	Common system's register write via SPI	

Table 19. DAC system command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DAC0-3 (CH1 = X, CH0 = X) subsystem's commands: Dev_IO1 = 1, Dev_IO0 = 1 => DAC	*Mnemonic*
DEV_AD	RW_L	SYS_L = 1	Dev_IO1	Dev_IO0	CH1	CH0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	Command description	
X	0	1	1	1	0	0	0	0	0	0	0	0	0	0	X	CMD_WGEN_STOP: Stop the auto_waveform generator	***CMD_WGEN_ STOP***
X	0	1	1	1	0	0	0	0	0	0	0	0	0	1	X	CMD_WGEN_START: Command to start auto-generation DAC waveform output	***CMD_WGEN***
x	0	1	1	1	0	0	0	0	0	0	0	0	1	0	X	CMD_CLEAR_DAC0: Command to set DAC output to a mid-scale level similar at POR. It also resets the slew rate state machine when it is progress. While wave gen is in progress, this command is ignored. Midscale level at user's 18-bit = 'h00000;	***CMD_CLR_ DAC0***
x	0	1	1	1	0	0	0	0	0	0	0	0	1	1	X	CMD_AO_ABORT: Abort the running AO overcurrent protection FSM after a detected overcurrent in VO or CO mode. CMD_AO_ABORT: Exit the running AO overcurrent	***CMD_AO_ ABORT***

Table 19. DAC system command*...continued*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DAC0-3 (CH1 = X, CH0 = X) subsystem's commands: Dev_IO1 = 1, Dev_IO0 = 1 => DAC	*Mnemonic*
																protection FSM after clearing the sticky status for AO overcurrent, AO_SHRT_S, and AO_OVRLOAD_S and overwriting the AO mode field of AO_config with the previous mode (VO or CO mode) and updating DAC value with user register DAC value. Then go to Idle state. CMD_AO_ABORT is ignored if the AO overcurrent protection FSM is in an Idle state.	
x	0	1	1	1	0	0	0	0	0	0	0	1	0	0	X	CMD_AO_ABORT_HIZ: Abort the running AO overcurrent protection FSM after a detected overcurrent in VO or CO mode. CMD_AO_ABORT_HIZ: Exit the AO overcurrent FSM after clearing the sticky status for AO overcurrent, AO_SHRT_S, and AO_OVRLOAD_S and resetting user programmed AO_MODE to HIZ (overwrite the AO_MODE field of SPI register to HiZ). Then go to Idle state. CMD_AO_ABORT_HIZ is ignored if the AO overcurrent protection FSM is in an idle state.	***CMD_AO_ABORT_HIZ***
x	0	1	1	1	0	0	0	0	0	0	0	1	0	1	X	CMD_CISW_ABORT: Abort the running CISW input overcurrent protection FSM after a detected overcurrent on CISW input. CMD_CISW_ABORT: Exit the CISW overcurrent protection FSM after clearing the overcurrent sticky status bits CISW_SHRT_S and CISW_OVRLOAD_S, disengaging CISW current limiter and overwriting CISW_ON bit register to 1. Then go to Idle state. CMD_CISW_ABORT is ignored if the CISW overcurrent protection FSM is in an Idle state.	***CMD_CISW_ABORT***
x	0	1	1	1	0	0	0	0	0	0	0	1	1	0	X	CMD_CISW_ABORT_HIZ: Abort the CISW input overcurrent protection FSM after triggered by an overcurrent detection on CISW input. CMD_CISW_ABORT_HIZ: Exit the CISW overcurrent protection FSM after clearing the overcurrent sticky status CISW_SHRT_S and CISW_OVRLOAD_S, overwriting, and overwriting the user-programmed CISW switch control (AIO_CONFIG.CISW_ON) configuration to open the switch. Then go to Idle state. CMD_CISW_ABORT_HIZ is ignored if the CISW overcurrent protection FSM is in an idle state.	***CMD_CISW_ABORT_HIZ***
X	0	1	1	1	0	0	0	0	0			Command future expansion					
x	1	1	1	1	0	0	0x20-0xFF									DAC0 subsystem's register read via SPI	
x	0	1	1	1	0	0	0x20-0xFF									DAC0 subsystem's register write via SPI	

7.7.4 SPI byte-wise write command

The second bit after the first SPI bit frame RW_L is 0, indicating that it is a write transaction. A SPI write command helps configure the internal registers of the chip. The register values are updated every eighth clock cycle with a byte of data starting from the MSB. A minimum of eight SCLKs are required to write the first byte of data in a multibyte register. For example, to update the first MSB-byte (bit 23:16) of the register that has 24-bit data width and bits 15 to 0 retain the old value of the register, eight SCLKs are required. The example below shows the host partial write value 0xA5 to bit 23 to bit 16 of register 0x0010.

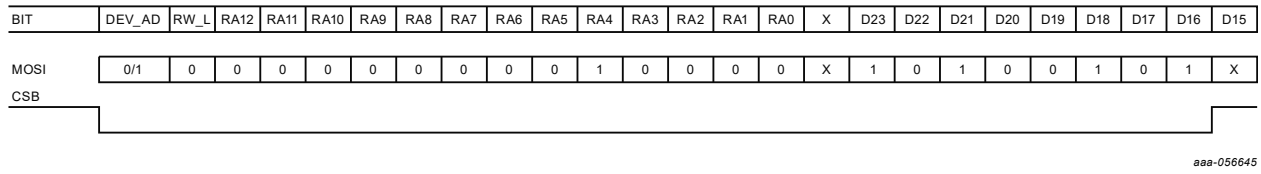


Figure 15. SPI register byte-wise write timing diagram

7.7.5 Register write with CRC enabled

Figure 16 and Figure 17 show host writes 16-bit and 24-bit internal register respectively. There are two CRC bytes sent from a host named CRC-2. The first CRC byte is calculated by the host from the first 16-bit data word, which includes device ID bit, RWL bit, RA bits, and do not care bit (0). The second CRC byte is calculated from the 16-bit WDATA[15:0] or WDATA[23:0] if the host writes to the 16-bit register or 24-bit register, respectively. There is always an extra empty byte (eight extra SCLKs) required to send after the second CRC byte. The device needs extra clocks to check/verify with the on-chip CRC logic if the data sent by the host is not corrupted. After the CRC byte is received and a match is found with the device-calculated CRC, then the register update will take place. The controller can decide to drive an extra seven more clock cycles to receive the calculated CRC data from the device or it can terminate the SPI frame by deasserting the CSB to high without affecting the register being updated.

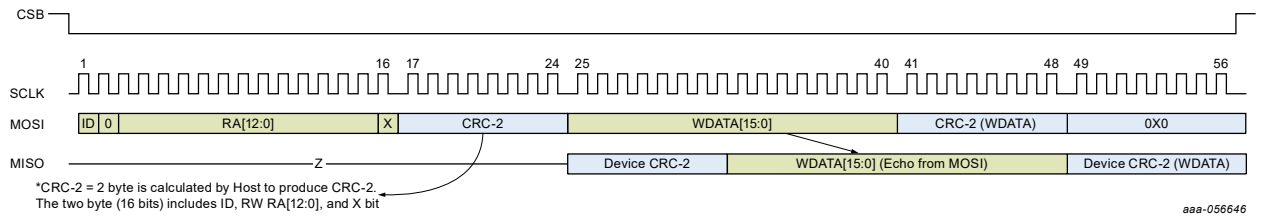


Figure 16. Host writes to register 16-bit with CRC enabled

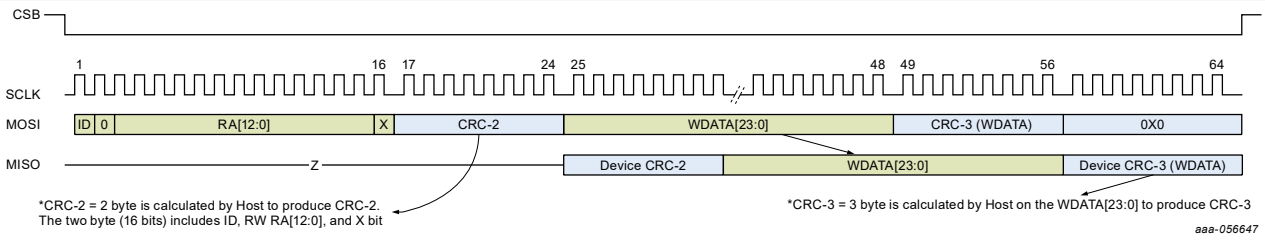


Figure 17. Host writes to register 24-bit with CRC enabled

7.7.6 DAC conversion timing

The DAC needs a minimum of 18 system clocks of wait time between the last SCLK edge and CSB/SYNDAC. However, it depends on which one is used to and is high at the end of the SPI frame. The time is specified as TDAC_wait in the EC table and violation of it leads to erroneous output (voltage or current) at pin AO.

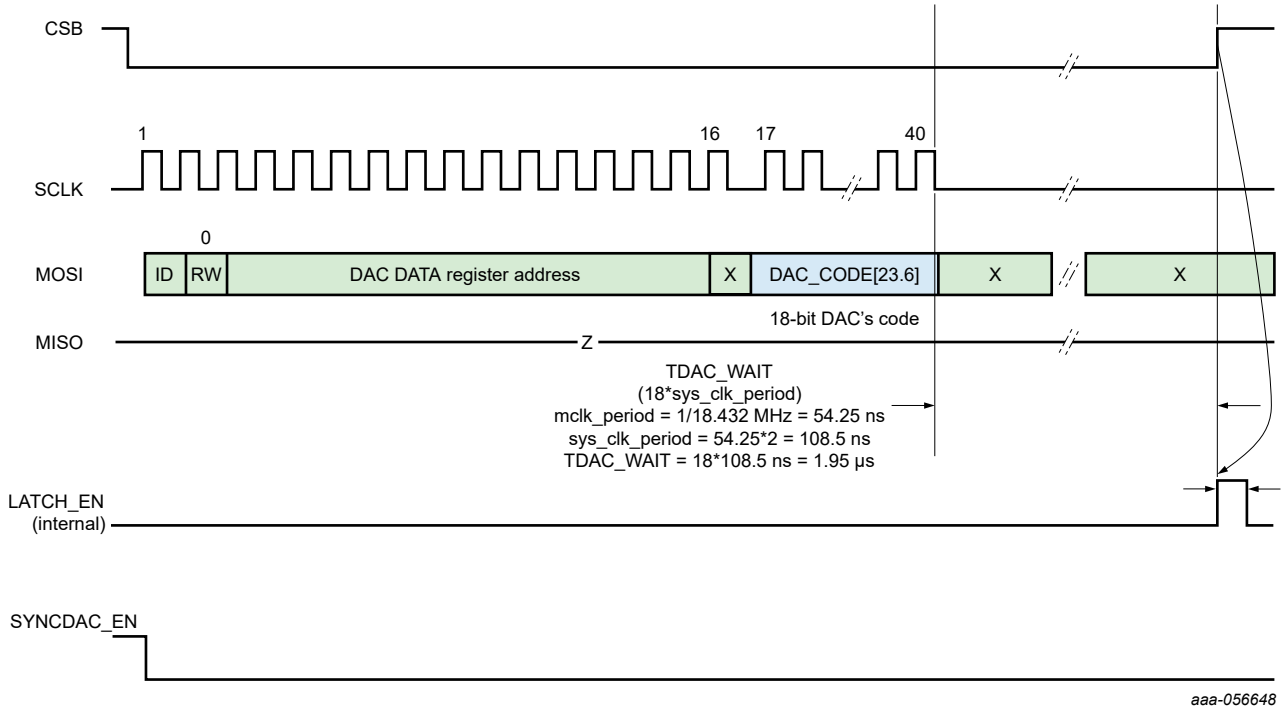


Figure 18. DAC AO_data write timing with CSB

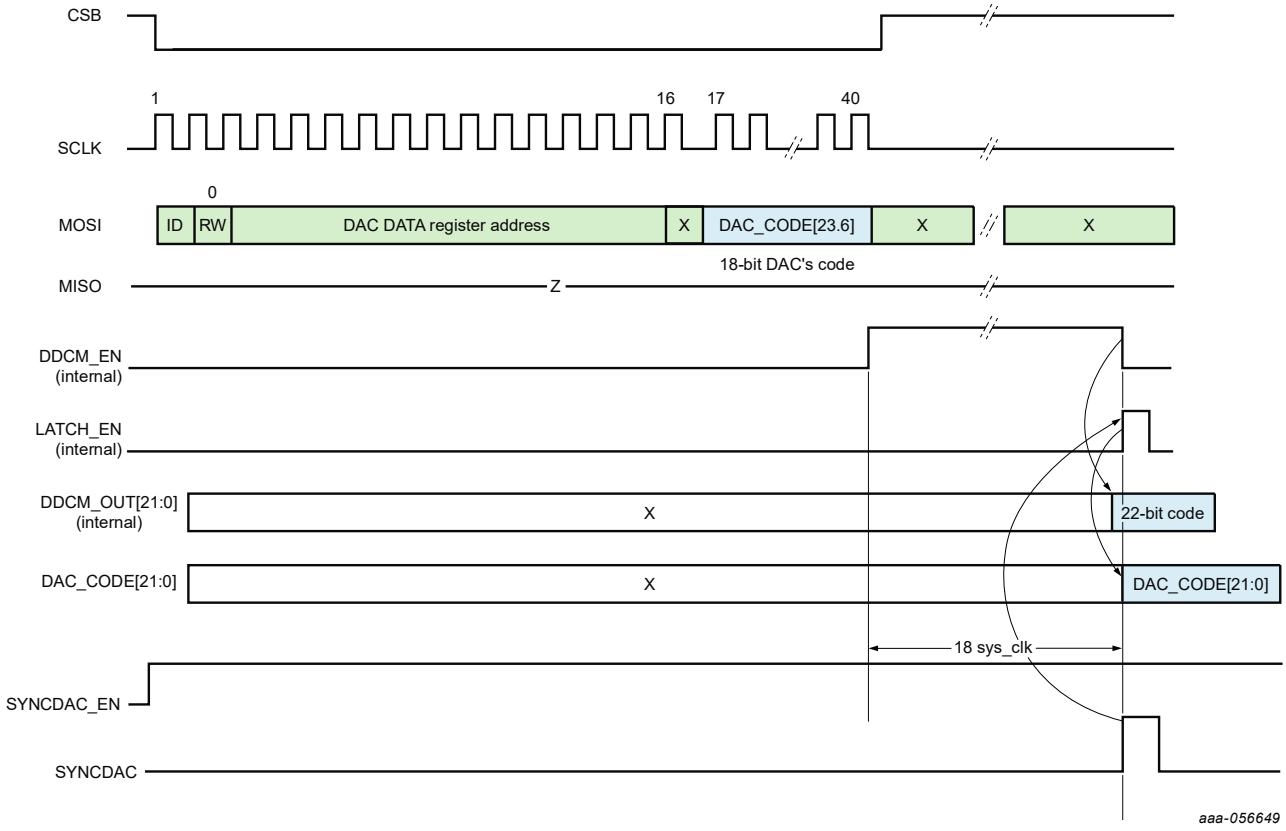


Figure 19. DAC AO_data write timing with SYNCDAC

7.7.7 CRC

CRC-8 generator

The NAFE33350 provides assurance of the integrity of the data communication. It can append 8-bit CRC data after the data transfers or revives. The CRC_EN is bit 7 in the SYS_CONFIG0 register, and its default 0 means CRC_EN is off. The following polynomial is always used in this chip:

$y = x^8 + x^2 + x + 1$ equivalent to the binary number is 100000111.

The CRC byte is an error detection byte that detects communication errors to and from the host and device. The CRC byte is the division remainder of the payload data of the CRC polynomial in which the polynomial function is $X^8 + X^2 + X + 1$. The 9-bit binary coefficients are: 100000111b. The payload data are either 2 bytes or 3 bytes depending on the data transfer operation.

When CRC is enabled, the CRC byte only appends after the 16-bit command (2 bytes).

16-bit command byte: The host computes the CRC over the 16-bit command byte and appends the CRC to the command on the third byte. The device performs the CRC calculation and compares the result to the CRC byte transmitted by the host. If the host and the device CRC values match, the command executes. Otherwise, the command does not execute, and the device asserts a CRC interrupt by pulling the INTB pin to the ground.

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is next to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is next to the leftmost Logic 1 of the new result. The procedure is repeated until the new result is less than the polynomial.

7.8 Thermal shutdown

The AO-AFE includes a thermal shutdown circuit to protect the device for overtemperature. If the temperature exceeds 145 °C, the thermal shutdown circuit asserts the global alarm for warning purposes. If the temperature exceeds 165 °C, the thermal shutdown turns off the chip for protection purposes.

7.9 Monitoring with global alarm

The AO-AFE provides a flexible and configurable global alarm to allow the user to configure it based on the specific application and need.

For device and input monitoring, various alarms and interrupts are available including programmable alarm thresholds for (1) temperature alarm, (2) channel-based overrange, and underrange alarms.

The GLOBAL_ALRM_STICKY determines the alarm-clearing behavior. If configured STICKY, clear the alarm bit by writing 1 to the bit position. If not cleared, the STICKY alarm does not respond to events anymore. Alarm bit changes as per the live event in NON-STICKY mode.

Table 20. Alarm and interrupt

GLOBAL ALARM ENABLE 0x32\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 °C.
	14	Reserved			Unused
	13	Reserved			Unused
	12	Reserved			Unused
	11	Reserved			Unused
	10	GPI_POS_ALRM	RW	0x0	Enables an alarm for rising edge detected at any of the GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enables an alarm for falling edge detected at any of the GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enables an alarm for registering a configuration error.
	7	Reserved			Unused
	6	Reserved			Unused
	5	Reserved			Unused
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enables an alarm when the XTAL or EXTCLK frequency varies with internal CLK by 20 %.
	3	PGA_OV_ALRM	RW	0x0	Enables an alarm when one or more data channels are overvoltage stressing the PGA.
	2	AO_OV_ALRM	RW	0x0	Enables an alarm when the AO voltage source is overloaded.
	1	AO_OI_ALRM	RW	0x0	Enables an alarm when AO current source is overloaded.
	0	TEMP_ALRM	RW	0x0	Enables a programmable temperature alarm, the triggering threshold is set in THRS_TEMP register bits.
GLOBAL ALARM INTERRUPT 0x33\h	15	OVER_TEMP_INT	RW	0x0	Flag asserts when DUT temp goes above 145C.
	14	Reserved			Unused
	13	Reserved			Unused
	12	Reserved			Unused
	11	Reserved	RW	0x0	Unused
	10	GPI_POS_INT	RW	0x0	Flag asserts when a rising edge is detected at any of the GPI pins.
	9	GPI_NEG_INT	RW	0x0	Flag asserts when a falling edge is detected at any of the GPI pins.
	8	CONFIG_ERROR_INT	RW	0x0	Flag asserts when configuration error detected.
	7	Reserved			Unused
	6	Reserved			Unused
	5	Reserved			Unused
	4	EXTCLK_FREQ_INT	RW	0x0	Flag asserts when the XTAL or EXTCLK frequency varies with internal CLK by 20 %.
	3	Reserved			Unused
	2	AO_OV_INT	RW	0x0	Flag asserts when AO voltage output is overloaded.
	1	AO_OI_INT	RW	0x0	Flag asserts when AO current output is overloaded.
	0	TEMP_INT	RW	0x0	Flag asserts if NAFE TS detects a temperature above the programmed threshold in register bits THRS_TEMP.

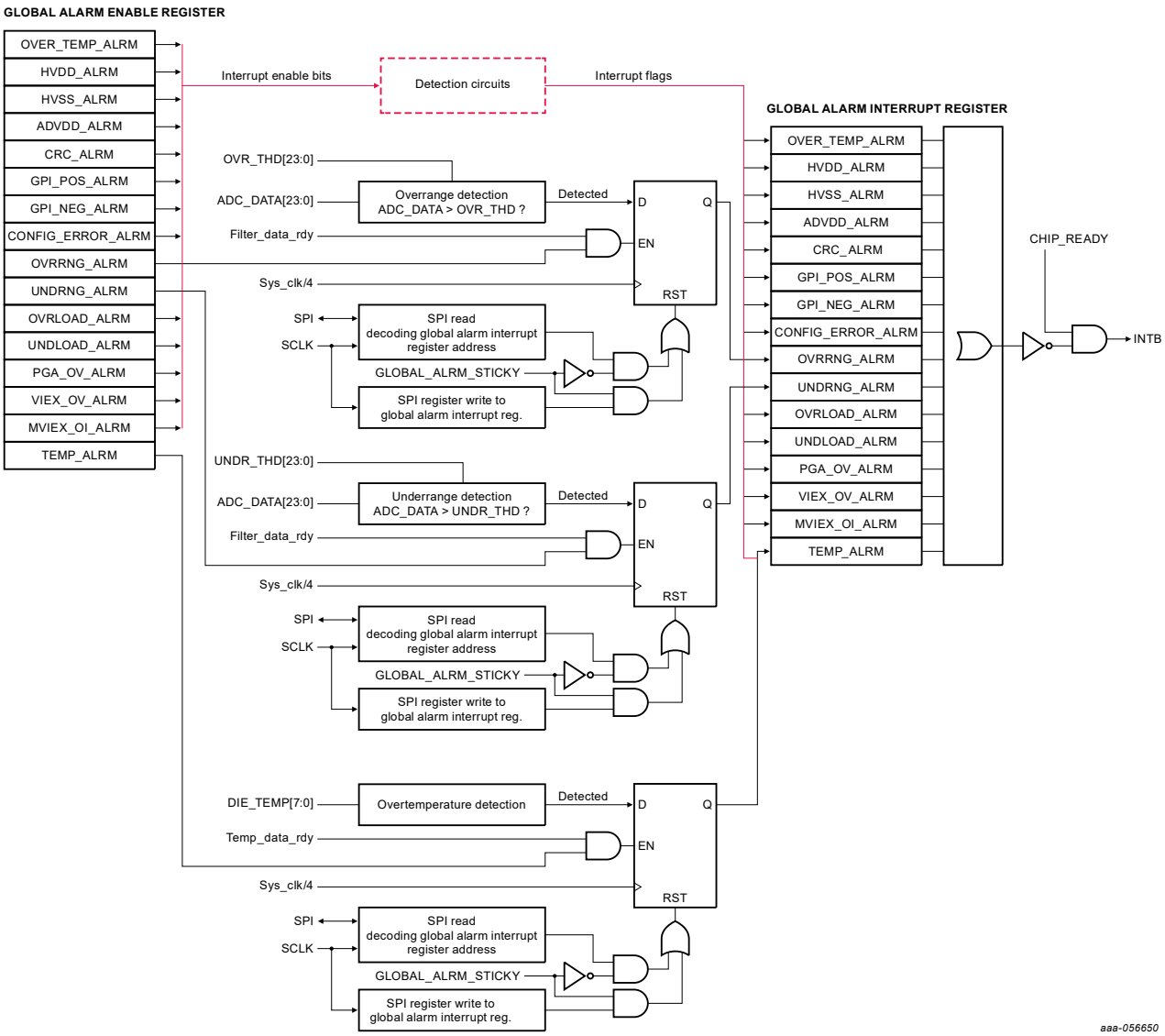


Figure 20. Alarm

Note: *The ADC-related alarms are available only in super set device NAFE33352 or NAFE93352.*

7.9.1 Interrupts

The INTB pin of the chip is a NOR function of the internal 15 bit of global alarm interrupt registers. Each of these global alarm interrupt register bits can be written 1 or 0, respectively, to enable or disable the SPI's register write command to global alarm enable register (Address = 0x2E\h).

Note: *Using SPI write to enable all the CH_DATA readback could be prepended with a channel-specific status byte by enabling STATUS_EN, each of the status bits is ORs of all 15 channels.*

The logic equivalence is shown in Figure 21.

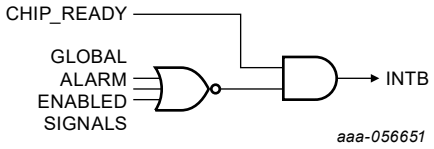


Figure 21. Interrupt

Each individual status bit is concatenated in a single byte listed in Table 21.

Table 21. Status byte description

Status bit function	Representation base		Bit index
	Channel	Global	
Not used	Not used		Not used
Not used	X		6
Not used	X		5
VIEX_OV_ALRM or VIEX_OI_ALRM	X		4
Not used	X		3
Current die temperature over user set threshold		X	2
Clock alarm error		X	1
Result of 3-bit logical OR of HVDD_ALRM, HVSS_ALRM, and HVDD_ALRM signals		X	0

These status bits behave independently of the SYS_CONFIG.3 state. They behave depending on what CMD_xy was issued:

Command CMD_SS: Status becomes sticky until the host initiates another conversion, then the status updates accordingly. The host can clear this channel base status by issuing CMD_CLEAR_DATA or CMD_CLEAR_REG.

Global alarm interrupt register (Address 0x2F\h) can be configured as non-sticky or sticky behavior via programing SYS_CONFIG0.3 (bit 3). Programming SYS_CONFIG0.3 = 0, non-sticky, and SYS_CONFIG0.3 = 1, sticky behavior to all 15 bit of global alarm interrupt register (GAI). When the sticky option is selected, the hardware sets each GAI register bit when an interrupt event occurs. This interrupt event occurrence corresponds to each functional bit described in the global alarm interrupt register. If the host again must see the next interrupt event, the host must clear whatever bit is set by writing 1.

Note: *Writing 1 to the bit that is 0 does not alter it to 1.*

7.9.2 Latched and not-latched alarm

When the non-sticky option is selected, the content of the GAI register reflects the current chip or channel conversion status at the time the host reads this register. The functionality of the INTB pin depends on how the host programs the SYS_CONFIG0.3 bit. For example, SYS_CONFIG0.3 = 1, sticky, INTB is deasserted low until all interrupts are clear, whereas SYS_CONFIG0.3 = 0, non-sticky, INTB is low whenever there is an interrupt occurring, and high whenever there is no interrupt at all. INTB can be toggling, meaning interrupt comes and goes regardless if the host keeps reading the GAI register.

The interrupt logic equation is shown below:

$$INTB = \sim\left(\left|glb\_alarm\_intr\_flags\right| \left|reset\_int\_flag\_r\right)$$

Note: *The reset_int_flag_r is set after the POR. It can also be set if a POR glitch has occurred. Then, INTB is asserted low.*

It is recommended that the host reads the SYS_STATUS0 register to see if the CHIP_READY is set before communication to the chip. Upon reading this register, INTB will be clear and deasserted high, waiting for the next interrupt event.

- CRC_ERROR status can now be read via SPI through SYS_STATUS0 register (bit 12) and it is clear on read. The CRC_ERROR flag can also be routed out to GPIO2 when SYS_CONFIG0 bit 0 is set to 1. GPIO2 now has dual functions: when SYS_CONFIG0.0 = 0: general-purpose I/O and when SYS_CONFIG0.0 = 1: CRC_ERROR flag output.

7.10 Channel-based configuration

The AO-AFE has:

- Configurable analog output
- Digital GPIOs (two can take analog inputs)
- On-chip scaled reference voltages for built-in self-test (BIST) functions

7.11 Use of factory-calibrated coefficients

The AO-AFE part is supplemented with factory-calibrated coefficients (CAL). The coefficients are calibrated at the NXP factory and stored in the non-volatile memory. Each gain and offset coefficient is a full 20-bit.

To use the factory coefficients, pick the appropriate coefficient pointer in the CH_CONFIG registers.

Table 22. Factory calibration

Pointer	Gain register	ADDR\h	Offset register	ADDR\h	NVM stored coefficient and setting
0	GAIN_COEF0[23:0]	50	OFFSET_ COEF0[23:0]	58	Voltage output, single-ended, measured at AO-GND
1	GAIN_COEF1[23:0]	51	OFFSET_ COEF1[23:0]	59	Current Output, Rs = 50 Ω, singled-ended, measured at AO-GND
2	GAIN_COEF2[23:0]	52	OFFSET_ COEF2[23:0]	5A	Available for the user
3	GAIN_COEF3[23:0]	53	OFFSET_ COEF3[23:0]	5B	Available for the user
4	GAIN_COEF4[23:0]	54	OFFSET_ COEF4[23:0]	5C	Available for the user
5	GAIN_COEF5[23:0]	55	OFFSET_ COEF5[23:0]	5D	Available for the user
6	GAIN_COEF6[23:0]	56	OFFSET_ COEF6[23:0]	5E	Available for the user
7	GAIN_COEF7[23:0]	57	OFFSET_ COEF7[23:0]	5F	Available for the user

7.12 GPIOs

The GPIO control and data registers are organized by 4x10 bits register.

- GPI_DATA (0x23\h): Read (R) only register. It detects a level logic from the pad.
- GPIO_CONFIG0 (0x24\h): Read/write (R/W) GPO_EN register. It enables an output path.
- GPIO_ CONFIG1(0x25\h): R/W GPIO_CON register. It connects the internal I/O to the pad.
- GPIO_CONFIG2 (0x26\h): R/W GPI_ENABLE. It enables the input path to allow reading data from the pad, looping back from GPO_DATA register and, or GPIO edges detection.

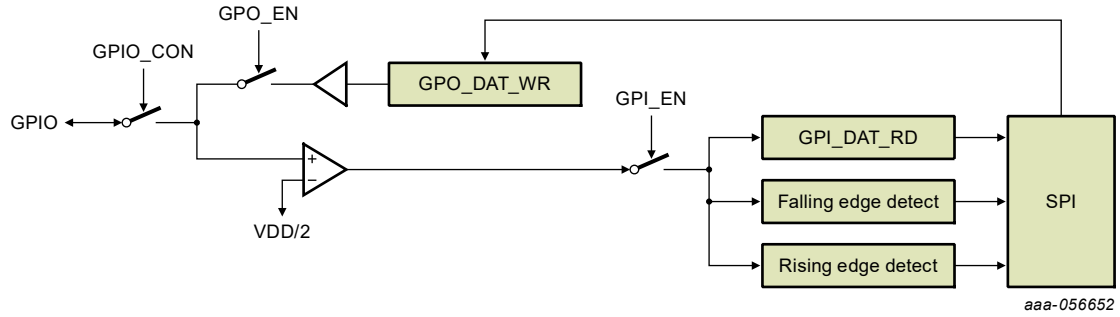


Figure 22. GPIO structure

While GPI_EN = 1 and GPIO_CON = 1, any transition from 0 ≥ 1 (positive edge) or 1 ≥ 0 (negative edge) sets the edge-detection register (GPI_EDGE_POS at 0x27 and GPI_EDGE_NEG at 0x28) to 1. This register is defined as sticky by nature and requires the host to clear it by writing 1 to the bit that is set to 1.

7.13 Chip reset

The AO-AFE has two types of reset mode: Chip POR and Command RESET.

When in reset, all HV-input pins, GPIO pins are in High-Z input mode and internal voltage reference is used. All user registers are set to their default values and the OTP shadow register content is reloaded. The input clock source defaults back to an internal RC oscillator.

Command CMD_RESET is the same as a hardware reset.

Command CMD_CLEAR_REG operates similarly to a software reset. It clears all user-accessible registers to default values except SYS_CONFIG0.9:8, CK_SRC_SEL[1:0].

Command CMD_RELOAD reloads the stored content from the on-chip non-volatile memory to the shadow register.

7.14 Analog output ranges

DAC code to analog output transfer function:

$$DAC_{code} = -AO_V * \frac{2^N}{5*VREF}$$

$$AO_V = -Code * \frac{5*VREF}{2^N}$$

Here, N is the DAC resolution (Up to 18-bit).

DAC codes span from $-2^{(N-1)}$ to $2^{(N-1)}-1$.

Table 23 reports the case for 18-bit resolution.

Vref = 2.5 V; DAC resolution = 18 bit

Voltage AO FSR = 25 V; AOV resolution ±10 V = 95.36 µV

Current AO FSR = 50 mA; AIV resolution ±20 mA = 190.73 nA

Table 23. 18-bit bipolar range

Voltage target output	Digital code (18-bit)	Voltage output (V)
12.5	131071	-12.499905
10	104858	-10.000038
5	52429	-5.000019

Table 23. 18-bit bipolar range...*continued*

95 µV	1	-0.000095
0	0	0.000000
- 95 µV	-1	0.000095
-5	-52429	5.000019
-10	-104858	10.000038
-12.5	-131072	12.500000
Current target output	**Digital code**	**Current output (A)**
0.025	131071	-0.025000
0.02	104858	-0.020000
0.004	20972	-0.004000
190 nA	1	190 nA
0	0	0.000000
- 190 nA	1	- 190 nA
-0.004	-20972	0.004000
-0.02	-104858	0.020000
-0.025	-131072	0.025000

The user can set the analog output to the unipolar range by setting AIO_CONFIG.UNIPOLAR_AO_MODE = 1\b. The following are the transfer function and ranges:

$LSBV = 25\ V/(2^N)$

AOV = 18.75 - DAC_CODE * LSBV

$LSBI = 0.05\ A/(2^N)$

AOI = 0.0375 - DAC_CODE * LSBI

Table 24. 18-bit unipolar voltage output range

DI decimal	DI HEX 2C	Voltage output (V)
131071	01FFFF	6.250095
117965	01CCCD	7.499981
96993	017AE1	9.500027
55050	00D70A	13.500023
0	000000	18.750000
-39322	036666	22.500038
-70779	02EB85	25.500011
-112722	0247AE	29.500008
-131072	020000	31.250000

Table 25. 18-bit unipolar current output range

DI decimal	DI HEX 2C	Current output (A)
131071	01FFFF	0.012500
117965	01CCCD	0.015000
91750	016666	0.020000

Table 25. 18-bit unipolar current output range...*continued*

DI decimal	DI HEX 2C	Current output (A)
13107	003333	0.035000
0	040000	0.037500
-65536	030000	0.050000
-91750	02999A	0.055000
-117965	023333	0.060000
-131072	020000	0.062500

7.15 Device calibration

The AO-AFE products include 32 user-accessible calibration coefficient registers divided into three groups:

- Gain: GAIN_COEF0[23:0] to GAIN_COEF7[23:0]
- Offset: OFFSET_COEF0[23:0] to OFFSET_COEF7[23:0]
- Extra-CAL COEFF: EXTAR_COEF0[23:0] to EXTRA_COEF7[23:0]

To reduce the calibration error, the bit-width of gain, offset, and self-calibration coefficient registers are 24-bit wide. The DAC uses the 18 MSB of this coefficient.

The user can read and write the above user-calibration coefficients. During device power up or reset, the factory-calibrated coefficients that were stored in non-volatile memory (NVM) are loaded into these registers, if available.

Table 26 describes the calibration coefficient registers.

Table 26. Calibration coefficient registers

Pointer	Gain register	ADDR\h	Offset register	ADDR\h	NVM stored coefficient and setting
0	GAIN_COEF0[23:0]	80	OFFSET_COEF0[23:0]	90	Voltage Output, single-ended, measured at AO-GND
1	GAIN_COEF1[23:0]	81	OFFSET_COEF1[23:0]	91	Current Output, Rs = 50 Ω, single-ended, measured at AO-GND
2	GAIN_COEF2[23:0]	82	OFFSET_COEF2[23:0]	92	
3	GAIN_COEF3[23:0]	83	OFFSET_COEF3[23:0]	93	
4	GAIN_COEF4[23:0]	84	OFFSET_COEF4[23:0]	94	
5	GAIN_COEF5[23:0]	85	OFFSET_COEF5[23:0]	95	
6	GAIN_COEF6[23:0]	86	OFFSET_COEF6[23:0]	96	
7	GAIN_COEF7[23:0]	87	OFFSET_COEF7[23:0]	97	

7.15.1 Offset and gain calibration

The ideal transfer characteristic is

$$y = x$$

The actual transfer characteristic is

$$\boldsymbol{y} = G_a \cdot x + O_a$$

Where Ga and Oa are the actual gain and actual offset respectively.

The calibrated transfer characteristic is

$$\boldsymbol{y} = G_a \cdot G_c \cdot x + G_c \cdot (O_a - O_c)$$

Where Gc and Oc are the correction gain and offset coefficients, respectively.

$$\begin{cases} G_c = \frac{1}{G_a} \\ O_c = O_a \end{cases}$$

7.15.2 DAC digital gain and offset calibration coefficients

Offset calibration registers are 18-bit registers and their values are in two's complement format.

Table 27. Gain and offset coefficients

Analog output - gain coefficients		
Gain calibration coefficient (hexadecimal)	**Gain calibration coefficient (decimal)**	**Gain calibration factor = Gain_coeff./(2^{16})**
03FFFF	262143	3.9999847
020000	131072	2.0000000
010001	65537	1.0000153
010000	65536	1.0000000
00FFFF	65535	0.9999847
008000	32768	0.5000000
000000	0	0.0000000
Analog output - offset voltage		
Offset calibration coefficient (hexadecimal)	**Offset calibration coefficient (decimal)**	**Offset calibration voltage out (V)**
01FFFF	131071	12.4999046
010000	65536	6.2500000
000001	1	0.0000954
000000	0	0.0000000
03FFFF	-1	-0.0000954
030000	-65536	-6.2500000
020000	-131072	-12.5000000
Analog output - offset voltage		
Offset calibration coefficient (hexadecimal)	**Offset calibration coefficient (decimal)**	**Offset calibration voltage out (V)**
01FFFF	65536	24.9998093
010000	1	12.5000000
000001	0	0.0001907
000000	-1	0.0000000
03FFFF	-65536	-0.00019107
030000	-131072	-12.5000000
020000	65536	-25.0000000

8 Limiting values

This section describes the absolute maximum rating and the safe operating area.

8.1 Absolute maximum rating

Table 28 describes the absolute maximum rating for various terminals in NAFE33350.

Table 28. Absolute maximum rating

Description	Min	Max	Units
HVDD to AGND	-0.3	33	V
AGND to HVSS	-0.3	33	V
HVDD to HVSS	-0.3	55	V
AVDD to AGND	-0.3	5.5	V
DVDD to DGND	-0.3	5.5	V
AGND to DGND	-0.3	0.3	V
Screw terminal AO to HVDD (include in series external diodes and sense resistor)	-70	36	V
Screw terminal AO to HVSS, with external diode and series 50 Ω sense resistor	-36	65	V
AI1P, AI1N, Vsense, IsenseP, IsenseN to HVDD include 5 kΩ external current limiting resistor	-70	36	V
AI1P, AI1N, Vsense, IsenseP, IsenseN to HVSS, with external 5 kΩ resistor in series for current limit with a duration of less than one hour	-36	65	V
CISW to HVSS or CISW to HVDD (if internal, the CISW switch is off)	-60	60	V
CISW to GND, when CISW is ON and AFE is functionally operating	-36	36	V
GPIO0... GPIO4 to DGND	-0.3	VDVDD+0.3	V
OSCIN to DGND	-0.3	VDVDD+0.3	V
SCLK, DIN, DOUT, CSB, SYNCDAC, INTB to DGND	-0.3	VDVDD+0.3	V
LDOCAP to DGND	-0.3	2.1	V
REFEXT/REFNR, REFDACBUF to AGND	-0.3	VAVDD+0.3	V
AGNDDACREF to AGND	-0.3	0.3	V
COMPIN, HARTIN to HVVD	—	0.3	V
HVSS to COMPIN, HARTIN	—	0.3	V

8.2 Safe operating area

The safe operating area of the NAFE33350 represents the max power dissipation and maximum ambient temperature allowable to meet the maximum operating junction temperature, Tjmax = 150 °C.

The system designers must design their system not to exceed the maximum operating junction temperature, Tjmax = 150 °C.

The junction temperature is a function of ambient temperature, thermal resistance, and power dissipation as below:

$$Tj = Tamb + Rth*Pdis$$

So, given the package thermal resistance, the Tamb, and Pdis must fit in the safe operating area, as reported in Figure 23.

Example: Tjmax = 150 °C, Rth = 35 °C/W, Pdismax = 1 W

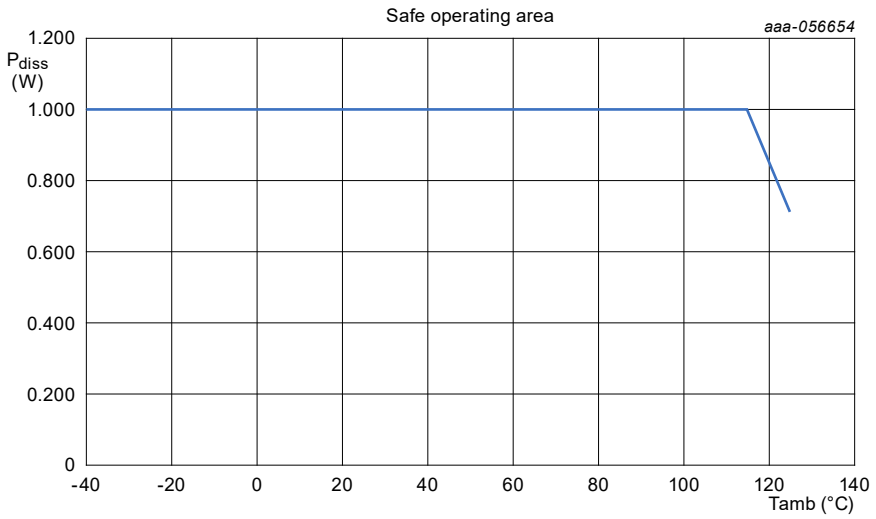


Figure 23. Safe operating area

To increase the safety, NAFE33350 monitors the temperature junction with an integrated temperature sensor and provides an automatic warning alarm when the Tj is over 145 °C.

9 Thermal characteristics

Table 29 provides the thermal characteristics of NAFE33350.

Table 29. Thermal characteristics

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings can cause malfunction or permanent damage to the device.

Description		Symbol	Min	Max	Units
Operating temperature	—	—	—	—	°C
Ambient	—	T_{amb}	-40	125	
Junction	—	Tj	-40	150	
Storage temperature	—	TSTO	-55	150	°C
Peak package reflow temperature	[1] [2]	TPPRT	—	260	°C
Junction to board (bottom exposed pad soldered to board)	[3]	RθJB	—	20	°C/W
Junction to ambient with four-layer board	[4] [5]	RθJA	—	35	°C/W

[1] Pin soldering temperature limit is for a maximum duration of 10 seconds. Not designed for immersion soldering. Exceeding these limits can cause malfunction or permanent damage to the device.

[2] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts and parametric.

[3] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[5] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

10 Electrical specifications

This section describes the analog output and the common system.

10.1 Analog output

Table 30 provides the analog output electrical characteristics of NAFE33350.

Table 30. Analog output electrical characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at T_{amb} = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

Parameter	Symbol	Conditions	Mlin	Typ	Max	Unit
Voltage output range						
Voltage full-scale range	VOUT	±12.5 V full range	—	±12.5	—	V
Voltage linear range	VOUT		-10	—	10	V
Voltage output initial accuracy without calibration						
Total unadjusted error	VTUE	TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error at room temperature	VTUE_Ai	Initial accuracy without CAL coefficients. Internal reference. T_{amb} = 40 °C. AO_TCC = 00\b	—	1.1	1.6	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Internal reference. T_{amb} = -25 °C to 105 °C. AO_TCC = 00\b	—	1.2	1.7	%FS
Offset error	VOFF_Ai	Initial offset error without factory CAL coefficients. Internal reference. T_{amb} = 40 °C. AO_TCC = 00\b	-30	-15	0	mV
Gain error	VGE_Ai	Initial gain error without factory CAL coefficients. Internal reference. T_{amb} = 40 °C. AO_TCC = 00\b	0.5	1.0	1.5	%FS
INL error	VINL_Ai	Initial offset error without factory CAL coefficients. External voltage reference. T_{amb} = 40 °C. AO_TCC = 00\b	-0.3	0.2	0.3	mV
Voltage output initial accuracy with user calibration coefficients						
Total unadjusted error		TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error	VTUE_Auc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = 40 °C.	—	0.0035	0.01	%FS
Total unadjusted error over temperature	VTUE_OTuc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = -25 °C to 105 °C	—	0.02	0.08	%FS
		Initial accuracy with user calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C	—	0.025	0.1	
Calibrated offset error	VOFF_Auc	Initial calibrated offset error with user CAL coefficients. Internal reference, T_{amb} = 40 °C	-0.1	0.025	0.1	mV
Calibrated gain error	VGE_Auc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = 40 °C.	—	0.0013	0.005	%FS
	VGE_OTuc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = -25 °C to 105 °C	—	0.0175	0.07	
		Initial accuracy with user calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C	—	0.02	0.08	
INL error	VINLuc	Initial calibrated INL error with user CAL coefficients. External voltage reference, T_{amb} = 40 °C	-0.3	0.2	0.3	mV
Voltage output initial accuracy with factory calibration coefficients						
Total unadjusted error		TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error	VTUE_Afc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = 40 °C.	—	0.0375	0.15	%FS
Total unadjusted error over temperature	VTUE_OTfc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = -25 °C to 105 °C	—	0.05	0.2	%FS
		Initial accuracy with factory calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C	—	0.055	0.22	
Calibrated offset error	VOFF_Afc	Initial calibrated offset error with applied factory CAL coefficients. Internal reference, T_{amb} = 40 °C	-0.2	0.05	0.2	mV
Calibrated gain error	VGE_Afc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = 40 °C.	—	0.035	0.14	%FS
	VGE_OTfc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. T_{amb} = -25 °C to 105 °C	—	0.0475	0.19	
		Initial accuracy with factory calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C	—	0.0525	0.21	

Table 30. Analog output electrical characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at T_{amb} = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

Parameter	Symbol	Conditions	Mlin	Typ	Max	Unit
Calibrated INL error	VINL_Afc	Initial calibrated INL error with factory CAL coefficients. External voltage reference, T_{amb} = 40 °C	-0.3	0.2	0.3	mV
Voltage output drift over temperature						
Total drift error	VTDE	VTDE [V/V] = (GEv+OE+INL)/FS/(DeltaTemperature)				
Total drift error	VTDE	Internal voltage reference, AO_TCC = 00\b. T_{amb} = -25 °C to 105 °C.	—	2.5	10	ppm/°C
		Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C.	—	2.5	10	
Offset drift	VOFFd	Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C.	-2	0.5	2	µV/°C
Gain drift	VGEd	Internal voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C.	-8	2	8	ppm/°C
Gain drift	VGEd	External voltage reference, AO_TCC = 1x\b. T_{amb} = -40 °C to 125 °C.	-2	0.5	2	ppm/°C
Gain drift over time(2)	VGEd1khr	External voltage reference, AI_TCC = 1x\b. T_{amb} = 125 °C.	—	50	—	ppm/1000h
		Internal voltage reference, AI_TCC = 00\b. T_{amb} = 125 °C.	—	1000	—	ppm/1000h
INL drift	VINLd	External voltage reference, AO_TCC = 00\b. T_{amb} = -40 °C to 125 °C.	-0.5	0.125	0.5	µV/°C
Voltage output						
Voltage headroom		HVDD-AOx	2	—	—	V
Voltage footroom		AOx-HVSS	2	—	—	V
Short-circuit current threshold		Detection time < 5 µs	—	±60	—	mA
Short-circuit current limiter		Programmable timer = 10 µs to 100 µs	±65	—	±80	mA
Overload-circuit current threshold		Detection time < 5 µs	±25	—	—	mA
Overload-circuit current threshold		Detection time < 5 µs (default)	±5	—	—	mA
Overload-circuit current limiter		Timer = 1 ms to 10 ms/ ∞. Programmable within the operating current range	-25	±5	25	mA
Load resistor		Delta Vout criteria	1	100	—	kΩ
Capacitive load stability		RL = 1 MΩ with external compensation capacitor 15 pF. Settling time (HS 10 µs, 0.1 %)	—	—	20	nF
		RL = 1 kΩ with external compensation capacitor 15 pF. Settling time (HS 10 µs, 0.1 %)	—	—	20	nF
		RL = 1 kΩ with external compensation capacitor 100 pF. Settling time (HS 1 ms, 0.1 %)	—	—	2	µF
DC output impedance		Voltage output enabled, VOUT = ±10 V, IOUT = 0-20 10 mA	—	0.01	—	Ω
		Output disabled DIS1 (AOMODE = 0, VSA ON)	—	10	—	MΩ
		Voltage output disabled DIS2 (AOMODE = 0, VSA OFF and AO connected to VSA)	—	150	—	kΩ
ILEAK		Voltage output disabled. High-Z	—	1	—	nA
DC PSRR_HV		Vout 0 V, HVDD/HVSS = ±7 V to ±24 V, AVDD = 3.3 V	—	10	—	µV/V
DC PSRR_LV		Vout 0 V, HVDD/HVSS = ±15 V, AVDD = 3 V to 3.6 V	—	10	—	µV/V
Input impedance VSENSE		No output load, VSA = ON, ±10 V	—	1000	—	MΩ
Current output range						
Output current full-scale range	IOUT	±25.0 mA full range	—	±25.0	—	mA
Output current linear range	IOUT	±25.0 mA full range	-20	—	20	mA
Current output initial accuracy without calibration						
Total unadjusted error		ITUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error at room temperature	ITUE_Ai	Initial accuracy without CAL coefficients. Internal reference. AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = 40 °C.	—	0.5	1.00	%FS
Total unadjusted error over temperature	ITUE_OTi	Initial accuracy without CAL coefficients. Internal reference. AO_TCC= 01\b. External Rsense = 50 Ω. T_{amb} = -25 °C to 105 °C.	—	0.6	1.10	%FS
Offset error	IOFF_Ai	Initial offset error without factory CAL coefficients. Internal reference, T_{amb} = 25 °C. External Rsense = 50 Ω.	-70	-30	10	µA
Gain error	IGE_Ai	Initial gain error without factory CAL coefficients. Internal reference, T_{amb} = 25 °C. External Rsense = 50 Ω	0.0	1.0	2.0	%FS
INL error	IINL_Ai	Initial INL error without factory CAL coefficients. External reference, T_{amb} = 40 °C. AO_TCC = 01\b. External Rsense = 50 Ω.	-0.6	0.4	0.6	µA

Table 30. Analog output electrical characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at T_{amb} = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

Parameter	Symbol	Conditions	Mlin	Typ	Max	Unit
Current output initial accuracy with user calibration coefficients						
Total unadjusted error	ITUE	ITUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error	ITUE_Auc	Initial accuracy with user calibration. AO_TCC = 01\b, External Rsense = 50 Ω. T_{amb} = 40 °C.	—	0.0025	0.01	%FS
Total unadjusted error over temperature	ITUE_OTuc	Initial accuracy with user calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -25 °C to 105 °C.	—	0.02	0.08	%FS
		Initial accuracy with user calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -40 °C to 125 °C.	—	0.025	0.1	
Calibrated offset error	IOFF_Auc	Initial calibrated offset error with user CAL coefficients. Internal reference, external Rsense = 50 Ω. T_{amb} = 40 °C.	-0.5	0	0.5	µA
Calibrated gain error	IGE_Auc	Initial calibrated gain error with user calibration coefficients. AO_TCC = 01\b, external Rsense = 50 Ω. T_{amb} = 40 °C.	-0.0035	-0.0015	0.0005	%FS
	IGE_OTuc	Initial calibrated gain error with user calibration coefficients at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -25 °C to 105 °C.	—	0.0175	0.07	
		Initial calibrated gain error with user calibration at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -40 °C to 125 °C.	—	0.02	0.08	
INL error	IINL_Auc	Initial calibrated INL error with user CAL coefficients. External voltage reference, T_{amb} = 40 °C. External Rsense = 50 Ω	-0.6	0.4	0.6	µA
Current output initial accuracy with factory calibration coefficients						
Total unadjusted error	ITUE	ITUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error	ITUE_Afc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 01\b, external Rsense = 50 Ω. T_{amb} = 40 °C.	—	0.0375	0.15	%FS
Total unadjusted error over temperature	ITUE_OTfc	Initial accuracy with factory calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -25 °C to 105 °C.	—	0.05	0.2	%FS
		Initial accuracy with factory calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -40 °C to 125 °C.	—	0.055	0.22	
Calibrated offset error	IOFF_Afc	Initial calibrated offset error with factory CAL coefficients. Internal voltage reference, External Rsense = 50 Ω. T_{amb} = 40 °C.	-1.75	0.15	1.75	µA
Calibrated gain error	IGE_Afc	Initial calibrated gain error with factory calibration coefficients. Internal voltage reference, AO_TCC=01\b, External Rsense = 50 Ω. T_{amb} = 40 °C.	-0.14	0.035	0.14	%FS
	IGE_OTfc	Initial calibrated gain error with factory calibration coefficients at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -25 °C to 105 °C.	-0.19	0.0475	0.19	
		Initial calibrated gain error with factory calibration at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. T_{amb} = -40 °C to 125 °C.	-0.21	0.0525	0.21	
Calibrated INL error	IINL_Afc	Initial calibrated INL error with factory CAL coefficients. External voltage reference, AO_TCC = 11\b. External Rsense = 50 Ω. T_{amb} = 40 °C.	-0.6	0.4	0.6	µA
Current output drift over temperature						
TUE drift		ITDE [A/A] = (GEa+OE+INL)/FS/DeltaTemp				
TUE drift	ITDE	Internal voltage reference, T_{amb} = -25 °C to 105 °C. AO_TCC = 01\b. External Rsense = 50 Ω	—	2.5	10	ppm/°C
		Internal voltage reference, T_{amb} = -40 °C to 125 °C. AO_TCC = 01\b. External Rsense = 50 Ω	—	2.5	10	
Offset drift	IOFFd	Internal voltage reference, T_{amb} = -40 °C to 125 °C. AO_TCC = 01\b. External Rsense = 50 Ω	-4	1	4	nA/°C
Gain drift	IGEd	Internal voltage reference, T_{amb} = -40 °C to 125 °C. AO_TCC = 01\b. External Rsense = 50 Ω	-8	2	8	ppm/°C
	IGEd	External voltage reference, T_{amb} = -40 °C to 125 °C. AO_TCC = 02\b. External Rsense = 50 Ω	-2	0.5	2	ppm/°C
INL drift	IINLd	External voltage reference, T_{amb} = -40 °C to 125 °C. AO_TCC = 11\b. External Rsense = 50 Ω	-0.4	0.1	0.4	nA/°C
Current output						
Output voltage headroom		(HVDD-AOx), gain error < 0.1 % with 20 mA.	1.5	1.1	—	V
Output voltage footroom		(AOx-HVSS), gain error < 0.1 % with -20 mA.	1.5	1.1	—	V
Load resistor		±20 mA and HVDD and HVSS set to meet the voltage headroom and footroom.	0	—	750	Ω
Inductive load stability		RL = 1 MΩ with external compensation capacitor 15 pF. (HS settling time 20 µs, 0.1 %)	—	—	200	nH
		RL = 1 kΩ with external compensation capacitor 15 pF. (HS Settling time 20 µs, 0.1 %)	—	—	200	nH

Table 30. Analog output electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at T_{amb} = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

Parameter	Symbol	Conditions	Mlin	Typ	Max	Unit
		RL = 1 kΩ with external compensation capacitor 100 pF. (LP Settling time 100 µs, 0.1 %)	—	—	100	µH
ILEAK		Output disabled	—	1	—	nA
DC PSRR_HV		Iout = 0 mA, HVDD/HVSS = ±7 V to ±24 V, AVDD = 3.3 V	—	0.1	—	µA/V
DC PSRR_LV		Iout = 0 mA, HVDD/HVSS = ±15 V, AVDD = 3.0 V to 3.6 V	—	0.1	—	µA/V
Input impedance ISENSE P, N		No output load, Common mode, Rext = 50 Ω	—	250	—	kΩ

10.2 Common system

Table 31 provides the common system EC characteristics of NAFE33350.

Table 31. Common system EC table

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at T_{amb} = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature sensor						
Temperature sensor resolution		Die temperature	—	1/64	—	°C
Temperature sensor accuracy		Die temperature	—	±3	—	°C
Internal voltage reference						
Output voltage	VREF	Internal reference, REF_INT		2.496		V
Initial accuracy		T_{amb} = 40 °C with internal reference	-0.5		0.5	%
Temperature coefficient	TCVREF	T_{amb} = -25 °C to 105 °C	—	±4	±10	ppm/°C
		T_{amb} = -40 °C to 125 °C	—	±6	±15	
Long-term stability(2)	LTS		—	1000	—	ppm over 1000h
Load regulation		0.1 mA sourcing and sinking current load	—	1	—	mV/mA
Supply regulation	SVREF	3 V ≤ VAVDD ≤ 3.6 V, T_{amb} = 40 °C	—	10	—	µV/V
DACREFBUF						
Load regulation		0.5 mA sourcing and sinking current load	—	10	—	µV/mA
Supply regulation	SVREF	3 V ≤ VAVDD ≤ 3.6 V, T_{amb} = 40 °C	—	10	—	µV/V
Power supplies						
High-voltage supply	VHV	VHVDD - VHVSS	14		—	V
Positive high-voltage supply	VHVDD	Referenced to AGND	7	15	—	V
Negative high-voltage supply	VHVSS	Referenced to AGND	-32	-15	—	V
Low-supply voltage	VVDD	VDD = VAVDD = VDVDD. Referenced to AGND	2.97	3.30	—	V
Low-voltage supply quiescent current	IVDD	Current output mode 0 mA (PA_ON = 1, VSA_ON = 1, CSA_ON = 1, CISW_ON = 0) VSENSE_pin = 0 V, HVDD = -HVSS = 15 V, AVDD = DVDD = 3.3 V, AO_SYSCFG.AO_ON = 0xb11, all other settings are POR default.	—	7.2	7.8	mA
High-voltage quiescent current	IHVDD		—	2.4	2.6	mA
High-voltage quiescent current	IHVSS		—	2.3	2.5	mA
Total quiescent power			—	95	103	mW
Digital I/Os						
Logic HIGH input voltage	VIH		0.7*VDVDD	—	—	V
Logic LOW input voltage	VIL		—	—	0.3*VDVDD	V
Input voltage hysteresis			—	0.3	—	V
Logic HIGH output voltage	VOH	IOH = 3 mA	0.8*VDVDD	—	—	V
Logic LOW output voltage	VOL	IOL = -3 mA	—	—	0.2*VDVDD	V
Oscillators						
Clock frequency accuracy		Internal oscillator -40 °C to 125 °C	—	0.2	1.1	%
Clock frequency Accuracy		Internal oscillator -25 °C to 105 °C	—	0.2	0.9	%
Input clock duty cycle		External clock applied to OSCIN pin. Frequency = 18.432 MHz	45	50	55	%
Oscillator input startup time	SUT OSCIN	18.432 MHz	—	50	—	µS

10.3 SPI timing specification

Table 32 provides the SPI timing specification details for NAFE33350.

Table 32. SPI timing specification

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at T_{amb} = 40 ºC, unless otherwise stated.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Serial interface						
SCLK frequency	f_{SCLK}	—	—	8	32	MHz
SCLK high-pulse width	t_{SCLK_H}	—	14.5	—	—	ns
SCLK low-pulse width	t_{SCLK_L}	—	14.5	—	—	ns
COTI setup time	t_{IS}	Time to SCLK falling edge	5	—	—	ns
COTI hold time	t_{IH}	Time after SCLK falling edge	5	—	—	ns
CITO transition time	t_{OT}	Time after SCLK rising edge	—	10.5	15	nA
CSB high pulse width	t_{CWH}	CSB high pulse width	32	—	—	ns
CSB falling setup time	t_{CFS}	Time before SCLK first rising edge	5	—	25	ns
CSB rising setup time	t_{CRS}	Time before SCLK rising edge	5	—	25	ns
DAC conversion wait time	t_{DAC_WAIT}	Required delay wait time from last falling edge of SCLK to the rising edge of CSB pin when SYNDAC_EN = 0. Required delay wait time from last falling edge of SCLK to the rising edge of SYNDAC pin when SYNDAC_EN = 1.	18	—	—	# of sys clock
SYNCDAC pulse width	$t_{SYNCDAC\_PW}$	SYNCDAC signal pulse width with SYNCDAC_EN = 1	2	—	—	# of sys clock

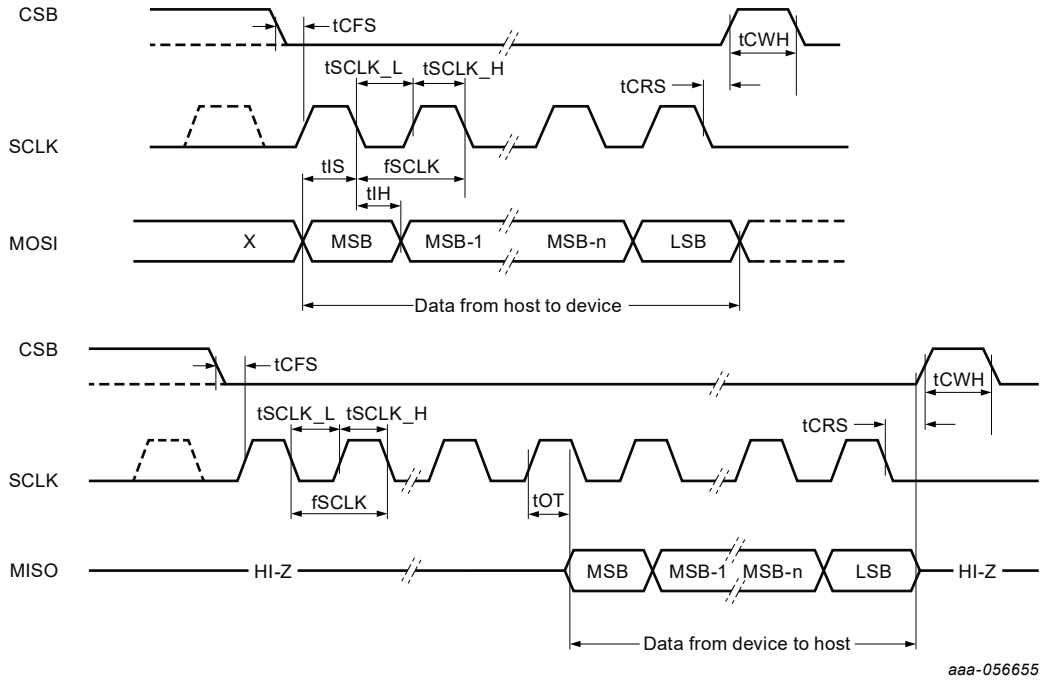


Figure 24. SPI timing

Table 33. Internal LDO output for digital core

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LDO regulation		2.97 V < VDVDD < 3.63 V, 1 µF bypass cap	—	15	—	mV/V

Table 34. CISW internal resistor

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On-resistance initial error	IE_RON	T_{amb} = -40 °C. I = 2 mA	—	200	—	Ω
On-resistance over temp	OVT_RON	T_{amb} = -25 °C to 105 °C. I = ±22 mA	185	—	215	Ω
On-resistance over temp	OVT_RON	T_{amb} = -40 °C to 125 °C. I = ±22 mA	180	—	220	Ω
On-resistance linear error	LE_RON	T_{amb} = 40 °C. I = ±22 mA	—	0.3	—	Ω/mA
On-resistance non-linear error	NLE_RON	T_{amb} = 40 °C. I = ±22 mA	—	±2	—	Ω
On-resistance linear error	LED_RON	T_{amb} = -40 °C to 125 °C. I = ±22 mA	—	0.2	TBD	Ω/mA/C
On-resistance non-linear error	NLED_ RON	T_{amb} = -40 °C to = 125 °C. I = ±22 mA	—	±0.02	TBD	Ω/C
Over current threshold - low to high	—	—	—	35	—	mA
Over current threshold - high to low	—	—	—	30	—	
Current limiter settling	—	—	—	20	—	mA
Current limiter settling time	—	—	—	30	—	µS
Iq CISW	—	—	—	10	—	µA

Table 35. Reliability stress

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Post-stress VREF voltage drift	HAST	With Pre-Con, 130 ºC/85 % RH up to 384 hours with higher power supplies	-0.75	—	0.75	%
	TMCL	-65 ºC to 150 ºC temperature cycle at 500 and 1000 cycles read points	-0.75	—	0.75	%
	HTOL	125 ºC with highest supply voltages (±26 V, 3.63 V) up to 2000 hrs	-0.75	—	0.75	%
	Pre-Con	Bake: 125 ºC/24 hr, Soak: 30 ºC/60 % RH/192 hr, Reflow: 260 ºC/3 cyc	-0.75	—	0.75	%
	HTSL	175 ºC up to 600 hours	-0.75	—	0.75	%
Post-stress gain error drift	HAST	With Pre-Con, 130 ºC/85 % RH up to 384 hours with higher power supplies	-0.75	—	0.75	%
	TMCL	-65 ºC to 150 ºC temperature cycle at 500 and 1000 cycles read points	-0.75	—	0.75	%
	HTOL	125 ºC with highest supply voltages (±26 V, 3.63 V) up to 2000 hrs	-0.75	—	0.75	%
	Pre-Con	Bake: 125 ºC/24 hr, Soak: 30 ºC/60 %RH/192 hr, Reflow: 260 ºC/3 cyc	-0.75	—	0.75	%
	HTSL	175 ºC up to 600 hours	-0.75	—	0.75	%

11 Application information

This section described the AO Voltage Output and AO Current Output modes.

11.1 AO Voltage Output mode

Figure 25 shows the AO Voltage Output mode for NAFE33350.

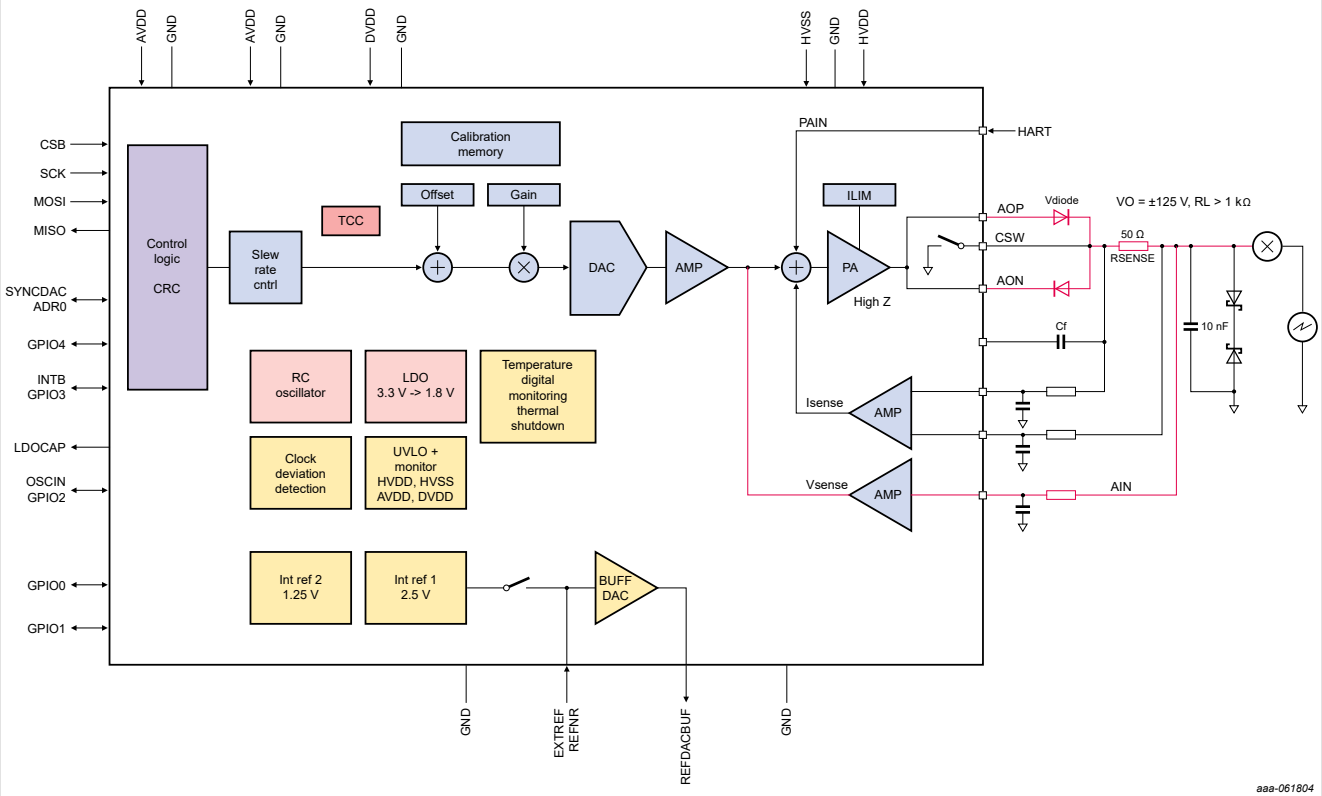


Figure 25. AO Voltage Output mode

11.1.1 Output compliance voltage

The maximum output voltage is defined in Table 30.

The maximum allowable output compliance voltage can be calculated as below:

$$Voutmax = HVDD - HEADROOM - Vdiode - I*RSENSE$$

$$Voutmin = HVSS + HEADROOM + Vdiode + I*RSENSE$$

V_{REF} = 2.5 V with internal reference voltage.

11.2 AO Current Output mode

Figure 26 shows the AO Current Output mode for NAFE33350.

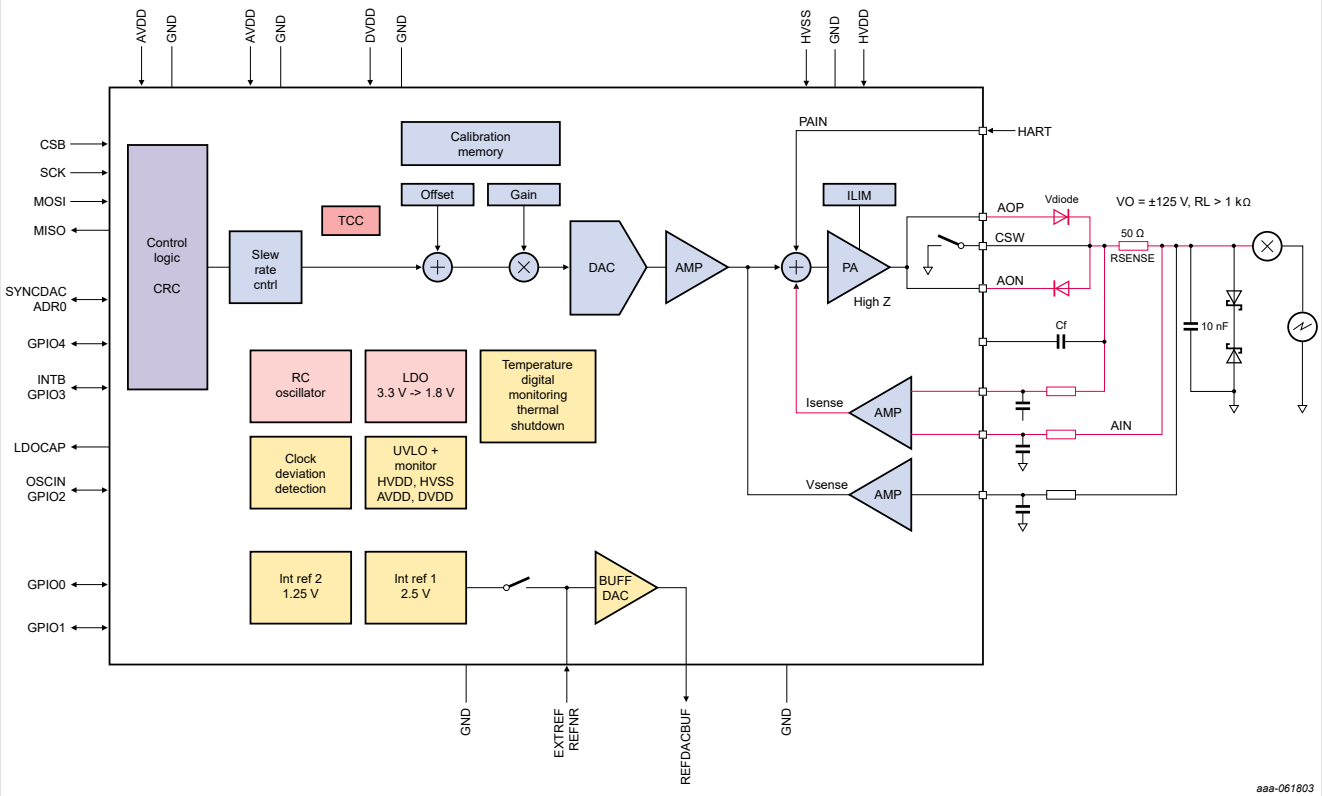


Figure 26. AO Current Output mode

12 Typical operating characteristics

Figure 27 to Figure 46 describe the typical operating characteristics of NAFE33350.

Typical operating characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, T_{amb} = 40 °C, unless otherwise specified.

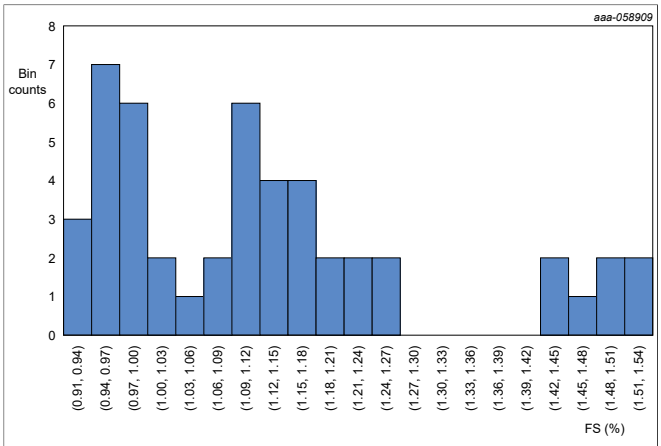


Figure 27. Voltage output uncalibrated TUE

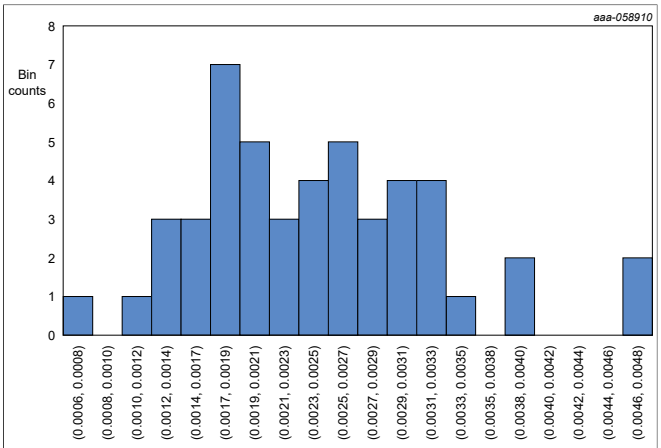


Figure 28. Voltage output user calibrated TUE

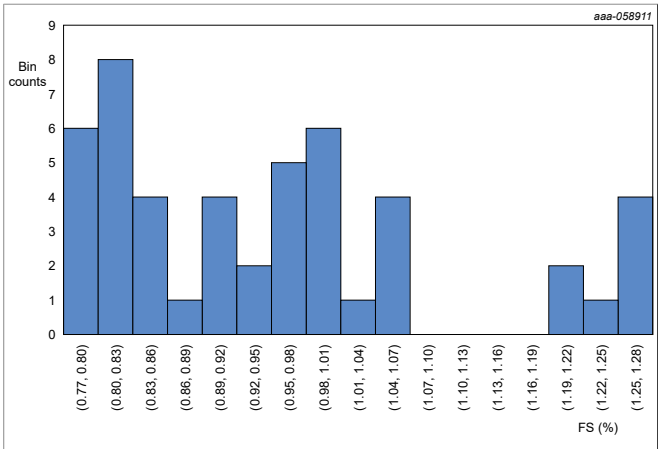


Figure 29. Voltage output uncalibrated gain error

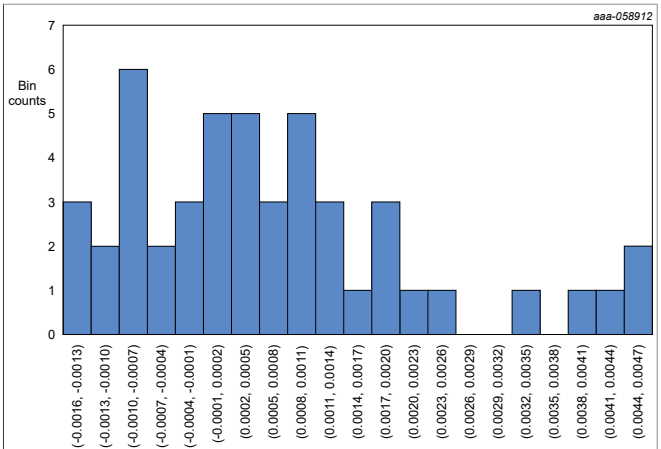


Figure 30. Voltage output user calibrated gain error

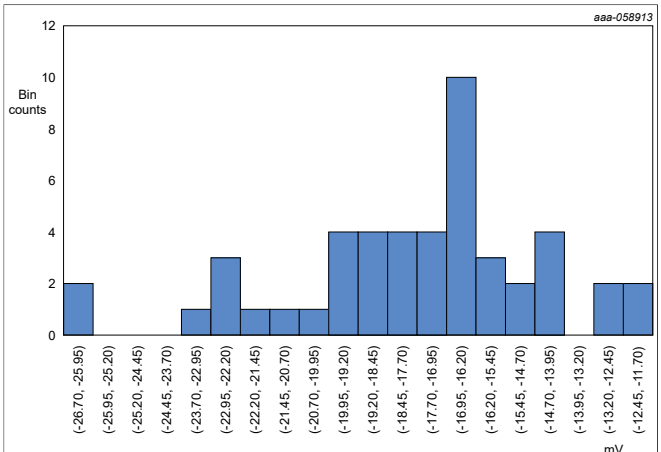


Figure 31. Voltage output uncalibrated offset error

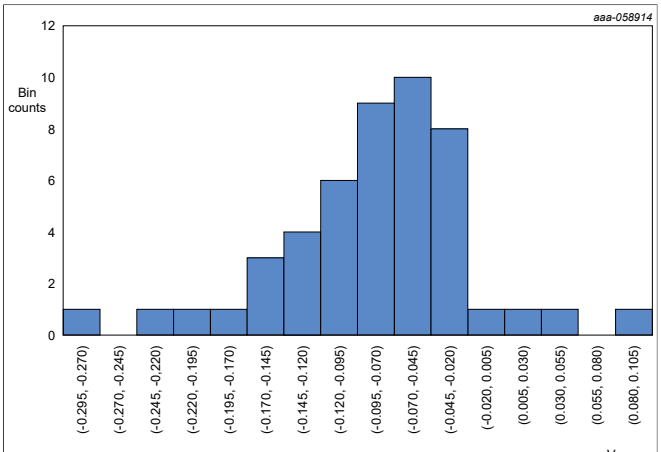


Figure 32. Voltage output user calibrated offset error

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, T_{amb} = 40 °C, unless otherwise specified.

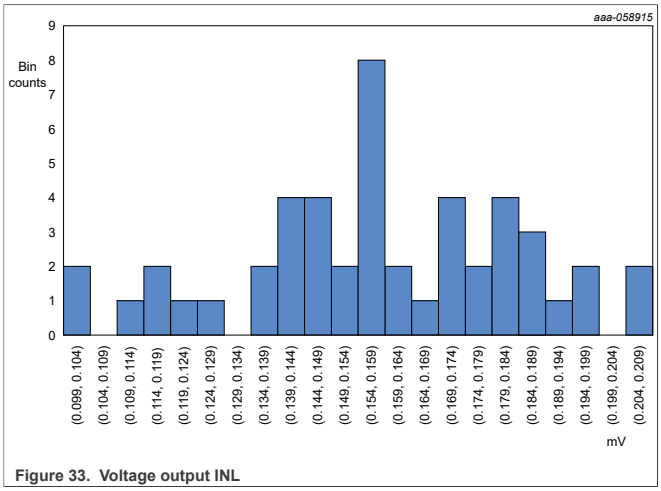


Figure 33. Voltage output INL

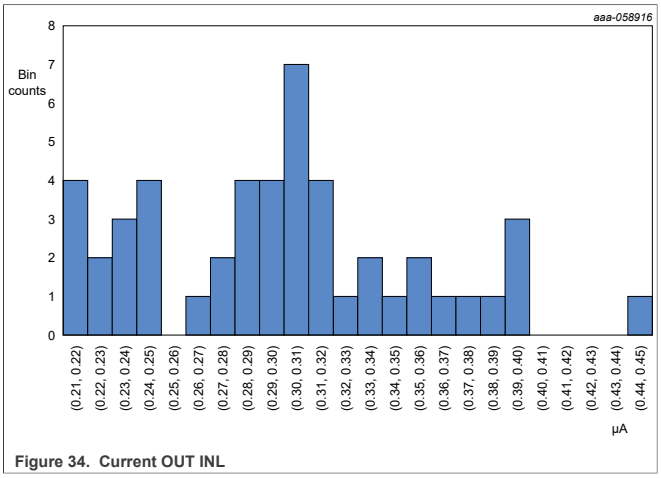


Figure 34. Current OUT INL

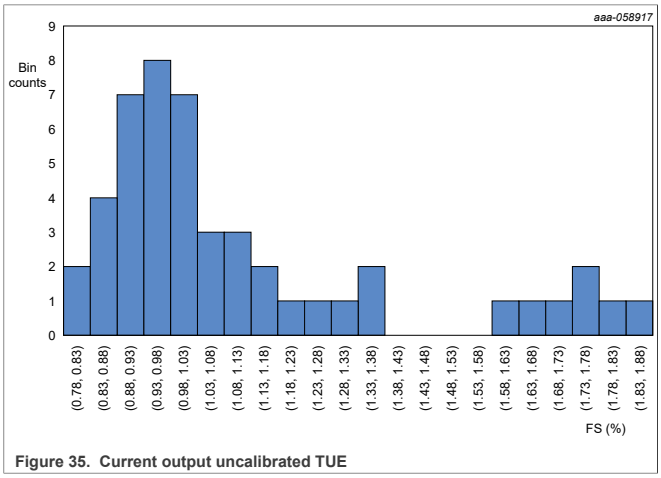


Figure 35. Current output uncalibrated TUE

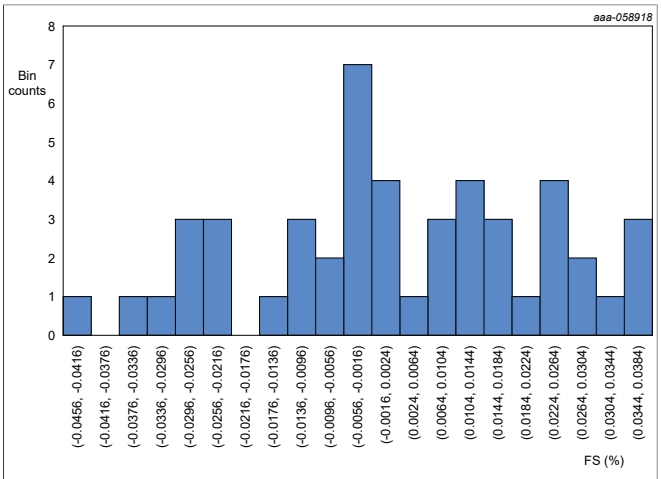


Figure 36. Current output user calibrated TUE

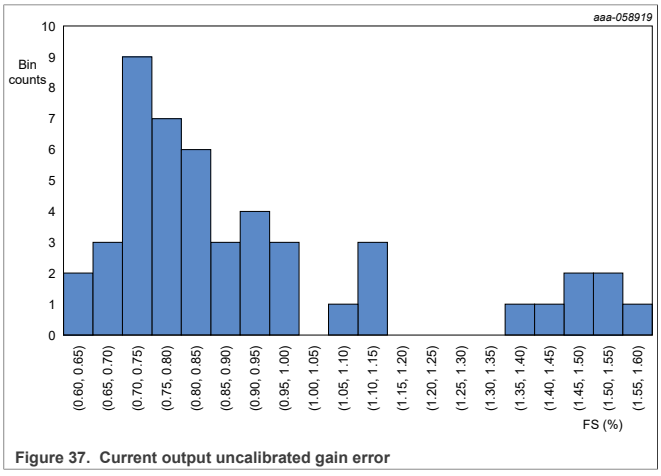


Figure 37. Current output uncalibrated gain error

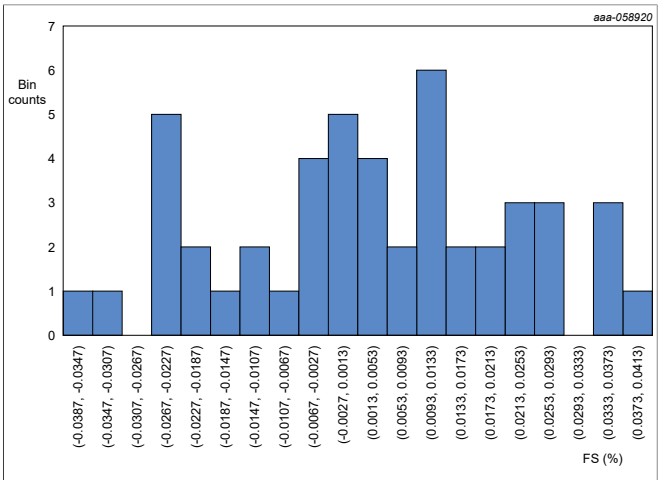


Figure 38. Current output user calibrated gain error

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, T_{amb} = 40 °C, unless otherwise specified.

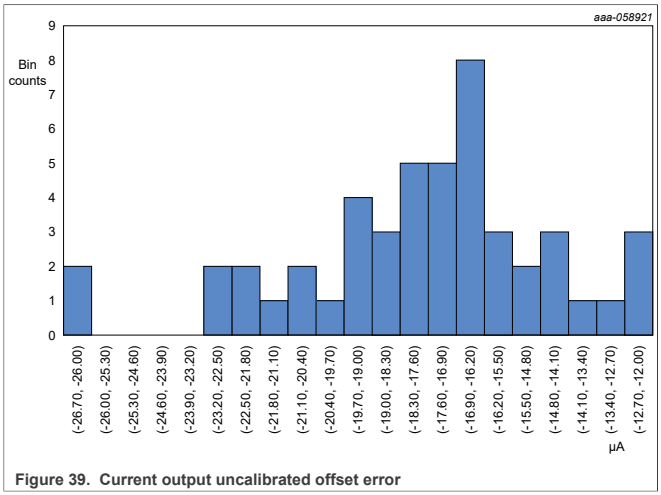


Figure 39. Current output uncalibrated offset error

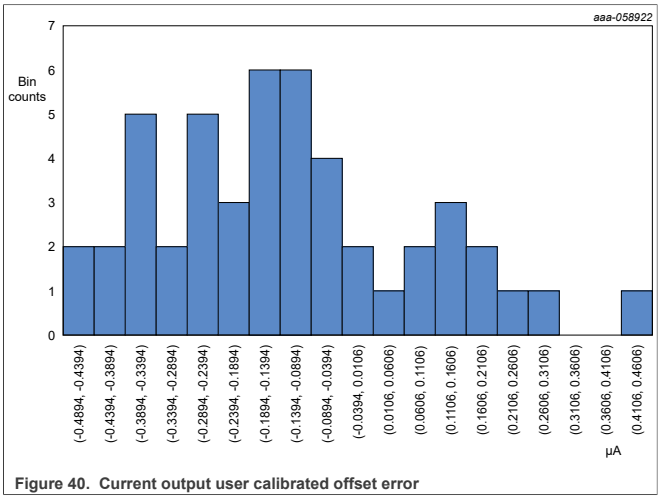


Figure 40. Current output user calibrated offset error

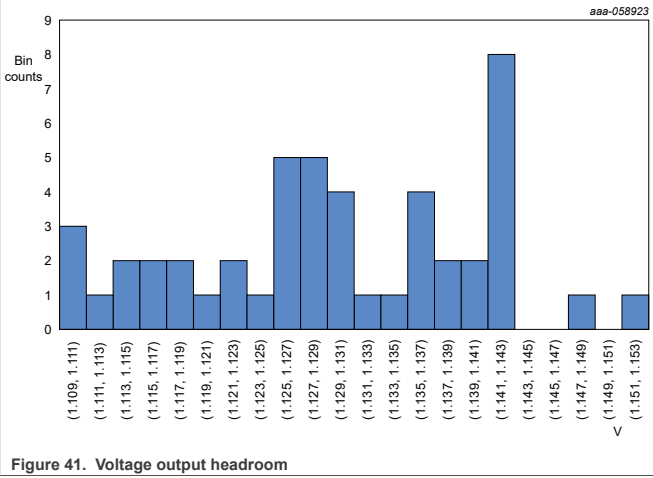


Figure 41. Voltage output headroom

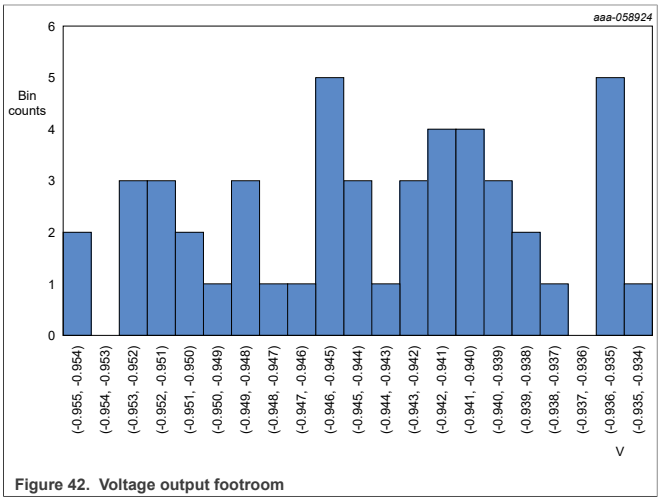


Figure 42. Voltage output footroom

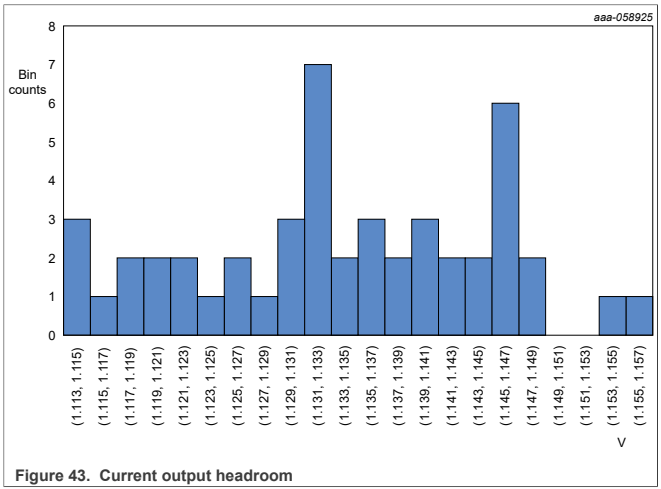


Figure 43. Current output headroom

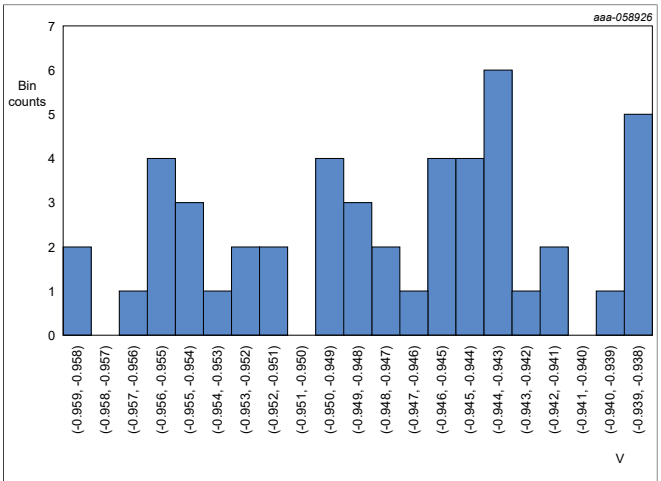


Figure 44. Current output footroom

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, T_{amb} = 40 °C, unless otherwise specified.

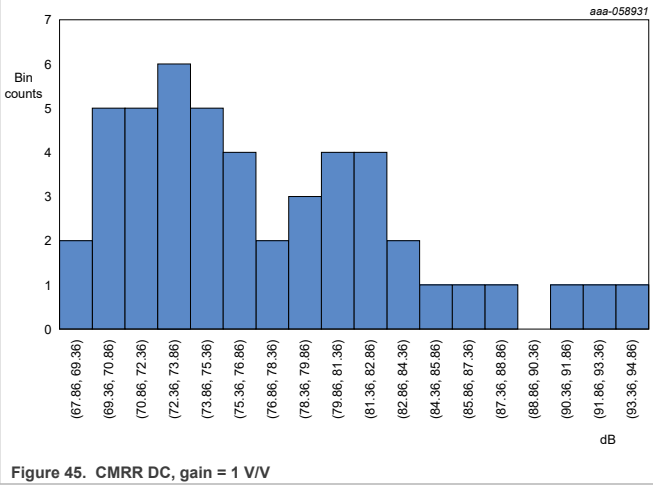


Figure 45. CMRR DC, gain = 1 V/V

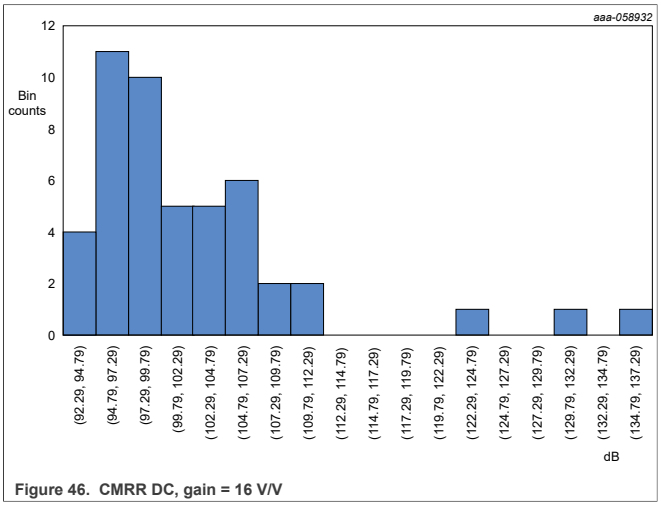


Figure 46. CMRR DC, gain = 16 V/V

13 Package outline

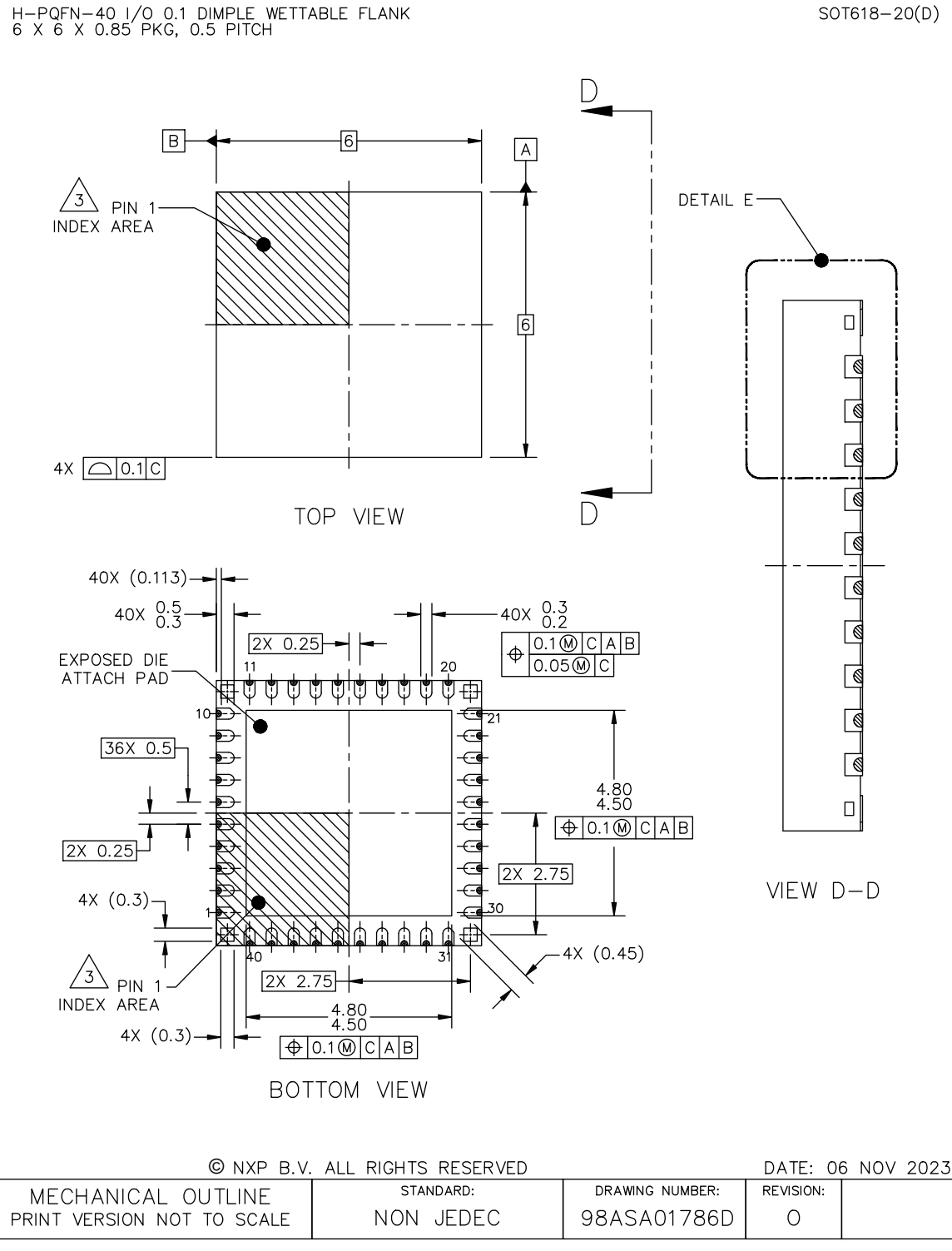
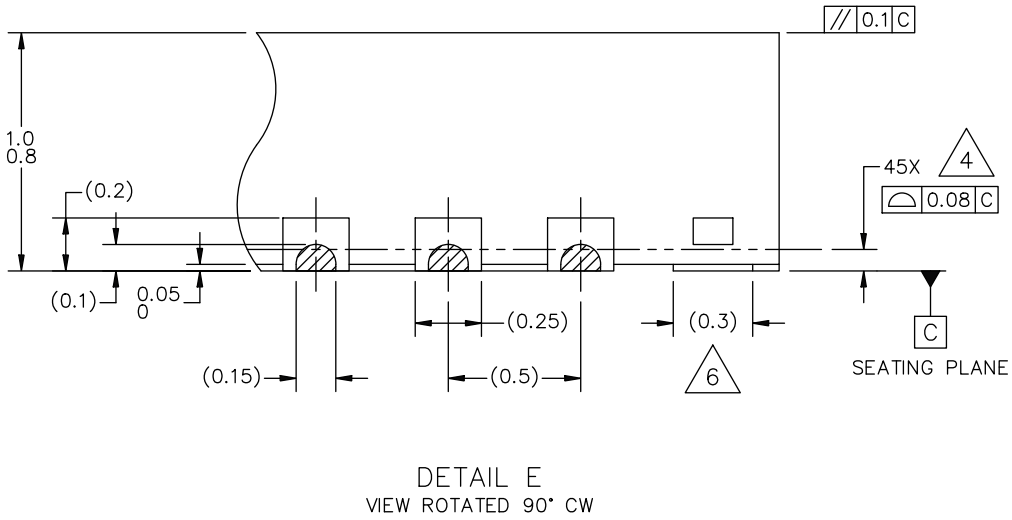


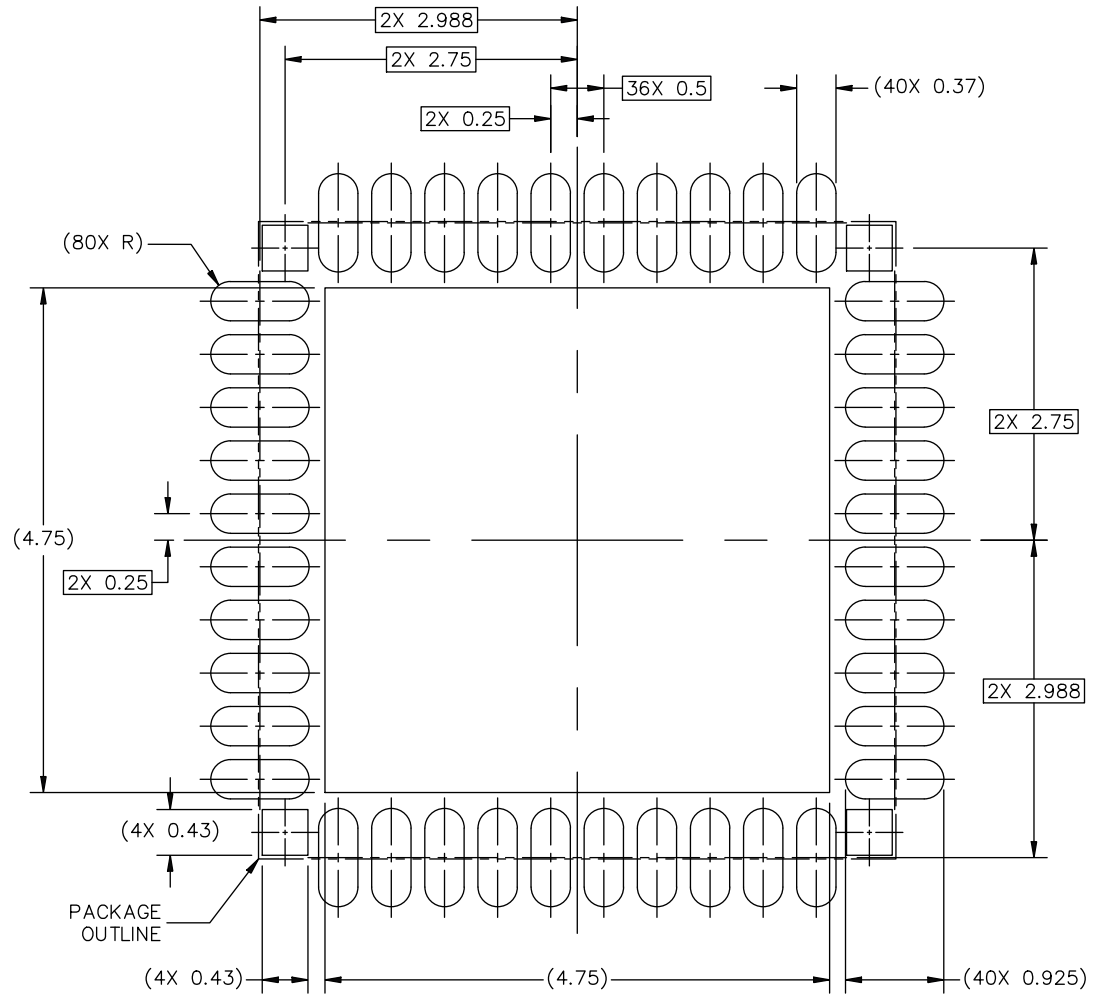
Figure 47. Package outline HVQFN40 (SOT618-20(D))



DATE: 06 NOV 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01786D	REVISION: O	

Figure 48. Package outline detail HVQFN40 (SOT618-20(D))



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 06 NOV 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01786D	REVISION: O	

Figure 49. Reflow soldering footprint part 1 for HVQFN40 (SOT618-20(D))

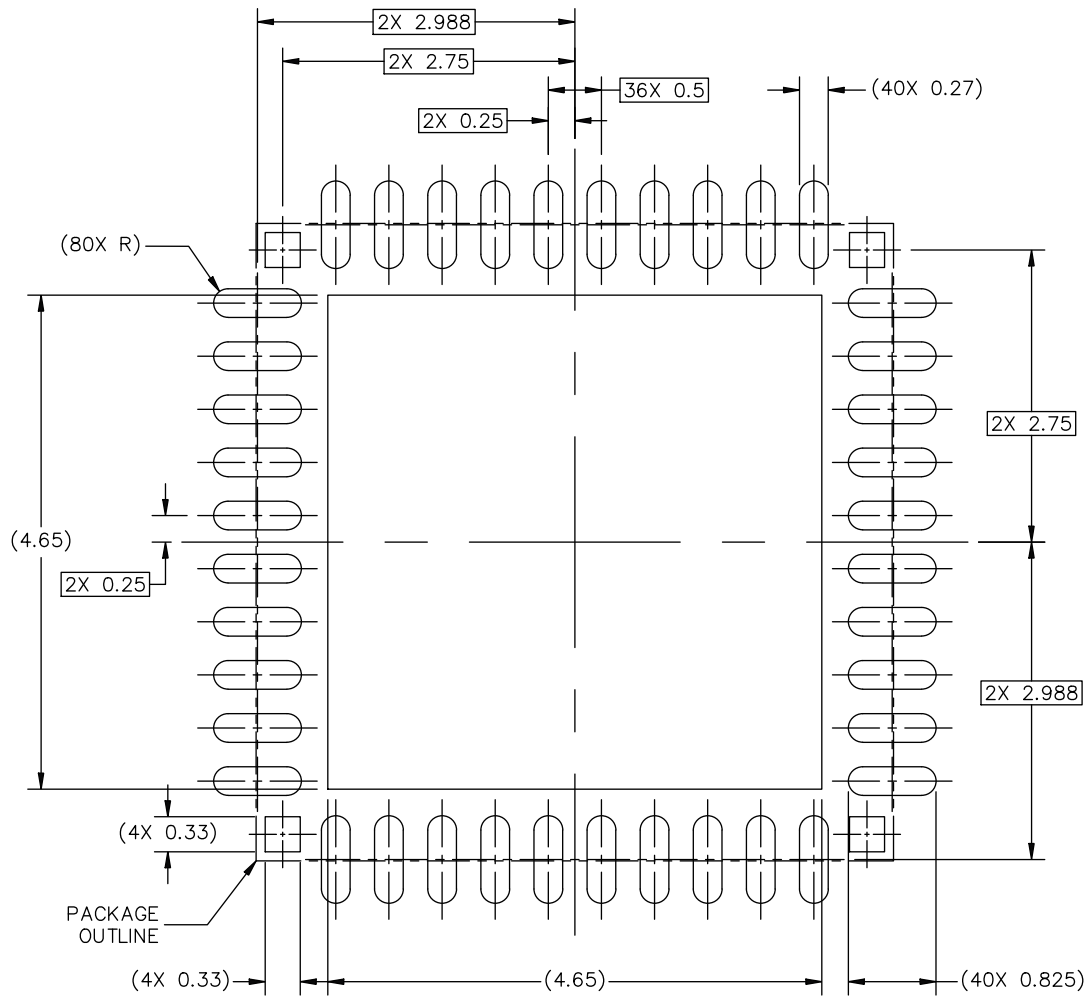


Figure 50. Reflow soldering footprint part 2 for HVQFN40 (SOT618-20(D))

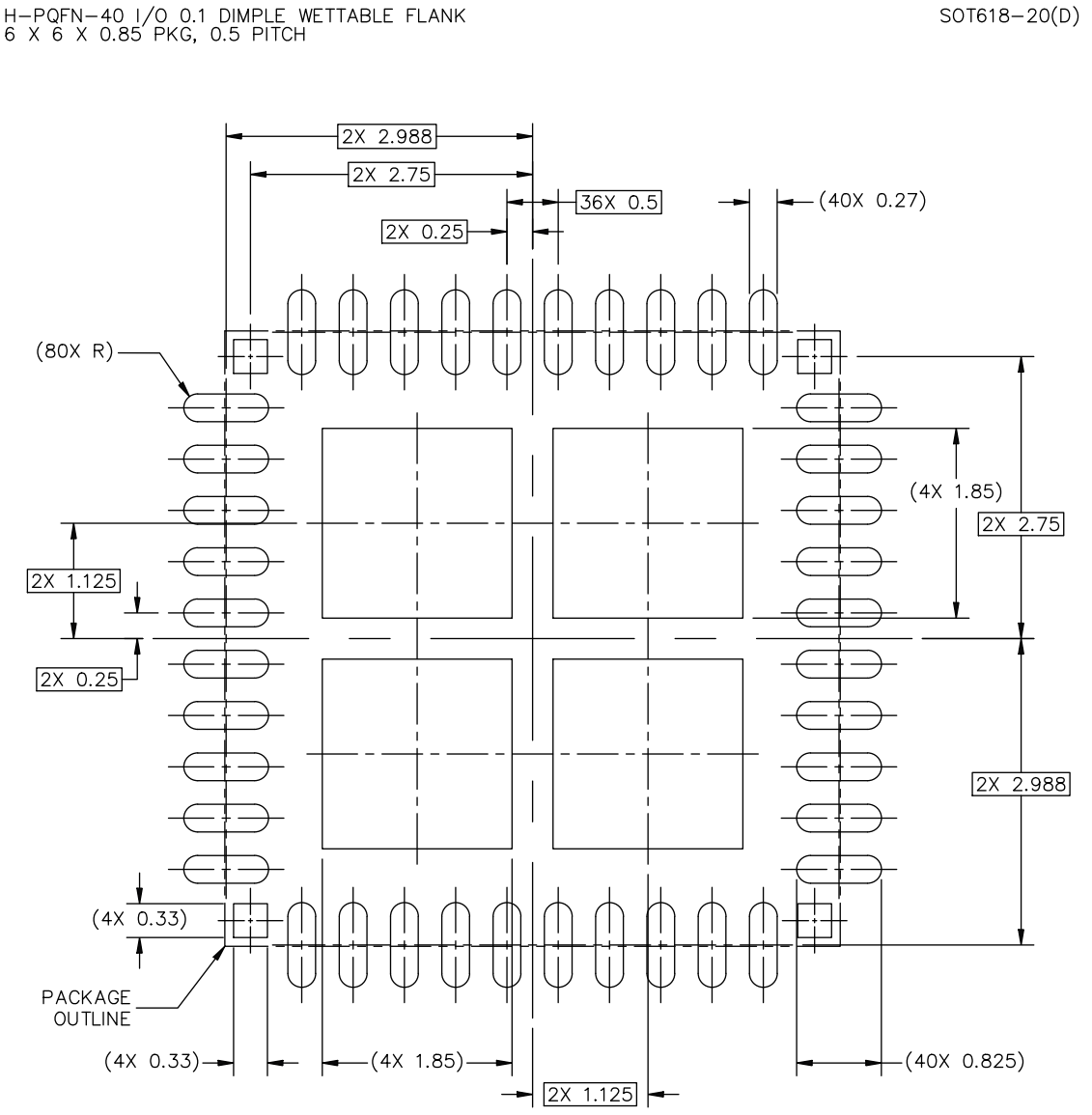


Figure 51. Reflow soldering footprint part 3 for HVQFN40 (SOT618-20(D))

Figure 52. Package outline notes HVQFN40 (SOT618-20(D))

14 Acronyms

Table 36 describes the acronyms used in this datasheet.

Table 36. Acronyms

Acronym	Description
AFE	Analog Front-End
ADC	Analog-to-Digital Converter
AOI	Automated Optical Inspection
AWG	Automatic Wave Generator
BIST	Built-In Self-Test
BSD	Berkeley Software Distribution
CITO	Controller Input Target Output
COTI	Controller Output Target Input
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
EFT	Electrical Fast Transient
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
FSM	Finite State Machine
FSR	Functional Safety Requirement
CL	Capacitive Load
HV	High Voltage
GPIO	General-Purpose Input/Output
GPO	General-Purpose Output
HTOL	High-Temperature Operating Life
LDO	Low-DropOut regulator
RC	Resistor-Capacitor
RH	Relative Humidity
LP	Low Power
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NVM	Non-Volatile Memory
OTP	One Time Programmable
PA	Power Amplifier
PGA	Programmable Gain Amplifier
POR	Power-On Reset
SPI	Serial Peripheral Interface

Table 36. Acronyms...*continued*

Acronym	Description
TRIAMP	TRansImpedance AMPlifier
TVS	Transient Voltage Suppressor
VREF	Voltage REFerence
VSA	Vector Signal Analyzer

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16 Revision history

Table 37 summarizes revisions to this document.

Table 37. Revision history

Document ID	Release date	Description
NAFE33350 v.1.0	14 January 2026	Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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