NT2H2421G0

NTAG 224 DNA - NFC T2T compliant IC

Rev. 3.1 — 5 April 2023 Product data sheet

1 General description

NTAG 224 DNA is an innovative security IC solution, compliant with NFC Type 2 Tag with 208 bytes of user memory. The technology uses multi-layered protection to support a broad range of NFC-based applications that can be trusted to protect products, services and IoT-driven user experiences.

NTAG 224 DNA IC comes with a Secure Unique NFC (SUN) message authentication. The IC can automatically add its UID and incremental tap counter to the programmed NDEF (NFC Data Exchange Format) message through ASCII mirroring, and uses an AES-128 key to secure the message with a cryptographic message authentication code (CMAC). The SUN functionality supports advanced protection to verify a tag's authenticity and integrity, whilst also enabling secured unique user experiences served in real time. The IC uses AES-128 cryptography and is Common Criteria EAL3+ (AVA.VAN.2) targeted.

NTAG 224 DNA also offers a 3-pass Mutual authentication with an AES-128 key, ensuring that only an authorized reader can access tag data. This advanced two-way authentication scheme can protect sensitive data against unauthorized access and/or a malicious change attempt.

NTAG 224 DNA offers in addition an ECC-based originality signature to assure tag origin. The originality signature can be further customized and permanently locked during tag initialization.

The NTAG 224 DNA is compliant with NFC Forum Type 2 Tag ([1]) and ISO/IEC14443 Type A part 1 to 3 ([2]).

1.1 Contactless energy and data transfer

Communication to NTAG 224 DNA can be established only when the IC is connected to an antenna. Form and specification of the coil is out of scope of this document, general recommendations can be found in the NTAG antenna design guide (see [4]).

When NTAG 224 DNA is positioned in the RF field, the high-speed RF communication interface allows the transmission of the data with a baud rate of 106 kbit/s.

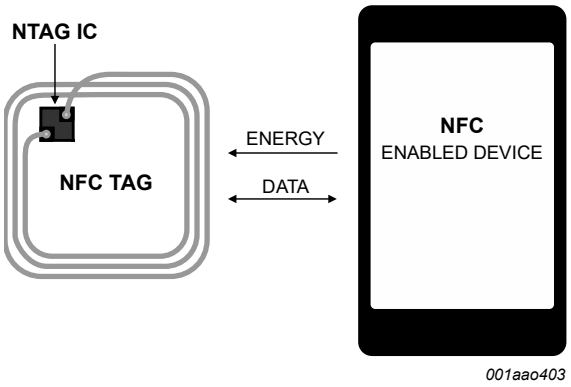


Figure 1. Contactless NTAG 224 DNA system

1.2 Simple deployment and better user experience

NTAG 224 DNA offers specific features designed to improve integration into physical objects and to enhance user experience:

- The fast read capability allows scanning the complete NDEF message with only one FAST_READ command, therefore reducing the overhead in high throughput production environments
- The RF performance allows for more flexibility in the choice of shape, dimension and material of form factors

1.3 Security

- EAL3+ AVA.VAN.2 Common Criteria certification
- Secure Unique NFC (SUN) message authentication for data authenticity and integrity protection
- 3-pass mutual Authentication with AES-128 with 128-bit key length
- Automatic NFC Tap Counter, which counts each tap
- NXP programmed 7-byte UID for each device
- Pre-programmed Capability Container with one time programmable bits
- Field programmable read-only locking function
- Pre-programmed ECC-based originality signature with an option to customize and permanently lock
- AES-based originality key leveraging the AES authentication to check the NXP origin of the IC

Note: NTAG 224 DNA comes with an external CC EAL3+ certification targeting basic attack potential (AVA_VAN.2). Hence, the contactless IC does not claim to be completely resistant. In case of broader protection is required, products with a higher security certification should be considered.

1.4 NFC Forum Tag 2 Type compliance

NTAG 224 DNA IC provides full compliance with the NFC Forum Tag 2 Type technical specification (see [2]) and enables NDEF data structure (see [3]).

1.5 Anti-collision

An anti-collision function allows operating more than one tag in the field simultaneously. The anti-collision algorithm selects each tag individually. It ensures that the execution of a transaction with a selected tag is performed correctly without interference from another tag in the field.

2 Features and benefits

- Contactless transmission of data and supply energy
- Operating frequency of 13.56 MHz
- Data transfer of 106 kbit/s
- Data integrity of 16-bit CRC, parity, bit coding, bit counting
- Operating distance up to 100 mm (depending on various parameters as e.g. field strength and antenna geometry)
- 7-byte serial number (cascade level 2 according to ISO/IEC 14443-3)
- Automatic NFC counter triggered at the first read command after a reset
- Secure Unique NFC (SUN) message authentication feature implemented via ASCII mirroring of the UID, NFC counter and CMAC into the NDEF message in the user memory, which changes on every readout after a reset
- 3-pass mutual Authentication with AES-128 with 128-bit key length
- ECC-based originality signature, offering the option to customize and permanently lock the signature
- Fast read command
- True anti-collision
- 50 pF input capacitance

2.1 EEPROM

- 304 bytes organized in 76 pages with 4 bytes per page
- 208 bytes freely available user Read/Write area (52 pages)
- 4 bytes initialized capability container with one time programmable access bits
- Field programmable read-only locking function per page for the first 16 pages
- Field programmable read-only locking function above the first 16 pages per 4 pages
- Configurable memory access authentication protection with optional limit of unsuccessful attempts
- Anti-tearing support for capability container (CC), lock bits and NFC counter
- Pre-programmed ECC-based originality signature, offering the possibility for customizing and permanently locking the signature
- Setting for galvanic or capacitive tag tamper and sensing
- Data retention time of 10 years
- Write endurance 100.000 cycles

3 Applications

- **Advanced anti-counterfeiting protection**
  Reliably verify authenticity of physical goods, anytime, anywhere using an NFC enabled device. Also consider automated authentication of NFC tagged consumables and parts in embedded devices.
- **Improved supply chain visibility and control**
  Visibly help track products along the supply chain, and reduce grey market diversion. Enable more transparent and secure supply chains, e.g. with unique content, tailored services or exclusive privileges loyalty rewards.
- **Augmented user experiences**
  Use product opening status to prompt targeted messages, e.g. pre-/post-retail. Evolve the user experience by engaging with greater personalization, e.g. with unique content, tailored services or exclusive privileges.
- **Proof of presence**
  Provide trusted proof that a person was at a given location at specific times, allowing proof of servicing or visiting times, and other time/location-based events.

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_i	input frequency		-	13.56	-	MHz
C_i	input capacitance	T_{amb} = 22 °C, f_i = 13.56 MHz, 2.2 V RMS	-	50.0	-	pF
EEPROM characteristics						
t_{ret}	retention time	T_{amb} = 22 °C	10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C	100000	-	-	cycle

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
NT2H2421G0DUD	FFC Bump	8 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format, Au bumps, 208 bytes user memory, 50 pF input capacitance	-
NT2H2421G0DUF	FFC Bump	8 inch wafer, 75 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format, Au bumps, 208 bytes user memory, 50 pF input capacitance	-

6 Block diagram

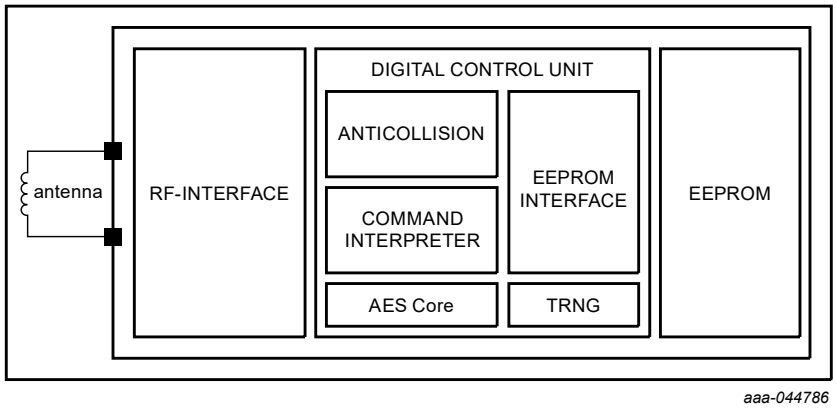


Figure 2. Block diagram of NTAG 224 DNA

7 Pinning information

7.1 Pinning

The pinning of the NTAG 224 DNA wafer delivery is shown in section "Bare die outline" (see Section 14).

Table 3. Pin allocation table

Pin	Symbol	
LA	LA	Antenna connection LA
LB	LB	Antenna connection LB
TEST	TP	Test Pin
GND	GND	Ground Pin

8 Functional description

8.1 Block description

NTAG 224 DNA ICs consist of a 304 bytes EEPROM, RF interface, and Digital Control Unit (DCU). Energy and data are transferred via an antenna consisting of a coil with a few turns which is directly connected to NTAG 224 DNA.

No further external components are necessary. Refer to [4] for details on antenna design.

- RF interface:
  - modulator/demodulator
  - rectifier
  - clock regenerator
  - Power-On Reset (POR)
  - voltage regulator
- Anti-collision: multiple cards may be selected and managed in sequence
- Command interpreter: processes memory access commands supported by the NTAG 224 DNA
- True Random Number Generator (TRNG)
- Crypto coprocessor: Advanced Encryption Standard (AES)
- EEPROM interface
- NTAG 224 DNA EEPROM : 304 bytes, organized in 76 pages of 4 bytes per page.
  - 10 bytes reserved for manufacturer data
  - 6 bytes used for the read-only locking mechanism and RFUI
  - 4 bytes available as capability container
  - 208 bytes user programmable read/write memory
  - 32 byte AES keys
  - 44 bytes of configuration data and RFUI

8.2 RF interface

The RF-interface is based on the ISO/IEC 14443 Type A standard.

During operation, the NFC device generates an RF field. The RF field must always be present with short pauses for data communication. It is used for both communication and as power supply for the tag.

For both directions of data communication, there is one start bit at the beginning of each frame. Each byte is transmitted with an odd parity bit at the end except for REQA and WUPA commands. The LSB of the byte with the lowest address of the selected block is transmitted first.

For a multi-byte parameter, the least significant byte is always transmitted first. As an example, when reading from the memory using the READ command, byte 0 from the addressed block is transmitted first. It is then followed by bytes 1 to byte 3 out of this block. The same sequence continues for the next block and all subsequent blocks.

8.3 Data integrity

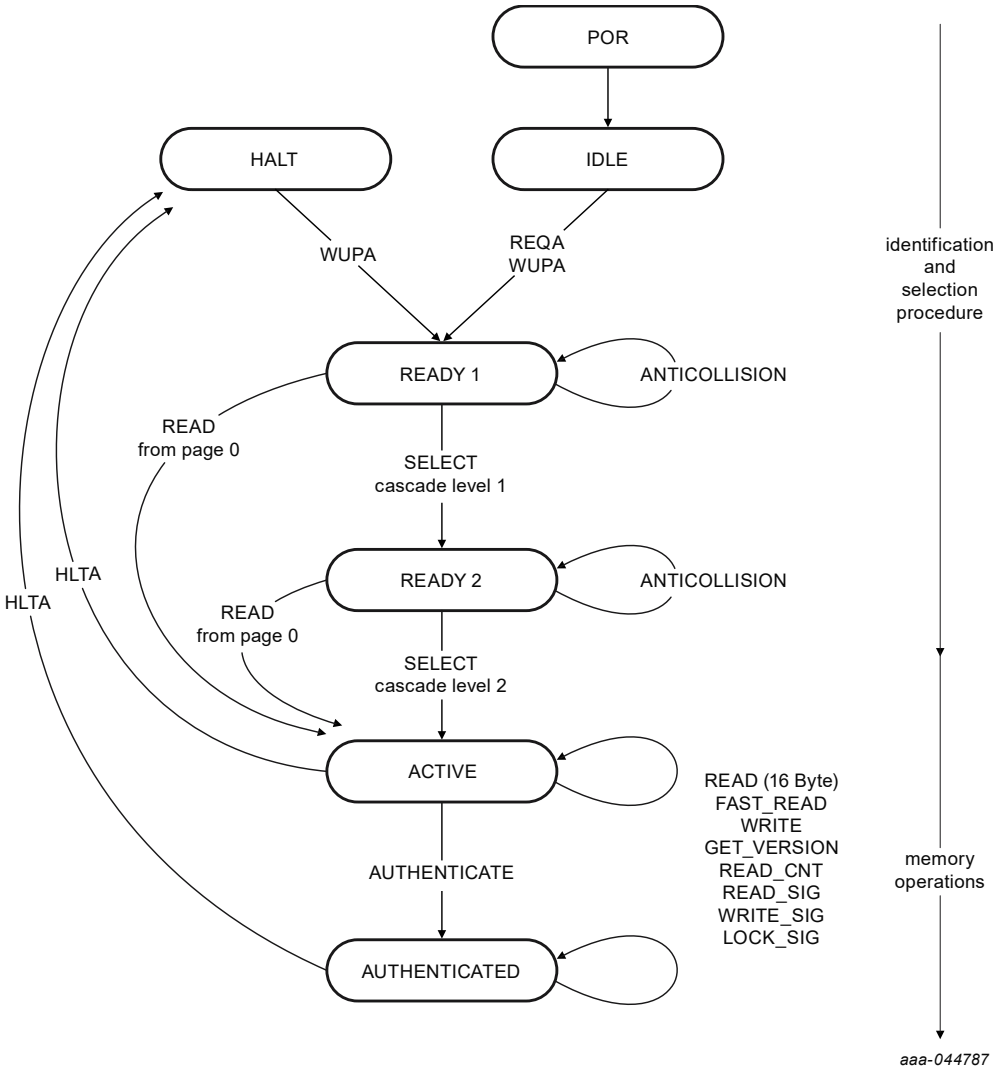
Following mechanisms are implemented in the contactless communication link between NFC device and NTAG to ensure very reliable data transmission:

- Bit count checking and bit coding to distinguish between "1", "0" and no information
- NAK1 response on user commands in case of parity or CRS error
- Parity bits for each byte

- 16-bit Cyclic Redundancy Check (CRC) according to ISO/IEC 14443-3, see [1], calculated over all preceding bytes in the same communication frame
- Channel monitoring (protocol sequence and bit stream analysis)
- Secure Unique NFC (SUN) CMAC mirror to protect the data integrity of the mirrored UID and NFC counter

8.4 Communication principle

The NFC device initiates the commands and the Digital Control Unit of the NTAG 224 DNA decodes them. The command response is depending on the state of the IC and for memory operations also on the access conditions valid for the corresponding page.



Remark: In all states, the command interpreter returns to the idle state on receipt of an unexpected command. If the IC was previously in the HALT state, it returns to that state.

Figure 3. State diagram

8.4.1 IDLE state

After a reset, NTAG 224 DNA switches to the IDLE state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received in this state is interpreted as an error and NTAG 224 DNA remains in the IDLE state.

After correctly executed HLTA command out of the ACTIVE or AUTHENTICATED state, the default waiting state changes from the IDLE state to the HALT state. This state can then be exited with a WUPA command or by a reset only.

8.4.2 READY1 state

In this state, the NFC device resolves the first part of the UID (3 bytes) using the ANTICOLLISION or SELECT commands in cascade level 1. This state is correctly exited after execution of either of the following commands:

- SELECT command from cascade level 1: the NFC device switches NTAG 224 DNA into READY2 state where the second part of the UID is resolved.
- READ command (from address 0): all anti-collision mechanisms are bypassed and the NTAG 224 DNA switches directly to the ACTIVE state.

Remark: The response of NTAG 224 DNA to the cascade level 1 SELECT command is a byte with b3 set to 1. In accordance with ISO/IEC 14443, this bit indicates that the anti-collision cascade procedure has not yet finished.

If more than one NTAG is in the NFC device field, a READ command from address 0 selects all NTAG 224 DNA devices. In this case, a collision occurs due to different serial numbers. Any other data received in the READY1 state is interpreted as an error and depending on its previous state NTAG 224 DNA returns to the IDLE or the HALT state.

8.4.3 READY2 state

In this state, NTAG 224 DNA supports the NFC device in resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, READY2 state can be skipped using a READ command (from address 0) as described for the READY1 state.

Remark: The response of NTAG 224 DNA to the cascade level 2 SELECT command is the Select Acknowledge (SAK) byte. In accordance with ISO/IEC 14443, this byte indicates if the anti-collision cascade procedure has finished. NTAG 224 DNA is now uniquely selected and only this device communicates with the NFC device even when other contactless devices are present in the NFC device field.

If more than one NTAG 224 DNA is in the NFC device field, a READ command from address 0 selects all NTAG 224 DNA devices. In this case, a collision occurs due to the different serial numbers.

Any other data received when the device is in state READY2 is interpreted as an error. Depending on its previous state, the NTAG 224 DNA returns to either the IDLE state or the HALT state.

8.4.4 ACTIVE state

Some memory operations and other functions like the originality signature read-out can be operated in the ACTIVE state.

The ACTIVE state is exited with the HLTA command. Upon reception of an HLTA command, the NTAG 224 DNA transits to the HALT state. An invalid command received when the device is in this state is interpreted as an error. Depending on its previous state, NTAG 224 DNA returns to either the IDLE state or the HALT state.

NTAG 224 DNA transits to the AUTHENTICATED state after successful 3-pass mutual authentication using the AUTHENTICATE command.

8.4.5 AUTHENTICATED state

In this state, also operations on memory pages, which are configured as authentication protected, can be accessed on top of the operation that is allowed in ACTIVE state on pages that are not access protected.

The AUTHENTICATED state is exited with the HLTA command and upon reception NTAG 224 DNA transits to the HALT state. An invalid command received when the device is in this state is interpreted as an error. Depending on its previous state, NTAG 224 DNA returns to either the IDLE state or the HALT state.

Authentication is performed using AES Authentication described in Section 8.9.1.

8.4.6 HALT state

HALT and IDLE states constitute the two wait states implemented in NTAG 224 DNA. An already processed NTAG 224 DNA can be set into the HALT state using the HLTA command. In the anti-collision phase, this state helps the NFC device to distinguish between processed tags and tags yet to be selected. NTAG 224 DNA can only exit this state on execution of the WUPA command or reset. Any other data received when the device is in this state is interpreted as an error and NTAG 224 DNA TT state remains unchanged.

8.5 Memory organization

The EEPROM memory is organized in pages with 4 bytes per page. NTAG 224 DNA has 76 pages in total. The memory organization can be seen in Table 4, and the functionality of the different memory sections is described in the following sections.

Table 4. Memory organization NTAG 224 DNA

<table>
<tr><th colspan="2">Page Addr</th><th colspan="4">Byte number within a page</th><th rowspan="2">Description</th></tr>
<tr><th>Dec</th><th>Hex</th><th>0</th><th>1</th><th>2</th><th>3</th></tr>
<tr><td>0</td><td>0h</td><td colspan="4">serial number</td><td rowspan="3">Manufacturer data and static lock bits</td></tr>
<tr><td>1</td><td>1h</td><td colspan="4">serial number</td></tr>
<tr><td>2</td><td>2h</td><td>serial number</td><td>internal</td><td>lock bits</td><td>lock bits</td></tr>
<tr><td>3</td><td>3h</td><td colspan="4">Capability Container CC</td><td>Capability Container</td></tr>
<tr><td>4</td><td>4h</td><td colspan="4" rowspan="5">user memory</td><td rowspan="5">user memory</td></tr>
<tr><td>5</td><td>5h</td></tr>
<tr><td>...</td><td></td></tr>
<tr><td>38</td><td>26h</td></tr>
<tr><td>55</td><td>37h</td></tr>
<tr><td>56</td><td>38h</td><td colspan="3">dynamic lock bits</td><td>RFUI</td><td>Dynamic lock bits</td></tr>
<tr><td>57</td><td>39h</td><td colspan="4">CFG_0</td><td rowspan="4">Configuration pages</td></tr>
<tr><td>58</td><td>3Ah</td><td colspan="4">CFG_1</td></tr>
<tr><td>59</td><td>3Bh</td><td colspan="4">RFUI</td></tr>
<tr><td>60</td><td>3Ch</td><td colspan="4">RFUI</td></tr>
</table>

Table 4. Memory organization NTAG 224 DNA*...continued*

Page Addr		Byte number within a page				Description
Dec	Hex	0	1	2	3	
61	3Dh	KEY_CFG	RFUI			
62	3Eh	TT_CTT_CFG	RFUI			
63	3Fh	NFC_CNT_LIM			RFUI	
64	40h	AES_KEY				
65	...					
66						
67	43h					
68	44h	SUNCMAC_KEY				
69	45h					
70	46h					
71	47h					
72	48h	RFUI				
73	49h	RFUI				
74	4Ah	RFUI				
75	4Bh	RFUI				

8.5.1 UID/serial number

The unique 7-byte serial number (UID) and its two check bytes are programmed into the first 9 bytes of memory: It covers page addresses 00h, 01h and the first byte of page 02h. The second byte of page address 02h is reserved for internal data. These bytes are programmed and write protected in the production test.

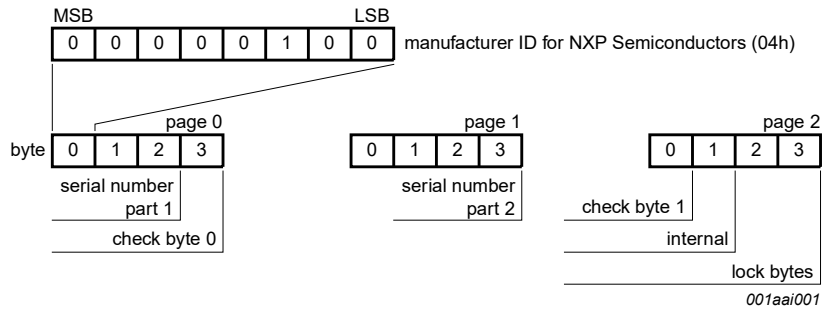


Figure 4. UID/serial number

In accordance with ISO/IEC 14443-3, check byte 0 (BCC0) is defined as CT ⊕ SN0 ⊕ SN1 ⊕ SN2. Check byte 1 (BCC1) is defined as SN3 ⊕ SN4 ⊕ SN5 ⊕ SN6.

SN0 holds the Manufacturer ID for NXP Semiconductors (04h) in accordance with ISO/IEC 14443-3.

8.5.2 Static lock bytes

The bits of byte 2 and byte 3 of page 02h represent the field programmable read-only locking mechanism. Each page from 03h (CC) to 0Fh can be individually locked by setting the corresponding locking bit Lx to logic 1 to prevent further write access. The locked page becomes read-only memory.

The three least significant bits of lock byte 0 are the block-locking bits. Bit 2 deals with pages 0Ah to 0Fh, bit 1 deals with pages 04h to 09h and bit 0 deals with page 03h (CC). Once the block-locking bits are set, the locking configuration for the corresponding memory area is frozen.

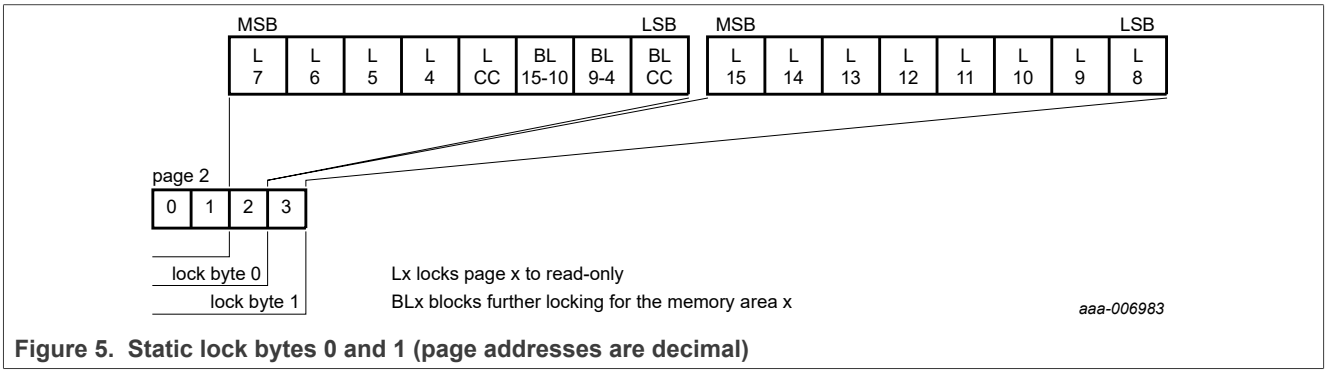


Figure 5. Static lock bytes 0 and 1 (page addresses are decimal)

For example if BL15-10 is set to logic 1, then bits L15 to L10 (lock byte 1, bit[7:2]) can no longer be changed. A WRITE command to block 02h, sets the static locking and block-locking bits. Data bytes 2 and 3 of the WRITE command, and the contents of the actual lock bytes stored in the memory, are a bit-wise OR. The result becomes the new content of the lock bytes. This process is irreversible. If a bit is set to logic 1, it cannot be changed back to logic 0.

The content of bytes 0 and 1 of page 02h is unaffected by the corresponding data bytes of the WRITE command.

The default value of the static lock bytes is 00 00h.

Any write operation to the static lock bytes is tearing-proof.

8.5.3 Dynamic Lock Bytes

To lock the pages of NTAG 224 DNA starting at page address 10h until page 37h, so called dynamic lock bytes are used. Dynamic lock bytes are located at page 38h. Three lock bytes cover the memory area of 160 data bytes. The granularity of one lock bit is 4 pages for NTAG 224 DNA (Figure 6). The programming of dynamic lock bits is irreversible. If a bit is set to logic 1, it cannot be changed back to logic 0.

Remark: It is recommended to set all bits marked with RFUI to 0, when writing to the dynamic lock bytes.

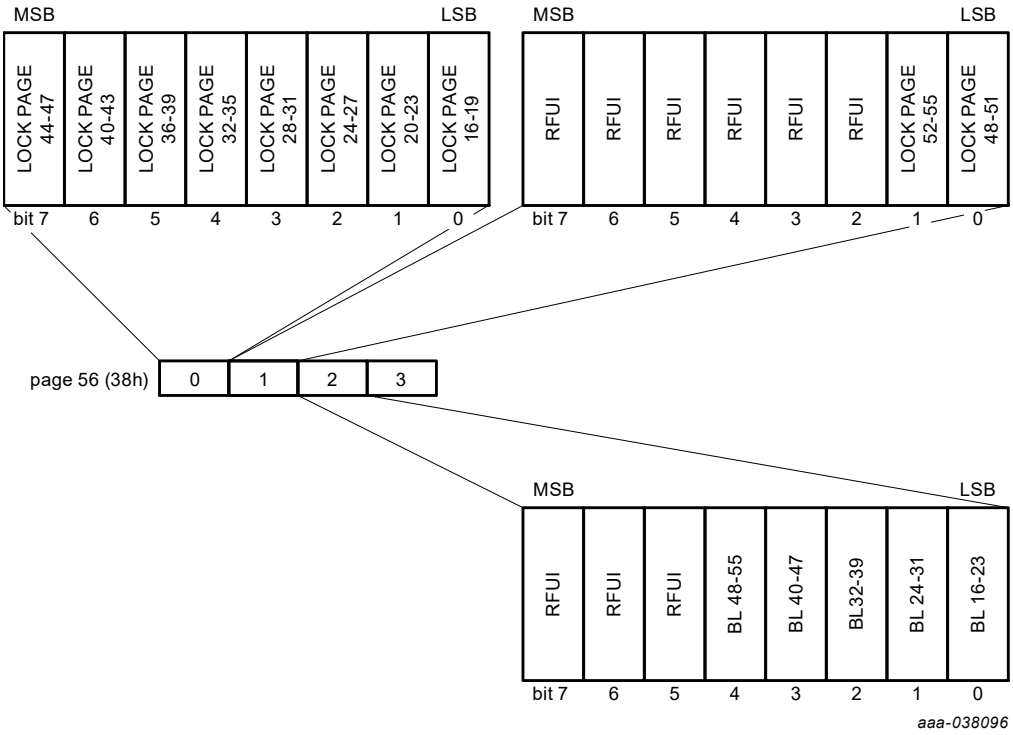


Figure 6. NTAG 224 DNA Dynamic lock bytes 0, 1 and 2 (page addresses are decimal)

The default value of the dynamic lock bytes is 00 00 00h. The value of byte 3 is always 00h when read.

Any write operation to the dynamic lock bytes is tearing-proof.

8.5.4 Capability Container (CC bytes)

The Capability Container CC (page 3) is programmed during the IC production according to the NFC Forum Type 2 Tag specification (see [2]). These bytes may be modified by a WRITE command.

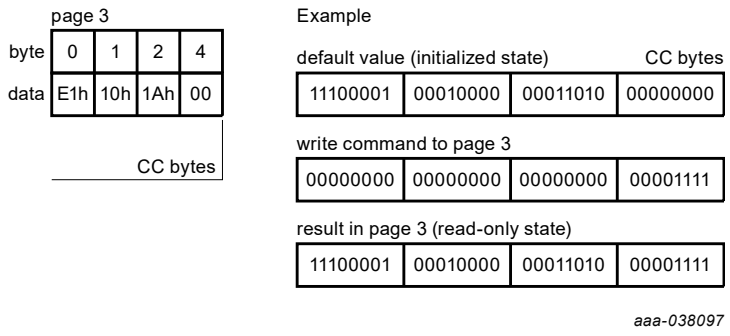


Figure 7. CC bytes example

The parameter bytes of the WRITE command and the current contents of the CC bytes are bit-wise OR'ed. The result is the new CC bytes content. This process is irreversible and once a bit is set to logic 1, it cannot be changed back to logic 0.

Byte 2 in the capability container defines the available memory size for NDEF messages. The configuration at delivery is shown in Table 5.

Table 5. NDEF memory size

IC	Value in byte 2	NDEF memory size
NTAG 224 DNA	1Ah	208 bytes

Any write operation to the CC bytes is tearing-proof.

The default values of the CC bytes at delivery are defined in Section 8.5.6.

8.5.5 Data pages

Pages 04h to 37h for NTAG 224 DNA are the 208 byte user memory read/write area.

The access to a part of the user memory area can be restricted using 3-pass mutual authentication. See Section 8.9 for further details.

The default values of the data pages at delivery are defined in Section 8.5.6.

8.5.6 Memory content at delivery

The capability container in page 03h and the data pages 04h and 05h of NTAG 224 DNA are pre-programmed as defined in Table 6.

Table 6. Memory content at delivery NTAG 224 DNA

Page Address	Byte number within page			
	0	1	2	3
03h	E1h	10h	1Ah	00h
04h	01h	03h	E0h	0Ah
05h	44h	03h	00h	FEh

The default content of the data pages from page 06h and onwards is not defined at delivery.

8.5.7 Configuration pages

Pages 39h to 4Bh for NTAG 224 DNA are used to configure the memory access restriction, to configure the ASCII mirror feature and tag tamper feature for galvanic or capacitive measurement. The location of the configuration elements is defined in Table 7.

Table 7. Configuration Pages

Page Address		Byte number			
Dec	Hex	0	1	2	3
57	39h	CFG_B0	TT	MIRROR_PAGE	AUTH0
58	3Ah	CFG_B1	RFUI	AUTHLIM0	AUTHLIM1
59	3Bh	RFUI			
60	3Ch	RFUI			
61	3Dh	KEY_CFG	RFUI	RFUI	RFUI
62	3Eh	RFUI	RFUI	RFUI	RFUI
63	3Fh	NFC_CNT_LIM			RFUI
64	40h	AES_KEY			

Table 7. Configuration Pages*...continued*

Page Address		Byte number			
Dec	Hex	0	1	2	3
65	41h				
66	42h				
67	43h				
68	44h	SUNCMAC_KEY			
69	45h				
70	46h				
71	47h				
72	48h	RFUI	RFUI	RFUI	RFUI
73	49h	RFUI	RFUI	RFUI	RFUI
74	4Ah	RFUI	RFUI	RFUI	RFUI
75	4Bh	RFUI	RFUI	RFUI	RFUI

Table 8. CFG_B0 configuration byte

Bit number							
7	6	5	4	3	2	1	0
MIRROR_EN	RFUI		MIRROR_BYTE		RFUI	RFUI	RFUI

Table 9. User memory protection AUTH0 configuration byte

Bit number							
7	6	5	4	3	2	1	0
RFUI	AUTH0 [6:0]						

Table 10. CFG_B1 configuration byte

Bit number							
7	6	5	4	3	2	1	0
PROT	LOCK_ USR_CFG	RFUI	NFC_ CNT_EN	RFUI	RFUI	RFUI	RFUI

Table 11. AUTHLIM0 configuration byte

Bit number							
7	6	5	4	3	2	1	0
AUTH_LIM [7:0]							

Table 12. AUTHLIM1 configuration byte

Bit number							
7	6	5	4	3	2	1	0
RFUI						AUTH_ LIM [9]	AUTH_ LIM [8]

Table 13. KEY_CFG configuration byte

Bit number							
7	6	5	4	3	2	1	0
LOCK_ SUNCMAC_ KEY	LOCK_ AES_KEY	BLOCK_ LOCK_KEY	RFUI				

Table 14. Configuration parameter descriptions

Field	Bit	Values at delivery	Description
MIRROR_EN	1	0b	Enables or disables the ASCII mirror functionality, if a valid MIRROR_PAGE address is set. This bit can be changed if LOCK_USR_CFG is not set. 0b ... ASCII mirror disabled 1b ... UID, NFC counter, TT and SUNCMAC ASCII mirror enabled
MIRROR_BYTE	2	00b	2 bits define the byte position within the page defined by the MIRROR_PAGE address (beginning of mirror) where the ASCII mirror shall begin. These bits can be changed if LOCK_USR_CFG is not set.
MEAS_DBL_ RANGE	1	0b	MEAS_DBL_RANGE bit set to 1 doubles the current defined in CTT _CURR_ TRIM for measurement in CTT mode. This bit can be changed if LOCK_USR_ CFG is not set. 0b ... current as defined by CTT _CURR_TRIM 1b ... current defined by CTT _CURR_TRIM will be doubled
MIRROR_PAGE	8	00h	MIRROR_PAGE address defines the page for the beginning of the mirroring. This byte can be changed if LOCK_USR_CFG is not set. A value >03h enables the ASCII mirror feature. The maximum valid value is 2Bh. If the ASCII mirror in given communication state is exceeding the accessible user memory, the ASCII mirror is disabled.
AUTH0	7	4Ch	AUTH0 defines the page address from which 3-pass mutual authentication is required. Valid address range for byte AUTH0 is from 00h to 4Bh. If AUTH0 is set to a page address outside the valid address range, the AES authentication protection is effectively disabled, but still keeping AES authentication procedure working. This byte can be changed if LOCK_USR_CFG is not set.
PROT	1	1b	PROT bit is defining the type of protection of the password protected memory part assuming the AUTH0 byte value is within the range of 00h and 4Bh. This bit can be changed if LOCK_USR_CFG is not set. 0b ... write access only is protected by the 3-pass mutual authentication 1b ... read and write access is protected by the 3-pass mutual authentication
LOCK_USR_ CFG	1	0b	LOCK_USR_CFG permanently locks the configuration elements in blocks 39h, 3Ah, and 3Fh after subsequent reset. If the bit is set to 1b it cannot be set back to 0b.

Table 14. Configuration parameter descriptions...*continued*

Field	Bit	Values at delivery	Description
			0b ... configuration elements in blocks 39h, 3Ah, and 3Fh are not locked 1b ... configuration elements in blocks 39h, 3Ah, and 3Fh are permanently locked
NFC_CNT_EN	1	0b	NFC_CNT_EN enables or disables the incrementation of the NFC counter. This bit can be changed if LOCK_USR_CFG is not set. 0b ... NFC counter increment disabled 1b ... NFC counter increment enabled If the NFC counter increment is enabled, the NFC counter will be automatically increased by 1 at the first READ or FAST_READ command after a reset until the limiting value is reached (refer to Section 8.6)
AUTH_LIM	10	000h	Limitation of failed authentication attempts. Valid value range for byte AUTH_LIM is from 00h to 3FEh. AUTH_LIM can be changed if LOCK_USR_CFG is not set. 000h ... limiting of failed authentication attempts disabled 001h - 3FEh ... maximum number of failed authentication attempts
LOCK_ SUNCMAC_KEY	1	0d	LOCK_SUNCMAC_KEY permanently locks the SUNCMAC_KEY in blocks 44h-47h. If the bit is set to 1b, it cannot be set back to 0b. 0b ... SUNCMAC_KEY in blocks 44h-47h is not locked 1b ... SUNCMAC_KEY in blocks 44h-47h is locked
LOCK_AES_KEY	1	0b	LOCK_AES_KEY permanently locks the AES_KEY in blocks 40h-43h. If the bit is set to 1b, it cannot be set back to 0b. 0b ... AES_KEY in blocks 40h-43h is not locked 1b ... AES_KEY in blocks 40h-43h is locked
BLOCK_LOCK_ KEY	1	0b	BLOCK_LOCK_KEY permanently locks the block 3Dh containing LOCK_ SUNCMAC_KEY and LOCK_AES_KEY. If the bit is set to 1b, it cannot be set back to 0b. 0b ... LOCK_SUNCMAC_KEY and LOCK_AES_KEY in block 3Dh is not locked 1b ... LOCK_SUNCMAC_KEY and LOCK_AES_KEY in block 3Dh is not locked is locked permanently
NFC_CNT_LIM	24	FFFFFFh	NFC_CNT_LIM defines the maximum value of the NFC counter (refer to Section 8.6). This bit can be changed if LOCK_USR_CFG is not set. 000000h … NFC counter limit is same as FFFFFFh 000001h - FFFFFFh … once the NFC counter has reached the NFC counter limit the counter will not be increased and will return with NAK on the first READ or FAST_READ command after a reset. After that the IC returns to the IDLE/HALT state.
AES_KEY	128	All 0h	AES_KEY refer to Section 8.9.1.
SUNCMAC_KEY	128	All 0h	SUNCMAC_KEY refer to Section 8.8.
RFUI	-	not defined	Reserved for future use.

Remark: The LOCK_USR_CFG, LOCK_SUNCMAC_KEY, BLOCK_LOCK_KEY bits activate the permanent write protection of the corresponding configuration memory sections. If write protection is enabled, each write attempt to locked elements leads immediately to a NAK response.

8.6 NFC counter function

NTAG 224 DNA features an NFC counter function. This function enables NTAG 224 DNA to automatically increase the 24-bit counter value by 1, triggered by the first valid

- READ command or
- FAST-READ command

if the NFC counter value is smaller than FF FF FFh and the NFC_CNT_LIM (see Section 8.5.7) is disabled or higher than the NFC counter value after the NTAG 224 DNA tag is powered by an RF field.

Once the NFC counter has reached the maximum value of FF FF FFh hex or the NFC counter value is same or higher than the NFC_CNT_LIM value, the NFC counter does not increase anymore. On READ or FAST_READ after reset, the NAK answer is returned and NTAG 224 DNA becomes effectively unusable.

The NFC counter increment is enabled or disabled with the NFC_CNT_EN bit (see Section 8.5.7).

The actual NFC counter value can be read with

- READ_CNT command or
- NFC counter mirror feature

8.7 ASCII mirror function

NTAG 224 DNA features an ASCII mirror function. This function enables NTAG 224 DNA to virtually mirror

- 7 byte UID (see Section 8.5.1)
- 3 byte NFC counter value (see Section 8.6)
- 8 byte SUNCMAC

into the physical memory of the IC in ASCII code. On the READ or FAST READ command to the involved user memory pages, NTAG 224 DNA responds with the virtual memory content of the UID and/or NFC counter value and or Tag Tamper message in ASCII code.

The required length of the reserved physical memory for the mirror functions and the order for the ASCII mirrors is specified in Table 11. If the ASCII mirror exceeds the accessible user memory area, the data will not be mirrored.

Table 15. Required memory placeholder space for ASCII mirror

ASCII mirror and order	Required number of bytes in the physical memory
UID + NFC counter + TT message mirror + SUNCMAC	38 bytes (14 bytes for UID + 1 byte separation + 6 bytes NFC counter value + 1 byte separation + 16 byte SUNCMAC value)

The MIRROR_PAGE value defines the page where the ASCII mirror shall start and the MIRROR_BYTE value defines the starting byte within the defined page.

The ASCII mirror function is enabled with MIRROR_EN set to 1b and MIRROR_PAGE value >03h.

The ASCII mirror elements are separated automatically with an "x" character (78h ASCII code).

Remark: Please note that the number of bytes (see Table 15) of the ASCII mirror shall not exceed the boundary of the user memory. Therefore it is required to use only valid values for MIRROR_BYTE and MIRROR_PAGE to ensure a proper functionality. If the ASCII mirror exceeds the user memory area, the ASCII mirrors shall be disabled.

8.7.1 UID ASCII mirror function

This function enables NTAG 224 DNA to virtually mirror the 7 byte UID in ASCII code into the physical memory of the IC. The length of the UID ASCII mirror requires 14 bytes to mirror the UID in ASCII code. On the READ or FAST READ command to the involved user memory pages, NTAG 224 DNA responds with the virtual memory content of the UID in ASCII code.

For an example see Table 16.

8.7.2 NFC counter mirror function

This function enables NTAG 224 DNA to virtually mirror the 3 byte NFC counter value in ASCII code into the physical memory of the IC. The length of the NFC counter mirror requires 6 bytes to mirror the NFC counter value in ASCII code. On the READ or FAST READ command to the involved user memory pages, NTAG 224 DNA responds with the virtual memory content of the NFC counter in ASCII code.

For an example see Table 17.

Remark: To enable the NFC counter increment itself (see Section 8.7), the NFC_CNT_EN bit shall be set to 1b.

8.7.3 SUNCMAC mirror function

The SUNCMAC is calculated over the UID, NFC counter and Tag Tamper information. This function enables NTAG 224 DNA to virtually mirror the 8 byte SUNCMAC in ASCII code into the physical memory of the IC. The length of the SUNCMAC ASCII mirror requires 16 bytes to mirror the SUNCMAC in ASCII code.

To validate the mirrored data of UID, NFC counter and Tag Tamper information see Section 8.8

8.8 SUNCMAC

8.8.1 SUNCMAC calculation

The 8-byte SUNCMAC is calculated using AES according to the CMAC standard described in NIST Special Publication 800-38B (refer to [9]). Padding is applied according to this standard.

The MAC used in NTAG 224 DNA is truncated by using only the 8 even-numbered bytes out of the 16 bytes output as described NIST Special Publication 800-38B (refer to [9]) when represented in most-to-least-significant order.

The initialization vector used for the SUNCMAC computation is the zero byte IV as prescribed in NIST Special Publication 800-38B (refer to [9]).

The SUNCMAC is defined as follows:

SUNCMAC = MACt (SUNCMAC_KEY; DynamicSUNData)

with DynamicSUNData being the data in hex values (not mirrored ASCII values) of the UID and NFC.

with DynamicSUNData being the data in hex values (not mirrored ASCII values) of the UID, NFC counter and Tag Tamper.

The data from the mirrored information for the SUNCMAC calculation needs to be transferred as shown below.

14 Byte UID need to be transferred from ASCII to Hex value as shown in Table 16.

Table 16. UID mirrored data example

UID mirror data	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10	Byte 11	Byte 12	Byte 13	Byte 14
Mirrored data in hex	30	34	45	31	34	31	31	32	34	43	32	38	38	30
Mirrored ASCII character	0	4	E	1	4	1	1	2	4	C	2	8	8	0

For this example, the data of the UID for the SUNCMAC calculation are 04E141124C2880h.

6 Byte NFC counter mirror needs to be transferred from ASCII to Hex value as shown in Table 17.

Table 17. NFC counter mirrored data example

NFC counter mirror data	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Mirrored data in hex	30	30	30	34	41	46
Mirrored ASCII character	0	0	0	4	A	F

For this example, the data of the NFC Counter value for SUNCMAC calculation is 0004AFh.

For the example, the DynamicSUNData for the SUNCMAC calculation is 04E141124C28800004AFh.

8.8.2 Programming of the SUNCMAC key

The 16 bytes of the SUNCMAC key are programmed to memory pages from 44h to 47h. The keys are stored in memory as shown in the table below. The key itself can be written during personalization or at any later stage using the WRITE command. For both commands, byte 0 is always sent first.

Table 18. SUNCMAC_KEY memory configuration

Page Address		Byte Number			
Dec	Hex	0	1	2	3
68	44h	K00	K01	K02	K03
69	45h	K04	K05	K06	K07
70	46h	K08	K09	K10	K11
71	47h	K12	K13	K14	K15

On example of SUNCMAC_KEY = 000102030405060708090A0B0C0D0E0Fh, the command sequence needed for key programming with WRITE command is:

- A2 44 0F 0E 0D 0C CRC
- A2 45 0B 0A 09 08 CRC
- A2 46 07 06 05 04 CRC
- A2 47 03 02 01 00 CRC

The memory content after those WRITE commands is shown in the table below:

Table 19. SUNCMAC_KEY memory configuration based on example configuration

Page Address		Byte Number			
Dec	Hex	0	1	2	3
68	44h	0Fh	0Eh	0Dh	0Ch
69	45h	0Bh	0Ah	09h	08h
70	46h	07h	06h	05h	04h
71	47h	03h	02h	01h	00h

The content of memory pages holding the SUNCMAC key can never be directly read neither by READ nor by FAST READ commands.

8.9 AES authentication protection

The memory write or read/write access to a configurable part of the memory can be constrained by a 3-pass mutual authentication. The 128-bit secret AES key is typically programmed into the relevant configuration pages at the tag personalization stage.

The AUTH_LIM parameter specified in Section 8.5.7 can be used to limit the amount of failed authentication. Once this limit is exceeded, protected memory part cannot be authenticated and accessed any longer.

By default, authentication protection is disabled by an AUTH0 value of 4Bh. AES_KEY is freely writable in this state. Access to the configuration pages and any part of the user memory can be restricted by setting AUTH0 to a page address within the available memory space. This page address is the first one protected (see Section 8.9.4).

8.9.1 AES authentication

The AES authentication implemented in the NTAG 224 DNA proves that two entities hold the same secret and each entity can be seen as a reliable partner for onwards communication. The applied encryption algorithm ek() is the AES encryption in Cipher-Block Chaining (CBC) mode as described in ISO/IEC 10116 (see [10]). The Initialization Vector (IV) of the first encryption of the protocol is the all zero block. The following table shows the communication flow during authentication:

Table 20. AES authentication

#	Reader device	Data exchanged	Tag	
1	The reader device is always the entity which starts an authentication procedure. This is done by sending the command AUTHENTICATE.	"1Ah" → AUTHENTICATE		Step 1
2		← "AFh" || 16 bytes *ek(RndB)*	The tag generates a 16-byte-random number *RndB*. This random number is **en**ciphered with the key, denoted by *ek(RndB),* and is then transmitted to the reader device.	
3	The reader device itself generates a 16-byte-random number *RndA*. This *RndA* is concatenated with *RndB*' and **en**ciphered with the key. *RndB*' is generated by rotating the original *RndB* left by 8 bits. This token *ek(RndA || RndB')* is sent to the tag.	→ "AFh" || 32 bytes *ek(RndA || RndB')*		
4		← "00h" || 16 bytes *ek(RndA')*	The tag runs a **de**cipherment on the received token and therefore gains *RndA* + *RndB*'. The tag can now verify the sent *RndB*' by comparing it with the *RndB*' obtained by rotating the original *RndB* left by 8 bits internally. A successful verification proves to the tag that the tag and the reader device posses the same secret key. If the verification fails, the tag stops the authentication procedure and returns an error message. As the tag also received the random number *RndA*, generated by the reader device, it can perform a rotate left operation by 8 bits on *RndA* to gain *RndA',* which is **en**ciphered again, resulting in *ek(RndA').* This token is sent to the reader device.	Step 2
5	The reader device runs a **de**cipherment on the received *ek(RndA')* and therefore gains *RndA'* for comparison with the reader device-internally rotated *RndA'*. If the comparison fails, the reader device exits the procedure and may halt the tag.			
6			The tag sets the state to authenticate.	

The cryptographic method is based on AES in CBC mode according to NIST Special Publication 800-38A (see [8]).

See command details in Section 10.6. The used key is a 128-bit AES_KEY.

Note: To reduce the risk on tag-only side channel attacks on AES key, the failed authentication limit (AUTH_LIM) can be set.

8.9.2 AES Authentication example

A numerical example of a AES authentication process is shown below in Table 21. The AES key used in this example has a value of all zeros.

Table 21. Numerical AES authentication example

#	Reader device	Data exchanged	Tag
1	start the authentication procedure	→ 1A00 CRC16	
2		← AF A04C124213C186 F22399D33AC2A30215 B34408A23D8AEA266 CAB947EA8E0118D CRC16	generate RndB = B9E2FC789B64BF23 7CCCAA20EC7E6E48 IV = 0000000000000000 0000000000000000 ek(RndB) = A04C124213C186F2 2399D33AC2A30215
3	decipher ek(RndB) to retrieve RndB generate RndA = 13C5DB8A5930439F C3DEF9A4C675360F RndB' = E2FC789B64BF237C CCAA20EC7E6E48B9 IV = 0000000000000000 0000000000000000 ek(RndA+RndB´) = 35C3E05A752E0144 BAC0DE51C1F22C56 B34408A23D8AEA26 6CAB947EA8E0118D	→ AF 35C3E05A752E0144 BAC0DE51C1F22C56 CRC16	
4		← 00 DB5A73B3BC9D0501 D0C52177DE630619 CRC16	decipher ek(RndA+RndB´) to retrieve RndA and verify RndB' RndA' = C5DB8A5930439FC3 DEF9A4C675360F13 IV = 0000000000000000 0000000000000000 ek(RndA´) = DB5A73B3BC9D0501 D0C52177DE630619
5	decipher and verify ek(RndA')		

8.9.3 Programming of the AES key

The 16 bytes of the AES_KEY are programmed to memory pages from 40h to 43h. The key is stored in memory as shown in Table 22. The key itself can be written during personalization or at any later stage using the WRITE command. For both commands, Byte 0 is always sent first.

Table 22. AES key memory configuration

Page Address		Byte Number			
Dec	Hex	0	1	2	3
64	40h	K00	K01	K02	K03
65	41h	K04	K05	K06	K07
66	42h	K08	K09	K10	K11
67	43h	K12	K13	K14	K15

On example of AES Key = 000102030405060708090A0B0C0D0E0Fh, the command sequence needed for key programming with WRITE command is:

- A2 40 0F 0E 0D 0C CRC
- A2 41 0B 0A 09 08 CRC
- A2 42 07 06 05 04 CRC
- A2 42 03 02 01 00 CRC

The memory content after those WRITE commands is shown in the table below:

Table 23. AES key memory configuration based on example configuration

Page Address		Byte Number			
Dec	Hex	0	1	2	3
64	40h	0Fh	0Eh	0Dh	0Ch
65	41h	0Bh	0Ah	09h	08h
66	42h	07h	06h	05h	04h
67	43h	03h	02h	01h	00h

The content of memory pages holding the SUNCMAC key can never be directly read neither by READ nor by FAST READ commands.

8.9.4 Configuration for memory access via AES authentication

The behavior of the memory access rights depending on the authentication is configured with the configuration byte AUTH0 (located in byte 3 of pages 39h, see Section 8.5.7) and the PROT bit (located in byte 0 of block 3Ah, see Section 8.5.7).

- AUTH0 defines the page address from which the authentication is required. Valid address values for byte AUTH0 are from 00h to 4Ch.
- Setting AUTH0 to a value to 4Ch effectively disables memory protection.
- PROT determines if write access is restricted or both read and write access are restricted.

8.9.5 Limiting failed authentication attempts

To reduce the risk on tag-only side channel attacks on AES key, the maximum allowed number of failed authentication attempts can be set using AUTH_LIM. This mechanism is disabled by setting AUTH_LIM to a value of 000h, which is also the initial state of NTAG 224 DNA.

If AUTH_LIM is not equal to 000h, each failed authentication attempt is internally counted and stored. The count operation features anti-tearing support. As soon as this internal counter reaches the number specified in AUTH_LIM, any further failed authentication attempt leads to a permanent locking of the protected part of the

memory for the specified access rights. Specifically, each subsequent authentication fails independent if the authentication would be successful or not.

Any successful authentication, before reaching the limit of failed authentication attempts, decrements the internal counter by value 10h. In case the counter is at value of 10h or below the counter is reset.

8.9.6 Protection of configuration pages

The configuration pages can be protected by the 3-pass authentication as well. The protection level is defined with the PROT bit.

The protection is enabled by setting the AUTH0 byte to a value that is within the addressable memory space before relevant configuration page address.

8.10 Originality signature

The NTAG 224 DNA offers a feature to verify the origin of a tag confidently, using the ECC-based originality signature stored in a hidden part of memory. The originality signature can be read with the READ_SIG command.

The purpose of the ECC originality check during (pre-)personalization is to protect customer investments by identifying mass penetration of non-NXP originated NTAG 224 DNA ICs into an infrastructure. As individual signatures can still be copied, it does not completely prevent hardware copy or emulation of individual NTAG 224 DNA ICs. As such, a valid signature is not a full guarantee. Therefore, this signature validation should be complemented with a check to detect if multiple ICs with the sameUID are being introduced in the system.

The NTAG 224 DNA provides the possibility to customize the originality signature to personalize the IC individually for specific application.

At delivery, the NTAG 224 DNA is pre-programmed with the NXP originality signature described below. This signature is locked in the dedicated memory. If needed, the signature can be unlocked with the LOCK_SIG command. It is reprogrammed with a custom-specific signature using the WRITE_SIG command during the personalization process by the customer. The signature can be permanently locked afterward with the LOCK_SIG command to avoid further modifications.

Remark: If no customized originality signature is required, it is recommended to lock the NXP signature permanently during the initialization process with the LOCK_SIG command.

In addition to the ECC-based originality signature, the NTAG 224 DNA features an AES-based NXP originality check. For that NXP programs, an NXP owned diversified AES originality key into the hidden part of the memory which can be used with the AUTHENTICATE command to check whether the IC is a genuine NXP product.

8.10.1 Originality Signature at delivery

At the delivery, the NTAG 224 DNA is programmed with an NXP digital signature based on standard Elliptic Curve Cryptography (curve name secp192r1), according to the ECDSA algorithm. The use of a standard algorithm and curve ensures easy software integration of the originality check procedure in NFC devices.

Each NTAG 224 DNA UID is signed with an NXP private key and the resulting 48-byte signature is stored in a hidden part of the NTAG 224 DNA memory during IC production.

This signature can be retrieved using the READ_SIG command and verified in the NFC device by using the corresponding ECC public key provided by NXP. In case the NXP public key is stored in the NFC device, the complete signature verification procedure can be performed offline.

To verify the signature, for example with the use of the public domain cryptolibrary OpenSSL, the tool domain parameters are set to secp192r1. It is defined within the standards for elliptic curve cryptography SEC ([7]).

Details on how to check that the NXP signature value is provided in following application note ([5]). It is foreseen to offer an online and offline way to verify originality of NTAG 224 DNA.

9 Command overview

NTAG 224 DNA activation follows part 2 and part 3 of ISO/IEC 14443 Type A. After NTAG 224 DNA has been selected, it can either be deactivated using the ISO/IEC 14443 HLTA command, or the NTAG 224 DNA commands (e.g. READ or WRITE) can be performed. For more details about the card activation, refer to [1]

9.1 NTAG 224 DNA command overview

All available commands for NTAG 224 DNA are shown in Table 24.

Table 24. Command overview

Command[1]	ISO/IEC 14443	NFC FORUM	Command code (hexadecimal)
Request	REQA	SENS_REQ	26h (7 bit)
Wake-up	WUPA	ALL_REQ	52h (7 bit)
Anti-collision CL1	Anti-collision CL1	SDD_REQ CL1	93h 20h
Select CL1	Select CL1	SEL_REQ CL1	93h 70h
Anti-collision CL2	Anti-collision CL2	SDD_REQ CL2	95h 20h
Select CL2	Select CL2	SEL_REQ CL2	95h 70h
Halt	HLTA	SLP_REQ	50h 00h
GET_VERSION	-	-	60h
READ	-	READ	30h
FAST_READ	-	-	3Ah
WRITE	-	WRITE	A2h
READ_CNT	-	-	39h
AUTHENTICATE - Part 1	-	-	1Ah
AUTHENTICATE - Part 2	-	-	AFh
READ_SIG	-	-	3Ch
WRITE_SIG	-	-	A9h
LOCK_SIG	-	-	ACh

[1] Unless otherwise specified, all commands use the coding and framing as described in [1].

9.2 Timings

The command and response timings shown in this document are not to scale and values are rounded to 1 µs.

All given command and response transmission times refer to the data frames including start of communication and end of communication. They do not include the encoding (like the Miller pulses). An NFC device data frame contains the start of communication (1 "start bit") and the end of communication (one logic 0 + 1-bit length of unmodulated carrier). An NFC tag data frame contains the start of communication (1 "start bit") and the end of communication (1-bit length of no subcarrier).

The minimum command response time is specified according to [1] as an integer n which specifies the NFC device to NFC tag frame delay time. The frame delay time from NFC tag to NFC device is at least 87 µs. The maximum command response time is specified as a timeout value. Depending on the command, the T_{ACK} value

specified for command responses defines the NFC device to NFC tag frame delay time. It does this for either the 4-bit ACK value specified in Section 9.3 or for a data frame.

All command timings are according to ISO/IEC 14443-3 frame specification as shown for the Frame Delay Time in Figure 9. For more details, refer to [1].

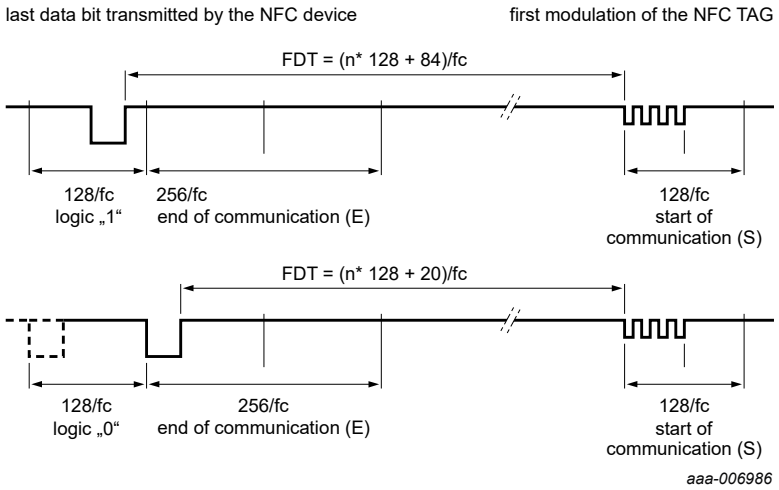


Figure 8. Frame Delay Time (from NFC device to NFC tag)

Remark: Due to the coding of commands, the measured command timings usually exclude (a part of) the end of communication. This factor shall be considered when comparing the specified with the measured times.

9.3 NTAG ACK and NAK

NTAG uses a 4-bit ACK / NAK as shown in Table 25.

Table 25. ACK and NAK values

Code (4 bit)	ACK/NAK
Ah	Acknowledge (ACK)
0h	NAK for invalid argument (i.e. invalid page address)
1h	NAK for parity or CRC error
4h	NAK for failed authentication counter overflow or NFC counter exceeding the limit
5h	NAK for EEPROM write error
6h	NAK if valid page indicators are corrupted for the given tearing protected pages. This can be due to memory content corruption caused by an attack.
7h	NAK for EEPROM write error

9.4 ATQA and SAK responses

NTAG 224 DNA replies to a REQA or WUPA command with the ATQA value shown in Table 26. It replies to a Select CL2 command with the SAK value shown in Table 27. The 2-byte ATQA value is transmitted with the least significant byte first (44h).

Table 26. ATQA response of the NTAG 224 DNA

		Bit number															
Sales type	**Hex value**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
NT2H2421G0	00 44h	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Table 27. SAK response of the NTAG 224 DNA

		Bit number							
Sales type	**Hex value**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
NT2H2421G0	00h	0	0	0	0	0	0	0	0

Remark: The ATQA coding in bits 7 and 8 indicate the UID size according to Ref. 1 independent from the settings of the UID usage.

Remark: The bit numbering in the ISO/IEC 14443 starts with LSB = bit 1 and not with

LSB = bit 0. So 1 byte counts bit 1 to bit 8 instead of bit 0 to 7.

10 NTAG commands

10.1 GET_VERSION

The GET_VERSION command is used to retrieve information on the NTAG family, the product version, storage size and other product data required to identify the specific NTAG IC.

This command is also available on other NTAG products to have a common way of identifying products across platforms and evolution steps.

The GET_VERSION command has no arguments and replies the version information for the specific NTAG IC type. The command structure is shown in Figure 9 and Table 28.

Table 31 shows the required timing.

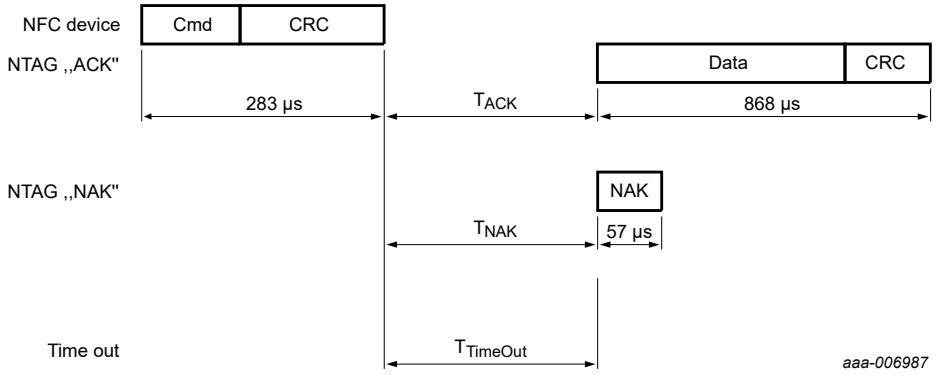


Figure 9. GET_VERSION command

Table 28. GET_VERSION command

Name	Code	Description	Length
Cmd	60h	Get product version	1 byte
CRC	-	CRC according to [1]	2 bytes

Table 29. GET_VERSION response

Name	Code	Description	Length
Data	-	Product version information (see Table 30)	8 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4 bits

Table 30. GET_VERSION data response for NTAG 224 DNA

Byte no.	Description	NTAG 224 DNA	Interpretation
0	fixed Header	00h	
1	vendor ID	04h	NXP Semiconductors
2	product type	04h	NTAG

Table 30. GET_VERSION data response for NTAG 224 DNA*...continued*

Byte no.	Description	NTAG 224 DNA	Interpretation
3	product subtype	02h	50 pF
4	major product version	05h	5
5	minor product version	00h	V0
6	storage size	10h	208 byte user memory
7	protocol type	03h	ISO/IEC 14443-3 compliant

Remark: For the NTAG 224 DNA, the calculation formula from other NTAG types for the user memory size out of the storage size byte cannot be used.

Table 31. GET_VERSION timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
GET_VERSION	n=9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 9.2.

10.2 READ

The READ command requires a start page address, and returns 16 bytes of four NTAG 224 DNA pages. For example, if address (Addr) is 03h then the content pages 03h, 04h, 05h, 06h are returned. So call roll-over mechanism applies if the READ command address is near the end of the accessible memory area. The same mechanism also applies if at least part of the addressed pages is within an authentication protected area. For details on the command structure, refer to Figure 10 and Table 32.

Table 34 shows the required timing.

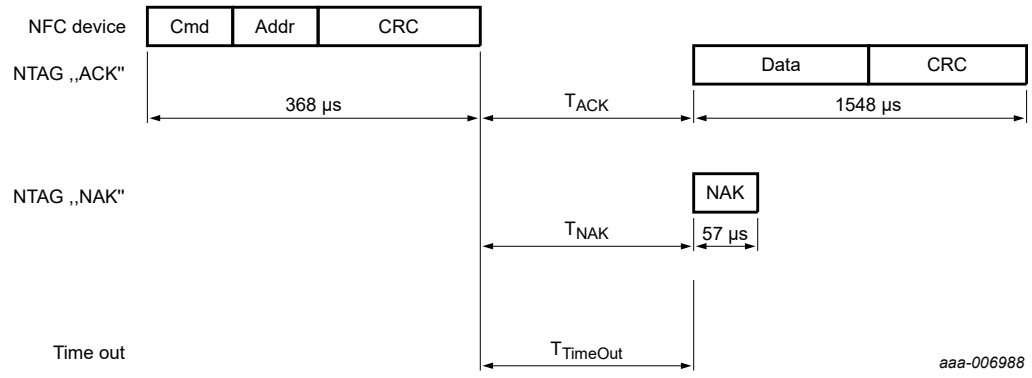


Figure 10. READ command

Table 32. READ command

Name	Code	Description	Length
Cmd	30h	read four pages	1 byte
Addr	-	start page address	1 byte
CRC	-	CRC according to [1]	2 bytes

Table 33. READ response

Name	Code	Description	Length
Data	-	Data content of the addressed pages	16 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4 bits

Table 34. READ timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ	n=9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 9.2.

In the initial state of NTAG 224 DNA, all memory pages in the range from 00h until 4Bh are allowed as Addr parameter to the READ command.

Addressing a memory page beyond address 4Bh results in a NAK response from NTAG 224 DNA.

A roll-over mechanism is implemented to continue reading from page 00h once the end of the accessible memory is reached. For example, reading from address 49h on an NTAG 224 DNA results in pages 49h, 4Ah, 4Bh and 00h being returned.

The following conditions apply if part of the memory is authentication protected for read access:

- if NTAG 224 DNA is in the ACTIVE state
  - addressing a page which is equal or higher than AUTH0 results in a NAK response
  - addressing a page lower than AUTH0 results in data being returned with the roll-over mechanism occurring just one page before the AUTH0 defined page
- if NTAG 224 DNA is in the AUTHENTICATED state
  - the READ command behaves like on an NTAG 224 DNA without access protection

Remark: SUNCMAC_KEY and AES_KEY values cannot be read out of the memory. When reading from the pages holding those two values, all 00h bytes are replied to the NFC device instead.

10.3 FAST_READ

The FAST_READ command requires a start page address and an end page address and returns the bytes of the addressed pages. For example if the start address is 03h and the end address is 07h then pages 03h, 04h, 05h, 06h and 07h are returned. If either start or end address is out of the accessible area, NTAG 224 DNA replies a NAK. For details on the command structure, refer to Figure 11 and Table 35.

Table 37 shows the required timing.

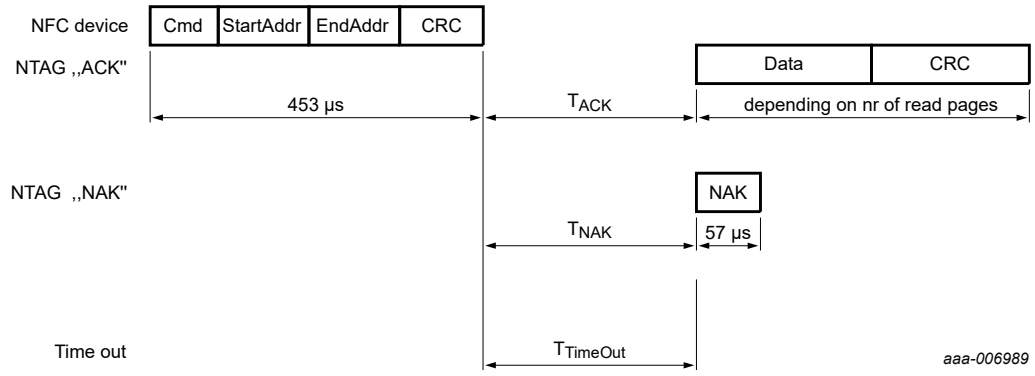


Figure 11. FAST_READ command

Table 35. FAST_READ command

Name	Code	Description	Length
Cmd	3Ah	read multiple pages	1 byte
StartAddr	-	start page address	1 byte
EndAddr	-	end page address	1 byte
CRC	-	CRC according to [1]	2 bytes

Table 36. FAST_READ response

Name	Code	Description	Length
Data	-	data content of the addressed pages	n*4 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4 bits

Table 37. FAST_READ timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
FAST_READ	n=9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 9.2.

In the initial state of NTAG 224 DNA, all memory pages in the range from 00h to 4Bh are allowed as StartAddr parameter to the FAST_READ command.

Addressing a memory page beyond address 4Bh results in a NAK response from NTAG 224 DNA.

The EndAddr parameter must be equal to or higher than the StartAddr otherwise NAK response is provided.

The following conditions apply if part of the memory is authentication protected for read access:

- if NTAG 224 DNA is in the ACTIVE state
  - if any requested page address is equal or higher than AUTH0 a NAK is replied
- if NTAG 224 DNA is in the AUTHENTICATED state
  - the FAST_READ command behaves like on an NTAG 224 DNA without access protection

Remark: SUNCMAC_KEY and AES_KEY values cannot be read out of the memory. When reading from pages holding those two values, all 00h bytes are replied to the NFC device instead.

Remark: The FAST_READ command is able to read out the whole accessible memory. Nevertheless, receive buffer of the NFC device must be able to handle the requested amount of data as there is no chaining possibility.

10.4 WRITE

The WRITE command requires a block address, and writes 4 bytes of data into the addressed NTAG 224 DNA page. The WRITE command is shown in Figure 12 and Table 38.

Table 40 shows the required timing.

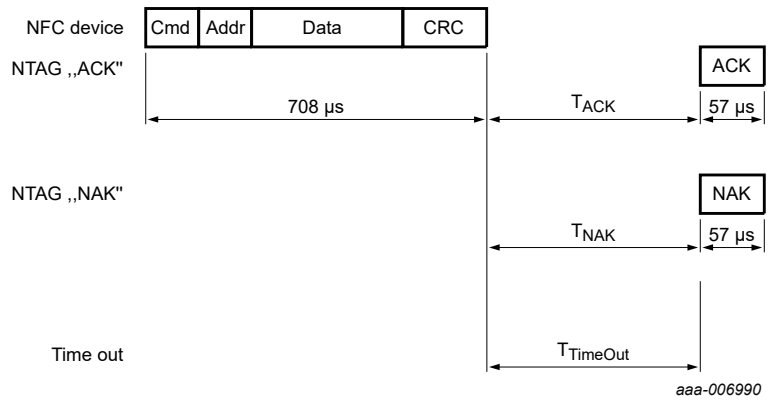


Figure 12. WRITE command

Table 38. WRITE command

Name	Code	Description	Length
Cmd	A2h	write one page	1 byte
Addr	-	page address	1 byte
Data	-	data	4 bytes
CRC	-	CRC according to [1]	2 bytes

Table 39. WRITE response

Name	Code	Description	Length
ACK/NAK	see Table 25	see Section 9.3	4 bits

Table 40. WRITE timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE	n=9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 9.2.

In the initial state of NTAG 224 DNA, page address 02h to 4Bh are valid Addr parameters to the WRITE command.

Addressing a memory page beyond address 4Bh results in a NAK response from NTAG 224 DNA.

Pages which are locked against writing cannot be reprogrammed using WRITE command. The locking mechanisms include static and dynamic lock bits as well as specific lock bits of different configuration elements.

The following conditions apply if part of the memory is authentication protected for write access:

- if NTAG 224 DNA is in the ACTIVE state
  - writing to a page which address is equal or higher than AUTH0 results in a NAK response
- if NTAG 224 DNA is in the AUTHENTICATED state
  - the WRITE command behaves like on an NTAG 224 DNA without access protection

NTAG 224 DNA features tearing protected write operations to specific memory content. The following pages are protected against tearing events during a WRITE operation:

- page 02h containing static lock bits
- page 03h containing CC bits
- page 38h containing the additional dynamic lock bits for the NTAG 224 DNA

10.5 READ_CNT

The READ_CNT command is used to read out the current value of the NFC one-way counter of the NTAG 224 DNA. The command has a single argument specifying the counter number and returns the 24-bit counter value of the corresponding counter. The command structure is shown in Figure 13 and Table 41.

Table 43 shows the required timing.

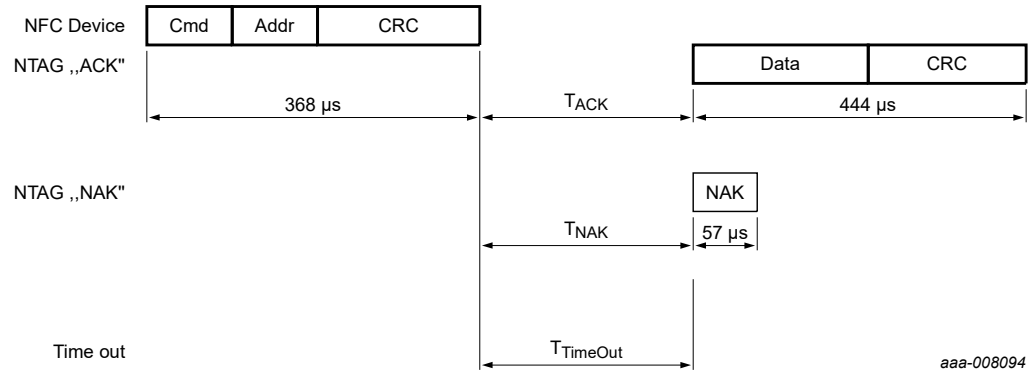


Figure 13. READ_CNT command

Table 41. READ_CNT command

Name	Code	Description	Length
Cmd	39h	read counter	1 byte
Addr	02h	NFC counter address	1 byte
CRC	-	CRC according to [1]	2 bytes

Table 42. READ_CNT response

Name	Code	Description	Length
Data	-	counter value	3 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4 bits

Table 43. READ_CNT timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ_CNT	n=9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 9.2.

10.6 AUTHENTICATE

Description: The authentication process is detailed in Section 8.9.

Executing an HLTA command results in losing the authentication status.

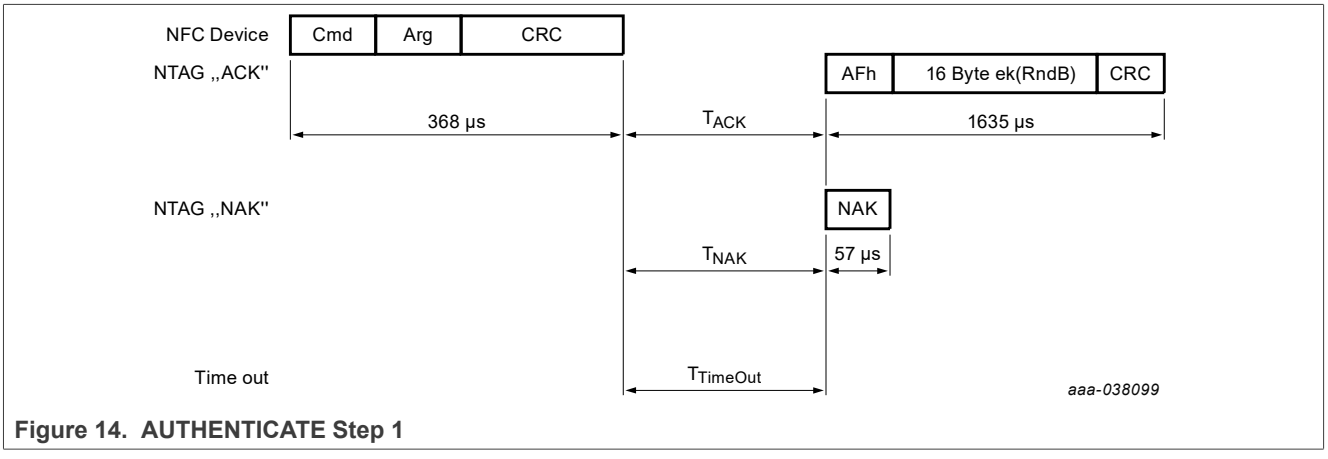


Figure 14. AUTHENTICATE Step 1

Table 44. AUTHENTICATE part 1 command

Name	Code	Description	Length
Cmd	1Ah	authentication part 1	1 byte
Arg	00h	fixed value 00h as argument	1 byte

Table 44. AUTHENTICATE part 1 command*...continued*

Name	Code	Description	Length
CRC	-	CRC according to [1]	2 bytes

Table 45. AUTHENTICATE part 1 response

Name	Code	Description	Length
AFh	AFh	first response byte indicates that the authentication process needs a second command part	1 byte
ek(RndB)	-	16-byte encrypted NTAG random number RndB	16 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4-bit

Table 46. AUTHENTICATE part 1 timing

These times exclude the end of communication of the NFC device.

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
AUTHENTICATE part 1	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	10 ms

Table 47. AUTHENTICATE Step 2

Code	Parameter	Data	Integrity mechanism	Response
AFh	-	ek(RndA+RndB')	Parity, CRC	'00' + ek(RndA')

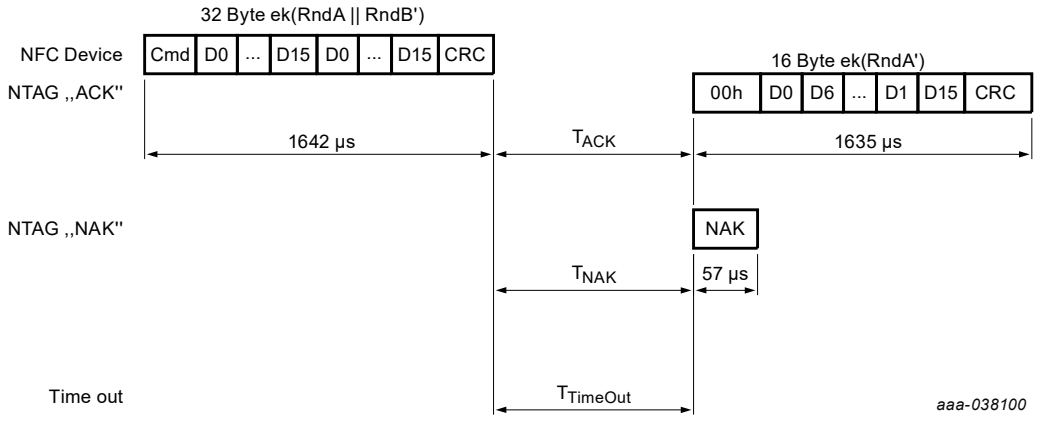


Figure 15. AUTHENTICATE Step 2

Table 48. AUTHENTICATE part 2 command

Name	Code	Description	Length
Cmd	AFh	fixed first byte for the AUTHENTICATE part 2 command	1 byte
ek(RndA || RndB')	-	32-byte encrypted random numbers RNDA concatenated by RndB'	32 bytes
CRC	-	CRC according to [1]	2 bytes

Table 49. AUTHENTICATE part 2 response

Name	Code	Description	Length
00h	00h	first response byte indicates that the authentication process is finished after this command	1 byte
ek(RndA')	-	16-byte encrypted, shifted NFC device random number RndA'	16 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4-bit

Table 50. AUTHENTICATE part 2 timing

These times exclude the end of communication of the NFC device.

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
AUTHENTICATE part 2	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	10 ms

10.7 READ_SIG

The READ_SIG command returns an IC-specific, 48 byte ECC signature, to verify the originality signature with the public key. The signature is pre-programmed at chip production and can be changed (see Section 10.8) if the originality signature has been unlocked with the LOCK_SIG command (see Section 10.9). The command structure is shown in Figure 16 and Table 51.

Table 53 shows the required timing.

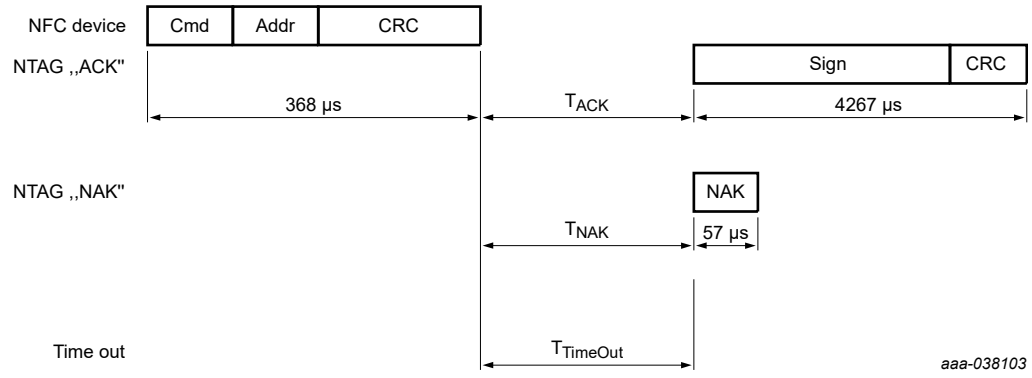


Figure 16. READ_SIG command

Table 51. READ_SIG command

Name	Code	Description	Length
Cmd	3Ch	read ECC signature	1 byte
Addr	00h	RFU, is set to 00h	1 byte
CRC	-	CRC according to [1]	2 bytes

Table 52. READ_SIG response

Name	Code	Description	Length
Signature	-	ECC signature	48 bytes
CRC	-	CRC according to [1]	2 bytes
NAK	see Table 25	see Section 9.3	4 bits

Table 53. READ_SIG timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ_SIG	n=9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 9.2.

Details on how to check that the signature value is provided in the following Application note ([5]).

10.8 WRITE_SIG

The WRITE_SIG command allows the writing of a customized originality signature into the dedicated originality signature memory.

The WRITE_SIG command requires an originality signature block address (see Table 57), and writes 4 bytes of data into the addressed originality signature block. The WRITE_SIG command is shown in Figure 17 and Table 54.

Table 56 shows the required timing.

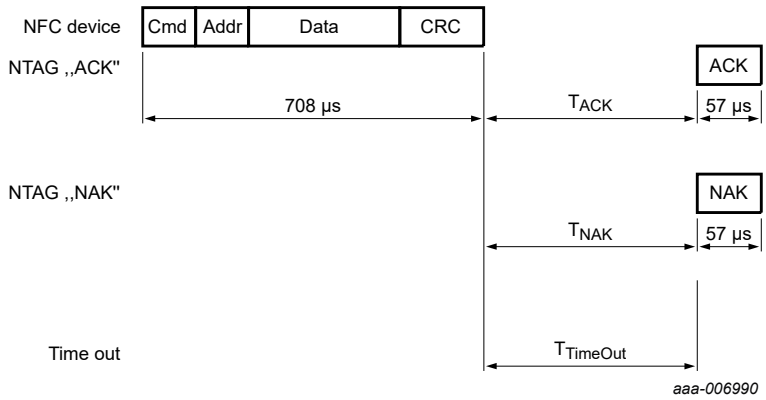


Figure 17. WRITE_SIG command

Table 54. WRITE_SIG command

Name	Code	Description	Length
Cmd	A9h	write one originality signature block	1 byte
Addr	-	block address	1 byte
Data	-	signature bytes to be written	4 bytes
CRC	-	CRC according to [1]	2 bytes

Table 55. WRITE_SIG response

Name	Code	Description	Length
ACK/NAK	see Table 25	see Section 9.3	4 bits

Table 56. WRITE_SIG timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE_SIG	n = 9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 9.2.

In the initial state of NTAG 224 DNA, the originality signature block address 00h to 0Bh are valid Addr parameters to the WRITE_SIG command.

Addressing a memory block beyond address 0Bh results in a NAK response from NTAG 224 DNA.

Table 57. Blocks for the WRITE_SIG command

Originality signature block	byte 0	byte 1	byte 2	byte 3
00h	LSByte			
01h				
...				
0Ah				
0Bh				MSByte

10.9 LOCK_SIG

The LOCK_SIG command allows the user to unlock, lock or permanently lock the dedicated originality signature memory.

The originality signature memory can only be unlocked if the originality signature memory is not permanently locked.

Permanently locking of the originality signature with the LOCK-SIG command is irreversible and the originality signature memory can never be unlocked and reprogrammed again.

The LOCK_SIG command is shown in Figure 18 and Table 58.

Table 60 shows the required timing.

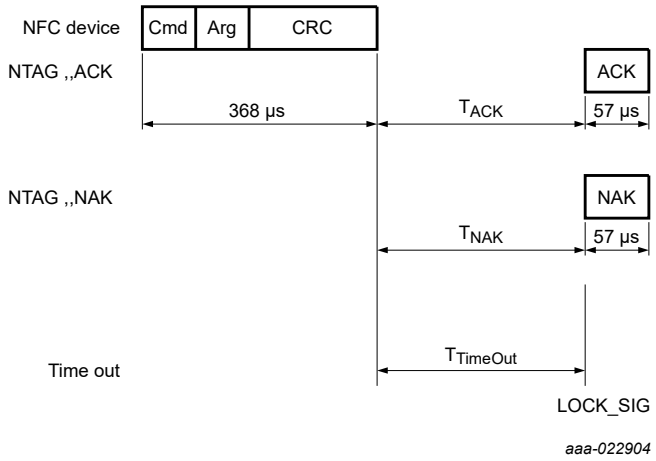


Figure 18. LOCK_SIG command

Table 58. LOCK_SIG command

Name	Code	Description	Length
Cmd	ACh	lock signature	1 byte
Arg	-	locking action	1 byte
		00h - unlock	
		01h - lock	
		02h - permanently lock	
CRC	-	CRC according to [1]	2 bytes

Table 59. LOCK_SIG response

Name	Code	Description	Length
ACK/NAK	see Table 25	see Section 9.3	4 bits

Table 60. LOCK_SIG timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
LOCK_SIG	n = 9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 9.2.

11 Limiting values

Stresses exceeding one or more of the limiting values can cause permanent damage to the device. Exposure to limiting values for extended periods can affect device reliability.

Table 61. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter		Min	Max	Unit
$P_{d,max}$	maximum power dissipation		-	120	mW
$I_{LA-LB,max}$	maximum input current		-	40	mA
T_{stg}	storage temperature		-55	125	°C
T_{amb}	ambient temperature		-25	+70	°C
V_{ESD}	electrostatic discharge voltage on LA/LB, DP/GND	[1]	-	2	kV

[1] ANSI/ESDA/JEDEC JS-001; Human body model: C = 100 pF, R = 1.5 kΩ

CAUTION

This device has limited built-in ElectroStatic Discharge (ESD) protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

12 Characteristics

Table 62. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_i	input frequency		-	13.56	-	MHz
C_i	input capacitance[1]	T_{amb} = 25 °C	-	50.0	-	pF
EEPROM characteristics						
t_{ret}	retention time	T_{amb} = 22 °C	10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C	100.000	-	-	cycle

[1] f_i = 13.56 MHz; 2.2 V RMS

13 Wafer specification

For more details on the wafer delivery forms, see [6].

Table 63. Wafer specifications NTAG 224 DNA

Wafer	
diameter	200 mm typical (8 inches)
maximum diameter after foil expansion	210 mm
thickness	
NT2H2421G0DUD	120 µm ± 15 µm
NT2H2421G0DUF	75 µm ± 10 µm
flatness	not applicable
Potential Good Dies per Wafer (PGDW)	42521
Wafer backside	
material	Si
treatment	ground and stress relieve
roughness	R_a max = 0.5 µm
	R_t max = 5 µm
Chip dimensions	
step size[1]	x = 832 µm
	y = 832 µm
gap between chips[1]	typical = 20 µm
	minimum = 5 µm
Passivation	
type	sandwich structure
material	PSG / nitride
thickness	500 nm / 600 nm
Au bump (substrate connected to VSS)	
material	> 99.9 % pure Au
hardness	35 to 80 HV 0.005
shear strength	> 70 MPa
height	18 µm
height uniformity	within a die = ±2 µm
	within a wafer = ±3 µm
	wafer to wafer = ±4 µm
flatness	minimum = ±1.5 µm
size	LA, LB, GND, TP = 80 µm × 80 µm
size variation	±5 µm
under bump metallization	sputtered TiW

[1] The step size and the gap between chips may vary due to changing foil expansion

13.1 Fail die identification

Electronic wafer mapping covers the electrical test results and additionally the results of mechanical/visual inspection. No ink dots are applied.

14 Delivery

The customer purchasing a product of the NTAG 224 DNA family has to make sure that they receive the evaluated version. This section describes the measures that are needed to ensure delivery of the evaluated version.

The evaluated version of the NTAG 224 DNA can be ordered from NXP by referencing the respective commercial type name as listed in Section 5.

NXP offers two ways of delivery of the product:

1. The customer collects the product themselves at the NXP site.
2. The product is sent by NXP to the customer and protected by special measures.

These methods are described in Section 14.2 and Section 14.3 respectively.

14.1 Delivery as a wafer

When the product is delivered as wafer, there reside functional and non-functional ICs on the wafer. The non-functional ICs cannot be used but have to be handled securely, too. These ICs must be destroyed to such an extent that no analysis or misuse is possible after destruction. The non-functional ICs (scrap) shall be handled secure until the destruction.

Information about non-functional items is accessible via the eMAP-Portal (http://wmt.nxp.com). The Access sheet with the Login data is enclosed with the delivery to allow the download of the electronic wafer map file. In this case, the information about non-functional ICs is stored in a so-called wafer map file. The electronic wafer map file covers the electrical test results and additionally the results of mechanical/visual inspection.

14.2 Delivery Method One: The customer collects the product themselves

The customer fetches the product from the following location:

NXP Semiconductors (Thailand)

303 Chaengwattana Rd.Laksi

Bangkok

10210 Thailand

This method guarantees that the customer gets authentic products.

14.3 Delivery Method Two: The Product is sent by NXP and protected by special measures

To guarantee that the product is not manipulated during the delivery, NXP has defined three security measures:

1. The product is delivered in parcels sealed with special tapes. The customer can examine these tapes in order to make sure that they have not been manipulated.
2. The customer shall identify the product as described in Section 10.1.
3. The customer should check the originality by verification of the Originality Signature Section 8.10.1.

These measures shall be applied to ensure that a genuine chip is in use. The product is delivered directly to the customer or via the Global Distribution Center:

NXP Semiconductors Netherlands B.V.

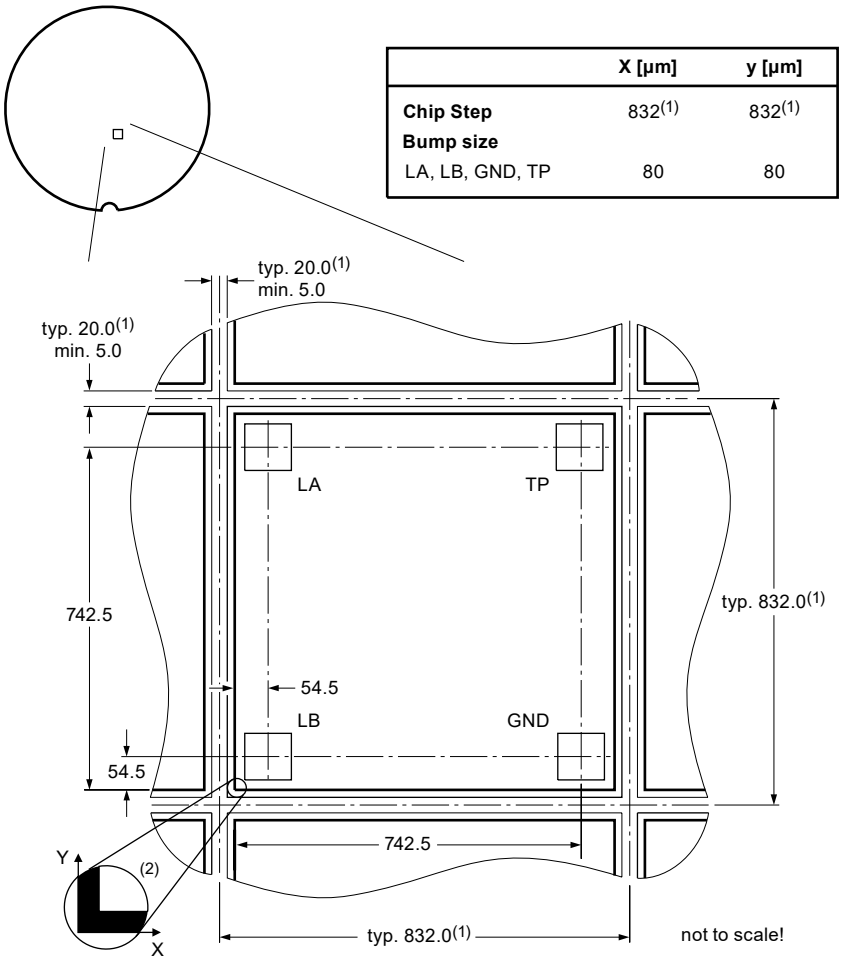
(Global Distribution Centre)

c/o CEVA Logistics (Malaysia) Sdn Bhd

Lot 9A Jalan Tiang U8/92, Bukit Jelutong Industrial Park, 40150 Shah Alam, Selangor Darul Ehsan, MALAYSIA

15 Bare die outline

For more details on the wafer delivery forms, see [6].



(1) the air gap and thus the step size may vary due to varying foil expansion
(2) all dimensions in µm, pad locations measured from metal ring edge (see detail)

aaa-050978

Figure 19. Bare die outline NTAG 224 DNA

16 Abbreviations

Table 64. Abbreviations and symbols

Acronym	Description
ACK	Acknowledge
ATQA	Answer to request, Type A
CRC	Cyclic Redundancy Check
CC	Capability container
CT	Cascade Tag (value 88h) as defined in ISO/IEC 14443-3 Type A
ECC	Elliptic Curve Cryptography
EEPROM	Electrically Erasable Programmable Read-Only Memory
FDT	Frame Delay Time
FFC	Film Frame Carrier
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
NAK	Not Acknowledge
NFC device	NFC Forum device
NFC tag	NFC Forum tag
NV	Non-Volatile memory
REQA	Request command, Type A
RF	Radio Frequency
RFUI	Reserver for Future Use - Implemented
RMS	Root Mean Square
SAK	Select acknowledge, type A
SECS-II	SEMI Equipment Communications Standard part 2
TiW	Titanium Tungsten
UID	Unique IDentifier
WUPA	Wake-up Protocol type A

17 References

[1] **ISO/IEC 14443** - International Organization for Standardization

[2] **NFC Forum Tag 2 Type Operation, Technical Specification** - NFC Forum, 31.05.2011, Version 1.1

[3] **NFC Data Exchange Format (NDEF), Technical Specification** - NFC Forum, 24.07.2006, Version 1.0

[4] **AN11276 NTAG Antenna Design Guide** - Application note, Document number 2421**[1]

[5] **AN11350 NTAG Originality Signature Validation** - Application note, Document number 2604**[1]

[6] **General specification for 8" wafer on UV-tape; delivery types** - Delivery Type Description, Document number 1005**[1]

[7] **Certicom Research. SEC 2** - Recommended Elliptic Curve Domain Parameters, version 2.0, January 2010

[8] **NIST Special Publication 800-38A** - National Institute of Standards and Technology (NIST). Recommendation for BlockCipher Modes of Operation.

[9] **NIST Special Publication 800-38B** - National Institute of Standards and Technology (NIST). Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication. https://csrc.nist.gov/publications/detail/sp/800-38b/final

[10] **ISO/IEC 10116: Information technology - Security techniques - Modes of operation for an n-bit block cipher** - International Organization for Standardization, 2017

1 ** ... document version number

18 Revision history

Table 65. Revision history

Document ID	Release date	Data sheet status	Supersedes
NT2H2421G0 v.3.1	20230405	Product data sheet	NT2H2421G0 v.3.0
Modifications:	• Bump size changed from 60 µm to 80 µm in Section 13 and Figure 19		
NT2H2421G0 v.3.0	20220218	Product data sheet	NT2H2421G0 v.2.0
Modifications:	• Data sheet status changed to "Product data sheet", security status changed to "Company public"		
NT2H2421G0 v.2.0	20220205	Preliminary data sheet	NT2H2421G0 v.1.1
Modifications:	• Editorial changes		
NT2H2421G0 v.1.1	20211220	Objective data sheet	NT2H2421G0 v.1.0
Modifications:	• Updated section "General description" (see Section 1) • Updated section "Applications" (see Section 3) • PGDW updated in section "Wafer specification" (see Table 63)		
NT2H2421G0 v.1.0	20211125	Objective data sheet	NT2H2421G0 v.0.4
Modifications:	• General update		
NT2H2421G0 v.0.4	20201028	Objective data sheet	
Modifications:	• First draft		

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

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Tables

Figures

Contents

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