NTP5210

NTAG 5 switch - NFC Forum-compliant PWM and GPIO bridge

Rev. 1.0 — 28 May 2019 Objective short data sheet
547710 COMPANY PUBLIC

1 General description

NTAG 5 switch is designed as an MCU replacement in gaming, lighting, and smart-factory applications. This NFC tag adds connectivity and increases flexibility while saving energy and lowering the bill of materials.

With its GPIO and PWM functionality, the tag fits perfectly in gaming, lighting and smart factory applications.

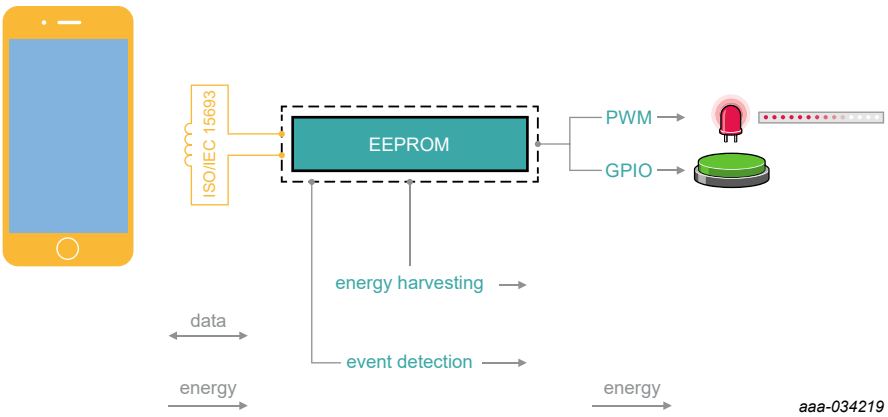


Figure 1. NTAG 5 switch overview

To fulfill security requirements, the tag offers data protection based on plain password authentication. An elliptice curve based, re-programmable originality signature can be used to verify the origin of the product.

For low power budget requirement applications, NTAG 5 switch features energy harvesting capability with a regulated output as well as a very low power consumption host interface with standby mode and hard power down capability.

GPIOs or PWM output channels and a configurable event detection pin complete the host interface.

The tag is offered with a large choice of delivery forms like XQFN16, TSSOP16 or SO8 package as well as bare die.

2 Features and benefits

- Interoperable and high performance NFC interface
  - ISO/IEC 15693 and NFC Forum Type 5 Tag compliant
  - 64-bit Unique Identifier
- Reliable and robust memory
  - 512 bytes (4096 bits) user EEPROM on top of configuration memory
  - 40 years data retention
  - Write endurance of 1 000 000 cycles
- Configurable contact interface
  - One configurable event detection pin
  - Two GPIOs
  - Two Pulse Width Modulation (PWM) channels as multiplexed GPIOs and/or ED pin
  - 1.8 V to 5 V supply voltage
- Scaleable security for access and data protection
  - Read only protection as defined in NFC Forum Type 5 Tag specification
  - Full, read-only, or no memory access based on 32-bit password
  - Optional 64-bit password protection
  - ECC based cutomizable originality signature
- Low power budget application support
  - Energy harvesting with regulated output voltage
  - Low power stand-by current <6 µA
  - Hard power down current <0.25 µA
- Very robust architecture
  - -40°C to 105°C operating temperature
- Extensive product support package
  - Feature specific application notes
  - Development board
  - Software
  - Hands-on training

3 Applications

- Use cases
  - Authenticity check and data protection
  - Late "in the box" configuration
  - LED driver configuration
  - GPIO
- Applications
  - Lighting
  - Smart home
  - Industrial
  - Gaming

4 Quick reference data

Table 1. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General							
f_i	input frequency	ISO/IEC 15693		13.553	13.56	13.567	MHz
Operating conditions							
T_{amb}	ambient temperature			-40	25	105	°C
V_{CC}	supply voltage	on pin V_{CC}		1.62	-	5.5	V
Current consumption							
I_{VCC}	V_{CC} supply current	V_{CC} = 1.8V		-	150	-	µA
Energy harvesting VOUT pad							
V_{out}	output voltage	configurable load current 0.3mA to 10mA		1.8	-	3.0	V
C_L	load capacitance	needs to come from calculation		-	1.1	-	µF

5 Ordering information

Table 2. Ordering information

Type number	Package Name	Description
NTP52101G0JHK	XQFN16	Type 5 Tag with GPIOs, PWM and 512 bytes user EEPROM
NTP52101G0JTT	TSSOP16	Type 5 Tag with GPIOs, PWM and 512 bytes user EEPROM
NTP52101G0JT	SO8	Type 5 Tag with GPIOs, PWM and 512 bytes user EEPROM
NTP52101G0FUA	Wafer	Type 5 Tag with GPIOs, PWM and 512 bytes user EEPROM

6 Block diagram

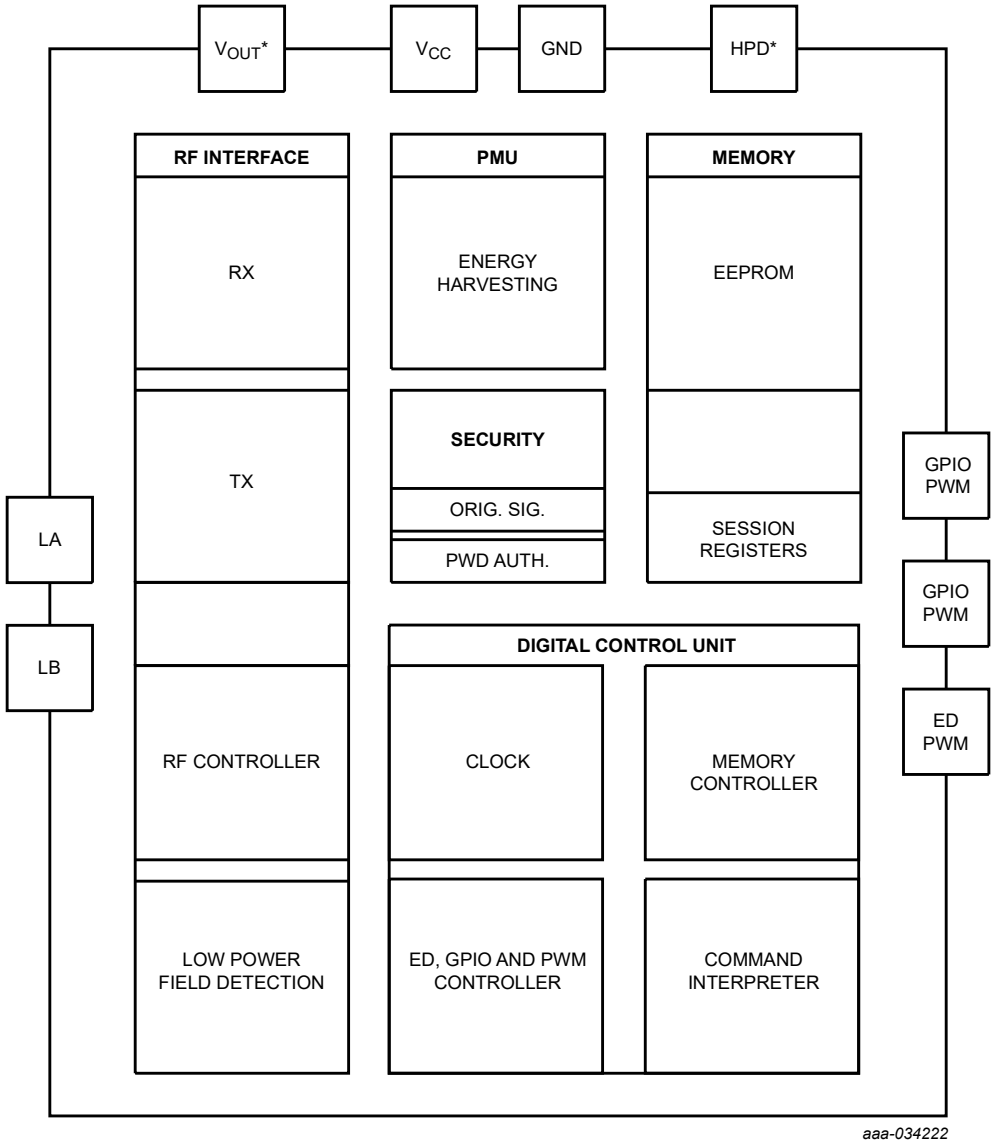
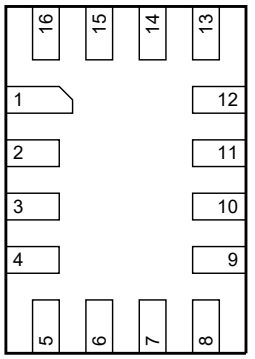


Figure 2. Block diagram NTAG 5 switch

7 Pinning Information



Transparent top view

Figure 3. Pin configuration for XQFN16 package

Table 3. Pin description for XQFN16

Pin	Symbol	Description	When unused
1	GND	Ground	connect to GND
2	GND	Ground	connect to GND
3	N.C.	not connected	keep floating
4	N.C.	not connected	keep floating
5	N.C.	not connected	keep floating
6	GPIO1/PWM1	Multiplexed GPIO1 and PWM1	keep floating
7	GPIO0/PWM0	Multiplexed GPIO0 and PWM0	keep floating
8	ED/PWM0	Multiplexed event detection and PWM0	keep floating
9	V_{CC}	External power supply	keep floating
10	HPD	Hard power down	keep floating
11	GND	Ground	connect to GND
12	V_{OUT}	Energy harvesting voltage output	keep floating
13	N.C.	not connected	keep floating
14	LB	Antenna connection	keep floating
15	LA	Antenna connection	keep floating
16	N.C.	not connected	keep floating

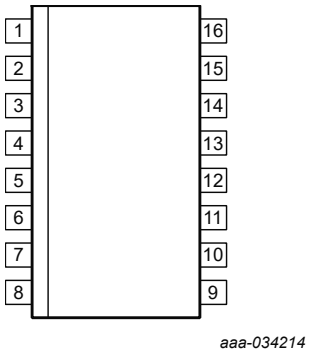


Figure 4. Pin configuration for TSSOP16 package

Table 4. Pin description for TSSOP16

Pin	Symbol	Description	When unused
1	LA	Antenna connection	keep floating
2	N.C.	not connected	keep floating
3	GND	Ground	connect to GND
4	GND	Ground	connect to GND
5	N.C.	not connected	keep floating
6	N.C.	not connected	keep floating
7	N.C.	not connected	keep floating
8	GPIO1/PWM1	Multiplexed GPIO1 and PWM1	keep floating
9	GPIO0/PWM0	Multiplexed GPIO0 and PWM0	keep floating
10	ED/PWM0	Multiplexed event detection and PWM0	keeep floating
11	V_{CC}	External power supply	keep floating
12	HPD	Hard power down	keep floating
13	GND	Ground	connect to GND
14	V_{OUT}	Energy harvesting voltage output	keep floating
16	LB	Antenna connection	keep floating

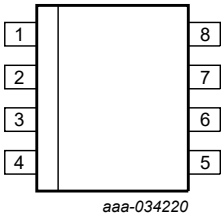


Figure 5. Pin configuration for SO8 package

Table 5. Pin description for SO8

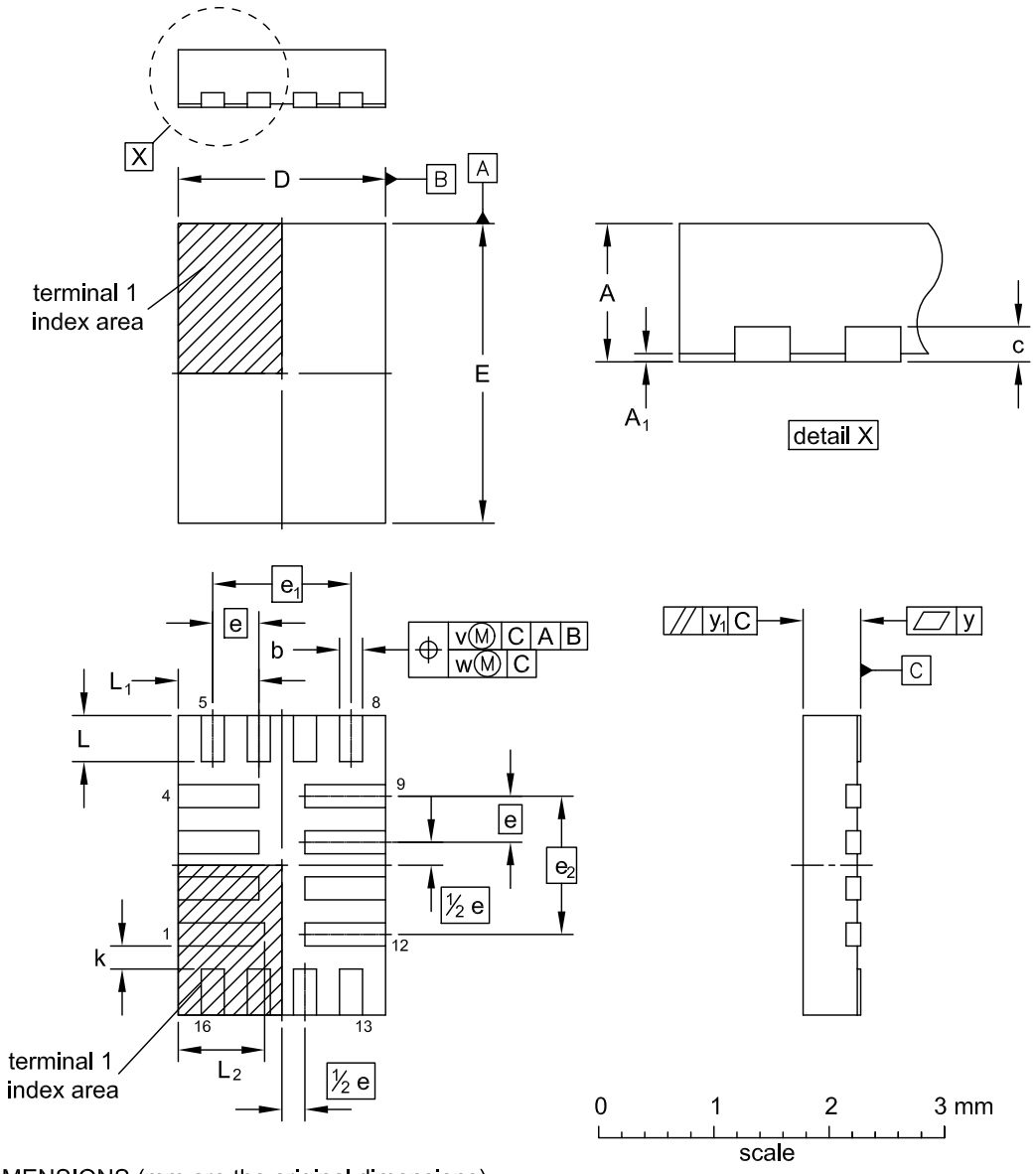
Pin	Symbol	Description	When unused
1	GND	Ground	connect to GND
2	LA	Antenna connection	keep floating
3	LB	Antenna connection	keep floating
4	GND	Ground	connect to GND
5	GPIO1/PWM1	Multiplexed GPIO1 and PWM1	keep floating
6	GPIO0/PWM0	Multiplexed GPIO0 and PWM0	keep floating
7	ED/PWM0	Multiplexed event detection and PWM0	keep floating
8	V_{CC}	External power supply	keep floating

8 Limiting values

Table 6. Limiting values In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature	all packages		-65	+150	°C
T_j	junction temperature				+125	°C
V_{ESD}	electrostatic discharge voltage	Charge Device Model		-2	2	kV
		Human Body Model		-2	2	kV
V_i	supply voltage	on pin V_{CC}		-0.5	7.15	V
V_i	input voltage	on pin ED,HPD		-0.5	7.15	V
V_i	RF input voltage	on pin LA/LB		-0.5	5.6	Vp
V_i	input voltage	on pin LA; LB is 0V; sine wave of 13.56 MHz		-0.5	5.2	Vp
V_i	input voltage	on pin LB; LA is 0V; sine wave of 13.56 MHz		-0.5	5.2	Vp
$I_{i(max)}$	maximum input current	La/Lb;peak		-168	168	mA

9 Package outline



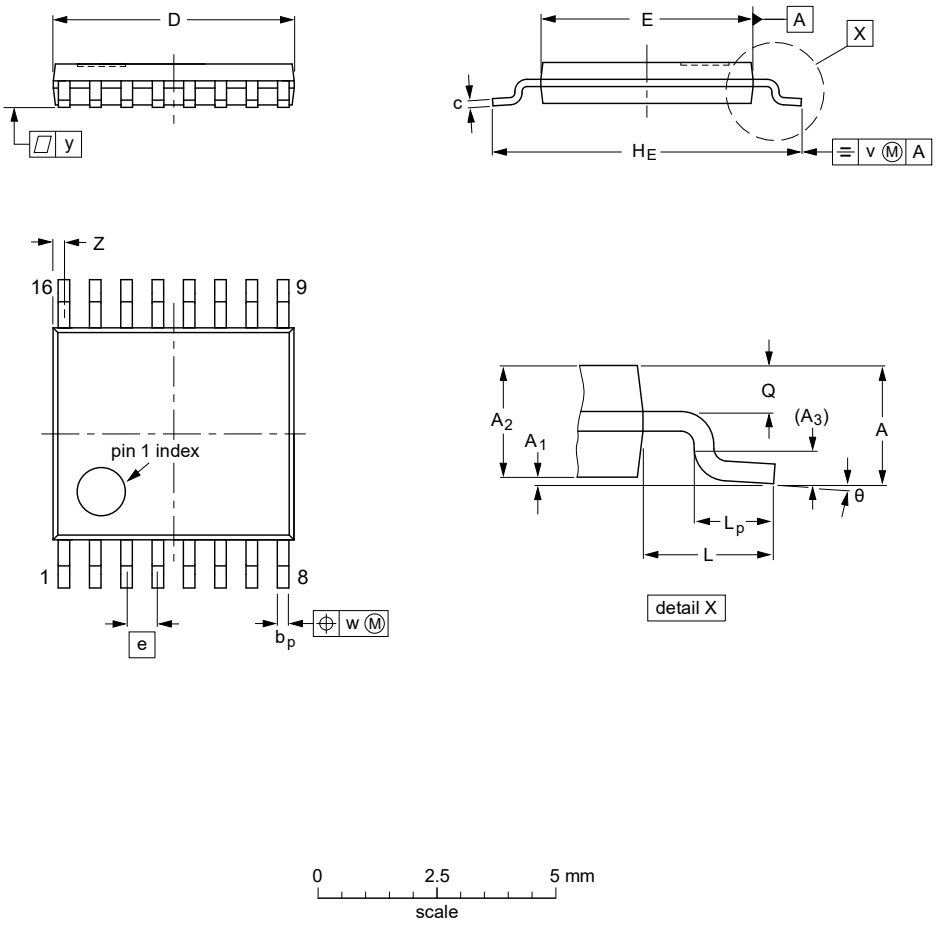
DIMENSIONS (mm are the original dimensions)

UNIT		$A^{(1)}$	A_1	b	c	$D^{(1)}$	$E^{(1)}$	e	e_1	e_2	k	L	L_1	L_2	v	w	y	y_1
mm	MAX	0.50	0.05	0.25		1.90	2.70					0.45	0.75	0.80				
	NOM			0.20	0.127	1.80	2.60	0.40	1.20	1.20	0.2	0.40	0.70	0.75	0.1	0.05	0.05	0.1
	MIN		0.00	0.15		1.70	2.50					0.35	0.65	0.70				

Notes
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

Figure 6. Package outline XQFN16

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

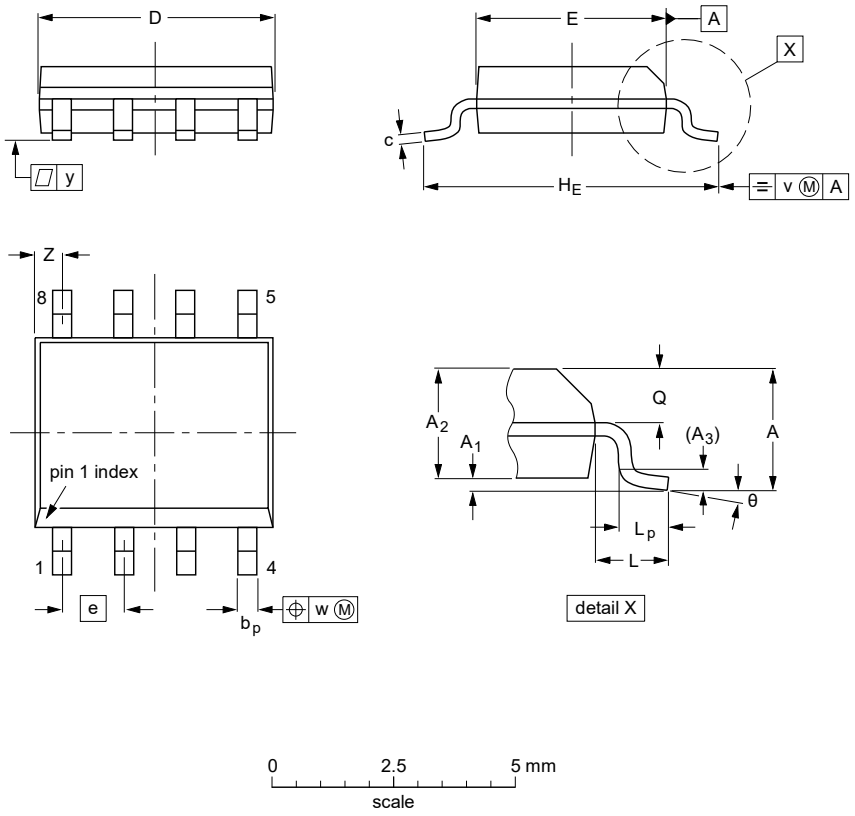
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 7. Package outline TSSOP16

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 8. Package outline SO8

10 References

[1] NFC Forum Type 5 Tag Specification

[2] ISO/IEC 15693

[3] AN11203 - NTAG 5 Use of PWM, GPIO and Event detection

[4] AN12364 - NTAG 5 Bi-directional data exhange

[5] AN12365 - NTAG 5 How to use energy harvesting

[6] AN12366 - NTAG 5 Memory Configuration and Scalable Security

[7] AN12368 - NTAG 5 Link I²C Master mode

[8] AN12369 - NTAG 5 Use of High datarates

[9] AN12428 - NTAG 5 design recommendations for FCC and CE certifications

[10] AN12429 - NTAG 5 Stand-by and Hard Power down modes of operation

[11] ANxxxxx - NTAG 5 General Application Circuit

[12] ANxxxxx - Antenna Design Guide

11 Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTP5210_SDS v.1.0	20190528	Objective short data sheet		-
	• Initial Version			

12 Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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