

# NWP2081T

## Half-bridge driver IC

Rev. 1 — 3 September 2013

Product data sheet

### 1. General description

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The NWP2081T is a high-voltage monolithic integrated circuit made using the latch-up free Silicon-On-Insulator (SOI) process. The circuit is designed for driving MOSFETs in a half-bridge configuration.

### 2. Features and benefits

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- Latch-up free and robust half-bridge driver
- Output driver capability:  $I_{O(\text{sink})} = 400 \text{ mA}$  and  $I_{O(\text{source})} = 200 \text{ mA}$
- Maximum frequency 800 kHz
- Outputs in phase with CLK input
- Adjustable dead-time
- Low active shutdown input

### 3. Applications

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- Driver (via external MOSFETs) for any kind of load in a half-bridge configuration

### 4. Ordering information

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Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NWP2081T	SO8	plastic small outline package; 8 leads	SOT96-1



## 5. Block diagram

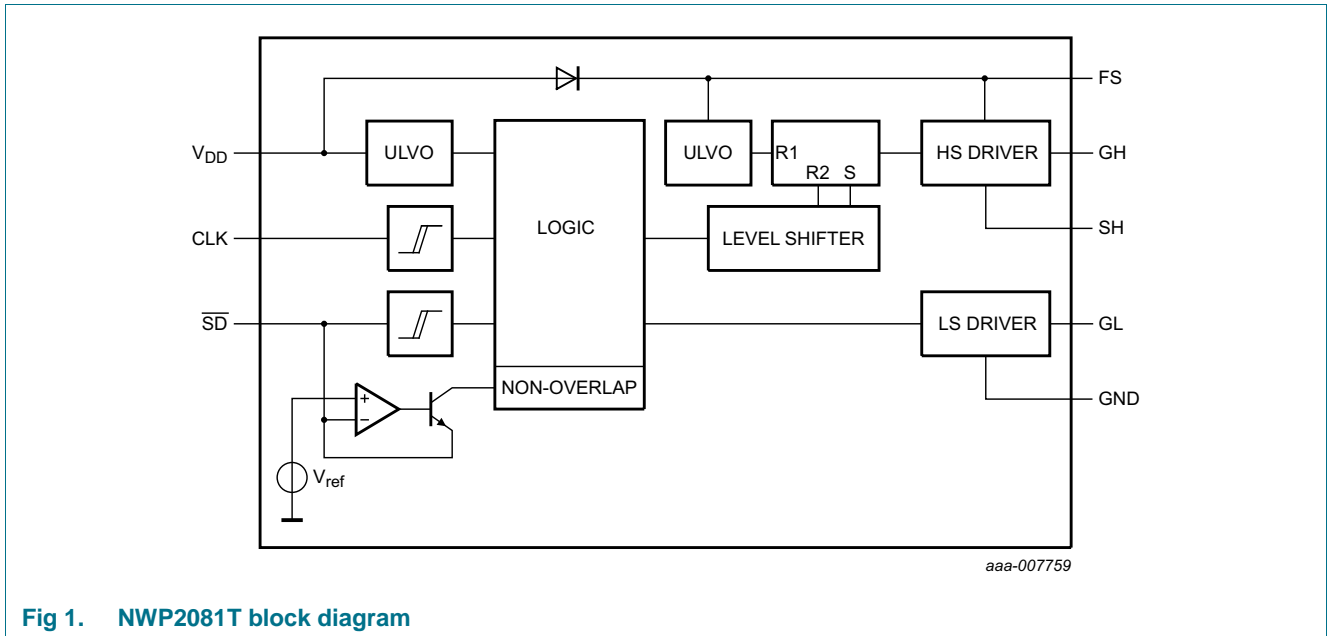


Fig 1. NWP2081T block diagram

Refer to [Figure 4](#) for detailed information on the required application components.

## 6. Pinning information

### 6.1 Pinning

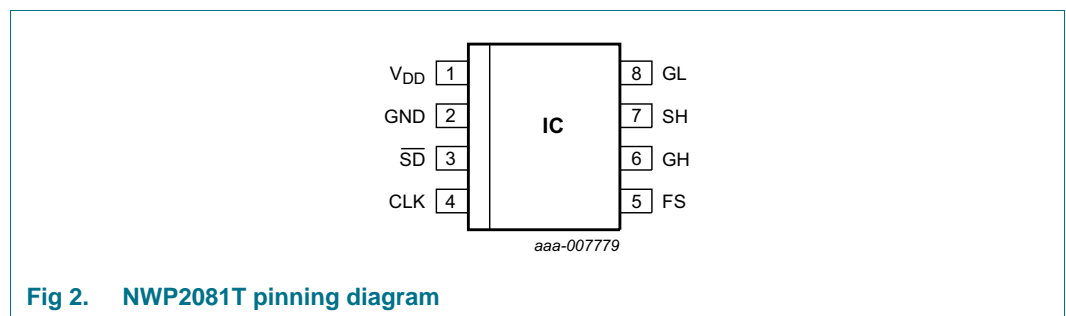


Fig 2. NWP2081T pinning diagram

### 6.2 Pin description

Table 2. Pin description NWP2081T

Symbol	NWP2081T (SO8)	Description
V <sub>DD</sub>	1	IC supply
GND	2	IC ground and low-side driver return
$\overline{SD}$	3	low active analog shutdown input and non-overlap time setting
CLK	4	clock logic input
FS	5	floating supply voltage

Table 2. Pin description NWP2081T ...continued

Symbol	NWP2081T (SO8)	Description
GH	6	high-side MOSFET gate
SH	7	high-side MOSFET source
GL	8	low-side MOSFET gate

## 7. Functional description

### 7.1 Start-up state

The IC enters the start-up state when the supply voltage on pin  $V_{DD}$  increases. In the start-up state, the high-side power transistor is non-conducting and the low-side power transistor is switched on. The internal circuit is reset and the capacitor on the bootstrap pin FS is charged. The start-up state is defined until the value of  $V_{DD} =$  the  $V_{DD(start)}$  value. After which the IC switches to the oscillation state.

The circuit enters the start-up state again when the voltage on pin  $V_{DD} < V_{DD(stop)}$ .

### 7.2 NWP2081T oscillation state

In the oscillation state, the output voltage of the GL and GH drivers depend on the logical signals CLK and  $\overline{SD}$  (see [Table 3](#)).

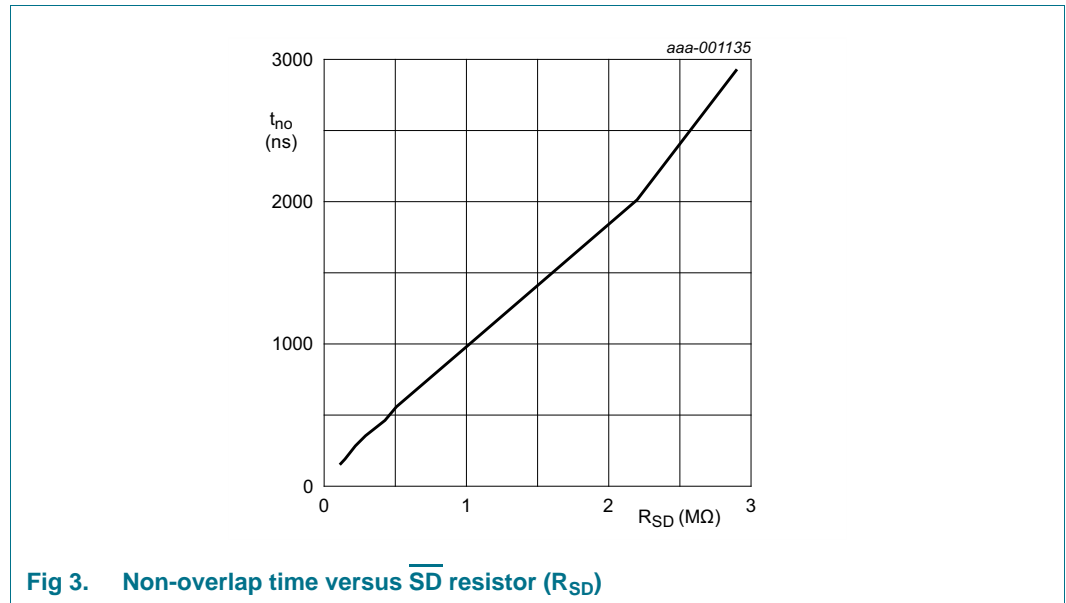
Table 3. NWP2081T logic table

State	CLK	$\overline{SD}$	GH	GL
start-up	-	-	LOW	HIGH
oscillation	0	1	LOW	HIGH
oscillation	1	1	HIGH	LOW
oscillation	0	0	LOW	LOW
oscillation	1	0	LOW	LOW

**7.3 NWP2081T non-overlap time**

The external resistor ( $R_{SD}$ ) on pin  $\overline{SD}$  sets the non-overlap time of the NWP2081T. The relationship between this resistor value and actual dead-time is listed in [Figure 3](#).

It is essential to add a 10 nF to 100 nF decoupling capacitor across  $R_{SD}$  to ensure a noise immune dead-time system.



**Fig 3. Non-overlap time versus  $\overline{SD}$  resistor ( $R_{SD}$ )**

**7.4 NWP2081T shutdown protection**

When the voltage at pin  $\overline{SD}$  is pulled below  $V_{IH}$ , the internal sink drivers of the pins GL and GH are immediately enabled to switch off the external power MOSFETs.

The shutdown comparator has a hysteresis of  $V_{hys(SD)}$  to avoid multiple switching.

Preferably, pin  $\overline{SD}$  is pulled low via a collector of a transistor (see [Figure 4](#)) to avoid loading of this pin (Influences the non-overlap time settings) at normal operation.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage	nominal	0	15.5	V
V <sub>FS</sub>	voltage on pin FS		V <sub>SH</sub>	V <sub>SH</sub> + 15.5	V
V <sub>SH</sub>	voltage on pin SH	source high-side MOSFET	-3	+600	V
		t < 1 μs	-14	+600	V
V <sub>CLK</sub>	voltage on pin CLK	logic input for output drivers	0	15.5	V
V <sub>i(SD)</sub>	input voltage on pin $\overline{SD}$	logic input for output drivers and analog input for non-overlap setting	0	15.5	V
SR	slew rate	on pin SH; repetitive	-6	+6	V/ns
T <sub>j</sub>	junction temperature		-40	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
V <sub>ESD</sub>	electrostatic discharge voltage	human body model:	<a href="#">[1]</a>		
		pins FS, GH and SH	-	1	kV
		pins V <sub>DD</sub> , $\overline{SD}$ , CLK, and GL	-	2	kV
		charge device model:	<a href="#">[2]</a>		
	all pins	-	500	V	

[1] In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] In accordance with the Charged Device Model (CDM): equivalent to discharging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

## 9. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
<b>SO8</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	<a href="#">[1]</a> 160	K/W

[1] In accordance with IEC 60747-1.

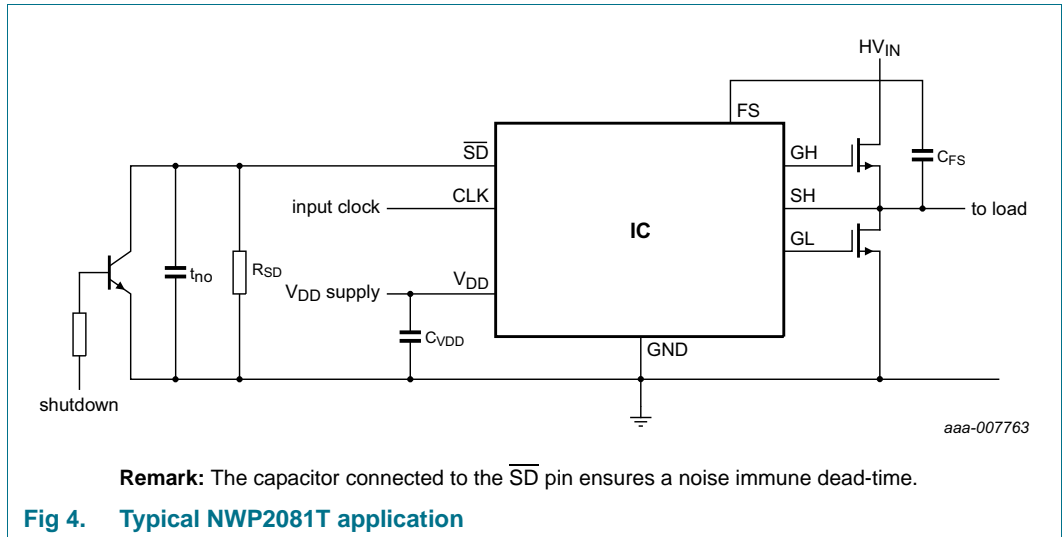
## 10. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ }^\circ\text{C}$ ; all voltages are measured with respect to SGND;  $V_{DD} = 12.8\text{ V}$ ; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>High-voltage supply</b>						
$I_{leak}$	leakage current	FS = GH = SH = 600 V	-	-	10	$\mu\text{A}$
<b>Start-up state</b>						
$I_{VDD}$	current on pin $V_{DD}$		420	520	620	$\mu\text{A}$
$V_{DD(start)}$	start supply voltage		9	10	11	V
$V_{DD(stop)}$	stop supply voltage		8	8.5	9	V
$V_{DD(hys)}$	hysteresis of supply voltage	start-to-stop	1	1.5	2	V
<b>Pin CLK input</b>						
$V_{IH}$	HIGH-level input voltage		2.7	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{I(CLK)}$	input current on pin CLK		-	0	1	$\mu\text{A}$
<b>Pin SD input</b>						
$V_{IH}$	HIGH-level input voltage	to activate shutdown	1.6	2.2	2.8	V
$V_{hys(SD)}$	hysteresis voltage on pin $\overline{SD}$		-	400	-	mV
$t_{no}$	non-overlap time	$R_{SD} = 100\text{ k}\Omega$ ; typical minimum	-	140	-	ns
		$R_{SD} = 3\text{ M}\Omega$ ; typical maximum	-	2.4	-	$\mu\text{s}$
<b>Gate drivers</b>						
$I_{O(source)}$	output source current	$V_{FS} = V_{VDD} = 12\text{ V}$ ; $V_{SH} = 0\text{ V}$ ; $V_{GH} = V_{GL} = 8\text{ V}$	-	200	-	mA
$I_{O(sink)}$	output sink current	$V_{FS} = V_{VDD} = 12\text{ V}$ ; $V_{SH} = 0\text{ V}$ ; $V_{GH} = V_{GL} = 4\text{ V}$	-	400	-	mA
$V_{d(bs)}$	bootstrap diode voltage	$I_{d(bs)} = 20\text{ mA}$	-	2.3	-	V
$V_{UVLO}$	undervoltage lockout voltage	reset	3.6	4.2	4.8	V
$I_{FS}$	current on pin FS	$V_{FS} = V_{VDD} = 12\text{ V}$ ; $V_{SH} = 0\text{ V}$	27	32	37	$\mu\text{A}$
$f_{max}$	maximum frequency		800	-	-	kHz

11. Application information



12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

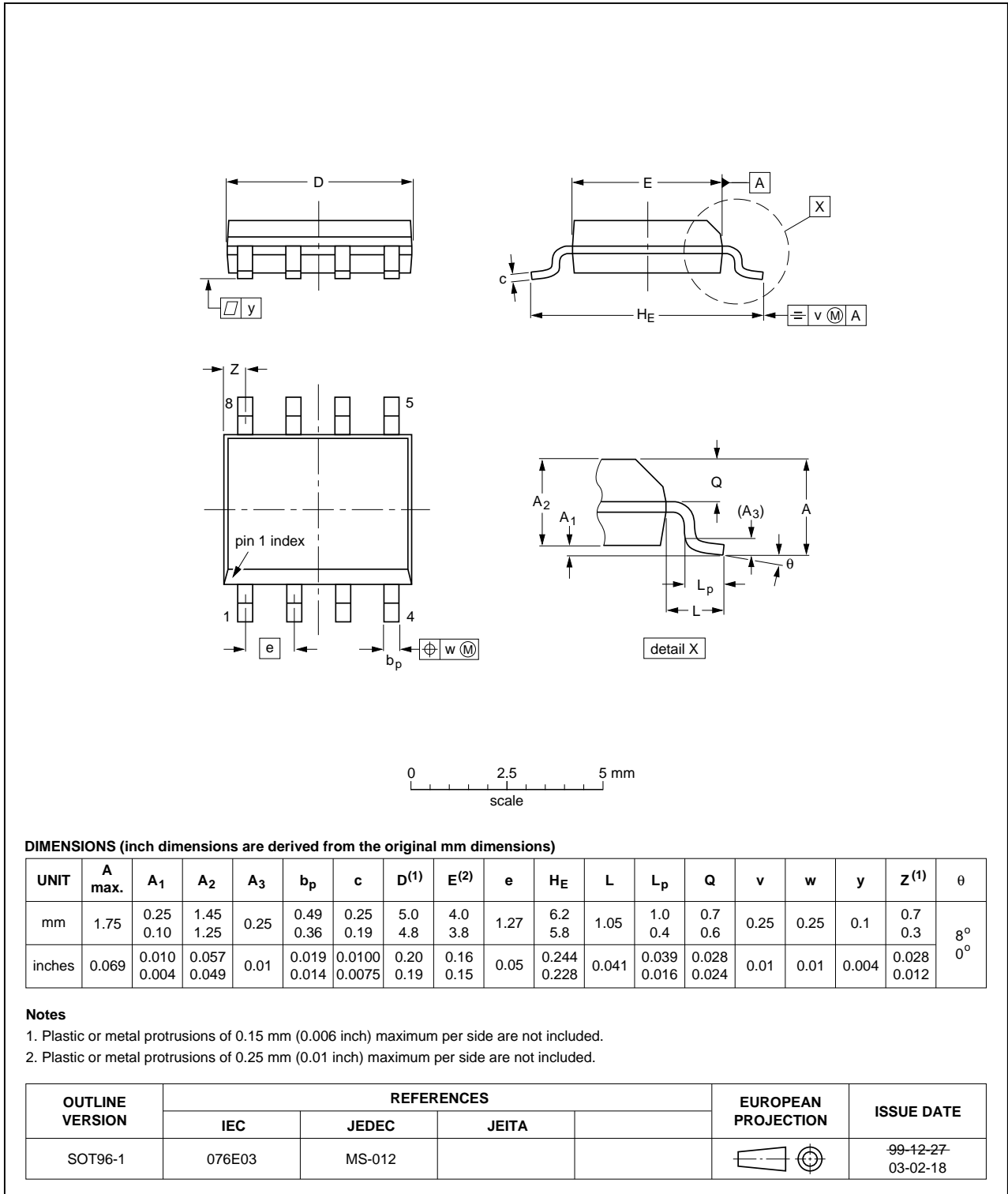


Fig 5. Package outline SOT96-1 (SO8)



## 13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NWP2081T v.1	20130903	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## 16. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>1</b>
<b>4</b>	<b>Ordering information</b> .....	<b>1</b>
<b>5</b>	<b>Block diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>2</b>
6.1	Pinning .....	2
6.2	Pin description .....	2
<b>7</b>	<b>Functional description</b> .....	<b>3</b>
7.1	Start-up state .....	3
7.2	NWP2081T oscillation state .....	3
7.3	NWP2081T non-overlap time .....	4
7.4	NWP2081T shutdown protection .....	4
<b>8</b>	<b>Limiting values</b> .....	<b>5</b>
<b>9</b>	<b>Thermal characteristics</b> .....	<b>5</b>
<b>10</b>	<b>Characteristics</b> .....	<b>6</b>
<b>11</b>	<b>Application information</b> .....	<b>7</b>
<b>12</b>	<b>Package outline</b> .....	<b>8</b>
<b>13</b>	<b>Revision history</b> .....	<b>9</b>
<b>14</b>	<b>Legal information</b> .....	<b>10</b>
14.1	Data sheet status .....	10
14.2	Definitions .....	10
14.3	Disclaimers .....	10
14.4	Trademarks .....	11
<b>15</b>	<b>Contact information</b> .....	<b>11</b>
<b>16</b>	<b>Contents</b> .....	<b>12</b>

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