1. General description

The NX20P5090 is an advanced 5 A unidirectional power switch for USB PD. It includes under voltage lockout, over voltage lockout, reverse current protection and over-temperature protection circuits. It is designed to automatically isolate the power switch terminals when a fault condition occurs. Both VBUS and VINT pins have 29 V tolerance in shutdown mode. Two NX20P5090 chips can be used in parallel to support dual power inputs connecting to the same charging circuit.

The device has a default 23 V over voltage protection threshold, and the OVP threshold can be adjusted by using an external resistor divider on OVLO pin. A 15 ms de-bounce time is deployed every time before the device is switched ON, followed by a soft start to limit the inrush current.

Designed for operation from 2.5 V to 20 V, it is used in USB PD power control applications to offer essential protection and enhance system reliability.

NX20P5090 is offered in a small 15 bump, 2.56 x 1.54 x 0.555 mm WLCSP package.

2. Features and benefits

- Wide supply voltage range from 2.5 V to 20 V
- ISW maximum 5 A continuous current
- 29 V tolerance on both VBUS and VINT pin
- 30 mΩ (typical) Low ON resistance
- Adjustable VBUS over voltage protection
- Built in slew rate control for inrush current limit
- All time two level reverse-current protection
- Protection circuitry
  - Over-Temperature Protection
  - Over-Voltage Protection
  - Under-Voltage Lockout
  - Reverse Current Protection
- Surge protection:
  - IEC61000-4-5 exceeds ±90 V on VBUS without capacitor
  - IEC61000-4-5 exceeds ±100 V on VBUS with 22 uF capacitor
ESD protection
- IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
- HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
- CDM AEC standard Q100-01 (JESD22-C101E)
- Specified from –40 °C to +85 °C

3. Applications

- Smart and feature phones
- Tablets, eBooks
- Notebooks

4. Ordering information

Table 1. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Temperature range</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>NX20P5090UK</td>
<td>WLCSP15</td>
<td>–40 °C to +85 °C</td>
<td>wafer level chip-scale package; 15 bumps; 2.56 x 1.54 x 0.555 mm (Backside coating included)</td>
<td>SOT1392-1</td>
<td></td>
</tr>
</tbody>
</table>

4.1 Ordering options

Table 2. Ordering options

<table>
<thead>
<tr>
<th>Type number</th>
<th>Orderable part number</th>
<th>Package</th>
<th>Packing method</th>
<th>Minimum order quantity</th>
<th>Temperature range</th>
</tr>
</thead>
<tbody>
<tr>
<td>NX20P5090UK</td>
<td>NX20P5090UKAZ</td>
<td>WLCSP15</td>
<td>REEL 7&quot; Q2/T3  &quot;SPECIAL MARK CHIPS DP</td>
<td>3000</td>
<td>T_{amb} = –40 °C to +85 °C</td>
</tr>
</tbody>
</table>

5. Marking

Table 3. Marking

<table>
<thead>
<tr>
<th>Line</th>
<th>Marking</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>X20PPD</td>
<td>basic type name</td>
</tr>
<tr>
<td>B</td>
<td>mmmmmmmnn</td>
<td>wafer lot code (mmmmmm) and wafer number (nn)</td>
</tr>
<tr>
<td>C</td>
<td>ZtDYWW</td>
<td>manufacturing code: Z = foundry location, t = assembly location, D = RoHS code (dark green), YY = assembly year code, WW = assembly week code</td>
</tr>
</tbody>
</table>
6. Functional diagram

![Logic symbol](image1)

**Fig 1. Logic symbol**

![Logic diagram](image2)

**Fig 2. Logic diagram**

7. Pinning information

7.1 Pinning

![Pin configuration](image3)

**Fig 3. Pin configuration WLCSP15**

![Ball mapping](image4)

**Fig 4. Ball mapping for WLCSP15**

7.2 Pin description
Table 4. Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBUS</td>
<td>B2, C2, D2, E1, E2</td>
<td>VBUS (Power Input)</td>
</tr>
<tr>
<td>VINT</td>
<td>A1, B1, C1, D1</td>
<td>VINT (Power Output)</td>
</tr>
<tr>
<td>OVLO</td>
<td>B3</td>
<td>$V_{OVLO}$ threshold input</td>
</tr>
<tr>
<td>ACK</td>
<td>A2</td>
<td>Power Good Acknowledge (open-drain output)</td>
</tr>
<tr>
<td>GND</td>
<td>C3, D3, E3</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>EN</td>
<td>A3</td>
<td>enable input (active LOW)</td>
</tr>
</tbody>
</table>
8. Functional description

8.1 **EN-input**

A HIGH on EN disables the channel MOSFET and all protection circuits, putting the device into low power mode. A LOW on EN enables the protection circuits and the MOSFET. There is an internal 1 MΩ pull-down resistor on the EN pin to ensure the power switch conduction in a dead-battery situation. A 15 ms de-bounce time has been deployed before device turn-on. EN pin has 29 V tolerance.

8.2 **Under-voltage lockout**

When EN is LOW and VBUS < VUVLO, the Under-Voltage LockOut (UVLO) circuits disable the power MOSFET. Once VBUS exceeds VUVLO and no other protection circuit is active, the channel MOSFET state is controlled by the EN pin.

8.3 **Over-voltage lockout**

When EN is LOW and VBUS > VOVLO, the over-voltage lockout (OVLO) circuit disables the power MOSFET. Once VBUS drops below VOVLO and no other protection circuit is active, the power MOSFET resumes operation.

OVLO pin is used to set the over-voltage threshold. The default over-voltage threshold is 23 V when OVLO pin shorts to GND. Connecting a resistor divider to the OVLO pin (see Figure 5) adjusts the over voltage threshold from 4 V to 23 V using Equation 1:

\[
V_{ovlo} = V_{th(o vlo)} \times (R1 + R2)/(R2) \tag{1}
\]

When the voltage on OVLO pin is below 0.1 V, the device defaults to the 23 V OVP threshold.

8.4 **Over-temperature protection**

When EN is LOW and the device temperature exceeds 140 °C the Over-Temperature Protection (OTP) circuit disables the power MOSFET and sets the ACK output Hi-Z. Once the device temperature decreases below 115 °C and no other protection circuit is active, the state of the N-channel MOSFET is controlled by the EN pin again.

---

**Table 5. Function table**

<table>
<thead>
<tr>
<th>EN</th>
<th>VBUS</th>
<th>VINT</th>
<th>ACK</th>
<th>Operation mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>&lt; 2.5 V</td>
<td>X</td>
<td>Z</td>
<td>Under-voltage lockout; switch open</td>
</tr>
<tr>
<td>L</td>
<td>2.5 V &lt; VBUS &lt; VOVLO</td>
<td>X</td>
<td>L</td>
<td>Enabled; switch closed; charging mode</td>
</tr>
<tr>
<td>L</td>
<td>&gt; VOVLO</td>
<td>X</td>
<td>Z</td>
<td>Over-temperature protection; switch open</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Disable; switch open</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>VINT&gt;VBUS</td>
<td>Z</td>
<td>Reverse Current Protection; Switch open</td>
</tr>
</tbody>
</table>

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.
8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. The ACK pin indicates the state of the power switch. When no fault is detected and power switch is conducting, ACK goes output low, otherwise it stays at high impedance. The pull up resistor value is recommend to be 10 KΩ to 200 KΩ.

8.6 Reverse Current Protection

NX20P5090 has all time reverse current protection regardless of the EN logic level. Once the voltage on VINT is higher than VBUS for 45 mV, the RCP circuit is triggered after a 3.7ms de-glitch time. If the voltage gap is greater than 120 mV, RCP triggers immediately to switch off the power MOSFET.

During the start up de-glitch time, if the device detects the VINT voltage is higher than VBUS by 45 mV, the power MOSFET does not turn on.

The RCP circuit helps by providing the capability of parallel connection of two USB charging ports to a single charger input, without backward leakage.

9. Application diagram

The NX20P5090 is typically used on a USB port charging path in a portable, battery operated device. The ACK signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level that it is connected to.

When the default 23 V OVP threshold is used, the OVLO pin shorts to GND. If an adjustable OVP threshold is needed, a resistor divider is connected to the OVLO pin.

For best performance, it is recommended to keep input and output traces short and capacitors as close to the device as possible. Regarding thermal performance, it is recommended to increase the PCB area around VINT and VBUS pins.

Fig 5. NX20P5090 application with one charging input

R1 and R2 are only needed for adjustable VOVLO; to use default VOVLO threshold, connect OVLO to GND
R1 is recommended to use minimum 1 MΩ resistor
COUT minimum is recommended to be 1 uF
10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I$</td>
<td>input voltage</td>
<td>VBUS [1]</td>
<td>-0.5</td>
<td>+29</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VINT [1]</td>
<td>-0.5</td>
<td>+29</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OVLO</td>
<td>-0.5</td>
<td>VBUS</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN [2]</td>
<td>-0.5</td>
<td>+29</td>
<td>V</td>
</tr>
<tr>
<td>$V_O$</td>
<td>output voltage</td>
<td>ACK</td>
<td>-</td>
<td>+6.0</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IK}$</td>
<td>input clamping</td>
<td>EN: $V_I &lt; -0.5$ V</td>
<td>-50</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SK}$</td>
<td>switch clamping</td>
<td>VBUS; VINT; $V_I &lt; -0.5$ V</td>
<td>-50</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SW}$</td>
<td>continuous switch</td>
<td>$T_{amb} = 85$ °C</td>
<td>-</td>
<td>5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>current</td>
<td>$T_{amb} = 105$ °C</td>
<td>-</td>
<td>3.5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>peak switch current</td>
<td>100μs pulse, 2% duty cycle</td>
<td>-</td>
<td>10</td>
<td>A</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>$T_{amb} = 25$ °C</td>
<td>-</td>
<td>1.45</td>
<td>W</td>
</tr>
</tbody>
</table>

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

### 11. Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{I}$</td>
<td>input voltage</td>
<td>VBUS</td>
<td></td>
<td>2.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VINT</td>
<td></td>
<td>2.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN</td>
<td></td>
<td>0</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$V_{O}$</td>
<td>output voltage</td>
<td>ACK</td>
<td></td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$T_{j\text{max}}$</td>
<td>maximum junction temperature</td>
<td></td>
<td></td>
<td>-40</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td></td>
<td></td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

### 12. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td></td>
<td></td>
<td>67.2</td>
<td>KW</td>
</tr>
</tbody>
</table>

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] This $R_{th(j-a)}$ is calculated based on JEDE2S2P board. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts.
13. Static characteristics

Table 9. Static characteristics
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_{amb} = 25$ °C</th>
<th>$T_{amb} = -40$ °C to +85 °C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_{IH}$ HIGH-level input voltage; $V_{IL}$ LOW-level input voltage; $V_{OL}$ LOW-level output voltage; $R_{pd}$ pull-down resistance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>HIGH-level input voltage</td>
<td>$EN$ pin; $VI(VBUS) = 2.5$ V to 20 V</td>
<td>1.2</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>LOW-level input voltage</td>
<td>$EN$ pin; $VI(VBUS) = 2.5$ V to 20 V</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>LOW-level output voltage</td>
<td>ACK; $I_O = 8$ mA; $VI(VBUS) = 2.5$ V to 20 V</td>
<td>-</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$R_{pd}$</td>
<td>pull-down resistance</td>
<td>$EN$</td>
<td>-</td>
<td>-</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$I_q$</td>
<td>VBUS quiescent current</td>
<td>$EN = 0$ V; $VI(VBUS) = 5.0$ V; $I_O = 0$ A; $VI(VINT) = 0$ V</td>
<td>70</td>
<td>95</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{S(OFF)}$</td>
<td>VBUS OFF-state leakage current</td>
<td>$EN = 5.0$ V; $VI(VBUS) = 5.0$ V; $I_O = 0$ A; $VI(VINT) = 0$ V</td>
<td>5</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{S(ON)}$</td>
<td>RCP leakage current</td>
<td>$EN = 0$ V; $VI(VINT) = 5$ V; $V(VBUS) = 0$ V</td>
<td>1</td>
<td>5</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>OVLO input leakage Current</td>
<td>$VOVLO = V_{IN(OVLO)}$</td>
<td>-</td>
<td>-</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>under-voltage lockout release voltage</td>
<td>$VBUS$ Rising; $EN = 0$ V</td>
<td>2.37</td>
<td>2.24</td>
<td>V</td>
</tr>
<tr>
<td>$V_{hys(UVLO)}$</td>
<td>under-voltage lockout hysteresis voltage</td>
<td>$VBUS$ Falling</td>
<td>-</td>
<td>-</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OVLO}$</td>
<td>Default overvoltage lockout voltage</td>
<td>$VBUS$ Rising; $EN = 0$ V; $OVLO$ short to GND</td>
<td>23</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN(OVLO)}$</td>
<td>external OVLO set threshold voltage</td>
<td>$V_{I(VBUS)} = 2.5$ V to 20 V; $EN = 0$ V; $OVLO$ short to GND</td>
<td>22.5</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{big}$</td>
<td>RCP trigger voltage</td>
<td>$V_{big} = V_{I(VINT)} - V_{I(VBUS)}$</td>
<td>45</td>
<td>10</td>
<td>mV</td>
</tr>
<tr>
<td>$C_{i}$</td>
<td>input capacitance</td>
<td>$EN$ pin; $VI(VBUS) = 5$ V</td>
<td>4.5</td>
<td>-</td>
<td>pF</td>
</tr>
</tbody>
</table>
13.1 Graphs

Fig 7. On-state quiescent current versus input voltage

- $V_{(VBUS)} = 20\,V;\, EN = 5\,V$
- $T_{amb} = +85\,^\circ C$.
- $T_{amb} = +25\,^\circ C$.
- $T_{amb} = -40\,^\circ C$.

Fig 8. OFF-state quiescent current versus input voltage

- $EN = 0\,V;\, IO = 0\,A$
- $T_{amb} = +85\,^\circ C$.
- $T_{amb} = +25\,^\circ C$.
- $T_{amb} = -40\,^\circ C$.

Fig 9. OFF-state leakage current on VBUS pin

- $V_{(VINT)} = 20\,V;\, EN = 5\,V$
- $T_{amb} = +85\,^\circ C$.
- $T_{amb} = +25\,^\circ C$.
- $T_{amb} = -40\,^\circ C$.

Fig 10. OFF-state leakage current on VINT pin

- $EN = 5\,V;\, IO = 0\,A$
- $T_{amb} = +85\,^\circ C$.
- $T_{amb} = +25\,^\circ C$.
- $T_{amb} = -40\,^\circ C$. 
Fig 11. Reverse leakage current versus temperature

$EN = 0\,\text{V};\ V_{(VINT)} = 5\,\text{V};\ VBUS = 0\,\text{V}$

Fig 12. External OVLO set threshold versus temperature

$EN = 0\,\text{V};\ V_{(VBUS)} = 5\,\text{V}$

Fig 13. 90 V surge voltage without device

IEC61000-4-5 90 V

$EN = 0\,\text{V};\$OVLO short to GND; no capacitor on VBUS

(1) $I_{(VBUS)}$

(2) $V_{(VBUS)}$

(3) $V_{(OVLO)}$

Fig 14. 90 V surge with device
IEC61000-4-5 100 V

Fig 15. 100 V surge voltage without device

Fig 16. 100 V surge with device

EN = 0 V; OVLO short to GND; 22 uF capacitor on VBUS

(1) I(VBUS)
(2) V(VBUS)
(3) V(D(VINT))
13.2 ON resistance

Table 10. ON resistance
At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>( T_{\text{amb}} = 25 , ^\circ\text{C} )</th>
<th>( T_{\text{amb}} = -40 , ^\circ\text{C} ) to +85 , ^\circ\text{C}</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{ON}} )</td>
<td>ON resistance</td>
<td>( I_{\text{LOAD}} = 1 , \text{A} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{I(VBUS)}} = 5.0 , \text{V} )</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 30</td>
<td>36</td>
<td>-</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{I(VBUS)}} = 20 , \text{V} )</td>
<td>- 30</td>
<td>36</td>
<td>-</td>
</tr>
</tbody>
</table>

\[ R_{\text{ON}} = \frac{V_{\text{SW}}}{I_{\text{LOAD}}} \]

Fig 17. Test circuit for measuring ON resistance

13.3 ON resistance test circuit and graphs

- Fig 18. ON resistance versus temperature

- (1) \( V_{\text{I(VBUS)}} = 2.5 \, \text{V} \)
- (2) \( V_{\text{I(VBUS)}} = 5.0 \, \text{V} \)
- (3) \( V_{\text{I(VBUS)}} = 9.0 \, \text{V} \)
- (4) \( V_{\text{I(VBUS)}} = 12.0 \, \text{V} \)
- (5) \( V_{\text{I(VBUS)}} = 20.0 \, \text{V} \)
## 14. Dynamic characteristics

**Table 11. Dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 20.*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>( T_{\text{amb}} = 25 , ^\circ\text{C} )</th>
<th>( T_{\text{amb}} = -40 , ^\circ\text{C} ) to +85 , ^\circ\text{C}</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{en}} )</td>
<td>Enable Time</td>
<td>From EN to ( V_{\text{INT}} ) = 10% of ( V_{\text{BUS}} ); (Including 15ms debounce time); ( V_{\text{BUS}} = 5 , \text{V} ); ( C_{\text{load}} = 100 , \mu\text{F} ); ( R_{\text{load}} = 100 , \Omega )</td>
<td>-</td>
<td>21.9</td>
<td>-</td>
</tr>
<tr>
<td>( t_{\text{TLH}} )</td>
<td>VINT rise time</td>
<td>( V_{\text{INT}} ) from 10% to 90% ( V_{\text{BUS}} ); ( C_{\text{load}} = 100 , \mu\text{F} ); ( R_{\text{load}} = 100 , \Omega ) ( V_{\text{INT}} = 5 , \text{V} )</td>
<td>-</td>
<td>3.4</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{INT}} = 20 , \text{V} )</td>
<td>-</td>
<td>6.9</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{INT}} = 20 , \text{V} ); ( V_{\text{BUS}} = 20 , \text{V} ); OVPLO pin short to GND</td>
<td>-</td>
<td>122</td>
<td>-</td>
</tr>
<tr>
<td>( t_{\text{doff}} )</td>
<td>RCP de-glitch time</td>
<td>From ( V_{\text{INT}} &gt; V_{\text{BUS}} + 45 , \text{mV} ) to switch off</td>
<td>-</td>
<td>3.7</td>
<td>2.6</td>
</tr>
<tr>
<td>( t_{\text{dis(RCP)}} )</td>
<td>RCP turn off time</td>
<td>From ( V_{\text{INT}} &gt; V_{\text{BUS}} + 120 , \text{mV} ) to switch off [1]</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>( t_{\text{on}} )</td>
<td>turn-on time</td>
<td>EN to ( V_{\text{INT}} ) = 90% ( V_{\text{BUS}} ) ( V_{\text{INT}} = 5.0 , \text{V} )</td>
<td>-</td>
<td>25.3</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{INT}} = 20 , \text{V} )</td>
<td>-</td>
<td>29.2</td>
<td>-</td>
</tr>
<tr>
<td>( t_{\text{off}} )</td>
<td>turn-off time</td>
<td>EN to ( V_{\text{INT}} ) = 10% ( V_{\text{BUS}} ) ( V_{\text{INT}} = 5.0 , \text{V} ); ( C_{\text{load}} = 100 , \mu\text{F} ); ( R_{\text{load}} = 100 , \Omega )</td>
<td>-</td>
<td>23</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{INT}} = 20 , \text{V} ); ( C_{\text{load}} = 100 , \mu\text{F} ); ( R_{\text{load}} = 100 , \Omega )</td>
<td>-</td>
<td>23</td>
<td>-</td>
</tr>
</tbody>
</table>

\[1\] Guaranteed by design
14.1 Waveforms and test circuit

![Waveforms and test circuit diagram]

Test Condition is given in Table 12

<table>
<thead>
<tr>
<th>Supply voltage V\text{EXT}</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>\text{VBUS}</td>
<td>\text{C}_L</td>
</tr>
<tr>
<td>2.5 \text{ V} to 20 \text{ V}</td>
<td>100 \text{ \mu F}</td>
</tr>
</tbody>
</table>
Fig 21. Turn on time and in-rush current at 5 V

- $V_{(\text{VBUS})} = 5.0$ V; $R_L = 100$ $\Omega$; $C_L = 100$ $\mu$F
- (1) $\text{VINT}$
- (2) $\text{EN}$
- (3) $I_{(\text{VBUS})}$

Fig 22. Turn on time and in-rush current at 20 V

- $V_{(\text{VBUS})} = 20.0$ V; $R_L = 100$ $\Omega$; $C_L = 100$ $\mu$F
- (1) $\text{VINT}$
- (2) $\text{EN}$
- (3) $I_{(\text{VBUS})}$

Fig 23. Turn off time at 5 V

- $V_{(\text{VBUS})} = 5.0$ V; $R_L = 100$ $\Omega$; $C_L = 100$ $\mu$F
- (1) $\text{VINT}$
- (2) $\text{EN}$
- (3) $I_{(\text{VBUS})}$

Fig 24. Turn off time at 20 V

- $V_{(\text{VBUS})} = 20.0$ V; $R_L = 100$ $\Omega$; $C_L = 100$ $\mu$F
- (1) $\text{VINT}$
- (2) $\text{EN}$
- (3) $I_{(\text{VBUS})}$
15. Package outline

WLCSP15: wafer level chip-scale package; 15 bumps; 2.56 x 1.54 x 0.555 mm (Backside coating included)

Fig 25. Package outline SOT1392-1

<table>
<thead>
<tr>
<th>Unit</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>e1</th>
<th>e2</th>
<th>v</th>
<th>w</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>max</td>
<td>0.595</td>
<td>0.260</td>
<td>0.350</td>
<td>0.35</td>
<td>2.59</td>
<td>1.57</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mm</td>
<td>nom</td>
<td>0.555</td>
<td>0.230</td>
<td>0.325</td>
<td>0.32</td>
<td>2.56</td>
<td>1.54</td>
<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
<td>0.05</td>
</tr>
<tr>
<td>min</td>
<td>0.515</td>
<td>0.200</td>
<td>0.290</td>
<td>0.29</td>
<td>2.53</td>
<td>1.51</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Backside coating 25 µm

Fig 25. Package outline SOT1392-1 (WLCSP15)
16. Packing information

16.1 Packing method

Table 13. Dimensions and quantities

<table>
<thead>
<tr>
<th>Reel dimensions d × w (mm)</th>
<th>SPQ/PQ (pcs)</th>
<th>Reels per box</th>
<th>Outer box dimensions l × w × h (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>180 × 12</td>
<td>3000</td>
<td>1</td>
<td>209 × 206 × 37</td>
</tr>
</tbody>
</table>

[1] d = reel diameter; w = tape width.

View ordering and availability details at NXP order portal, or contact your local NXP representative.
### 16.2 Product orientation

Fig 27. Product orientation in carrier tape

### 16.3 Carrier tape dimensions

Fig 28. Carrier tape dimensions

**Table 14. Carrier tape dimensions**

In accordance with IEC 60286-3.

<table>
<thead>
<tr>
<th>A₀ (mm)</th>
<th>B₀ (mm)</th>
<th>K₀ (mm)</th>
<th>T (mm)</th>
<th>P₁ (mm)</th>
<th>W (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.67 ± 0.05</td>
<td>2.69 ± 0.05</td>
<td>0.70 ± 0.05</td>
<td>0.25 ± 0.02</td>
<td>4.0 ± 0.1</td>
<td>12 ± 0.3 / 0.1</td>
</tr>
</tbody>
</table>
16.4 Reel dimensions

Fig 29. Schematic view of reel

Table 15. Reel dimensions
In accordance with IEC 60286-3.

<table>
<thead>
<tr>
<th>A [nom] (mm)</th>
<th>W2 [max] (mm)</th>
<th>B [min] (mm)</th>
<th>C [min] (mm)</th>
<th>D [min] (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>18.4</td>
<td>1.5</td>
<td>12.8</td>
<td>20.2</td>
</tr>
</tbody>
</table>
16.5 Barcode label

![Barcode Label Diagram]

**Fig 30. Example of typical box and reel information barcode label**

**Table 16. Barcode label dimensions**

<table>
<thead>
<tr>
<th>Box barcode label</th>
<th>Reel barcode label</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>l × w (mm)</strong></td>
<td><strong>l × w (mm)</strong></td>
</tr>
<tr>
<td>100 × 75</td>
<td>100 × 75</td>
</tr>
</tbody>
</table>
17. Soldering of WLCSP packages

17.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 “Wafer Level Chip Scale Package” and in application note AN10365 “Surface mount reflow soldering description”.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

17.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

17.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17.

Table 17. Lead-free process (from J-STD-020D)

<table>
<thead>
<tr>
<th>Package thickness (mm)</th>
<th>Package reflow temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Volume (mm³)</td>
</tr>
<tr>
<td>&lt; 350</td>
<td>350 to 2000</td>
</tr>
<tr>
<td>1.6</td>
<td>260</td>
</tr>
<tr>
<td>1.6 to 2.5</td>
<td>260</td>
</tr>
<tr>
<td>&gt; 2.5</td>
<td>250</td>
</tr>
</tbody>
</table>

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.
17.3.1 Stand off
The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

17.3.2 Quality of solder joint
A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

17.3.3 Rework
In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.
Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 “Surface mount reflow soldering description”.

17.3.4 Cleaning

Cleaning can be done after reflow soldering.
18. Revision history

<table>
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<th>Data sheet status</th>
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19. Legal information

19.1 Data sheet status

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<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
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