P3B1602DP

I3C Repeater and Bidirectional Voltage Level Translator

Rev. 1.0 — 8 July 2026 Product data sheet

1 General description

The P3B1602DP is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation.

The P3B1602DP is targeted toward I3C/I2C or other serial communication buses with large capacitive loading, supporting CL up to 100 pF. Longer one-shot ON duration ensures that the signal is driven during rising/falling edges, even for large capacitive loads and large round-trip delay caused by long trace.

2 Features and benefits

- Auto direction sensing and bidirectional voltage level translation
- Wide supply voltage range:
  - V_{CCA}: 0.72 V to 1.98 V and V_{CCB}: 1.08 V to 3.63 V
- Longer one-shot pulse for driving larger capacitive loads with reduced ringing and overshoot
- No power-sequencing required
- Maximum frequency (SDR data rate):
  - Open-drain: 3.4 MHz (3.4 Mbit/s)
  - Push-pull: 12.5 MHz (12.5 Mbit/s)
- Supports I3C/I2C/SMBus interfaces (does not support clock stretching)
- OE pin tolerant to 3.63 V
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2000 V
  - CDM JESD22-C101E exceeds 500 V
- I/O latch-up current 100 mA, JESD 78
- Package:
  - TSSOP8 (3 x 3 x 1.1 mm)
- Specified from -40 °C to +125 °C

3 Applications

- I3C/I2C/SMBus
- Server

4 Ordering information

Table 1 describes the ordering information for P3B1602DP.

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
P3B1602DP	B1602	TSSOP8	Plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

4.1 Ordering options

Table 2 describes the ordering options for P3B1602DP.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3B1602DP	P3B1602DPJ	TSSOP8	REEL 13" Q1/T1 *STANDARD MARK SMD	2,500	T_{amb} = -40 °C to +125 °C

5 Block diagram

Figure 1 shows the labeled block diagram for P3B1602DP.

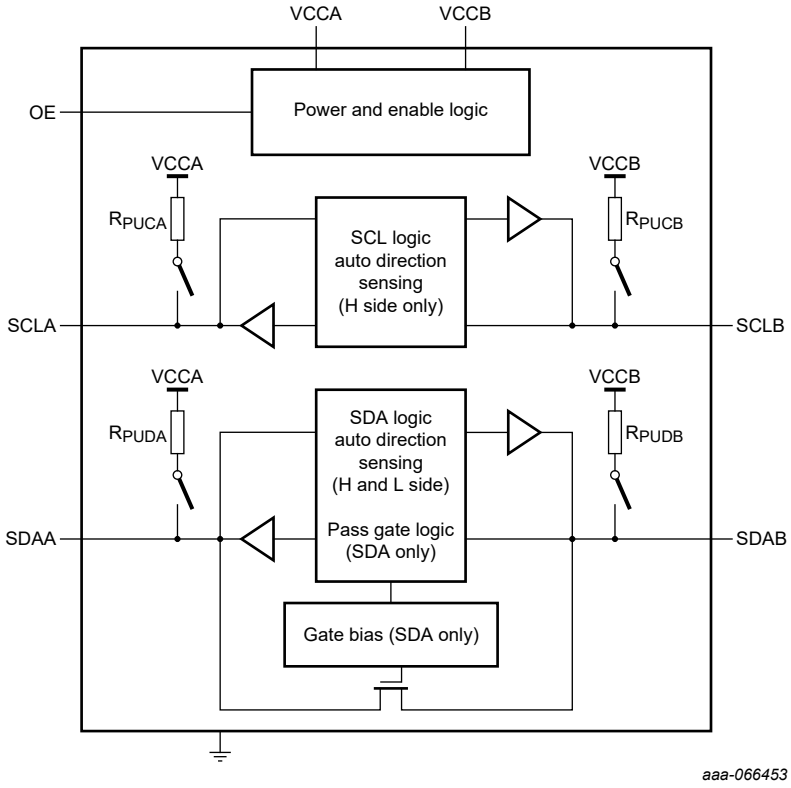


Figure 1. Block diagram

When OE = Low, the RupXX is disabled. For more details, refer Section 7.

6 Pinning information

This section provides the pin configuration and description for P3B1602DP.

6.1 Pinning

Figure 2 show the pinning of TSSOP8 package offered for P3B1602DP.

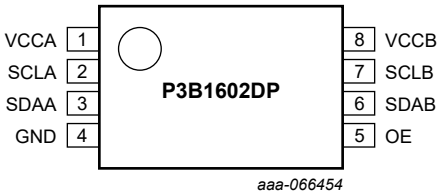


Figure 2. Pin configuration of TSSOP (MSOP8)

6.2 Pin description

Table 3 provides detailed description of various pins on TSSOP8 package offered for P3B1602DP.

Table 3. Pin description

Symbol	Pin	Type	Description
VCCA	1	Supply	Port A supply voltage (0.72 V to 1.98 V)
SCLA	2	Input/output	Serial clock port A bus
SDAA	3	Input/output	Serial data port A bus
GND	4	Supply	Ground supply voltage
OE	5	Input	Active high enable pin
SDAB	6	Input/output	Serial clock port B bus
SCLB	7	Input/output	Serial data port B bus
VCCB	8	Supply	Port B supply voltage (1.08 V to 3.63 V)

7 Functional description

Refer to Figure 1.

7.1 Architecture

I3C SCL and SDA have different characteristics as explained below:

- SCL clock line is PP (push-pull) and unidirectional from the I3C controller to target. Multicontroller support is allowable. It does not support clock stretching.
- SDA data line can be either push-pull or open-drain. It's bidirectional.

Based on it, the P3B1602DP has two different topologies corresponding to SCL and SDA.

Table 4. Function table

Supply voltage		Input[1]	Input/output [1]	
V_{CCA}	V_{CCB}	OE	A	B
0.72 V to 1.98 V and $V_{CCA} \leq V_{CCB}$	1.08 V to 3.63 V	L	Z	Z
0.72 V to 1.98 V and $V_{CCA} \leq V_{CCB}$	1.08 V to 3.63 V	H	Input or output	Output or input
GND [2]	GND [2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.
[2] When either V_{CCA} or V_{CCB} is at GND level, the device goes into Power-down mode.

SCAA/B and SDAA/B have different architectures. See details in Section 7.1.1 and Section 7.1.2.

7.1.1 Architecture for clock line (SCLA and SCLB)

The architecture of the device I/O channel is shown in Figure 3. The device does not require an extra input signal to control the direction of data flow from A port or B port. As a change of driving direction is possible when both sides are in HIGH state, the control logic recognizes the first falling edge and grants it control over the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In a communication error or some other unforeseen incident that drive both connected sides to be drivers at the same time, the internal logic automatically prevents a stuck-at situation, so both I/Os return to HIGH level once released from being driven LOW.

The SCLA port I/O has an internal 10 kΩ pullup resistor to VCCA. The SCLB port I/O has an internal 10 kΩ pullup resistor to VCCB. If a smaller value of pullup resistor is required, add an external resistor in parallel to the internal 10 kΩ. This pullup resistor affects the VOL level.

When OE goes LOW, the internal pullups of the P3B1602DPare disabled. The pulldown resistor is not recommended to avoid incorrect I/O logic level.

This architecture supports both I3C, I2C and SMBus interfaces. It can drive large load capacitance up to 100 pF and longer PCB traces. Note: It does not support clock stretching.

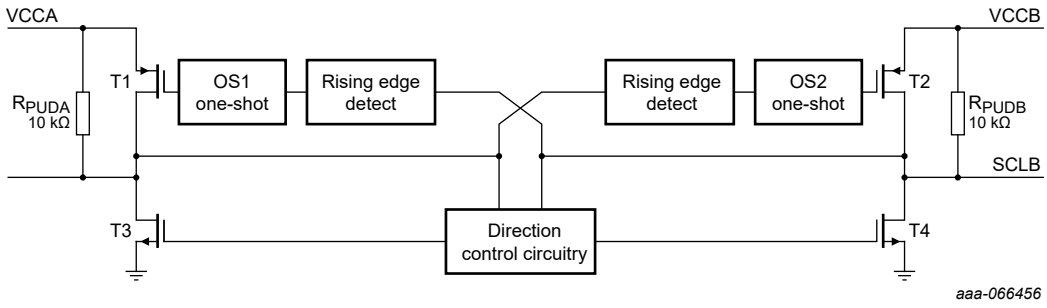


Figure 3. Architecture of P3B1602 clock line (SCLA and SCLB)

7.1.2 Architecture of data line (SDAA and SDAB)

Figure 4 describes the SDA architecture of P3B1602DP design for both push-pull and open-drain mode. The architecture uses edge-rate accelerator circuitry (for both high-to-low and low-to-high), N-channel pass gate transistor, and a pullup resistor (providing DC-bias and drive capabilities) to meet these requirements. The design is directionless and does not need a direction control signal. The implementation supports both low-speed open-drain operation and high-speed push-pull operation. The N-channel pass device T5 is on only during the low input cycle and off during the high input cycle.

When transmitting data from A-ports, during a rising edge and A port voltage = V_{IH}, both PMOS transistor T1 and T2 are turned on by OS1 (one-shot) and OS2 (one-shot) for a short duration (25 ns Typ) respectively to reduce the low to high transition time. Similarly, during a falling edge, when transmitting data from A to B and voltage = V_{IL}, the OS4 one-shot turns on the N-channel transistor T4 for 25 ns (Typ) which speeds up the high to low transition. The OS3 and T3 on the input side (A-port) do not turn on.

When transmitting data from B-ports, during a rising edge and B port voltage = V_{IH}, both PMOS transistor T1 and T2 are turned on by OS1 (one-shot) and OS2 (one-shot) for a short duration (25 ns Typ) respectively to reduce the low to high transition time. Similarly, during a falling edge, when transmitting data from B to A and voltage = V_{IL}, the OS3 one-shot turns on the N-channel transistor T3 for 25 ns (Typ) which speeds up the high to low transition. The OS4 and T4 on the input side (B-port) do not turn on.

- R_{PUDA} or R_{PUDB} = 5 kΩ when:
  - The input signal is High with OE enabled and switches S1 or S2 are closed.
- R_{PUDA} or R_{PUDB} = 10 kΩ when:
  - The input signal is low with OE enabled and switches S1 or S2 are open.

When OE is low, R_{PUDA} or R_{PUDB} equals High Z.

The internal pullup resistor R_{PUDA} and R_{PUDB} are 10 kΩ parallel to another 10 kΩ controlled by the switch S1 and S2 respectively. The switches S1 and S2 are controlled by their respective input signal and OE.

For open-drain application, the external pullup resistor might be required for rising time adjustment. The external pullup resistor can be either on A side or B side. The maximum rising time can be estimated with R_{PU_EXT} × (CLA + CLB). Here, R_{PU_EXT} is an external pullup resistor, CLA is total load capacitance on the A side, and CLB is total load capacitance on the B side.

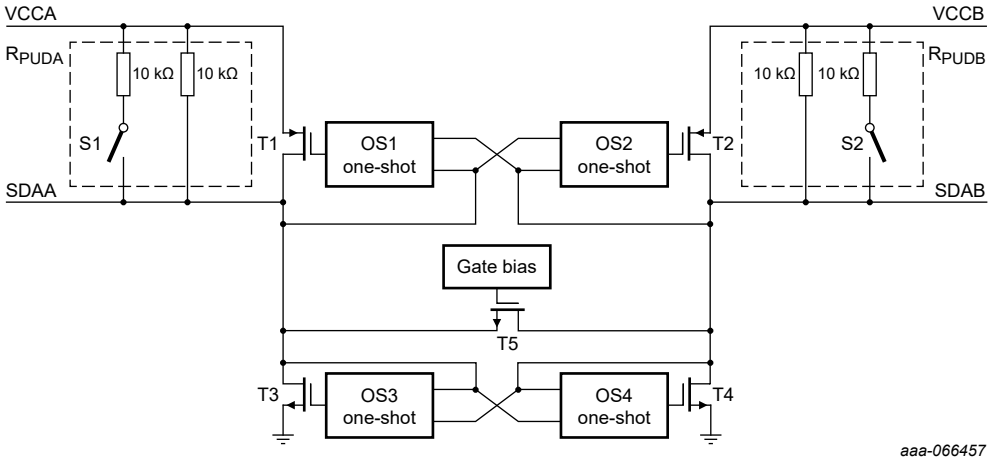


Figure 4. Architecture of P3B1602DP data line (SDAA and SDAB)

7.2 Input driver requirements

As the P3B1602DP is a switch-type translator, the properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (tTHL), and propagation delay (tPHL) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with an output impedance below 50 Ω is used.

7.3 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. The P3B1602DP has a longer one-shot pulse for driving larger capacitive loads (~ 100 pF).

If required, a series resistor (start with 33 Ω) on the signal path is recommended.

7.4 Power up

During operation, V_{CCA} must never be higher than V_{CCB}. However, during power up, once V_{CCA} is within limiting value, $V_{CCA} \geq V_{CCB}$ does not damage the device, so either power supply can be ramped up first.

There is no special power up sequencing required. The P3B1602DP includes circuitry that disables all output ports when either V_{CCA} or V_{CCB} is switched off. If the V_{CCB} is powered up later, it takes less than 100 µs for the internal circuit to start up.

7.5 Enable and disable

An output enable input (OE) is used to enable/disable the device. The OE logic level is a constant value and can be tolerated to V_{CCB}. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. Enable time (t_{en}) indicates the time required for one-shot circuitry to become operational after OE is taken HIGH, when the supply is already within operation range. Before the t_{en} (7 µs max), the I/O status must be ignored.

To ensure the high-impedance OFF-state during power up or power-down, pin OE must be tied to GND through a pulldown resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

7.6 Pullup/pulldown resistors on I/O lines

The A port I/O has an internal pullup resistor R_{PUDA} to V_{CCA}. The B port I/O has an internal pullup resistor R_{PUDB} to V_{CCB}. For more details, refer Section 7.1.1 and Section 7.1.2. If a smaller value of pullup resistor is required, add an external resistor in parallel to the internal 10 kΩ. This pullup resistor affects the VOL level.

When OE goes LOW, the internal pull-ups of the P3B1602DP are disabled.

The pulldown resistor is not recommended to avoid incorrect I/O logic level.

8 Application information

P3B1602DP can drive larger capacitive loads (up to 100 pF) and longer PCB traces (40 inch). It can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device can support both open-drain and push-pull interfaces like I3C/I2C/SMBus. Refer to Figure 5 for the typical application circuit.

If the PCB trance length is too long (> 30 cm) or the parasitic impedance is too large, the I/O signal can have overshoot/undershoot or oscillation. A series resistor (Rs) on each I/O pin is recommended to reduce the overshoot/undershoot and avoid the oscillation. The recommended value is 30 Ω. Adjust the Rs value for optimized signal integrity is required based on with different wire lengths and PCB parasitic R/L/C. Ensure that the Rs value is not too high to affect the VOL level.

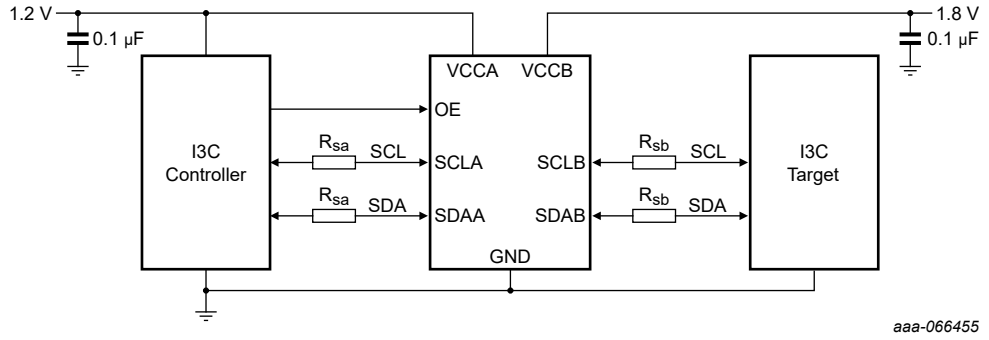


Figure 5. Typical application

A series resistor (30 Ω Typ) on the signal path is recommended for signal integrity. The value depends on system validation (0 Ω to 100 Ω).

9 Limiting values

Table 5 describes the limiting values of P3B1602DP.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	Supply voltage A	$V_{CCA} \leq V_{CCB}$	[1]	-0.5	+2.5	V
V_{CCB}	Supply voltage B		[2]	-0.5	+4.2	V
V_I	Input voltage	A port		-0.5	+2.5	V
		OE input		-0.5	+4.2	V
		B port		-0.5	+4.2	V
V_o	Output voltage	Active mode				
		A or B port	[2][3]	-0.5	VCCO + 0.5	V
		Power-down or 3-state mode				
		A port		-0.5	+2.5	V
		B port		-0.5	+4.2	V
T_{stg}	Storage temperature			-65	+150	°C

[1] The minimum input and minimum output voltage ratings can be exceeded, provided the input and output current ratings are observed.
[2] V_{CCo} is the supply voltage associated with the output.
[3] V_{CCo} + 0.5 V must not exceed the associated V_{CCo} maximum limiting value.

10 Thermal characteristics

This section describes the thermal characteristics of P3B1602DP.

Table 6. Thermal resistance information[1][2]

Symbol	Parameter	Value (type)	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance [1]	223.7	°C/W

Table 6. Thermal resistance information[1][2] *...continued*

Symbol	Parameter	Value (type)	Unit
ψ_{JT}	Junction-to-top of package thermal characterization parameter [1]	25.1	°C/W
$R_{\theta JC}$	Junction to case thermal resistance [3]	116.5	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] The thermal test board meets JEDEC specification for this package (JESD51-7).
[3] Junction-to-Case thermal resistance is determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.

11 Recommended operation conditions

This section describes the recommended operation conditions of P3B1602DP.

Table 7. Recommended operation conditions[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	Supply voltage A	$V_{CCA} \leq V_{CCB}$	[1][2]	0.72	1.98	V
V_{CCB}	Supply voltage B		[2]	1.08	3.63	V
VI_{OE}	OE input voltage			-0.3	3.63	V
T_{amb}	Ambient temperature			-40	+125	°C
T_j	Junction temperature		[3]	-40	+125	°C
Δt/ΔV	Input transition rise and fall rate	SDAA or SDAB; push-pull driving				
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V	[2]	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] VCCA must be less than or equal to VCCB and 1.98 V.
[3] The T_j limits are supported by proper thermal PCB design taking the power consumption and the thermal resistance into account.

12 Static characteristics

This section explains the static characteristics of P3B1602DP.

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	High-level input voltage for SCL, SDA, and OE	A port					
		V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 1.08 V to 3.63 V		V_{CCA} - 0.2			V
		V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V; $V_{CCA} \leq V_{CCB}$		min(V_{CCA} - 0.2, 0.65 × V_{CCA})			V
		B port					

Table 8. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V; $V_{CCA} \leq V_{CCB}$		0.65 × V_{CCB}			V
		OE input					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V; $V_{CCA} \leq V_{CCB}$		0.65			V
V_{IL_SCL}	Low-level input voltage for SCL	SCLA or SCLB					
		V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 1.08 V to 3.63 V	[1]	-		0.35 × V_{CCI}	V
		V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V; $V_{CCA} \leq V_{CCB}$	[1]	-		0.35 × V_{CCI}	V
V_{IL_SDA}	Low-level input voltage for SDA	SDAA or SDAB					
		V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 1.08 V to 3.63 V	[2]	-		0.35 × V_{CCA}	V
		V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V; $V_{CCA} \leq V_{CCB}$	[2]	-		0.35 × V_{CCA}	V
V_{IL_OE}	Low-level input voltage for OE	OE input					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V; $V_{CCA} \leq V_{CCB}$		-		0.3	V
V_{OH_SDA}	High-level output voltage for SDA	IO = -20 µA					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V	[3]	0.8 × V_{CCo}		-	V
V_{OH_SCL}	High-level output voltage for SCL	IO = -10 µA					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V	[3]	0.8 × V_{CCo}		-	V
V_{OL_SDA}	Low-level output voltage for SDA	SDAA or SDAB; IO = 1 mA	[3] [4]				
		V_I = 0.15 V; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V		-.		0.3	V
V_{OL_SCL}	Low-level output voltage for SCL	SCLA or SCLB; IO = 1 mA	[3] [4]				
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V		-		0.2	V
I_I	Input leakage current	OE = 0 V, V_{CCA}, or V_{CCB}; V_I = 0 V or V_{CCI}; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V		-		5	µA

Table 8. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	OE = 0 V V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V	[3]	-		10	µA
		V_{CCA} = 0 V or V_{CCB} = 0 V				10	µA
I_{CC}	Supply current	OE = V_{CCA}, V_I = V_{CCI}; I_O = 0 A	[1]				
		I_{CCA}					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V		-		25	µA
		V_{CCA} = 1.98 V; V_{CCB} = 0 V		-		25	µA
		V_{CCA} = 0 V; V_{CCB} = 3.63 V		-3			µA
		I_{CCB}					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V		-		25	µA
		V_{CCA} = 1.98 V; V_{CCB} = 0 V		-5			µA
		V_{CCA} = 0 V; V_{CCB} = 3.63 V		-		25	µA
		I_{CCA} + I_{CCB}					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.08 V to 3.63 V		-		40	µA
CI	Input capacitance	OE input; V_{CCA} = 1.2 V; V_{CCB} = 3.3 V		-	2	-	pF
CI/O	Input/output capacitance	A port	[5]	-	7	-	pF
		B port	[5]	-	5.5	-	pF

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{IL} of A & B port is the value with respect to V_{CCA}.
[3] V_{CCo} is the supply voltage associated with the output.
[4] This specification has more margins. The R_{on} (resistance between input and output at low stage) max = 50 Ω. The equation for V_{OL} is $V_{OL} = V_I + I_o \times R_{on}$.
[5] The CI/O is defined when A port and B port are isolated.

13 Dynamic characteristics

This section explains the dynamic characteristics of P3B1602DP.

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

Voltages are referred to GND (ground = 0 V); for test circuit, see Figure 8; for waveform, see Figure 6 and Figure 7.

Symbol	Parameter	Conditions	V_{CCB}				Unit
			1.08 V to 1.32 V		1.62 V to 3.63 V		
			Min	Max	Min	Max	
V_{CCA} = 0.8 V ± 10 %, $V_{CCA} \leq V_{CCB}$							

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referred to GND (ground = 0 V); for test circuit, see Figure 8; for waveform, see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		V_{CCB}				Unit
				1.08 V to 1.32 V		1.62 V to 3.63 V		
				Min	Max	Min	Max	
t_{pd_SCL}	SCL propagation delay	SCLA to SCLB; CL = 50 pF			9.5		8.3	ns
		SCLB to SCLA; CL = 50 pF			12		11.3	ns
		SCLA to SCLB; CL = 100 pF			10		8	ns
		SCLB to SCLA; CL = 100 pF			13.3		12	ns
t_{pd_SDA}	SDA propagation delay	SDAA to SDAB; CL = 50 pF			10		8.6	ns
		SDAB to SDAA; CL = 50 pF			8.5		7.2	ns
		SDAA to SDAB; CL = 100 pF			11.3		10.6	ns
		SDAB to SDAA; CL = 100 pF			10.2		8.9	ns
t_{en}	Enable time	OE to A, B; CL = 50 pF			7		7	µs
		OE to A, B; CL = 100 pF			7		7	µs
t_{dis}	Disable time	OE to A, B; CL = 50 pF	[2]		4		4	µs
		OE to A, B; CL = 100 pF	[2]		4		4	µs
t_{t_SCL}	SCL transition time	SCLA; CL = 50 pF			3.6		3.6	ns
		SCLA; CL = 100 pF			4.5		4.5	ns
		SCLB; CL = 50 pF			3.1		3.3	ns
		SCLB; CL = 100 pF			4.2		4.3	ns
t_{t_SDA}	SDA transition time	SDAA; CL = 50 pF			13.8		5.4	ns
		SDAA; CL = 100 pF			15		9	ns
		SDAB; CL = 50 pF			6.8		6.5	ns
		SDAB; CL = 100 pF			7.3		6.7	ns
tsk(o)	Output skew time	Delta between channels			9		9	ns
tW	Pulse width	Data inputs		62.5		62.5		ns
fdata	Data rate	SDR	[3] [4]	0.128	8	0.128	8	Mbit/s

[1] t_{en} is the same as t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Delay between OE going LOW and when the outputs are disabled.
[3] Assume CL (load capacitance) ≤ 50 pF and equal time for 1 bit and 0 bit information. The one-shot accelerator duration is a fixed value (50 ns max) at this V_{CCA} = 0.8 V ± 10 % and V_{CCB} condition.
[4] The specification is SDR per bit. For example, the 10 Mbit/s equivalents to 10 MHz.

Table 10. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

Voltages are referred to GND (ground = 0 V); for test circuit, see Figure 8; for waveform, see Figure 6 and Figure 7.

Symbol	Parameter	Conditions	V_{CCB}				Unit
			1.08 V to 1.32 V		1.62 V to 3.63 V		
			Min	Max	Min	Max	
V_{CCA} = 0.9 V to 1.32 V, $V_{CCA} \leq V_{CCB}$							

Table 10. Dynamic characteristics for temperature range -40 °C to +125 °C[1]*...continued*

Voltages are referred to GND (ground = 0 V); for test circuit, see Figure 8; for waveform, see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		V_{CCB}				Unit
				1.08 V to 1.32 V		1.62 V to 3.63 V		
				Min	Max	Min	Max	
t_{pd_SCL}	SCL propagation delay	SCLA to SCLB; CL = 50 pF			5.7		5.3	ns
		SCLB to SCLA; CL = 50 pF			5.3		4.2	ns
		SCLA to SCLB; CL = 100 pF			6.6		5.9	ns
		SCLB to SCLA; CL = 100 pF			6.1		5	ns
t_{pd_SDA}	SDA propagation delay	SDAA to SDAB; CL = 50 pF			6.7		6.5	ns
		SDAB to SDAA; CL = 50 pF			5.4		4	ns
		SDAA to SDAB; CL = 100 pF			8.5		7.6	ns
		SDAB to SDAA; CL = 100 pF			6.7		5.3	ns
t_{en}	Enable time	OE to A, B; CL = 50 pF			7		7	µs
		OE to A, B; CL = 100 pF			7		7	µs
t_{dis}	Disable time	OE to A, B; CL = 50 pF	[2]		4		4	µs
		OE to A, B; CL = 100 pF	[2]		4		4	µs
t_{t_SCL}	SCL transition time	SCLA; CL = 50 pF			3.5		3.8	ns
		SCLA; CL = 100 pF			4.7		4.4	ns
		SCLB; CL = 50 pF			3.4		3.2	ns
		SCLB; CL = 100 pF			4.6		4.7	ns
t_{t_SDA}	SDA transition time	SDAA; CL = 50 pF			7.1		4.2	ns
		SDAA; CL = 100 pF			8.5		6.5	ns
		SDAB; CL = 50 pF			7.1		4.9	ns
		SDAB; CL = 100 pF			8.1		6.3	ns
tsk(o)	Output skew time	Delta between channels			4		6	ns
tW	Pulse width	Data inputs		40		40		ns
fdata	Data rate	SDR	[3] [4]	0.128	12.5	0.128	12.5	Mbit/s

[1] t_{en} is the same as t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Delay between OE going LOW and when the outputs are disabled.
[3] Assume CL (load capacitance) ≤ 50 pF and equal time for 1 bit and 0 bit information. The one-shot accelerator duration is a fixed value (35 ns max) at this V_{CCA} = 0.9 V to 1.32 V and V_{CCB} condition.
[4] The specification is SDR per bit. For example, the 10 Mbit/s equivalents to 10 MHz.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

Voltages are referred to GND (ground = 0 V); for test circuit, see Figure 8; for waveform, see Figure 6 and Figure 7.

Symbol	Parameter	Conditions	V_{CCB}			Unit
			1.62 V to 3.63 V			
			Min		Max	
V_{CCA} = 1.8 V ± 10 %, $V_{CCA} \leq V_{CCB}$						

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1]*...continued*

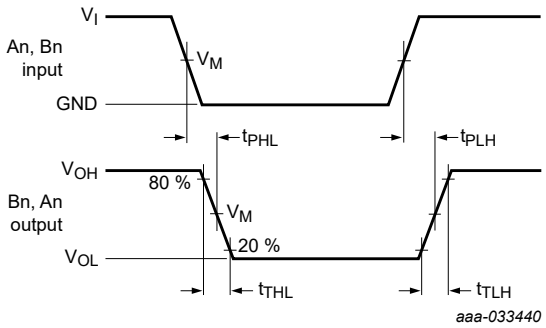
Voltages are referred to GND (ground = 0 V); for test circuit, see Figure 8; for waveform, see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		V_{CCB}		Unit
				1.62 V to 3.63 V		
				Min	Max	
t_{pd_SCL}	SCL propagation delay	SCLA to SCLB; CL = 50 pF			3.1	ns
		SCLB to SCLA; CL = 50 pF			2.5	ns
		SCLA to SCLB; CL = 100 pF			4	ns
		SCLB to SCLA; CL = 100 pF			3.3	ns
t_{pd_SDA}	SDA propagation delay	SDAA to SDAB; CL = 50 pF			3.5	ns
		SDAB to SDAA; CL = 50 pF			3	ns
		SDAA to SDAB; CL = 100 pF			4	ns
		SDAB to SDAA; CL = 100 pF			3.8	ns
t_{en}	Enable time	OE to A, B; CL = 50 pF			7	µs
		OE to A, B; CL = 100 pF			7	µs
t_{dis}	Disable time	OE to A, B; CL = 50 pF	[2]		4	µs
		OE to A, B; CL = 100 pF	[2]		4	µs
t_{t_SCL}	SCL transition time	SCLA; CL = 50 pF			3	ns
		SCLA; CL = 100 pF			4.2	ns
		SCLB; CL = 50 pF			3.1	ns
		SCLB; CL = 100 pF			4.5	ns
t_{t_SDA}	SDA transition time	SDAA; CL = 50 pF			3.3	ns
		SDAA; CL = 100 pF			4.4	ns
		SDAB; CL = 50 pF			3.8	ns
		SDAB; CL = 100 pF			4.9	ns
tsk(o)	Output skew time	Delta between channels			1.5	ns
tW	Pulse width	Data inputs		40		ns
fdata	Data rate	SDR	[3] [4]	0.128	12.5	Mbit/s

[1] t_{en} is the same as t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Delay between OE going LOW and when the outputs are disabled.
[3] Assume CL (load capacitance) ≤ 50 pF and equal time for 1 bit and 0 bit information. The one-shot accelerator duration is a fixed value (35 ns max) at this V_{CCA} = 1.8 V ± 10 % and V_{CCB} condition.
[4] The specification is SDR per bit. For example, the 10 Mbit/s equivalents to 10 MHz.

14 Waveforms

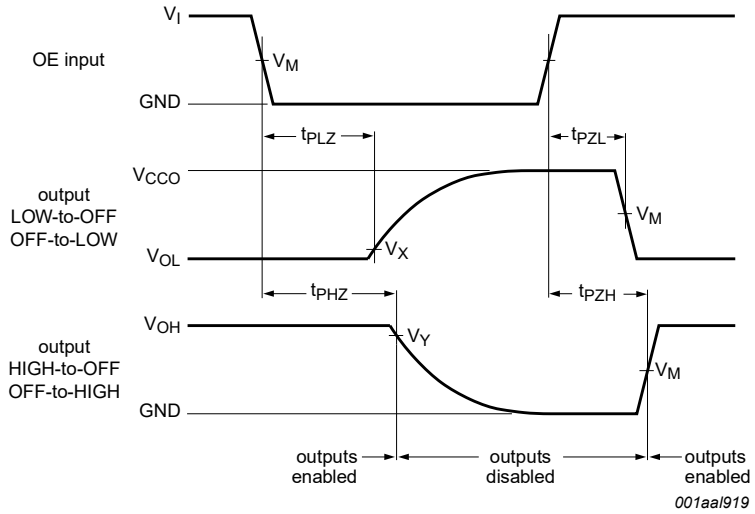
This section covers the waveform information, including test circuits and test data to support the information.



Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. The data input (A, B) to data output (B, A) propagation delay times



Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

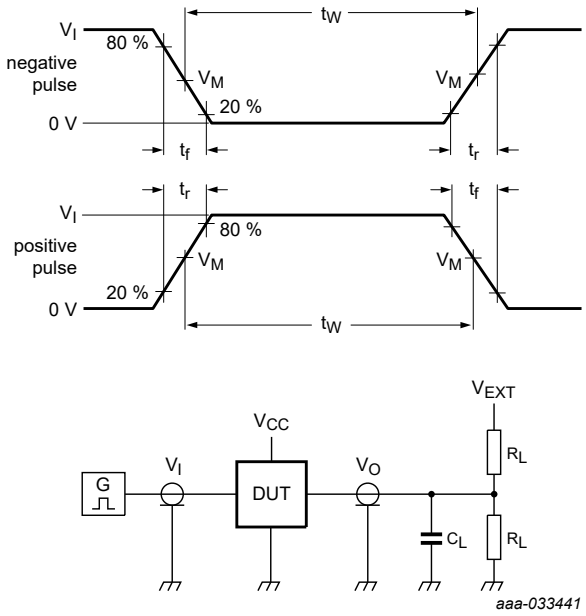
Figure 7. Enable and disable times

Table 12. Measurement points

V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

Supply voltage	Input [1]	Output [2]		
V_{CCO}	V_M	V_M	V_X	V_Y
0.8 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	V_{OL} + 0.08 V	V_{OH} - 0.08 V
1.2 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	V_{OL} + 0.12 V	V_{OH} - 0.12 V
1.8 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	V_{OL} + 0.18 V	V_{OH} - 0.18 V
3.3 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	V_{OL} + 0.30 V	V_{OH} - 0.30 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 13.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance

C_L = Load capacitance including jig and probe capacitance

V_{EXT} = External voltage for measuring switching times

Figure 8. Test circuit for measuring switching times

Table 13. Test data

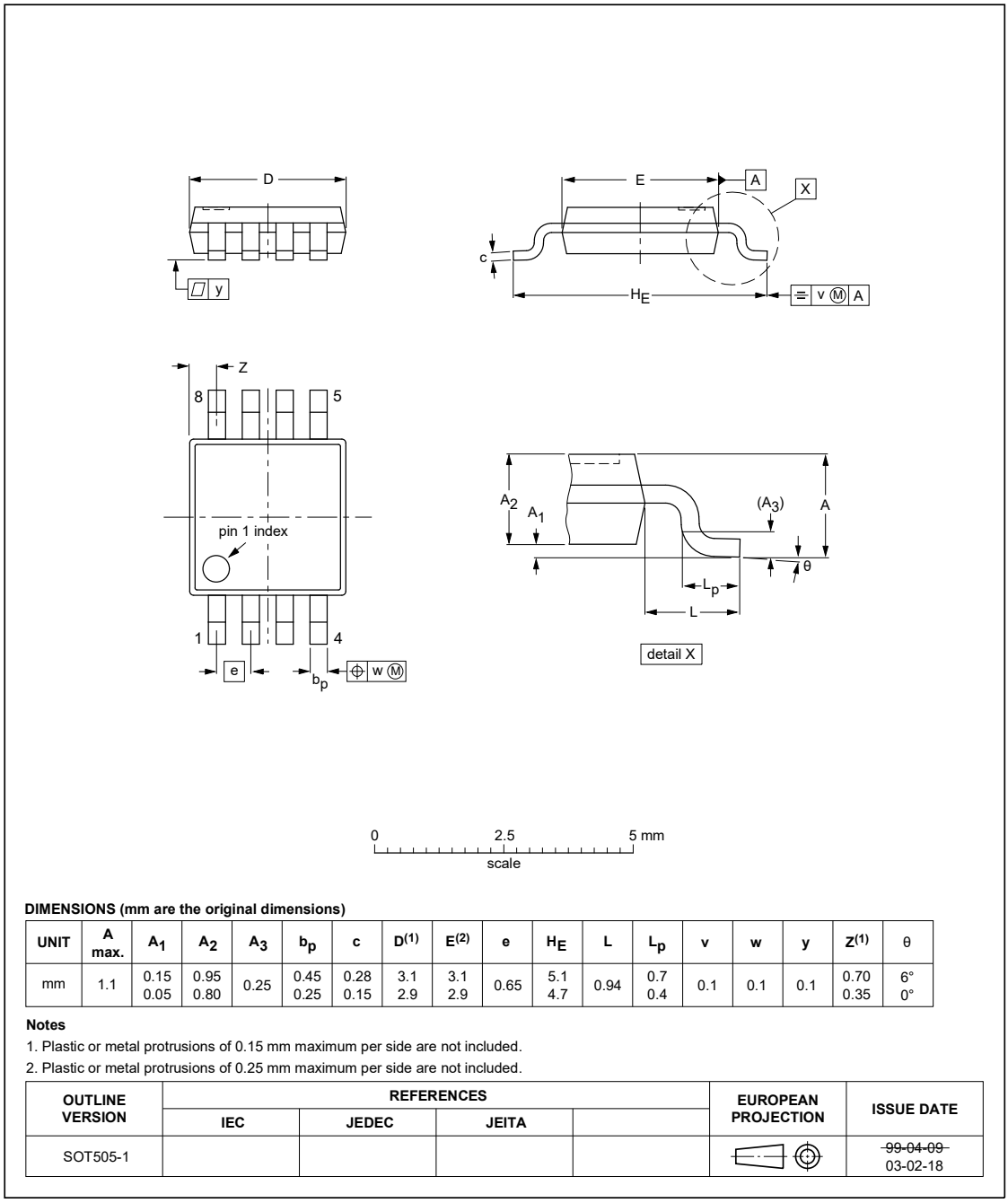
Supply voltage		Input		Load		V_{EXT}		
V_{CCA}	V_{CCB}	V_I [1]	Δt/ΔV	C_L [2]	R_L [3]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [4]
0.72 V to 1.98 V; and ≤ V_{CCB}	1.08 V to 3.63 V	V_{CCI}	≤ 10 ns/V	50 pF	50 kΩ, 1 MΩ	Open	Open	2 × V_{CCO}

[1] V_{CCI} is the supply voltage associated with the input.
[2] For I3C maximum C_L.
[3] For measuring data rate, pulse width, propagation delay, and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.
[4] V_{CCO} is the supply voltage associated with the output.

15 Package outline

This section contains a package outline diagram for the TSSOP8 package.

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Figure 9. Package outline SOT505-1 (TSSOP8)

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and Table 15

Table 14. SnPb eutectic process (from J-STD-020D)

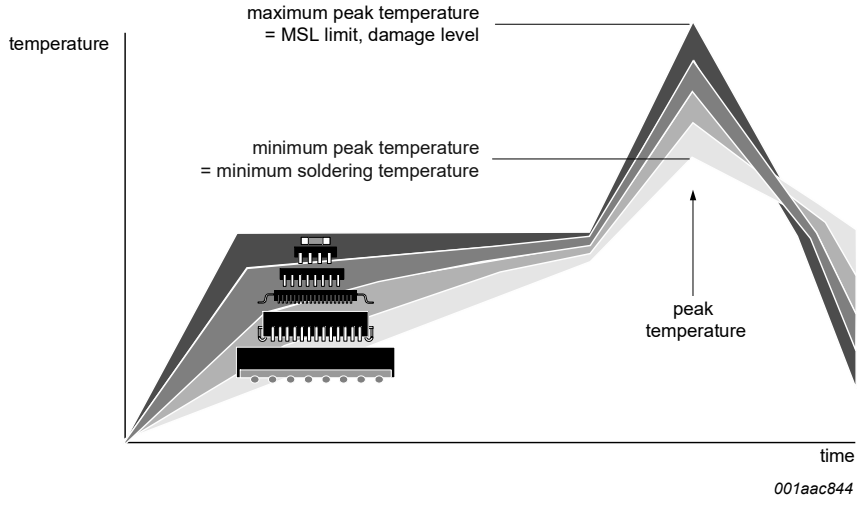
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Figure 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Footprint information

This section contains PCB footprint information for the TSSOP8 package.

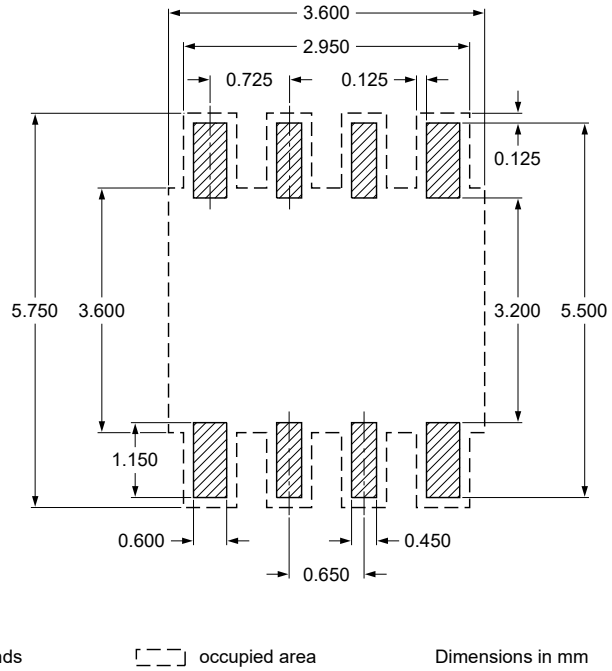


Figure 11. PCB footprint for SOT505-1 (TSSOP8)

18 Acronyms

Table 16 describes the acronyms used in this document.

Table 16. Acronyms

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
PCB	Printed-Circuit Board
PMOS	P-channel Metal-Oxide Semiconductor
SDR	Single Data Rate
SMBus	System Management Bus
SMD	Surface Mount Device

19 Revision history

Table 17 summarizes revisions to this document.

Table 17. Revision history

Document ID	Release date	Description
P3B1602DP v.1.0	8 July 2026	• Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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