1. General description

The PCA9846 is an ultra-low voltage, quad bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any or all SCx/SDx channels can be selected, determined by the programmable control register. This feature allows multiple devices with the same I²C-bus address to reside on the same bus. The switch device can also separate a heavily loaded I²C-bus into separate bus segments, eliminating the need for a bus buffer.

An active LOW reset input allows the PCA9846 to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I²C-bus state machine and deselects all the channels, as does the internal Power-On Reset (POR) function.

The pass gates of the switches are constructed such that the VDD1 pin is used to limit the maximum high voltage which is passed by the PCA9846. This allows the use of different bus voltages on each channel, so that 0.8 V, 1.8 V, 2.5 V or 3.3 V parts can communicate without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 3.6 V tolerant.

2. Features and benefits

- Ultra-low voltage operation, down to 0.8 V to interface with next-generation CPUs
- 1-of-4 bidirectional translating switch
- Fm+ I²C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- 2 address pins allowing up to 16 devices on the I²C-bus
- Channel selection via I²C-bus
- Power-up with all switch channels deselected
- Low R_on switches
- Allows voltage level translation between 0.8 V, 1.8 V, 2.5 V and 3.3 V buses
- Reset via I²C-bus software command
- I²C Device ID function
- No glitch on power-up
- Supports hot insertion since all channels are de-selected at power-on
- Low standby current
NXP Semiconductors

PCA9846

4-channel ultra-low voltage, Fm+ I2C-bus switch with reset

- 3.6 V tolerant inputs
- 0 Hz to 1 MHz clock frequency
- ESD protection exceeds 6000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Two packages offered: TSSOP16 and HVQFN16

3. Ordering information

Table 1. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Topside marking</th>
<th>Package Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCA9846BS[1]</td>
<td>846</td>
<td>HVQFN16</td>
<td>plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm</td>
<td>SOT629-1</td>
</tr>
<tr>
<td>PCA9846PW</td>
<td>PCA9846</td>
<td>TSSOP16</td>
<td>plastic thin shrink small outline package; 16 leads; body width 4.4 mm</td>
<td>SOT403-1</td>
</tr>
</tbody>
</table>

[1] Package is in development. Contact NXP for availability.

3.1 Ordering options

Table 2. Ordering options

<table>
<thead>
<tr>
<th>Type number</th>
<th>Orderable part number</th>
<th>Package Name</th>
<th>Packing method</th>
<th>Minimum order quantity</th>
<th>Temperature range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCA9846BS[1]</td>
<td>PCA9846BSJ</td>
<td>HVQFN16</td>
<td>Reel 13&quot; Q1/T1 *Standard mark SMD</td>
<td>6000</td>
<td>( T_{\text{amb}} = -40 \degree \text{C to } +85 \degree \text{C} )</td>
</tr>
<tr>
<td>PCA9846PW</td>
<td>PCA9846PWJ</td>
<td>TSSOP16</td>
<td>Reel 13&quot; Q1/T1 *Standard mark SMD</td>
<td>2500</td>
<td>( T_{\text{amb}} = -40 \degree \text{C to } +85 \degree \text{C} )</td>
</tr>
<tr>
<td>PCA9846PW</td>
<td>PCA9846PWZ</td>
<td>TSSOP16</td>
<td>Reel 13&quot; Q1/T1 *Standard mark SMD</td>
<td>500</td>
<td>( T_{\text{amb}} = -40 \degree \text{C to } +85 \degree \text{C} )</td>
</tr>
</tbody>
</table>

[1] Package is in development. Contact NXP for availability.
4. Block diagram

Fig 1. Block diagram of PCA9846
5. Pinning information

5.1 Pinning

5.2 Pin description

Table 3. Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD1</td>
<td>1 15</td>
<td>logic level power supply</td>
</tr>
<tr>
<td>A0</td>
<td>2 16</td>
<td>address input 0</td>
</tr>
<tr>
<td>RESET</td>
<td>3 1</td>
<td>active LOW reset input</td>
</tr>
<tr>
<td>SD0</td>
<td>4 2</td>
<td>serial data 0</td>
</tr>
<tr>
<td>SC0</td>
<td>5 3</td>
<td>serial clock 0</td>
</tr>
<tr>
<td>SD1</td>
<td>6 4</td>
<td>serial data 1</td>
</tr>
<tr>
<td>SC1</td>
<td>7 5</td>
<td>serial clock 1</td>
</tr>
<tr>
<td>VSS</td>
<td>8 6</td>
<td>supply ground</td>
</tr>
<tr>
<td>SD2</td>
<td>9 7</td>
<td>serial data 2</td>
</tr>
<tr>
<td>SC2</td>
<td>10 8</td>
<td>serial clock 2</td>
</tr>
<tr>
<td>SD3</td>
<td>11 9</td>
<td>serial data 3</td>
</tr>
<tr>
<td>SC3</td>
<td>12 10</td>
<td>serial clock 3</td>
</tr>
<tr>
<td>A1</td>
<td>13 11</td>
<td>address input 1</td>
</tr>
<tr>
<td>SCL</td>
<td>14 12</td>
<td>serial clock line</td>
</tr>
<tr>
<td>SDA</td>
<td>15 13</td>
<td>serial data line</td>
</tr>
<tr>
<td>VDD2</td>
<td>16 14</td>
<td>core logic power supply</td>
</tr>
</tbody>
</table>

[1] HVQFN16 package die supply ground is connected to both the VSS pin and the exposed center pad. The VSS pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.
6. **Functional description**

Refer to Figure 1 “Block diagram of PCA9846”.

### 6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9846 is shown in Figure 4. The device pins A0 and A1 must be connected to a valid logic signal — HIGH, LOW, SCL or SDA — to ensure a valid slave address, since no internal pull-up resistors are provided.

![Slave address](aaa-011933)

See Table 4.

**Fig 4. Slave address**
Table 4. Address selection

<table>
<thead>
<tr>
<th>PCA9846 address pins</th>
<th>8-bit I²C-bus address</th>
<th>Slave address/bit pattern master must send</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1  A0</td>
<td>A7 A6 A5 A4 A3 A2 A1 A0 - R/W</td>
<td></td>
</tr>
<tr>
<td>0   SCL 0x0E0h</td>
<td>1 1 1 0 0 0 0</td>
<td>0/1</td>
</tr>
<tr>
<td>0   0 0x0E2h</td>
<td>1 1 1 0 0 0 1</td>
<td>0/1</td>
</tr>
<tr>
<td>0   SDA 0x0E4h</td>
<td>1 1 1 0 0 0 1</td>
<td>0/1</td>
</tr>
<tr>
<td>0   1 0x0E6h</td>
<td>1 1 1 0 0 1 1</td>
<td>0/1</td>
</tr>
<tr>
<td>1   SCL 0x0E8h</td>
<td>1 1 1 0 0 1 0</td>
<td>0/1</td>
</tr>
<tr>
<td>1   0 0x0EAh</td>
<td>1 1 1 0 0 1 1</td>
<td>0/1</td>
</tr>
<tr>
<td>1   SDA 0x0ECh</td>
<td>1 1 1 0 1 1 0</td>
<td>0/1</td>
</tr>
<tr>
<td>1   1 0x0EEh</td>
<td>1 1 1 0 1 1 1</td>
<td>0/1</td>
</tr>
<tr>
<td>SCL SCL 0x0B0h</td>
<td>1 0 1 1 0 0 0</td>
<td>0/1</td>
</tr>
<tr>
<td>SCL 0 0x0B2h</td>
<td>1 0 1 1 0 0 1</td>
<td>0/1</td>
</tr>
<tr>
<td>SCL SDA 0x0B4h</td>
<td>1 0 1 1 0 1 0</td>
<td>0/1</td>
</tr>
<tr>
<td>SCL 1 0x0B6h</td>
<td>1 0 1 1 0 1 1</td>
<td>0/1</td>
</tr>
<tr>
<td>SDA SCL 0x0B8h</td>
<td>1 0 1 1 1 0 0</td>
<td>0/1</td>
</tr>
<tr>
<td>SDA 0 0x0BAh</td>
<td>1 0 1 1 1 0 1</td>
<td>0/1</td>
</tr>
<tr>
<td>SDA SDA 0x0BCh</td>
<td>1 0 1 1 1 1 0</td>
<td>0/1</td>
</tr>
<tr>
<td>SDA 1 0x0BEh</td>
<td>1 0 1 1 1 1 1</td>
<td>0/1</td>
</tr>
</tbody>
</table>

6.2 Software Reset General Call, and device ID addresses

Two other addresses can be sent to the device.

- General Call address: allows to reset the device through the I²C-bus upon reception of the right I²C-bus sequence. See Section 6.2.1 “Software Reset” for more information.

- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision), See Section 6.2.2 “Device ID (PCA9846 ID field)” for more information.
6.2.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address ‘0000 000’ with the R/W bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address ‘0000 0000’ (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.
   If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a ‘Software Reset Abort’. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 7.

---

**Fig 7. Software Reset sequence**

<table>
<thead>
<tr>
<th>S</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>A</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>A</th>
<th>P</th>
</tr>
</thead>
<tbody>
<tr>
<td>START condition</td>
<td>SWRST Call I²C-bus address</td>
<td>SWRST data = 06h</td>
<td>PCA9846 is reset. Registers are set to default power-up values.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W acknowledge from slave(s)</td>
<td>acknowledge from slave(s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.2.2 Device ID (PCA9846 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I^2C-bus address followed by the R/W bit set to 0 (write): ‘1111 1000’.
3. The master sends the I^2C-bus slave address of the slave device it needs to identify. The LSB is a ‘Don’t care’ value. Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
4. The master sends a Re-START command.
   **Remark:** A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.
5. The master sends the Reserved Device ID I^2C-bus address followed by the R/W bit set to 1 (read): ‘1111 1001’.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.
   **Remark:** The reading of the Device ID can be stopped anytime by sending a NACK command.

If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9846, the Device ID is shown in **Figure 8**.

```
<table>
<thead>
<tr>
<th>manufacturer</th>
<th>part identification</th>
<th>revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>1 0 0 0 0 1 0 1 1</td>
<td>0 0 0</td>
</tr>
</tbody>
</table>
```

**Fig 8. PCA9846 Device ID field**
6.3 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9846, which will be stored in the control register. If multiple bytes are received by the PCA9846, it will save the last byte received. This register can be written and read via the I²C-bus.

![Control register diagram]

If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a ‘no acknowledge’.

Fig 9. Device ID field read operation

Fig 10. Control register
6.3.1 Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9846 has been addressed. All 8 bits of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I2C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection. Notice that multiple channels may simultaneously be selected.

Table 5. Control register
Write = channel selection; Read = channel status

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>channel 0 disabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>channel 0 enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>channel 1 disabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>channel 1 enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>channel 2 disabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>channel 2 enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>channel 3 disabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>channel 3 enabled</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>no channel selected;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>power-up/reset default state</td>
</tr>
</tbody>
</table>

Remark: Several channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacitance.

6.4 RESET input

The RESET input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of \( t_{\text{rstL}} \), the PCA9846 will reset its registers and I2C-bus state machine and will deselect all channels.

6.5 Power-on reset

When power is applied to \( V_{DD} \), an internal Power-On Reset (POR) holds the PCA9846 in a reset condition until \( V_{DD} \) has reached \( V_{POR} \). At this point, the reset condition is released and the PCA9846 registers and I2C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected.

6.6 Power-on reset requirements

In the event of a glitch or data corruption, PCA9846 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Power-on reset is shown in Figure 11.
4-channel ultra-low voltage, Fm+ I²C-bus switch with reset

Table 6 specifies the performance of the power-on reset feature for PCA9846 for both types of power-on reset.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(dV/dt)ᵢ</td>
<td>fall rate of change of voltage</td>
<td>Figure 11</td>
<td>0.1</td>
<td>-</td>
<td>2000</td>
<td>ms</td>
</tr>
<tr>
<td>(dV/dt)ᵢ</td>
<td>rise rate of change of voltage</td>
<td>Figure 11</td>
<td>0.1</td>
<td>-</td>
<td>2000</td>
<td>ms</td>
</tr>
<tr>
<td>td(rst)</td>
<td>reset delay time</td>
<td>Figure 11; re-ramp time when V_DD2 drops to V_POR(min) − 50 mV or below 0.2 V to VSS</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>μs</td>
</tr>
<tr>
<td>ΔV_DD(gl)</td>
<td>glitch supply voltage difference</td>
<td>Figure 12</td>
<td>[1]</td>
<td>-</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>t_w(gl)/VDD</td>
<td>supply voltage glitch pulse width</td>
<td>Figure 12</td>
<td>[2]</td>
<td>-</td>
<td>10</td>
<td>μs</td>
</tr>
<tr>
<td>V_POR(trip)</td>
<td>power-on reset trip voltage</td>
<td>falling V_DD2</td>
<td>0.7</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>rising V_DD2</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>V</td>
</tr>
</tbody>
</table>

[1] Level that V_DD2 can glitch down to with a ramp rate = 0.4 μs/V, but not cause a functional disruption when t_w(gl)/VDD < 1 μs.

[2] Glitch width that will not cause a functional disruption when ΔV_DD(gl) = 0.5 × V_DD2.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t_w(gl)/VDD) and glitch height (ΔV_DD(gl)) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 12 and Table 6 provide more information on how to measure these specifications.

VPOR is critical to the power-on reset. V_POR is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_POR differs based on the V_DD2 being lowered to or from 0 V. Figure 13 and Table 6 provide more details on this specification.
Fig 13. Power-on reset voltage (V\textsubscript{POR})
6.7 Voltage level translation between I2C-buses

Today’s complex systems often use multiple power supplies to maximize power savings and to meet the operating specifications of the devices used. This means that various I2C-buses are also operating at differing voltage levels and cannot simply connect together. In addition, modern microcontrollers operate down to 0.8 V to save power, further complicating the connection of I2C-buses.

The PCA9846 is specifically designed to seamlessly handle these voltage level translation issues. Any combination of bus voltages can be intermixed on the PCA9846 and correctly translated to the other bus at Fm+ (1 MHz) speed.

Figure 14 shows a typical application. The microcontroller acts as the master and operates at 0.8 V with its I2C-bus swinging between 0 V and 0.8 V. The temperature sensor on channel 0 of the PCA9846 has a voltage of 3.3 V, while the GPIO Expander on channel 1 operates down to 1.8 V to interface with chip select and reset inputs on various other ICs also operating at 1.8 V. Channel 2 of the PCA9846 is connected to the I2C-bus of a power management device, operating at 2.5 V. The other channels of PCA9846 are simply left unconnected.

In this example, VDD1 of the PCA9846 is a bias supply and is set at the lowest bus voltage, or 0.8 V of the microcontroller. VDD1 sets the input switching points of each SCL and SDA at 0.3 × VDD1 for a LOW level and 0.7 × VDD1 for a HIGH level.

VDD2 is the core logic supply from which most of the PCA9846 circuitry runs and must be greater than 1.65 V.

The I2C-bus is open-drain, so pull-up resistors are needed on each I2C-bus segment. This is where the voltage level translation happens. The pass transistor internal to the PCA9846 limit the output voltage to the lower of VDD1 or VDD2. The pull-up resistors will then limit the HIGH level of each bus segment to the power supply of the devices on that segment. Note that the pull-up resistors on channel 0 are connected to 3.3 V, the and resisters on channel 1 are connected to 1.8 V, while the resistors on channel 2 are connected to 2.5 V — effectively translating the 0.8 V signal swing of the microcontroller to the correct voltage level for each peripheral.

It is possible to level shift from a higher voltage microcontroller connected to VDD1 to lower voltage peripherals on the downstream side — the opposite of this particular example, as long as VDD1 > 0.8 V and VDD2 > 1.65 V.

One thing to note is noise margin on each I2C-bus segment is somewhat reduced due to the input levels set by VDD1. Especially in this example, the I2C-bus LOW level is 0.3 × VDD1 or 0.24 V, so extreme care must be taken to ensure all bus segments meet this specification. It also means that static offset buffers may not work correctly if the offset side is connected to the PCA9846.

Another point to examine is that there is no buffering capability between the upstream and the downstream buses. This is simply a pass transistor, which acts like a switch and a series resistor, between these bus segments. The series resistance is the Ron of the pass transistor and is inversely proportional to the minimum of VDD1 + VTH or VDD2, where VTH is approximately 0.8 V. Refer to Table 8 for some representative Ron values. An upcoming application note will explain Ron more thoroughly. Therefore, a careful analysis of bus capacitance and pull-up resistor values is called for.
A further point to consider is pull-up resistor selection. Since multiple channels can be simultaneously selected, the pull-up resistors on each channel are connected in parallel. Ensure each device can correctly drive the effective pull-up resistor value and still meet the LOW-level specifications.

Fig 14. Typical application for PCA9846 with differing bus voltages
7. Characteristics of the I\textsuperscript{2}C-bus

The PCA9846 is an I\textsuperscript{2}C slave device. Data is exchanged between the master and the PCA9846 through write and read commands conforming to the I\textsuperscript{2}C-bus protocol. The two communication lines are SCL (serial clock) and SDA (serial data), both of which must be connected to $V_{DD1}$ through pull-up resistors.

7.1 Write commands

Data is transmitted to the PCA9846 by sending its device address and setting the Least Significant Bit (LSB) to a logic 0 (see Table 4 for device addresses), which the PCA9846 acknowledges (ACK). The control register byte is sent after the address that determines which downstream channel is connected to the upstream channel by bit 0 through bit 2. Bit 7 through bit 3 are ignored and can be written with any data. There is no limit on the number of bytes sent after the address and before a STOP condition, only the last byte written before the STOP condition is recognized and the selected channel is enabled only at the following STOP condition.

![Fig 15. Write control register](aaa-019449)

Refer to Table 4.

7.2 Read commands

Data is read from the PCA9846 by sending its device address and setting the Least Significant Bit (LSB) to a logic 1 (see Table 4 for device addresses), which the PCA9846 acknowledges. The control register byte is read by the master with each byte either ACK or NACK by the master. If the master ACKs the control register byte, it continues to send register data until the master NACKs, signaling the transaction is complete. There is no limit on the number of bytes read from the PCA9846.

The control register bit definitions are shown in Figure 10. Bit 0 through bit 2 will show the enabled channels (as determined by the last write).

![Fig 16. Read control register](aaa-019450)

Refer to Table 4.
8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to VSS (ground = 0 V).[1]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>supply voltage</td>
<td></td>
<td>-0.5</td>
<td>+4.0</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;I&lt;/sub&gt;</td>
<td>input voltage</td>
<td></td>
<td>-0.5</td>
<td>+4.0</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;I&lt;/sub&gt;</td>
<td>input current</td>
<td></td>
<td>-</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;O&lt;/sub&gt;</td>
<td>output current</td>
<td></td>
<td>-</td>
<td>±25</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>supply current</td>
<td></td>
<td>-</td>
<td>±100</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>ground supply current</td>
<td></td>
<td>-</td>
<td>±100</td>
<td>mA</td>
</tr>
<tr>
<td>P&lt;sub&gt;tot&lt;/sub&gt;</td>
<td>total power dissipation</td>
<td></td>
<td>-</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>T&lt;sub&gt;stg&lt;/sub&gt;</td>
<td>storage temperature</td>
<td>operating</td>
<td>-60</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;amb&lt;/sub&gt;</td>
<td>ambient temperature</td>
<td>operating</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

9. Static characteristics

Table 8. Static characteristics

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = −40 °C to +85 °C; unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DD1&lt;/sub&gt;</td>
<td>supply voltage 1</td>
<td>V&lt;sub&gt;DD1&lt;/sub&gt; = 3.6 V, V&lt;sub&gt;DD2&lt;/sub&gt; = 3.6 V; SC0 to SC7 and SD0 to SD7 not connected; RESET = V&lt;sub&gt;DD1&lt;/sub&gt;; A0 = A1 = SCL; continuous register read/write</td>
<td>0.8</td>
<td>-</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD2&lt;/sub&gt;</td>
<td>supply voltage 2</td>
<td></td>
<td>1.65</td>
<td>-</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;DD(VDD2)&lt;/sub&gt;</td>
<td>supply current on pin V&lt;sub&gt;DD2&lt;/sub&gt;</td>
<td></td>
<td>-</td>
<td>5</td>
<td>12</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD1&lt;/sub&gt; = 3.6 V, V&lt;sub&gt;DD2&lt;/sub&gt; = 3.6 V; SC0 to SC7 and SD0 to SD7 not connected; RESET = V&lt;sub&gt;DD1&lt;/sub&gt;; A0 = A1 = SCL; continuous register read/write</td>
<td>f&lt;sub&gt;SCL&lt;/sub&gt; = 0 kHz</td>
<td>-</td>
<td>1000</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>12</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>20</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65</td>
<td>150</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;DD(VDD1)&lt;/sub&gt;</td>
<td>supply current on pin V&lt;sub&gt;DD1&lt;/sub&gt;</td>
<td></td>
<td>-</td>
<td>5</td>
<td>+2</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD1&lt;/sub&gt; = 3.6 V, V&lt;sub&gt;DD2&lt;/sub&gt; = 3.6 V; SC0 to SC7 and SD0 to SD7 not connected; RESET = V&lt;sub&gt;DD1&lt;/sub&gt;; A0 = A1 = SCL; continuous register read/write</td>
<td>f&lt;sub&gt;SCL&lt;/sub&gt; = 0 kHz</td>
<td>-</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>15</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>45</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>VPOR</td>
<td>power-on reset voltage</td>
<td></td>
<td>-</td>
<td>1.2</td>
<td>1.5</td>
<td>V</td>
</tr>
</tbody>
</table>
Table 8. Static characteristics \( \ldots \) continued

\( V_{SS} = 0 \) V; \( T_{amb} = -40 \) °C to +85 °C; unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IL} )</td>
<td>LOW-level input voltage</td>
<td>( V_{DD1} \leq 1.1 ) V</td>
<td>-0.5</td>
<td>-</td>
<td>+0.2 ( V_{DD1} )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>HIGH-level input voltage</td>
<td>( V_{DD1} \leq 1.1 ) V</td>
<td>0.8 ( V_{DD1} )</td>
<td>-</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( I_{OL} )</td>
<td>LOW-level output current</td>
<td>( V_{OL} = 0.4 ) V; ( V_{DD2} \leq 2 ) V</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{L} )</td>
<td>leakage current</td>
<td>( V_{I} = V_{DD} ) or ( V_{SS} )</td>
<td>-1</td>
<td>-</td>
<td>+1</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( C_{i} )</td>
<td>input capacitance</td>
<td>( V_{I} = V_{SS} ); all channels disabled</td>
<td>-</td>
<td>20</td>
<td>40</td>
<td>pF</td>
</tr>
</tbody>
</table>

Select inputs A0 to A1, RESET

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IL} )</td>
<td>LOW-level input voltage</td>
<td>( V_{DD1} \leq 1.1 ) V</td>
<td>-0.5</td>
<td>-</td>
<td>+0.2 ( V_{DD1} )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>HIGH-level input voltage</td>
<td>( V_{DD1} = 1.1 ) V</td>
<td>0.8 ( V_{DD1} )</td>
<td>-</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( I_{LI} )</td>
<td>input leakage current</td>
<td>pin at ( V_{DD2} ) to 3.6 V or ( V_{SS} )</td>
<td>-1</td>
<td>-</td>
<td>+1</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( C_{i} )</td>
<td>input capacitance</td>
<td>( V_{I} = V_{SS} ) or ( V_{DD1} )</td>
<td>-</td>
<td>5</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

Pass gate

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{on} )</td>
<td>ON-state resistance</td>
<td>ON resistance of the pass transistor between SCL and SCx, and SDA and SDx</td>
<td>( V_{DD1} = 0.8 ) V; ( V_{DD2} \geq 1.65 ) V; ( V_{i(sw)} = 0.16 ) V; ( I_{O} = 3 ) mA</td>
<td>-</td>
<td>15</td>
<td>24</td>
</tr>
<tr>
<td>( I_{O(sw)} )</td>
<td>switch output current</td>
<td>( V_{DD2} = 1.65 ) V to 3.6 V; ( V_{i(sw)} = V_{DD1} = 3.6 ) V; ( V_{i(sw)} = V_{DD1} = 3.6 ) V</td>
<td>0</td>
<td>-</td>
<td>100</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( I_{L} )</td>
<td>leakage current</td>
<td>( V_{I} = V_{DD} ) or ( V_{SS} )</td>
<td>-1</td>
<td>-</td>
<td>+1</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( C_{io} )</td>
<td>input/output capacitance</td>
<td>( V_{I} = V_{SS} ); all switches disabled</td>
<td>-</td>
<td>8</td>
<td>15</td>
<td>pF</td>
</tr>
</tbody>
</table>

Ron = \frac{(Vo(sw) - V_{i(sw)})}{I_o}; V_{i(sw)} and I_o are defined in Table 8

Fig 17. Ron test circuit
### Table 9. Dynamic characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Standard-mode I²C-bus</th>
<th>Fast-mode I²C-bus</th>
<th>Fast-mode Plus I²C-bus</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>t_PD</td>
<td>propagation delay from SDA to SDx, or SCL to SCx</td>
<td></td>
<td>-</td>
<td>1[1]</td>
<td>-</td>
<td>1[1]</td>
</tr>
<tr>
<td>f_SCL</td>
<td>SCL clock frequency</td>
<td></td>
<td>0</td>
<td>100</td>
<td>0</td>
<td>400</td>
</tr>
<tr>
<td>t_BUF</td>
<td>bus free time between a STOP and START condition</td>
<td></td>
<td>4.7</td>
<td>-</td>
<td>1.3</td>
<td>-</td>
</tr>
<tr>
<td>t_HD;STA</td>
<td>hold time (repeated) START condition</td>
<td></td>
<td>4.0</td>
<td>-</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>t_LOW</td>
<td>LOW period of the SCL clock</td>
<td></td>
<td>4.7</td>
<td>-</td>
<td>1.3</td>
<td>-</td>
</tr>
<tr>
<td>t_HIGH</td>
<td>HIGH period of the SCL clock</td>
<td></td>
<td>4.0</td>
<td>-</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>t_SU;STA</td>
<td>set-up time for a repeated START condition</td>
<td></td>
<td>4.7</td>
<td>-</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>t_SU;STO</td>
<td>set-up time for STOP condition</td>
<td></td>
<td>4.0</td>
<td>-</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>t_HD;DAT</td>
<td>data hold time</td>
<td></td>
<td>0[3]</td>
<td>3.45</td>
<td>0[3]</td>
<td>0.9</td>
</tr>
<tr>
<td>t_SU;DAT</td>
<td>data set-up time</td>
<td></td>
<td>250</td>
<td>-</td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>t_r</td>
<td>rise time of both SDA and SCL signals</td>
<td></td>
<td>-</td>
<td>1000</td>
<td>-</td>
<td>20 × (V_DD / 5.5 V)[4]</td>
</tr>
<tr>
<td>t_f</td>
<td>fall time of both SDA and SCL signals</td>
<td></td>
<td>-</td>
<td>300</td>
<td>-</td>
<td>20 × (V_DD / 5.5 V)[4]</td>
</tr>
<tr>
<td>C_b</td>
<td>capacitive load for each bus line</td>
<td></td>
<td>-</td>
<td>400</td>
<td>-</td>
<td>400</td>
</tr>
<tr>
<td>t_SP</td>
<td>pulse width of spikes that must be suppressed by the input filter</td>
<td></td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>50</td>
</tr>
<tr>
<td>t_VD;DAT</td>
<td>data valid time</td>
<td></td>
<td>-</td>
<td>3.45</td>
<td>-</td>
<td>0.9</td>
</tr>
<tr>
<td>t_VD;ACK</td>
<td>data valid acknowledge time</td>
<td></td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>RESET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_\text{rst})_L</td>
<td>LOW-level reset time</td>
<td></td>
<td>100</td>
<td>-</td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>t_rst</td>
<td>reset time</td>
<td></td>
<td>SDA clear</td>
<td>500</td>
<td>-</td>
<td>500</td>
</tr>
<tr>
<td>t_REC;STA</td>
<td>recovery time to START condition</td>
<td></td>
<td>0</td>
<td>-</td>
<td>0</td>
<td>-</td>
</tr>
</tbody>
</table>
Pass gate propagation delay is calculated from the 20 Ω typical $R_{on}$ and the 50 pF load capacitance.

After this period, the first clock pulse is generated.

A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Necessary to be backwards compatible to Fast-mode.

In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

The maximum $t_{HD,DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD,DAT}$ or $t_{VD,ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

Fig 18. Definition of timing on the I²C-bus

Fig 19. Definition of RESET timing
Rise and fall times refer to $V_{IL}$ and $V_{IH}$.

Fig 20. I²C-bus timing diagram
11. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**DIMENSIONS (mm are the original dimensions)**

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A₁ (max.)</th>
<th>A₂</th>
<th>A₃</th>
<th>b_p</th>
<th>c</th>
<th>D₁</th>
<th>E₁</th>
<th>e</th>
<th>H_E</th>
<th>L</th>
<th>L_p</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>Z₁ (max)</th>
<th>θ</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>1.1</td>
<td>0.15</td>
<td>0.95</td>
<td>0.25</td>
<td>0.30</td>
<td>0.2</td>
<td>5.1</td>
<td>4.5</td>
<td>0.65</td>
<td>6.6</td>
<td>1</td>
<td>0.75</td>
<td>0.4</td>
<td>0.2</td>
<td>0.13</td>
<td>0.40</td>
<td>8°</td>
</tr>
</tbody>
</table>

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

---

**Fig 21. Package outline SOT403-1 (TSSOP16)**
HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm

**DIMENSIONS (mm are the original dimensions)**

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A(1)_{max.}</th>
<th>A_1</th>
<th>b</th>
<th>c</th>
<th>D_{h}</th>
<th>E(1)</th>
<th>E_{h}</th>
<th>e</th>
<th>e_1</th>
<th>e_2</th>
<th>L</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>y_1</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>1</td>
<td>0.05</td>
<td>0.38</td>
<td>0.23</td>
<td>4.1</td>
<td>3.9</td>
<td>2.25</td>
<td>4.1</td>
<td>3.9</td>
<td>2.25</td>
<td>0.65</td>
<td>1.95</td>
<td>1.95</td>
<td>0.75</td>
<td>0.50</td>
</tr>
</tbody>
</table>

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

---

**Fig 22. Package outline SOT629-1 (HVQFN16)**
12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities
12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11.

<table>
<thead>
<tr>
<th>Package thickness (mm)</th>
<th>Package reflow temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 2.5</td>
<td>235</td>
</tr>
<tr>
<td>≥ 2.5</td>
<td>220</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package thickness (mm)</th>
<th>Package reflow temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 1.6</td>
<td>260</td>
</tr>
<tr>
<td>1.6 to 2.5</td>
<td>260</td>
</tr>
<tr>
<td>&gt; 2.5</td>
<td>250</td>
</tr>
</tbody>
</table>

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.
For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

Fig 23. Temperature profiles for large and small components.
13. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP16 package

**Fig 24.** PCB footprint for SOT403-1 (TSSOP16); reflow soldering

<table>
<thead>
<tr>
<th>DIMENSIONS in mm</th>
<th>P1</th>
<th>P2</th>
<th>Ay</th>
<th>By</th>
<th>C</th>
<th>D1</th>
<th>D2</th>
<th>Gx</th>
<th>Gy</th>
<th>Hx</th>
<th>Hy</th>
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<tbody>
<tr>
<td></td>
<td>0.650</td>
<td>0.750</td>
<td>7.200</td>
<td>4.500</td>
<td>1.350</td>
<td>0.400</td>
<td>0.600</td>
<td>5.600</td>
<td>5.300</td>
<td>5.800</td>
<td>7.450</td>
</tr>
</tbody>
</table>

Refer to the package outline drawing for actual layout
Fig 25. PCB footprint for SOT629-1 (HVQFN16); reflow soldering
14. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>CDM</td>
<td>Charged-Device Model</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>ESD</td>
<td>ElectroStatic Discharge</td>
</tr>
<tr>
<td>Fm+</td>
<td>Fast-mode Plus</td>
</tr>
<tr>
<td>HBM</td>
<td>Human Body Model</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>I²C-bus</td>
<td>Inter-Integrated Circuit bus</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed-Circuit Board</td>
</tr>
<tr>
<td>SMBus</td>
<td>System Management Bus</td>
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15. Revision history

<table>
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<th>Data sheet status</th>
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<th>Supersedes</th>
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<td>20170404</td>
<td>Product data sheet</td>
<td>201703016I</td>
<td>PCA9846 v.1</td>
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Modifications:

- Section 6.7 "Voltage level translation between I²C-buses": Minor text edits to clarify operation of device.
- Table 1 "Ordering information": Corrected topside marking for PCA9846PW; no change to device.

| PCA9846 v.1  | 20151109     | Product data sheet | -             | -            |
16. Legal information

16.1 Data sheet status

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<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term ‘short data sheet’ is explained in section “Definitions”.
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at URL http://www.nxp.com.

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For sales office addresses, please send an email to: salesaddresses@nxp.com
## 18. Contents

1. General description ........................................... 1
2. Features and benefits ....................................... 1
3. Ordering information ......................................... 2
   3.1 Ordering options ........................................ 2
4. Block diagram ................................................ 3
5. Pinning information .......................................... 4
   5.1 Pinning .................................................. 4
   5.2 Pin description ......................................... 4
6. Functional description ....................................... 5
   6.1 Device address .......................................... 5
   6.2 Software Reset General Call, and device ID addresses .......... 6
   6.2.1 Software Reset ....................................... 7
   6.2.2 Device ID (PCA9846 ID field) .......................... 8
6.3 Control register ........................................... 9
   6.3.1 Control register definition ............................ 10
6.4 RESET input ............................................... 10
6.5 Power-on reset ............................................ 10
6.6 Power-on reset requirements .............................. 11
6.7 Voltage level translation between I2C-buses ................. 13
7. Characteristics of the I2C-bus ............................ 15
   7.1 Write commands ........................................ 15
   7.2 Read commands .......................................... 15
8. Limiting values ............................................... 16
9. Static characteristics ....................................... 16
10. Dynamic characteristics .................................... 19
11. Package outline ............................................ 22
12. Soldering of SMD packages ................................. 24
   12.1 Introduction to soldering ................................ 24
   12.2 Wave and reflow soldering .............................. 24
   12.3 Wave soldering ......................................... 24
   12.4 Reflow soldering ....................................... 25
13. Soldering: PCB footprints .................................. 27
14. Abbreviations ............................................... 29
15. Revision history ............................................. 29
16. Legal information ........................................... 30
   16.1 Data sheet status ...................................... 30
   16.2 Definitions ............................................ 30
   16.3 Disclaimers ............................................. 30
   16.4 Trademarks ............................................. 31
17. Contact information ......................................... 31
18. Contents .................................................... 32

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