PCU9656

24-bit UFm 5 MHz I^{2}C-bus 100 mA 40 V LED driver

Rev. 1 — 8 December 2011

Product data sheet

1. General description

The PCU9656 is a UFm I^{2}C-bus controlled 24-bit LED driver optimized for voltage switch dimming and blinking 100 mA Red/Green/Blue/Amber (RGBA) LEDs. Each LEDn output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz (typical) with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LEDn output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCU9656 operates with a supply voltage range of 2.3 V to 5.5 V and the 100 mA open-drain outputs allow voltages up to 40 V for the LED supply.

The PCU9656 is one of the first LED controller devices in a new Ultra Fast-mode (UFm) family. UFm devices offer higher frequency (up to 5 MHz).

The active LOW Output Enable input pin ($\overline{\text{OE}}$) blinks all the LEDn outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I^{2}C-bus addresses allow all or defined groups of PCU9656 devices to respond to a common I^{2}C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I^{2}C-bus commands. Six hardware address pins allow up to 64 devices on the same bus.

The Software Reset (SWRST) Call allows the master to perform a reset of the PCU9656 through the I^{2}C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output NAND FETs to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

A new feature to control LEDn output pattern is incorporated in the PCU9656. A new control byte called ‘Chase Byte’ allows enabling or disabling of selective LEDn outputs depending on the value of the Chase Byte. This feature greatly reduces the number of bytes to be sent to the PCU9656 when repetitive patterns need to be displayed as in creating a marquee chasing effect.

2. Features and benefits

- 24 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
- 5 MHz Ultra Fast-mode unidirectional I^{2}C-bus interface
- 256-step (8-bit) linear programmable brightness per LEDn output varying from fully off (default) to maximum brightness using a 97 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 24 Hz to 10.73 s and duty cycle from 0 % to 99.6 %
- 24 open-drain outputs can sink between 0 mA to 100 mA and are tolerant to a maximum off state voltage of 40 V. No input function.
- Output state change programmable on the Acknowledge (bit 9, this bit is always set to 1 by master) or the STOP Command to update outputs byte-by-byte or all at the same time (default to ‘Change on STOP’).
- Active LOW Output Enable ($\overline{\text{OE}}$) input pin allows for hardware blinking and dimming of the LEDs
- Six hardware address pins allow 64 PCU9656 devices to be connected to the same UFm I^{2}C-bus and to be individually programmed
- Four software programmable UFm I^{2}C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for ‘All Call’ so that all the PCU9656s on the I^{2}C-bus can be addressed at the same time and the second register used for three different addresses so that $^1/_3$ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for I^{2}C-bus address.
- A Chase Byte allows execution of predefined ON/OFF pattern for the 24 LEDn outputs
- Software Reset feature (SWRST Call) allows the device to be reset through the UFm I^{2}C-bus
- 25 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on USDA/USCL inputs
- Glitch-free LEDn outputs on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage (V_{DD}) range of 2.3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- –40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offered: LQFP48

3. Applications

- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCU9656B	PCU9656	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5. Block diagram

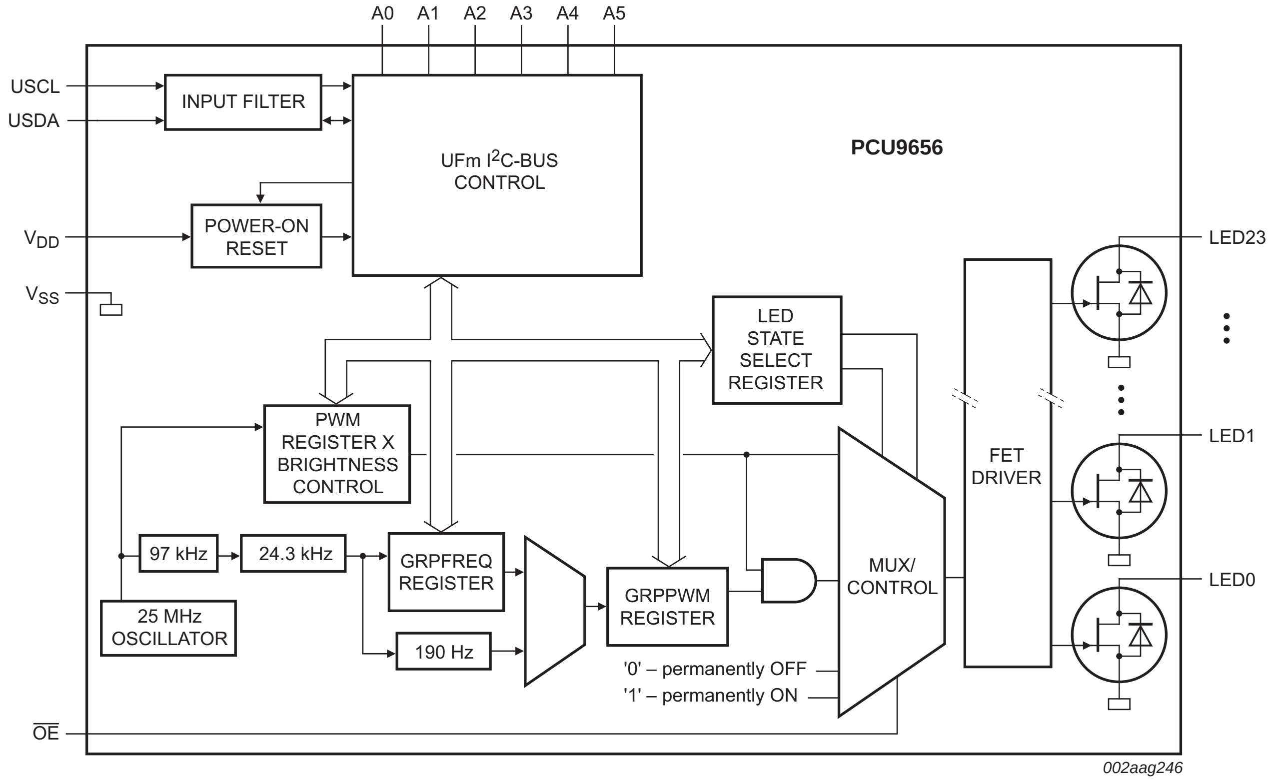


Fig 1. Block diagram of PCU9656

6. Pinning information

6.1 Pinning

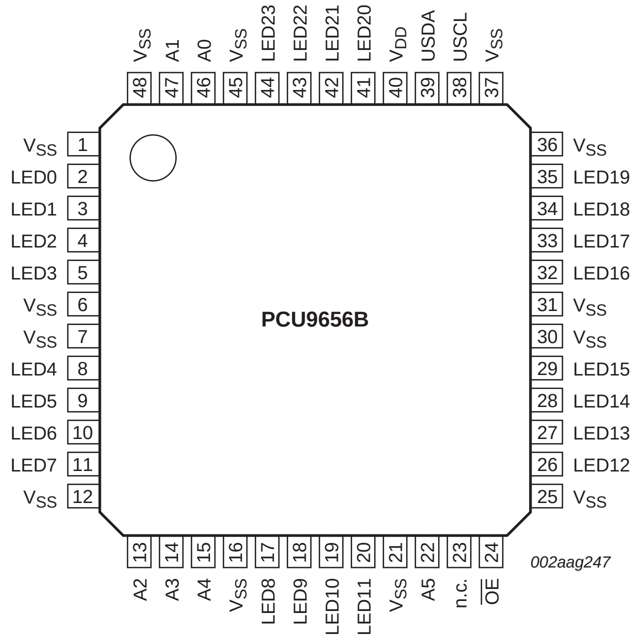


Fig 2. Pin configuration for LQFP48

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
V_{SS}	1, 6, 7, 12, 16, 21, 25, 30, 31, 36, 37, 45, 48	power supply	supply ground
LED0	2	O	LED driver 0
LED1	3	O	LED driver 1
LED2	4	O	LED driver 2
LED3	5	O	LED driver 3
LED4	8	O	LED driver 4
LED5	9	O	LED driver 5
LED6	10	O	LED driver 6
LED7	11	O	LED driver 7
A2	13	I	address input 2
A3	14	I	address input 3
A4	15	I	address input 4
LED8	17	O	LED driver 8
LED9	18	O	LED driver 9
LED10	19	O	LED driver 10

Table 2. Pin description *…continued*

Symbol	Pin	Type	Description
LED11	20	O	LED driver 11
A5	22	I	address input 5
n.c.	23	I	do not connect; reserved input
$\overline{\text{OE}}$	24	I	active LOW output enable for LEDs
LED12	26	O	LED driver 12
LED13	27	O	LED driver 13
LED14	28	O	LED driver 14
LED15	29	O	LED driver 15
LED16	32	O	LED driver 16
LED17	33	O	LED driver 17
LED18	34	O	LED driver 18
LED19	35	O	LED driver 19
USCL	38	I	UFm serial clock line
USDA	39	I	UFm serial data line
V_{DD}	40	power supply	supply voltage
LED20	41	O	LED driver 20
LED21	42	O	LED driver 21
LED22	43	O	LED driver 22
LED23	44	O	LED driver 23
A0	46	I	address input 0
A1	47	I	address input 1

7. Functional description

Refer to Figure 1 “Block diagram of PCU9656”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

There are a maximum of 64 possible programmable addresses using the six hardware address pins. One of these addresses cannot be used as it is reserved for Software Reset (SWRST), leaving a maximum of 63 addresses. Using other reserved addresses can reduce the total number of possible addresses even further.

7.1.1 Regular UFm I²C-bus slave address

The UFm I²C-bus slave address of the PCU9656 is shown in Figure 3. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW externally.

Remark: Using reserved I²C-bus addresses will interfere with other devices, but only if the devices are on the bus and/or the bus will be open to other I²C-bus systems at some later date. In a closed system where the designer controls the address assignment these addresses can be used since the PCU9656 treats them like any other address. The LED All Call and Software Reset and PCA9564 or PCA9665 slave address (if on the bus) can never be used for individual device addresses.

- PCU9656 LED All Call address (1110 000) and Software Reset (0000 0110) which are active on start-up
- PCA9564 (0000 000) or PCA9665 (1110 000) slave address which is active on start-up
- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

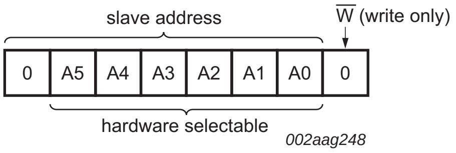


Fig 3. Slave address

The last bit of the address byte defines the operation to be performed. No Read available with UFm. For UFM I²C-bus, there is only write operation in slave device.

7.1.2 LED All Call UFm I^{2}C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000
- Programmable through I^{2}C-bus (volatile programming)
- At power-up, LED All Call I^{2}C-bus address is enabled

See Section 7.3.9 “ALLCALLADR, LED All Call UFm I^{2}C-bus address” for more detail.

Remark: The default LED All Call I^{2}C-bus address (E0h or 1110 000) must not be used as a regular I^{2}C-bus slave address since this address is enabled at power-up. All of the PCU9656s on the I^{2}C-bus will respond to the address if sent by the I^{2}C-bus master.

7.1.3 LED Sub Call UFm I^{2}C-bus addresses

- 3 different UFm I^{2}C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: E2h or 1110 001
  - SUBADR2 register: E4h or 1110 010
  - SUBADR3 register: E8h or 1110 100
- Programmable through UFm I^{2}C-bus (volatile programming)
- At power-up, all Sub Call UFm I^{2}C-bus addresses are disabled

See Section 7.3.8 “SUBADR1 to SUBADR3, UFm I^{2}C-bus subaddress 1 to 3” for more detail.

7.1.4 Software Reset UFm I^{2}C-bus address

The address shown in Figure 4 is used when a reset of the PCU9656 needs to be performed by the master. The Software Reset address (SWRST Call) must be used with $\overline{W}$ = logic 0. If $\overline{W}$ = logic 1, the PCU9656 does not recognize the SWRST. See Section 7.6 “Software reset” for more detail.

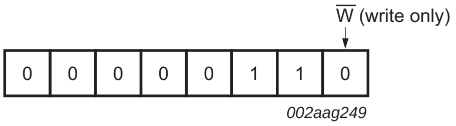


Fig 4. **Software Reset address**

Remark: The Software Reset UFm I^{2}C-bus address is a reserved address and cannot be used as a regular UFm I^{2}C-bus slave address or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCU9656, which will be stored in the Control register.

The lowest 6 bits are used as a pointer to determine which register will be accessed (D[5:0]). The highest bit is used as Auto-Increment Flag (AIF).

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature. Bit 6 of the Control register is not used.

reset state = 80h

Remark: The Control register does not apply to the Software Reset UFm I²C-bus address.

Fig 5. Control register

When the Auto-Increment Flag is set (AIF = logic 1), the six low order bits of the Control register are automatically incremented after a write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

Table 3. Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for all registers. D[5:0] roll over to 0h after the last register 26h is accessed.
1	0	1	Auto-Increment for individual brightness registers only. D[5:0] roll over to 02h after the last register (19h) is accessed.
1	1	0	Auto-Increment for global control registers and CHASE register. D[5:0] roll over to 1Ah after the last register (1Ch) is accessed.
1	1	1	Auto-Increment for individual brightness registers; global control registers and CHASE register. D[5:0] roll over to 02h after the last register (1Ch) is accessed.

[1] AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 3 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 24 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when the LED drivers must be globally programmed with different settings during the same I²C-bus communication, for example, global brightness or blinking change.

AIF + AI[1:0] = 111b is used when the 24 LED drivers must be individually programmed with different values in addition to global programming.

Only the 6 least significant bits D[5:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[5:0] is the first register that will be addressed (write operation), and can be anywhere between 0h and 26h (as defined in Table 4). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI2. See Table 3 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1010 0000, then the register addressing sequence will be (in hex):
20 → 21 → … → 26 → 0 → 1 → 2 → … → 19 → 02 → 03 → … → 19 → 02 … as long as the master keeps writing data.

7.3 Register definitions

Table 4. Register summary[1][2]

Register number (hex)	D5	D4	D3	D2	D1	D0	Name	Type	Function
00	0	0	0	0	0	0	MODE1	write only	Mode register 1
01	0	0	0	0	0	1	MODE2	write only	Mode register 2
02	0	0	0	0	1	0	PWM0	write only	brightness control LED0
03	0	0	0	0	1	1	PWM1	write only	brightness control LED1
04	0	0	0	1	0	0	PWM2	write only	brightness control LED2
05	0	0	0	1	0	1	PWM3	write only	brightness control LED3
06	0	0	0	1	1	0	PWM4	write only	brightness control LED4
07	0	0	0	1	1	1	PWM5	write only	brightness control LED5
08	0	0	1	0	0	0	PWM6	write only	brightness control LED6
09	0	0	1	0	0	1	PWM7	write only	brightness control LED7
0A	0	0	1	0	1	0	PWM8	write only	brightness control LED8
0B	0	0	1	0	1	1	PWM9	write only	brightness control LED9
0C	0	0	1	1	0	0	PWM10	write only	brightness control LED10
0D	0	0	1	1	0	1	PWM11	write only	brightness control LED11
0E	0	0	1	1	1	0	PWM12	write only	brightness control LED12
0F	0	0	1	1	1	1	PWM13	write only	brightness control LED13
10	0	1	0	0	0	0	PWM14	write only	brightness control LED14
11	0	1	0	0	0	1	PWM15	write only	brightness control LED15
12	0	1	0	0	1	0	PWM16	write only	brightness control LED16
13	0	1	0	0	1	1	PWM17	write only	brightness control LED17

Table 4. Register summary[1][2] *…continued*

Register number (hex)	D5	D4	D3	D2	D1	D0	Name	Type	Function
14	0	1	0	1	0	0	PWM18	write only	brightness control LED18
15	0	1	0	1	0	1	PWM19	write only	brightness control LED19
16	0	1	0	1	1	0	PWM20	write only	brightness control LED20
17	0	1	0	1	1	1	PWM21	write only	brightness control LED21
18	0	1	1	0	0	0	PWM22	write only	brightness control LED22
19	0	1	1	0	0	1	PWM23	write only	brightness control LED23
1A	0	1	1	0	1	0	GRPPWM	write only	group duty cycle control
1B	0	1	1	0	1	1	GRPFREQ	write only	group frequency
1C	0	1	1	1	0	0	CHASE	write only	chase control
1D	0	1	1	1	0	1	LEDOUT0	write only	LEDn output state 0
1E	0	1	1	1	1	0	LEDOUT1	write only	LEDn output state 1
1F	0	1	1	1	1	1	LEDOUT2	write only	LEDn output state 2
20	1	0	0	0	0	0	LEDOUT3	write only	LEDn output state 3
21	1	0	0	0	0	1	LEDOUT4	write only	LEDn output state 4
22	1	0	0	0	1	0	LEDOUT5	write only	LEDn output state 5
23	1	0	0	0	1	1	SUBADR1	write only	I^{2}C-bus subaddress 1
24	1	0	0	1	0	0	SUBADR2	write only	I^{2}C-bus subaddress 2
25	1	0	0	1	0	1	SUBADR3	write only	I^{2}C-bus subaddress 3
26	1	0	0	1	1	0	ALLCALLADR	write only	LED All Call I^{2}C-bus address

[1] Only D[5:0] = 00 0000 to 10 0110 are allowed and will be recognized. D[5:0] = 10 0111 to 11 1111 are reserved and may not be recognized.

[2] When writing to the Control register, bit 6 should be programmed with logic 0 for proper device operation.

7.3.1 Mode register 1, MODE1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AIF	not user programmable	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled (write default logic 1).
6	AI1	W	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 3.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 3.
5	AI0	W	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 3.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 3.
4	SLEEP	W	0	Normal mode[1].
			1*	Low power mode. Oscillator off[2].
3	SUB1	W	0*	PCU9656 does not respond to I²C-bus subaddress 1.
			1	PCU9656 responds to I²C-bus subaddress 1.
2	SUB2	W	0*	PCU9656 does not respond to I²C-bus subaddress 2.
			1	PCU9656 responds to I²C-bus subaddress 2.
1	SUB3	W	0*	PCU9656 does not respond to I²C-bus subaddress 3.
			1	PCU9656 responds to I²C-bus subaddress 3.
0	ALLCALL	W	0	PCU9656 does not respond to LED All Call I²C-bus address.
			1*	PCU9656 responds to LED All Call I²C-bus address.

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 1. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking or dimming is possible when the oscillator is off.

7.3.2 Mode register 2, MODE2

Table 6. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	not user programmable	0*	reserved, write must always be a logic 0
6	-	not user programmable	0*	reserved, write must always be a logic 0
5	DMBLNK	W	0*	group control = dimming.
			1	group control = blinking.
4	INVRT	W	0*	reserved, write must always be a logic 0
3	OCH	W	0*	outputs change on STOP command[1]
			1	outputs change on ninth clock cycle (SCL)
2	-	W	1*	reserved, write must always be a logic 1
1	-	W	0*	reserved, write must always be a logic 0
0	-	W	1*	reserved, write must always be a logic 1

[1] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCU9656. Applicable to registers from 02h (PWM0) to 22h (LEDOUT) only.

7.3.3 PWM0 to PWM23, individual brightness control

Table 7. PWM0 to PWM23 - PWM registers 0 to 23 (address 02h to 19h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	PWM0	7:0	IDC0[7:0]	W	0000 0000*	PWM0 Individual Duty Cycle
03h	PWM1	7:0	IDC1[7:0]	W	0000 0000*	PWM1 Individual Duty Cycle
04h	PWM2	7:0	IDC2[7:0]	W	0000 0000*	PWM2 Individual Duty Cycle
05h	PWM3	7:0	IDC3[7:0]	W	0000 0000*	PWM3 Individual Duty Cycle
06h	PWM4	7:0	IDC4[7:0]	W	0000 0000*	PWM4 Individual Duty Cycle
07h	PWM5	7:0	IDC5[7:0]	W	0000 0000*	PWM5 Individual Duty Cycle
08h	PWM6	7:0	IDC6[7:0]	W	0000 0000*	PWM6 Individual Duty Cycle
09h	PWM7	7:0	IDC7[7:0]	W	0000 0000*	PWM7 Individual Duty Cycle
0Ah	PWM8	7:0	IDC8[7:0]	W	0000 0000*	PWM8 Individual Duty Cycle
0Bh	PWM9	7:0	IDC9[7:0]	W	0000 0000*	PWM9 Individual Duty Cycle
0Ch	PWM10	7:0	IDC10[7:0]	W	0000 0000*	PWM10 Individual Duty Cycle
0Dh	PWM11	7:0	IDC11[7:0]	W	0000 0000*	PWM11 Individual Duty Cycle
0Eh	PWM12	7:0	IDC12[7:0]	W	0000 0000*	PWM12 Individual Duty Cycle
0Fh	PWM13	7:0	IDC13[7:0]	W	0000 0000*	PWM13 Individual Duty Cycle
10h	PWM14	7:0	IDC14[7:0]	W	0000 0000*	PWM14 Individual Duty Cycle
11h	PWM15	7:0	IDC15[7:0]	W	0000 0000*	PWM15 Individual Duty Cycle
12h	PWM16	7:0	IDC16[7:0]	W	0000 0000*	PWM16 Individual Duty Cycle
13h	PWM17	7:0	IDC17[7:0]	W	0000 0000*	PWM17 Individual Duty Cycle
14h	PWM18	7:0	IDC18[7:0]	W	0000 0000*	PWM18 Individual Duty Cycle
15h	PWM19	7:0	IDC19[7:0]	W	0000 0000*	PWM19 Individual Duty Cycle
16h	PWM20	7:0	IDC20[7:0]	W	0000 0000*	PWM20 Individual Duty Cycle
17h	PWM21	7:0	IDC21[7:0]	W	0000 0000*	PWM21 Individual Duty Cycle
18h	PWM22	7:0	IDC22[7:0]	W	0000 0000*	PWM22 Individual Duty Cycle
19h	PWM23	7:0	IDC23[7:0]	W	0000 0000*	PWM23 Individual Duty Cycle

A typical 97 kHz frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LEDn output off) to FFh (99.6 % duty cycle = LEDn output at maximum brightness). Applicable to LEDn outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT5 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \tag{1}$$

7.3.4 GRPPWM, group duty cycle control

Table 8. GRPPWM - Group brightness control register (address 1Ah) bit description
*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
1Ah	GRPPWM	7:0	GDC[7:0]	W	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190 Hz typical frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LEDn outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 24 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LEDn output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LEDn outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT5 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \tag{2}$$

7.3.5 GRPFREQ, group frequency

Table 9. GRPFREQ - Group Frequency register (address 1Bh) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	GRPFREQ	7:0	GFRQ[7:0]	W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a ‘Don’t care’ when DMBLNK = 0. Applicable to LEDn outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT5 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{24}(s) \tag{3}$$

7.3.6 CHASE control

Table 10. CHASE - Chase pattern control register (address 1Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
1Ch	CHASE	7:0	CHC[7:0]	W	0000 0000*	CHASE register

CHASE is used to program the LEDn output ON/OFF pattern. The contents of the CHASE register is used to enable one of the LEDn output patterns, as indicated in Table 11.

By repeated, sequential access to this table via the CHASE register, a chase pattern, e.g., marquee effect, can be easily programmed with minimal number of commands. Once the CHASE register is accessed, the data bytes that follow will be used as an index value to pick the LEDn output patterns defined by Table 11 “CHASE sequence”.

This register always updates on ninth clock cycle (USCL). It is used to gate the $\overline{OE}$ signal at each of the LEDn pins such that:

- $\overline{OE}$ = 1: all LEDs are off
- $\overline{OE}$ = 0: those LEDs corresponding to the ‘X’s in Table 11 are on

Any write to this register takes effect at the ninth clock cycle (USCL).

Table 11. CHASE sequence
X = enabled; empty cell = disabled.

Command	Hex	LED channel																								Description
		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
00	00	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	all LEDs ON
01	01																									all LEDs OFF
02	02		X		X		X		X		X		X		X		X		X		X		X		X	½ chase B
03	03	X		X		X		X		X		X		X		X		X		X		X		X		½ chase A
04	04			X			X			X			X			X			X			X			X	⅓ chase C
05	05		X			X			X			X			X			X			X			X		⅓ chase B
06	06	X			X			X			X			X			X			X			X			⅓ chase A
07	07	X																								LTR_0_ON (1× Left to Right_START)
08	08		X																							LTR_1_ON
09	09			X																						LTR_2_ON
10	0A				X																					LTR_3_ON
11	0B					X																				LTR_4_ON
12	0C						X																			LTR_5_ON
13	0D							X																		LTR_6_ON
14	0E								X																	LTR_7_ON
15	0F									X																LTR_8_ON
16	10										X															LTR_9_ON
17	11											X														LTR_10_ON
18	12												X													LTR_11_ON
19	13													X												LTR_12_ON
20	14														X											LTR_13_ON
21	15															X										LTR_14_ON
22	16																X									LTR_15_ON
23	17																	X								LTR_16_ON
24	18																		X							LTR_17_ON
25	19																			X						LTR_18_ON
26	1A																				X					LTR_19_ON
27	1B																					X				LTR_20_ON

Table 11. CHASE sequence *…continued*

X = enabled; empty cell = disabled.

Command	Hex	LED channel																								Description
		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
28	1C																						X			LTR_21_ON
29	1D																							X		LTR_22_ON
30	1E																								X	LTR_23_ON (1× Left to Right_END)
31	1F	X	X																							2× Left to Right_START
32	20			X	X																					
33	21					X	X																			
34	22							X	X																	
35	23									X	X															
36	24											X	X													
37	25													X	X											
38	26															X	X									
39	27																	X	X							
40	28																			X	X					
41	29																					X	X			
42	2A																							X	X	2× Left to Right_END
43	2B	X	X	X																						3× Left to Right_START
44	2C				X	X	X																			
45	2D							X	X	X																
46	2E										X	X	X													
47	2F													X	X	X										
48	30																X	X	X							
49	31																			X	X	X				
50	32																						X	X	X	3× Left to Right_END
51	33	X	X	X	X																					4× Left to Right_START
52	34					X	X	X	X																	
53	35									X	X	X	X													
54	36													X	X	X	X									
55	37																	X	X	X	X					

Table 11. CHASE sequence *…continued*

X = enabled; empty cell = disabled.

Command	Hex	LED channel																								Description
		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
56	38																					X	X	X	X	4× Left to Right_END
57	39	X	X	X	X	X																				5× Left to Right_START
58	3A						X	X	X	X	X															
59	3B											X	X	X	X	X										
60	3C																X	X	X	X	X					
61	3D																					X	X	X	X	5× Left to Right_END
62	3E	X	X	X	X	X	X																			6× Left to Right_START
63	3F							X	X	X	X	X	X													
64	40													X	X	X	X	X	X							
65	41																			X	X	X	X	X	X	6× Left to Right_END
66	42	X																							X	1× Implode_START
67	43		X																					X		
68	44			X																			X			
69	45				X																	X				
70	46					X															X					
71	47						X													X						
72	48							X											X							
73	49								X									X								
74	4A									X							X									
75	4B										X					X										
76	4C											X			X											
77	4D												X	X												1× Implode_END
78	4E	X	X																					X	X	2× Implode_START
79	4F			X	X																	X	X			
80	50					X	X													X	X					
81	51							X	X									X	X							
82	52									X	X					X	X									
83	53											X	X	X	X											
84	54												X	X												2× Implode_END

Table 11. CHASE sequence *…continued*

X = enabled; empty cell = disabled.

Command	Hex	LED channel																								Description
		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
85	55	X	X	X																			X	X	X	3× Implode_START
86	56				X	X	X													X	X	X				
87	57							X	X	X							X	X	X							
88	58										X	X	X	X	X	X										
89	59											X	X	X	X											
90	5A												X	X												3× Implode_END
91	5B	X	X	X	X																	X	X	X	X	4× Implode_START
92	5C					X	X	X	X									X	X	X	X					
93	5D									X	X	X	X	X	X	X	X									
94	5E											X	X	X	X											
95	5F												X	X												4× Implode_END
96	60	X																								Left to Right_WIPE_START
97	61	X	X																							
98	62	X	X	X																						
99	63	X	X	X	X																					
100	64	X	X	X	X	X																				
101	65	X	X	X	X	X	X																			
102	66	X	X	X	X	X	X	X																		
103	67	X	X	X	X	X	X	X	X																	
104	68	X	X	X	X	X	X	X	X	X																
105	69	X	X	X	X	X	X	X	X	X	X															
106	6A	X	X	X	X	X	X	X	X	X	X	X														
107	6B	X	X	X	X	X	X	X	X	X	X	X	X													
108	6C	X	X	X	X	X	X	X	X	X	X	X	X	X												
109	6D	X	X	X	X	X	X	X	X	X	X	X	X	X	X											
110	6E	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X										
111	6F	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X									
112	70	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
113	71	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X							

Table 11. CHASE sequence *…continued*

X = enabled; empty cell = disabled.

Command	Hex	LED channel																								Description
		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
114	72	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X						
115	73	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X					
116	74	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				
117	75	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
118	76	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
119	77	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Left to Right_WIPE_END
120	78																								X	Right to Left_WIPE_START
121	79																							X	X	
122	7A																						X	X	X	
123	7B																					X	X	X	X	
124	7C																				X	X	X	X	X	
125	7D																			X	X	X	X	X	X	
126	7E																		X	X	X	X	X	X	X	
127	7F																	X	X	X	X	X	X	X	X	
128	80																X	X	X	X	X	X	X	X	X	
129	81															X	X	X	X	X	X	X	X	X	X	
130	82														X	X	X	X	X	X	X	X	X	X	X	
131	83													X	X	X	X	X	X	X	X	X	X	X	X	
132	84												X	X	X	X	X	X	X	X	X	X	X	X	X	
133	85											X	X	X	X	X	X	X	X	X	X	X	X	X	X	
134	86										X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
135	87									X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
136	88								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
137	89							X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
138	8A						X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
139	8B					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
140	8C				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
141	8D			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Table 11. CHASE sequence *…continued*

X = enabled; empty cell = disabled.

Command	Hex	LED channel																								Description
		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
142	8E		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
143	8F	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Right to Left_WIPE_END
144	90																									All LEDn outputs disabled for CHASE byte = 90h to FFh. Reserved for future use. CHASE byte = FFh is used to exit the CHASE mode.

7.3.7 LEDOUT0 to LEDOUT5, LED driver output state

Table 12. LEDOUT0 to LEDOUT5 - LED driver output state register (address 1Dh to 22h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
1Dh	LEDOUT0	7:6	LDR3	W	00*	LED3 output state control
		5:4	LDR2	W	00*	LED2 output state control
		3:2	LDR1	W	00*	LED1 output state control
		1:0	LDR0	W	00*	LED0 output state control
1Eh	LEDOUT1	7:6	LDR7	W	00*	LED7 output state control
		5:4	LDR6	W	00*	LED6 output state control
		3:2	LDR5	W	00*	LED5 output state control
		1:0	LDR4	W	00*	LED4 output state control
1Fh	LEDOUT2	7:6	LDR11	W	00*	LED11 output state control
		5:4	LDR10	W	00*	LED10 output state control
		3:2	LDR9	W	00*	LED9 output state control
		1:0	LDR8	W	00*	LED8 output state control
20h	LEDOUT3	7:6	LDR15	W	00*	LED15 output state control
		5:4	LDR14	W	00*	LED14 output state control
		3:2	LDR13	W	00*	LED13 output state control
		1:0	LDR12	W	00*	LED12 output state control
21h	LEDOUT4	7:6	LDR19	W	00*	LED19 output state control
		5:4	LDR18	W	00*	LED18 output state control
		3:2	LDR17	W	00*	LED17 output state control
		1:0	LDR16	W	00*	LED16 output state control
22h	LEDOUT5	7:6	LDR23	W	00*	LED23 output state control
		5:4	LDR22	W	00*	LED22 output state control
		3:2	LDR21	W	00*	LED21 output state control
		1:0	LDR20	W	00*	LED20 output state control

LDRx = 00 — LED driver x is off (default power-up state).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.8 SUBADR1 to SUBADR3, UFm I^{2}C-bus subaddress 1 to 3

Table 13. SUBADR1 to SUBADR3 - UFm I^{2}C-bus subaddress registers 1 to 3 (address 23h to 25h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
23h	SUBADR1	7:1	A1[7:1]	W	1110 001*	I^{2}C-bus subaddress 1
		0	A1[0]	W only	0*	reserved (must write logic 0)
24h	SUBADR2	7:1	A2[7:1]	W	1110 010*	I^{2}C-bus subaddress 2
		0	A2[0]	W only	0*	reserved (must write logic 0)
25h	SUBADR3	7:1	A3[7:1]	W	1110 100*	I^{2}C-bus subaddress 3
		0	A3[0]	W only	0*	reserved (must write logic 0)

Subaddresses are programmable through the UFm I^{2}C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not recognize these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device recognize these addresses (MODE1 register).

Only the 7 MSBs representing the I^{2}C-bus subaddress are valid. The LSB in SUBADRx register is a reserved bit and must write logic 0.

When SUBx is set to logic 1 in MODE1 register, the corresponding I^{2}C-bus subaddress can be used during a UFm I^{2}C-bus write sequence.

7.3.9 ALLCALLADR, LED All Call UFm I^{2}C-bus address

Table 14. ALLCALLADR - LED All Call UFm I^{2}C-bus address register (address 26h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
26h	ALLCALLADR	7:1	AC[7:1]	W	1110 000*	ALLCALL I^{2}C-bus address register
		0	AC[0]	W only	0*	reserved (must write logic 0)

The LED All Call I^{2}C-bus address allows all the PCU9656s on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 (power-up default state)). This address is programmable through the I^{2}C-bus and can be used during a UFm I^{2}C-bus write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I^{2}C-bus address are valid. The LSB in ALLCALLADR register is a reserved bit and must write logic 0.

If ALLCALL bit = 0 in MODE1 register, the device does not recognize the address programmed in register ALLCALLADR.

7.4 Active LOW output enable input

The active LOW output enable ($\overline{\text{OE}}$) pin, allows to enable or disable all the LEDn outputs at the same time.

- When a LOW level is applied to $\overline{\text{OE}}$ pin, all the LEDn outputs are enabled as defined by the CHASE register.
- When a HIGH level is applied to $\overline{\text{OE}}$ pin, all the LEDn outputs are high-impedance.

The $\overline{\text{OE}}$ pin can be used as a synchronization signal to switch on/off several PCU9656 devices at the same time. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{\text{OE}}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{\text{OE}}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{\text{OE}}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

Remark: During power-down, slow decay of voltage supplies may keep LEDs illuminated. Consider disabling LEDn outputs using HIGH level applied to $\overline{\text{OE}}$ pin.

7.5 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCU9656 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCU9656 registers and I^{2}C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.6 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the UFm I^{2}C-bus to be reset to the power-up state value through a specific formatted I^{2}C-bus command.

The SWRST Call function is defined as the following:

1. A START command is sent by the UFm I^{2}C-bus master.
2. The reserved SWRST UFm I^{2}C-bus address ‘0000 011’ with the R/$\overline{\text{W}}$ bit set to ‘0’ (write) is sent by the I^{2}C-bus master.
3. Since PCU9656 is a UFm I^{2}C-bus device, no acknowledge is returned to the I^{2}C-bus master.
4. Once the SWRST Call address has been sent, the master sends 2 bytes with two specific values (SWRST data byte 1 and byte 2): Byte 1 = A5h, Byte 2 = 5Ah.

   If more than 2 bytes of data are sent, they will be ignored by the PCU9656.

5. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent, the master sends a STOP command to end the SWRST Call: the PCU9656 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

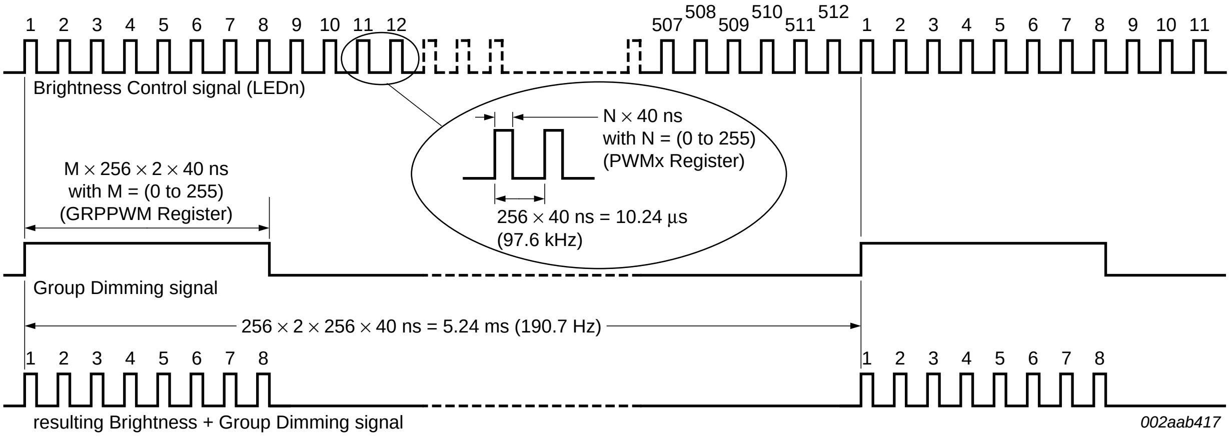
Remark: The reset stage is also the standby state with the internal oscillator turned off. It takes 500 μs for the oscillator to be up and running once the SLEEP bit has been set to a logic 1. PWM registers should not be accessed within the 500 μs window.

7.7 Individual brightness control with group dimming/blinking

A 97 kHz typical frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 24 LEDn outputs):

- A lower 190 Hz typical frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to $\frac{1}{10.73}$ Hz (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 40 ns.

Minimum pulse width for Group Dimming is 20.48 μs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 2 pulses of the LED Brightness Control signal (pulse width = N × 40 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 4 (8 pulses).

Fig 6. Brightness + Group Dimming signals

8. Characteristics of the PCU9656 Ultra Fast-mode I²C-bus

The PCU9656 LED controller uses the new Ultra Fast-mode (UFm) I²C-bus to communicate with the UFm I²C-bus capable host controller. It uses two lines for communication. They are a serial data line (USDA) and a serial clock line (USCL). The UFm is a unidirectional bus that is capable of higher frequency (up to 5 MHz). The UFm I²C-bus slave devices operate in receive-only mode. That is, only I²C writes to PCU9656 are supported.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the USDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

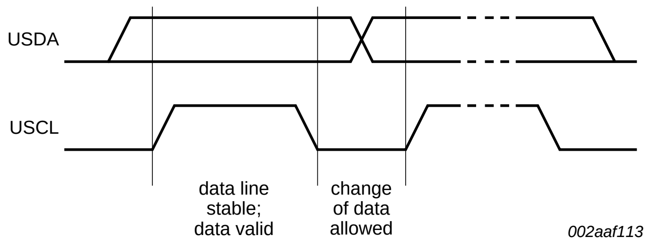


Fig 7. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 8).

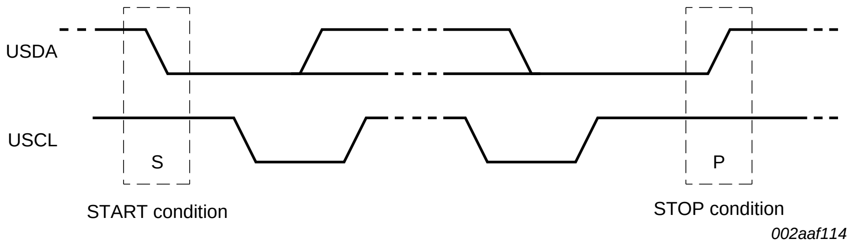


Fig 8. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 9).

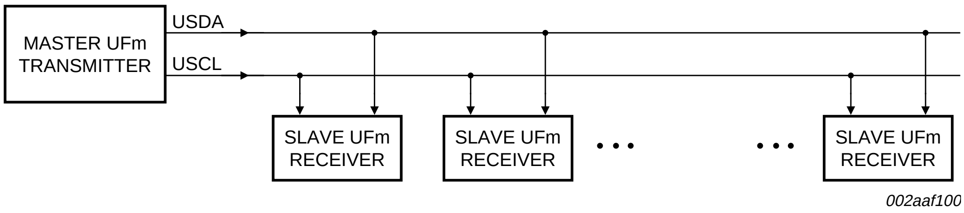


Fig 9. System configuration

8.3 Data transfer

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one bit that is always set to 1. The master generates an extra related clock pulse.

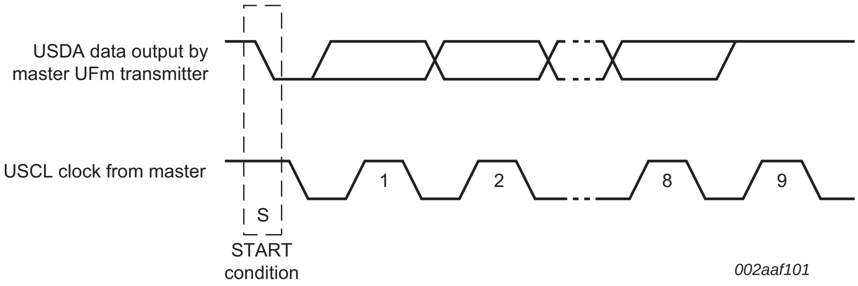
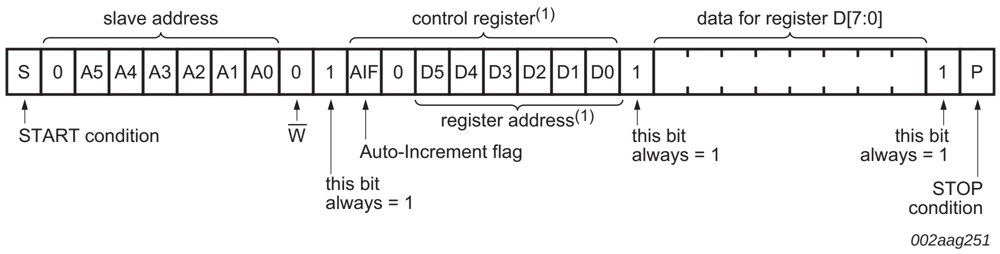


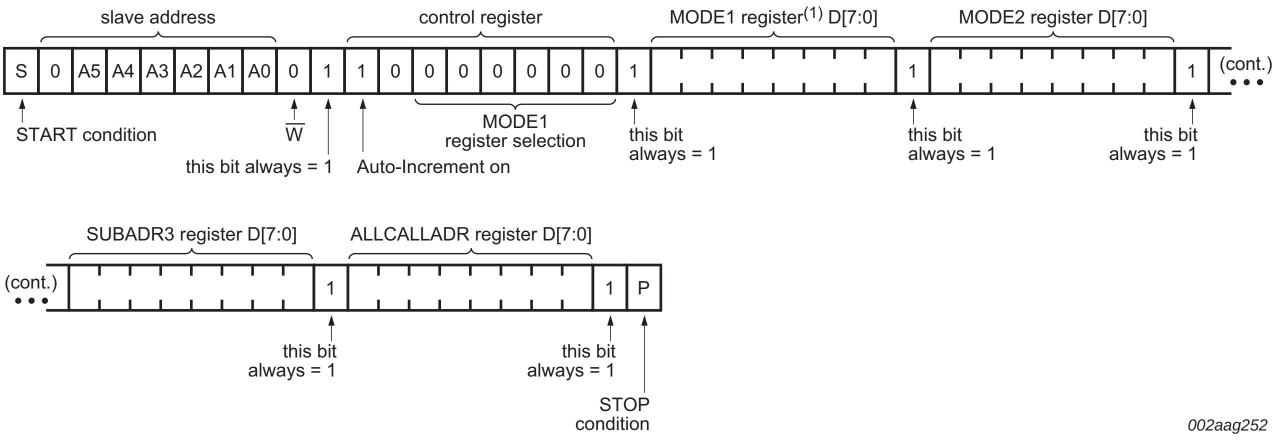
Fig 10. Data transfer

9. Bus transactions



(1) See Table 4 for register definition.

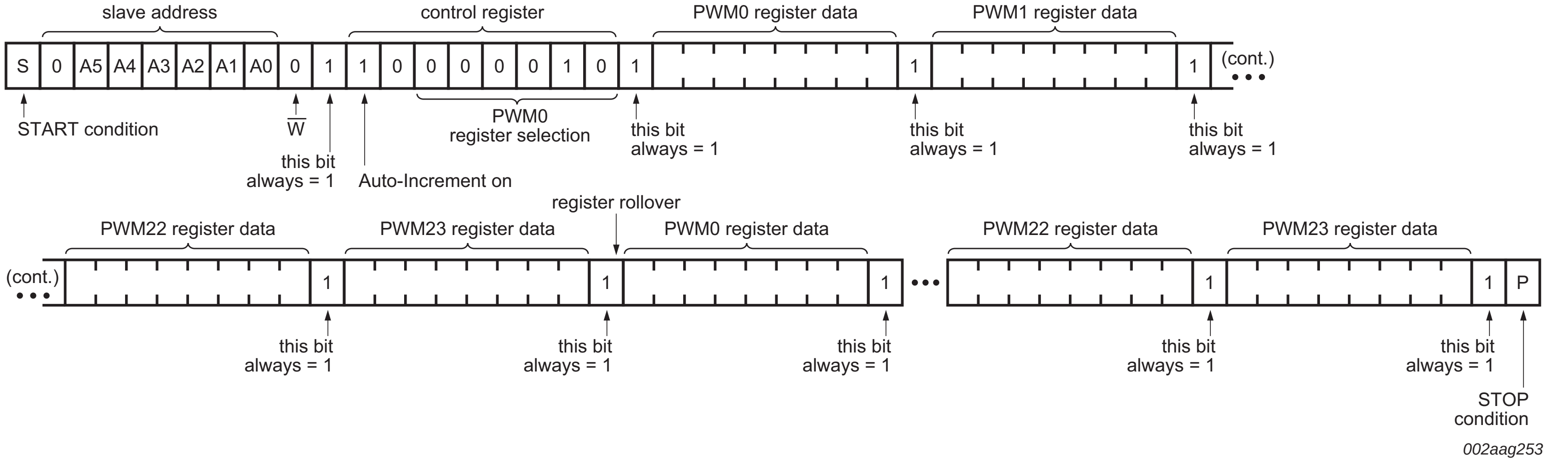
Fig 11. Write to a specific register



(1) AI1, AI0 = 00b. See Table 3 for Auto-Increment options.

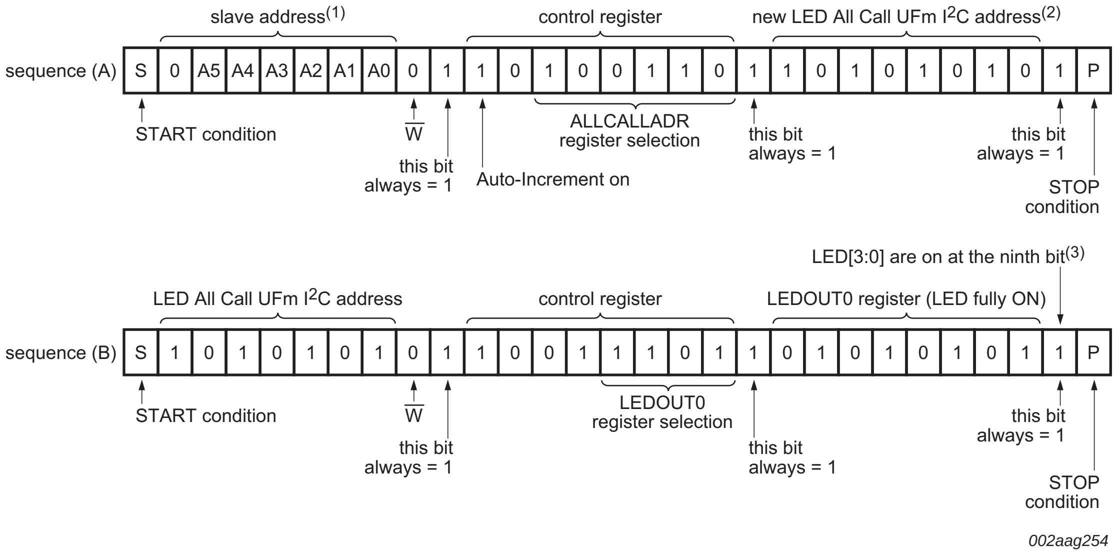
Remark: Care should be taken to load the appropriate value here in the AI1 and AI0 bits of the MODE1 register for programming the part with the required Auto-Increment options.

Fig 12. Write to all registers using the Auto-Increment feature



This example assumes that AIF + AI[1:0] = 101b.

Fig 13. Multiple writes to Individual Brightness registers only using the Auto-Increment feature



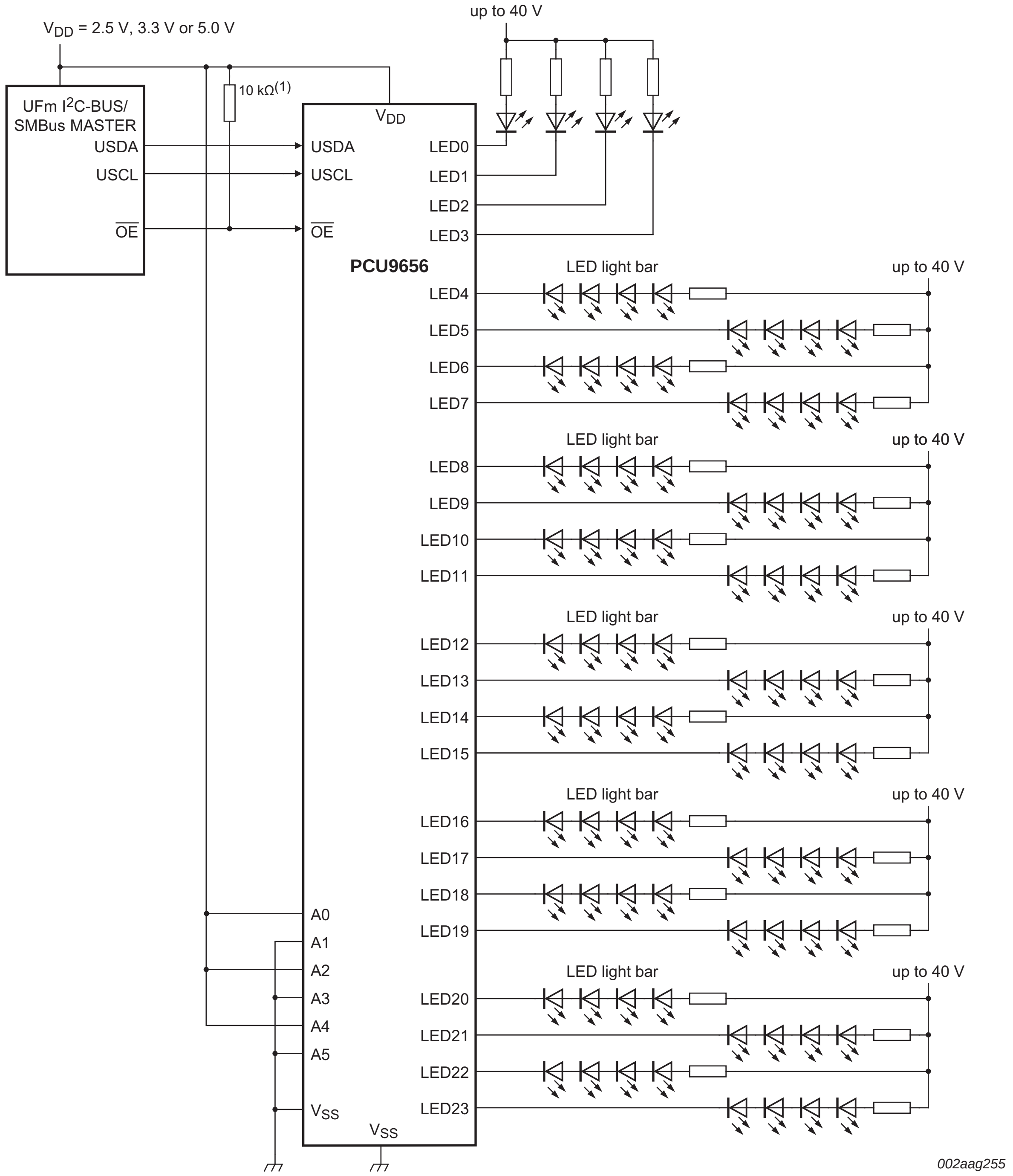
(1) In this example, several PCU9656s are used and the same sequence (A) (above) is sent to each of them.

(2) ALLCALL bit in MODE1 register is previously set to 1 for this example.

(3) OCH bit in MODE2 register is previously set to 1 for this example.

Fig 14. LED All Call UFm I²C-bus address programming and LED All Call sequence example

10. Application design-in information



(1) OE requires pull-up resistor if control signal from the master is open-drain.

I^{2}C-bus address = 0010 101x.

Remark: During power-down, slow decay of voltage supplies may keep LEDs illuminated. Consider disabling LEDn outputs using HIGH level applied to OE pin.

Fig 15. Typical application

10.1 Junction temperature calculation

A device junction temperature can be calculated when the ambient temperature or the case temperature is known.

When the ambient temperature is known, the junction temperature is calculated using Equation 4 and the ambient temperature, junction to ambient thermal resistance and power dissipation.

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{tot} \quad (4)$$

where:

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = junction to ambient thermal resistance

P_{tot} = (device) total power dissipation

When the case temperature is known, the junction temperature is calculated using Equation 5 and the case temperature, junction to case thermal resistance and power dissipation.

$$T_j = T_{case} + R_{th(j\text{-}c)} \times P_{tot} \quad (5)$$

where:

T_j = junction temperature

T_{case} = case temperature

$R_{th(j\text{-}c)}$ = junction to case thermal resistance

P_{tot} = (device) total power dissipation

Here are two examples regarding how to calculate the junction temperature using junction to case and junction to ambient thermal resistance. In the first example (Section 10.1.1), given the operating condition and the junction to ambient thermal resistance, the junction temperature of PCU9656B, in the LQFP48 package, is calculated for a system operating condition in 50 °C[1] ambient temperature. In the second example (Section 10.1.2), based on a specific customer application requirement where only the case temperature is known, applying the junction to case thermal resistance equation, the junction temperature of the PCU9656B, in the LQFP48 package, is calculated.

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[1] 50 °C is a typical temperature inside an enclosed system. The designers should feel free, as needed, to perform their own calculation using the examples.

10.1.1 Example 1: T_j calculation when T_{amb} is known (PCU9656B, LQFP48)

$R_{th(j-a)}$ = 63 °C/W

T_{amb} = 50 °C

LEDn output low voltage (LED V_{OL}) = 0.5 V

LEDn output current per channel = 80 mA

Number of outputs = 24

$I_{DD(max)}$ = 18 mA

$V_{DD(max)}$ = 5.5 V

1. Find P_{tot} (device total power dissipation):
   - output total power = 80 mA × 24 × 0.5 V = 960 mW
   - chip core power consumption = 18 mA × 5.5 V = 99 mW

   P_{tot} = (960 + 99 + 10 + 10) mW = **1059 mW**
2. Find T_j (junction temperature):

   $T_j = (T_{amb} + R_{th(j-a)} \times P_{tot})$ = (50 °C + 63 °C/W × 1059 mW) = **116.7 °C**

10.1.2 Example 2: T_j calculation where only T_{case} is known

This example uses a customer's specific application of the PCU9656B, 24-channel LED controller in the LQFP48 package, where only the case temperature (T_{case}) is known.

$T_j = T_{case} + R_{th(j-c)} \times P_{tot}$, where:

$R_{th(j-c)}$ = 18 °C/W

T_{case} (measured) = 94.6 °C

V_{OL} of LED ~ 0.5 V

$I_{DD(max)}$ = 18 mA

$V_{DD(max)}$ = 5.5 V

LEDn output voltage LOW = 0.5 V

LEDn output current:

60 mA on 1 port = (60 mA × 1)

50 mA on 6 ports = (50 mA × 6)

40 mA on 2 ports = (40 mA × 2)

20 mA on 12 ports = (20 mA × 12)

1 mA on 3 ports = (1 mA × 3)

1. Find P_{tot} (device total power dissipation)
    - output current (60 mA × 1 port); output power (60 mA × 1 × 0.5 V) = 30 mW
    - output current (50 mA × 6 ports); output power (50 mA × 6 × 0.5 V) = 150 mW
    - output current (40 mA × 2 ports); output power (40 mA × 2 × 0.5 V) = 40 mW
    - output current (20 mA × 12 ports); output power (20 mA × 12 × 0.5 V) = 120 mW
    - output current (1 mA × 3 ports); output power (1 mA × 3 × 0.5 V) = 1.5 mW

    Output total power = **341.5 mW**

    - chip core power consumption = 18 mA × 5.5 V = 99 mW

    P_{tot} (device total power dissipation) = **440.5 mW**
2. Find T_j (junction temperature):

    $T_j = T_{case} + R_{th(j\text{-}a)} \times P_{tot}$ = 94.6 °C + 18 °C/W × 440.5 mW = **102.5 °C**

11. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin			V_{SS} – 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage			V_{SS} – 0.5	40	V
$I_{O(LEDn)}$	output current on pin LEDn			-	100	mA
$I_{OL(tot)}$	total LOW-level output current	LED driver outputs; V_{OL} = 0.5 V	[1]	2400	-	mA
I_{SS}	ground supply current	per V_{SS} pin		-	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C		-	1.8	W
		T_{amb} = 85 °C		-	0.72	W
P/ch	power dissipation per channel	T_{amb} = 25 °C		-	100	mW
		T_{amb} = 85 °C		-	45	mW
T_j	junction temperature		[2]	-	+125	°C
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature	operating		–40	+85	°C

[1] Each bit must be limited to a maximum of 100 mA and the total package limited to 2400 mA due to internal busing limits.

[2] Refer to Section 10.1 for calculation.

Table 16. LQFP48 power dissipation and output current capability

Measurement	LQFP48
T_{amb} = 25 °C	
maximum power dissipation (chip + output drivers)	1590 mW
maximum power dissipation (output drivers only)	1460 mW
maximum drive current per channel	$< \frac{1460\ mW}{24\text{-}bit \times 0.5\ V} = 121.7\ mA$ [1]
T_{amb} = 60 °C	
maximum power dissipation (chip + output drivers)	1030 mW
maximum power dissipation (output drivers only)	901 mW
maximum drive current per channel	$< \frac{901\ mW}{24\text{-}bit \times 0.5\ V} = 75.1\ mA$
T_{amb} = 80 °C	
maximum power dissipation (chip + output drivers)	714 mW
maximum power dissipation (output drivers only)	585 mW
maximum drive current per channel	$< \frac{585\ mW}{24\text{-}bit \times 0.5\ V} = 48.8\ mA$

[1] This value signifies package’s ability to handle more than 100 mA per output driver. The device’s maximum current rating per output is 100 mA.

12. Thermal characteristics

Table 17. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	LQFP48	[1]	63	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case	LQFP48	[1]	18	°C/W

[1] Calculated in accordance with JESD 51-7.

13. Static characteristics

Table 18. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	on pin V_{DD}; operating mode; no load; f_{USCL} = 5 MHz				
		V_{DD} = 2.7 V	-	0.5	5.5	mA
		V_{DD} = 3.6 V	-	1.5	8	mA
		V_{DD} = 5.5 V	-	17	25	mA
I_{stb}	standby current	on pin V_{DD}; no load; f_{USCL} = 0 Hz; I/O = inputs; $V_I = V_{DD}$				
		V_{DD} = 2.7 V	-	0.5	5	µA
		V_{DD} = 3.6 V	-	1.0	10	µA
		V_{DD} = 5.5 V	-	6	15	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS} [1]	-	1.70	2.0	V
UFm I^{2}C-bus inputs USCL and USDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	6	10	pF
LED driver outputs (LED[23:0])						
$V_{drv(LED)}$	LED driver voltage		0	-	40	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; $V_{DD} \geq$ 4.5 V [2]	100	-	-	mA
I_{LOH}	HIGH-level output leakage current	$V_{drv(LED)}$ = 5 V	-	-	±1	µA
		$V_{drv(LED)}$ = 40 V	-	±1	15	µA
R_{on}	ON-state resistance	V_{OL} = 0.5 V; V_{DD} = 2.3 V	-	2	5	Ω
C_o	output capacitance		-	15	40	pF
$\overline{\text{OE}}$ input						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.7	5	pF
Address inputs (A[5:0])						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each bit must be limited to a maximum of 100 mA and the total package limited to 2400 mA due to internal busing limits.

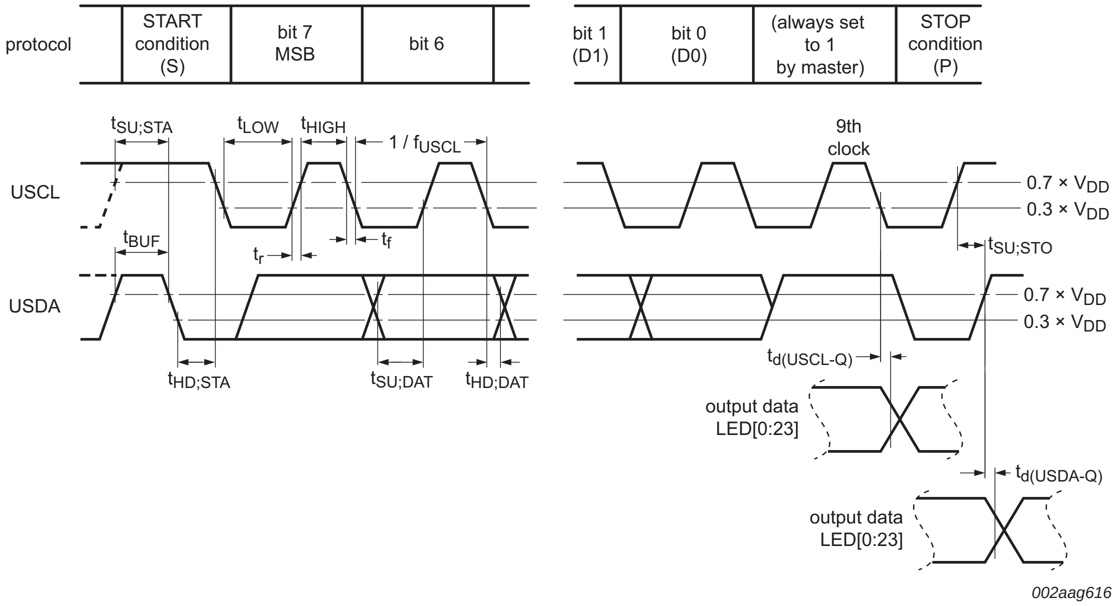
14. Dynamic characteristics

Table 19. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{USCL}	USCL clock frequency		-	-	5	MHz
t_{BUF}	bus free time between a STOP and START condition		0.08	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.05	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.05	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition		0.05	-	-	µs
$t_{HD;DAT}$	data hold time		10	-	-	ns
$t_{SU;DAT}$	data set-up time		30	-	-	ns
t_{LOW}	LOW period of the USCL clock		0.05	-	-	µs
t_{HIGH}	HIGH period of the USCL clock		0.05	-	-	µs
t_f	fall time of both USDA and USCL signals		-	-	50	ns
t_r	rise time of both USDA and USCL signals		-	-	50	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	10	ns
Output propagation delay						
t_{PLH}	LOW to HIGH propagation delay	$\overline{OE}$ to LEDn; MODE2[1:0] = 01	-	-	150	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{OE}$ to LEDn; MODE2[1:0] = 01	-	-	150	ns
Output port timing[1][2]						
$t_{d(USCL-Q)}$	delay time from USCL to data output	USCL to LEDn; MODE2[3] = 1; LEDOUTx = 01; outputs change on ninth clock cycle (USCL)	-	-	450	ns
$t_{d(USDA-Q)}$	delay time from USDA to data output	USDA to LEDn; MODE2[3] = 0; LEDOUTx = 01; outputs change on STOP condition	-	-	450	ns

[1] For LED off to fully on, LED fully on to off, or LED individual brightness control to off.

[2] For LED off to individual brightness control or changes in the individual brightness control value, there is a synchronization that may take up to 15 µs for the change to take effect.



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 16. UFm I^{2}C-bus timing and output timing diagram

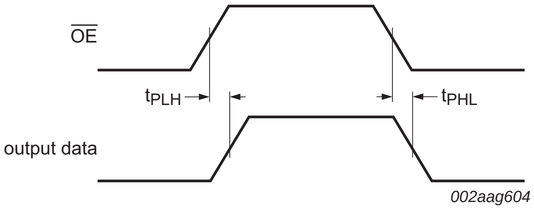
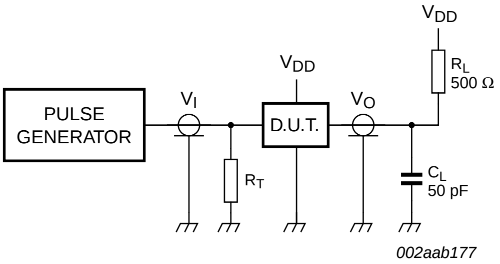


Fig 17. Output propagation delay

15. Test information



R_L = Load resistor for LEDn.

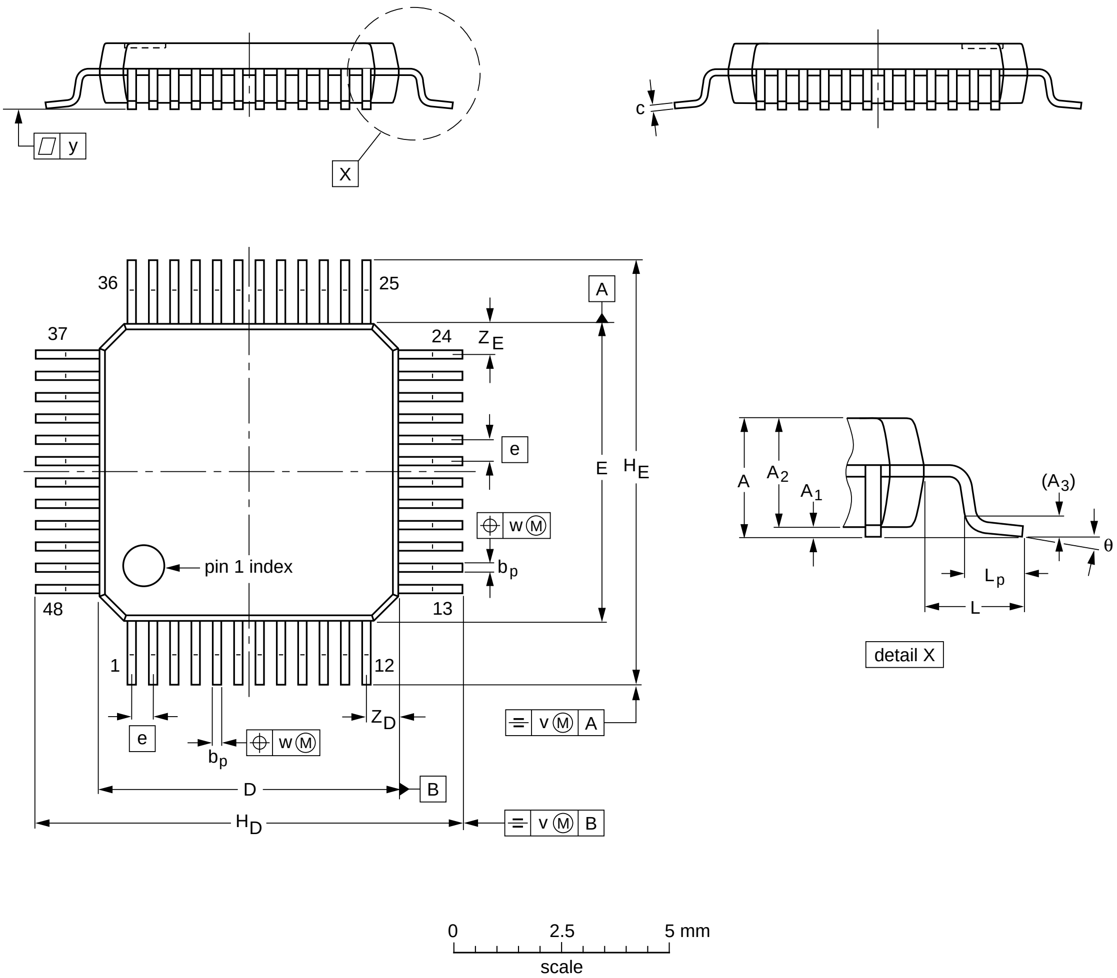
C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 18. Test circuitry for switching times

16. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 19. Package outline SOT313-2 (LQFP48)

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 20 and 21

Table 20. SnPb eutectic process (from J-STD-020C)

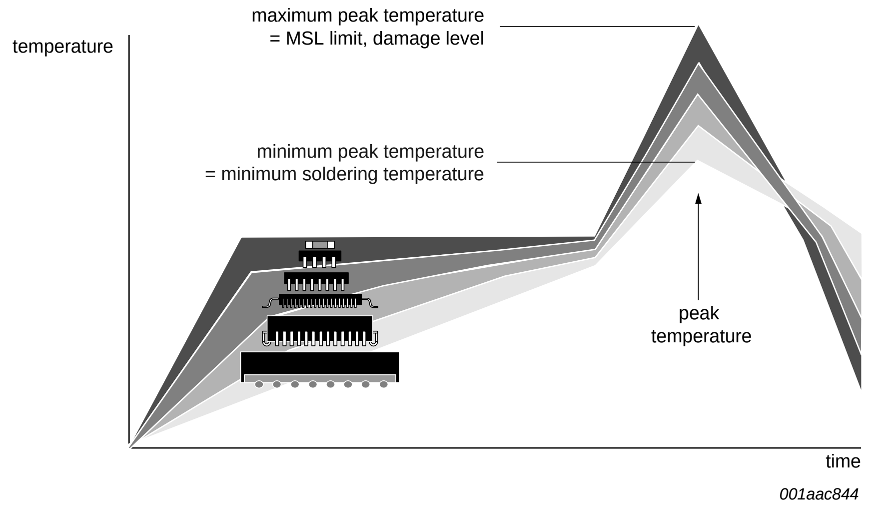
Package thickness (mm)	**Package reflow temperature (°C)**	
	Volume (mm^3)	
	< 350	**≥ 350**
< 2.5	235	220
≥ 2.5	220	220

Table 21. Lead-free process (from J-STD-020C)

Package thickness (mm)	**Package reflow temperature (°C)**		
	Volume (mm^3)		
	< 350	**350 to 2000**	**> 2000**
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.



MSL: Moisture Sensitivity Level

Fig 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

19. Abbreviations

Table 22. Abbreviations

Acronym	Description
ACK	Acknowledge
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
I^{2}C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus
UFm	Ultra-Fast mode (I^{2}C-bus)

20. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCU9656 v.1	20111208	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Contact information

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