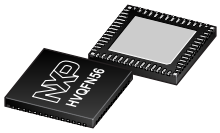
PF09

Nine-channel power management IC with advanced system safety monitoring

Rev. 1.3 — 16 December 2025 **Product data sheet**



1 Overview

The PF09 is a power management integrated circuit (PMIC) optimized for high performance i.MX9x based applications. It Integrates multiple high-efficiency switch mode and linear voltage regulators to support base system power from a pre-regulated system rail (3.3 V to 5.0 V). It provides low quiescent current in STANDBY (STBY) and low-power Off modes. Built-in multiple time programmable configuration stores key startup configurations, drastically reducing the number of external components typically used to set the output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C communication after startup, offering flexibility for different system states.

The PF09 is developed in compliance with the ISO 26262 standard, including safety features, with Fail-safe outputs and integrated self-test mechanisms, becoming part of a safety-oriented system partitioning targeting high-integrity safety levels up to ASIL D, and complying with the IEC61508 industrial safety specification targeting high safety integrity levels up to SIL 2.

2 Features and benefits

- Up to five buck regulators with internal power stage and programable current limits
- Three low-dropout linear regulators with load switch operation
- Ultra-low power always-on LDO supply
- Two external voltage monitoring inputs
- Programmable I/O interfacing pins
- Advanced frequency management with frequency spread spectrum
- Multi-channel analog multiplexer for system voltage monitoring
- High speed I^2C interface with up to 3.4 MHz operation
- Advanced thermal monitoring and thermal shutdown protection
- Functional safety architecture to target up to ASIL D automotive applications
- Functional safety architecture to target up to SIL 2 industrial applications
- Multiple-time programmable configuration (MTP)
- 56-pin QFN Package with exposed pad
- Automotive qualified by AEC-Q100 rev J up to Grade 1

3 Applications

- Automotive infotainment
- High-end consumer and industrial
- Connectivity domain controller
- Telematics

4 Simplified application diagram

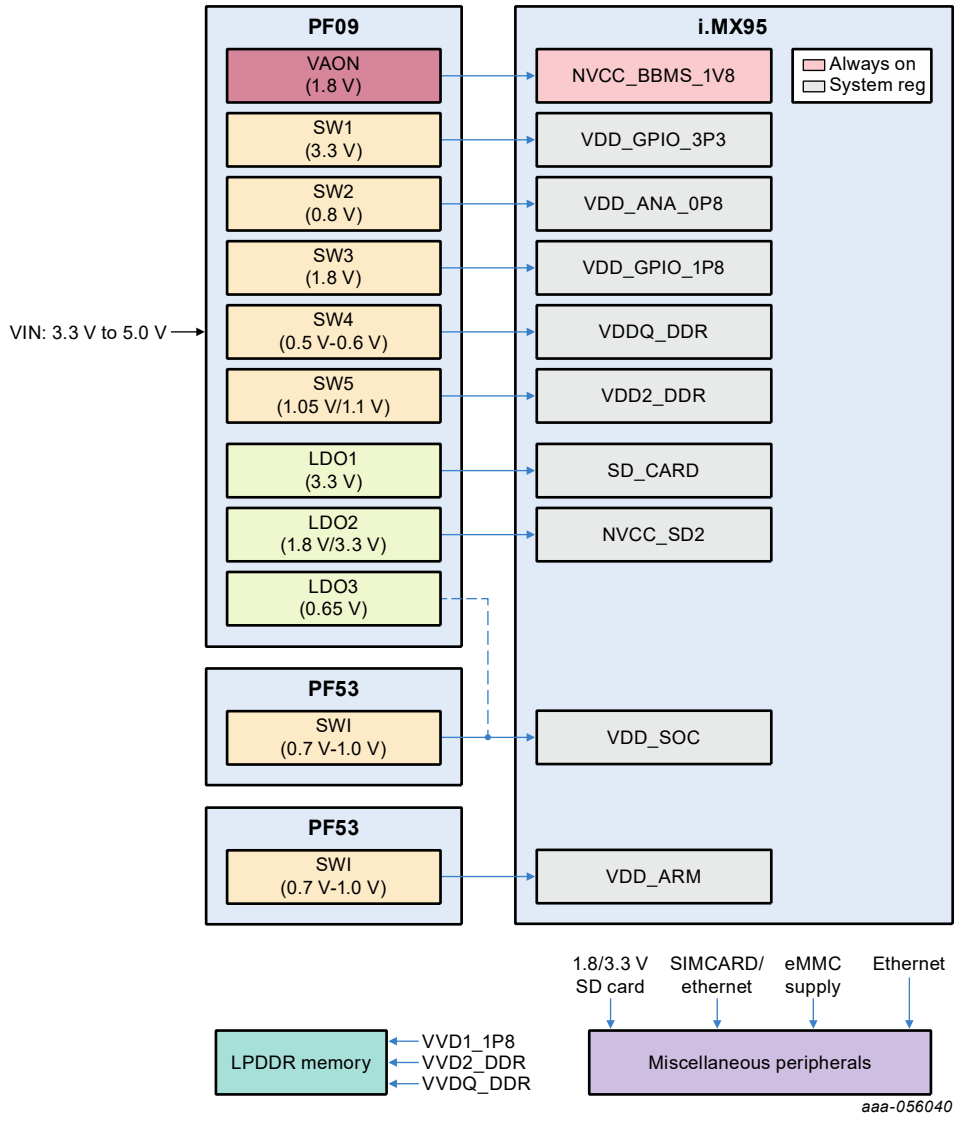


Figure 1. Simplified application diagram i.MX95

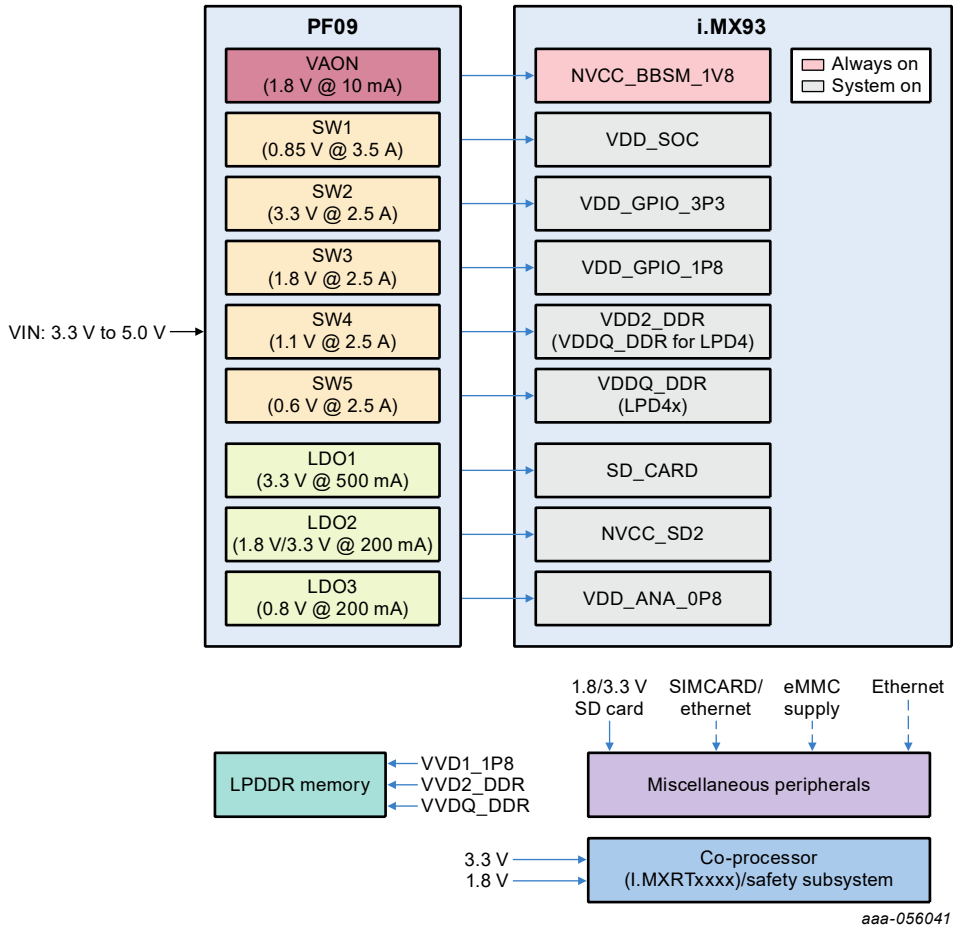


Figure 2. Simplified application diagram i.MX93

5 Ordering information

Table 1. Ordering information

Type number [1]	Package		
	Name	Description	Version
PF0900	HVQFN56	HVQFN56, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 56 terminals, 0.5 mm pitch, 8 mm x 8 mm x 0.53 mm body	SOT684-32(DD)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

Table 2. Ordering options

Part number [1][2]	Target market	NXP processor	System comments	Safety grade	OTP ID
MPF0900AMDA0ES	Automotive	N/A	Not programmed	ASIL D	DA0
MPF0900AMBA0ES	Automotive	N/A	Not programmed	ASIL B	BA0
MPF0900AMMA0ES	Automotive	N/A	Not programmed	QM	MA0
MPF0900AMBA1ES	Automotive	i.MX 95	LPDDR5 memory	ASIL B	BA1
MPF0900AMBA2ES	Automotive	i.MX 95	LPDDR4X memory	ASIL B	BA2
MPF0900AMMA1ES	Automotive	i.MX 95	LPDDR5 memory	QM	MA1
MPF0900AMMA2ES	Automotive	i.MX 95	LPDDR4X memory	QM	MA2
MPF0900AMMA5ES	Automotive	i.MX 93	LPDDR4X memory	QM	MA5
MPF0900AVNA0ES	Industrial	N/A	Not programmed	QM	NA0
MPF0900AVSA0ES	Industrial	N/A	Not programmed	SIL 2	SA0
MPF0900AVNA1ES	Industrial	i.MX 95	LPDDR5 memory	QM	NA1
MPF0900AVNA2ES	Industrial	i.MX 95	LPDDR4X memory	QM	NA2
MPF0900AVNA5ES	Industrial	i.MX 93	LPDDR4X memory	QM	NA5
MPF0900AVSA1ES	Industrial	i.MX 95	LPDDR5 memory	SIL 2	SA1
MPF0900AVSA2ES	Industrial	i.MX 95	LPDDR4X memory	SIL 2	SA2
PPF0900AMBA7ES	Automotive	i.MX943 Auto	LPDDR5	ASIL B	BA7
PPF0900AMBA8ES	Automotive	i.MX943 Auto	LPDDR4	ASIL B	BA8
PPF0900AMMA7ES	Automotive	i.MX943 Auto	LPDDR5	QM	MA7
PPF0900AMMA8ES	Automotive	i.MX943 Auto	LPDDR4	QM	MA8

[1] P = Engineering sample part number (PPF09x)
[2] M = Production part number (MPF09x)

6 Device versioning

The PF09 is a family of devices aiming to provide versatile and scalable power management to various types of automotive and industrial systems and platforms. Here is an example showing decoding of the PF09 part number nomenclature:

PPF09**00**AM**D**A0ES

At the first level, the PF09 family features various device members with a scalable number of channels with pin-to-pin and software compatibility, to improve system cost optimization. Hardware scalability is identified by the last two digits of the device core number, for example, PF09**XX**.

At the second level, each device allows functional safety scalability to meet the needs of automotive applications ranging from QM up to ASIL D, as well as industrial applications targeting a safety integrity level up to SIL 2.

Automotive QM = **M**

Automotive ASIL B = **B**

Automotive ASIL D = **D**

Industrial SIL 2 = **S**

Table 3 below provides the functional safety feature partitioning for all standard safety grades.

Table 3. Device versioning strategy

Safety Functions [1] [2]	QM	ASIL B	ASIL D	SIL 2
External VMON1	N/A	Available[3]	Available[3]	Available[3]
External VMON2	N/A	Available[3]	Available[3]	Available[3]
FCCU interface	N/A	Available	Available	Available
ERRMON Interface	N/A	N/A	Available	Available
VIN_OV monitor	Available	Available	Available	Available
Watchdog manager	Static watchdog	Static watchdog	Dynamic watchdog	Static watchdog
FS0B operating mode	Fault mode	Active safe state	Active safe state	Active safe state
Self-test routine	N/A	Enabled	Enabled	Enabled
ABIST on demand	N/A	N/A	Available	Available
LBIST routine	N/A	N/A	Power-up / on- demand	Power-up / on- demand
Dynamic cyclic redundancy check (CRC)	N/A	N/A	Enabled	Enabled
Bandgap monitor	Interrupt only	Interrupt / shutdown	Interrupt / shutdown	Interrupt / shutdown
VDIG overvoltage (OV)	Interrupt only	Interrupt / shutdown	Interrupt / shutdown	Interrupt / shutdown
DMS safety handshake	N/A	N/A	Enabled	Enabled

[1] Available features can be enabled or disabled in OTP. Please refer to the specific OTP configuration report for specific information.
[2] Enabled features are enabled all the time to provide real-time protection.
[3] May not be available in some part numbers with a reduced feature set.

Note that the first and second levels of customization are done at the fab, therefore, features marked as N/A in a specific device means they are not physically present on the device. To get the desired functionality, it may

be required to move up to a different tier or generate a custom request to create a new device customization if possible.

Finally, at the third level, all members of the PF09 family are provided with one-time programmable (OTP) registers to set the default hardware configuration and behaviors of the device at power-up. OTP configuration bits are discussed throughout this document in order to provide visibility of the possible configuration that can be achieve within the context of the functional behaviors of each configuration. However, OTP configuration is only possible during the part number customization stage (OTP ID generation) and cannot be modified during system operation.

OTP emulation and programming performed by the customer is allowed during engineering development using NXP's latest graphical user interface and socketed evaluation board.

The customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

Contact your NXP representative for more detailed information on how to request a custom configuration or in-house programming procedure to generate custom parts suitable to your specific system needs.

7 Functional block diagram

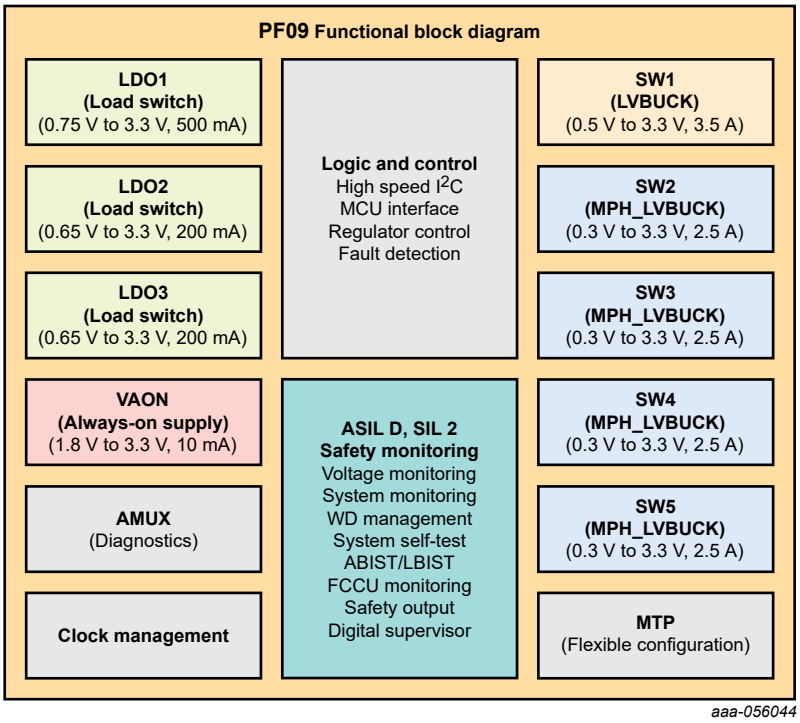


Figure 3. Functional block diagram

8 Internal block diagram

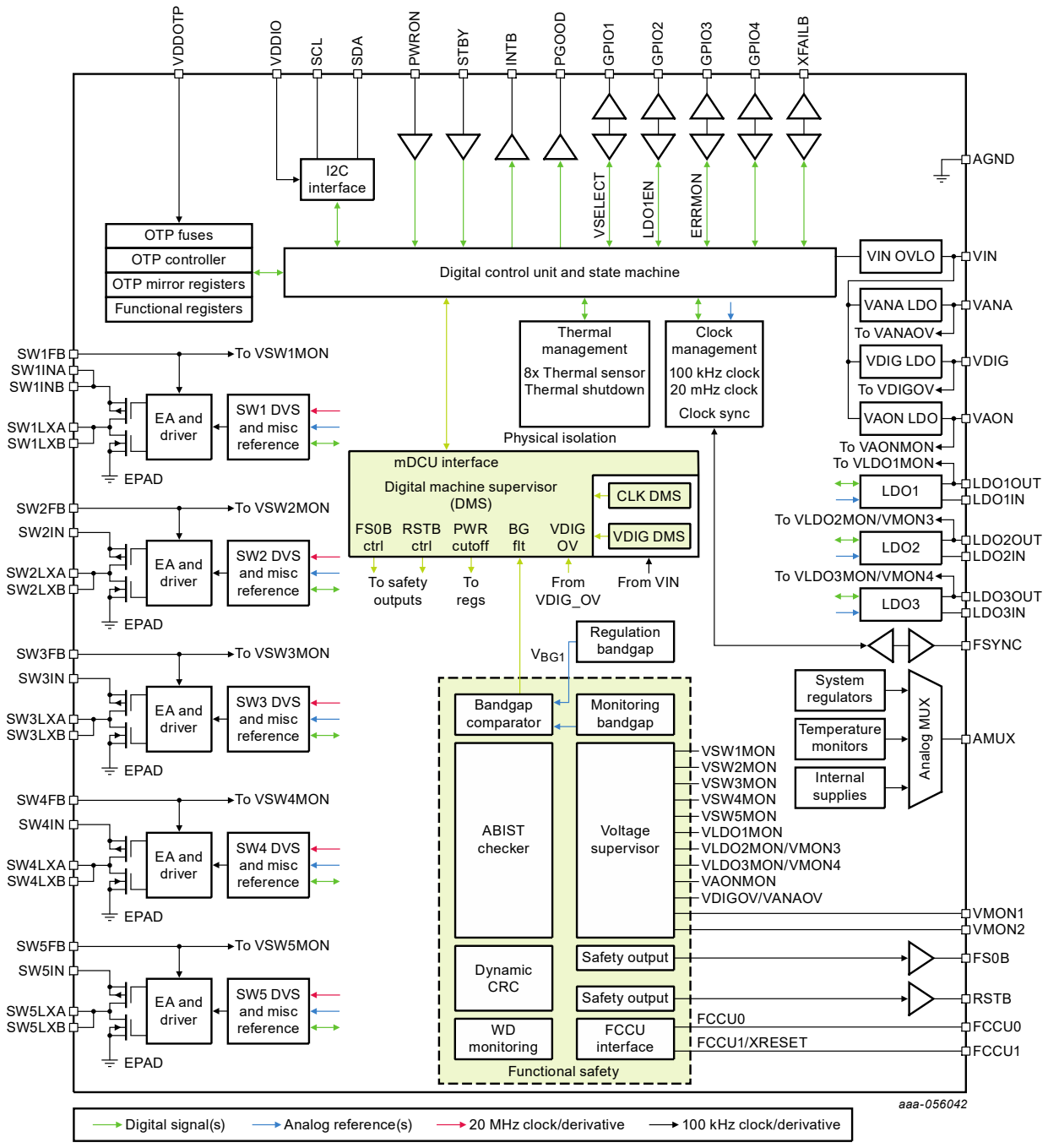


Figure 4. Internal Block Diagram

9 Pinning information

9.1 Pinning

The PF09 is offered in a 56-pin, 8 x 8 mm^2 body size QFN with exposed pad and wettable flanks.

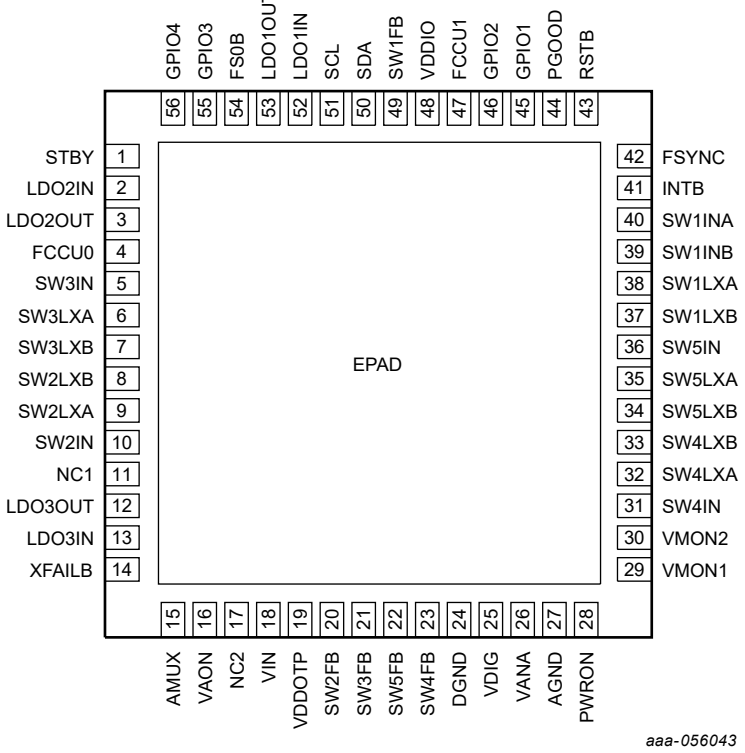


Figure 5. PF09 package pinout (top view)

9.2 Pin description

Table 4. QFN56 Pin description

Pin	Pin name	Description	Min	Max	Units
1	STBY	STANDBY request	-0.3	6.0	V
2	LDO2IN	LDO2 input	-0.3	6.0	V
3	LDO2OUT	LDO2 output	-0.3	6.0	V
4	FCCU0	FCCU fault monitoring input 0	-0.3	6.0	V
5	SW3IN	SW3 Input	-0.3	6.0	V
6	SW3LXA	SW3 switching node A	-0.3	6.0	V
7	SW3LXB	SW3 switching node B	-0.3	6.0	V
8	SW2LXB	SW2 switching node B	-0.3	6.0	V
9	SW2LXA	SW2 switching node A	-0.3	6.0	V
10	SW2IN	SW2 input	-0.3	6.0	V

Table 4. QFN56 Pin description*...continued*

Pin	Pin name	Description	Min	Max	Units
11	NC1	Not connected	-0.3	6.0	V
12	LDO3OUT	LDO3 output	-0.3	6.0	V
13	LDO3IN	LDO3 input	-0.3	6.0	V
14	XFAILB	External fail	-0.3	6.0	V
15	AMUX	Analog multiplexer output	-0.3	6.0	V
16	VAON	Always-on output	-0.3	6.0	V
17	NC2	Not connected	-0.3	6.0	V
18	VIN	PMIC input supply	-0.3	6.0	V
19	VDDOTP	OTP supply	-0.3	10.0	V
20	SW2FB	SW2 feedback	-0.3	6.0	V
21	SW3FB	SW3 feedback	-0.3	6.0	V
22	SW5FB	SW5 feedback	-0.3	6.0	V
23	SW4FB	SW4 feedback	-0.3	6.0	V
24	DGND	Digital ground	-0.3	0.3	V
25	VDIG	Internal digital supply	-0.3	2.0	V
26	VANA	Internal analog supply	-0.3	2.0	V
27	AGND	Analog ground	-0.3	0.3	V
28	PWRON	Power on request	-0.3	6.0	V
29	VMON1	External VMON1	-0.3	6.0	V
30	VMON2	External VMON2	-0.3	6.0	V
31	SW4IN	SW4 Input	-0.3	6.0	V
32	SW4LXA	SW4 switching node A	-0.3	6.0	V
33	SW4LXB	SW4 switching node B	-0.3	6.0	V
34	SW5LXB	SW5 switching node B	-0.3	6.0	V
35	SW5LXA	SW5 switching node A	-0.3	6.0	V
36	SW5IN	SW5 input	-0.3	6.0	V
37	SW1LXB	SW1 switching node B	-0.3	6.0	V
38	SW1LXA	SW1 switching node A	-0.3	6.0	V
39	SW1INB	SW1 input B	-0.3	6.0	V
40	SW1INA	SW1 input A	-0.3	6.0	V
41	INTB	Interrupt request	-0.3	6.0	V
42	FSYNC	Clock sync input	-0.3	6.0	V
43	RSTB	MCU reset pin	-0.3	6.0	V
44	PGOOD	Power good	-0.3	6.0	V
45	GPIO1	Programmable IO1	-0.3	6.0	V
46	GPIO2	Programmable IO2	-0.3	6.0	V

Table 4. QFN56 Pin description*...continued*

Pin	Pin name	Description	Min	Max	Units
47	FCCU1	XRESET / FCCU fault monitoring input 1	-0.3	6.0	V
48	VDDIO	I/O supply input	-0.3	6.0	V
49	SW1FB	SW1 feedback	-0.3	6.0	V
50	SDA	I2C data	-0.3	6.0	V
51	SCL	I2C clock	-0.3	6.0	V
52	LDO1IN	LDO1 input	-0.3	6.0	V
53	LDO1OUT	LDO1 output	-0.3	6.0	V
54	FS0B	Fail-safe output	-0.3	6.0	V
55	GPIO3	Programmable IO3	-0.3	6.0	V
56	GPIO4	Programmable IO4	-0.3	6.0	V
57	EPAD	Exposed pad ground	-0.3	0.3	V

10 General product description

10.1 Features

- Up To five buck regulators with internal power stage
  - SW1 single-phase operation, 0.5 V to 3.3 V @ 3.5 A with up to 1.5 % DC accuracy
  - SW2 multi-phase operation, 0.3 V to 3.3 V @ 2.5 A with up to 1.5 % DC accuracy
  - SW3 multi-phase operation, 0.3 V to 3.3 V @ 2.5 A with up to 1.5 % DC accuracy
  - SW4 multi-phase operation, 0.3 V to 3.3 V @ 2.5 A with up to 1.5 % DC accuracy
  - SW5 multi-phase operation, 0.3 V to 3.3 V @ 2.5 A with up to 1.5 % DC accuracy
  - Programmable current limit
- Three low-dropout linear regulators.
  - LDO1: LDO/load switch with output voltage from 0.75 V to 3.3 V @ 500 mA.
  - LDO2 and LDO3: low-power LDO/load switch with output voltage from 0.65 V to 3.3 V @ 200 mA
- Ultra-low power always-on LDO supply
  - Configurable output voltage: 1.8 V, 3.0 V or 3.3 V with up to 2 % DC accuracy
- Two external voltage monitoring inputs
  - Dynamic monitoring voltage selection
  - Selectable monitoring threshold with up to 1% monitoring accuracy
- Programmable I/O interface
- Advanced frequency management with frequency spread spectrum
- Multi-channel analog multiplexer for system voltage monitoring
- High-speed I^2C interface with up to 3.4 MHz operation
- Advanced thermal monitoring and thermal shutdown protection
- Functional safety architecture to target up to ASIL D automotive applications
- Functional safety architecture to target up to SIL 2 industrial applications
- Multiple-time programmable (MTP) configuration
- 56-pin QFN package with exposed pad
- Automotive qualified by AEC-Q100 rev J up to Grade 1

10.2 Power tree summary

Table 5. PF09 voltage regulator summary.

Regulator	Type	Input Supply	Output Range	Rated Current
SW1	Single-phase buck regulator	3.3 V to 5.5 V[1]	0.5 V to 3.3 V	3.5 A DC current
SW2	Multi-phase buck regulator	3.3 V to 5.5 V[1]	0.3 V to 3.3 V	2.5 A DC current
SW3	Multi-phase buck regulator	3.3 V to 5.5 V[1]	0.3 V to 3.3 V	2.5 A DC current
SW4	Multi-phase buck regulator	3.3 V to 5.5 V[1]	0.3 V to 3.3 V	2.5 A DC current
SW5	Multi-phase buck regulator	3.3 V to 5.5 V[1]	0.3 V to 3.3 V	2.5 A DC current
LDO1	LDO with load switch	1.8 V to 5.5 V	0.75 V to 3.3 V	500 mA
LDO2	LDO with load switch	1.8 V to 5.5 V	0.65 V to 3.3 V	200 mA
LDO3	LDO with load switch	1.8 V to 5.5 V	0.65 V to 3.3 V	200 mA
VAON	Always-on low-power LDO	2.7 V to 5.5 V	1.8 V, 3.0 V, 3.3 V	10 mA

[1] Input supply for switching regulators must be capable to sink current to avoid overvoltage condition during the power-down sequence of the device.

10.3 Device identification

The DEV_ID[4:0] bits are provided to identify the core ID for each member of the PF09 family.

Table 6. DEVICE_ID bit field

DEV_ID[4:0]	Device
00000	PF0900
00001	PF0901
00010	PF0902
….	….
11111	PF0931

The FS_ID[2:0] bits are provided to identify the functional safety target level of a specific part number within the PF09 family.

Table 7. FS_ID bit field

FS_ID[2:0]	Device
000	QM
001	ASIL B
010	ASIL D
011	SIL 2
100	Reserved
101	Reserved
110	Reserved
111	Reserved

The functional safety target level is assigned based on the safety functions available on a specific part number and the corresponding FMEDA analysis, assuming such functions are utilized as recommended in the product safety manual.

It is responsibility of the system designer to evaluate custom OTP configurations which are using a subset of the safety mechanism provided on the corresponding device.

The DEVICE_FAM[7:0] bits is provided to identify the family code for the PF09.

Table 8. DEVICE_FAM bit field

DEVICE_FAM[7:0]	Device family
0x09	PF09

The OTP program ID registers are provided to track and identify the OTP configuration of standard and custom-programmed devices provide by NXP.

The PROG_IDH[4:0] bits provide the hexadecimal coding of the first OTP ID character (A - Z).

Table 9. PROG_IDH bit field

PROG_IDH[4:0]	OTP ID First Letter
00000	A
00001	B

Table 9. PROG_IDH bit field*...continued*

PROG_IDH[4:0]	OTP ID First Letter
00010	C
00011	D
00100	E
00101	F
00110	G
00111	H
01000	J
01001	K
01010	L
01011	M
01100	N
01101	P
01110	Q
01111	R
10000	S
10001	T
10010	U
10011	V
10100	W
10101	X
10110	Y
10111	Z
11000 - 11111	NOT ASSIGNED

The PROG_IDL[5:0] bits provide the hexadecimal coding of the second OTP ID character (1 - 9 and A – Z).

Table 10. PROG_IDL bit field

PROG_IDL[4:0]	OTP ID second letter
000000	0
000001	1
000010	2
000011	3
000100	4
000101	5
000110	6
000111	7
001000	8
001001	9

Table 10. PROG_IDL bit field*...continued*

PROG_IDL[4:0]	OTP ID second letter
001010	A
001011	B
001100	C
001101	D
001110	E
001111	F
010000	G
010001	H
010010	J
010011	K
010100	L
010101	M
010110	N
010111	P
011000	Q
011001	R
011010	S
011011	T
011100	U
011101	V
011110	W
011111	X
100000	Y
100001	Z
100010	NOT ASSIGNED
100011	NOT ASSIGNED
….	….
111111	NOT ASSIGNED

The OTP_VIN_SEL bit is provided to select the intended input voltage in the system.

Table 11. OTP_VIN_SEL bit

OTP_VIN_SEL	Input voltage selection
0	5.0 V
1	3.3 V

Selecting the right input voltage for the specific system allows for optimization of the power generation stage when system input voltage is 3.3 V. For input voltages larger than 3.3 V, the OTP_VIN_SEL bit must be set to 5.0 V to improve system robustness.

11 Functional state machine description

11.1 Functional state machine

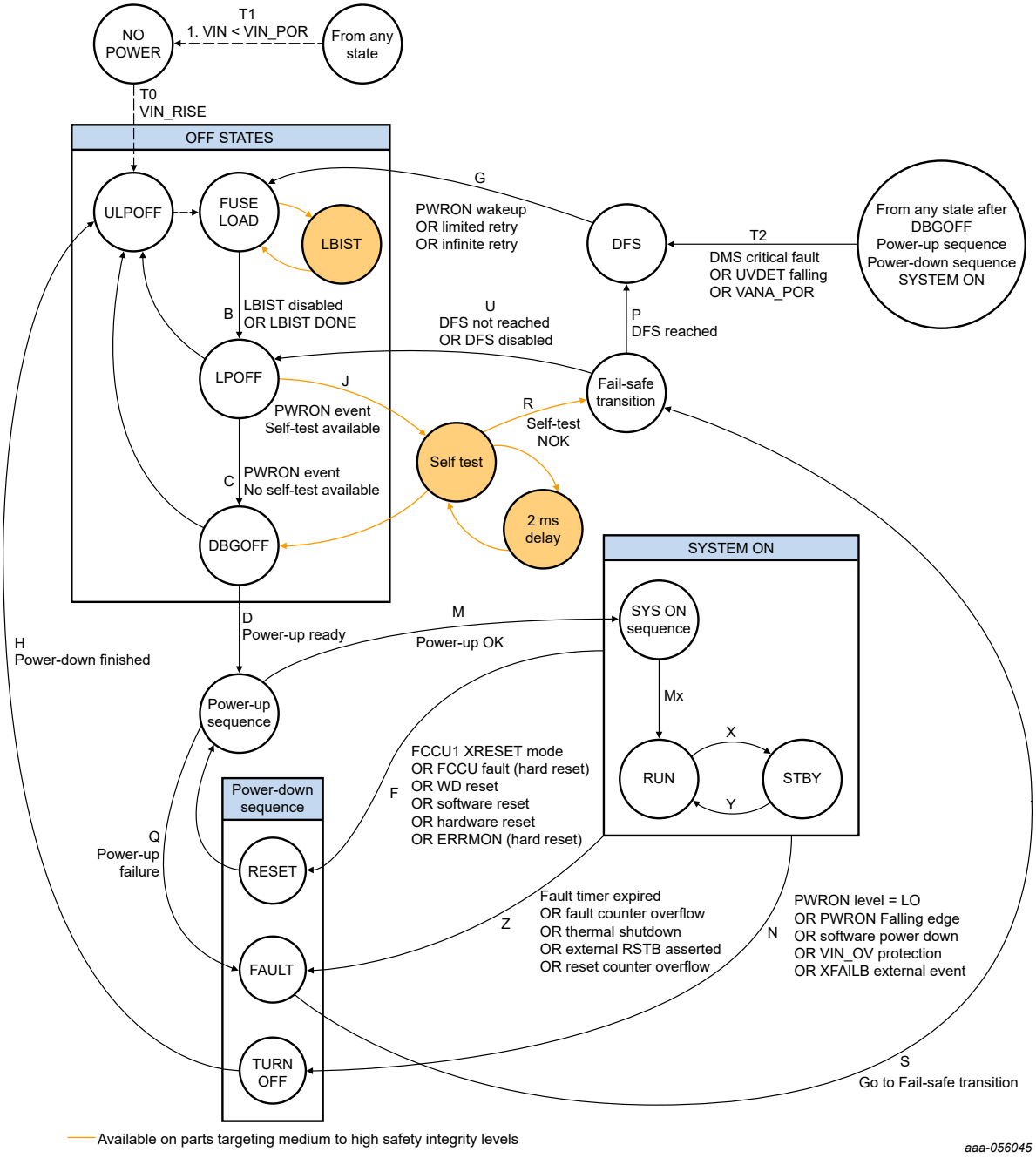


Figure 6. PF09 Functional state machine

11.2 State descriptions

11.2.1 VIN cold boot initialization

When the VIN is applied for the first time (VIN crossing the $V_{IN\_POR\_RISE}$ threshold), the PF09 will automatically perform an initialization sequence prior to evaluating a power-up event. If no power-on event is present after the initialization sequence, the device will move to the corresponding low-power state based on the mode of operation of the PWRON pin set in the OTP registers.

If the VAON is configured as an always-on supply, the VAON regulator will be enabled as part of the initialization sequence to ensure the supply is up in regulation by the time the system is ready to request a power-up event.

In devices targeting a high safety integrity level (ASIL/SIL) where the LBIST routine is available, the logic self-test routine is performed as part of the fuse loading routine to ensure the logic gates controlling the functional safety mechanism are healthy at power up.

In devices targeting a quality management (QM) safety integrity level or low safety integrity levels where the LBIST routine is not be available, the logic controller will proceed to the LPOFF state right after the fuse loading routine is finished.

During the fuse loading, the OTP registers implement a CRC verification to ensure there are no flip bits at power-up. If an OTP loading error is detected, the corresponding fault flag (_NOK - Register Address Flags: 0x2D) is asserted high and the system will not be allowed to proceed to normal operation to prevent unsafe operation.

When the state machine enters the LPOFF state, the device will be ready to evaluate the power-on event to proceed with the power-up sequence.

Table 12. VIN_POR thresholds

Symbol	Description	Min	Typ	Max	Unit
$V_{IN\_POR\_RISE}$	VIN power-on reset threshold (rising)	2.7	2.8	2.9	V
$V_{IN\_POR\_FALL}$	VIN power-on reset threshold (falling)	2.5	2.6	2.7	V

11.2.2 ULPOFF state

The ULPOFF (Ultra-low power off) state is provided to allow the PMIC to remain in an OFF condition with minimum functional operation, minimum quiescent current and the ability to wake up if the PWRON pin is asserted high.

If the VAON is set as an always-on regulator, the configuration of the VAON regulator is maintained during the ULPOFF state as long as the VIN does not fall below the $V_{IN\_POR\_FALL}$ threshold.

When the device successfully disables the internal VDIG supply in the ULPOFF state, it is expected that all notification flags will be lost and reset to the default state once a wake-up event is present.

11.2.3 LPOFF state

During the LPOFF (Low-power off) state, only the VAON regulator can be enabled if it is configured as an always-on supply via the OTP configuration. All other system regulators will remain disabled until the power-up sequence is started.

In the LPOFF state, the PF09 is able to evaluate a power-on event on the PWRON pin, based on the configuration selected by the OTP_PWRON_MODE bit.

In a system using the PWRON pin in *level sensitive* mode, the LPOFF state becomes a transitory state upon a wake-up event detected in the ULPOFF state. This allows the system to take advantage of the lowest quiescent current in the ULPOFF state when the device is intended to remain in the OFF condition.

In systems requiring to operate the PWRON pin in *edge sensitive* mode, the LPOFF state becomes the static low-power state for the system, since the PWRON pin is expected to be pulled up to VIN externally. In this scenario, the device will automatically detect a wake-up event upon entering the ULPOFF state, and proceed to perform the fuse load routine and move into the LPOFF state to wait for a Falling edge on the PWRON pin to generate a valid power-on event.

11.2.4 DBGOFF state

During normal system operation, the DBGOFF (debug off) state will be a transitory state between a power-on event and the power-up sequence. It serves as the gating state to ensure the PMIC is ready to start a power-up sequence, and allow synchronization of two or more PMICs providing full power architecture to a complex system.

If the VDDIO supply is provided externally, the device is able to communicate through the I^2C bus during the DBGOFF state, allowing the PMIC to operate in development/debugging modes. In such scenarios, the DBGOFF state becomes a full-biased OFF state, to allow full access to the functional and OTP registers to enable OTP emulation and/or OTP fuse programming. Contact your NXP representative for detailed instructions on OTP emulation and fuse programming.

If the VAON is set as an always-on Regulator, the VAON supply is monitored for OV/UV conditions to ensure the supply is in regulation before allowing the power-up sequence to start.

If the XFAILB synchronization function is available, the device will use the DBGOFF state as the synchronization point to start the power-up sequence. The PF09 will release the XFAILB pin internally when it is ready to start the Power-up sequence, based on the following conditions:

- Self-test has finished (if self-test is available in the device)
- && The LBIST_STATUS[1:0] is different from 0b10 (if LBIST is available in the device)
- && the fuse loading (_NOK - Register Address Flags: 0x2D) flags are not asserted
- && V_{AON} has reached regulation (if VAON set as always-on regulator)
- && VIN < VIN_OV (if the VIN_OV monitor is enabled)
- && T_J is at least 10 °C below the TSD threshold
- && VDDOTP < 3.0 V

If any of the conditions mentioned above are not met, the XFAILB will remain asserted and the device will remain in the DBGOFF state until all conditions are met. Once the XFAILB pin has been internally released, the device will monitor the XFAILB pin to pause the power-up sequence until the pin has been released HIGH by all devices connected to it.

If the XFAILB synchronization function is not available, the XFAILB status is no longer a condition to proceed with the power-up sequence and the following conditions must be met to allow the power-up sequence to be started:

- Self-test has finished (if self-test is available in the device)
- && The LBIST_STATUS[1:0] is different from 0b10 (if LBIST is available in the device)
- && the fuse loading (_NOK - Register Address Flags: 0x2D) flags are not asserted
- && V_{AON} has reached regulation (if VAON set as an always-on regulator)
- && VIN < VIN_OV (if VIN_OV monitor is enabled)
- && T_J is at least 10 °C below the TSD threshold
- && VDDOTP < 3.0 V

In the event the device is stuck in the DBGOFF state, a power-off event in the PWRON pin will send the device to the corresponding OFF state and wait for a new power-up event to attempt the power-up sequence again.

11.2.5 Self-test routine

In devices with a high safety integrity level (ASIL/SIL) the self-test routine is performed when the state machine transitions out of the LPOFF state. During the self-test, the PF09 performs a startup self-check routine to verify the integrity of the system:

The high speed oscillator circuit is operating within a maximum of 6 % tolerance.

The outputs of both the voltage generation bandgap and the monitoring bandgap are not drifting apart from each other.

A CRC is performed on the mirror registers during the self-test routine, to ensure the integrity of the OTP registers before powering up.

Analog built-in test on all voltage monitors and Safety I/Os is performed. (Refer to section Section 14.8 for details on ABIST implementation.)

To allow for varying settling times for the internal bandgap and oscillators, the self-test routine is executed up to three times (with 2 ms between each test) if a failure is encountered. If all three checks result in a failure, the state machine will proceed to the Fail-safe transition to prevent operation with a potential latent fault present.

A failure in the ABIST test is not interpreted as a self-test failure, and it will only set the corresponding ABIST flag in order to prevent the system from exiting a safe state after power-up.

11.2.6 Power-up sequence

The PF09 provides a highly configurable power-up sequence to enable the system regulators and general purpose IO pins in a specific order and timing during the power-up state.

The default configuration for the power-up sequence is loaded from the OTP registers to ensure the system always turns on with the correct configuration every power-up cycle as defined on each specific part number.

The RSTB pin is also programmable as part of the power-up sequence, and it is used as the condition to enter the SYSTEM ON states.

Voltage monitoring functions are provided during the power-up sequence to ensure the system is brought out of reset only if all voltage regulators enabled before the RSTB pin have reached regulation and are operating properly.

The RSTB may be released in the middle of the Power-up sequence. In this case, the remaining supplies in the power-up still continue to ramp up while the state machine enters the system-on states to process fault conditions actively.

Refer to section Section 12.3.3 for details.

11.2.7 RUN State

If the power-up sequence is completed successfully, the state machine transitions directly into the RUN state. The RUN State is a full-featured state providing full functionality and monitoring as described in this document.

All safety-related monitoring is fully operational during the RUN State if the corresponding feature is enabled via OTP or functional registers.

Upon entering the RUN State, the I^2C functional registers are loaded with the default values set by the OTP registers, or with the default configuration. The MCU is expected to perform a booting sequence to modify the PMIC functional configuration as required by the application.

All registers to control the regulators' output voltage, operating modes, interrupt masks and other miscellaneous functions can be written to or read from the functional I^2C register map during the SYSTEM ON states once the power-up sequence is finalized.

11.2.8 STANDBY state

The STANDBY state is a secondary functional state with programmable functionality to prioritize either system monitoring or low-power operation.

After the device enters the RUN state, the MCU is able to request to enter the STANDBY state by asserting the STBY pin with the correct polarity as defined by the STBY_POL bit. Refer to section Section 12.8.3 for a detailed description of the STBY pin operation.

The default configuration of the STBY registers is loaded from the OTP registers upon starting the power-up sequence. All functional I^2C registers are accessible to read and write during the STANDBY state, as long as the proper VDDIO is supplied.

The OTP_LP_STBY bit is provided to select whether the device enters the STANDBY state in a low-power mode or monitored mode.

Table 13. OTP_LP_STBY bit

OTP_LP_STBY	Low-power STANDBY
0	Monitored STANDBY
1	Low-power STANDBY

When the PF09 is operating in monitored STANDBY mode, the device operates based on the configuration in the STANDBY registers, with most monitoring functions available.

When the PF09 is operating in the low-power STANDBY mode, the device functionality is limited, to achieve low quiescent currents.

Table 14. STANDBY operation summary

Function	Monitored STANDBY	Low-power STANDBY
High-frequency clock	Always on	Enabled on demand (during I^2C communication)
Switching regulators mode	OFF, PWM or PFM	OFF or PFM
FS0B pin status (In Active safe state)	Always asserted (safe state)	Always asserted (safe state)
Internal voltage monitors	Enabled with voltage regulator	Disabled
External voltage monitors	Enabled (if VMONx_EN = 1)	Disabled
WD timer	Enabled (if WD_EN = 1)	Disabled
FCCU monitoring	Enabled [1][2]	Disabled
ERRMON monitoring	Enabled[1]	Disabled
Clock monitoring	Enabled	Disabled
Dynamic CRC	Enabled[1]	Disabled
The digital machine supervisor	Disabled	Disabled
The bandgap monitor	Enabled	Disabled
Thermal monitor	Enabled	Disabled
AMUX block	Available	Disabled

[1] If block is available in the device and/or OTP configuration.
[2] FCCU monitoring allowed with limited functionality in the safe state.

The selection of the STANDBY mode is done during the OTP device customization stage, and will remain fixed in the customized part number.

When the device transitions from the RUN to the STANDBY state, the system will trigger a PWRDN_I interrupt. The PWRDN_I event will assert the INTB pin only if the PWRDN_M = 0 (interrupt un-masked). By default, the PWRDN_M bit is masked upon power up.

11.2.9 Power-down sequence

Three types of events may lead to the power-down sequence.

- Non-faulty or requested turn-off event
- Turn-off events due to a PMIC fault
- Reset event

During the power-down sequence, the system regulators are disabled as described in the power-down sequencing section.

11.2.9.1 TURNOFF state

Non-faulty turn-off events move directly into the corresponding low-power state as soon as the power-down sequence is finalized.

If the VAON is set to operate as an always-on regulator, the VAON output will remain enabled during the turn-off event and into the low-power modes. If the VAON is set as a system regulator, the VAON regulator will be disabled as defined in the power-down sequence.

All other system regulators will be disabled as defined in the power-down sequence.

11.2.9.2 FAULT state

Turn-off events due to a PMIC fault will move into the Fail-safe transition as soon as the power down sequence is finalized.

If the VAON is set as an always-on regulator, the VAON output will remain enabled during a fault event transitioning through the Fail-safe transition. If the VAON is set as a system regulator, the VAON output will be disabled as defined in the power-down sequence.

All other system regulators are disabled as defined in the power-down sequence.

11.2.9.3 RESET state

A RESET state is provided to allow the system to refresh the configuration without looping through a full power cycle.

During a reset event, the system can decide whether the VAON supply remains enabled, to maintain the always-on domain or turn off to generate a full system reset condition.

When a reset event has occurred, the device turns off the system regulators as defined by the power-down sequence, and it will power back up without the need of a new power-on event.

11.2.10 Fail-safe transition

During the Fail-safe transition, the VAON remains enabled if it is configured as an always-on regulator. All system regulators will remain disabled until the next power-up sequence.

The state machine provides a Fail-safe counter (FS_CNT[3:0]) to prevent a non-recoverable cyclic failure from happening.

When the state machine enters the fail-safe transition, the FS_CNT[3:0] is compared and increased; if FS_CNT[3:0] reaches the maximum count, the device will move directly to the Deep Fail-safe state and wait for a valid condition to exit the state.

11.2.11 Deep Fail-safe (DFS) state

The DFS state is intended to work as a temporary lockdown state upon a cyclic critical failure condition. Because the system may land in the DFS state and remain there indefinitely, the DFS state is designed to consume as little current as possible, with just the minimum blocks enabled to perform the operations defined in this state.

The maximum number of times the device can pass through the Fail-safe transition continuously prior to moving into the DFS state is programmed using the OTP_MAX_FS_CNT[3:0] bits.

When OTP_MAX_FS_CNT[3:0] = 0x00, the DFS state will be disabled and the FSM will not be able to enter this state by means of the fault counting mechanism, however more critical failures such as the temporary loss of VIN or VANA, or other safety-critical failures, may still result in the transition to the DFS state to ensure the system operates only under controlled safe conditions.

When the OTP_MAX_FS_CNT[3:0] != 0x00 and the FS_CNT [3:0] = OTP_MAX_FS_CNT [3:0], the device will enter the DFS state.

FS_CNT[3:0] can be cleared manually during the SYSTEM ON states, or by a number of good watchdog refreshes when WD_OK_FDC[2:0] != 0x00.

In this state, the PGOOD and RSTB pins remain asserted low all the time.

In devices targeting high safety integrity levels where the FS0B is operating in Active Safe-state mode, the FS0B pin will remain asserted low during the DFS state.

For QM or devices targeting low safety integrity levels where the FS0B is operating in Fault status mode, the FS0B will be asserted if the FS0B_DFS = 1, or another fault caused it to assert previously.

During DFS state, the VAON regulator will be disabled regardless of the operating mode, as well as all other system regulators to prevent further damage to the system.

The PF09 provides various mechanisms to exit the DFS state, either requested externally via the PWRON pin or generated automatically by the auto retry timer. One or more mechanisms to exit the DFS state are selectable via the OTP registers during the device customization stage.

The OTP_PWRON_DFS bit is provided to allow the device to wake up from the DFS state via the PWRON pin.

Table 15. OTP_PWRON_DFS bit

OTP_PWRON_DFS	Description
0	PWRON is not able to exit DFS
1	PWRON able to exit DFS

The OTP_RETRY_DFS bit is provided to allow the device to wake up from the DFS state via the auto retry timer.

Table 16. OTP_RETRY_DFS bit

OTP_RETRY_DFS	Description
0	Auto retry Disabled
1	Auto retry Enabled

When PF09 is configured to exit DFS via the PWRON pin, a LOW to HIGH transition on the PWRON pin will force the device out of the DFS state. If the PWRON pin was high when entering the DFS state, it must go low first and be toggled HIGH again in order to recognize a valid exit from DFS.

When PF09 is configured to exit the DFS state via the auto-retry timer, the device will remain in the DFS state until the retry timer (TRETRY) is expired. When the retry timer reaches it maximum value, the device will increase the eight-bit RETRY_CNT[7:0] by one and proceed to attempt a power-up event.

When auto retry is enabled, the retry timer is increased exponentially every 15 counts. The retry timer is calculated as follows: TRETRY = TBASE_RETRY * (2 ^ RETRY_CNT[7:4])

Table 17. Auto-retry timer summary

RETRY_CNT [7:4] [MSB]	Retry timer [ms]	Retry time [sec]	Retry Time [min]
0000	100	0.1	0.001666667
0001	200	0.2	0.003333333
0010	400	0.4	0.006666667
0011	800	0.8	0.013333333
0100	1600	1.6	0.026666667
0101	3200	3.2	0.053333333
0110	6400	6.4	0.106666667
0111	12800	12.8	0.213333333
1000	25600	25.6	0.426666667
1001	51200	51.2	0.853333333
1010	102400	102.4	1.706666667
1011	204800	204.8	3.413333333
1100	409600	409.6	6.826666667
1101	819200	819.2	13.65333333
1110	1638400	1638.4	27.30666667
1111	3276800	3276.8	54.61333333

The retry mask bits OTP_RETRY_MSK[3:0] are provided to set the maximum value for the four most significant bits (4-MSB) of the RETRY_CNT[7:0].

For example, when the retry counter is reset to 0, The device uses the 100 ms retry timer for 15 power-up retry attempts. When the 4 MSB of the retry counter are increased, the TRETRY is re-calculated and the device uses the new TRETRY for the next 15 power-up retry attempts. This process will repeat until the counter reaches the OTP_RETRY_MSK[3:0], where it remains clamped to this value using the corresponding TRETRY for every following power-up retry attempt.

The OTP_RETRY_MODE bit is provided to select whether the auto-retry timer tries to exit the DFS state for a limited number of times, or every time it enters the DFS state.

Table 18. Autoretry dynamic characteristics

OTP_RETRY_MODE	Auto-retry timer mode
0	limited retry
1	infinite retry

In “Limited Retry” operation, the PF09 will try to exit the DFS state until the 4-MSB of the RETRY_CNT[7:0] reach the value of the OTP_RETRY_MSK[3:0] bits. When the 4-MSB of the RETRY_CNT[7:0] reach the OTP_RETRY_MSK[3:0] value, the auto-retry timer is disabled and the system will no longer be able to exit the DFS state via the auto-retry timer.

During “infinite retry” operation, the device will try to exit the DFS state every time the TRETRY expires. When the 4-MSB of the RETRY_CNT[7:0] reach the OTP_RETRY_MSK[3:0] value, the 4-MSB of the retry counter value will be clamped and the device will use the corresponding TRETRY for every following power-up retry attempt.

The auto-retry function is intended to allow the system to retry operation in a timely manner, providing system availability during random fault conditions. At the same time, it provides a power saving strategy when the system experiences a non-recoverable cyclic fault condition, by reducing the frequency at which the device tries to exit the DFS state on every fault cycle.

The retry timer can be rescaled down by writing 0x00 to RETRY_CNT[7:0], which resets it.

If the VIN < UVDET by the time there is a valid condition for leaving the DFS state, the device will wait in the DFS state until VIN > UVDET.

Table 19. Auto-retry time base

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
T_{BASE_RETRY}	Auto-retry time base	95	100	105	ms

11.2.12 VDDOTP modes

The PF09 supports OTP fuse bank configuration and Debug mode through the VDDOTP pin.

- If VDDOTP = GND, the device loads the configuration from the OTP fuses and operates in Normal mode.
- If VDDOTP ≥ 1.3 V, the device enters Debug mode. The OTP configuration is accessible through mirror registers, and the device operates in a limited functionality mode.
- If VDDOTP ≥ 7.5 V, the device enters Programming mode and the OTP configuration is defined in the OTP registers, allowing the device to fuse the OTP registers. This configuration will be loaded in normal operation. Configuration emulation and programming (OTP) can be performed by the customer during engineering development using NXP's latest graphical user interface and an evaluation board. Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

Table 20. VDDOTP pin electrical characteristics

Function name	Description	Symbol	Min	Typ	Max	Unit
VDDOTP_OTP	VDDOTP 1.5 V threshold	VDDOTP1P4TH	1.3	1.4	1.5	V
VDDOTP_DBG	VDDOTP 3.0 V threshold	VDDOTP3P0TH	2.9	3.0	3.1	V
VDDOTP_PGR	VDDOTP programming voltage range	VDDOTP_PRG	7.5	–	8.5	V

11.2.12.1 Debug operation

The PF09 allows temporary configuration to debug or test a customized power-up configuration in the system. To access Debug mode, the VDDOTP pin should be pulled up to high above VDDOTP3P0TH.

In Debug mode, the following conditions are valid:

- I^2C communication uses standard communication, with no CRC and secure write disabled
- The default I^2C address is 0x08, regardless of the address configured by OTP
- Watchdog operation/monitoring is disabled
- Secure write is disabled
- XRESET pin is disabled
- FCCU is disabled
- DVSMIN and DVSMAX limits are disabled

The PF09 can operate normally using the Debug mode configuration, as long as VIN does not go below the UVDET threshold. If VIN is lost (VIN < UVDET) the mirror registers will be reset, and Debug mode configuration must be performed again.

The DBG_MODE flag is provided to indicate the device is in Debug mode.

Table 21. Sys_Diag (register 0x82)

DBG_MODE	Debug mode
0	Disabled
1	Enabled

11.2.12.1.1 Test mode

The device is able to operate in TEST mode. In TEST mode, the system shall be able to access the OTP mirror registers as well as all registers needed for OTP programming.

In TEST mode, the following conditions are valid:

- I^2C communication uses standard communication, with no CRC and secure write disabled
- The default I^2C address is 0x08, regardless of the address configured by OTP
- Watchdog operation/monitoring is disabled
- Secure write is disabled
- XRESET pin is disabled
- FCCU is disabled
- DVSMIN and DVSMAX limits are disabled

11.2.12.1.1.1 OTP emulation

OTP Emulation mode allows the user to modify OTP mirror registers before powering up. This facilitates exercising different features of the PF09 while deciding on the best configuration for a given application. This is especially useful when optimizing the SWx compensation for the desired transient response.

In emulation mode, only a VIN < UVDET or a critical DMS fault condition sends the device into the DFS state and causes a fuse reload upon exiting the DFS state.

11.2.12.1.1.2 OTP fuse programming

OTP fuse burning is performed in the DBGOFF state.

To burn the OTP fuses, devices must enter Test mode and write the desired values in the mirror registers.

Once the proper configuration is set on the mirror registers, the device is configured.

The programming command is executed while VDDOTP has a programming voltage between 7.5 V < VDDOTP < 8.5 V.

12 General device operation

12.1 UVDET

VIN > UVDET is a mandatory condition for the PMIC to start a power-on cycle. Once a power-on cycle is started, the device allows full operation as long as VIN does not fall below the falling UVDET threshold.

When VIN falls below the UVDET threshold in any state after the DBGOFF state, the device moves to the Deep Fail-safe state and waits for proper conditions to exit the DFS state.

When the VIN crosses the UVDET threshold on the rising edge, the devices will set the UVDET_FAIL flag to 1 to provide debugging information to the system. The UVDET_FAIL bit can be cleared by writing a 1 to it.

Table 22. UVDET electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{UVDET_RISE}	Rising UVDET	2.8	2.85	2.9	V
V_{UVDET_FALL}	Falling UVDET	2.7	2.75	2.8	V

12.2 VIN OV monitoring

The VIN_OV monitor is provided as a last-resort protection against a VIN supply out of range, and its main purpose is to prevent PMIC operation with a VIN condition out of the maximum operating range of the PF09.

The VIN_OV monitoring can be enabled or disabled by default in the OTP registers via the OTP_VIN_OV_EN bit, and the function can be disabled during the system-on states for system debugging purposes via the VIN_OV_EN functional bit.

Table 23. VIN_OV_EN bit

VIN_OV_EN	VIN OV monitor
0	Disabled
1	Enabled

When the VIN_OV monitor is enabled, The device monitors its input voltage and is can be programmed to react to an over-voltage as defined by the VIN_OV_SDWN bit. The default value of the VIN_OV_SDWN bit is set in the OTP registers via the OTP_VIN_OV_SDWN bit.

Table 24. VIN_OV_SDWN bit

VIN_OV_SDWN	VIN OV reaction
0	Interrupt Only
1	PMIC Shutdown

The VIN_OV is available during the monitored system-on states (RUN and STANDBY) and also during a power-up event to ensure the system is not started with a VIN fault condition present.

If a VIN_OV condition is present during a power-up event, the device will not allow the power-up sequence to start, regardless of the value of the VIN_OV_SDWN, to prevent the system from starting with a potential fault condition.

VIN_OV monitoring is provided with a programmable debounce to select the filtering time to detect a VIN_OV event. The default value for the VIN_OV_DBNC[1:0] is set in the OTP registers via the OTP_VIN_OV_DBNC[1:0] bits.

Table 25. VIN_OV_DBNC bit field

VIN_OV_DBNC[1:0]	VIN OV debounce value (us)
00	10
01	100
10	1000
11	Reserved

Table 26. VIN_OV electrical characteristics

Symbol	Description	Min	Typ	Max	Unit
V_{IN_OV}	VIN overvoltage rising	5.65	5.8	5.95	V
$V_{IN\_OV\_HYS}$	VIN overvoltage hysteresis	50	100	125	mV

12.3 Device power-up

12.3.1 IC startup

The PF09 provides a quick startup time from the point VIN crosses the VIN_POR threshold until the RSTB pin is released.

For practical purposes, the power-up timing is considered from the wake-up event (exit ULPOFF or exit the DFS) until the device is ready to start the power-up sequence (PWRUP_READY), assuming no event is gating the power-up sequence.

In devices with high safety integrity levels (ASIL/SIL) where the LBIST is available, the LBIST routine will be performed as part of the initial configuration right after the wake-up event and will be followed by a fresh fuse loading.

In devices with no LBIST available, the initial configuration requires only a single fuse loading event, thus reducing the overall turn-on time.

When VAON is configured as a system regulator, the VAON supply can be configured to turn on during the power-up sequence, and it will not be considered as a gating factor to reach PWRUP_READY condition.

Pulling up the PWRON pin to VIN or VAON is possible to ensure an automatic PWRON event at cold boot before the system MCU can take over the control of the PWRON pin. In that scenario, the PWRON event will be evaluated after the fuse-loading routine is finished (entering the LPOFF state).

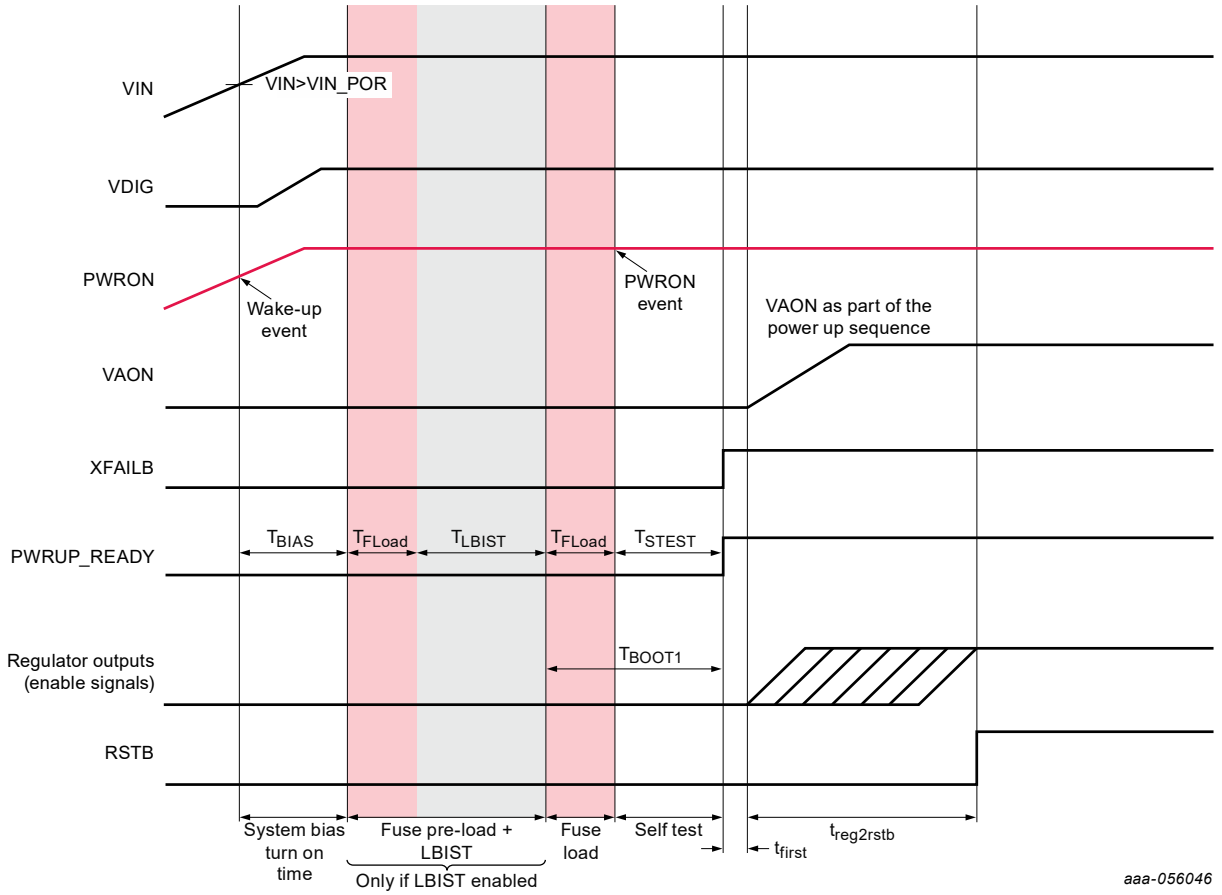


Figure 7. PF09 Startup from cold boot (VAON as system regulator)

When VAON is configured as an always-on regulator, the VAON must be within regulation in order to reach the PWRUP_READY condition.

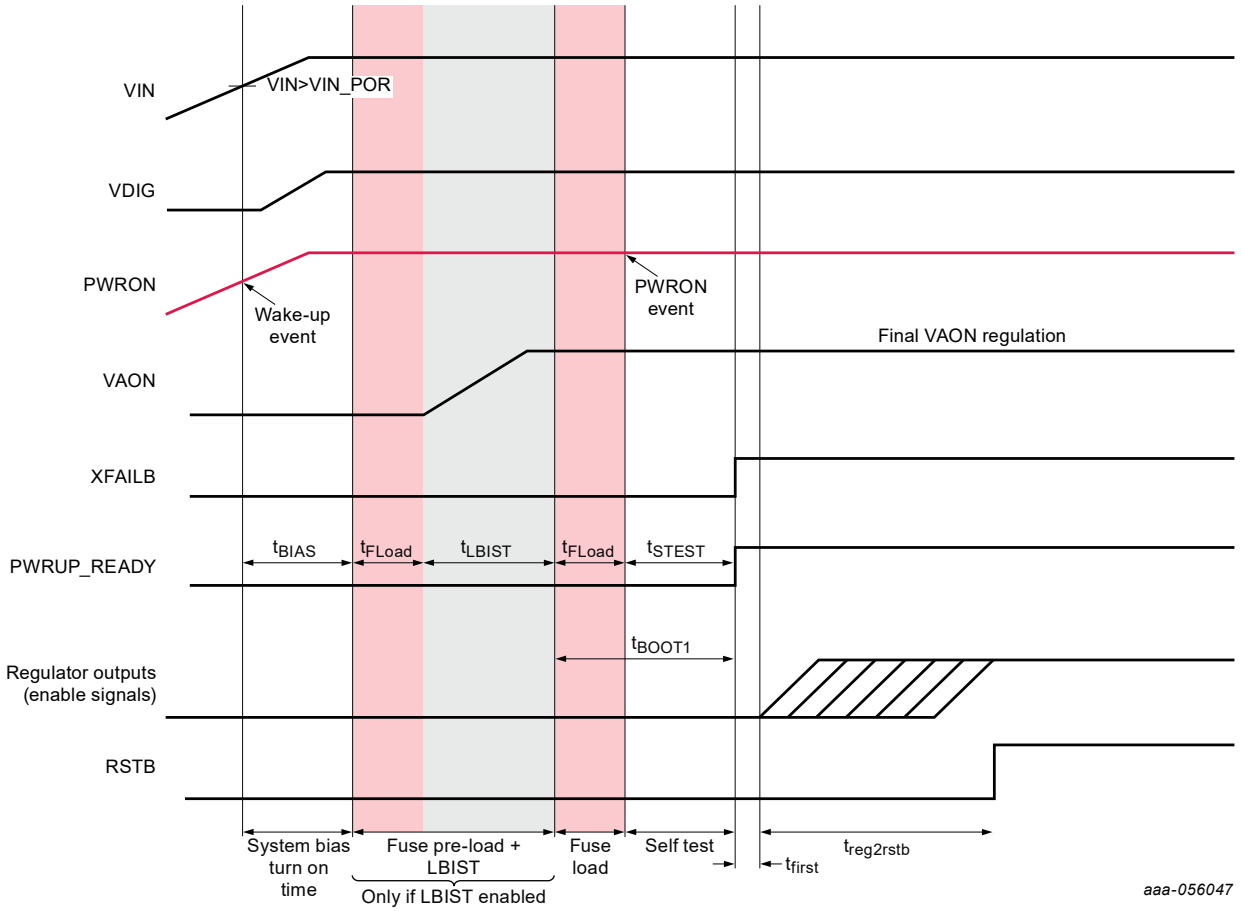


Figure 8. PMIC Startup from Cold boot (VAON Always-on)

A cold boot without a default PWRON event will proceed to load an initial configuration and then return to the ULPOFF state until a valid wake-up event is present on the PWRON pin.

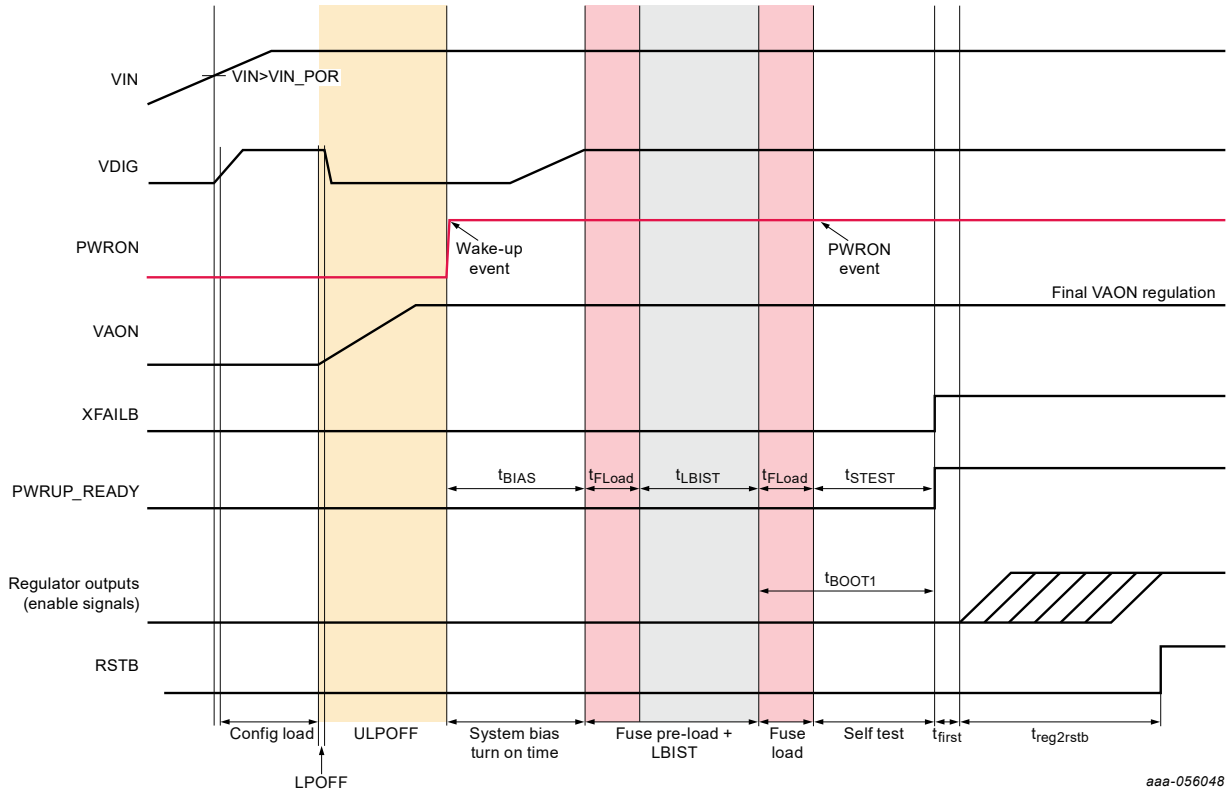


Figure 9. PMIC Startup from Cold boot (No default PWRON event)

When waking up from the DFS state, the device will proceed to load the initial configuration. If the VAON is configured as an always-on supply, it will turn on the regulator, and the VAON output is required to be in regulation in order to reach the PWRUP_READY condition.

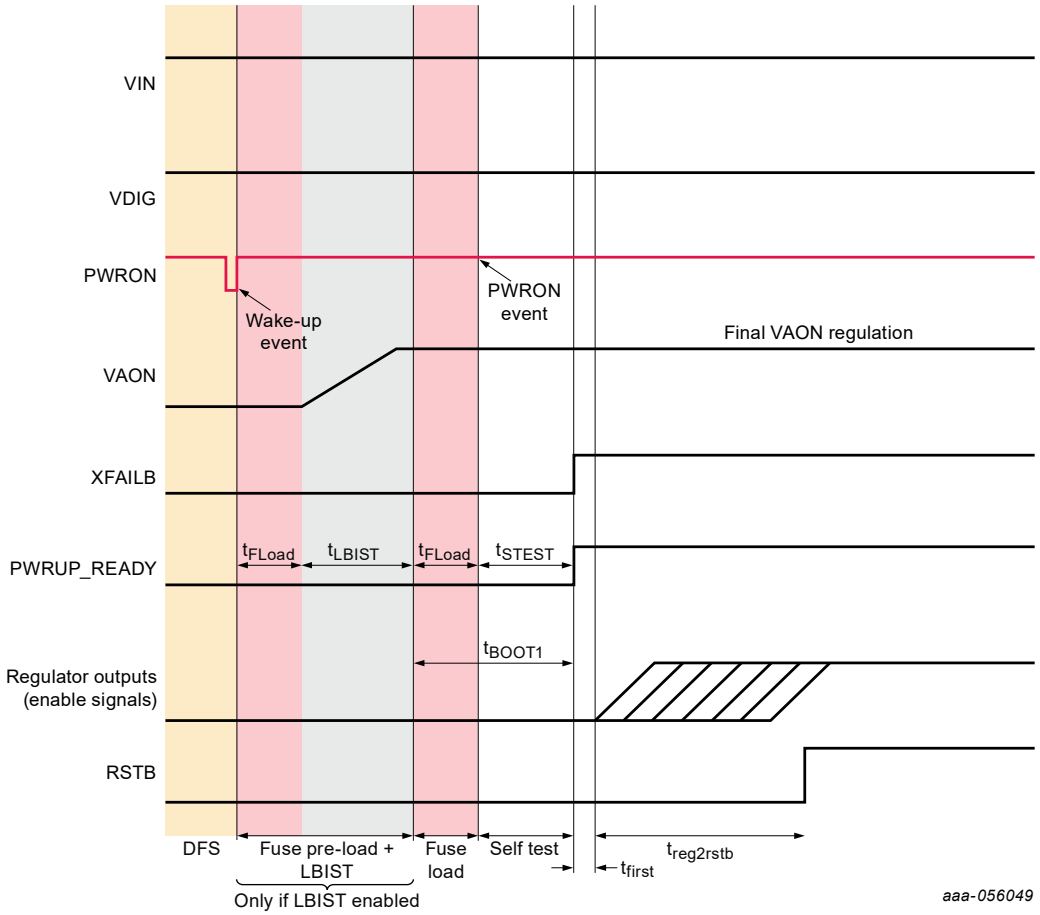


Figure 10. PMIC wake-up from DFS

The default timing for the external regulators to start up is set via the OTP bits as described in Section 12.3.3.

Table 27. IC startup dynamic characteristics

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
t_{Bias}	System bias turn-on time • From wake-up event (PWRON or cold boot) • Analog core biasing until digital supply is in regulation.	–	370	625	µs
t_{FLoad}	Fuse load time • VDIG in regulation to FUSE_LOAD_DONE	–	190	200	µs
t_{STEST}	Self-test time • From PWRON event detected until STEST_DONE • PWRUP_READY = STEST_DONE, assuming no event is gating the power-up sequence.	–	770	800	µs
t_{LBIST}	LBIST test time • LBIST enabled • Includes initial fuse load	–	–	4.5	ms
t_{First}	Time from PWRUP_READY to regulator in first slot to start rising.	–	–	100	µs

12.3.2 Power-up events

Upon loading the OTP fuses, the device will evaluate a PWRON event in the LPOFF State based on the OTP_PWRON_MODE bit.

When OTP_PWRON_MODE = 0, the PWRON pin must be pulled high to generate a power-on event. If the PWRON pin is low during the LPOFF, the device will return to the ULPOFF until a new wake-up condition is present.

When OTP_PWRON_MODE = 1, the PWRON pin must see a high to low transition and remain low for as long as the PWRON_DBNC timer, to generate a power-on event. If the PWRON pin has not experienced a high to low transition, the device will remain in the LPOFF until a valid PWRON event is present.

Upon a power up event reaching the DBGOFF state, the device will proceed to the power-up sequence only if:

VIN > UVDET

&& T_J is at least 10 °C below the TSD threshold

&& VIN < VIN_OV (unless the OV is disabled or OTP_VIN_OV_SDWN = 0)

&& TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0

&& LBIST_STATUS[1:0] is different from “10” (If LBIST enabled)

&& XFAILB pin is released high. (If XFAILB enabled)

12.3.3 Regulator Power-up sequence

The PF09 provides two different ways to power up.

Time-based power up: the system regulators are sequenced up in up to 254 slots, with a constant time separation between each slot.

Dynamic power up: the system regulators are turned on sequentially only after regulators in the previous hierarchical level have reached the point of regulation.

The selection of the default Power-up sequence behaviors is done in OTP during the device OTP customization stage.

12.3.3.1 Time-based power-up

When the OTP_SEQ_MODE = 0, the device will power up in time-based mode.

In the time-based mode, the OTP_SEQ_TBASE[1:0] bits set the default time base for the power-up and power-down sequencer.

Table 28. Default sequencer time base

OTP_SEQ_TBASE[1:0]	SEQ_TBASE[1:0]	Sequencer time base [µs]
00	00	30
01	01	120
10	10	250
11	11	500

After power-up, the SEQ_TBASE[1:0] bits can be modified during the system-on states in order to change the sequencer timing during RUN-to-STANDBY transitions as well as during the power-down sequence.

The PF09 controls the power-up sequencing for the switching regulator, LDO regulators, external VMON inputs, and GPIO pins, as well as controlling the release of the RSTB signal as programmed in the respective

OTP_xxxx_SEQ[7:0] bits. The GPOx_SEQ[7:0] bits for the programmable IOs are valid only if the IO pin is configured as a GPO. (OTP_GPIOx_MODE = 0.)

Table 29. List of channels with selectable power-up sequencing

Channel	OTP bits	Functional bits (power-down sequence)	Required condition
SW1	OTP_SW1_SEQ[7:0]	SW1_SEQ[7:0]	–
SW2	OTP_SW2_SEQ[7:0]	SW2_SEQ[7:0]	–
SW3	OTP_SW3_SEQ[7:0]	SW3_SEQ[7:0]	–
SW4	OTP_SW4_SEQ[7:0]	SW4_SEQ[7:0]	–
SW5	OTP_SW5_SEQ[7:0]	SW5_SEQ[7:0]	–
LDO1	OTP_LDO1_SEQ[7:0]	LDO1_SEQ[7:0]	–
LDO2	OTP_LDO2_SEQ[7:0]	LDO2_SEQ[7:0]	–
LDO3	OTP_LDO3_SEQ[7:0]	LDO3_SEQ[7:0]	–
VAON	OTP_VAON_SEQ[7:0]	VAON_SEQ[7:0]	–
RSTB	OTP_RSTB_SEQ[7:0]	RSTB_SEQ[7:0]	–
GPIO1	OTP_GPO1_SEQ[7:0]	GPO1_SEQ[7:0]	OTP_GPIO1_MODE = 00 or 01
GPIO2	OTP_GPO2_SEQ[7:0]	GPO2_SEQ[7:0]	OTP_GPIO2_MODE = 00 or 01
GPIO3	OTP_GPO3_SEQ[7:0]	GPO3_SEQ[7:0]	OTP_GPIO3_MODE = 00 or 01
GPIO4	OTP_GPO4_SEQ[7:0]	GPO4_SEQ[7:0]	OTP_GPIO4_MODE = 00 or 01
VMON1	OTP_VMON1_SEQ[7:0]	VMON1_SEQ[7:0]	–
VMON2	OTP_VMON2_SEQ[7:0]	VMON2_SEQ[7:0]	–

The _SEQ[7:0] bits set the corresponding channel sequence from 0 to 254. A sequence code of 0x00 indicates that the particular channel is not part of the power-up sequence, that is:

- Remains OFF in the case of a regulator
- Remains low in the case of a GPO
- Remains disabled in the case of an external VMON

Regulators, GPIOs and voltage monitors that are not enabled during the power-up sequence can be enabled during the SYSTEM ON states via the functional registers.

Table 30. Channel sequence

OTP_SWx_SEQ[7:0] OTP_LDOx_SEQ[7:0] OTP_GPOx_SEQ[7:0] OTP_VMONx_SEQ[7:0] OTP_RSTB_SEQ[7:0]	SWx_SEQ[7:0] LDOx_SEQ[7:0] GPOx_SEQ[7:0] VMONx_SEQ[7:0] RSTB_SEQ[7:0]	Sequence slot	Startup time [µs]
00000000	00000000	Off	Off
00000001	00000001	0	SLOT0
00000010	00000010	1	SEQ_TBASE x SLOT1
00000011	00000011	2	SEQ_TBASE x SLOT2
…	…	…	…
11111101	11111101	252	SEQ_TBASE x SLOT252
11111110	11111110	253	SEQ_TBASE x SLOT253

Table 30. Channel sequence*...continued*

OTP_SWx_SEQ[7:0] OTP_LDOx_SEQ[7:0] OTP_GPOx_SEQ[7:0] OTP_VMONx_SEQ[7:0] OTP_RSTB_SEQ[7:0]	SWx_SEQ[7:0] LDOx_SEQ[7:0] GPOx_SEQ[7:0] VMONx_SEQ[7:0] RSTB_SEQ[7:0]	Sequence slot	Startup time [µs]
11111111	11111111	254	SEQ_TBASE x SLOT254

If the power good verification mechanism is enabled (OTP_PWRUP_CHK = 1), the device requires all the monitored supplies enabled in the sequence to be within regulation before the RSTB pin can be released.

If RSTB is not programmed in the OTP sequence and OTP_PWRUP_CHK = 0, the RSTB pin will release by default after the last regulator/GPO/VMON has been enabled.

If RSTB is not programmed in the OTP sequence and OTP_PWRUP_CHK = 1, the RSTB pin will release after all regulators in the power up sequence are in regulation.

If the _SEQ[7:0] bits of all channels are set to 0x00 (OFF) and a PWRON event is present, the device will power up in secondary operation. In such a scenario, the device will enter the RUN state without any regulator or external VMON enabled or GPO pin releasing high.

The secondary device operation is a special use case of the Power-up sequence to address the scenario where the PF09 is working as a secondary PMIC, and supplies are meant to be enabled by the MCU during the system operation. In this scenario the RSTB of primary and secondary PMICs are connected together to create an OR condition in which the RSTB signal to the MCU is released only after all PMICs are up in the RUN state.

The PWRUP_I interrupt is asserted when the time slot of the last regulator in the sequence has ended, to indicate the end of the Power-up sequence. By default, the PWRUP_M bit is unmasked at power up to ensure the INTB pin is always asserted to indicate the end of the Power-up sequence to the system MCU.

Upon a power up, readiness of the minimum voltages rails needed for the system to operate is indicated by the release of the RSTB pin. At this point the MCU may not yet be ready to listen and react to an Interrupt event, however, if the sequence extends past the release of the RSTB pin, the MCU can use the INTB as the notification that all system supplies are up and running.

When returning from the STANDBY into the RUN state, the RSTB pin does not generate a transition, therefore the MCU does not know for sure when the PMIC has successfully changed to the RUN state and is ready for full operation. By ensuring the PWRUP_I interrupt is not masked upon entering the STANDBY state, the system can rely on the INTB pin asserting once the device has successfully entered the RUN state to indicate the system is ready to perform full operation.

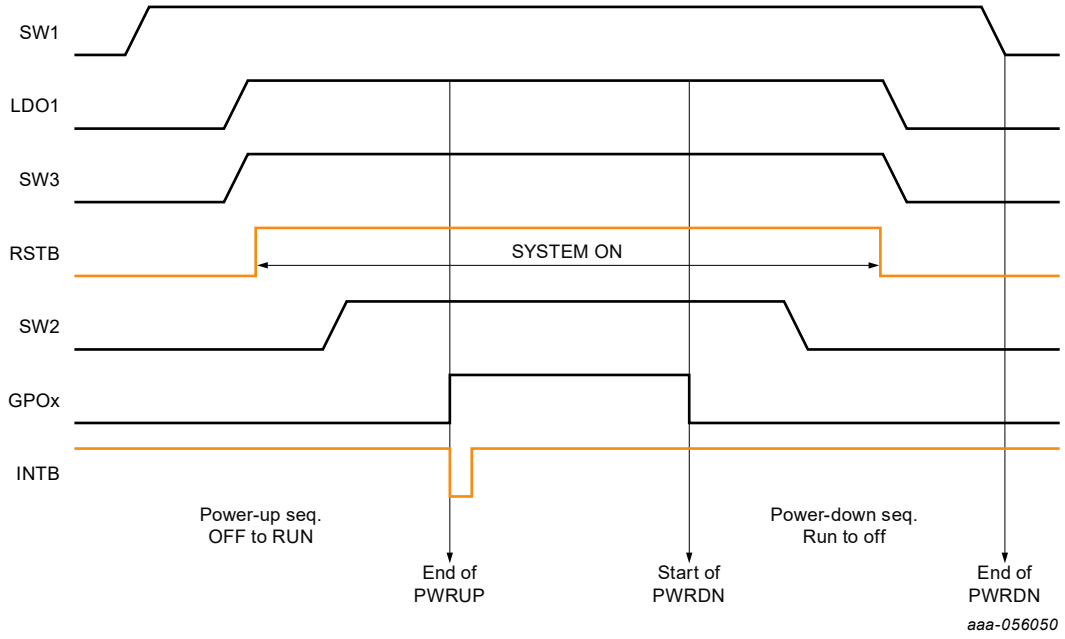


Figure 11. Power up/down Transitions

12.3.3.2 Dynamic power-up

When the OTP_SEQ_MODE = 1, the device will power up in dynamic mode.

When operating in dynamic mode, the device uses the OTP_XXX_SEQ[7:0] bits to set the order in which the system regulators will be enabled during the power-up sequence. The particular slot selection is not relevant for the power-up sequence, instead, the slot number is used to create a hierarchical order during power-up. (Regulators with lower slot numbers belong to a lower hierarchical level).

When the OTP_SEQ_MODE = 1, the power-down sequence still uses the XXX_SEQ[7:0] and TBASE[1:0] bits to power down in the reverse time-based sequence as defined in Section 12.4.

Table 31. Dynamic power down sequence example

Channel	OTP_XXX_SEQ[7:0]	Sequenced power up/down slot	Dynamic hierarchical level
SW1	0000_0010	Slot 1	Level 2
SW2	0000_0100	Slot 3	Level 3
SW3	0000_1000	Slot 7	Level 5
SW4	0000_0111	Slot 6	Level 4
SW5	0000_0011	Slot 3	Level 3
GPIO1	0000_1000	Slot 7	Level 5
LDO1	0000_0010	Slot 1	Level 2
LDO2	0000_0000	OFF	OFF
VAON	0000_0001	Slot 0	Level 1
RSTB	0001_1111	Slot 31	Level 7

Regulators with the lower hierarchical level power up first, and regulators in the next hierarchical level will start powering up only after the previous regulators have reached the point of regulation.

The OTP_SEQ_TSET[1:0] bits are provided to set the settling timer, to allow regulators to reach regulation after they have been enabled.

Table 32. Dynamic sequence settling time

OTP_SEQ_TSET[1:0]	Dynamic sequence settling time
00	500 µs
01	1000 µs
10	2000 µs
11	4000 µs

When regulators and GPIO in the same hierarchical level are enabled, the settling timer is started, and the voltage regulators will be monitored for OV and UV during and after their turn-on ramp.

If any of the regulators in the current hierarchical level is not able to reach regulation before the settling timer is expired, the device will detect a power-up failure and start a power-down event right away. See section Section 12.6.5 for more details.

When all regulators in the same or previous hierarchical level are in regulation, the sequencer will proceed to the next hierarchical level and restart the settling timer for the following hierarchical level.

When a GPIO is configured as general purpose output (GPO) and enabled in the Power-up sequence, the device will release the pin in the corresponding hierarchical level and it will start sensing the actual state of the pin to ensure it has been released properly. If the GPIOx pin is not released properly for longer than the settling time, the device will detect a power-up failure and start a power-down event right away.

When a VMONx is enabled in the Power-up sequence, the monitor is expected to see the external supply applied to the pin and in regulation within the settling timer. If the external voltage applied to the VMONx is not able to reach regulation when the settling timer expires, the device will detect a power-up failure and start a power-down event right away.

When RSTB is not programmed in a slot in the Power-up sequence, the RSTB is released as soon as the last regulator in the sequence reaches regulation.

When RSTB is programmed in a slot in the Power-up sequence, the device will release the RSTB in the corresponding hierarchical level, and it will start sensing the state of the pin to ensure it has been released properly. In such a scenario, even though the RSTB signal has already been released, the PMIC will not enter the RUN state until the last regulator has reached regulation properly.

When the device enters the RUN state, it will assert the PWRUP_I interrupt and assert the INTB pin to inform the MCU that it has finished the Power-up sequence properly.

The device will start monitoring system-on fault conditions only after the dynamic Power-up sequence is finished. At this point PGOOD can be released, if all regulators in the sequence are within regulation.

12.4 Power down

12.4.1 Turn-off events

Turn-off events may be requested by the MCU (non-PMIC fault related) or may be due to a critical failure of the PMIC (hard fault condition).

12.4.1.1 Non-PMIC failure turn-off events

When OTP_PWRON_MODE = 0, the device will start a power-down event when the PWRON pin is pulled low.

When OTP_PWRON_MODE = 1, the device will start a power-down event when the PWRON pin sees a transition from high to low and remains low for longer than TRESET And OTP_PWRON_RST_EN = 0

When VIN_OV_EN = 1 and VIN_OV_SDWN = 1, the device will start a power-down event when a VIN_OV event is present.

The device will start a power-down event If the OTP_XFAILB_EN = 1 and the XFAILB pin is pulled low externally.

When a PMIC OFF command is sent by writing SYS_CMD[7:0] = 0xA5, the device will start a 500 µs shutdown timer.

When the shutdown timer is started, the device will trigger an SDWN_I interrupt and assert the INTB pin, provided it is not masked. If the 500 µs timer is expired, the device will start a turn-off event. If the SDWN_I bit is cleared before the 500 µs shutdown timer is expired, the shutdown request is stopped and the shutdown timer is reset.

When the VAON is configured as an always-on regulator, the OTP_XFAILB_VAON bit is used to configure the behavior of the VAON upon an external XFAILB event

Table 33. VAON reaction on XFAILB

OTP_XFAILB_VAON	VAON reaction on XFAILB
0	VAON not affected
1	VAON reset

When OTP_XFAILB_VAON = 0, the VAON will remain enabled while the device cycles through the LPOFF State.

When OTP_XFAILB_VAON = 1, the VAON will be disabled at the end of the power down sequence, and enabled again once the power-down delay is over and the device enters the LPOFF State.

12.4.1.2 Turn-off event due to a hard fault condition

The PF09 will start a power-down event when any of the following conditions are present:

- When an OV, UV or ILIM condition is present long enough for the fault timer to expire.
- When FAULT_CNT[3:0] = FAULT_MAX_CNT[3:0]
- When T_J is at least 10 °C below the TSD threshold
- When the reset counter reaches the maximum count (RESET_CNT = RESET_MAX)
- When the RSTB pin is shorted externally for longer than the OTP_RSTB_TSHORT[1:0] timer

12.4.2 Reset conditions

The PF09 will start a reset event when any of the following events are present:

- A watchdog failure
- A fault condition in the XRESET input (FCCU1 pin)
- A fault condition in the FCCU interface (if programmed to generate the reset)
- A fault condition in the ERRMON input (if programmed to generate the reset)
- A reset event can be initiated by the PWRON pin in Edge-sensitive mode and OTP_PWRON_RST_EN = 1

A software reset can be requested by writing SYS_CMD[7:0] = 0x3E

Reset events can be classified into two types:

1. Hard reset
2. Soft reset

Regardless of which type of reset event is generated, if the FS0B pin is operating in active Safe-state mode, the FS0B pin will be asserted low and remain low through the reset event until the MCU is able to release the pin via the I^2C command.

12.4.2.1 Hard reset

During a Hard reset, the RSTB signal will be asserted as all system regulators, GPOx and VMONs are powered down as indicated in the power down sequence.

The following events can generate a hard reset:

- A watchdog failure
- The PWRON pin used in edge-sensitive mode with the PWRON_RST_EN = 1
- A software reset via the SYS_CMD register
- The FCCU1 pin operating in XRESET mode with the XRST_MODE = 0
- The FCCU failure with the FCCUx_RESET = 10
- The ERRMON failure when ERRMON_RESET = 1

If the VAON is set as an always-on regulator, the PF09 uses the VAON_RESET_EN bit to choose whether the VAON output is included in the RESET event or not.

Table 34. VAON always-on reset reaction

VAON_RESET_EN	VAON always-on reset reaction
0	VAON Reset disabled
1	VAON Reset enabled

By default, the VAON_RESET_EN bit is reset to 0 at power up. The MCU must set this bit during the MCU boot-up sequence if the VAON is required to perform a reset together with the rest of the system regulators when the reset event is present.

During a hard reset event, if the VAON is set as a system regulator, the VAON regulator is disabled as defined in the power-down sequence.

When a hard reset condition is present, the device will clear all the interrupt latches before starting the new power-up sequence, to allow the device to release and assert the INTB pin when the PWRUP_I is latched upon power-up sequence.

12.4.2.2 Soft reset

The following events can generate a soft reset:

- The XRESET input (FCCU1 pin) with XRST_MODE = 1
- An FCCU failure with the FCCUx_RESET [1:0] = 01

When the VAON is set as an always-on regulator, the soft reset does not have any impact on this regulator.

If the VAON is set as a system regulator, the VAON_RESET_EN bit will set the behavior of the VAON during a soft reset event.

Table 35. Soft reset impact

VAON_RESET_EN	Soft reset impact
0	VAON ignores the soft reset
1	VAON reloads default configuration

Selected functions whose SOFTRST_EN bits are set to 1 can reload the default OTP values during the soft reset event.

The WD_SOFTRST_EN bit is provided to allow the WD_DURATION[3:0] bits to keep the current value or be reset to the default OTP value during a soft reset event.

Table 36. WD duration on soft reset

WD_SOFTRST_EN	WD duration on soft reset
0	No reset
1	Reset to default OTP

When the GPIOx pins are configured as general purpose outputs, the GPOx_SOFTRST_EN bits are provided to decide whether the respective GPO should keep the current values or reload the default configuration when a soft reset is present.

Table 37. Effect of soft reset on GPO

GPOx_SOFTRST_EN	Soft reset impact
0	Output ignores the soft reset
1	Reset to default value

The default value for GPIO bits is evaluated based on the OTP_GPIOx_SEQ bits:

- If OTP_GPIOx_SEQ = 0x00, the output is defaulted to LOW.
- If OTP_GPIOx_SEQ != 0x00, the output is defaulted to HIGH.

The behavior of the system regulators (SWx/LDOx) upon a soft reset is controlled by the corresponding SWx_SOFTRST_EN/LDOx_SOFTRST_EN bits.

Table 38. Effect of soft reset on system regulators

SWx_SOFTRST_EN LDOx_SOFTRST_EN	Soft reset tmpact
0	Ignores the soft reset
1	Reload the default value

System regulators that are set to react to a soft reset will react based on the default configuration set by the OTP registers.

Regulators that were enabled in the Power-up sequence will remain enabled, but if the output voltage was changed during the system operation, it will return to the default voltage level set by the OTP bits.

Regulators that were not enabled during the power-up sequence, but were turned on during the SYSTEM ON states, will be disabled when the default value is reloaded.

The VMONx_SOFTRST_EN bit is provided to determine whether the external VMON input will maintain the current configuration or return to the default configuration when a soft reset is present.

Table 39. Effect of soft reset on external VMON input

VMONx_SOFTRST_EN	Soft reset impact
0	Ignores the soft reset
1	Reload the default value

When the VMONx is programmed to reload the default value on a soft reset, the corresponding voltage monitoring will be disabled if the block was not enabled by default during the power up sequence.

If VMON1 or VMON2 are enabled when a soft reset occurs, the voltage monitoring will be masked during the soft reset, and the VMON mask timer will be started. The voltage monitoring channel will be unmasked after the VMON mask timer VMONx_TMASK[1:0] has expired, and the system will start monitoring for OV/UV conditions at the default voltage level.

The RSTB can be programmed to remain released or assert temporarily to generate a physical reset condition for the MCU. The RSTB_SOFTRST[1:0] bits are provided to program the behavior of the RSTB pin upon a soft reset condition.

Table 40. RSTB pulse on soft reset

RSTB_SOFTRST[1:0]	RSTB pulse on soft reset
00	No RSTB assertion
01	Assert RSTB for 100 µs
10	Assert RSTB for 500 µs
11	Assert RSTB for 1000 µs

The OTP_RSTB_SOFTRST[1:0] is provided to set the default value of the RSTB_SOFTRST[1:0] bits.

In applications where the watchdog timer is enabled at power-up, if the RSTB pin is programmed to assert temporarily during a soft reset, the device will stop the watchdog timer during the reset event and it will restart with the default configuration after the RSTB pin is released, to allow the system to perform the initial configuration and start servicing the watchdog again.

When a soft reset event is present, the device will clear all the interrupt latches before reloading the default values into the functional register. This allows the device to assert the INTB pin when the PWRUP_I is latched, when all voltages finished transitioning to the default values.

12.4.2.3 Reset counter

When the device has started a reset event, the value in the RESET_CNT[3:0] bits will be increased. If the RESET_CNT[3:0] reaches the maximum number of reset events allowed by the RESET_MAX[3:0] bits, the system will detect a cyclic reset failure and it will perform a fault power-down sequence and proceed to the Fail-safe transition.

The MCU is expected to clear the RESET_CNT[3:0] when it is able to regain proper operation after the reset condition. The RESET_CNT[3:0] will be reset automatically when the state machine enters the LPOFF state, to ensure the system starts with a clean count on a fresh power-up event. The RESET_MAX[3:0] is loaded with the values on the OTP_RESET_MAX[3:0] bits.

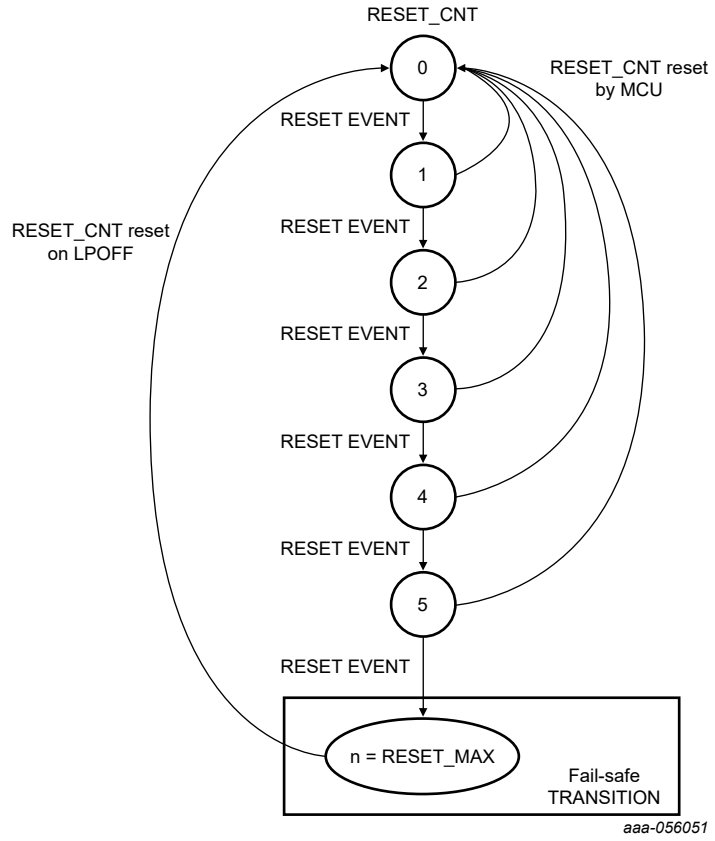


Figure 12. Reset counter strategy.

The device can bypass the cyclic reset failure by setting the RESET_MAX[3:0] = 0x00. In this scenario, the PMIC will be able to keep generating reset events, however, the device will never be able to proceed to a fault shutdown.

If the cyclic reset failure is bypassed, the RESET_CNT[3:0] value will still be increased for every reset event until it reaches the maximum count (0b1111), and it will keep that value until the counter is reset manually or when the device crosses into the LPOFF state.

12.4.3 Early warning

When a power down is initiated due to a fault condition, an EWARN_I interrupt will be set, and the INTB pin will be asserted before it starts the Power-down sequence.

The following fault modes will generate an EWARN interrupt:

- Fault timer expired
- FAULT_CNT = FAULT_MAX_CNT
- Thermal shutdown (T_J > TSD)
- A hard reset event
- A VIN_OV event when VIN_OV_SDWN=1
- A turn-off event due to RSTB being asserted externally

The OTP_EWARN_TIME[1:0] allows the user to select a time delay from when the EWARN interrupt is generated and the power-down sequence is started.

Table 41. EWARN delay time

OTP_EWARN_TIME[1:0]	EWARN delay time
00	100 µs
01	5 ms
10	20 ms
11	50 ms

12.4.4 Power-down sequencing

The PF09 provides a highly flexible scheme to control the power-down sequence. It relies on the configuration of the _SEQ[7:0] bits and the SEQ_TBASE[1:0] bits to set the order in which the voltage regulators, GPIO, or voltage monitors will be sequenced down during a power-down event.

The values of the _SEQ[7:0] and SEQ_TBASE[1:0] bits are set by default, as defined by the Power-up sequence in the OTP registers. The regulators, GPIO, and VMON, will perform the power-down sequence in the reverse order with respect to the Power-up sequence, that is, channels with the higher slot in their corresponding _SEQ[7:0] bits will be disabled first, and those with the lower slot will be disabled last.

Channels whose _SEQ[7:0] bits are set to 0x00 will be disabled first, before the sequenced slots are disabled.

In scenarios where the system requires a different power-down sequencing, the MCU can change the values in the _SEQ[7:0] and SEQ_TBASE[1:0] bits during the SYSTEM ON states to ensure the PMIC will sequence down in the next power cycle following the new values.

When the device passes through any of the OFF States, the SEQ_TBASE[1:0] and _SEQ[7:0] bits are reloaded with the default values in the OTP registers before it starts the next power-up sequence, to ensure the system is able to power up with a valid Power-up sequence.

If all of the sequence bits are set to _SEQ[7:0] = 0x00, all the system regulators, VMONx, GPOx, and RSTB pins will be turned off at once when the power-down sequencer is invoked.

12.4.4.1 VAON power-down control

The behavior of the VAON during a power-down sequence is dependent on the mode of operation of this LDO.

When the VAON is configured as a “system regulator”, it will be included in the Power-down sequence based on the _SEQ[7:0] bits, as described in the previous section.

When the VAON is configured as an “always-on regulator”, the output will remain enabled during the power-down sequence, and during the OFF states, to ensure the system doesn’t lose this voltage during the full power cycle.

If the power down is started by an OV/UV condition on the VAON supply operating as an always-on regulator, the reaction of the output will depend on the fault mode configuration of the VAON regulator. Refer to Section 12.6.3 for detailed description of the VAON behavior in this particular scenario.

If the device reaches the Deep Fail-safe state (DFS), the VAON output will be disabled to protect the system, and default operation will be recovered once the device exit the DFS state and the OTP fuses are reloaded.

12.4.4.2 Power-down delay

A programable delay after the power-down sequence can be set using the PD_SEQ_DLY[2:0] bits.

Table 42. Delay after power-down sequence

PD_SEQ_DLY[2:0]	Delay after power-down sequence
000	No delay
001	1 ms
010	5 ms
011	10 ms
100	50 ms
101	100 ms
110	250 ms
111	500 ms

The default value of the power-down delay is set via the OTP_PD_SEQ_DLY[2:0] bits, and the MCU can modify the value during the SYSTEM ON states via the PD_SEQ_DLY[2:0] bits.

After a power-down sequence is started, the PWRON pin is masked until the power-down sequences are finished and the programmable power-down delay is over. Only then can the device power up again if a power-up event is present.

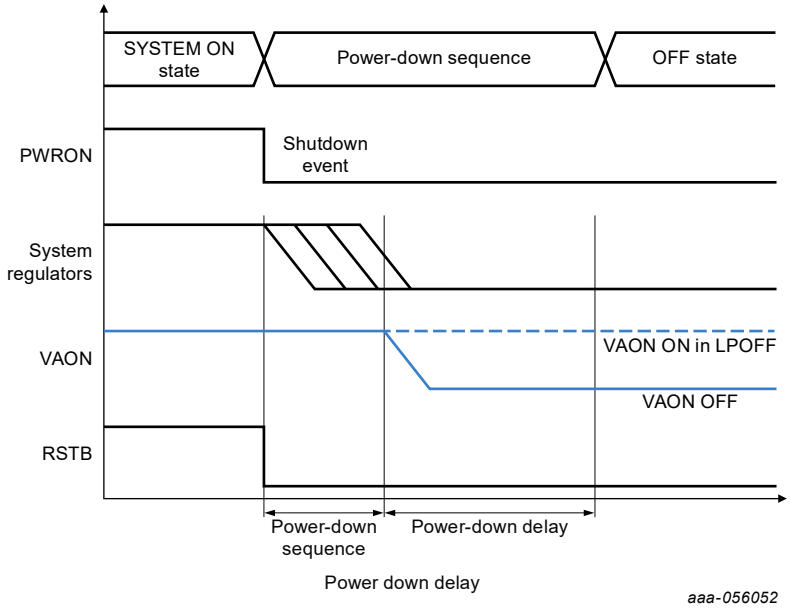


Figure 13. Power-down delay

12.5 RUN/STANDBY transitions

The PF09 provides independent configuration for the voltage regulators during the RUN and STANDBY states. the PF09 relies on the power-up and power-down sequencing to ensure proper transition between these two states.

Figure 14 shows an example of the Power-up/down sequence when transitioning from RUN to STANDBY and back to the RUN state.

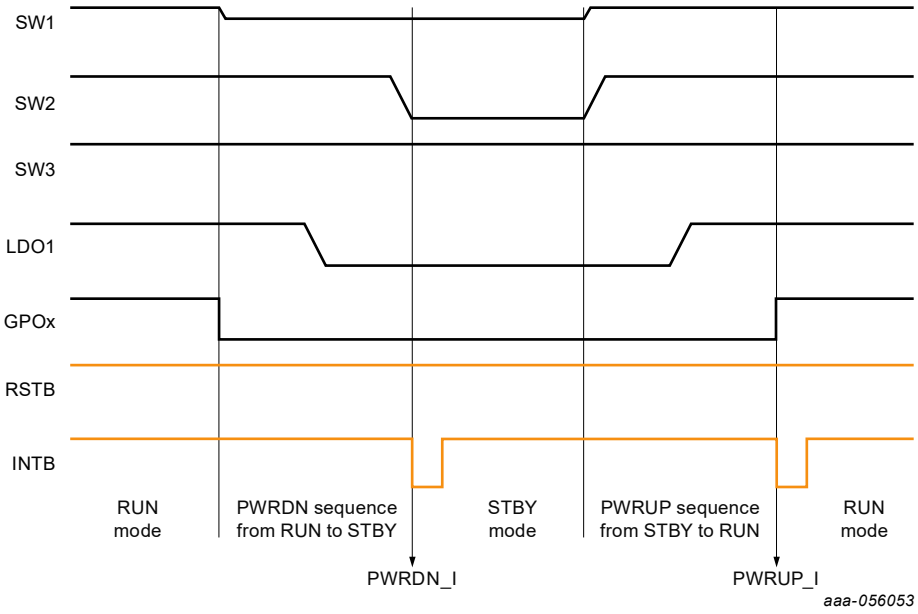


Figure 14. RUN and STANDBY transitions

12.5.1 RUN to STANDBY transition

When transitioning from RUN to STANDBY, the power-down sequencer is started if any of the system regulators in the power-up sequence needs to be turned off in the STANDBY State.

Regulators with the bits _SEQ[7:0] = 0x00 and whose STANDBY configuration is different from the RUN configuration will change to the corresponding STANDBY mode first, followed by the regulators / GPIOs with a power-down slot assigned in the _SEQ[7:0] bits.

If system regulators are not turned off during this transition, the power-down sequence for such regulators is ignored and the voltage transition happens at the beginning of the power-down sequence.

The PWRDN_I interrupt is set at the end of the transition from RUN to STANDBY when the Power-down sequence is finished.

Note that any associated dynamic voltage scaling (DVS) transitions on the switching regulators will be considered within the power-down sequence, and the PWRDN_I interrupt will be asserted only after all the switching regulators have finished their DVS cycle during the transition. However, because the LDO regulators are discharged passively through the internal pulldown resistor, the changes in the LDO regulators are considered finished right after the new configuration is applied, without taking into consideration the discharge time due to the external capacitor.

12.5.2 STANDBY to RUN transition

When transitioning from the STANDBY state to the RUN state, the time-based Power-up sequence is followed by any of the system regulators set up to enabled during the transition from STANDBY to RUN.

If none of the regulators toggle from OFF to ON, and only voltage changes are being performed when exiting the STANDBY state, the changes in the system regulators are made simultaneously rather than going through the power-up sequencer.

During the transition from STANDBY to RUN, for regulators with the bits _SEQ[7:0] = 0x00 and whose RUN configuration is set to OFF, the regulator will be disabled first, before the power-up sequencer is started.

The PWRUP_I interrupt is set when the device has finished transitioning from STANDBY to RUN.

12.6 Fault management

The PF09 provides a flexible fault management scheme to detect and react to internal and external faults:

- Voltage regulators are monitored internally for overvoltage, undervoltage, and overcurrent.
- Dedicated inputs are used to monitor external supplies for overvoltage and undervoltage.

In devices with safety monitoring, external error monitoring is provided via the XRESET, FCCU, and/or ERRMON interfaces.

Internal random fault conditions are monitored through the various mechanisms provided by the functional safety architecture. Refer to Section 14 for detailed descriptions and fault handling of safety-related mechanisms.

The fault protection mechanisms upon a system regulator fault can be programmed to one or more of the following reactions:

- Set the corresponding interrupt latch and assert the INTB pin if the interrupt is not masked.
- Disable the failing output if the corresponding _STATE bit is set to 0.
- Start the fault timer, if programmed by the TIMER_FAULT[3:0] bits.
- Assert the PGOOD pin low of the corresponding OV/UV, if fault condition is not bypassed.
- Increase the fault counter, if the OV/UV fault condition is not bypassed.
- Assert the FS0B pin (based on device configuration).

The fault protection mechanisms upon an external VMONx OV/UV fault can be programmed to one or more of the following reactions:

- Set the corresponding interrupt latch and assert the INTB pin if the interrupt is not masked.
- Start the fault timer if programmed by the TIMER_FAULT[3:0] bits.
- Assert the PGOOD pin low if the corresponding OV/UV if fault condition is not bypassed.
- Increase the fault counter if the OV/UV fault condition is not bypassed.
- Assert the FS0B pin (based on device configuration).

The fault protection mechanisms upon an FCCU fault can be programmed to one or more of the following reactions:

- Set the corresponding interrupt latch and assert the INTB pin if the interrupt is not masked.
- Assert the FS0B pin.
- Generate a reset condition as defined by the FCCUx_RESET[1:0] bits.

The fault protection mechanisms upon an ERRMON fault can be programmed to one or more of the following reactions:

- Set the corresponding interrupt latch and assert the INTB pin if the interrupt is not masked.
- Assert the FS0B pin.
- Generate a reset condition as defined by the ERRMON_RESET bit.

Fault conditions are classified based on the severity of their reactions:

- Hard faults: fault conditions that cause the device to start a power-down sequence. It is assumed that such a fault may limit the ability of the system (MCU) to properly acknowledge and recover from the fault condition, therefore the PMIC is required to take a definite action to bring the system to a known “good” state to resume proper operation.
- Soft faults: fault conditions that do not start a power-down sequence. It is assumed such faults do not limit the ability of the system to acknowledge and try to act upon the fault condition. Soft faults are signalled by one or more mechanisms, such as the interrupt registers, INTB, FS0B_S or PGOOD pins. The MCU is expected to listen to any of these signals as defined by the system designer, and the system is expected to perform a

corrective action before the PMIC detects a lack of response and proceeds to evaluate the fault conditions as a hard fault.

12.6.1 Fault counter

The PF09 features a programmable fault counter to avoid fault cycling during system operation.

The device uses the FAULT_MAX_CNT[3:0] bits to set the maximum number of soft faults allowed before the PMIC detects a cyclic fault condition and generates a hard fault condition.

When the FAULT_MAX_CNT[3:0] = 0x00, the soft fault condition will still be detected but the system will not be able to generate a system shutdown due to a hard fault.

When the FAULT_MAX_CNT[3:0] is different from 0x00, the PMIC will generate a hard fault when the FAULT_CNT[3:0] = FAULT_MAX_CNT[3:0].

The default value of the FAULT_MAX_CNT[3:0] bits is set by the OTP_FAULT_MAX_CNT[3:0] bits to ensure the system starts operation with a valid configuration. However, the MCU is allowed to change the value of the FAULT_MAX_CNT[3:0] bits at any time to adjust the PMIC reaction to the needs of the application.

If the FAULT_CNT[3:0] < FAULT_MAX_CNT[3:0], the device will initiate the corresponding fault protection mechanism based on the type of fault and the configuration in the functional register bits.

OV, UV, and ILIM faults in the voltage regulators and external VMON will increased the fault counter only if the fault is not bypassed, and no other persistent OV, UV, or ILIM fault is currently present on any of the system regulators or external VMON blocks.

FCCU and ERRMON faults will increase the FAULT_CNT[3:0] only if the FS0B pin transitions from high to low, to prevent multiple fault detections from a fault condition that hasn't been properly cleared out by the MCU.

The MCU is expected to implement a fault acknowledgement routine to read the faults and clear the fault counter when it has taken proper action, and the system is ready to resume normal operation. By implementing such a routine, the system ensures that no fault conditions are stacking up in the fault counter and prevents a random condition from generating a hard fault right away.

The fault counter can be cleared manually by writing the FAULT_CNT[3:0] = 0x00 via an I^2C command, or automatically by allowing the watchdog interface to reduce the counter gradually when a number of consecutive good watchdog refreshes have been performed. Refer to Section 14.4.3 for more details on using the watchdog interface to decrease the fault counter automatically.

12.6.2 System regulators and external VMON fault management

The switching regulators and LDOs are provided with internal voltage monitors to detect overvoltage (OV) and undervoltage (UV) conditions during the Power-up sequence and the SYSTEM ON states. Additionally, overcurrents are detected and protected during the system-on states by the ILIM mechanism.

Note that the voltage monitoring is only able to detect and protect against OV/UV conditions in the monitored STANDBY state (OTP_LP_STBY = 0). If the device is configured to go into the low-power STANDBY state, all monitoring blocks will be disabled to allow the lowest quiescent current possible with the assumption that STANDBY is considered a safe state in which the system will not perform critical activity, therefore no safety monitoring is required.

Refer to Section 13.3 for detailed operation and configuration of the OV/UV monitoring blocks.

Fault reaction of the system regulators and external voltage monitors can be managed through the dedicated fault management bit provided for each block.

12.6.2.1 Output state control

Switching regulators and LDOs supplied by the PF09 are provided with an _OV_STATE bit to select whether the regulator is kept enabled or disabled when the corresponding regulator experiences an OV condition.

Table 43. Regulation reaction on OV condition

SWx_OV_STATE, LDOx_OV_STATE	Regulator reaction on OV
0	Output disabled
1	Output enabled

Switching regulators and LDOs supplied by the PF09,are provided with an _UV_STATE bit to select whether the regulator is kept enabled or disabled when the corresponding regulator experience an UV condition.

Table 44. Regulation reaction on UV condition

SWx_UV_STATE LDOx_UV_STATE	Regulator reaction on UV
0	Output disabled
1	Output enabled

By default the _OV_STATE and _UV_STATE bits are set to 1, and the MCU is expected to configure the reaction of each specific supply during the system configuration sequence, during the booting stage.

The table below lists all the functional bits associated with enabling/disabling the voltage regulators when they experience an OV/UV condition.

Table 45. Bits used to disable regulator during UV or OV

Regulator	Bit to disable the regulator during undervoltage	Bit to disable the regulator during overvoltage
SW1	SW1_UV_STATE	SW1_OV_STATE
SW2	SW2_UV_STATE	SW2_OV_STATE
SW3	SW3_UV_STATE	SW3_OV_STATE
SW4	SW4_UV_STATE	SW4_OV_STATE
SW5	SW5_UV_STATE	SW5_OV_STATE
LDO1	LDO1_UV_STATE	LDO1_OV_STATE
LDO2	LDO2_UV_STATE	LDO2_OV_STATE
LDO3	LDO3_UV_STATE	LDO3_OV_STATE
VAON	VAON_UV_STATE[1]	VAON_OV_STATE[1]

[1] The _STATE bits for the VAON are only applicable when the VAON is working as a system regulator. (not valid in Always-on mode)

When a regulator is programmed to be disabled upon an OV or UV, a _FLT_REN bit is provided to decide whether a regulator can return to its previous configuration or remain disabled after it has been disabled due to an OV or UV condition.

Table 46. Output re-enable

SWx_FLT_REN LDOx_FLT_REN	Output re-enable
0	Output remains disabled
1	Output enabled

If a switching regulator is programmed to turn off upon an OV or UV fault ant the SWx_FLT_REN = 1, the switching regulator will be re-enabled 500 µs after the regulator output has finished its discharge cycle.

If an LDO regulator is programmed to turn off upon an OV or UV fault and the LDOx_FLT_REN = 1, the LDO regulator will allow up to 1000 µs to discharge the output before trying to turn the LDO back on.

If an LDO or switching regulator is programmed to turn off upon an OV or UV fault and the _FLT_REN bit is set to 0, the regulator will remain disabled and the MCU can turn it back on by toggling off and on the corresponding enable/mode bits.

The _FLT_REN bits are defaulted to 1 at power-up, and the MCU is expected to configure the desired behavior for each voltage regulator during the system configuration sequence during the booting stage.

12.6.2.2 Fault bypass control

The PF09 provides a set of fault bypass configuration bits to assign different levels of priority to each specific fault for each voltage regulator and external voltage monitor.

The system LDOs and switching regulators are provided with an _IL_BYP bit to bypass the ILIM protection mechanisms. By default, the _IL_BYP bits are set to 1 and the MCU is expected to set the desired configuration during the system configuration sequence at power-up.

Table 47. ILIM protection bypass bit

SWx_IL_BYP LDOx_IL_BYP	ILIM protection
0	Enabled
1	Bypassed

The System LDOs and switching regulators are provided with an _OV_BYP bits to bypass the OV protection mechanism on the respective block. By default the _OV_BYP bits are set to 0 and the MCU is expected to set the desired configuration during the system configuration sequence at power-up.

Table 48. OV protection bypass bit

SWx_OV_BYP LDOx_OV_BYP	OV protection
0	Enabled
1	Bypassed

The System LDOs and switching regulators are provided with an _UV_BYP bits to bypass the UV protection mechanism on the respective block. By default the _UV_BYP bits are set to 0 and the MCU is expected to set the desired configuration during the system configuration sequence at power-up.

Table 49. UV protection bypass bit

SWx_UV_BYP LDOx_UV_BYP	UV protection
0	Enabled
1	Bypassed

The table below lists all the functional bits associated with enabling/disabling the voltage regulators when they experience an OV/UV condition.

Table 50. Bits to enable/disable regulators at UV/OV

Regulator	bit to bypass a current limit	bit to bypass an undervoltage	bit to bypass an overvoltage
SW1	SW1_IL_BYP	SW1_UV_BYP	SW1_OV_BYP
SW2	SW2_IL_BYP	SW2_UV_BYP	SW2_OV_BYP

Table 50. Bits to enable/disable regulators at UV/OV*...continued*

Regulator	bit to bypass a current limit	bit to bypass an undervoltage	bit to bypass an overvoltage
SW3	SW3_IL_BYP	SW3_UV_BYP	SW3_OV_BYP
SW4	SW4_IL_BYP	SW4_UV_BYP	SW4_OV_BYP
SW5	SW5_IL_BYP	SW5_UV_BYP	SW5_OV_BYP
LDO1	LDO1_IL_BYP	LDO1_UV_BYP	LDO1_OV_BYP
LDO2	LDO2_IL_BYP	LDO2_UV_BYP	LDO2_OV_BYP
LDO3	LDO3_IL_BYP	LDO3_UV_BYP	LDO3_OV_BYP
VAON	—	VAON_UV_BYP	VAON_OV_BYP

Bypassing the fault detection prevents the specific fault from incrementing the counter, starting the fault timer, or disabling the regulator, if programmed to turn off upon the specific fault.

Bypassing the OV/UV fault detection will also prevent the OV/UV condition from asserting the PGOOD pin when the corresponding PG_EN is set to 1.

If a specific fault is bypassed, the PF09 will still set the corresponding interrupt bit and the INTB pin will be asserted if the interrupt is not masked.

12.6.2.3 Fault timer

To prevent a persistent fault condition, the PF09 provides a programmable fault timer in order to generate a hard fault in the event the soft-fault condition due to an OV,UV or ILIM cannot be cleared.

The default value for the duration of the fault timer is set by the OTP_TIMER_FAULT[3:0] bits, however the timer duration can be changed during the system-on states by modifying the TIMER_FAULT[3:0] bits in the I^2C registers.

Table 51. Fault timer

TIMER_FAULT [3:0]	Fault timer value
0000	Disabled
0001	1 ms
0010	2 ms
0011	4 ms
0100	8 ms
0101	16 ms
0110	32 ms
0111	64 ms
1000	128 ms
1001	256 ms
1010	512 ms
1011	1024 ms
1100	2048 ms
1101	Reserved
1110	Reserved

Table 51. Fault timer*...continued*

TIMER_FAULT [3:0]	Fault timer value
1111	Reserved

While the fault timer is in progress, the processor is expected to take action to clear the fault condition. For example, it could reduce its load in the event of a current limit fault, or turn off the regulator in the event of an overvoltage fault.

If the fault is cleared before the fault timer expires, the state machine will resume normal operation, and the fault timer will be restarted on the next fault condition.

If the fault does not clear before the timer expires, a hard fault is generated and the device will start a power-down sequence. Once system regulators are turned off after a hard-fault shutdown, the device will move to the Fail-safe transition in order to keep track of the number failing events in the system.

When the fault timer is disabled (TIMER_FAULT[3:0] = 0b0000), a persistent fault will not be able to start a hard-fault condition. The system designer is responsible for planning the proper fault handling strategy suitable to each specific application.

12.6.3 VAON fault management

12.6.3.1 VAON always-on mode

When the VAON supply is configured as an always-on supply, the fault detection and reaction depends on the state and the fault mode configuration during the SYSTEM ON states.

In the low-power states, a low-power analog undervoltage monitor is implemented to detect when the VAON output has gone below the VAON_LP_UV threshold. The low-power voltage monitor is intended to prevent the system from becoming unresponsive due to a latch-up condition in the VAON domain, and it should not be considered a safety-related block during the safety analysis of the PMIC.

When the VAON output falls below the VAON_LP_UV threshold during the OFF states, the regulator will generate a self-reset cycle, applying an internal pulldown resistor for 600 µs to ensure the output voltage is discharged, in order to ensure the load is able to cross its POR threshold before it proceeds to re-enable the VAON output.

When the state machine reaches the DBGOFF state, the VAON will be monitored for OV and UV to ensure the VAON output is in regulation before the power-up sequence can be started.

During the low-power STANDBY state (OTP_LP_STBY = 1) the VAON reaction to an OV/UV condition is selected via the OTP_VAON_FMODE bit.

When the OTP_VAON_FMODE = 0, the VAON will ignore any OV/UV conditions and no protective reaction will be available.

When the OTP_VAON_FMODE = 1, the low-power undervoltage monitor will be enabled to allow the system to detect the VAON falling below the VAON_LP_UV threshold and generate a full PMIC power-down sequence.

In the low-power STANDBY state, the system may not support I^2C communication, and most of the monitoring circuits are disabled, including the system watchdog timer. A temporary loss of the VAON may result in a non-responsive system. Therefore, when the VAON_LP_UV condition is present, the PF09 will start a full reset condition, including the VAON supply last in the power-down sequence and applying the power-down delay after the VAON Is disabled, in order to allow enough time for all rails to be discharged properly before the system can re-enable the VAON regulator when it reaches the LPOFF state.

During the monitored system-on states (RUN and monitored STANDBY state), the VAON low-power undervoltage monitor is disabled to allow the system to manage safety-related fault conditions via the programable OV/UV monitor on VAON.

The reaction to an OV/UV condition is defined by the OTP_VAON_FMODE bit:

When OTP_VAON_FMODE = 0 the VAON reacts in “notification mode” upon an OV/UV condition.

When OTP_VAON_FMODE = 1 the VAON reacts in “Reset mode” upon an OV/UV.

When the VAON reaction is set to notification mode, the block follows similar protection rules as defined in the fault management for the system regulators:

- OV/UV Interrupt flag is set and the INTB pin asserted if the interrupt is not masked.
- PGOOD is asserted if OV/UV condition is not bypassed and VAON_PG_EN = 1.
- Fault counter is increased if OV/UV condition is not bypassed.
- Global fault timer is started if OV/UV condition is not bypassed.
- The FS0B pin will be asserted as defined by the pin configuration.

If the VAON fault reaction is set to notification mode, the VAON regulator will not be turned off internally when a hard fault is detected and the device starts a power-down sequence.

When the VAON fault reaction is set to RESET mode, an OV/UV fault condition can start the following protective mechanism:

- The OV/UV Interrupt flag is set and the INTB pin asserted if the interrupt is not masked.
- PGOOD is asserted if the OV/UV condition is not bypassed and VAON_PG_EN = 1.
- Fault counter is increased if the OV/UV condition is not bypassed.
- The FS0B pin will be asserted as defined by the pin configuration.

The dedicated VAON fault timer is started if the OV/UV condition is not bypassed, and the PMIC will require the fault to be acknowledged to prevent a total system shutdown.

When the VAON fault reaction is set to RESET mode, a dedicated fault timer is provided to allow the system to acknowledge an OV/UV fault before the VAON fault timer is expired. The MCU must acknowledge the OV/UV fault on the VAON regulator by clearing the corresponding VAON_OV_I or VAON_UV_I interrupt flags.

If the fault condition is still present by the time the VAON_OV_I or VAON_UV_I flags are cleared, the flag will be set again right away and the VAON fault timer is restarted.

The default duration of the VAON fault timer is set via the OTP_VAON_TFLT[2:0] bits and it can be modified during the system-on states via the VAON_TFLT[2:0] bits.

Table 52. VAON fault timer duration

VAON_TFLT [2:0]	VAON fault timer
000	500 us
001	1 ms
010	2 ms
011	5 ms
100	10 ms
101	25 ms
110	50 ms
111	100 ms

In RESET mode, a current limit condition in the VAON regulator will not start the VAON fault timer, however, an UV condition generated due to a current limit protection will be able to start the VAON fault timer and start a full PMIC reset if the condition is not corrected.

If the OV/UV fault is acknowledged before the fault timer is expired, the fault timer is stopped and the system will resume normal operation until a new OV/UV condition is detected.

If the OV/UV fault is not acknowledged before the fault timer expires, the PMIC will generate a hard fault and start a full power-down sequence, including the VAON regulator at the end of the power-down sequence. The power-down delay will be applied after the VAON is disabled, to allow the VAON output to be discharged.

Once the power-down sequence is finished, the device will proceed to the Fail-safe transition and the VAON supply will be re-enabled as soon as the state machine enters the LPOFF state.

When the VAON is operating in Reset mode, the VAON_OV_BYP and the VAON_UV_BYP bits are used to bypass the protective reaction of the OV/UV condition, however the PF09 will still generate the corresponding interrupt event to allow the system to track the fault conditions with a lower priority.

In Reset mode, the following VAON configuration bits have no effect on the fault management strategy for the VAON regulator.

- VAON_FLT_REN
- VAON_OV_STATE
- VAON_UV_STATE

The table below summarizes the fault management strategy for the VAON supply in Always-on node.

Table 53. VAON always-on fault management strategy

State	Fault mode (OTP_VAON_FMODE)	Fault reaction
OFF states	Don't care	An UV condition in the VAON supply crossing the VAON_LP_UV threshold will generate a self-reset of its output.
RUN state and monitored STANDBY	OTP_VAON_FMODE = 0	OV/UV interrupt is generated PGOOD Asserted. Fault counter increased. Global fault timer started.
	OTP_VAON_FMODE = 1	OV/UV Interrupt is generated PGOOD asserted. Fault counter increased. VAON fault timer started. MCU must acknowledge and clear OV/UV flags. If fault condition is cleared, return to normal operation If fault condition is not cleared, hard fault includes VAON.
Low-power STANDBY	OTP_VAON_FMODE = 0	UV/OV conditions are ignored.
	OTP_VAON_FMODE = 1	An UV crossing the VAON_LP_UV threshold will generate a full PMIC power down (including the VAON)

12.6.3.2 VAON as system regulator

When VAON is configured as a system regulator, the OTP_VAON_FMODE bit has no effect on the reaction when an OV/UV fault is detected in the VAON supply.

In order to allow the lowest power consumption during the low-power STANDBY state, the OV/UV monitoring circuits are disabled, therefore the PF09 will not detect any OV/UV condition in the VAON output.

During the SYSTEM ON states (RUN and Monitored STANDBY states), the PF09 will react to an OV/UV following the same rules as defined in in the fault management for system regulators:

- OV/UV interrupt flag is set and INTB pin asserted if the interrupt is not masked.

- PGOOD is asserted if OV/UV condition is not bypassed and VAON_PG_EN = 1.
- Fault counter is increased if OV/UV condition is not bypassed.
- Global fault timer is started if OV/UV condition is not bypassed.
- The VAON output is disabled if the VAON_OV_STATE / VAON_UV_STATE = 0.
- The VAON output will be re-enabled automatically if the VAON_FLT_REN = 1
- The FS0B pin will be asserted as defined by the pin configuration.
- During the hard fault, the VAON will be disabled as indicated by the power-down sequence (VAON_SEQ[7:0] bits).

Table 54. VAON System regulator fault management

State	Fault mode (OTP_VAON_FMODE)	Fault reaction
RUN State and monitored STANDBY	Don’t care	OV/UV interrupt is generated PGOOD asserted. Fault counter increased. Global fault timer started. Hard fault includes VAON (in sequencer).
Low-power STANDBY	Don’t care	No monitoring available.

12.6.4 Fault monitoring during time-based power up

The OTP_PWRUP_CHK bit is provided to select whether the output of the switching regulators is verified during the Power-up sequence. It is used as a gating condition to release or not release the RSTB pin.

Table 55. OTP_PWRUP_CHK bit

OTP_PWRUP_CHK	Power good verification
0	Disabled
1	Enabled

When the OTP_PWRUP_CHK = 0, the output voltage of the regulators is not checked during the Power-up sequence and a power-good indication is not required to release the RSTB pin. All regulators enabled after the RSTB is released will start checking for faults after their corresponding blanking period.

When the OTP_PWRUP_CHK = 1, the output voltage of the regulators is verified during the Power-up sequence and a power-good condition is required to release the RSTB.

When RSTB is ready to be de-asserted, the device will check for any OV/UV condition in the regulators that have been already turned on. If all regulators power up before RSTB is in regulation, the RSTB is released and the Power-up sequence will continue.

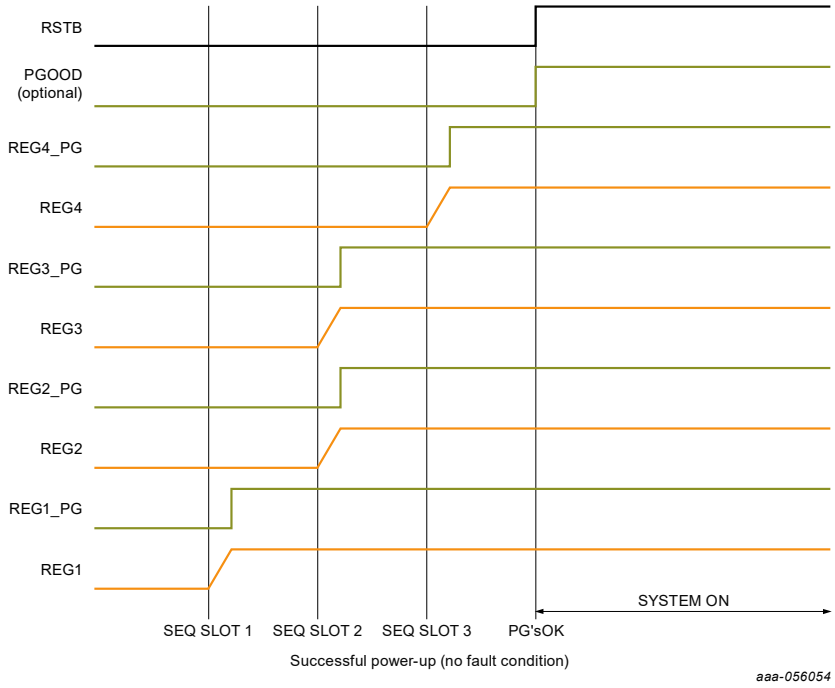


Figure 15. Successful power-up (no fault condition)

If any of the regulators power up before RSTB is out of regulation, the RSTB pin will not be released and the Power-up sequence is stopped for up to 2 ms to allow for all regulators to settle.

If the fault condition is cleared and all regulators are in regulation within the 2 ms timer, the RSTB pin is released and the Power-up sequence will continue where it stopped.

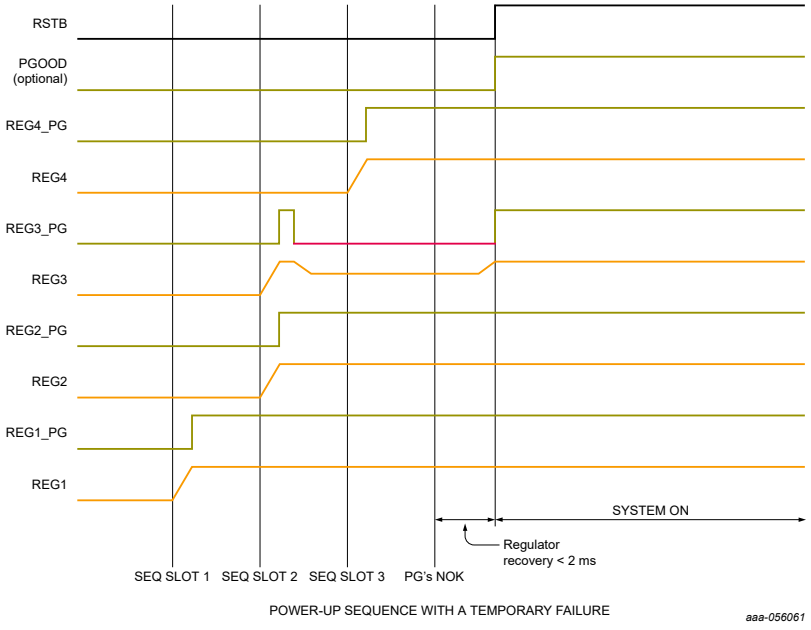


Figure 16. Power-up sequence with temporary failure

If the fault condition is not cleared within the 2 ms timer, the Power-up sequence will be aborted, and the regulators enabled so far will be turned off immediately to proceed to the Fail-safe transition.

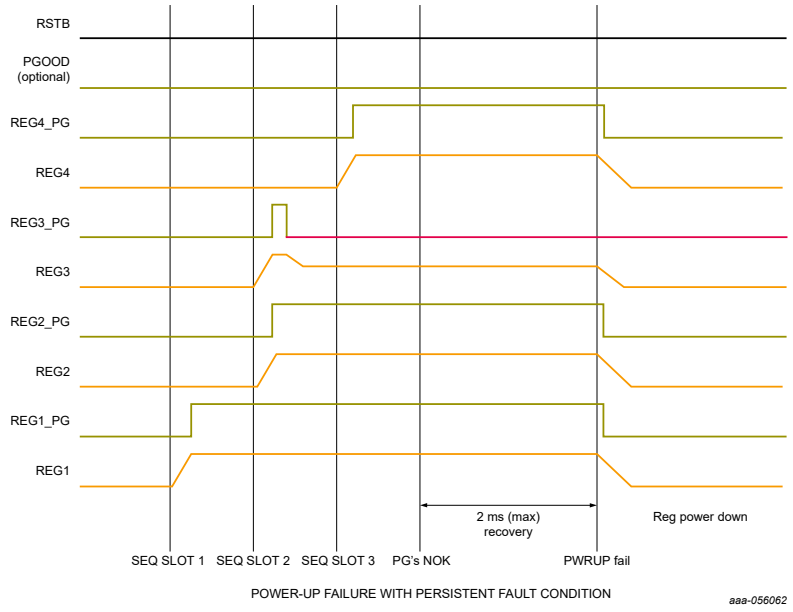


Figure 17. Power-up failure with persistent fault condition

After the RSTB is released, an OV/UV or ILIM condition will trigger a fault detection and protection mechanism as described in section Section 12.6.2.

If a regulator fault occurs after RSTB is released but before the Power-up sequence is finalized, the Power-up sequence will continue to power up if the fault condition is not enough to start a hard fault, based on the fault management rules during the SYSTEM ON states.

During the Power-up sequence, the PGOOD pin will be used as an external indicator of an OV/UV failure when the RSTB is ready to be de-asserted, since the PG_EN bits for all regulators are reset to 1 at power up.

When the OTP_PWRUP_CHK = 1, the RSTB must be set to release at a later slot than any of the voltage regulators needed by the system before going out of the reset condition. This will allow sufficient time for all regulators to reach their corresponding regulation point during the power-up sequence and avoid false fault conditions due to the regulators ramping up too slowly.

When the RSTB pin is intended to be released before all of the switching and LDO regulators, the OTP_PWRUP_CHK bit should always be set to 0, to prevent the system from generating a power-up failure event.

When OTP_PWRUP_CHK = 1, if any IO is used as a GPOx, it may be released at any time in the Power-up sequence, as long as the RSTB does not try to release before there is an actual regulator enabled to check for a power good condition (system-level configuration).

12.6.5 Fault monitoring during dynamic power up

When operating in dynamic power-up, the PF09 will start monitoring for OV and UV conditions as soon as the regulator is enabled. If an OV/UV condition is detected while the Power-up sequence is in progress, such condition will be used as a gating factor to prevent the regulator on the next hierarchical level from turning on until all regulators enabled previously are in regulation.

When regulators in the next hierarchical level are enabled, the settling timer is restarted to allow the new regulators to ramp up and reach regulation.

If any of the regulators enabled in the current or previous hierarchical level fall out of regulation and the settling timer is expired, the Power-down sequence will be stopped and it will proceed to power down all regulators immediately.

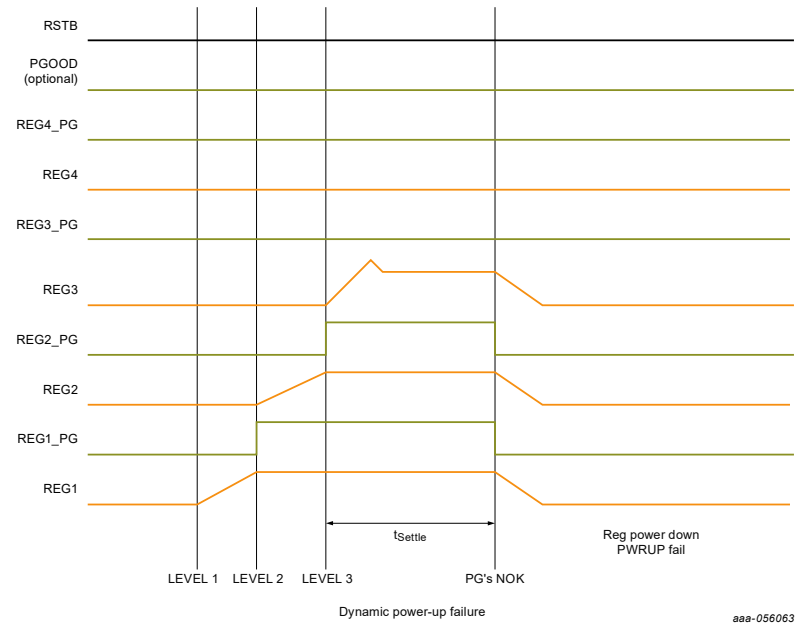


Figure 18. Dynamic power-up failure

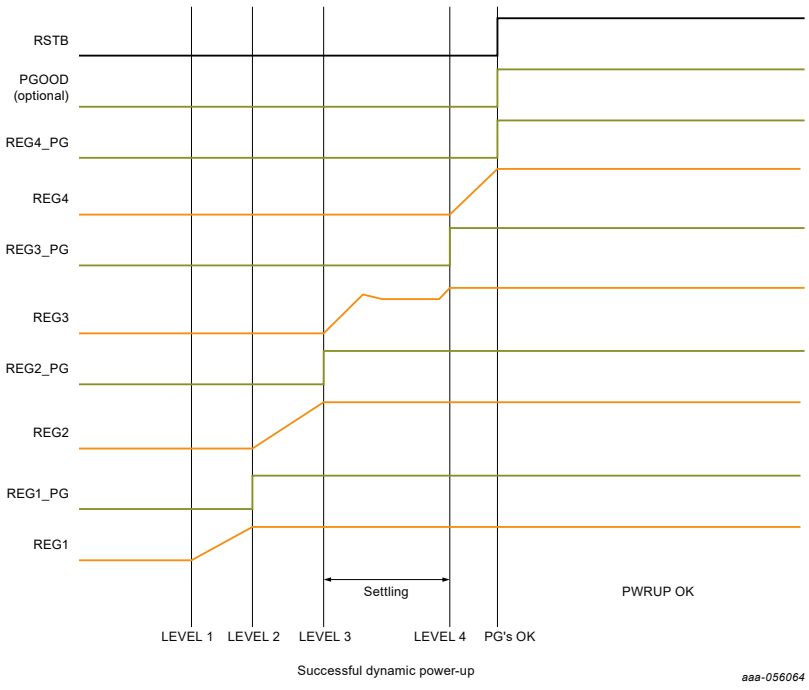


Figure 19. Successful dynamic power-up

12.7 System diagnostics

12.7.1 System fault flags

The PF09 provides dedicated flags to improve the system diagnostics when fault, reset or turn-off conditions have been detected.

System diagnostic flags can be cleared manually by writing a 1 to the corresponding bit, and the values of the flags will remain unchanged as long as the digital supply (VDIG) does not cross the internal POR threshold. The following scenarios will cause a loss of the internal VDIG, hence a loss of the system fault flag:

- VIN goes below the VIN_POR threshold
- The device is in the ULPOFF state.
- VDIG supply is shorted externally (fault condition)

Table 56 provides a summary of the system diagnostic faults available in the PF09 devices.

Table 56. System diagnostic flags

Diagnostic flag	Description
DCRC_FLG	Flag is set when a dynamic CRC error is present
DFS_FLG	Flag is set when device is waking up from the DFS state
VIN_OV_FLG	Flag is set when a VIN_OV condition is present
XFAIL_FLG	Flag is set when a power-down event was initiated via the XFAILB pin.
WD_FLG	Flag is set when a watchdog reset event is initiated.
XRESET_FLG	Flag is set when an external reset is requested via the XRESET or FCCU blocks
SFAULT_FLG	Flag is set when a soft fault is present (OV/UV/ILIM)
HFAULT_FLG	Flag is set when a hard fault is present.

The hard-fault event has dedicated flags to trace the source of failure.

Table 57. Hard-fault Flags

Hard-fault Flag	Description
UVDET_FAIL	This flag is set automatically when the device crosses the UVDET threshold in the rising edge, to indicate the device is waking up from the DFS state after a VIN < UVDET condition.
RSTB_FAIL	The RSTB is externally held low for longer than the OTP_RSTB_TSHORT[1:0]
PU_FAIL	A power-up failure started the hard fault.
RESET_FAIL	The Reset counter reaches the maximum number of events allowed. (RESET_CNT[3:0] = RESET_MAX[3:0])
FLTCNT_FAIL	The Fault counter reaches the maximum number of failures allowed. (FAULT_CNT[3:0] = FAULT_MAX_CNT)
REG_FAIL	A fault condition in a regulator causes a hard fault. (Fault timer, VAON UV not acknowledged)
TSD_FAIL	A power-down sequence is initiated due to a thermal shutdown event.

The MCU is able to read the fault flags during the system-on states in order to obtain information about the previous failure, provided the state machine is able to power up successfully after such a failure.

12.7.2 Interrupt management

The MCU can be notified of any interrupt event through the INTB pin and the various interrupt registers provided by the PF09. The INTB pin is a reflection of a logic OR of all the interrupt status bits allowed to control the pin.

Interrupts are reported in two levels on the interrupts registers: At first level, the SYSTEM_INT register provides information about the interrupt register that originated the interrupt event. At the second level, the remaining interrupt registers provide the exact source for the interrupt event.

The corresponding SYSTEM_INT bits are set when the INTB pin is asserted by any of the second-level interrupt bits that have not been masked. Likewise, when the second-level interrupt bit is cleared, the corresponding first-level interrupt bit on the SYSTEM_INT register is cleared automatically.

Table 58. System interrupt flags

System interrupt flag	Source of interrupt
STATUS1_I	Bit is set when interrupt is generated in register: • STATUS1_INT
STATUS2_I	Bit is set when interrupt is generated in registers: • STATUS2_INT • STATUS3_INT
MODE_I	Bit is set when interrupt is generated in register: • SW_MODE_INT
ILIM_I	Bit is set when interrupt is generated in registers: • SW_ILIM_INT • LDO_ILIM_INT
UV_I	Bit is set when interrupt is generated in registers: • SW_UV_INT • LDO_UV_INT
OV_I	Bit is set when interrupt is generated in registers: • SW_OV_INT • LDO_OV_INT
GPIO_I	Bit is set when interrupt is generated in registers: • PWRON_INT • IO_INT
EWARN_I	The EWARN_I is the only interrupt bit in the system without a mask bit, and it will cause the INTB pin to assert every time a critical fault is causing the device to shut down.

Whenever an interrupt event occurs, the corresponding interrupt latch bit (_I) will be set, and the system must write a 1 to the corresponding status bit to clear the interrupt.

Each second-level interrupt is provided with a mask bit to control whether a given interrupt latch bit can assert the INTB pin low or not. Only the PWRUP_I interrupt is not masked by default, in order to allow the INTB pin to assert when the power-up sequence is finished.

Faults or conditions with a steady state are provided with a sense bit xxx_S to read the current status of such conditions. Interrupts generated by transient faults or events do not provide sense bits.

Table 59. Interrupt latch, interrupt mask, and sense bits

Bit value	Interrupt latch [_I]	Interrupt mask [_M]	Sense bit [_S]
0	No event present	Asserts INTB (not-masked)	Condition is not present
1	Event latched	Does not assert INTB (masked)	Condition is currently present

Table 60. Interrupt register set

Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SYSTEM INT	EWARN_I	GPIO_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
STATUS1 INT	SDWN_I	FREQ_RDY_I	DCRC_I	I2C_CRC_I	PWRUP_I	PWRDN_I	FSYNC_FLT_I	VIN_OV_I
STATUS1 MSK	SDWN_M	FREQ_RDY_M	DCRC_M	I2C_CRC_M	PWRUP_M	PWRDN_M	FSYNC_FLT_M	VIN_OV_M
STATUS1 SNS	–	–	–	–	–	–	FSYNC_FLT_S	VIN_OV_S
STATUS2 INT	VANA_OV_I	VDIG_OV_I	BGMON_I	CLKMON_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
STATUS2 MSK	VANA_OV_M	VDIG_OV_M	BGMON_M	CLKMON_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M
STATUS2 SNS	VANA_OV_S	VDIG_OV_S	BGMON_S	CLKMON_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
STATUS3 INT	–	–	LDO1EN_I	VSELECT_I	WD_ERROR_I	BAD_CMD_I	LBIST_DONE_I	SHS_I
STATUS3 MSK	–	–	LDO1EN_M	VSELECT_M	WD_ERROR_M	BAD_CMD_M	LBIST_DONE_M	SHS_M
SW MODE INT	DVSMAX_I	DVSMIN_I	-	SW5_MODE_I	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
SW MODE MSK	DVSMAX_M	DVSMIN_M	-	SW5_MODE_M	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
SW ILIM INT	SW1LS_OCP_I	–	–	SW5_IL_I	SW4_IL_I	SW3_IL_I	SW2_IL_I	SW1_IL_I
SW ILIM MSK	SW1LS_OCP_M	–	–	SW5_IL_M	SW4_IL_M	SW3_IL_M	SW2_IL_M	SW1_IL_M
SW ILIM SNS	–	–	–	SW5_IL_S	SW4_IL_S	SW3_IL_S	SW2_IL_S	SW1_IL_S
LDO ILIM INT	–	–	–	–	–	LDO3_IL_I	LDO2_IL_I	LDO1_IL_I
LDO ILIM MSK	–	–	–	–	–	LDO3_IL_M	LDO2_IL_M	LDO1_IL_M
LDO ILIM SNS	–	–	–	–	–	LDO3_IL_S	LDO2_IL_S	LDO1_IL_S
SW UV INT	MON2_UV_I	MON1_UV_I	–	SW5_UV_I	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
SW UV MSK	MON2_UV_M	MON1_UV_M	–	SW5_UV_M	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
SW UV SNS	MON2_UV_S	MON1_UV_S	–	SW5_UV_S	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
SW OV INT	MON2_OV_I	MON1_OV_I	–	SW5_OV_I	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
SW OV MSK	MON2_OV_M	MON1_OV_M	–	SW5_OV_M	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M
SW OV SNS	MON2_OV_S	MON1_OV_S	–	SW5_OV_S	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
LDO UV INT	–	–	–	–	VAON_UV_I	LDO3_UV_I	LDO2_UV_I	LDO1_UV_I
LDO UV MSK	–	–	–	–	VAON_UV_M	LDO3_UV_M	LDO2_UV_M	LDO1_UV_M
LDO UV SNS	–	–	–	–	VAON_UV_S	LDO3_UV_S	LDO2_UV_S	LDO1_UV_S
LDO OV INT	–	–	–	–	VAON_OV_I	LDO3_OV_I	LDO2_OV_I	LDO1_OV_I
LDO OV MSK	–	–	–	–	VAON_OV_M	LDO3_OV_M	LDO2_OV_M	LDO1_OV_M
LDO OV SNS	–	–	–	–	VAON_OV_S	LDO3_OV_S	LDO2_OV_S	LDO1_OV_S
PWRON INT	–	–	–	PWRON_8S_I	PWRON_4S_I	PWRON_3S_I	PWRON_2S_I	PWRON_1S_I
PWRON MSK	–	–	–	PWRON_8S_M	PWRON_4S_M	PWRON_3S_M	PWRON_2S_M	PWRON_1S_M
IO INT	–	–	ERRMON_I	FCCU1_I	FCCU0_I	PGOOD_FLT_I	FS0B_FLT_I	RSTB_FLT_I
IO MSK	–	–	ERRMON_M	FCCU1_M	FCCU0_M	PGOOD_FLT_M	FS0B_FLT_M	RSTB_FLT_M
IO SNS	–	GPIO4_S	GPIO3_S	FCCU1_S	FCCU0_S	PGOOD_S	FS0B_S	RSTB_S
SHORT SNS	GPIO2_S	GPIO1_S	FS0B_S2H	FS0B_S2L	PGOOD_S2H	PGOOD_S2L	RSTB_S2H	RSTB_S2L

I/O pins are provided with a sense bit to allow the system to monitor the real-time status of the pin. An I/O sense bit equal to 0 means the pin is physically sensed low, and a sense bit equal to 1 means the pin is physically sensed high.

Table 61. I/O pin sense bits

I/O pin	Sense bit
RSTB	RSTB_S
FS0B	FS0B_S
PGOOD	PGOOD_S
GPIO1	GPIO1_S
GPIO2	GPIO2_S
GPIO3	GPIO3_S

Table 61. I/O pin sense bits*...continued*

I/O pin	Sense bit
GPIO4	GPIO4_S
FCCU0	FCCU0_S
FCCU1	FCCU1_S

12.7.3 System test commands

The SYS_CMD[7:0] bit field is provided to request various system tests or commands.

Table 62. SYS_CMD[7:0] bit field

SYS_CMD[7:0]	System command
0xA5	Software turn-off request
0x3E	Software reset request
0x55	ABIST on demand request
0x4A	LBIST on demand request
0x9C	RSTB pulse request
0x75	INTB pulse request
0xB3	XRESET to FCCU request
0xBA	FCCU to XRESET request
0x2C	STANDBY request
All other codes[1]	Invalid command

[1] An Invalid command in the SYS_CMD[7:0] bits will be ignored, and the BAD_CMD_I interrupt will be generated. The BAD_CMD_I interrupt will assert the INTB pin if the interrupt is not masked.

12.8 I/O interface pins

The PF09 PMIC is fully programmable via the I^2C interface, however additional interfacing between MCU, PF09, and other companion PMICs is provided by direct logic interfacing pins.

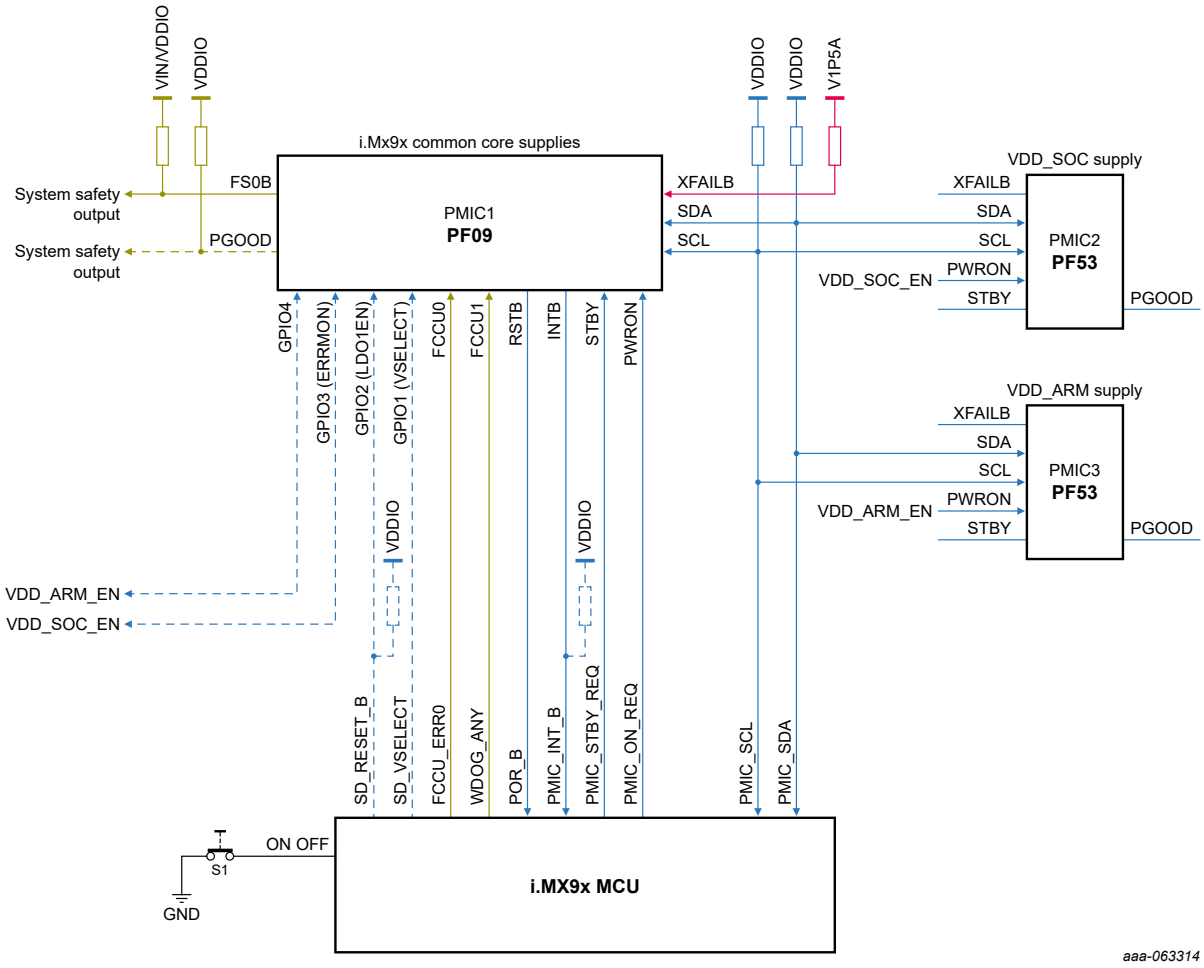


Figure 20. PF09 System interface IO signals

12.8.1 Interfacing I/O electrical characteristics

Table 63. Electrical characteristics

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	PWRON				
$V_{IN\_MAX\_PWRON}$	Maximum input voltage	–	–	5.5	V
V_{IH_PWRON}	PWRON input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_PWRON}	PWRON input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_PWRON}	PWRON input buffer hysteresis	60	–	–	mV
R_{PD_PWRON}	PWRON internal pulldown	–	10	25	MΩ
	STBY				
$V_{IN\_MAX\_STBY}$	Maximum input voltage	–	–	5.5	V

Table 63. Electrical characteristics*...continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{IH_STBY}	STBY input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_STBY}	STBY input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_STBY}	STBY input buffer hysteresis	100	–	–	mV
FCCU1 (XRESET Mode)					
$V_{IN\_MAX\_XRESET}$	Maximum input voltage	–	–	5.5	V
VIH_XRESET	XRESET input high voltage • Minimum voltage to ensure a high state	$0.7*V_{DDIO}$	–	–	V
V_{IL_XRESET}	XRESET input low voltage • Maximum voltage to ensure a low state	–	–	$0.3*V_{DDIO}$	V
I_{HYS_XRESET}	XRESET input buffer hysteresis	100	–	–	mV
R_{PD_XRESET}	XRESET internal pull-down	400	800	1300	kΩ
INTB					
V_{OL_INTB}	INTB output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_INTB}	INTB output low current	–	–	10	mA
t_{INTB_PULSE}	INTB test pulse	90	100	110	µs
$V_{IN\_MAX\_RSTB}$	Maximum input voltage	–	–	5.5	V
RSTB					
V_{IH_RSTB}	RSTB input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_RSTB}	RSTB input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_RSTB}	RSTB input buffer hysteresis	100	–	–	mV
$V_{OH\_RSTB\_VDDIO}$	RSTB output high voltage • OTP_RSTB_MODE [1:0] = 01.	V_{DDIO} – 0.5	–	–	V
$V_{OH\_RSTB\_VAON}$	RSTB output high voltage • OTP_RSTB_MODE [1:0] = 10	V_{AON} – 0.5	–	–	V
V_{OL_RSTB}	RSTB output low voltage • Maximum voltage at 10mA load	–	–	0.4	V
I_{OL_RSTB}	RSTB output low current	–	–	10	mA
I_{OH_RSTB}	RSTB output high current • OTP_RSTB_MODE = 01 or 10	–	–	2	mA
t_{RSTB_PULSE}	RSTB pulse duration	90	100	110	µs
PGOOD					
$V_{IN\_MAX\_PGOOD}$	Maximum input voltage	–	–	5.5	V

Table 63. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{IH_PGOOD}	PGOOD input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_PGOOD}	PGOOD input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_PGOOD}	PGOOD input buffer hysteresis	100	–	–	mV
V_{OL_PGOOD}	PGOOD output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_PGOOD}	PGOOD output low current	–	–	10	mA
GPIO1					
$V_{IN\_MAX\_GPIO1}$	Maximum input voltage	–	–	5.5	V
V_{IH_GPIO1}	GPIO1 input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_GPIO1}	GPIO1 input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_GPIO1}	GPIO1 input buffer hysteresis	100	–	–	mV
V_{OL_GPIO1}	GPIO1 output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_GPIO1}	GPIO1 output low current	–	–	10	mA
$V_{OH\_GPIO1\_VIN}$	GPIO1 output high voltage • OTP_GPIO1_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	–	–	V
I_{OH_GPIO1}	GPIO1 output high current	–	–	2	mA
R_{PD_GPIO1}	GPIO1 internal pull-down • In VESELECT mode	1	2	4	MΩ
GPIO2					
$V_{IN\_MAX\_GPIO2}$	Maximum input voltage	–	–	5.5	V
V_{IH_GPIO2}	GPIO2 input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_GPIO2}	GPIO2 input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_GPIO2}	GPIO2 input buffer hysteresis	100	–	–	mV
V_{OL_GPIO2}	GPIO2 output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_GPIO2}	GPIO2 output low current	–	–	10	mA
$V_{OH\_GPIO2\_VIN}$	GPIO2 output high voltage • OTP_GPIO2_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	–	–	V
I_{OH_GPIO2}	GPIO2 output high current	–	–	2	mA

Table 63. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
R_{PD_GPIO2}	GPIO2 internal pulldown • In LDO1EN mode	1	2	4	MΩ
	GPIO3				
$V_{IN\_MAX\_GPIO3}$	Maximum input voltage	–	–	5.5	V
V_{IH_GPIO3}	GPIO3 input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_GPIO3}	GPIO3 input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_GPIO3}	GPIO3 input buffer hysteresis	100	–	–	mV
V_{OL_GPIO3}	GPIO3 output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_GPIO3}	GPIO3 output low current	–	–	10	mA
$V_{OH\_GPIO3\_VIN}$	GPIO3 output high voltage • OTP_GPIO3_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	–	–	V
I_{OH_GPIO3}	GPIO3 output high current	–	–	2	mA
	GPIO4				
$V_{IN\_MAX\_GPIO4}$	Maximum input voltage	–	–	5.5	V
V_{IH_GPIO4}	GPIO4 input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_GPIO4}	GPIO4 input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_GPIO4}	GPIO4 input buffer hysteresis	100	–	–	mV
V_{OL_GPIO4}	GPIO4 output low voltage • Maximum voltage at 10mA load	–	–	0.4	V
I_{OL_GPIO4}	GPIO4 output low current	–	–	10	mA
$V_{OH\_GPIO4\_VIN}$	GPIO4 output high voltage • OTP_GPIO4_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	–	–	V
	FS0B				
$V_{IN\_MAX\_FS0B}$	Maximum input voltage	–	–	5.5	V
V_{IH_FS0B}	FS0B input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_FS0B}	FS0B input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_FS0B}	FS0B input buffer hysteresis	100	–	–	mV
V_{OL_FS0B}	FS0B output low voltage • Maximum voltage at 10mA load	–	–	0.4	V

Table 63. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
I_{OL_FS0B}	FS0B output low current	–	–	10	mA
	XFAILB				
$V_{IN\_MAX\_XFAILB}$	Maximum input voltage	–	–	5.5	V
V_{IH_XFAILB}	XFAILB input high voltage • Minimum voltage to ensure a high state	1.4	–	–	V
V_{IL_XFAILB}	XFAILB input low voltage • Maximum voltage to ensure a low state	–	–	0.4	V
I_{HYS_XFAILB}	XFAILB input buffer hysteresis	100	–	–	mV
V_{OL_XFAILB}	XFAILB output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_XFAILB}	XFAILB output low current	–	–	10	mA
R_{XPU_XFAILB}	XFAILB external pullup • Pullup to VANA	–	10	–	kΩ
C_{XFAILB}	XFAIL recommended decoupling EMC capacitance	–	100	–	nF
	I^2C interface				
V_{OL_SDA}	SDA output low voltage • Maximum voltage at 20 mA load	–	–	0.4	V
V_{IH_SDA}	SDA input high voltage • Minimum voltage to ensure a high state	$0.7*V_{DDIO}$	–	–	V
V_{IL_SDA}	SDA input low voltage • Maximum voltage to ensure a low state	–	–	$0.3*V_{DDIO}$	V
V_{IH_SCL}	SCL input high voltage • Minimum voltage to ensure a high state	$0.7*V_{DDIO}$	–	–	V
V_{IL_SCL}	SCL input low voltage • Maximum voltage to ensure a low state	–	–	$0.3*V_{DDIO}$	V
F_{I2C_FMP}	I^2C operating frequency • Fast-mode plus	–	–	1	MHz
F_{I2C_HS}	I^2C operating frequency • High speed	–	–	3.4	MHz
$R_{XPU\_SCL\_FMP}$	SCL external pullup Fast mode plus • Pullup to VDDIO • I^2C Fast mode	–	2.2	–	kΩ
$R_{XPU\_SDA\_FMP}$	SDA external pullup Fast mode plus • Pullup to VDDIO • I^2C Fast mode	–	2.2	–	kΩ

Table 63. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
$R_{XPU\_SCL\_HS}$	SCL external pullup high speed • Pullup to VDDIO • I^2C high speed	–	0.8	–	kΩ
$R_{XPU\_SDA\_HS}$	SDA external pullup high speed • Pullup to VDDIO • I^2C high speed	–	0.8	–	kΩ

12.8.2 PWRON

The PWRON is an input signal to the PF09 that acts as a power-up event signal for the device. It provides two modes of operations as programmed by the OTP_PWRON_MODE bit.

Table 64. PWRON operation mode

OTP_PWRON_MODE	PWRON operation mode
0	Level Sensitive
1	Edge Sensitive

Refer to Section 12.3 for details on power-up requirements.

12.8.2.1 Level-sensitive mode

When the PWRON is programmed in In level-sensitive mode, the PWRON pin is used to command the PMICs to generate a power on/off event by controlling the pin high or low, respectively.

When the PWRON pin is asserted low, the device is forced into the corresponding off state, and pulling the PWRON pin high will generate a power-on event.

PWRON may be pulled up to VIN with an external pullup resistor, if the device is intended to come up automatically when the main power is applied.

12.8.2.2 Edge-sensitive mode

When the PWRON is programmed in edge-sensitive mode, PWRON may be pulled up to VIN through a 470 kΩ resistor connected to a pushbutton or a controlled signal to generate a Falling-edge pulse on the PWRON pin.

In this mode, the PWRON pin is expected to be pulled up to VIN all the time, hence the system must make a tradeoff between having an ultra-low quiescent current in the OFF state and the ability to operate in edge transition.

In edge sensitive mode, a Falling edge on the PWRON pin is used to generate a power-up event when the device is in the LPOFF state.

During the system-on states, the PWRON pin is used to request a turnoff event by generating a new falling-edge transition and holding the PWRON pin low for as long as the selected time to reset (TRESET).

Table 65. Time to reset

TRESET[1:0]	Time to reset
00	100 µs

Table 65. Time to reset*...continued*

TRESET[1:0]	Time to reset
01	2 sec
10	8 sec
11	16 sec

In the edge-sensitive mode, The PF09 uses the PWRON_DBNC[1:0] bits to set the PWRON pin debounce on the rising and Falling edges.

Table 66. PWRON pin debounce

PWRON_DBNC[1:0]	Falling-edge debounce	Rising-edge debounce
00	32 ms	32 ms
01	32 ms	32 ms
10	125 ms	32 ms
11	750 ms	32 ms

The OTP_PWRON_DBNC[1:0] bits are used to set the default debounce time for the PWRON pin upon a power up.

The PWRON_1S_I, PWRON_2S_I, PWRON_3S_I, PWRON_4S_I and PWRON_8S_I interrupts are generated when the PWRON pin is held low for longer than 1 s, 2 s, 3 s, 4 s and 8 s respectively.

If PWRON_RST_EN = 1, pressing the PWRON for longer than the delay programmed by OTP_TRESET[1:0] will force a PMIC reset.

If PWRON_RST_EN = 0, the device will start a turnoff event after the pushbutton is pressed for longer than TRESET[1:0].

12.8.3 STBY

When the STBY pin is asserted, the device is directed to enter the STANDBY state, and when de-asserted, it will return to the RUN state.

The STBY pin is programmable as active-high or active-low using the STBY_POL bit.

Table 67. STBY pin polarity

STBY (pin)	STBY_POL	STANDBY control
0	0	Not in STANDBY mode
0	1	In STANDBY mode
1	0	In STANDBY mode
1	1	Not in STANDBY mode

The OTP_STBY_POL bit is provided to set the default value of the STBY_POL bit.

The PF09 features a selectable STANDBY request window to allow the system to safely move into the STANDBY state when the STBY pin is toggled, and to prevent random access to the STANDBY state.

To exit the STANDBY state, the device requires only the STBY pin toggle in the corresponding state, without the need for any STANDBY request command.

The OTP_STBY_REQ bit is provided to configure the operation of the STANDBY request window.

Table 68. STANDBY request window

OTP_STBY_REQ	STANDBY request window
0	Always open
1	Open on request

When the STANDBY request window is set to “always open”, the device can transition in and out of the STANDBY states at any time by toggling the STBY pin, as defined by the STBY_POL polarity bit.

When the STANDBY request window is set to “open on request”, the PF09 requires a STANDBY request command to open the request window. To start a STANDBY request, the MCU must send the SYS_CMD = 0x2C via I^2C communication, and it must assert the STBY pin within 20 ms while the STANDBY request window is open.

When the STANDBY request window is set to "open on request", the system can also start a STANDBY request via software by fixing the STBY pin to a specific voltage, sending the STANDBY request and then changing the STBY_POL bit via I^2C communication within the open window (20 ms).

If the STBY pin does not get a valid voltage within the STANDBY request window (20 ms), the PF09 will close the window and send a BAD_CMD_I interrupt to notify the system that the STANDBY request was not fulfilled.

12.8.4 INTB

The INTB pin is an open-drain, active-low output used to notify the MCU when a specific event is present on the PMIC. In the application, INTB is typically pulled up to VDDIO with an external 100 kΩ resistor.

The INTB pin behaves as an OR result of all unmasked interrupt signals asserted in the interrupt registers. It will assert (i.e., be pulled low) when any of the interrupt events occur and the corresponding event is unmasked, and it can be de-asserted only after each unmasked interrupt has been cleared by writing a “1” to the interrupt bit.

The PF09 provides a system-level mechanism to request an interrupt pulse on demand, to test the ability of the INTB pin to toggle high and low at any time during the system operation. When the interrupt pulse is requested, the INTB pin will assert for 100 µs and then de-assert to its normal state.

When requesting an interrupt pulse, the system must first clear all the interrupts to ensure the INTB pin is properly released, and then proceed to request the interrupt pulse by writing the SYS_CMD = 0x75. The MCU can then monitor whether the pin is able to toggle high and low as expected.

Refer to Section 12.7.2 for detailed information about the events reported through the INTB pin.

12.8.5 RSTB

The RSTB pin is a programmable open-drain or push-pull, active-low output that is used to bring the processor (and peripherals) into and out of RESET.

The OTP_RSTB_MODE[1:0] bit is provided to select the type of buffer used on the RSTB pin.

Table 69. RSTB buffer type

OTP_RSTB_MODE[1:0]	RSTB buffer type
00	Open drain
01	Push-pull to VDDIO
10	Push-pull to VAON
11	Open drain

When operating as a push-pull driver, the RSTB output-high voltage can be set internally to VDDIO or VAON via the OTP_RSTB_MODE[1:0] bits.

When RSTB is configured as an open-drain output, the RSTB can be pulled up to VDDIO or VAON by a 10 kΩ to 100 kΩ external resistor.

When the device is out of the SYSTEM ON states, the RSTB pin is driven low to keep the system in the RESET condition until a Power-up sequence is generated successfully.

During the Power-up sequence, the RSTB is de-asserted in the time slot programmed by the RSTB_SEQ[7:0] bits. The RSTB pin being released (pulled high) in the Power-up sequence is interpreted as the start of the system-on state.

When a system power-down or hard reset event is initiated, the RSTB pin is asserted low, as indicated in the power-down sequence.

12.8.5.1 RSTB pin diagnostic

Upon entering the system-on states, the RSTB is provided with a programmable short-detection timer to set the maximum acceptable time before a short in the RSTB pin is considered a fault condition.

Table 70. RSTB short-detection timer

OTP_RSTB_TSHORT[1:0]	Short detection timer
00	Hard fault disabled
01	500 µs
10	1000 ms
11	8000 ms

When a RSTB short condition is detected, the device will generate a hard-fault condition and start a power-down sequence.

When the hard fault is disabled, a short condition will not generate a hard fault event, but the condition will still be reported to the MCU via the RSTB_FLT_I.

During the system-on states, the short-detection timer is intended to be used in two ways based on the system needs:

When the PMIC is operating stand-alone, or no other devices are able to control the RSTB bus, the short-detection timer is used to ensure the RSTB pin state is indeed high.

When PMIC is operating in multi-device systems, where more than one device is able to control the RSTB bus, the short-detection timer is used to detect when another device has asserted the RSTB bus low, and starts counting before it can consider such event as a fault condition.

The RSTB_S flag is provided to read the real-time state of the RSTB pin.

Table 71. State of RSTB pin

RSTB_S	RSTB state
0	Low
1	High

The RSTB_FLT_I interrupt is provided to notify that a short-to-high or short-to-low condition has been present on the RSTB pin. If the RSTB_FLT_I interrupt is unmasked, the INTB pin will be driven low.

The RSTB_FLT_I bit can be cleared by writing a 1 to it.

The RSTB_S2H flag is provided to sense a real time short-to-high condition in the RSTB pin. When the RSTB pin is being driven low internally, and the RSTB_S is sensing a high state, the RSTB_S2H flag is set HIGH until this condition is removed.

The RSTB_S2L flag is provided to sense a real-time short-to-low condition in the RSTB pin. When the RSTB pin is released high internally, and the RSTB_S is sensing a low state, the RSTB_S2L flag is set HIGH until condition is removed.

The system can request a self-reset pulse via the SYS_CMD bits. When SYS_CMD = 0x9C, the RSTB pin will assert for 100 µs and then de-assert to its normal state.

When the RSTB pin is directed to assert by the MCU, the PF09 will monitor the pin during the 100 µs assertion time to ensure the pin is able to go low. If the pin is not able to go low, the device detects a short-to high-event and asserts the RSTB_FLT_I flag.

12.8.6 PGOOD

PGOOD is a dedicated open-drain output used as a *power good* (PG) indicator. In the application, PGOOD can be pulled up to VDDIO (1.8 V or 3.3 V) with a 10 kΩ to 100 kΩ external resistor.

The PF09 implements an individual power good monitor for every regulator and voltage monitor available in the device. Each PG monitor reports its status via I^2C registers.

The status of the PGOOD pin is a logic AND function of the internal PG signals of the selected voltage monitors. The selection of the regulators being reported by the PGOOD pin is done via the PG_EN bits.

Table 72. Voltage reels PGOOD triggers

PG_EN bits	Option	PGOOD Control
SW1_PG_EN	0	SW1 does not control PGOOD
	1	SW1 controls PGOOD
SW2_PG_EN	0	SW2 does not control PGOOD
	1	SW2 controls PGOOD
SW3_PG_EN	0	SW3 does not control PGOOD
	1	SW3 controls PGOOD
SW4_PG_EN	0	SW4 does not control PGOOD
	1	SW4 controls PGOOD
SW5_PG_EN	0	SW5 does not control PGOOD
	1	SW5 controls PGOOD
LDO1_PG_EN	0	LDO1 does not control PGOOD
	1	LDO1 controls PGOOD
LDO2_PG_EN	0	LDO2 does not control PGOOD
	1	LDO2 controls PGOOD
LDO3_PG_EN	0	LDO3 does not control PGOOD
	1	LDO3 controls PGOOD
VAON_PG_EN	0	VAON does not control PGOOD
	1	VAON controls PGOOD

Table 72. Voltage reels PGOOD triggers*...continued*

PG_EN bits	Option	PGOOD Control
VMON1_PG_EN	0	VMON1 does not control PGOOD
	1	VMON1 controls PGOOD
VMON2_PG_EN	0	VMON2 does not control PGOOD
	1	VMON2 controls PGOOD

The PGOOD pin is released high when the all of the voltage monitors selected to control the PGOOD pins are in regulation (within the UV/OV range), and it will be asserted low when any of such regulators goes above or below the programmed OV/UV thresholds.

In order to ensure the system is still capturing OV/UV fault conditions even when the PGOOD pin is not assigned to report a specific condition, all regulators will report the corresponding status and fault events via the interrupt bits, regardless of the configuration of the PG_EN bits. For more details on interrupt management, refer to section 16.7.2 Interrupt Management.

The PGOOD pin will report the power good status of all regulators that have been enabled during the RUN or the monitored STANDBY (OTP_LP_STBY = 0) states, and the pin will be asserted low if there are no regulators or VMON blocks enabled in the system.

When the PF09 is operating in the low-power STANDBY state (OTP_LP_STBY = 1), all voltage monitors are disabled to ensure the lowest quiescent current possible. In this scenario, the PGOOD pin will remain released as long as there are one or more regulators/VMONs enabled in the system.

During the Power-up sequence, the PGOOD pin is held low. It will be released high only after the RSTB pin is released in the Power up sequence to allow the system to receive the power good status as soon as the system is brought out of reset. Refer to section 16.6.4 Fault Monitoring during Time Based Power-up for details on the power good monitoring during the Power-up sequence.

12.8.6.1 PGOOD pin diagnostic

The PGOOD_S flag is provided to read the real-time state of the PGOOD pin.

Table 73. PGOOD_S flag

PGOOD_S	PGOOD state
0	LOW
1	HIGH

The PGOOD_FLT_I interrupt is provided to notify a short-to-high or short-to-low condition has been present on the PGOOD pin. If a fault condition is present on the PGOOD pin, and the PGOOD_FLT_I interrupt is unmasked, the INTB pin will be asserted low. The PGOOD_FLT_I can be cleared by writing a 1 to it.

The PGOOD_S2H flag is provided to sense a real time short-to-high condition in the PGOOD pin. When the PGOOD pin is being driven low internally, and the PGOOD_S is sensing a high state, the PGOOD_S2H flag will be set HIGHuntil the condition is cleared.

The PGOOD_S2L flag is provided to sense a real time short-to-low condition in the PGOOD pin. When the PGOOD pin is released high internally, and the PGOOD_S is sensing a low state, the PGOOD_S2L flag will be set HIGH until the condition is cleared.

12.8.7 FS0B

The FS0B pin is an active-low, open-drain safety output. The FS0B pin can be pulled up to VDDIO or VIN externally with a 10 kΩ to 470 kΩ resistor, based on the system requirements.

The operation of the FS0B pin depends on the safety integrity level of the device.

In non-safety devices (QM), the FS0B pin operates in Fault status mode.

In automotive safety devices (ASIL B/C/D), the FS0B pin operates in Active Safe-state mode.

In industrial safety devices (SIL 2) the FS0B pin operates in Active Safe-state mode.

Detailed description of the Active Safe-state mode is provided in section 18.5 FS0B Active Safe State Mode.

12.8.7.1 Fault status mode

In Fault status mode, the FS0B pin can be programmed to assert when a specific fault event is present. The FS0B fault control bits are provided to allow the FS0B pin to assert when either of the selected fault conditions is present.

When an FS0B fault control bit is set to 0, the fault event will assert the corresponding fault flag, but it will not be able to control the FS0B pin.

When an FS0B fault control bit is set to 1, the fault event will assert the corresponding fault flag and also assert the FS0B pin to report the fault condition to the system.

The FS0B pin will be released when all the system fault flags are cleared, by writing a 1 to the flag. Refer to section 16.7.1 System Fault Flags for a detailed description of the system fault flags.

Table 74. FS0B Fault control bits

FS0B Fault Control	Description
FS0B_DCRC	Allows FS0B to assert on dynamic CRC event
FS0B_DFS	Allows FS0B to assert when entering the DFS state
FS0B_VIN_OV	Allows FS0B to assert on a VIN_OV event
FS0B_XFAIL	Allows FS0B to assert when the XFAILB is asserted externally
FS0B_WD	Allows FS0B to assert when a watchdog event is present
FS0B_XRESET	Allows FS0B to assert when an reset is requested via the XRESET or FCCU
FS0B_SFAULT	Allows FS0B to assert when a soft fault is present
FS0B_HFAULT	Allows FS0B to assert when a hard fault is present: • Fault timer expired • FAULT_CNT = FAULT_MAX_CNT • RESET_CNT = RESET_MAX • Power up failure • Thermal shutdown • The RSTB pin short-to-low detected. • VIN crossing the UVDET on the Falling edge

12.8.8 FCCU1 (XRESET mode)

The FCCU1 pin is a programmable input pin in the PF09 to provide monitoring of external fault signals with various modes of operation. In devices where the FCCU operation is not available, the FCCU1 pin uses the OTP_FCCU1_MODE[1:0] bits to enable the external reset (XRESET) operation.

Table 75. FCCU1 pin operation when FCCU block is not available in the system.

OTP_FCCU0_MODE[1:0]	OTP_FCCU1_MODE[1:0]	FCCU1 Operation
Don’t care	00	No operation

Table 75. FCCU1 pin operation when FCCU block is not available in the system.*...continued*

OTP_FCCU0_MODE[1:0]	OTP_FCCU1_MODE[1:0]	FCCU1 Operation
Don't care	01	No operation
Don't care	10	No operation
Don't care	11	XRESET enabled

In devices where the FCCU operation is available, the FCCU1 pin operation is set based on the OTP_FCCU1_MODE[1:0] and OTP_FCCU0_MODE[1:0] bits.

Table 76. FCCU1 pin operation when FCCU block is available in the system.

OTP_FCCU0_MODE[1:0]	OTP_FCCU1_MODE[1:0]	FCCU1 Operation
00, 01, 10	00	No operation
00, 01, 10	01	FCCU1 single-ended Level detection[1]
00, 01, 10	10	FCCU1 single-ended PWM detection[1]
00, 01, 10	11	XRESET enabled
11	00, 01[2]	FCCU bi-stable[1]
11	11	Hybrid mode (XRESET / FCCU bi-stable) [1]

[1] For a detailed description of the FCCU operation, refer to section 18.7 FCCU Monitoring.
[2] Code 10 in the OTP_FCCU1_MODE[1:0] shall not be used when the FCCU Bistable mode is selected.

When the XRESET is enabled, the FCCU1 pin operates as an external reset input (XRESET). When the input is asserted, the device will generate a reset event to place the PMIC in a default known state. Refer to section 16.4.2 Reset Conditions for a detailed description of the implementation of a reset condition.

The polarity to detect a reset condition on the XRESET input is configured using the FCCU1_POL bit.

Table 77. XRESET polarity

FCCU1_POL	XRESET polarity
0	Reset event on rising edge
1	Reset event on Falling edge

The OTP_FCCU1_POL bit is provided to set the default value for the FCCU1_POL at power-up.

The XRST_DBNC[1:0] bits are provided to program the debounce filter to detect an external reset event on either the rising or Falling edge of the XRESET input.

Table 78. XRESET debounce timer

XRST_DBNC[1:0]	XRESET debounce timer
00	10 µs
01	50 µs
10	500 µs
11	1000 µs

The OTP_XRST_DBNC[1:0] bits are provided to set the default value for the XRST_DBNC[1:0] bits at power-up.

The XRST_MODE bit is provided to set the reset type generated upon an XRESET event.

Table 79. XRST_MODE

XRST_MODE	Reset type
0	hard reset
1	soft reset

The OTP_XRST_MODE bit is provided to set the default value of the XRST_MODE at power-up.

The XRESET input is always monitored during the RUN state, and the system can select to allow monitoring of the external reset signal in the STANDBY state via the XRST_STBY_EN bit.

Table 80. XRST_STBY_EN bit

XRST_STBY_EN	XRESET operation in STANDBY
0	Disabled
1	Enabled

The OTP_XRST_STBY_EN is used to set the default operation of the XRESET input in the STANDBY state.

12.8.9 GPIO1

The GPIO1 pin is a programable general-purpose IO with selectable open-drain or push-pull output buffer. The GPIO1 pin is configurable as a general-purpose output (GPO) or a dedicated input to perform the VSELECT operation via the OTP_GPIO1_MODE[1:0] bit.

Table 81. GPIO1 mode

OTP_GPIO1_MODE[1:0]	GPIO1 mode
00	Open-drain output
01	Push-pull output
10	Reserved
11	VSELECT input

The GPIO1_S flag is provided to read the real-time state of the GPIO1 pin.

Table 82. GPIO1_S flag

GPIO1_S	GPIO1 State
0	Low
1	High

12.8.9.1 GPO mode

When the GPIO1 is used as a general-purpose output (GPO mode), the pin will be asserted low during the OFF states. It can be set high by default during the Power-up sequence, or manually during the system-on states.

When the output is set as an open drain, the GPIO1 pin can be pulled up to any voltage lower than VIN with an external resistor between 10 kΩ to 470 kΩ.

System requirements must be taken into account when selecting the pullup voltage and resistance. To prevent the output from being pulled high in the ULPOFF state, the selection must ensure that the pullup voltage is not present during OFF condtions.

When the output is set as a push-pull driver, the PF09 will use the VIN internally to set the high state on the GPIO1 pin.

The GPIO1 uses the OTP_SEQ_TBASE[1:0] and the OTP_GPO1_SEQ[7:0] bits to enable the GPO by default at a specific time slot during the Power-up sequence. Refer to section 16.3.3 Regulator Power-up Sequence, for a detailed description of the Power-up sequence.

The GPIO1 pin is designed to have independent control configuration during the RUN and the STANDBY states, to allow full control of the GPIO1 when going in and out of the STANDBY state.

In the RUN state, the level of the GPIO1 pin can be controlled manually via the GPIO1_RUN bit.

Table 83. GPIO1 state in RUN

GPIO1_RUN	GPIO1 state
0	Low
1	High

In the STANDBY state, the level of the GPIO1 pin can be controlled manually via the GPIO1_STBY bit.

Table 84. GPIO1 state in STANDBY

GPIO1_STBY	GPIO1 state
0	Low
1	High

12.8.9.2 VSELECT mode

When the GPIO1 is operating in VSELECT mode, the GPIO1 pin is used as an input to select the output voltage of LDO2 when VSELECT_EN = 1. In this mode of operation, the pin is provided with an internal pulldown resistor to force a solid low condition in the event of a floating pin.

The VSELECT mode is available only when the LDO2 is operating in LDO mode. In all other LDO2 modes of operation, the GPIO1 will operate as a GPO output regardless of the value in the OTP_GPIO1_MODE bit.

When the GPIO1 is operating in VSELECT mode, the output voltage of the LDO2 will be set via the GPIO1 pin, or via the I^2C bits (VLDO2_RUN[4:0] / VLDO2_STBY[4:0]).

Table 85. LDO2 voltage selection

VSELECT_EN	GPIO1 pin	LDO2 voltage selection
1	Low	3.3 V
1	High	1.8 V
0	X	VLDO2_RUN[4:0] / VLDO2_STBY[4:0]

The default value for the VSELECT_EN bit is set to 1 after power on, to allow the system MCU to keep control of the LDO2 voltage.

In order to prevent an undetected transition of the LDO2 via the VSELECT, the device will generate the VSELECT_I interrupt every time the VSELECT input toggles.

12.8.10 GPIO2

The GPIO2 pin is a programable general-purpose IO with a selectable open-drain or push-pull output buffer. The GPIO pin is configurable as a general-purpose output (GPO) or a dedicated input to perform the LDO1EN operation via the OTP_GPIO2_MODE[1:0] bit.

Table 86. GPIO2 mode

OTP_GPIO2_MODE[1:0]	GPIO2 mode
00	Open-drain output
01	Push-pull output
10	Reserved
11	LDO1EN input

The GPIO2_S flag is provided to read the real-time state of the GPIO2 pin.

Table 87. GPIO2_S flag

GPIO2_S	GPIO2 State
0	Low
1	High

12.8.10.1 GPO mode

When the GPIO2 is used as a general-purpose output (GPO mode), the pin will be asserted low during the OFF states. il can be set high by default during the Power-up sequence, or manually during the system-on states.

When the output is set as an open drain, the GPIO2 pin can be pulled up to any voltage lower than VIN with an external resistor between 10 kΩ and 470 kΩ. System requirements must be taken into account when selecting the pullup voltage and resistance. To prevent the output from being pulled high in the ULPOFF state, the selection must ensure that the pullup voltage is not present during off condtions.

When the output is set as a push-pull driver, the PF09 will use the VIN internally to set the high state on the GPIO2 pin.

The GPIO2 uses the OTP_SEQ_TBASE[1:0] and the OTP_GPO2_SEQ[7:0] bits to enable the GPO by default at a specific time slot during the Power-up sequence. Refer to section 16.3.3 Regulator Power-up Sequence, for a detailed description of the Power-up sequence.

The GPIO2 pin is designed to have independent control configuration during the RUN and the STANDBY states, to allow full control of the GPIO2 when going in and out of the STANDBY state.

In the RUN state, the level of the GPIO2 pin can be controlled manually via the GPIO2_RUN bit.

Table 88. GPIO2 state in RUN

GPIO2_RUN	GPIO2 state
0	Low
1	High

In the STANDBY state, the level of the GPIO2 pin can be controlled manually via the GPIO2_STBY bit.

Table 89. GPIO2 state in STANDBY

GPIO2_STBY	GPIO2 state
0	Low
1	High

12.8.10.2 LDO1EN mode

When the GPIO2 is operating in LDO1EN mode, the GPIO2 pin is used as an input to enable or disable the output voltage of LDO1 by hardware. In this mode of operation, the pin is provided with an internal pulldown resistor to force a solid low condition in the event of a floating pin.

The LDO1EN mode is designed to allow the system to control the on/off status of the LDO1 regulator either by forcing the GPIO2 pin high or low (hardware control) or by using the corresponding I^2C bits to enable or disable the regulator in RUN or STANDBY states respectively (software control).

Table 90. LDO1EN mode

GPIO2 operation	LDO1_RUN_EN/ LDO1_STBY_EN	GPIO2 pin	LDO1 output
LDO1EN input	0	Do not care	Disabled
LDO1EN input	1	Low	Disabled
LDO1EN input	1	High	Enabled

In order to prevent an undetected transition of the LDO1 via the LDO1EN, the device will generate the LDO1EN_I interrupt every time the LDO1EN input toggles.

12.8.11 GPIO3

The GPIO3 pin is a programmable general-purpose IO with a selectable open-drain or push-pull output buffer. The GPIO pin is configurable as a general purpose output (GPO) or as a dedicated input, to perform the ERRMON fault monitoring operation via the OTP_GPIO3_MODE[1:0] bits.

Table 91. GPIO3 mode

OTP_GPIO3_MODE[1:0]	GPIO3 mode
00	Open-drain output
01	Push-pull output
10	Reserved
11	ERRMON input

Refer to section 18.6 External Error monitoring (ERRMON) for a detailed description of the ERRMON operation.

The GPIO3_S flag is provided to read the real-time state of the GPIO3 pin regardless of whether the I/O is working as an input or an output.

Table 92. GPIO3 state

GPIO3_S	GPIO3 state
0	Low
1	High

12.8.11.1 GPO mode

When the GPIO3 is used as a general purpose output (GPO mode), the pin will be asserted low during the OFF states. It can be set high by default during the Power-up sequence, or manually during the system-on states.

When the output is set as an open drain, the GPIO3 pin can be pulled up to any voltage lower than VIN with an external resistor between 10 kΩ and 470 kΩ. System requirements must be taken into account when selecting the pullup voltage and resistance. To prevent the output from being pulled high in the ULPOFF state, the selection must ensure that the pullup voltage is not present during OFF condtions.

When the output is set as push-pull driver, the PF09 will use the VIN internally to set the high state on the GPIO3 pin.

The GPIO3 uses the OTP_SEQ_TBASE[1:0] and the OTP_GPO3_SEQ[7:0] bits, to enable the GPO by default at a specific time slot during the power-up sequence. Refer to section 16.3.3 Regulator Power-up Sequence, for a detailed description of the Power-up sequence.

The GPIO3 pin is designed to have independent control configuration during the RUN and the STANDBY states, to allow full control of the GPIO3 when going in and out of the STANDBY state.

In the RUN state, the level of the GPIO3 pin can be controlled manually via the GPIO3_RUN bit.

Table 93. GPIO3 state in RUN state

GPIO3_RUN	GPIO3 state
0	Low
1	High

In the STANDBY state, the level of the GPIO3 pin can be controlled manually via the GPIO3_STBY bit.

Table 94. GPIO3 state in STANDBY state

GPIO3_STBY	GPIO3 state
0	Low
1	High

12.8.12 GPIO4

The GPIO4 pin is a programmable general-purpose IO with a selectable open-drain or push-pull output buffer. The GPIO pin is configurable as a general-purpose output (GPO) via the OTP_GPIO4_MODE[1:0] bits.

Table 95. GPIO4 mode

OTP_GPIO4_MODE[1:0]	GPIO4 mode
00	Open-drain output
01	Push-pull output
10	Reserved
11	Reserved

The GPIO4_S flag is provided to read the real-time state of the GPIO4 pin.

Table 96. GPIO4_S flag

GPIO4_S	GPIO4 state
0	Low
1	High

12.8.12.1 GPO mode

When the GPIO4 is used as a general-purpose output (GPO mode), the pin will be asserted low during the OFF states. It can be set high by default during the Power-up sequence, or manually during the system-on states.

When the output is set as an open drain, the GPIO4 pin can be pulled up to any voltage lower than VIN with an external resistor between 10 kΩ and 470 kΩ.

System requirements must be taken into account when selecting the pullup voltage and resistance. To prevent the output from being pulled high in the ULPOFF state, the selection must ensure that the pullup voltage is not present during off condtions.

When the output is set as a push-pull driver, the PF09 will use the VIN internally to set the high state on the GPIO4 pin.

The GPIO4 uses the OTP_SEQ_TBASE[1:0] and the OTP_GPO4_SEQ[7:0] bits, to enable the GPO by default at a specific time slot during the power-up sequence. Refer to section 16.3.3 Regulator Power-up Sequence, for a detailed description of the Power up sequence.

The GPIO4 pin is designed to have independent control configuration during the RUN and the STANDBY states, to allow full control of the GPIO4 when going in and out of the STANDBY state.

In the RUN state, the level of the GPIO4 pin can be controlled manually via the GPIO4_RUN bit.

Table 97. GPIO4 state in RUN

GPIO4_RUN	GPIO4 state
0	Low
1	High

In the STANDBY state, the level of the GPIO4 pin can be controlled manually via the GPIO4_STBY bit.

Table 98. GPIO4 state in STANDBY

GPIO4_STBY	GPIO4 state
0	Low
1	High

12.8.13 XFAILB

XFAILB is a bidirectional pin with an open-drain output. The XFAILB is able to accept a pullup voltage from 1.4 V to 5.5 V, typically pulled up to VANA in order to reduce current consumption during the Low-power off state. Additionally, a 100 nF capacitor is recommended to improve the EMC performance.

The OTP_XFAILB_EN bit is used to enable or disable the XFAILB mode of operation.

Table 99. XFAIL operation

OTP_XFAILB_EN	XFAIL operation
0	Disabled
1	Enabled

When the XFAILB mode is disabled, a transition on the XFAILB pin is ignored during the power-up or SYSTEM ON states. Because of this, no synchronization is possible.

When the XFAILB mode is enabled, the XFAILB pin is used to synchronize two or more PMICs during power-up and power-down events.

12.8.13.1 Power-up synchronization

During the OFF states, the XFAILB pin is asserted low internally. It will remain asserted during the PWRON event until it is ready to start the power-up sequence. Once the device meets all the conditions to start the power-up sequence, the XFAILB is released internally.

If the XFAILB pin is pulled down externally, the device will prevent the Power-up sequence from starting until the pin is no longer held low externally.

This will help the PMICs to synchronize the Power-up sequence, only after all PMICs are ready to initiate a power-up sequence.

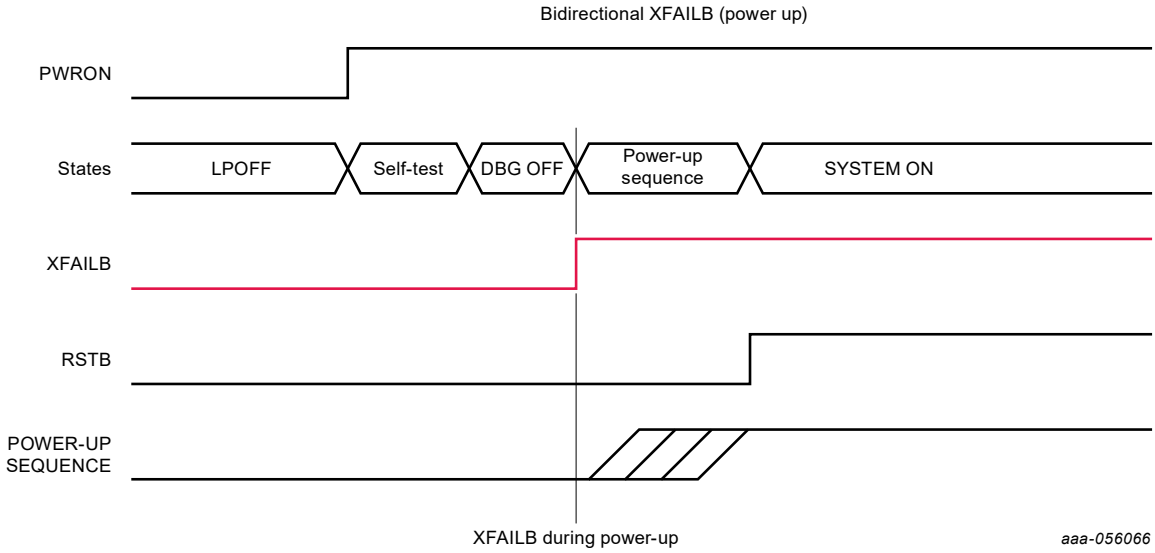


Figure 21. XFAILB during Power-up

12.8.13.2 Power-down synchronization

When two or more PMICs are synchronized using XFAILB, the power-down event can be started locally (requested by the MCU or due to a fault condition) or started externally when the PF09 detects a transition on the XFAILB bit.

When an internal power-up sequence failure is detected, the XFAILB pin will be asserted low right before the device starts turning off all the supplies that were already turned on during the Power-up sequence.

If XFAILB is asserted low externally during the Power-up sequence, the device will detect an external Power-up sequence failure, assert its own XFAILB pin, and turn off all supplies immediately.

During the system-on states, a turn-off event started locally will assert the XFAILB pin before starting the power-down sequence to request a turn-off event on all the devices connected to the XFAILB bus, in order to synchronize the power-down sequence of all the PMICs connected together.

During the SYSTEM ON states, If the XFAILB pin is externally pulled low, the PF09 will assert the XFAILB pin low internally, and the device will start a power-down sequence.

During a ard reset event (RSTB pin is asserted low), the device will assert the XFAILB pin low before it starts the power-down sequence, and it will hold the XFAILB pin low while the power-down sequence is in progress (including the power-down delay). At this point, the device will load the default configuration, release the XFAILB internally and wait until all PMICs have released the XFAIL bus, to start the new Power-up sequence at the same time.

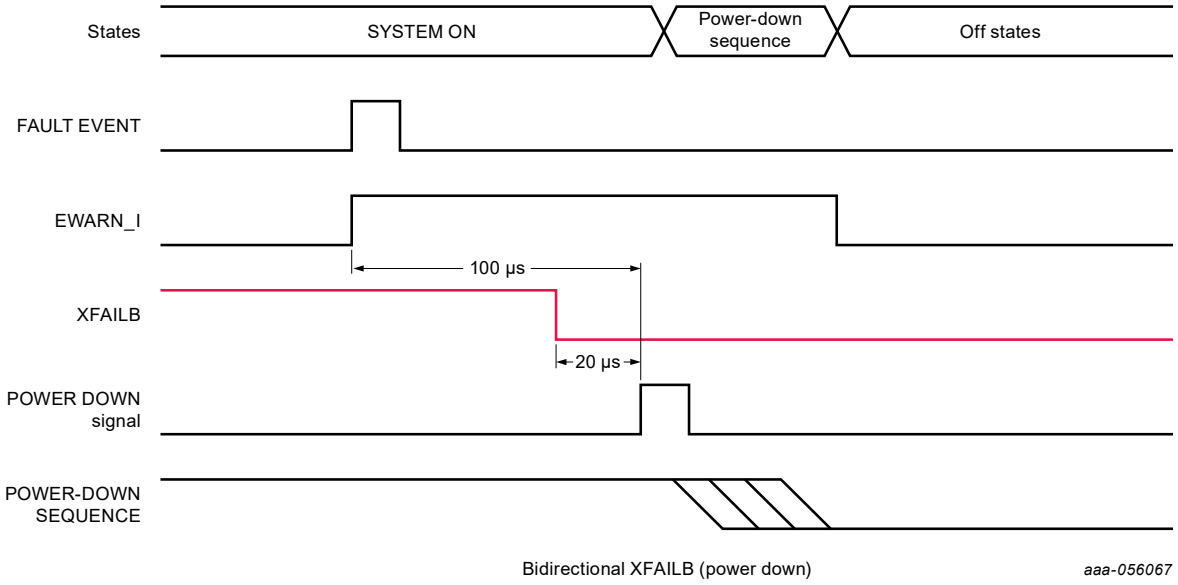


Figure 22. Bidirectional XFAILB (power-down)

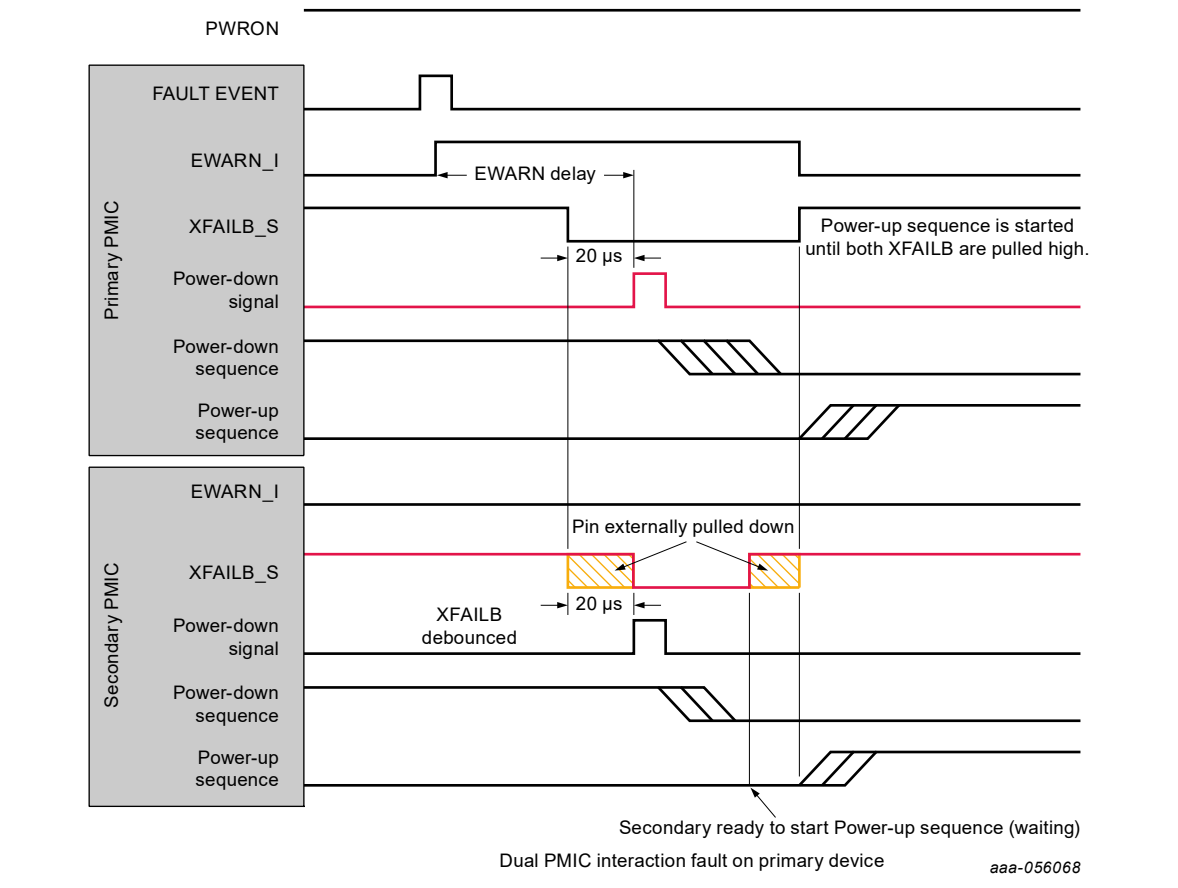


Figure 23. Dual PMIC interaction with fault on controller device

12.8.14 I²C Interface

Communication with the PF09 is done through a standard I²C protocol supporting various speeds to match various system requirements.

The SDA and SCL pins must be pulled up externally to VDDIO, and the selection of the external pullup resistors will depend on the maximum speed used in the system, as shown in the table below.

Table 100. I²C mode of operations

I²C mode	Speed	Pullup resistor	Access mode
Standard mode (Sm)	100 kbit/s	2.2 kΩ to 4.7 kΩ	Standard
Fast mode (Fm)	400 kbit/s	2.2 kΩ to 4.7 kΩ	Standard
Fast mode plus (Fm+)	1 Mbit/s	2.2 kΩ	Standard
High-speed mode (HS)	3.4 Mbit/s	0.8 kΩ	Single-byte “controller code” required

The PF09 High-speed mode (3.4 Mbit/s) is compatible with normal I²C devices on the same bus, but requires the controller to have an active pullup on the clock line, which is enabled during high-speed transfers. All high-speed transfers must be preceded by a single-byte "controller code" at fast or standard speed, to request the high-speed target devices to change to high-speed timing rules. This ensures that fast or normal speed devices will not try to participate in the transfer. For more details on the I²C protocol refer to the I2C-bus specification and user manual UM10204 available at https://www.nxp.com/.

The PF09 provides full I²C access during the RUN and the monitored STANDBY states. In the low-power STANDBY state, the PF09 features I²C communication on demand. This allows the PMIC to turn on the internal clock when an I²C transaction is started by the controller, perform the I²C command, and disable the internal clock when the bus goes idle, hence allowing the lowest power consumption during the low-power STANDBY state.

The default I²C device address is set in OTP during the part definition stage via the OTP_I2C_ADD[2:0] bit field.

Table 101. Setting up the I²C device address

OTP_I2C_ADD[2:0]	Device address
000	0x08
001	0x09
010	0x0A
011	0x0B
100	0x0C
101	0x0D
110	0x0E
111	0x0F

During an I²C transaction, the communication will latch after the eighthth bit of the last byte in the package is sent. If the data sent is not a multiple of eight bits and/or a bad I²C transaction is detected, the device will ignore the command and wait for a valid I²C transaction.

The device features a *burst mode*operation to read or write multiple contiguous registers without having to start a new transaction each time.

For more details on the I²C data package structure, please refer to the AN13107, PF series PMIC I2C-bus communication overview application note found at https://www.nxp.com/.

The PF09 provides various mechanisms on the I²C communication protocol to ensure proper communication and avoid system failures that could be caused by incorrect data.

12.8.14.1 I²C CRC verification

The I²C CRC mechanism is provide to verify the integrity of each I²C transaction. The CRC is enabled via the OTP_I2C_CRC_EN bit.

Table 102. Enabling the I²C CRC mechanism

OTP_I2C_CRC_EN	I²C CRC
0	Disabled
1	Enabled

The CRC calculation is based on the standard CRC-8-SAE as defined in the SAE-J1850 specificationn with the following characteristics.

Polynomial = 0x1D

Initial value = 0xFF

The CRC byte is calculated by shifting 24-bit data through the CRC polynomial. The 24-bit package is built as follows:

DEVICE_ADDR[b8] + REGISTER_ADDR [b8] +DATA[b8]

The DEVICE_ADDR is calculated as the seven-bit secondary address shifted left one space plus the corresponding read/write bit. (7Bit Address [b7] << 1) + R/W = DEVICE_ADDR[b8]

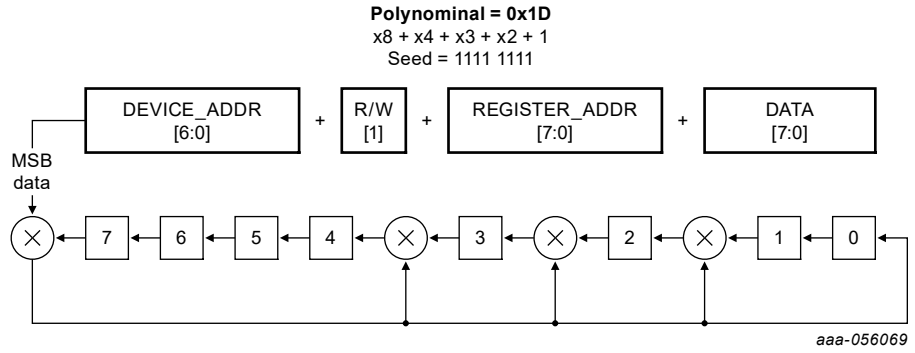


Figure 24. I²C CRC Polynomial

During an I²C write command, the MCU must calculate the CRC byte and send it after the data byte in the I²C package, to make a total of 32 bits per transaction.

After each I²C write transaction, the device calculates the corresponding CRC byte internally and compares it to the CRC sent by the MCU, to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the device ignores the current configuration command and sets the I2C_CRC_I. the I²C CRC interrupt will assert the INTB pin if the interrupt is not masked.

12.8.14.2 I²C secure write

A secure write protocol is implemented for specific registers critical to the functional safety of the device. The secure write functionality is enabled by the I2C_SECURE_EN bit, and the default value is set at power up via the OTP_I2C_SECURE_EN bit.

Table 103. Enabling I^2C secure write

I2C_SECURE_EN	I^2C secure write
0	Disabled
1	Enabled

When secure write is enabled, a specific sequence must be followed in order to grant write access on the corresponding secure register:

1. The MCU sends a command to modify the secure registers
2. The MCU reads a random code generated by the PMIC from the RANDOM_GEN register
3. The MCU must write the correct random code in the RANDOM_CHK register.

If RANDOM_CHK [7:0] matches the value in the RANDOM_GEN[7:0] bits, the device applies the configuration as requested by the initial command.

If RANDOM_CHK[7:0] is different from RANDOM_GEN[7:0], the device ignores the configuration command and waits for a new transaction.

In the event the MCU sends any other command instead of providing a value for the RANDOM_CHK register when the PF09 is expecting a random code confirmation, the device will cancel the ongoing secure write transaction and perform the new I^2C command.

In the event the MCU does not provide a value for the RANDOM_CHK register when the PF09 is expecting a random code confirmation, the I^2C transaction will time out 10 ms After the RANDOM_GEN code is generated, and the device will be ready for a new transaction.

The following table provides a list of all the bits requiring a secure write protocol when I2C_SECURE_EN = 1.

Table 104. Bit groups that may require a secure write protocol

Bit group	Description	Bit group	Description
System Configuration bits			
I2C_SECURE_EN	I2C secure write	STBY_POL	STBY pin polarity
RSTB_SOFTRST	RSTB pulse on soft reset	XRST_MODE	XRESET operating mode
VIN_OV_EN	VIN overvoltage protection	XRST_STBY_EN	XRESET operation in STANDBY
VIN_OV_SDWN	VIN overvoltage shutdown	XRST_DBNC	XRESET debounce timer
VIN_OV_DBNC	VIN overvoltage debounce	WD_EN	Watchdog counter
OV_DBNC	Regulator OV debounce	WD_DURATION	WD window duration
UV_DBNC	Regulator UV debounce	WD_OK_FCD	Fault counter reduction
FAULT_MAX_CNT	Maximum fault count	WD_NOK_MAX	WD NOK reset limit
TIMER_FAULT	Regulator fault timer	ERRMON_RESET	ERRMON reaction
RESET_MAX	Max reset events	ERRMON_TIME	ERRMON acknowledge time
FCCUx_POL	FCCU0 fault polarity FCCU1 fault polarity	FCCUx_RPULL_EN	FCCU0 internal pull resistor FCCU1 internal pull resistor
FCCUx_DBNC	FCCU0 debounce time FCCU1 debounce time	FCCUx_RESET	FCCU1 reset configuration FCCU1 reset configuration
FS0B_RELEASE	FS0B release command	VSELECT_EN	LDO2 VSELECT mode
SYS_CMD	System commands	–	–

Table 104. Bit groups that may require a secure write protocol*...continued*

Bit group	Description	Bit group	Description
GPIO Control Bits			
GPOx_SOFTRST_EN	GPO1 soft reset reaction GPO2 soft reset reaction GPO3 soft reset reaction GPO4 soft reset reaction	GPOx_RUN	GPO1 RUN control GPO2 RUN control GPO3 RUN control GPO4 RUN control
GPOx_STBY	GPO1 STANDBY control GPO2 STANDBY control GPO3 STANDBY control GPO4 STANDBY control	–	–
External VMON configuration bits			
VMONx_RUN	VMON1 RUN monitoring voltage VMON2 RUN monitoring voltage	VMONx_TMASK	VMON1 masking timer VMON2 masking timer
VMONx_EN	VMON1 operation VMON2 operation	VMONx_PG_EN	VMON1 PGOOD control VMON2 PGOOD control
VMONx_STBY	VMON1 STBY monitoring voltage VMON2 STBY monitoring voltage	–	–
Switching regulator control bits			
VSWx_RUN	SW1 RUN voltage SW2 RUN voltage SW3 RUN voltage SW4 RUN voltage SW5 RUN voltage	VSWx_STBY	SW1 STANDBY voltage SW2 STANDBY voltage SW3 STANDBY voltage SW4 STANDBY voltage SW5 STANDBY voltage
SWx_RUN_MODE	SW1 RUN operation SW2 RUN operation SW3 RUN operation SW4 RUN operation SW5 RUN operation	SWx_STBY_MODE	SW1 STANDBY operation SW2 STANDBY operation SW3 STANDBY operation SW4 STANDBY operation SW5 STANDBY operation
SWx_SLOWDVS	SW1 DVS ramp-down speed SW2 DVS ramp-down speed SW3 DVS ramp-down speed SW4 DVS ramp-down speed SW5 DVS ramp-down speed	SWx_SOFTRST_EN	SW1 soft reset reaction SW2 soft reset reaction SW3 soft reset reaction SW4 soft reset reaction SW5 soft reset reaction
SWx_UV_BYP	SW1 bypass UV detection SW2 bypass UV detection SW3 bypass UV detection SW4 bypass UV detection SW5 bypass UV detection	SWx_OV_BYP	SW1 bypass OV detection SW2 bypass OV detection SW3 bypass OV detection SW4 bypass OV detection SW5 bypass OV detection

Table 104. Bit groups that may require a secure write protocol*...continued*

Bit group	Description	Bit group	Description
SWx_UV_STATE	SW1 undervoltage reaction SW2 undervoltage reaction SW3 undervoltage reaction SW4 undervoltage reaction SW5 undervoltage reaction	SWx_OV_STATE	SW1 Overvoltage reaction SW2 Overvoltage reaction SW3 Overvoltage reaction SW4 Overvoltage reaction SW5 Overvoltage reaction
SWx_FLT_REN	SW1 output recovery SW2 output recovery SW3 output recovery SW4 output recovery SW5 o recovery	SWx_PG_EN	SW1 Enable PGOOD Control SW2 Enable PGOOD Control SW3 Enable PGOOD Control SW4 Enable PGOOD Control SW5 Enable PGOOD Control
SWx_IL_BYP	SW1 bypass ILIM detection SW2 bypass ILIM detection SW3 bypass ILIM detection SW4 bypass ILIM detection SW5 bypass ILIM detection	–	–
LDO regulator control bits			
LDOx_RUN_EN	LDO1 RUN control LDO2 RUN control LDO3 RUN control	LDOx_STBY_EN	LDO1 STANDBY Control LDO2 STANDBY Control LDO3 STANDBY Control
VLDOx_RUN	LDO1 RUN voltage LDO2 RUN voltage LDO3 RUN voltage	VLDOx_STBY	LDO1 STANDBY Voltage LDO2 STANDBY Voltage LDO3 STANDBY Voltage
LDOx_UV_BYP	LDO1 bypass UV detection LDO2 bypass UV detection LDO3 bypass UV detection	LDOx_OV_BYP	LDO1 bypass OV Detection LDO2 bypass OV Detection LDO3 bypass OV Detection
LDOx_IL_BYP	LDO1 bypass ILIM detection LDO2 bypass ILIM detection LDO3 bypass ILIM detection	LDOx_SOFTRST_EN	LDO1 soft reset Reaction LDO2 soft reset Reaction LDO3 soft reset Reaction
LDOx_FLT_REN	LDO1 output recovery LDO2 output recovery LDO3 output recovery	LDOx_PG_EN	LDO1 enable PGOOD control LDO2 enable PGOOD control LDO3 enable PGOOD control
LDOx_UV_STATE	LDO1 UV reaction LDO2 UV reaction LDO3 UV reaction	LDOx_OV_STATE	LDO1 OV reaction LDO2 OV reaction LDO3 OV reaction
VLDOxMON_TMASK	VLDO2MON masking timer VLDO3MON masking timer	–	–
VAON control bits			
VAON	VAON voltage	VAON_TFLT	VAON fault timer
VAON_UV_BYP	VAON undervoltage detection	VAON_OV_BYP	VAON overvoltage detection
VAON_UV_STATE	VAON undervoltage reaction	VAON_OV_STATE	VAON overvoltage reaction

Table 104. Bit groups that may require a secure write protocol*...continued*

Bit group	Description	Bit group	Description
VAON_FLT_REN	VAON output recovery	VAON_PG_EN	VAON PGOOD control
VAON_RESET_EN	VAON always-on reset	–	–

13 Functional blocks

13.1 Analog core and internal references

13.1.1 VANA

The PF09 uses a low-power analog supply to power various internal analog circuits. The VANA supply is disabled during the ULPOFF, LPOFF and DFS states to reduce power consumption on those states.

The VANA supply must be decoupled externally with a 1 µF capacitor. The system, however, is not allowed to use the supply to power external circuits, except for the scenarios where the VANA is used as the pullup voltage for the XFAILB pin.

An undervoltage detection circuit serves as the POR threshold for the circuits powered by this regulator inside of the PF09. When an undervoltage is detected in the VANA supply during the SYSTEM ON states, the device will move to the Deep Fail-safe state (DFS).

An overvoltage detection is provided in the VANA regulator as part of the functional safety architecture. When the VANA crosses the OV threshold, the VANA_OV_I interrupt bit is set and the INTB pin will be asserted low if the interrupt is not masked.

The VANA_OV_S bit provides the real-time status of the VANA overvoltage monitor.

Symbol	Parameter	Min	Typ	Max	Unit
VANA	VANA Output Voltage	1.55	1.6	1.65	V
CVANA	VANA output capacitor	—	1	—	µF

Table 105. VANA overvoltage status

VANA_OV_S	VANA overvoltage status
0	No OV detected
1	OV detected

13.1.2 VDIG

The PF09 uses a low-power digital supply to power the digital circuits inside the IC. The VDIG supply is disabled only during the ULPOFF states, to achieve the lowest power consumption in this state.

An undervoltage detection circuit serves as the POR threshold for the digital controller powered by this regulator inside of the PF09.

An overvoltage detection is provided in the VDIG regulator as part of the functional safety architecture. When the VDIG crosses the OV threshold, the VDIG_OV_I interrupt bit is set, and the INTB pin will be asserted low if the interrupt is not masked. Devices targeting a higher safety integrity level featuring a dedicated digital machine supervisor (DMS) provide a second level of protection against a VDIG_OV condition, to ensure a proper safe reaction even if such a condition causes the main digital controller to be unresponsive.

The VDIG_OV_S bit provides the real-time status of the VDIG overvoltage monitor.

Symbol	Parameter	Min	Typ	Max	Unit
VDIG	VDIG Output Voltage	1.55	1.6	1.65	V
CVDIG	VDIG output capacitor	—	1	—	µF

Table 106. VDIG overvoltage status

VDIG_OV_S	VDIG overvoltage status
0	No OV detected
1	OV detected

13.1.3 Internal bandgap references

The PF09 is provided with two fully independent bandgap references as part of the functional safety architecture.

The first bandgap regulator is dedicated to providing a voltage reference for the output voltage generation, and it is referred to as *main bandgap* through this document. The second bandgap regulator is used to provide a voltage reference to the OV/UV monitors, as well as other safety related blocks, and it is referred to as *monitoring bandgap* throughout this document.

13.2 System voltage generation

13.2.1 VAON

The VAON regulator is a standalone low-power LDO with low dropout operation. It supports an Always-on mode to provide voltage to the low-power domains intended to remain on during the PMIC off states. The VAON supports configurable output voltage with nominal current of 10 mA.

The VAON output is programmable to 1.8 V, 3.0 V or 3.3 V with up to +/- 2% accuracy.

Table 107. VAON output voltage

VAON[1:0]	VAON output voltage (V)
00	Off
01	1.8
10	3.0
11	3.3

By default, the VAON regulator uses the OTP_VAON[1:0] bits to set the initial voltage configuration as soon as power is applied.

The VAON can be configured in two different modes of operation based on the value of the OTP_VAON[1:0] and the OTP_VAON_SEQ[7:0] bits.

Table 108. VAON modes

OTP_VAON[1:0]	OTP_VAON_SEQ[7:0]	Mode	Control
00	Don’t care	System regulator	Default off (enabled via I^2C)
01, 10, 11	0x00	Always-on regulator	Enabled after fuse load
01, 10, 11	Not 0x00	System regulator	Enabled in Power-up sequence

13.2.1.1 Always-on mode

When power is applied for the first time, the PF09 will perform an initial configuration cycle to load the OTP configuration of the VAON regulator. If the VAON is set as an Always-on regulator, the VAON output will be enabled after fuse load.

When the VAON is configured in Always-on mode, the regulator output remains enabled all the time, as long as the VIN supply does not cross the UVDET threshold or the state machine does not enter the DFS state due to a critical fault condition. In scenarios such as these, the VAON will be enabled again after the new fuse-loading event when the device experiences a new cold boot or is able to wake up from the DFS state.

13.2.1.2 System regulator mode

When VAON is set as a system regulator, the VAON output will be allowed to turn on only during the SYSTEM ON states, following the power-up and power-down sequences, as configured via the OTP and functional registers.

In applications where the VAON block is used as a system regulator, the OTP_VAON[1:0] will be used to set the default voltage during the Power-up sequence. The VAON, however, can also remain disabled by default, and the VAON[1:0] functional bits can be used to set the output voltage during the SYSTEM ON state, allowing the MCU to enable the supply on the go at the required voltage level.

13.2.1.3 Electrical characteristics

Table 109. VAON electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, V_{IN} = 5.0 V, V_{AON} = 1.8 V, I_{AON} = 10 mA and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V, V_{AON} = 1.8 V, I_{AON} = 10 mA, and Ta = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{IN_VAON}	VAON operating input range	UVDET	–	5.5	V
I_{Q_VAON}	VAON quiescent current • Max IQ at T_A = 85°C	–	2	5	µA
I_{LIM_VAON}	VAON current limit	30	–	60	mA
$V_{AON\_PSRR\_AC}$	AC power supply rejection ratio • 400 kHz • 100 µA < I_{AON} ≤ 10 mA • V_{IN} = V_{AON} + 300 mV	30	–	–	dB
R_{DSON_VAON}	VAON dropout mode resistance	–	–	5	Ω
R_{PD_VAON}	VAON discharge pulldown resistor	–	60	100	Ω
V_{AON_OS}	VAON startup overshoot	–	–	200	mV
V_{AON_AC}	VAON load transient IAON_AC: 0 mA to 10 mA	-100	–	100	mV
V_{AON_TON}	VAON turn-on time • VAON enabled to 90 % of final value	–	–	1.7	ms
V_{AON_ACC}	VAON output voltage accuracy	-2	–	2	%
V_{AON_LOR}	VAON DC load regulation	-1	–	1	%
V_{AON_LIR}	VAON DC line regulation	-1	–	1	%
I_{VAON}	VAON nominal output current	10	–	–	mA
V_{AON_DROP}	VAON LDO minimum headroom • Minimum headroom to ensure regulation.	200	–	–	mV
$V_{AON\_LP\_UV}$	VAON low-power undervoltage threshold	1.4	1.5	1.6	V

13.2.2 SW1 (3.5 A peak/valley current mode buck regulator)

The PF09 features one low-voltage peak current mode (PCM) or valley current mode (VCM) buck regulator with wide output voltage range from 0.5 V to 3.3 V, with up to 1.5 % output accuracy and 3.5 A nominal load current capability.

The default voltage configuration for the SW1 regulator at power-up is set in OTP via the OTP_VSW1_RUN[7:0] bits, and the dynamic configuration of the output voltage during the RUN state is controlled via the VSW1_RUN[7:0] functional bits.

The default voltage configuration for the SW1 regulator to be used during the STANDBY state is set in OTP via the OTP_VSW1_STBY[7:0] bits, and the MCU can modify the target STANDBY voltage configuration of the SW1 regulator during any of the SYSTEM ON states via the VSW1_STBY[7:0] functional bits.

The MCU is expected to update the VSW1_STBY[7:0] bits before directing the PMIC to enter the STANDBY state. The selection of the VSW1_STBY[7:0] will depend on the system requirements of the specific low-power mode it wants to achieve at the system level.

Table 110. SW1 output voltage configuration bits

VSW1_RUN[7:0] VSW1_STBY[7:0]	Voltage setting
0x00 to 0x08	Reserved
0x09 to 0x91	0.50000 V to 1.35000 V in 6.25 mV steps
0x92 to 0x9E	Reserved
0x9F	1.50000 V
0xA0 to 0xD8	1.80000 V to 2.50000 V in 12.5 mV steps
0xD9 to 0xDF	Reserved
0xE0 to 0xF4	2.80000 V to 3.30000 V in 25.0 mV steps
0xF5 to 0xFF	Reserved

DVS is available under the following conditions:

1. Dynamic voltage scaling (DVS) range is between 0.65 V and 0.9 V.
2. The OV/UV threshold is +/-5% or wider.
3. DVS ramp must be 3.9 mV/µs or slower.

The VSW1_RUN[7:0] and VSW1_STBY[7:0] bits are implemented as secure write bits to ensure that the output voltages are not changed by mistake during the SYSTEM ON states.

The OTP_SW1_DVS[1:0] bits are used to program the default slew rate for the SW1 turn-on and turn-off ramps. During the SYSTEM ON states, the DVS rate can be changed dynamically to allow different voltage scaling slew rates as required by the system. The SYSTEM ON DVS rate is controlled by the SW1_DVS[1:0] bits on the functional registers.

Table 111. DVS ramp selection bits

SW1_DVS[1:0]	Clocking factor	SW1 ramp-up slope rate [1][2]	SW1 ramp-down slope rate[1][2]
00	8	1.95 mV/µs	1.95 mV/µs
01	4	3.9 mV/µs	3.9 mV/µs
10	2	7.8 mV/µs	7.8 mV/µs
11	1	15.6 mV/µs	15.6 mV/µs

[1] At 20 MHz high frequency clock selection.

[2] The slope rate is calculated as (6.25 [mV] * FREQ [MHz]) / (8 * clocking factor)

In applications where the output capacitance is larger than the recommended value, the SW1_SLOWDVS bit provides the option to force the ramp-down slope to the slowest discharge speed in order to ensure the output is able to fully discharge before a new turn-on cycle is started.

The SW1_SLOWDVS bit is reset to 1 at power-up, and the MCU can modify it during the SYSTEM ON states if the system requires a faster discharge on the SW1 regulator.

Table 112. DVS ramp-down selection bits

SW1_SLOWDVS	Ramp-down DVS
0	Same as ramp up
1	1.95 mV/µs

The SW1 regulator is only allowed to request a dynamic voltage change when the default OTP value is set to be within the DVS range. The DVS range is between 0.65 V and 0.9 V, with an OV/UV threshold of 5 % or wider and a DVS ramp of 3.9 mV/µs or slower. A voltage configuration outside of the DVS range will be fixed to the default OTP value, and any voltage change requested via the I^2C communication will be ignored to avoid an invalid configuration.

The OTP_SW1_DVSMAX[3:0] bits are provided to define the maximum high-voltage delta allowed during a DVS transition. Maximum high-voltage delta is calculated with respect to the default voltage setting selected by the OTP_VSW1_RUN[7:0] bits to ensure the system is not able to request a voltage change outside of the selected limits defined for a specific application.

Table 113. Maximum DVS selection bits

OTP_SW1_DVSMAX[3:0]	SW1 high-voltage delta
0000	0.025 V
0001	0.050 V
0010	0.075 V
0011	0.100 V
0100	0.125 V
0101	0.150 V
0110	0.175 V
0111	0.200 V
1000	0.225 V
1001	0.250 V
1010	0.275 V
1011	0.300 V
1100	0.325 V
1101	0.350 V
1110	0.375 V
1111	0.400 V

If the MCU tries to write a voltage value in SW1 higher than the OTP_SW1_DVSMAX[3:0] selection, the controller will ignore the command and send a DVSMAX_I interrupt. The DVSMAX_I interrupt will assert the INTB pin if the interrupt is not masked.

The OTP_SW1_DVSMIN[3:0] bits are provided to define the maximum low voltage delta allowed during a DVS transition. The maximum low-voltage delta is calculated with respect to the default voltage setting selected by the OTP_VSW1_RUN[7:0] bits, to ensure the system is not able to request a voltage change outside of the selected limits defined for a specific application.

Table 114. Minimum DVS selection bits

OTP_SW1_DVSMIN[3:0]	SW1 low-voltage delta
0000	0.025 V
0001	0.050 V
0010	0.075 V
0011	0.100 V
0100	0.125 V
0101	0.150 V
0110	0.175 V
0111	0.200 V
1000	0.225 V
1001	0.250 V
1010	0.275 V
1011	0.300 V
1100	0.325 V
1101	0.350 V
1110	0.375 V
1111	0.400 V

If the MCU tries to write a voltage value in SW1 lower than the OTP_SW1_DVSMIN[3:0] selection, the controller will ignore the command and send a DVSMIN_I interrupt. The DVSMIN_I interrupt will assert the INTB pin if the interrupt is not masked.

The SW1_RUN_MODE[1:0] bits are provided to change the mode of operation of the SW1 regulator during the RUN state. If the SW1 is enabled in the Power-up sequence, the SW1_RUN_MODE[1:0] will be set to PWM by default.

Table 115. Mode selection in RUN

SW1_RUN_MODE[1:0]	Mode selection in RUN
00	OFF
01	PWM
10	PFM
11	Reserved

The SW1_STBY_MODE[1:0] bits are provided to change the mode of operation of the SW1 regulators during the STANDBY state.

Table 116. Mode selection in STANDBY

SW1_STBY_MODE[1:0]	Mode selection in STANDBY
00	OFF

Table 116. Mode selection in STANDBY*...continued*

SW1_STBY_MODE[1:0]	Mode selection in STANDBY
01	PWM[1]
10	PFM
11	Reserved

[1] PWM selection is only available during the monitored STANDBY state. The regulator will operate in PFM when the device is in the LP_STANDBY state.

The default value for the SW1_STBY_MODE[1:0] bits is loaded at power-up from the OTP_SW1_STBY_EN bit.

Table 117. Default SW1 mode selection during STANDBY

OTP_SW1_STBY_EN	SW1 operation in STANDBY
0	OFF
1	PFM

When the SW1 regulator changes the mode between the PWM and PFM, The SW1_MODE_I interrupt will be generated when the mode transition is finished. The INTB pin will be asserted if the SW1_MODE interrupt is not masked.

The SW1_ILIM[1:0] bits are provided to program the current limit detection in the SW1 regulator. The default current limit is loaded at power up from the OTP_SW1_ILIM[1:0] bits.

Table 118. Current limit selection bits

SW1_ILIM[1:0]	Current limit
00	6.0 A
01	4.0 A
10	5.0 A
11	6.0 A

The SW1_PH[2:0] bits are provided to control the phase shift of the switching frequency. The default switching phase is loaded at power up from the OTP_SW1_PH[2:0] bits.

Table 119. SW1 phase shift selection bits

SW1_PH[2:0]	Phase control
000	45°
001	90°
010	135°
011	180°
100	225°
101	270°
110	315°
111	0°

13.2.2.1 3.3 V load switch operation

The load switch operation in SW1 is provided to support systems operating from a 3.3 V input supply requiring a 3.3 V gated output capable of being sequenced in the right order during the Power-up sequence. In such

scenarios, the SW1 block can be used as a low-drop load switch to enable the 3.3 V input to be switched on and off as required by the system.

The OTP_SW1LS_EN bit is provided to configure the SW1 block as a load awitch (SW1LS). In this mode of operation, no inductor is required, and the SW1LX pin is used as the output of the load switch, which must be connected to the SW1FB pin to monitor the output voltage.

When the SW1LS output is disabled, the internal HS FET becomes open and the internal pulldown is applied to discharge the output.

Table 120. Load switch mode selection bit

OTP_SW1LS_EN	SW1 mode
0	Regulator mode
1	Load switch mode

The SW1 load switch (SW1LS) is intended to take a 3.3 V input and gate the output using the SW1_RUN_MODE[1:0] and SW1_STBY_MODE[1:0] in the RUN and STANDBY states respectively.

Table 121. SW1LS control bits

SW1_RUN_MODE[1:0] SW1_STBY_MODE[1:0]	SW1LS Operation
00	Output disable (HS FET open)
01	Output enabled (without monitoring)
10	Output enabled (with monitoring)
11	Reserved (output disabled)

When the SW1LS output is enabled during the Power-up sequence, the SW1_RUN_MODE[1:0] will default to 0b10 (output enabled with monitoring). The system can change the configuration during the SYSTEM ON states.

The default value of the SW1_STBY_MODE[1:0] at power up is set based on the OTP_SW1_STBY_EN[1:0] and the OTP_LP_STBY bits.

Table 122. SW1LS default STANDBY configuration

OTP_SW1_STBY_EN	OTP_LP_STBY	SW1_STBY_MODE[1:0]	Default STANDBY operation
0	x	00	Output disable (HS FET open)
1	0	10	Output enabled with monitoring
1	1	01	Output enabled no monitoring

When the SW1LS output is enabled with no monitoring, the SW1 output will neither control the PGOOD pin nor generate an OV/UV condition.

When the SW1LS output is enabled with monitoring during the RUN state, the internal voltage monitor will be enabled and will expect a voltage as selected by the VSW1_RUN[7:0] bits.

When the SW1LS output is enabled with monitoring during the monitored STANDBY state, (OTP_LP_STBY = 0), the internal voltage monitor will be enabled and will expect a voltage as selected by the VSW1_STBY[7:0] bits.

When the internal monitor is expected to be enabled during the load switch operation, the system designer must ensure that the output voltage in the corresponding state is always set to 3.3 V or a lower value, and the OV/UV monitoring thresholds are wide enough to account for voltage losses in the load switch.

The SW1LS_OCP bit is provided to set the reaction of the SW1LS output when an overcurrent condition is present. The default value of the SW1LS_OCP bit is set in OTP via the OTP_SW1LS_OCP bit.

Table 123. SW1LS overcurrent protection bit

SW1LS_OCP	SW1LS overcurrent protection
0	Interrupt only
1	SW1LS OFF

When the SW1LS_OCP = 0, an OCP condition will set the SW1LS_OCP_I interrupt only without disabling the output voltage.

When the SW1LS_OCP = 1, an OCP condition will set the SW1LS_OCP_I interrupt and disable the SW1LS output immediately.

The SW1LS_OCP_I interrupt will assert the INTB pin if the interrupt is not masked.

Once the OCP mechanism has disabled the SW1LS output, the system will be able to recover the output by clearing the SW1LS_OCP_I bit.

13.2.2.2 Electrical characteristics

Table 124. SW1 electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, V_{SW1IN} = V_{IN} = UVDET to 5.5 V, V_{SW1FB} = 3.3 V, I_{SW1} = 1 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SW1IN} = 5.0 V, V_{SW1FB} = 3.3 V, I_{SW1} = 1000 mA, and Ta = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{SW1IN}	Operating input range[1] • Minimum headroom = VSW1FB + I_{OUT_MAX} * RON / DC. • I_{OUT_MAX} = minimum ILIM selected for SW1 • RON includes HS FET R_{DSON}, bond wire resistance, PCB trace resistance and inductor DCR. • Maximum duty cycle = 100%	UVDET	–	5.5	V
f_{SW}	Operating switching frequency	1.9	–	3.15	MHz
$V_{SW1ACC3}$	Output voltage accuracy • PWM mode • 0.5V ≤ V_{SW1FB} < 0.8V	-10	–	10	mV
$V_{SW1ACC1}$	Output voltage accuracy • PWM mode • 0.8V ≤ V_{SW1FB} < 1.35V	-1.5	–	1.5	%
$V_{SW1ACC2}$	Output voltage accuracy • PWM Mode • 1.5V ≤ V_{SW1FB} ≤ 3.3V	-1.5	–	1.5	%
$V_{SW1PFMACC3}$	Output voltage accuracy • PFM mode • 0.5V ≤ V_{SW1FB} < 0.8 V	-20	–	20	mV
$V_{SW1PFMACC1}$	Output voltage accuracy • PFM mode • 0.8V ≤ V_{SW1FB} < 1.35 V	-3	–	3	%
$V_{SW1PFMACC2}$	Output voltage accuracy • PFM Mode	-3	–	3	%

Table 124. SW1 electrical characteristics...*continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{SW1IN} = V_{IN} = UVDET to 5.5 V, V_{SW1FB} = 3.3 V, I_{SW1} = 1 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SW1IN} = 5.0 V, V_{SW1FB} = 3.3 V, I_{SW1} = 1000 mA, and Ta = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• 1.5V ≤ V_{SW1FB} ≤ 3.3V				
$V_{SW1RIPPLE}$	Output voltage ripple • PWM mode • Frequency Spread spectrum Disabled	–	6	–	mV
I_{SW1}	SW1 nominal current	3.5	–	–	A
I_{LIM1_SW1}	SW1 current limit • SW1_ILIM[1:0] = 01	2.8	4.0	5	A
I_{LIM2_SW1}	SW1 current limit • SW1_ILIM[1:0] = 10	3.8	5.0	6	A
I_{LIM3_SW1}	SW1 current limit • SW1_ILIM[1:0] = 00 or 11	4.75	6	7	A
I_{LIMN_SW1}	Negative current limit	1.8	2.5	3.62	A
V_{SOS_SW1}	Startup overshoot • SW1_DVS[1:0] = 11 (15.6 mV/µs) • V_{SW1IN} = 5.0 V • V_{SW1FB} = 3.3 V	-25	25	50	mV
t_{ONMIN_SW1}	Turn-on time • From 10 % to 90 % of end value • SW1_DVS[1:0] = 11 (15.6 mV/µs) • V_{SW1IN} = 5.0 V • V_{SW1FB} = 0.5 V	32	–	–	µs
t_{ONMAX_SW1}	Maximum turn-on time • From 10 % to 90 % of end value • SW1_DVS[1:0] = 00 (1.95 mV/µs) • V_{SW1IN} = 5.0 V • V_{SW1FB} = 3.3 V	–	–	1690	µs
η_{SW1_PWM1}	PWM efficiency at full load (see Table 12) • V_{SW1IN} = 5.0 V • V_{SW1FB} = 3.3 V • f_{SW1} = 2.5 MHz • TA = 25 °C	–	90	–	%
η_{SW1_PWM2}	PWM efficiency at 40% load • V_{SW1IN} = 5.0 V • V_{SW1FB} = 3.3 V • f_{SW1} = 2.5 MHz • T_A = 25 °C	–	94	–	%
η_{SW1_PWM3}	PWM efficiency at full load (see Table 12) • V_{SW1IN} = 5.0 V • V_{SW1FB} = 0.8 V • f_{SW1} = 2.5 MHz • T_A = 25 °C	–	73	–	%

Table 124. SW1 electrical characteristics...*continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{SW1IN} = V_{IN} = UVDET to 5.5 V, V_{SW1FB} = 3.3 V, I_{SW1} = 1 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SW1IN} = 5.0 V, V_{SW1FB} = 3.3 V, I_{SW1} = 1000 mA, and Ta = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
η_{SW1_PWM4}	PWM efficiency at 40 % load • V_{SW1IN} = 5.0 V • V_{SW1FB} = 0.8 V • f_{SW1} = 2.5 MHz • T_A = 25 °C	–	81.5	–	%
t_{DB_SW1}	Dead-band time	–	3	5	ns
t_{LXSR1_SW1}	Switching node slew time	–	2.5	–	ns
V_{LOTR1_SW1}	Transient load regulation (single phase) • 0.5 V ≤ V_{SW1FB} ≤ 1.35 V • I_{STEP} = 200 mA to 1.0 A, di/dt = 2.0 A/µs • f_{SW} = 2.5 MHz , C_{OUT} = 44 µF, L_{OUT} = 0.47 µH • V_{IN} = 5.0 V	-25	–	25	mV
V_{LOTR2_SW1}	Transient load regulation (single phase) • 1.5 V ≤ V_{SW1FB} ≤ 3.3 V • I_{STEP} = 200 mA to 1.0 A, di/dt = 2.0 A/µs • f_{SW} = 2.5 MHz, C_{OUT} = 44 µF, L_{OUT} = 0.47 µH • V_{IN} = 5.0 V	-3	–	3	%
$t_{PFM2PWM\_SW1}$	PFM to PWM transition time	10	–	50	µs
I_{QPFM_SW1}	SW1 regulator quiescent current • PFM mode output not switching • Max IQ at TA = 85 °C	–	15	20	µA
R_{DS25_SW1HS}	High-side FET R_{DSON} [2] • T_J = 25 °C • Including bond-wire and package resistance	–	46	–	mΩ
R_{DS125_SW1HS}	High-side FET R_{DSON}[2] • T_J = 125 °C • Including bond-wire and package resistance	–	60	–	mΩ
R_{DS25_SW1LS}	Low-side FET R_{DSON} [3] • T_J = 25 °C • Including bond-wire and package resistance	–	27	–	mΩ
R_{DS125_SW1LS}	Low-side FET R_{DSON} [3] • T_J = 125 °C • Including bond-wire and package resistance	–	35	–	mΩ
R_{DIS_SW1}	Discharge resistance • Regulator disabled and ramp completed	20	60	100	Ω
V_{SW1IN_LS}	Operating input range in load switch mode	–	3.3	3.5	V
$I_{LIM\_LS\_SW1}$	Load switch current limit	3.6	–	5.4	A
$T_{ON\_LS\_SW1}$	Load switch turn-on time	–	–	2000	µs
tOCP_LS_SW1	Load switch OCP deglitch time	500	–	–	µs

[1] UVDET represents the minimum functional level for the PF09; VSW1IN must meet the minimum headroom to ensure proper output voltage regulation.

[2] Typical high-side FET resistance due to packaging (bondwire + metal) at room temperature is 20.5mΩ.
[3] Typical low-side FET resistance due to packaging (bondwire + metal) at room temperature is 21mΩ.

Table 125. Recommended external components.

Symbol	Description	Min	Typ	Max	Units
L	Output inductor • Typical inductor DC resistance: < 25 mΩ • Minimum saturation current at full load: 7.0 A	–	0.47	–	µH
C_{OUT}	Effective output capacitance • 2x22 µF, 6.3 V • Low equivalent series resistance (ESR) ceramic capacitor	22	44	300	µF
C_{IN}	Input capacitor • 4.7 µF, 10 V • Low ESR ceramic capacitor	4.23	4.7	5.17	µF

13.2.3 SW2 - SW5 (2.5 A peak/valley current mode buck regulator)

The PF09 features four low-voltage, multiphase, peak current mode (PCM) or valley current mode (VCM) buck regulators with wide output voltage ranges from 0.3 V to 3.3 V, with up to 1.5 % output accuracy and 2.5 A nominal load current capability.

The default voltage configuration for the SW*x* regulator at power-up is set in OTP via the OTP_VSW*x*_RUN[7:0] bits, and the dynamic configuration of the output voltage during the RUN state is controlled via the VSW*x*_RUN[7:0] functional bits.

The default voltage configuration for the SW*x* regulator to be used during the STANDBY state is set in OTP via the OTP_VSW*x*_STBY[7:0] bits, and the MCU can modify the target STANDBY voltage configuration of the SW*x* regulator during any of the SYSTEM ON states via the VSW*x*_STBY[7:0] functional bits.

The MCU is expected to update the VSW*x*_STBY[7:0] bits before directing the PMIC to enter the STANDBY state. The selection of the VSW*x*_STBY[7:0] bits will depend on the system requirements of the specific low-power mode it wants to achieve at system level.

Table 126. SW2 voltage setting

VSWx_RUN[7:0] VSWx_STBY[7:0]	Voltage setting
0x00	0.30000V
0x01 to 0x91	0.45000 V to 1.35000 V in 6.25 mV steps
0x92 to 0x9E	Reserved
0x9F	1.50000 V
0xA0 to 0xD8	1.80000 V to 2.50000 V in 12.5 mV steps
0xD9 to 0xDF	Reserved
0xE0 to 0xF4	2.80000 V to 3.30000 V in 25.0 mV steps
0xF5 to 0xFF	Reserved

DVS is available under the following conditions:

1. DVS range is between 0.65 V and 0.9 V.
2. The OV/UV threshold is +/-5 % or wider.
3. The DVS ramp must be 3.9 mV/µs or slower.

The VSW*x*_RUN[7:0] and VSW*x*_STBY[7:0] bits are designed as secure write bits to ensure that output voltages are not changed by mistake during the SYSTEM ON states.

The OTP_SW*x*_DVS[1:0] bits are used to program the default slew rate for the SW regulator turn-on and turn-off ramps. During the SYSTEM ON states, the DVS range is between 0.65 V and 0.9 V, with an OV/UV threshold of 5 % or wider and a DVS ramp of 3.9 mV/µs or slower. The SYSTEM ON DVS rate is controlled by the SW*x*_DVS[1:0] bits on the functional registers.

Table 127. SWx ramp-down configuration

SW*x*_DVS[1:0]	Clocking factor	SW*x* ramp-up slope rate[1][2]	SW*x* ramp-down slope rate[1][2]
00	8	1.95 mV/µs	1.95 mV/µs
01	4	3.9 mV/µs	3.9 mV/µs
10	2	7.8 mV/µs	7.8 mV/µs
11	1	15.6 mV/µs	15.6 mV/µs

[1] At 20 MHz high-frequency clock selection
[2] The slope rate is calculated as (6.25 [mV] * FREQ [MHz]) / (8 * clocking factor).

In applications where the output capacitance is larger than the recommended value, the SWx_SLOWDVS bit provides the option to force the ramp-down slope to the slowest discharge speed, to ensure the output is able to fully discharge before a new turn-on cycle is started.

The SWx_SLOWDVS bit is reset to 1 at power-up and the MCU can modify it during the SYSTEM ON states if the system requires a faster discharge on the SWx regulator.

Table 128. Ramp-down DVS

SW*x*_SLOWDVS	Ramp-down DVS
0	Same as ramp up
1	1.95 mV/µs

The SWx regulator is only allowed to request a dynamic voltage change when the default OTP value is set to be within the DVS range (0.3 V to 1.35 V). A voltage configuration outside of the DVS range will be changed to the default OTP value, and any voltage change requested via the I^2C communication will be ignored to avoid an invalid configuration.

The OTP_SW*x*_DVSMAX[3:0] bits are provided to define the maximum high-voltage delta allowed during a DVS transition. Maximum high-voltage delta is calculated with respect to the default voltage setting selected by the OTP_VSW*x*_RUN[7:0] bits, to ensure the system is not able to request a voltage change outside of the selected limits defined for a specific application.

Table 129. SWx high-voltage delta

OTP_SWx_DVSMAX[3:0]	SWx high-voltage delta
0000	0.025 V
0001	0.050 V
0010	0.075 V
0011	0.100 V
0100	0.125 V
0101	0.150 V
0110	0.175 V

Table 129. SWx high-voltage delta*...continued*

OTP_SWx_DVSMAX[3:0]	SWx high-voltage delta
0111	0.200 V
1000	0.225 V
1001	0.250 V
1010	0.275 V
1011	0.300 V
1100	0.325 V
1101	0.350 V
1110	0.375 V
1111	0.400 V

If the MCU tries to write a voltage value in SW*x* higher than the OTP_SW*x*_DVSMAX[3:0] selection, the controller will ignore the command and send a DVSMAX_I interrupt. The DVSMAX_I interrupt will assert the INTB pin if the interrupt is not masked.

The OTP_SW*x*_DVSMIN[3:0] bits are provided to define the maximum low-voltage delta allowed during a DVS transition. The maximum low-voltage delta is calculated with respect to the default voltage setting selected by the OTP_VSW*x*_RUN[7:0] bits, to ensure the system is not able to request a voltage change outside of the selected limits defined for a specific application.

Table 130. SW1 low-voltage delta

OTP_SWx_DVSMIN[3:0]	SW1 low-voltage delta
0000	0.025 V
0001	0.050 V
0010	0.075 V
0011	0.100 V
0100	0.125 V
0101	0.150 V
0110	0.175 V
0111	0.200 V
1000	0.225 V
1001	0.250 V
1010	0.275 V
1011	0.300 V
1100	0.325 V
1101	0.350 V
1110	0.375 V
1111	0.400 V

If the MCU tries to write a voltage value in SW*x* lower than the OTP_SW*x*_DVSMIN[3:0] selection, the controller will ignore the command and send a DVSMIN_I interrupt. The DVSMIN_I interrupt will assert the INTB pin if the interrupt is not masked.

The SW*x*_RUN_MODE[1:0] bits are provided to change the mode of operation of the SW*x* regulator during the RUN state. If the SW*x* is enabled in the Power-up sequence, the SW*x*_RUN_MODE[1:0] will be set to PWM by default.

Table 131. Mode selection in RUN

SWx_RUN_MODE[1:0]	Mode selection in RUN
00	OFF
01	PWM
10	PFM
11	Reserved

The SW*x*_STBY_MODE[1:0] bits are provided to change the mode of operation of the SW*x* regulator during the STANDBY state.

Table 132. Mode selection in STANDBY

SWx_STBY_MODE[1:0]	Mode selection in STANDBY
00	OFF
01	PWM
10	PFM
11	Reserved

The default value for the SW*x*_STBY_MODE[1:0] bits is loaded at power-up from the OTP_SW*x*_STBY_EN bit.

Table 133. Default SWx mode selection in STANDBY

OTP_SWx_STBY_EN	SWx operation in STANDBY
0	OFF
1	PFM

When the SW*x* regulator changes the mode between the PWM and PFM, The SW*x*_MODE_I interrupt will be generated when the mode transition is finished. The INTB pin will be asserted if the SW*x*_MODE interrupt is not masked.

The SWx_ILIM[1:0] bits are provided to program the current limit detection in the SW*x* regulator. The default current limit is loaded at power up from the OTP_SWx_ILIM[1:0] bits.

Table 134. Current limit selection bits

SWx_ILIM[1:0]	Current limit
00	4.5A
01	2.6A
10	3.0A
11	4.5A

The SWx_PH[2:0] bits are provided to control the phase shift of the switching frequency. The default switching phase is loaded at power up from the OTP_SWx_PH[2:0] bits.

Table 135. SWx phase shift selection bits

SWx_PH[2:0]	Phase control
000	45°

Table 135. SWx phase shift selection bits*...continued*

SWx_PH[2:0]	Phase control
001	90°
010	135°
011	180°
100	225°
101	270°
110	315°
111	0°

13.2.3.1 Multiphase operation

Regulators SW2 and SW3 can be configured for dual-phase operation via the OTP_SW2CONFIG[1:0] bits.

Table 136. SW2 and SW3 multiphase configuration bits

OTP_SW2CONFIG[1:0]	SW2 and SW3 operation
00	Single-phase mode
01	Dual-phase mode
10	Reserved (disabled)
11	Reserved (disabled)

In single-phase mode, SW2 and SW3 operate independently ofeach other.

When SW2 and SW3 are configured in dual-phase mode, SW2 will become the primary channel and will control most of the configuration of the resulting multi-phase channel, with the exception of the phase configuration, which is controlled independently for each channel via the SW2_PH[2:0] and SW3_PH[2:0] bits, respectively.

Regulators SW4 and SW5 can be configured in dual-phase operation via the OTP_SW4CONFIG[1:0] bits. In single-phase mode, SW4 and SW5 operate independently of each other.

Table 137. SW4 and SW5 multiphase configuration bits

OTP_SW4CONFIG[1:0]	SW4 and SW5 operation
00	Single-phase mode
01	Dual-phase mode
10	Reserved (disabled)
11	Reserved (disabled)

When SW4 and SW5 are configured in dual-phase mode, SW4 will become the primary channel and will control most of the configuration of the resulting multi-phase channel, with the exception of the phase configuration, which is controlled independently for each channel via the SW4_PH[2:0] and SW5_PH[2:0] bits, respectively.

13.2.3.2 Electrical characteristics

Table 138. SW2 - SW5 electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, V_{SWxIN} = V_{IN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, and T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{SWxIN}	Operating input range[1] • Minimum headroom = V_{SWxFB} + I_{OUT_MAX} * RON / DC. • I_{OUT_MAX} = minimum ILIM selected for SWx. • RON includes HS FET R_{DSON}, bond wire resistance, PCB trace resistance and inductor DCR. • Maximum duty cycle = 100 %	UVDET	–	5.5	V
f_{SW}	Operating switching frequency	1.9	–	3.15	MHz
$V_{SWxACC3}$	Output voltage accuracy • PWM mode • 0.3 V ≤ V_{SWxFB} < 0.8 V	-10	–	10	mV
$V_{SWxACC1}$	Output voltage accuracy • PWM mode • 0.8 V ≤ V_{SWxFB} ≤ 1.35 V	-1.5	–	1.5	%
$V_{SWxACC2}$	Output voltage accuracy • PWM Mode • 1.5 V ≤ V_{SWxFB} ≤ 3.3 V	-1.5	–	1.5	%
$V_{SWxPFMACC1}$	Output voltage accuracy • PFM mode • 0.3 V ≤ V_{SWxFB} < 0.8 V	-20	–	20	mV
$V_{SWxPFMACC2}$	Output voltage accuracy • PFM mode • 0.8 V ≤ V_{SWxFB} ≤ 1.35 V	-3	–	3	%
$V_{SWxPFMACC3}$	Output voltage accuracy • PFM mode • 1.5 V ≤ V_{SWxFB} ≤ 3.3 V	-3	–	3	%
V_{SWxPP}	Output voltage ripple • PWM mode • Peak-to-peak	–	6	–	mV
I_{SWx}	Nominal current in single phase	2.5	–	–	A
I_{SWDP}	Nominal current in dual phase	5	–	–	A
I_{LIM1_SWx}	Current limit in single phase • SWx_ILIM[1:0] = 01	1.82	2.6	3.25	A
I_{LIM2_SWx}	Current limit in single phase • SWx_ILIM[1:0] = 10	2.28	3	3.7	A
I_{LIM3_SWx}	Current limit in single phase • SWx_ILIM[1:0] = 00 or 11	3.56	4.5	5.4	A
I_{LIM1_SWDP}	Current limit in dual phase • SWx_ILIM[1:0] = 01 (primary phase)	3.64	5.2	6.5	A
I_{LIM2_SWDP}	Current limit in dual phase	4.56	6	7.4	A

Table 138. SW2 - SW5 electrical characteristics*...continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{SWxIN} = V_{IN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, and T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• SWx_ILIM[1:0] = 10 (primary phase)				
I_{LIM3_SWDP}	Current limit in dual phase • SWx_ILIM[1:0] = 00 or 11 (primary phase)	7.12	9	10.8	A
I_{LIMN_SWx}	Negative current limit • Per phase	1	1.5	2.3	A
V_{SOS_SWx}	Startup overshoot • SWx_DVS[1:0] = 11 (15.6 mV/µs) • V_{SWxIN} = 5.0 V , V_{SWxFB} = 1.0 V	-25	25	50	mV
t_{ONMIN_SWx}	Turn-on time • From enable to 90 % of end value • SWx_DVS[1:0] = 11 (15.6 mV/µs) • V_{SWxIN} = 5.0 V, V_{SWxFB} = 0.5 V	32	–	–	µs
t_{ONMAX_SWx}	Maximum turn-on Time • From enable to 90 % of end value • SWx_DVS[1:0] = 00 (1.95 mV/µs) • V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.8 V	–	–	925	µs
$\eta_{SWx\_PWM\_1P8}$	PWM efficiency at full load • Single phase • V_{SWxIN} = 5.0 V , V_{SWxFB} = 1.8 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	86	–	%
$\eta_{SWx\_PWM\_1P8}$	PWM efficiency at 40 % load • Single phase • V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.8 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	90.5	–	%
$\eta_{SWx\_PWM\_1P0}$	PWM efficiency at full load • Single phase • V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	79	–	%
$\eta_{SWx\_PWM\_1P0}$	PWM efficiency at 40% load • Single phase • V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	86	–	%
$\eta_{SWx\_PWM\_0P8}$	PWM efficiency at full load • Single phase • V_{SWxIN} = 5.0 V, V_{SWxFB} = 0.8 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	75	–	%
$\eta_{SWx\_PWM\_0P8}$	PWM efficiency at 40 % load	–	83.5	–	%

Table 138. SW2 - SW5 electrical characteristics*...continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{SWxIN} = V_{IN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, and T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• Single phase • V_{SWxIN} = 5.0V, V_{SWxFB} = 0.8 V • f_{SW} = 2.5 MHz • T_A = 25 °C				
$\eta_{SWx\_PWM\_0P5}$	PWM efficiency at full load • Single phase • V_{SWxIN} = 5.0 V, V_{SWxFB} = 0.5 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	69	–	%
$\eta_{SWx\_PWM\_0P5}$	PWM efficiency at 40 % load • Single phase • V_{SWxIN} = 5.0 V, V_{SWxFB} = 0.5 V • f_{SW} = 2.5 MHz • T_A = 25 °C	–	77	–	%
t_{DB_SWx}	Dead-band time	–	3	5	ns
t_{LXSR1_SWx}	Switching node slew time	–	2.5	–	ns
V_{LOTR1_SWx}	Transient load regulation (single phase) • 0.5 V ≤ V_{SWxFB} ≤ 1.35 V • I_{STEP} = 200 mA to 1.0 A, di/dt = 2.0 A/µs • C_{OUT} = 44 µF, L_{OUT} = 0.47 µH, f_{SW} = 2.5 MHz • V_{SWxIN} = 5.0 V	-25	–	25	mV
V_{LOTR2_SWx}	Transient load regulation (sngle phase) • 1.5 V ≤ V_{SWxFB} ≤ 3.3 V • I_{STEP} = 200 mA to 1.0 A, di/dt = 2.0 A/µs • C_{OUT} = 44 µF, L_{OUT} = 0.47 µH, f_{SW} = 2.5 MHz • V_{SWxIN} = 5.0 V	-3	–	3	%
V_{LOTR1_SWxDP}	Transient load regulation (dual phase) • 0.5V ≤ V_{SWxFB} ≤ 1.35 V • I_{STEP} = 400 mA to 2.0A, di/dt = 4.0 A/µs • C_{OUT} = 44 µF (per phase) • L_{OUT} = 0.47 µH • f_{SW} = 2.5 MHz • V_{SWxIN} = 5.0 V	-25	–	25	mV
V_{LOTR2_SWxDP}	Transient load regulation (dual phase) • 1.5 V ≤ V_{SWxFB} ≤ 3.3 V • I_{STEP} = 200 mA to 2.0 A, di/dt = 4.0 A/µs • C_{OUT} = 44 µF (per phase) • L_{OUT} = 0.47 µH • f_{SW} = 2.5 MHz • V_{SWxIN} = 5.0V	-3	–	3	%
I_{QPFM_SWx}	PFM quiescent current • PFM mode (not switching) • Max IQ at TA = 85 °C	–	15	20	µA

Table 138. SW2 - SW5 electrical characteristics...*continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{SWxIN} = V_{IN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, typical external component values, f_{SW} = 2.5 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 0.5 A, and T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
$t_{PFM2PWM\_SWx}$	PFM to PWM transition time	10	–	50	µs
R_{DS25_SWxHS}	High-side FET R_{DSON}[2] • T_J = 25°C • Including bond-wire and package resistance	–	60	–	mΩ
R_{DS125_SWxHS}	High-side FET R_{DSON}[2] • T_J = 125°C • Including bond-wire and package resistance	–	75	–	mΩ
R_{DS25_SWxLS}	Low-side FET R_{DSON}[3] • T_J = 25°C • Including bond-wire and package resistance	–	32	–	mΩ
R_{DS125_SWxLS}	Low-side FET R_{DSON}[3] • T_J = 125°C • Including bond-wire and package resistance	–	42	–	mΩ
R_{DIS_SWx}	Discharge-resistance • Regulator disabled and ramp completed	20	60	100	Ω

[1] UVDET represents the minimum functional level for the PF09; VSW1IN must meet the minimum headroom to ensure proper output voltage regulation.
[2] Typical high-side FET resistance due to packaging (bondwire + metal) at room temp is 24 mΩ.
[3] Typical low-side FET resistance due to packaging (bondwire + metal) at room temp is 21 mΩ.

Table 139. SWx recommended external components.

Symbol	Description	Min	Typ	Max	Units
L	Output inductor • Nominal inductor DC resistance < 24 mΩ • Minimum saturation current at full load: 5.5 A	–	0.47	–	µH
C_{OUT}	Effective output capacitance • x 22 µF, 6.3 V • Low ESR ceramic capacitor.	22	44	300	µF
C_{IN}	Input capacitor • 4.7 µF, 10 V • Low ESR ceramic capacitor	4.23	4.7	5.17	µF

13.2.4 LDO1 (500 mA linear regulator with load switch mode)

LDO1 is a low dropout linear regulator with 500 mA current capability and input voltage range from 1.8 V to 5.5 V. It provides programmable output voltage between 0.75 V and 3.3 V, with up to 2 % output voltage accuracy.

The LDO1 output implements a configurable soft-start ramp control during power up (enable) and discharge mechanism during power down (disable).

The LDO1_RUN_EN bit is provided to enable or disabled the LDO1 output during the RUN state. The LDO1_RUN_EN bit will be set to 1 by default, if the LDO is enabled in the Power-up sequence, or 0 if it is disabled at power up.

Table 140. LDO1 output control in RUN

LDO1_RUN_EN	LDO1 output control
0	Disabled
1	Enable

The LDO1_STBY_EN bit is provided to enable or disable the LDO1 output during the STANDBY state, and its default value is loaded from the OTP_LDO1_STBY_EN bit at power up.

Table 141. LDO1 output control in STANDBY

LDO1_STBY_EN	LDO1 output control
0	Disabled
1	Enable

The VLDO1_RUN[4:0] and VLDO1_STBY[4:0] bits are provided to set the output voltage of the LDO1 during the RUN and STANDBY states respectively. The default values for the VLDO1_RUN[4:0] and VLDO1_STBY[4:0] bits are loaded from the respective OTP_VLDO1_RUN[4:0] and OTP_VLDO1_STBY[4:0] bits at power up.

LDO output voltage can be changed during the RUN mode operation. Maximum voltage step at the transition is +/-2 V.

Table 142. LDO1 output voltage selection bits

VLDO1_RUN[4:0] VLDO1_STBY[4:0]	LDO1 output voltage
00000	0.75 V
00001	0.80 V
00010	0.85 V
00011	0.90 V
00100	0.95 V
00101	1.00 V
00110	1.05 V
00111	1.10 V
01000	1.15 V
01001	1.20 V
01010	1.25 V
01011	1.30 V
01100	1.35 V
01101	1.40 V
01110	1.45 V
01111	1.50 V
10000	1.80 V
10001	1.90 V
10010	2.00 V
10011	2.10 V

Table 142. LDO1 output voltage selection bits*...continued*

VLDO1_RUN[4:0] VLDO1_STBY[4:0]	LDO1 output voltage
10100	2.20 V
10101	2.30 V
10110	2.40 V
10111	2.50 V
11000	2.60 V
11001	2.70 V
11010	2.80 V
11011	2.90 V
11100	3.00 V
11101	3.10 V
11110	3.20 V
11111	3.30 V

The LDO1 features a programmable soft-start time to set a fixed ramp-up time, regardless of the output voltage level. The ramp-up time is selected in OTP via the OTP_LDO1_SS bit.

Table 143. LDO1 soft-start selection bit

OTP_LDO1_SS	LDO1 ramp
0	Slow ramp
1	Fast ramp

13.2.4.1 Load switch mode

The OTP_LDO1LS bit is provided to allow the LDO to operate in load switch configuration

Table 144. LDO1 load switch selection mode

OTP_LDO1LS	LDO1 operating mode
0	LDO mode
1	Load switch mode

In load switch mode, the block is capable of taking an input as low as 1.8 V and enabling the output in the Power-up sequence, or enabling the output manually via the LDO1_RUN_EN and LDO1_STBY_EN bits.

When the LDO1 is operating in load switch mode, the monitoring voltage level is set by the VLDO1_RUN[4:0] and the VLDO1_STBY[4:0] bits in the RUN and Monitored STANDBY states respectively. It is responsibility of the system designer to set the voltage monitoring setpoint and the OV/UV monitoring threshold to a proper level, to account for DC losses in the pass FET.

13.2.4.2 Electrical characteristics

Table 145. LDO1 electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, V_{LDO1IN} = 1.8 V to 5.5 V, V_{IN} = UVDET to 5.5 V, V_{LDO1} = 3.3 V, I_{LDO1} = 500 mA, and typical external component values unless otherwise noted. Typical values are characterized at V_{LDO1IN} = 5.0 V, V_{LDO1} = 3.3 V, I_{LDO1} = 500 mA, T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{LDO1IN}	Operating input voltage range • 0.75 V ≤ V_{LDO1} ≤ 1.3 V	1.8	–	5.5	V
V_{LDO1IN}	Operating input voltage range • 1.35 V ≤ V_{LDO1} < 3.3 V	2.5	–	5.5	V
V_{HDR_LDO1}	Minimum input headroom	300	–	–	mV
V_{ACC_LDO1}	Output voltage accuracy • 0.75 V ≤ V_{LDO1} ≤ 1.3 V	-2.5	–	2.5	%
V_{ACC_LDO1}	Output voltage accuracy • 1.35 V ≤ V_{LDO1} ≤ 3.3 V	-2	–	2	%
V_{LOR_LDO1}	Load regulation	–	0.1	0.2	mV/mA
V_{LIR_LDO1}	Line regulation	–	–	20	mV
I_{LDO1}	LDO1 nominal current	500	–	–	mA
I_{LIM_LDO1}	Current limit	550	–	900	mA
I_{Q_LDO1}	Quiescent current	–	10	20	µA
R_{DSON_LDO1}	Drop-out/load switch resistance. R_{DSON} does not include the bonding wire and package resistance. @VLDOx = 3.3 V, ILDOx = 500 mA See Figure 25.	–	150	250	mΩ
R_{DSON_LDO1}	Drop-out/load switch resistance. R_{DSON} including the bonding wire and package resistance. VLDOx = 3.3 V, ILDOx = 500 mA. See Figure 25.	–	–	300	mΩ
$LDO1_{PSRR\_DC}$	DC power supply rejection ratio • 100 µA < I_{LDO1} ≤ 500 mA • V_{LDO1IN} = V_{LDO1} + 300 mV	50	–	–	dB
$LDO1_{PSRR\_AC}$	AC power supply rejection ratio • 400 kHz • 100 µA < ILDO1 ≤ 500 mA • VLDO1IN = VLDO1 + 300 mV	20	–	–	dB
t_{SS0_LDO1}	LDO1 soft-start time • From 10 % to 90 % of target voltage. • OTP_LDO1_SS = 0	320	–	520	µs
t_{SS1_LDO1}	LDO1 soft-start time • From 10 % to 90 % of target voltage. • OTP_LDO1_SS = 1	140	–	270	µs
t_{EN_LDO1}	LDO1 enable time • From enable signal to 10 % of target voltage. • V_{LDO1} = 3.3 V	–	–	125	µs

Table 145. LDO1 electrical characteristics*...continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{LDO1IN} = 1.8 V to 5.5 V, V_{IN} = UVDET to 5.5 V, V_{LDO1} = 3.3 V, I_{LDO1} = 500 mA, and typical external component values unless otherwise noted. Typical values are characterized at V_{LDO1IN} = 5.0 V, V_{LDO1} = 3.3 V, I_{LDO1} = 500 mA, T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
t_{OFF_LDO1}	Turn-off time • Output disabled to 10 % of initial value • V_{LDO1} = 3.3 V • I_{LDO1} = 0.0 mA • C_{OUT} = 2.2 µF	–	650	–	µs
V_{OS_LDO1}	Startup overshoot	–	–	2	%
V_{LOTR_LDO1}	Load transient response • I_{LDO1} = 200 mA step in 2.0 µs	-2	–	-2	%
t_{ON_LS1}	Load switch turn-on rise time	–	150	300	µs
I_{LIM_LS1}	Load switch mode current limit	550	–	900	mA
R_{PD_LDO1}	Output discharge resistor	–	60	100	Ω
R_{TBB_LDO1}	LDO DEBUG pulldown resistance – used to detect pin lift or pin disconnection • V_{DDOTP} > 3.0 V and in DBGOFF state	1	2	–	kΩ

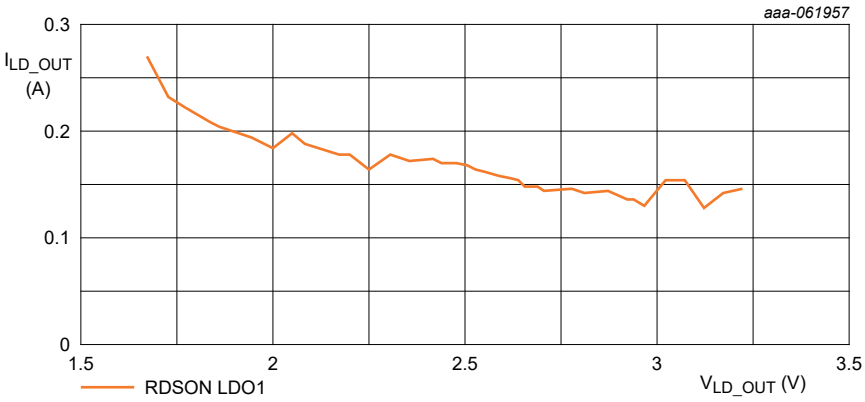


Figure 25. R_{DSON} vs. VLDOUT for LDO1

Table 146. LDO1 recommended external components.

Symbol	Description	Min	Typ	Max	Units
C_{OUT}	Effective output capacitance • 4.7 µF, 6.3 V (+/- 50 % variation) • X7R low ESR ceramic capacitor.	2.3	4.7	7	µF
C_{IN}	Input capacitor • 1 µF, 10 V • X7R Low ESR ceramic capacitor	0.5	1	2	µF

13.2.5 LDO2 / LDO3 (200 mA linear regulators with load switch mode)

LDO2 and LDO3 are low dropout linear regulators with 200 mA current capability and input voltage range from 1.8 V to 5.5 V. Both LDOs feature a programmable output voltage between 0.65 V and 3.3 V with up to 2 % output voltage accuracy.

Each LDO implements a configurable soft-start ramp control during power up (enable) and discharge mechanism during power down (disable).

The LDO*x*_RUN_EN bit is provided to enable or disabled the LDOx output during the RUN state. The LDOx_RUN_EN bit will be set to 1 by default if the LDO is enabled in the power-up sequence or 0 if it is disabled at power-up.

Table 147. LDOx output control in RUN

LDOx_RUN_EN	LDOx output xontrol
0	Disabled
1	Enable

The LDOx_STBY_EN bit is provided to enable or disable the LDO*x* output during the STANDBY state, and its default value is loaded from the OTP_LDO*x*_STBY_EN at power-up.

Table 148. LDOx output control in STANDBY

LDOx_STBY_EN	LDOx output control
0	Disabled
1	Enable

The VLDO*x*_RUN[4:0] and VLDO*x*_STBY[4:0] bits are provided to set the output voltage of the LDO*x* during the RUN and STANDBY states respectively.

The default values for the VLDO*x*_RUN[4:0] and VLDO*x*_STBY[4:0] bits are loaded from the respective OTP bits (OTP_VLDO*x*_RUN[4:0] and OTP_VLDO*x*_STBY[4:0]) at power up.

LDO output voltage can be changed during RUN mode operation. The maximum voltage step at the transition is +/-2 V.

Table 149. LDOx output voltage selection bits

VLDO*x*_RUN[4:0] VLDO*x*_STBY[4:0]	LDOx output voltage
00000	0.65 V
00001	0.70 V
00010	0.75 V
00011	0.80 V
00100	0.85 V
00101	0.90 V
00110	0.95 V
00111	1.00 V
01000	1.05 V
01001	1.10 V
01010	1.15 V
01011	1.20 V

Table 149. LDOx output voltage selection bits*...continued*

VLDO*x*_RUN[4:0] VLDO*x*_STBY[4:0]	LDOx output voltage
01100	1.25 V
01101	1.30 V
01110	1.40 V
01111	1.50 V
10000	1.80 V
10001	1.90 V
10010	2.00 V
10011	2.10 V
10100	2.20 V
10101	2.30 V
10110	2.40 V
10111	2.50 V
11000	2.60 V
11001	2.70 V
11010	2.80 V
11011	2.90 V
11100	3.00 V
11101	3.10 V
11110	3.20 V
11111	3.30 V

The LDOx features a programmable soft-start time to set a fixed ramp-up time regardless of the output voltage level. The ramp-up time is selected in OTP via the OTP_LDO*x*_SS bit.

Table 150. LDOx soft-start selection bit

OTP_LDOx_SS	LDOx ramp
0	Slow ramp
1	Fast ramp

Both LDO2 and LDO3 are provided with various modes of operation to address different systems. The mode of operation is selected on OTP via the OTP_LDOx_MODE[1:0] bits.

Table 151. LDOx load switch selection mode

OTP_LDOx_MODE[1:0]	LDOx operating mode
00	LDO mode
01	LDO bypass mode
10	Load switch mode
11	External VMON mode

13.2.5.1 Load switch mode

In load switch mode, the LDO works as an ON/OFF load switch controlled by the LDOx_RUN_EN, LDOx_STBY_EN and LDOx_SEQ[7:0] bits.

In load switch mode, the block is capable of taking an input as low as 1.8 V and enabling the output in the Power-up sequence or manually via the LDOx_RUN_EN and LDOx_STBY_EN bits.

When the LDOx is operating in the load switch mode, the monitoring voltage level is set by the VLDOx_RUN[4:0] and the VLDOx_STBY[4:0] bits in the RUN and monitored STANDBY states respectively. It is responsibility of the system designer to set the monitoring setpoint and the OV/UV monitoring threshold to a proper level to account for DC losses in the pass FET.

13.2.5.2 External VMON mode

Refer to section LDO2 / LDO3 External VMON Operation for a detailed description of the VMON operation on the LDOx block.

13.2.5.3 LDO bypass mode

The LDO bypass mode is provided to support applications requiring multiple PMICs to supply a complete power architecture where the PF09 is intended to be the main PMIC. In these systems, the PF09 performs control and monitoring of the system voltage supplies during normal operation, as well as driving the full system in the Low-power modes.

In such scenarios, LDOxOUT is intended to serve as an external voltage monitoring input, supervising an external regulator supplying high power to system loads during the RUN state. When the system is ready to enter the STANDBY state, the LDOx output can take over the voltage domain, allowing the system to fully disable the external regulators to minimize power consumption during the low-power operation.

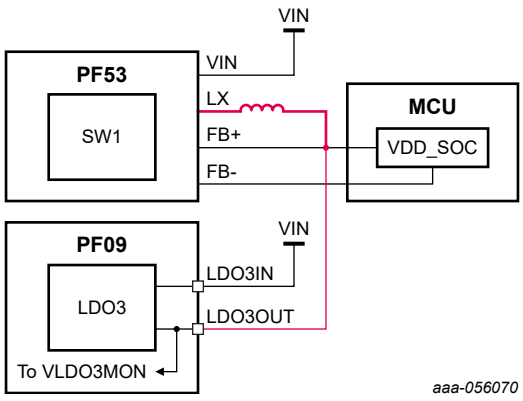


Figure 26. System connection in LDO bypass mode

When the LDO is operating in bypass mode, only the internal VLDOxMON is enabled during the Power-up sequence, and it remains enabled during the RUN state. The VLDOx_RUN[3:0] bits will be used to set the monitoring voltage level to be expected at the LDOxOUT pin.

When the LDOx block is enabled in bypass mode (in the sequence or manually), a programmable blanking time is set via the OTP_VLDOxMON_TSET[1:0] bits, to allow enough time for the external supply to ramp up and settle before allowing OV and UV protection.

Table 152. VLDOxMON blanking time configuration bits

OTP_VLDOxMON_TSET[1:0]	VLDOxMON blanking time
00	250 µs
01	500 µs
10	1000 µs
11	2500 µs

The default blanking time is set in the OTP registers, and it is available only during the LDOx turn-on transition in the Power-up or RUN state, where the LDOx block is operating as a voltage monitor for an external supply.

If the external supply reaches point of regulation before the settling timer has expired, the VLDOxMON will start monitoring right away, even before the blanking timer has ended. Refer to section LDO2 / LDO3 External VMON Operation for a detailed description of the VMON operation on the LDOx block.

If the VLDOxMON voltage selection is changed from one set point to another during the RUN state, the VLDOxMON will use the VLDOxMON_TMASK[1:0] bits to defined the masking timer for the OV and UV fault monitoring while the output voltage transitions to the new expected level.

Table 153. VLDOxMON masking timer

VLDOxMON_TMASK[3:0]	VLDOxMON masking timer
00	500 µs
01	1000 µs
10	2000 µs
11	5000 µs

When the PF09 transitions to the STANDBY state, the LDOx will use the LDOx_STBY_EN bit to decide whether or not to enable the LDOx output to support the low-power operation. If the LDOx_STBY_EN = 1, then the LDOx output will be turned on in the corresponding time slot as set by the VLODx_SEQ[7:0] bits.

When the device goes into the STANDBY state, the operation of the internal voltage monitor (VLDOxMON) will depend on whether the PF09 is in the monitored STANDBY or the low power STANDBY states.

Monitored STANDBY mode (OTP_LP_STBY = 0): in this mode, the LDO output will be monitored internally. During the transition into the Monitored STANDBY state, if the LDOx target voltage in the STANDBY state is lower than the RUN state voltage, the PF09 will apply an internal discharge resistor during the transition to ensure the LDO output is discharged properly and no false OV/UV condition is flagged.

Note: *Because the bypass mode of operation is intended to achieve very low power consumption in the power architecture, it is not recommended to use the Bypass mode when the system is prioritizing system monitoring over current consumption during the STANDBY mode.*

Low-power STANDBY mode (OTP_LP_STBY = 1): in this mode, no voltage monitoring is available and the internal VLDOxMON will be disabled. During the transition to the low-power STANDBY state, the LDOx output will remain tri-stated. Voltage discharge will be performed by the external load, to maximize power utilization in the Low-power mode.

When using the LDOx Bypass mode, it is responsibility of the system integrator to ensure the external voltage regulator is properly disabled in the correct sequence and is able to disable its output with high impedance, in order to allow a seamless transition between the external supply and the LDOx supplying the MCU core domain.

Likewise, the external voltage regulator must support pre-bias turn on conditions to allow proper transition between the voltage regulators.

NXP provides a complete solution to achieve full system power management with low-power support utilizing the PF5x family of devices to supply the high-power external core supply. The following waveforms provide the two possible scenarios when the LDOx is operating in bypass mode.

Scenario #1: the output voltage in RUN and STANDBY is constant; no voltage scaling is required.

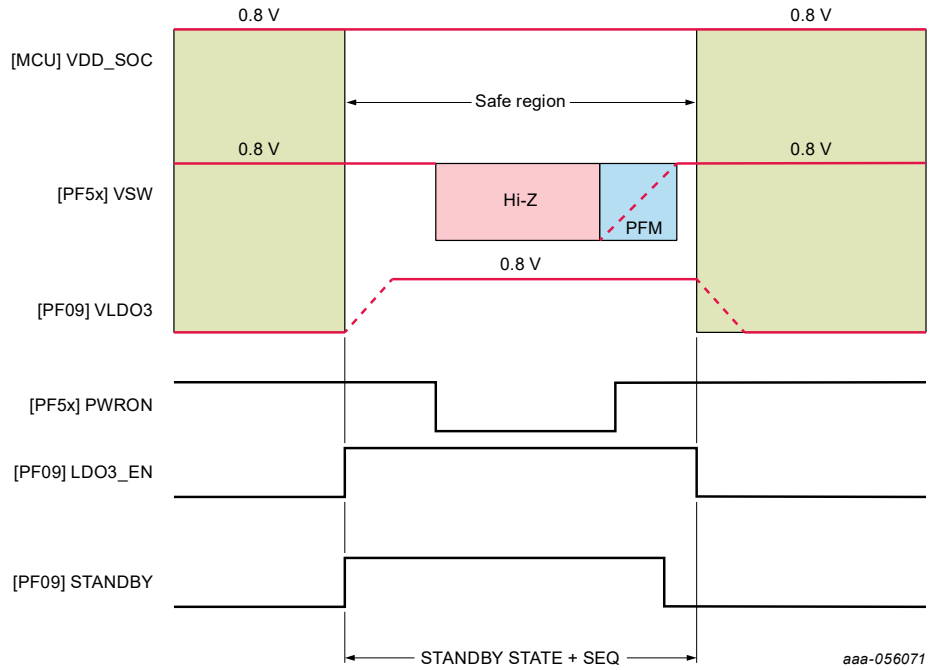


Figure 27. LDOx Bypass mode RUN to STANDBY transition without voltage scaling

Scenario #2 The output voltage in RUN and STANDBY is lower to achieve the lowest power consumption in the system.

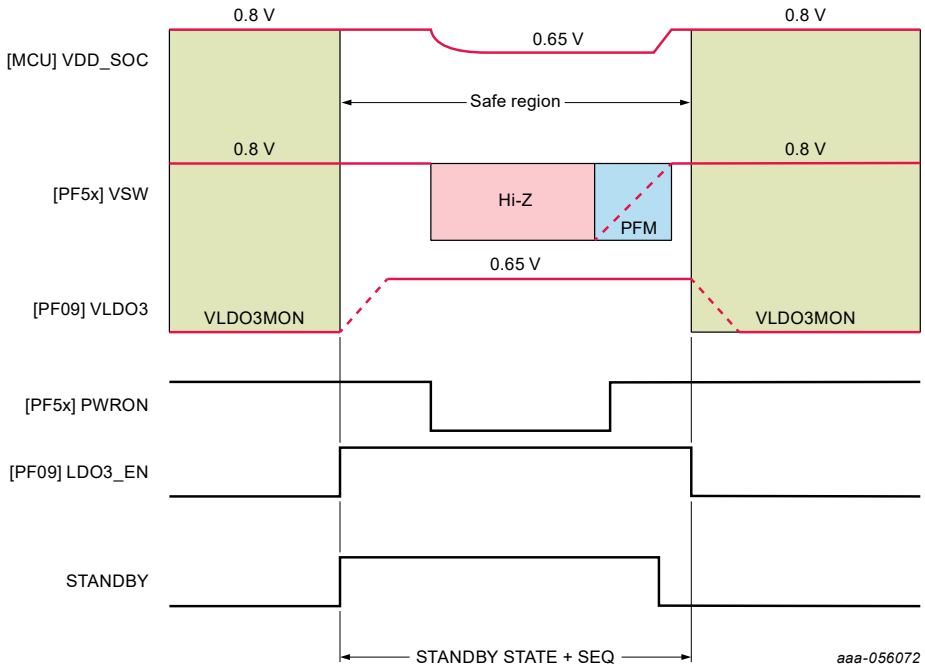


Figure 28. LDOx Bypass mode RUN to STANDBY transition with voltage scaling

13.2.5.4 Electrical characteristics

Table 154. LDO2/LDO3 electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, V_{LDOxIN} = 1.8 V to 5.5 V, V_{IN} = UVDET to 5.5 V, V_{LDOx} = 1.0 V, I_{LDOx} = 200 mA, typical external component values unless otherwise noted. Typical values are characterized at V_{LDOxIN} = 5.0 V, V_{LDOx} = 3.3 V, I_{LDOx} = 200 mA, T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{LDOxIN}	Operating input voltage range • 0.65 V ≤ V_{LDOx} ≤ 1.3 V	1.8	–	5.5	V
V_{LDOxIN}	Operating input voltage range • 1.35 V ≤ V_{LDOx} < 3.3 V	2.5	–	5.5	V
V_{HDR_LDOx}	Minimum input headroom • Valid from 2.5 V ≤ V_{LDOx} < 3.3 V	250	–	–	mV
V_{ACC_LDOx}	Output voltage accuracy • 0.65 V ≤ V_{LDOx} ≤ 1.3 V	-2.5	–	2.5	%
V_{ACC_LDOx}	Output voltage accuracy • 1.35 V ≤ V_{LDOx} < 3.3 V	-2	–	2	%
V_{LOR_LDOx}	Load regulation	–	0.1	0.2	mV/mA
V_{LIR_LDOx}	Line regulation	–	–	20	mV/mA
I_{LDOx}	LDOx nominal current	200	–	–	mA
I_{LIM_LDOx}	Current limit	250	–	450	mA
I_{Q_LDOx}	LDOx quiescent current	–	10	20	µA

Table 154. LDO2/LDO3 electrical characteristics*...continued*

All parameters are specified at T_A = -40 °C to 125 °C, V_{LDOxIN} = 1.8 V to 5.5 V, V_{IN} = UVDET to 5.5 V, V_{LDOx} = 1.0 V, I_{LDOx} = 200 mA, typical external component values unless otherwise noted. Typical values are characterized at V_{LDOxIN} = 5.0 V, V_{LDOx} = 3.3 V, I_{LDOx} = 200 mA, T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
R_{DSON_LDOx}	Drop-out/load switch resistance R_{DSON} does not include the bonding wire and package resistance. @VLDO1 = 3.3 V, ILDO1 = 200 mA	–	300	450	mΩ
R_{DSON_LDOx}	Drop-out/load switch resistance R_{DSON} including the bonding wire and package resistance. VLDOx = 3.3 V, ILDOx = 200 mA	–	–	1000	mΩ
$LDOx_{PSRR\_DC}$	DC power supply rejection ratio • 100 µA < I_{LDOx} ≤ 200 mA • V_{LDOxIN} = V_{LDOx} + 300 mV	55	–	–	dB
$LDOx_{PSRR\_AC}$	AC power supply rejection ratio • 400 kHz • 100 µA < I_{LDOx} ≤ 200 mA • V_{LDOxIN} = V_{LDOx} + 300 mV	20	–	–	dB
t_{SS0_LDOx}	LDOx soft-start time • From 10 % to 90 % of target voltage • OTP_LDOx_SS = 0	320	–	520	µs
t_{SS1_LDOx}	LDOx soft-start time • From 10 % to 90 % of target voltage. • OTP_LDOx_SS = 1	140	–	270	µs
t_{EN_LDOx}	LDOx Enable time • From enable signal to 10% of target voltage. • V_{LDOx} = 3.3 V	–	–	100	µs
t_{OFF_LDOx}	Turn-off time • Output disabled to 10 % of initial value • V_{LDOx} = 3.3 V • I_{LDOx} = 0.0 mA • C_{OUT} = 2.2 µF	–	600	–	µs
V_{OS_LDOx}	Startup overshoot	–	–	2	%
V_{LOTR_LDOx}	Load transient response • I_{LDOx} = 10 mA to 200 mA in 2.0 µs	-2	–	2	%
t_{ON_LSx}	Load switch turn-on rise time	–	150	300	µs
I_{LIM_LSx}	Load switch current limit	200	250	450	mA
R_{PD_LDOx}	Output discharge resistor – used to discharge the output capacitance to help LDOs reach the OV level faster	–	60	100	Ω
R_{PD_DBG}	LDOx DEBUG pulldown resistance - used for pin disconnection detection • V_{DDOTP} > 3.0 V and in DBGOFF State	1	2	–	kΩ

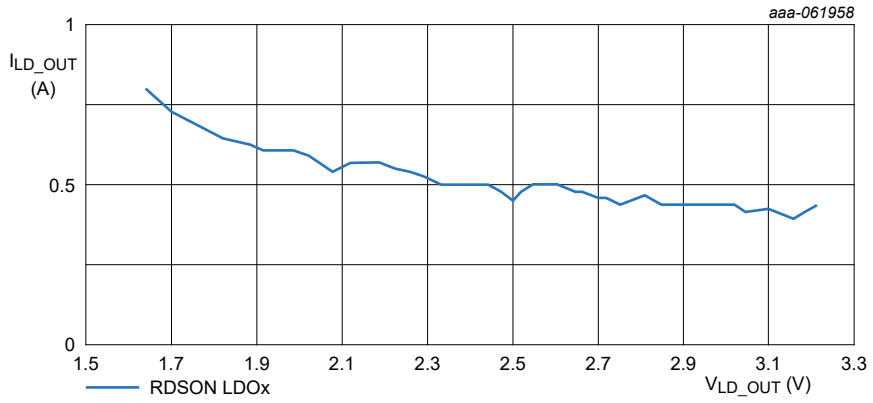


Figure 29. RDSON vs. VLDOUT for LDO2/LDO3

Table 155. Recommended external components.

Symbol	Description	Min	Typ	Max	Units
C_{OUT}	Effective output capacitance • 4.7 µF, 6.3 V (+/-50 % variation) • X7R low ESR ceramic capacitor.	2.2	4.7	7	µF
C_{IN}	Input capacitor • 1 µF, 10 V • X7R ow ESR ceramic capacitor	0.5	1	2	µF

13.3 Voltage monitoring

13.3.1 System-on monitoring

Each voltage regulator in the PF09 features an internal voltage monitor (VMON) capable of monitoring and handling undervoltage and overvoltage conditions in their corresponding outputs.

Each VMON is supplied from an independent reference generation block to provide a high level of independence between the voltage generation and the voltage monitoring circuits.

The internal VMONs are available during the RUN and monitored STANDBY states to detect real-time OV/UV voltages, and they will be used during the Power-up sequence to detect when regulators have reached the point of regulation and ensure the system is placed out of reset only after all voltage regulators are operating properly.

In the Low-power STANDBY state (OTP_LP_STBY = 1), internal voltage monitors will be disabled in order to achieve the lowest quiescent current during this mode.

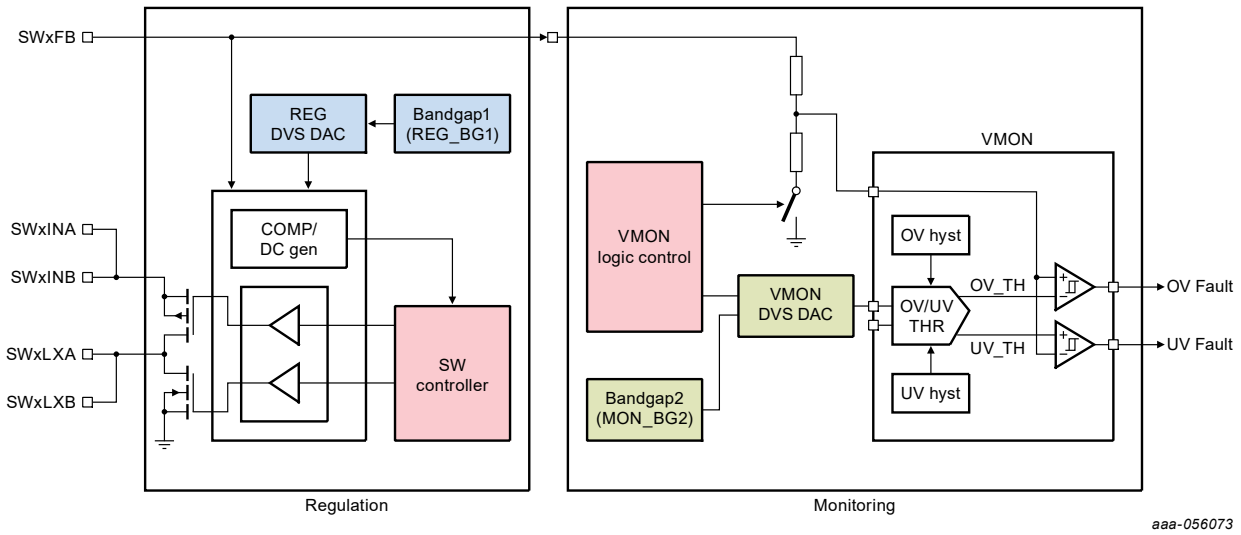


Figure 30. SW regulator VMON architecture

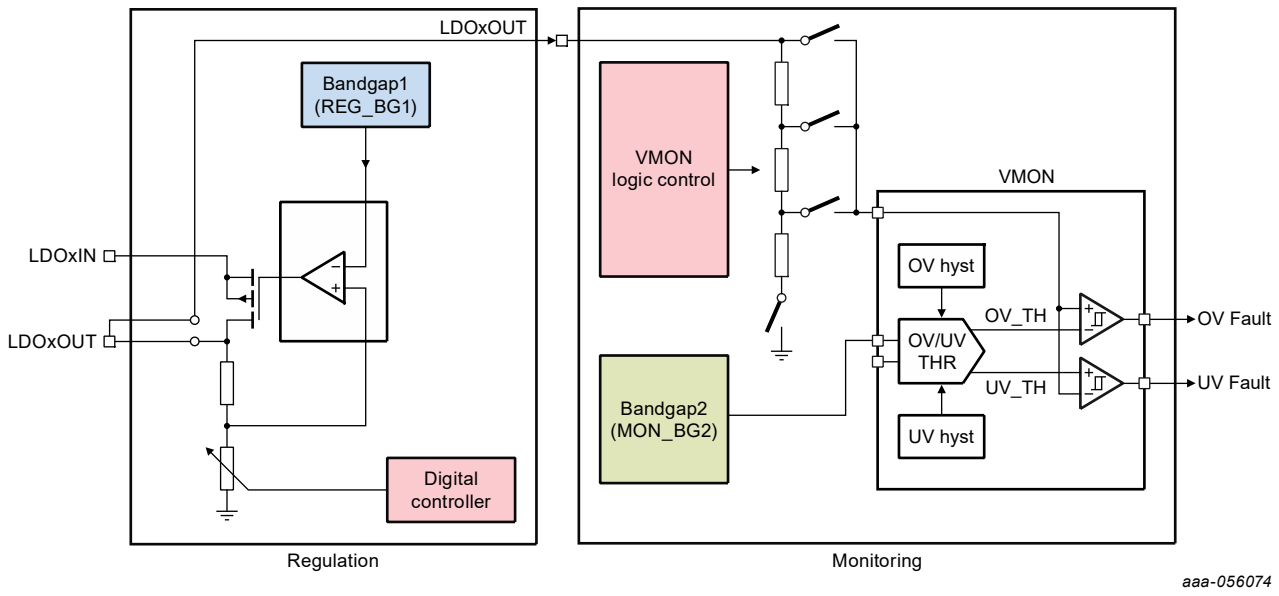


Figure 31. LDO VMON architecture

The undervoltage (UV) monitoring threshold for the switching regulators (SW1- SW5) is set in the OTP registers via the OTP_SWx_UVTH[2:0] bits.

Table 156. SWx UV threshold configuration bits

OTP_SWx_UVTH[2:0]	UV threshold
000	97.5%
001	97.0%
010	96.5%
011	96.0%

Table 156. SWx UV threshold configuration bits*...continued*

OTP_SWx_UVTH[2:0]	UV threshold
100	95.5%
101	95.0%
110	94.5%
111	94.0%

The overvoltage (OV) monitoring threshold for the switching regulators is set in the OTP registers via the OTP_SWx_OVTH[2:0] bits.

Table 157. SWx OV threshold configuration bits

OTP_SWx_OVTH[2:0]	OV threshold
000	102.5%
001	103.0%
010	103.5%
011	104.0%
100	104.5%
101	105.0%
110	105.5%
111	106.0%

For safety considerations, the OV/UV monitoring thresholds are selected in OTP during the part number configuration phase, and they are not allowed to be changed during system operation. However, the system can choose to open the monitoring range during the Monitored STANDBY state, to accommodate larger DC/AC output voltage accuracy on the SWx regulators due to the PFM operation.

The SWx_UVTH_STBY and SWx_OVTH_STBY bits are provided to select whether to use the same OV/UV monitoring threshold in RUN and STANDBY states or force the maximum OV/UV monitoring threshold during the STANDBY state.

Table 158. SWx UV threshold configuration bits during STANDBY

SWx_UVTH_STBY	UV threshold in STANDBY
0	Same as RUN state
1	Open to maximum threshold

Table 159. SWx OV threshold configuration bits during STANDBY

SWx_OVTH_STBY	OV threshold in STANDBY
0	Same as RUN state
1	Open to maximum threshold

By default, the SWx_UVTH_STBY and SWx_OVTH_STBY bits are set to 1 at power up, and the MCU can modify their values before requesting access to the STANDBY states.

The undervoltage monitoring threshold for the LDO regulators is set in the OTP registers via the OTP_LDOx_UVTH[2:0] bits.

Table 160. LDOx UV threshold configuration bits

OTP_LDOx_UVTH[2:0]	UV threshold
000	96.5 %
001	96.0 %
010	95.5 %
011	95.0 %
100	94.5 %
101	94.0 %
110	93.5 %
111	93.0 %

The overvoltage monitoring threshold for the LDO regulators is set in the OTP registers via the OTP_xxx_OVTH[2:0] bits.

Table 161. LDOx OV threshold configuration bits

OTP_LDOx_OVTH[2:0]	OV threshold
000	103.5 %
001	104.0 %
010	104.5 %
011	105.0 %
100	105.5 %
101	106.0 %
110	106.5 %
111	107.0 %

The UV and OV thresholds represent percentages of the nominal voltage programmed on each regulator. Settng the thresholds ensures that an undervoltage condition below the selected UV threshold or an overvoltage condition above the selected OV threshold will always be detected by the VMON circuit.

OV/UV monitoring for all SWx and LDOx regulator are provided with a hysteresis to prevent multiple fault detection on borderline conditions, however, because the SW regulators offer very tight monitoring as low as 2.5% of the nominal voltage selection, the PF09 provides the OTP_SWx_2P5TH_HYS bits to disable the hysteresis in the +/-2.5% monitoring threshold in order to avoid potential overlapping conditions between the voltage accuracy and the monitoring threshold accuracy specifications.

Table 162. Hysteresis on 2.5 % OV/UV threshold configuration bits

OTP_SWx_2P5TH_HYS	Hysteresis on 2.5 % OV/UV threshold
0	Disabled
1	Enabled

On part numbers using the 2.5% OV/UV monitoring threshold without hysteresis, it is recommended to select larger OV/UV debounce times to minimize multiple fault detection due to oscillating borderline conditions.

The debounce time required for an OV condition to be detected can be programmed in the functional register via the OV_DBNC[1:0] bits. The OV debounce time is global for all voltage monitors, and, by default, the configuration, is reset to the lowest condition (0b00) at power up. The MCU must configure the actual value

needed by the system during the system configuration stage to ensure no false OV conditions are detected during safe system operation.

Table 163. OV debounce time configuration bits

OV_DBNC[1:0]	OV debounce time
00	25 µs
01	50 µs
10	80 µs
11	125 µs

The debounce time required for an UV condition to be detected can be programmed in the functional register via the UV_DBNC[1:0] bits. The UV debounce time is global for all voltage monitors, and, by default, the configuration, is reset to the lowest condition (0b00) at power-up. The MCU must configure the actual value needed by the system during the system configuration stage to ensure no false UV conditions are detected during safe system operation.

Table 164. UV debounce time configuration bits

UV_DBNC[1:0]	UV debounce time
00	5 µs
01	15 µs
10	25 µs
11	40 µs

13.3.1.1 VMON during SW1 load switch operation

When the SW1 is programmed in load switch mode, the PF09 is expected to have a 3.3 V input supply and the output of the SW1LS is expected to follow the 3.3 V minus the DC voltage drop due to the current going through the SW1LS pass FET.

The system designer must select the proper voltage monitoring level during the RUN and the Monitored STANDBY states via the VSW1_RUN[7:0] and VSW1_STBY[7:0] bits respectively. Likewise, the system must provide adequate OV/UV thresholds to account for the voltage drop due to DC losses in the pass FET.

OV/UV monitoring thresholds for the load switch operation are configured in the OTP registers via the OTP_SW1_OVTH[2:0] and OTP_SW1_UVTH[2:0] bits.

13.3.1.2 VMON during LDOx load switch operation

When the LDOx is programmed in load switch mode, the LDO block is capable of receiving an input supply between 1.8 V and 3.3 V, and the output of the LDOxLS is expected to follow the input voltage minus the DC voltage drop due to the current going through the LDOxLS pass FET.

The system designer must select the proper voltage monitoring level during the RUN and the Monitored STANDBY states via the VLDOx_RUN[4:0] and VLDOx_STBY[4:0] bits respectively. Likewise, the system must provide adequate OV/UV thresholds to account for the voltage drop due to DC losses in the pass FET.

OV/UV monitoring thresholds for the load switch operation are configured in the OTP registers via the OTP_LDOx_OVTH[2:0] and OTP_LDOx_UVTH[2:0] bits.

13.3.2 VAON monitoring

The VAON regulator is provided with two internal monitoring circuits to ensure proper monitoring and reaction during the full operation of the system, maintaining minimum power consumption during the Low-power mode, and providing proper coverage for the safety requirements to maintain circuit independence during the safety-critical operating states.

The following section addresses voltage monitoring during the Power-up sequence, RUN and monitored STANDBY states supported by the programmable voltage monitoring circuit with independent reference supply.

VAON monitoring during the OFF states and low-power STANDBY state is performed only by the low-power undervoltage monitor as described in section 16.6.3 VAON Fault Management.

The VAONMON OV/UV debounce time follows the configuration set in the OV_DBNC[1:0] and UV_DBNC[1:0], like all the other regulators.

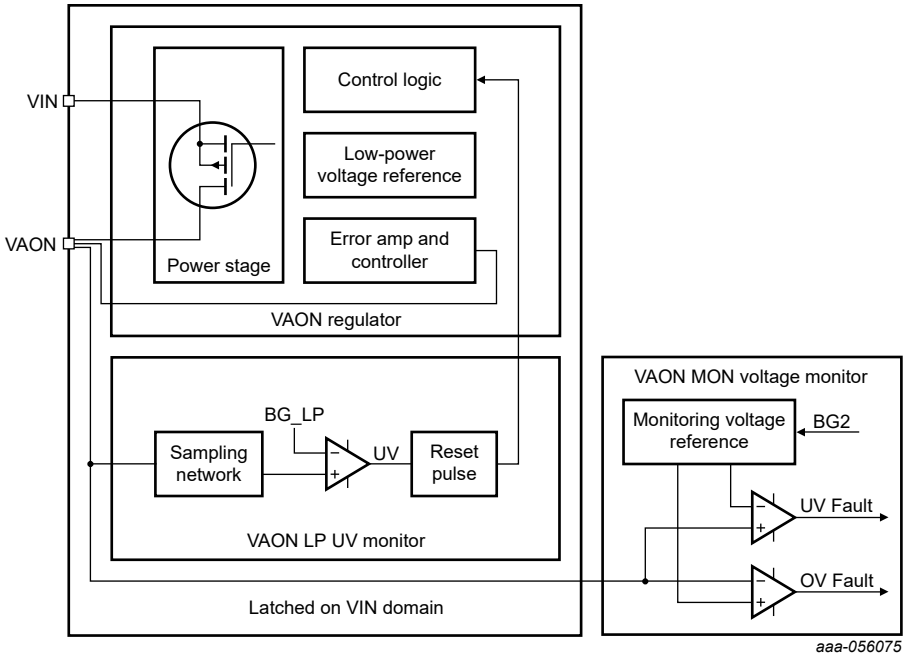


Figure 32. VAON voltage monitoring architecture

The undervoltage monitoring threshold for the VAONMON block is set in the OTP registers via the OTP_VAON_UVTH[1:0] bits.

Table 165. VAON UV threshold configuration bits

OTP_VAON_UVTH[1:0]	VAON UV threshold
00	97 %
01	95 %
10	93 %
11	91 %

The overvoltage monitoring threshold for the VAONMON block is set in the OTP registers via the OTP_VAON_OVTH[1:0] bits.

Table 166. VAON OV threshold configuration bits

OTP_VAON_OVTH[1:0]	VAON OV threshold
00	103 %
01	105 %
10	107 %
11	109 %

13.3.2.1 VAON as always-on regulator

When the VAON regulator is configured as an always-on regulator, the VAONMON block will be used during the DBGOFF state to ensure the VAON is within regulation before the PF09 can start the Power-up sequence.

OV/UV conditions will be detected and debounced based on the configuration bits provided above, and the fault reaction will be performed as described in section 16.6.3 VAON Fault Management.

13.3.2.2 VAON as system regulator

When VAON is operating as a system regulator, the VAONMON is enabled during the Power-up sequence to ensure the system has proper power before placing the MCU out of reset, and it will continue monitoring for OV/UV fault conditions based on the VAONMON configuration shown above.

Fault reaction will be performed as described in section 16.6.2 System Regulators and External VMON Fault Management.

13.3.3 External voltage monitoring

The PF09 features two dedicated external voltage monitors (VMON1 and VMON2) with selectable voltage references, to allow seamless monitoring of an external supply with dynamic voltage scaling (DVS) capability.

Two additional external voltage monitors are available at the LDO2 and LDO3 outputs, if the LDO regulators are not needed in the system.

13.3.3.1 VMON1 / VMON2

VMON1 and VMON2 are dedicated voltage monitors provided to allow the PF09 to monitor up to two external voltages generated outside the device. In such scenarios, the PF09 becomes the main power management safety controller to detect and notify when an OV/UV condition is present in the external voltage supplies.

Each VMON pin is provided with a weak internal pulldown resistor in order to detect a random pin disconnection at the VMONx pin.

The undervoltage monitoring threshold for the VMONx block is set in the OTP registers via the OTP_VMONx_UVTH[2:0] bits.

Table 167. VMONx UV threshold configuration bits

OTP_VMONx_UVTH[2:0]	UV threshold
000	96.5 %
001	96.0 %
010	95.5 %
011	95.0 %
100	94.5 %

Table 167. VMONx UV threshold configuration bits*...continued*

OTP_VMONx_UVTH[2:0]	UV threshold
101	94.0 %
110	93.5 %
111	93.0 %

The overvoltage monitoring threshold for the VMONx block is set in the OTP registers via the OTP_VMONx_OVTH[2:0] bits.

Table 168. VMONx OV threshold configuration bits

OTP_VMONx_OVTH[2:0]	OV threshold
000	103.5 %
001	104.0 %
010	104.5 %
011	105.0 %
100	105.5 %
101	106.0 %
110	106.5 %
111	107.0 %

For safety considerations, the OV/UV monitoring thresholds are selected in OTP during the part number configuration phase, and they are not allowed to be changed during system operation. However, the system can choose to open the monitoring range during the Monitored STANDBY state in order to accommodate larger DC/AC output voltage accuracy on the voltage regulator being monitored by the VMONx block.

The VMONx_UVTH_STBY and VMONx_OVTH_STBY bits are provided to select whether to use the same OV/UV monitoring threshold in RUN and STANDBY states or force the maximum OV/UV monitoring threshold during the STANDBY state.

Table 169. VMONx UV threshold selection in STANDBY

VMONx_UVTH_STBY	UV threshold in STANDBY
0	Same as RUN state
1	Open to maximum threshold

Table 170. VMONx OV threshold selection in STANDBY

VMONx_OVTH_STBY	OV thresholdin STANDBY
0	Same as RUN state
1	Open to maximum threshold

By default, the VMONx_UVTH_STBY and VMONx_OVTH_STBY bits are set to 1 at power up, and the MCU can modify their values before requesting access to the STANDBY states.

The UV and OV thresholds represent percentages of the nominal voltage programmed on each VMON block. Setting the thresholds ensures that an undervoltage condition below the selected UV threshold or an overvoltage condition above the selected OV threshold will always be detected by the VMON circuit.

The VMONx OV/UV debounce time follows the configuration set in the global OV_DBNC[1:0] and UV_DBNC[1:0] bits.

Both VMON1 and VMON2 are capable of monitoring an external voltage supply between 0.5 V and 1.275 V during the RUN and Monitoring STANDBY states by directly connecting the VMONx pin to the voltage monitoring point and setting the corresponding VMONx_RUN[4:0] and VMONx_STANDBY[4:0] bits. The default value for the target monitoring level for the VMONx is configurable in OTP via the OTP_VMONX_RUN[4:0] and OTP_VMONx_STBY[4:0] bits.

Table 171. VMONx monitoring voltage configuration bits

VMONx_RUN[4:0] VMONx_STBY[4:0]	VMONx monitoring voltage
00000	0.5000 V
00001	0.5250 V
00010	0.5500 V
00011	0.5750 V
00100	0.6000 V
00101	0.6250 V
00110	0.6500 V
00111	0.6750 V
01000	0.7000 V
01001	0.7250 V
01010	0.7500 V
01011	0.7750 V
01100	0.8000 V
01101	0.8250 V
01110	0.8500 V
01111	0.8750 V
10000	0.9000 V
10001	0.9250 V
10010	0.9500 V
10011	0.9750 V
10100	1.0000 V
10101	1.0250 V
10110	1.0500 V
10111	1.0750 V
11000	1.1000 V
11001	1.1250 V
11010	1.1500 V
11011	1.1750 V
11100	1.2000 V
11101	1.2250 V

Table 171. VMONx monitoring voltage configuration bits*...continued*

VMONx_RUN[4:0] VMONx_STBY[4:0]	VMONx monitoring voltage
11110	1.2500 V
11111	1.2750 V

In applications where the monitored outputs require dynamic voltage scaling during the system operation, the MCU must manage the voltage transitions in a safe way at the system level.

In order to manage dynamic transition of the external voltage, the VMONx block provides a programmable masking timer to prevent OV/UV conditions from happening during the external voltage transition.

When the VMONx voltage selection is changed from one set point to another, the VMONx masks the OV and UV fault monitoring for a period of time defined by the VMONx_TMASK[1:0] bits. The default value for the masking timer is set in OTP registers via the OTP_VMONx_TMASK[1:0] bits.

Table 172. VMONx masking timer configuration bits

VMONx_TMASK[1:0]	VMONx masking timer
00	500 µs
01	1000 µs
10	2000 µs
11	5000 µs

Because the PF09 does not have control over the DVS transition of the external supply, the MCU must first request a change on the VMON set point and then start the voltage transition on the external voltage supply directly afterwards. The system designer must take communication delays, as well as voltage slew rates, into consideration when selecting the masking time for the VMONx.

The external voltage monitoring pins can also perform monitoring of larger voltage levels by providing an external resistor divider to divide the output voltage to a lower input level suitable to the VMONx pin. The external resistive voltage divider must be calculated in such way that the resulting voltage matches the selected voltage reference set in the VMONx_RUN[4:0] and VMONx_STBY[4:0] bits.

The formula to calculate the resistor divider is described in Figure 33:

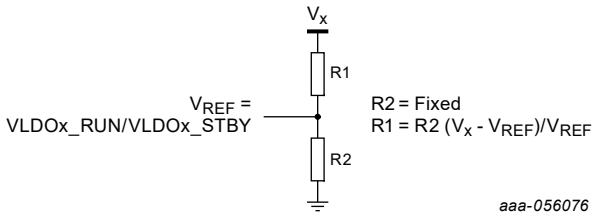


Figure 33. External VMON resistor divider calculation

When using an external resistive voltage divider, no DVS operation is supported on the monitored signal. R2 must be selected between 1 kΩ and100 kΩ and resistor accuracy should be rated 1 % or better to minimize overall monitoring accuracy fallouts.

When the VMONx is not enabled by default in the Power-up sequence, the monitoring block can be enabled manually via the VMONx_EN bit after the external supply has been enabled and is ready to be monitored.

Table 173. VMONx enable bit

VMONx_EN	VMONx monitoring
0	Disabled
1	Enabled

When the VMONx is enabled manually or in the Power-up sequence, a programmable blanking time is provided to allow enough time for the external supply to ramp up and settle before allowing OV and UV monitoring to detect faults. The default blanking timer is set on OTP via the OTP_VMONx_TSET[1:0] bits.

Table 174. VMONx settling time configuration bits

OTP_VMONx_TSET[1:0]	VMONx settling time
00	250 µs
01	500 µs
10	1000 µs
11	2500 µs

13.3.3.2 LDO2 / LDO3 external VMON operation

When the LDO2 or LDO3 is configured as an external voltage monitor (OTP_LDOx_MODE[1:0] = 11) the LDOx output will not be enabled, and the LDOxOUT pin becomes an input to monitor an external voltage supply. In this configuration, a weak internal pulldown resistor is enabled in order to detect a random pin disconnection at the LDOxOUT pin.

The VLDOxMON OV/UV debounce time is set by the global OV_DNBC[1:0] and UV_DBNC[1:0] bits and all other voltage monitoring functions are controlled by the corresponding LDOx bits as follows:

Table 175. LDOx control bits in VMON mode

Bits	VLDOxMON operation
OTP_LDOx_UVTH[2:0]	Set the undervoltage monitoring threshold
OTP_LDOx_OVTH[2:0]	Set the overvoltage monitoring threshold
VLDOx_RUN[4:0]	Set the nominal voltage monitoring level during the RUN state
VLDOx_STBY[4:0]	Set the nominal voltage monitoring level during the Monitoring STANDBY state

Table 176. VLDOxMON monitoring voltage configuration bits

VLDOx_RUN[4:0] VLDOx_STBY[4:0]	VLDOxMON monitoring voltage
00000	External divider VREF = 0.50 V
00001	0.70 V
00010	0.75 V
00011	0.80 V
00100	0.85 V
00101	0.90 V
00110	0.95 V
00111	1.00 V
01000	1.05 V

Table 176. VLDOxMON monitoring voltage configuration bits...*continued*

VLDOx_RUN[4:0] VLDOx_STBY[4:0]	VLDOxMON monitoring voltage
01001	1.10 V
01010	1.15 V
01011	1.20 V
01100	1.25 V
01101	1.30 V
01110	1.40 V
01111	1.50 V
10000	1.80 V
10001	1.90 V
10010	2.00 V
10011	2.10 V
10100	2.20 V
10101	2.30 V
10110	2.40 V
10111	2.50 V
11000	2.60 V
11001	2.70 V
11010	2.80 V
11011	2.90 V
11100	3.00 V
11101	3.10 V
11110	3.20 V
11111	3.30 V

In applications where the monitored output require dynamic voltage scaling during the system operation, the MCU must manage the voltage transitions in a safe way at system level.

In order to manage dynamic transition of the external voltage, the VLDOxMON block provides a programmable masking timer to prevent OV/UV conditions from happening during the external voltage transition.

When the VLDOxMON voltage selection is changed from one set point to another, the VLDOxMON will mask the OV and UV fault monitoring for a period of time defined by the VLDOxMON_TMASK[1:0] bits. The default value for the masking timer is set in OTP registers via the OTP_VLDOxMON_TMASK[1:0] bits.

Table 177. VLDOxMON masking timer configuration bits

VLDOxMON_TMASK[1:0]	VLDOxMON masking timer
00	500 µs
01	1000 µs
10	2000 µs
11	5000 µs

Because the PF09 does not have control over the DVS transition of the external supply, the MCU must first request a change on the VLDOxMON set point and then start the voltage transition on the external voltage supply right after. The system designer must takecommunication delays, as well as voltage slew rates, into consideration when selecting the masking time for the VLDOxMON.

The LDOx as external voltage monitoring pins can also perform monitoring of larger voltage levels by providing an external resistive voltage divider to bring the output voltage to a lower input level suitable for the VLDOxMON inputs.

In order to use the external resistive voltage divider, the VLDOx_RUN[4:0]/VLDOxSTBY[4:0] bits must be set to the lowest option (0b00000). The external resistive voltage divider must be calculated in such way that the resulting voltage matches the V_{REF} = 0.5 V.

The formula to calculate the resistor divider is described in Figure 34:

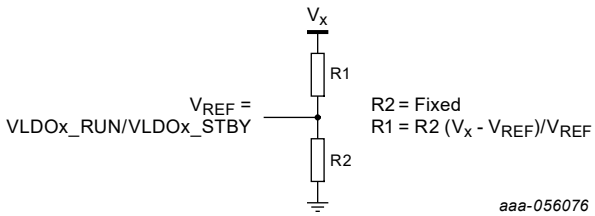


Figure 34. External VLDOxMON resistor divider calculation

When using an external resistive voltage divider, R2 must be selected between 1 kΩ and100 kΩ, and resistor accuracy should be rated 1 % or better to minimize overall monitoring accuracy fallouts.

When the VLDOxMON is not enabled by default in the Power-up sequence, the monitoring block can be enabled manually via the LDOx enable bits after the external supply has been enabled and is ready to be monitored. The LDOxRUN_EN bit is used to enable or disable the voltage monitor in the RUN state, and the LDOxSTBY_EN bit will control the monitoring block during the Monitored STANDBY states.

Table 178. VLDOxMON enable bit

LDOx_RUN_EN	VLDOxMON monitoring
0	Disabled
1	Enabled

When the VLDOxMON is enabled manually, a programmable blanking time is provided to allow enough time for the external supply to ramp up and settle before allowing OV and UV monitoring to detect faults. The OTP_VLDOxMON_TSET[1:0] bit is used to set the settling period after enabling the VLDOxMON block.

Table 179. VLDOxMON settling time configuration bits

OTP_VLDOxMON_TSET[1:0]	VLDOxMON settling time
00	250 µs
01	500 µs
10	1000 µs
11	2500 µs

13.3.4 Electrical characteristics

Table 180. Voltage monitor electrical characteristics

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V, V_{SWxFB} = 3.3 V (SW1), 1.0 V (SW2/SW3), 0.8 V(SW4/SW5), 3.3 V (LDO Regulator), 1.8 V (VAON), and TA = 25 °C unless otherwise noted. MONx applies to all internal voltage monitors: VSWxMON, VLDOxMON, VMONx and VAONMON.

Symbol	Description	Min	Typ	Max	Unit
I_{Q_MONx}	Block quiescent current	–	7	10	µA
t_{ON_MONx}	Voltage monitor settling time after enabled	–	–	30	µs
V_{UVHYS_MONx}	UV hysteresis • voltage difference between UV rising and falling thresholds	0.5	–	1	%
V_{UVACC_MONx}	UV threshold accuracy for Vref ≥ 0.75 V	-1	–	1	%
V_{UVACC_MONx}	UV threshold accuracy for Vref < 0.75 V	-1.5	–	-1.5	%
t_{UVDBN0_MONx}	UV debounce time • UV_DBNC[1:0] = 00	2.5	5	7.5	µs
t_{UVDBN1_MONx}	UV debounce time • UV_DBNC[1:0] = 01	10	15	20	µs
t_{UVDBN2_MONx}	UV debounce time • UV_DBNC[1:0] = 10	20	30	40	µs
t_{UVDBN3_MONx}	UV debounce time • UV_DBNC[1:0] = 11	25	40	55	µs
V_{OVACC_MONx}	OV threshold accuracy for Vref ≥ 0.75 V	-1	–	1	%
V_{OVACC_MONx}	OV threshold accuracy for Vref < 0.75 V	-1.5	–	-1.5	%
V_{OVHYS_MONx}	OV hysteresis • voltage difference between OV rising and falling thresholds	0.5	–	1	%
t_{OVDBN0_MONx}	OV debounce time • OV_DBNC[1:0] = 00	15	25	35	µs
t_{OVDBN1_MONx}	OV debounce time • OV_DBNC[1:0] = 01	35	50	65	µs
t_{OVDBN2_MONx}	OV debounce time • OV_DBNC[1:0] = 10	55	80	105	µs
t_{OVDBN3_MONx}	OV debounce time • OV_DBNC[1:0] = 11	90	125	160	µs
$I_{Q\_VAONMON}$	VAONMON quiescent current	–	7	10	µA
$t_{ON\_VAONMON}$	VAONMON settling time after enabled	–	–	30	µs
$V_{UVHYS\_VAONMON}$	VAONMON UV hysteresis • Voltage difference between UV rising and falling thresholds	1	–	2	%
$V_{UVACC\_VAONMON}$	VAONMON UV threshold accuracy	-2	–	2	%
$t_{UVDBN0\_VAONMON}$	VAONMON UV debounce • UV_DBNC[1:0] = 00	2.5	5	7.5	µs
$t_{UVDBN1\_VAONMON}$	VAONMON UV debounce • UV_DBNC[1:0] = 01	10	15	20	µs

Table 180. Voltage monitor electrical characteristics*...continued*

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V, V_{SWxFB} = 3.3 V (SW1), 1.0 V (SW2/SW3), 0.8 V(SW4/SW5), 3.3 V (LDO Regulator), 1.8 V (VAON), and TA = 25 °C unless otherwise noted. MONx applies to all internal voltage monitors: VSWxMON, VLDOxMON, VMONx and VAONMON.

Symbol	Description	Min	Typ	Max	Unit
$t_{UVDBN2\_VAONMON}$	VAONMON UV debounce • UV_DBNC[1:0] = 10	15	25	35	µs
$t_{UVDBN3\_VAONMON}$	VAONMON UV debounce • UV_DBNC[1:0] = 11	25	40	55	µs
$V_{OVACC\_VAONMON}$	VAONMON OV threshold accuracy	-2	–	2	%
$V_{OVHYS\_VAONMON}$	VAONMON OV hysteresis • Voltage difference between OV rising and falling thresholds	1	–	2	%
$t_{OVDBN0\_VAONMON}$	VAONMON OV debounce • OV_DBNC[1:0] = 00	20	30	40	µs
$t_{OVDBN1\_VAONMON}$	VAONMON OV debounce • OV_DBNC[1:0] = 01	35	50	65	µs
$t_{OVDBN2\_VAONMON}$	VAONMON OV debounce • OV_DBNC[1:0] = 10	55	80	105	µs
$t_{OVDBN3\_VAONMON}$	VAONMON OV debounce • OV_DBNC[1:0] = 11	90	125	160	µs

13.4 Clock management

The PF09 features an advanced clock management scheme, providing top-level control of the internal clock tree generation as well as external clock synchronization. It incorporates various analog blocks managed by a digital clock management interface supporting all the interaction among them.

- Low-power 100 kHz oscillator
- Internal high-frequency oscillator with programmable frequency
- Clock watchdog monitor
- Phase-locked loop (PLL)

13.4.1 High-frequency clock

The PF09 features an internal high-frequency clock with programmable frequency between 16 MHz and 20 MHz. The high-frequency clock provides clocking signals to support various digital functions, and to support the generation of the switching frequency for the five buck converters, when the device is set to operate solely with the internal clock.

The PF09 relies on the high-frequency clock to perform most of the system monitoring during the RUN and Monitored STANDBY states, and it is disabled during the Low-power STANDBY state and other Low-power OFF states to achieve minimum power consumption in these states.

13.4.1.1 Manual frequency tuning

The high-frequency clock is programmable via the CLK_FREQ [3:0] bits, to allow manual frequency tuning from 16 MHz to 24 MHz. When the device is generating the clock for the buck regulators internally, the switching frequency will be proportional to the selected frequency in the internal clock (divided by 8), allowing a selectable switching frequency range from 2 MHz to 3 MHz.

Table 181. Manual frequency tuning

CLK_FREQ[3:0]	High-frequency clock [MHz]	Switching regulator frequency [MHz]
0000	16.0	2.000
0001	17.0	2.125
0010	18.0	2.250
0011	19.0	2.375
0100	20.0	2.500
0101	21.0	2.625
0110	22.0	2.750
0111	23.0	2.875
1000	24.0	3.000
1001 - 1111	Reserved	Reserved

The default operating frequency is set in the OTP registers via the OTP_CLK_FREQ[3:0] bits.

A FREQ_RDY_I interrupt is provided to indicate the frequency has reached the selected target frequency. The frequency-ready interrupt will assert the INTB pin when the interrupt is not masked.

13.4.1.2 Spread spectrum

The internal oscillator features a selectable frequency spread spectrum with +/-10 % wide-frequency spread to help manage EMC in the automotive applications. When the frequency spread-spectrum feature is enabled, the switching regulators are expected to be set in PWM, to take full advantage of the frequency spreading in the switching node.

Frequency spread spectrum is available only when the device is set to generate the switching frequency from the internal frequency clock, and it will be disabled when the external clock synchronization is enabled.

The default enable condition of the spread spectrum is set in the OTP registers via the OTP_FSS_EN bit, and the MCU can enable or disable the spread spectrum during the SYSTEM ON states using the FSS_EN bit.

Table 182. Frequency spread spectrum enable bit

FSS_EN	Frequency spread spectrum
0	Disabled
1	Enabled

When spread spectrum is enabled, the device uses the CLK_FREQ[3:0] bits to select the center frequency for spread spectrum with the following settings:

Table 183. Frequency spread spectrum center frequency selection bits

CLK_FREQ[3:0]	Center frequency with 10% spread spectrum (MHz)
0000	18.0
0001	18.0
0010	18.0
0011	19.0
0100	20.0
0101	21.0

Table 183. Frequency spread spectrum center frequency selection bits*...continued*

CLK_FREQ[3:0]	Center frequency with 10% spread spectrum (MHz)
0110	22.0
0111	22.0
1000	22.0
1001 - 1111	Reserved

Note: *The center clock frequency is clamped at the min/max values to allow the spread spectrum to be performed within the clock frequency limits.*

The FSS_MODE bit is provided to select the type of spread spectrum, and the default operating mode for the spread spectrum is set in the OTP registers via the OTP_FSS_MODE bit.

Table 184. Spread-spectrum mode selection bit

FSS_MODE	Spread-spectrum mode
0	Triangular modulation
1	Pseudo-random Modulation

In triangular modulation, the frequency spectrum uses a 24 kHz frequency modulation to sweep the frequency with 0.5 % frequency steps.

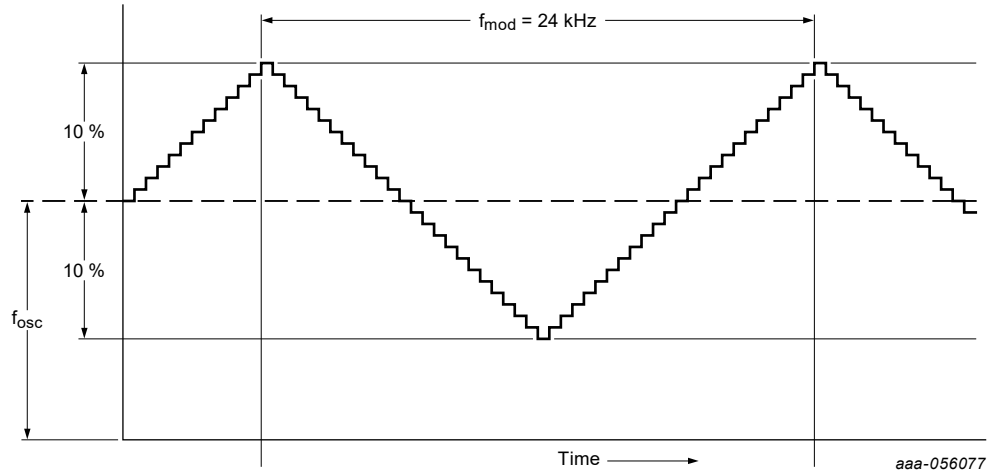


Figure 35. Triangular modulation

When the device is operating in pseudo-random modulation, the spread spectrum transitions gradually between the frequency base points (-10 % frequency level, the base frequency and 10 % frequency level), passing through three randomly generated frequency steps between each base point transition.

The random frequency step may cause the frequency to sweep in any direction before it reaches the next frequency base point, causing an aleatory modulation.

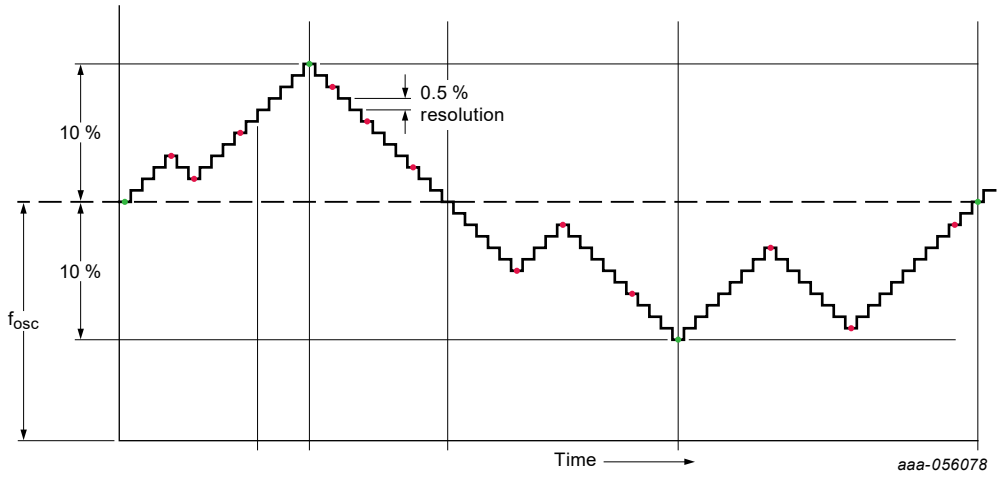


Figure 36. Pseudo-random modulation

13.4.2 Clock synchronization

The FSYNC pin is a bidirectional clock pin used to enable clock synchronization with one or more external devices. The pin is suitable for 1.8 V or 3.3 V level signals.

The mode of operation of the FSYNC pin is set on OTP via the OTP_FSYNC_MODE bits, and cannot be changed during the system operation.

Table 185. FSYNC mode selection bit

OTP_FSYNC_MODE	FSYNC operating mode
0	SYNCOUT mode
1	SYNCIN Mode

13.4.2.1 SYNCOUT mode

When the FSYNC pin is operating in SYNCOUT mode, the pin provides a signal toggling with the same frequency as the switching regulators (HFREQ_CLK / 8). In this mode, the device always uses the internal high-frequency clock to generate the switching frequency for the switching regulators.

The FSYNCOUT_EN bit is used to enable or disable the output frequency in the FSYNC pin. By default, the output frequency is disabled, and the MCU must enable it during the configuration phase.

Table 186. Enabling FSYNC output frequency enable bit

FSYNCOUT_EN	FSYNC output frequency
0	Disabled
1	Enabled

13.4.2.2 SYNCIN mode

When the FSYNC pin is operating in SYNCIN mode, an external clock can be fed via the FSYNC pin to synchronize the switching regulators to the external clock. When the external clock synchronization is enabled, the system is expected to operate the switching regulators in PWM mode to ensure clock synchronization.

When the external clock synchronization is enabled, the internal PLL is enabled to generate the switching regulator frequency from either the internal high frequency clock or the external frequency at the FSYNC pin,

however, the internal clock must be set to the frequency closest to the expected input frequency to ensure seamless transition to the internal clock, in the event a bad external frequency failure is present.

If the external clock is meant to start up after the PMIC has started up, the FSYNC pin must be maintained low until the external clock is applied.

The FSYNC pin accepts frequencies in two selectable ranges as defined by the FSYNC_RANGE bit.

Table 187. FSYNC input frequency range selection bit

FSYNC_RANGE	FSYNC input frequency range
0	2.1 MHz to 2.8 MHz
1	333 kHz to 475 kHz

By default, the FSYNC_RANGE bit is reset to 1 at power up, and the MCU must set it to the desired operating range after system startup and proceed to clear the FSYNC_FLT_I condition, to allow the PLL to generate the switching frequency from the valid external frequency.

The FSYNC pin must receive a clock signal within the selected input range with a duty cycle between 41 % to 59 % to recognize it as a valid frequency. If the external clock is not present or invalid, the device will automatically switch to the internal clock and set the FSYNC_FLT_I interrupt. The FSYNC_FLT_I will assert the INTB pin if it is not masked.

The FSYNC_FLT_S bit is set to 1 as long as the frequency watchdog detects an invalid (out of range) input frequency on the SYNC pin, and it will clear to 0 when the external frequency is back within the valid range.

The PF09 will switch back to the external switching frequency only when the FSYNC_FLT_I interrupt has been cleared and the frequency watchdog is detecting a valid input frequency.

13.4.2.3 Electrical characteristics

Table 188. FSYNC electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{FSYNC}	FSYNC output voltage level	–	V_{DDIO}	–	V
V_{OH_FSYNC}	FSYNC output high voltage • Minimum voltage at 2 mA load	V_{DDO}-0.5	–	–	V
I_{OH_FSYNC}	FSYNC output high current	–	–	2	mA
V_{OL_FSYNC}	FSYNC output low voltage • Maximum voltage at 10 mA load	–	–	0.4	V
I_{OL_FSYNC}	FSYNC output low current	–	–	2	mA
F_{OUT_FSYNC}	FSYNC output frequency	1.9	–	3.1	MHz
t_{PDLY_FSYNC}	FSYNC propagation delay	–	–	35	ns
V_{IH_FSYNC}	FSYNC Input high voltage • Minimum voltage to ensure a HIGH state	0.7*V_{DDIO}	–	–	V
$V_{IL\_FSYNCOUT}$	FSYNC Input low voltage • Maximum voltage to ensure a LOW state	–	–	0.4	V
$I_{HYS\_FSYNCOUT}$	FSYNC Input buffer hysteresis	100	–	400	mV
$I_{IN\_LEAK\_FSYNC}$	FSYNC input leakage • Pin shorted to 5.5 V	–	–	1	µA

Table 188. FSYNC electrical characteristics...*continued*

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
$F_{IN\_LF\_FSYNC}$	FSYNC low frequency input range • FSYNC_RANGE = 1	333	–	475	kHz
$F_{IN\_HF\_FSYNC}$	FSYNC high frequency input range • FSYNC_RANGE = 0	2.1	–	2.8	MHz
D_{IN_FSYNC}	FSYNC input duty cycle range	40	–	60	%

13.5 Analog multiplexer

The PF09 features a 32-channel analog multiplexer (AMUX) to allow a buffered access to various internal voltages via the AMUX pin. An internal divider ratio is applied on each channel to ensure the AMUX output is always within 1.65 V, making it suitable for 3.3 V or 1.8 V ADC inputs.

The AMUX_EN bit is provided to enable or disable the AMUX block.

Table 189. AMUX enable bit

AMUX_EN	AMUX block
0	AMUX disabled, pulled to ground
1	AMUX enabled.

The AMUX output is selected with the AMUX_SEL[4:0] bits.

Table 190. AMUX channel selection

AMUX_EN	AMUX_SEL[4:0]	AMUX Selection	Internal signal Dividing ratio
0	xxxxx	Disabled, pulled down	N/A
1	00000	Disabled - Hi-Z	N/A
1	00001	VIN	4.0
1	00010	BG REG	1.0
1	00011	BG MON	1.0
1	00100	VDIG	1.0
1	00101	VANA	1.0
1	00110	SW1_FB	1.0 (From 0.5 V to 1.5V) 2.5 (From 1.8 V to 3.3 V)
1	00111	SW2_FB	1.0 (From 0.5 V to 1.5 V) 2.5 (From 1.8 V to 3.3 V)
1	01000	SW3_FB	1.0 (From 0.5 V to 1.5 V) 2.5 (From 1.8 V to 3.3 V)
1	01001	SW4_FB	1.0 (From 0.3 V to 1.5 V) 2.5 (From 1.8 V to 3.3 V)
1	01010	SW5_FB	1.0 (From 0.3 V to 1.5 V) 2.5 (From 1.8 V to 3.3 V)
1	01011	LDO1	1.0 (from 0.75 V to 1.5 V)

Table 190. AMUX channel selection*...continued*

AMUX_EN	AMUX_SEL[4:0]	AMUX Selection	Internal signal Dividing ratio
			2.5 (from 1.8 V to 3.3 V)
1	01100	LDO2	1.0 (from 0.75 V to 1.5 V) 2.5 (from 1.8 V to 3.3 V)
1	01101	LDO3	1.0 (From 0.75 V to 1.5 V) 2.5 (From 1.8 V to 3.3 V)
1	01110	VAON	2.5
1	01111	TEMP_IC	1.0
1	10000	TEMP_SW1	1.0
1	10001	TEMP_SW2	1.0
1	10010	TEMP_SW3	1.0
1	10011	TEMP_SW4	1.0
1	10100	TEMP_SW5	1.0
1	10101	TEMP_LDO1	1.0
1	10110	TEMP_LDO2	1.0
1	10111	TEMP_LDO3	1.0
1	11000	VMON1	1.0
1	11001	VMON2	1.0
1	11010	VDIG_DMS	1.0
1	11011	Reserved	N/A
1	11100	Reserved	N/A
1	11101	Reserved	N/A
1	11110	Reserved	N/A
1	11111	Reserved	N/A

When the AMUX is enabled with AMUX_SEL = 0000, the AMUX output is placed in high impedance to allow multiple devices to connect to the same ADC input and drive the AMUX line one device at a time.

13.5.1 Electrical characteristics

Table 191. AMUX electrical characteristics

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and TA = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{AMUX_OUT}	AMUX output voltage range	0.3	–	1.65	V
V_{OFFSET}	AMUX output voltage offset (input to output)	-10	–	10	mV
I_{QAMUX}	AMUX quiescent current	–	185	–	µA
t_{AMUX_ON}	AMUX settling time (off-to-channel transition) • Max step size of 1.6 V • Bus capacitance 150 pF	–	–	50	µs
t_{AMUX_CHG}	AMUX settling time (channel-to-channel Transition)	–	–	50	µs

Table 191. AMUX electrical characteristics...*continued*

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and TA = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• Max step size of 1.6 V • Bus capacitance 150 pF				
V_{CLAMP}	AMUX clamping voltage	1.8	–	2.5	V
V_{DIV4V0}	Input divider ratio by 4 tolerance	3.95	4	4.05	–
V_{DIV2V5}	Input divider ratio by 2.5 tolerance	2.48	2.5	2.52	–
V_{DIV1V0}	Input divider ratio by 1 tolerance	0.995	1	1.005	–

13.6 Thermal monitors

The PF09 features nine temperature sensors spread around the die. The main thermal management sensor is located at the center of the die, and the rest are located in the vicinity of the voltage regulators:

- Center of die
- Vicinity of SW1
- Vicinity of SW2
- Vicinity of SW3
- Vicinity of SW4
- Vicinity of SW5
- Vicinity of LDO1
- Vicinity of LDO2
- Vicinity of LDO3

The output of the temperature sensors is internally connected to the AMUX, allowing the user to read the raw voltage equivalent to the temperature on each sensor. Sensor temperature at any point is calculated with the following formula:

$$T[\,^{\circ}\mathrm{C}] = \frac{V_{TSENSE} - V_{TSNS\_24C}}{T_{COF}} + 24\,^{\circ}\mathrm{C}$$

Where V_{TSENSE} is the thermal sensor voltage measured on the corresponding AMUX channel.

The temperature sensor at the center of the die is used to generate thermal interrupts and thermal shutdown. The processor can read outputs of the other temperature sensors and take appropriate action (such as reducing loading, or turning off a regulator) if the temperature exceeds desired limits at any point in the die.

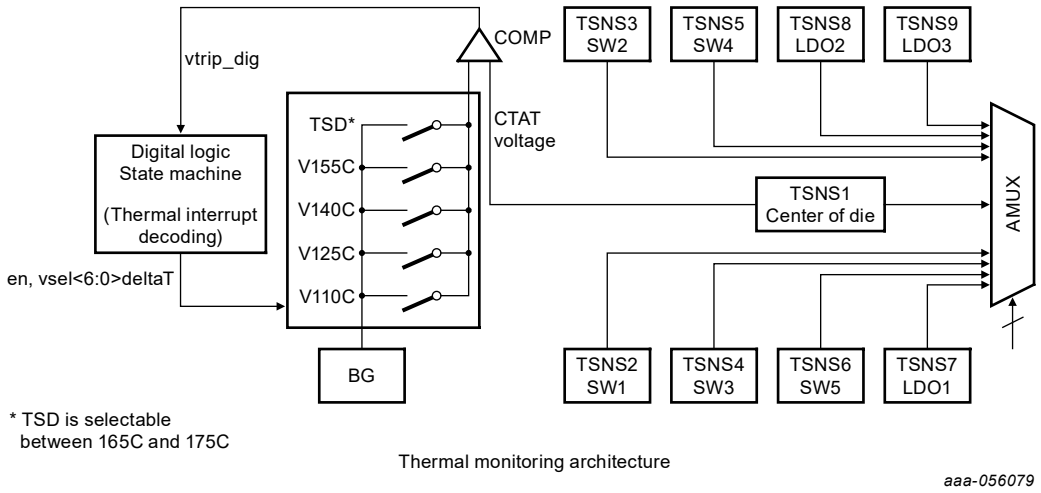


Figure 37. Thermal monitoring architecture

The central thermal monitoring is always enabled during the RUN state, to allow thermal protection during heavy loading conditions.

During the monitored STANDBY state, the thermal monitor operates in sample mode to optimize power utilization without sacrificing thermal monitoring availability.

In the Low-power STANDBY and OFF states, the thermal monitoring is disabled allow the system to achieve the lowest power consumption.

The PF09 provides four thermal thresholds to notify the system when the die temperature has crossed the respective threshold.

Table 192. Thermal thresholds notification bits

Thermal threshold	Interrupt bit	Mask bit	Sense bit
110 °C	THERM_110_I	THERM_110_M	THERM_110_S
125 °C	THERM_125_I	THERM_125_M	THERM_125_S
140 °C	THERM_140_I	THERM_140_M	THERM_140_S
155 °C	THERM_155_I	THERM_155_M	THERM_155_S

The thermal interrupt will be asserted when the die temp crosses the corresponding threshold on the rising edge, and it will assert the INTB pin as long as the corresponding interrupt is not masked.

The MCU can select the thermal warning relevant to the system to take appropriate action to bring down the temperature (either by turning off external regulators, reducing load, or turning on a fan).

A thermal shutdown (TSD) threshold is provided to start a shutdown event when the die temperature has crossed the TSD threshold during the RUN and monitored STANDBY states. When the device reaches the thermal shutdown, it will proceed to turn off the power supplies and it won't be able to restart until the die temperature has decreased below the TSD with a 10 °C hysteresis.

During the power-up event, the thermal monitor is used to gate the Power-up sequence if the die temperature is above the thermal shutdown threshold

13.6.1 Electrical characteristics

Table 193. Thermal monitoring electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
T_{COF}	Thermal sensor coefficient	–	-3.8	–	mV/ºC
V_{TSNS_24C}	Thermal sensor voltage at 24 ºC	–	1.38	–	V
T_{110C}	110 ºC temperature threshold	100	110	120	ºC
T_{125C}	125 ºC temperature threshold	115	125	135	ºC
T_{140C}	140 ºC temperature threshold	130	140	150	ºC
T_{155C}	155 ºC temperature threshold	145	155	165	ºC
T_{SD_165C}	Thermal shutdown threshold • Applies to devices with 165 °C thermal shutdown	155	165	175	ºC
T_{SD_175C}	Thermal shutdown threshold • Applies to devices with 175 °C thermal shutdown	165	175	185	ºC
T_{WARN_HYS}	Thermal threshold hysteresis	–	5	–	ºC
T_{SD_HYS}	Thermal shutdown hysteresis	–	10	–	ºC
t_{TMP_DBNC}	Debounce timer for temperature thresholds (on both rising and falling temperatures)	–	10	–	µs
$t_{S\_INTERVAL}$	Sampling interval time	–	3	–	ms
t_{S_WINDOW}	Sampling window	–	450	–	µs

14 Functional safety

The PF09 is developed in accordance with the ISO 26262 standard and in compliance with the industrial IEC61508 safety standard as a safety element out of context (SEooC). It provides a comprehensive set of functional safety features to reach an automotive safety integrity level up to ASIL D and industrial SIL 2.

The available safety monitoring features depend on the target safety integrity level and PF09 device version. A superset of the potential safety functions are listed below:

- Output voltage monitoring with dedicated bandgap reference
- Bandgap monitoring
- Protected I^2C protocol with CRC verification.
- Hash fault monitoring (dynamic CRC)
- System watchdog management
- Dedicated Fail-safe output (FS0B)
- System interface safety outputs (RSTB, PGOOD, INTB)
- External fault detection inputs (FCCU, ERRMON)
- Power-up analog self-test + ABIST on demand
- Power-up logic built-in self-test + LBIST on demand
- Fully isolated digital machine supervisor

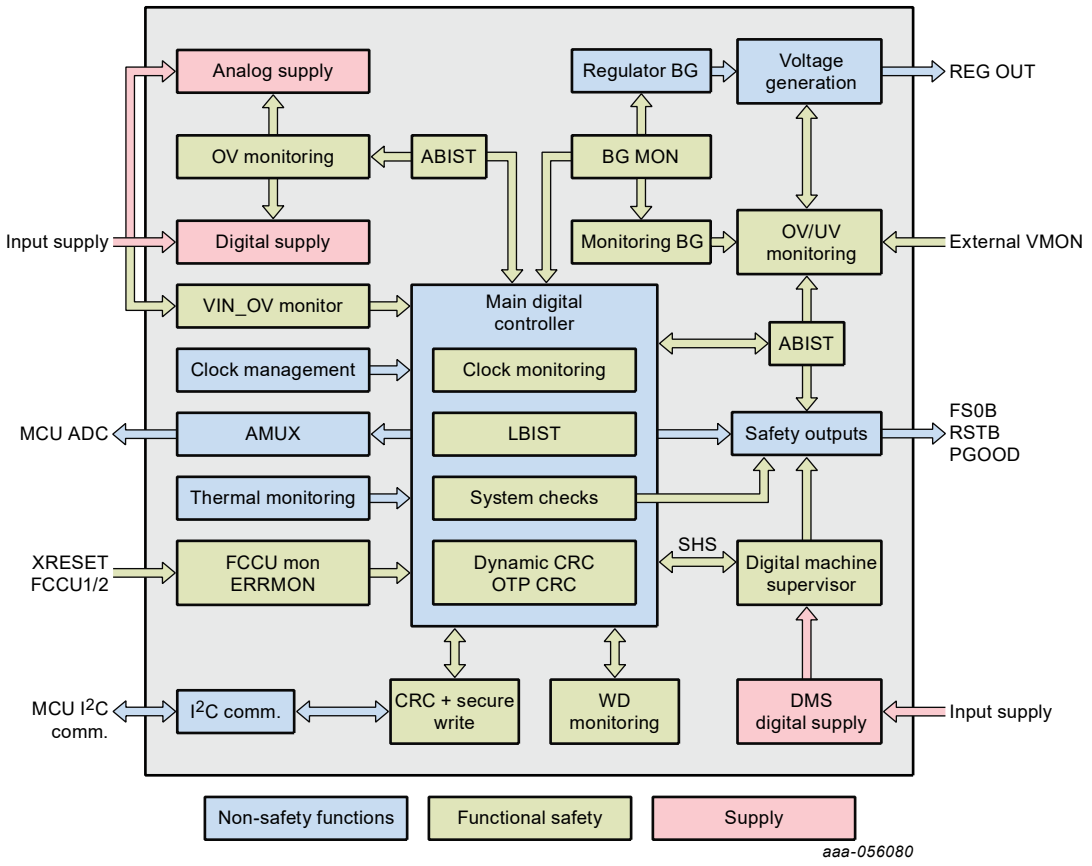


Figure 38. PF09 safety architecture diagram

14.1 Output voltage monitoring

The PF09 is intended to operate as the main safety controller for the full power management architecture, providing high precision OV/UV monitoring during the RUN and Monitored STANDBY states for the PF09 system regulators, as well as external regulators supplied by one or more companion PMICs.

The OV/UV monitoring circuits implement a dedicated bandgap reference which is fully independent from the bandgap reference used for the voltage generation.

Safety OV/UV monitoring is performed on the following regulators:

- Switch mode power supplies (SMPS): SW1, SW2, SW3, SW4, SW5
- Linear regulators (LDO): LDO1, LDO2, LDO3, VAON

External voltage monitoring is performed via the two dedicated external VMON pins.

- VMON1
- VMON2

Additional external voltage monitoring pins are available in the LDO2 and LDO3 if the regulators are not required in the system.

- VLDO2MON (LDO2OUT pin)
- VLDO3MON (LDO3OUT pin)

Refer to section 17.3 Voltage Monitoring for operational details of the safety-related VMON blocks.

Voltage monitoring of the VAON regulator in the Low-power modes (OFF and STANDBY states) is not considered to be a safety-related mechanism, therefore the undervoltage detection in such scenarios is designed to prioritize power consumption over physical independence of the voltage reference between the regulator and the voltage monitor.

14.1.1 Voltage monitoring during a pin disconnection

The switching regulators and LDOs are provided with a pin-lift mechanism to detect a random pin disconnection that could potentially lead to an *unsafe/undetectable* condition, resulting in a violation of the safety goal.

When the VAON operates as an always-on regulator with very low quiescent current, this rail is intended to supply the low-level voltage domain in the MCU in charge of communicating and interfacing with the PF09 device. It is assumed a pin disconnection in the VAON output will cause the MCU to become unresponsive, and such a fault will be detected by other mechanisms, therefore a pin-lift feature is not needed in the VAON.

14.1.1.1 Switching regulators FB disconnection

Each switching regulator is provided with an internal weak pullup resistor to VIN at its respective SWxFB pad, to ensure the VMON is able to perform a *safe* reaction when the regulation is operating in PWM mode.

A pullup on the FB node will force the VMON into to an OV condition, while the error amplifier will try to lower the output voltage by reducing the PWM, resulting in an incorrect OV fault detection but *safe* reaction to an FB pin disconnection.

It is assumed the PFM mode is intended to be used during low-power STANDBY mode, which is considered a safe state with no critical activity. In these scenarios, the internal pullup resistor will be disabled in the PFM mode to ensure proper operation of the PFM control loop.

14.1.1.2 LDO regulators output disconnection

The LDOs are provided with an internal mechanism to detect a real-time pin disconnection during normal operation. A current source injects small amounts of current with a frequency wide enough to cause a pin

disconnection to be detected as an OV condition, while resulting in a neglectable output ripple,during normal LDO operation.

14.2 Bandgap monitoring

The PF09 features an analog bandgap monitoring circuit to ensure the integrity of the regulation and the monitoring bandgaps by performing a real-time comparison between the output of both blocks. An absolute 5 % (typical) difference between the two bandgaps will be detected as a potential regulation or monitoring fault, and the device will start a protective mechanism.

At power up, the bandgap monitor is evaluated during the self test. A bandgap drift detected by the bandgap monitor will result in a failing self test, preventing a power-on event with an erroneous bandgap.

A bandgap failure during the Monitored SYSTEM ON states will assert the FS0B pin and set the BGMON_I interrupt, which in turn can assert the INTB pin if the interrupt is not masked.

The BGMON_S bit is provided to read the real-time status of the bandgap monitor.

Table 194. Bandgap monitor status bit

BGMON_S	Bandgap monitor status
0	No BG fault
1	BG fault detected

In devices with high safety integrity level (ASIL D/SIL 2), the independent digital machine supervisor (DMS) can be configured to perform protective reaction upon a random bandgap monitoring failure. Refer to section 18.12 Digital Machine Supervisor for detailed description and configurability of the DMS block.

14.3 Clock monitoring

A clock monitoring mechanism is implemented in the main digital block to perform a frequency comparison between the internal system clocks.

At power-up, the clock monitor evaluates the integrity of the internal clocks during the self-test. A considerable clock drift larger than +/-6 % between any of the internal clocks will result in a failing self test, thus preventing a power-on event with an erroneous clock leading to a potential single-point failure.

A clock drift larger than +/- 6 % between any of the internal clocks during the monitored SYSTEM ON states will assert the FS0B pin and set a CLKMON_I flag , which in turn can assert the INTB if the interrupt is not masked.

In devices with a high safety integrity level, clock failure diagnostic coverage is improved by the implementation of the DMS to detect a significant clock drift and stuck-at condition on any of the internal clocks, providing coverage against single-point failures and latent failures in the DMS block itself. Refer to section 18.12 Digital Machine Supervisor for detailed description and configurability of the DMS block.

14.4 Watchdog management

The PF09 features an advanced watchdog (WD) management interface to verify the system ability to write, read, and compute information to and from the PMIC. Total latency to generate a watchdog reset event will depend on the WD timer duration and the maximum bad WD refresh value set in the watchdog configuration registers. A watchdog reset event will be started when the internal bad watchdog counter reaches the maximum value programmed.

The system watchdog can be enabled by default via the OTP_WD_EN bit, and it can disabled or re-enabled manually during the RUN and the monitored STANDBY state by writing the WD_EN bit on the I^2C register map.

Table 195. System watchdog enable bit

WD_EN	WD Ttmer
0	WD disabled
1	WD enabled

The system watchdog is not available in the Low-power STANDBY or SYSTEM OFF states.

The PF09 family of devices supports two different modes of operation for the watchdog monitoring interface. The mode of operation depends on the target safety integrity level supported by each specific device version.

For QM and ASIL B devices requiring low to medium coverage, a static watchdog is used to ensure coverage for timing, stuck-at and I^2C data write conditions in the MCU.

For custom ASIL B, ASIL D and SIL 2 devices requiring medium to high coverage, a dynamic watchdog is used to ensure coverage for timing, stuck-at conditions, I^2C read/write and data computing condition in the MCU.

14.4.1 Static WD

On devices using the static watchdog, the WD_SEED[7:0] register will provide a static seed to clear the watchdog.

The WD_SEED[7:0] bits will be reset to the default value (0xA5) at power up and during hard reset conditions, however a soft reset will not reset the WD seed.

The system will always use the selected value in the WD_SEED[7:0] bits to calculate the response to service the PMIC watchdog, but the MCU can modify this value if it decides to use a different key for security purposes.

14.4.2 Dynamic WD

On devices using the dynamic watchdog, the WD_SEED [7:0] bits will provide a dynamic seed to be used to clear the watchdog.

The default value of the WD_SEED[7:0] bits at power-up and hard-reset conditions is reset to 0xA5, and it will recalculate every time a WD refresh is attempted (regardless of whether it is successful or not). A soft reset condition will not reset the WD_SEED[7:0] bits, to provide continuity to the previous dynamic seed generation loop.

The system can implement two different strategies to service the dynamic watchdog. based on the level of complexity required to ensure processing coverage:

1. Seed readback method: the MCU must read the current seed from the WD_SEED[7:0] bits, and use the value read to calculate the response key to service the current WD cycle.
2. Seed calculation method: the MCU will synchronize its starting seed with the PMIC during the booting sequence, and it must implement an algorithm to calculate the next seed using the same algorithm as the one implemented in the PF09 watchdog interface, such that it can keep servicing the watchdog without requiring any further seed synchronization from the PMIC. If the MCU falls out of synchronization, it can always read the current seed, or re-set the seed via I^2C, to regain synchronization with the PMIC.

The polynomial used to calculate the dynamic seed in the PF09 is provided below:

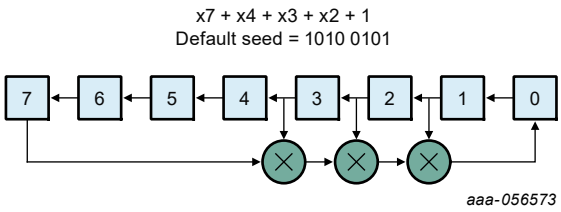


Figure 39. Dynamic watchdog polynomial

When operating in dynamic WD mode, WD_SEED = 0x00 or WD_SEED = 0xFF are invalid values. The PMIC will ignore the command and generate a WD_ERROR_I interrupt to notify the system that no action has been taken.

14.4.3 Servicing the watchdog timer

The procedure to clear the watchdog counter is the same for both static and dynamic watchdog, with the only difference that the seed required to clear the watchdog will keep changing when the dynamic WD mode is enabled, whereas the seed remains stable in the static WD mode.

To service the watchdog, the MCU must write a valid response in the WD_CLEAR[7:0] bits before the watchdog timer expires.

A valid response must meet the following conditions:

- The response is calculated as the bitwise NOT of the WD_SEED[7:0] bits.
- The response must be provided within an open window.

Providing a valid key into the WD_CLEAR[7:0] register will generate a WD_OK event.

When the MCU fails to clear the system watchdog (invalid response or WD duration expired), the device will generate a WD_NOK event, set the WD_ERROR_I flag, and the INTB will be asserted, as long as the interrupt is not masked

The watchdog timer will be reset after either a WD_OK or a WD_NOK event, to start a new service window.

The WD_DURATION[3:0] bits are used to set the duration of the watchdog timer to service the watchdog. The WD timer will expire when it reaches the value set on the WD_DURATION[3:0] while WD refresh is present.

Table 196. System watchdog timer configuration bits

WD_DURATION[3:0]	Watchdog timer duration
0000	1 ms
0001	2 ms
0010	4 ms
0011	8 ms
0100	16 ms
0101	32 ms
0110	64 ms
0111	128 ms
1000	256 ms
1001	512 ms
1010	1024 ms

Table 196. System watchdog timer configuration bits*...continued*

WD_DURATION[3:0]	Watchdog timer duration
1011	2048 ms
1100	4096 ms
1101	8192 ms
1110	16384 ms
1111	32768 ms

At power up, the WD timer will start counting only after the RSTB pin is released in the Power-up sequence. The default value of the WD_DURATION[3:0] bits is set on OTP by the OTP_WD_DURATION[3:0] bits.

The system can define a longer timer duration at power up, to allow the MCU to perform its booting sequence, and then reduce the timer duration to ensure a fault detection within the required system FTTI. When the WD_DURATION[3:0] bits are changed during the SYSTEM ON states, the WD timer will be restarted to ensure the system is properly synchronized with the MCU.

The OTP_WD_WINDOW[1:0] bits are provided to select the close/open ratio to service the system watchdog.

Table 197. System watchdog window configuration bits

OTP_WD_WINDOW[1:0]	Close window	Open window
00	0 %	100 %
01	25 %	75 %
10	50 %	50 %
11	75 %	25 %

When OTP_WD_WINDOW = 00, the device will use 100 % of the WD_DURATION as an open window to service the WD. Any other selection will close the watchdog window for the first part of the timer and open the window for the second part of the timer. Servicing the watchdog within the closed window, or failing to service the WD within the watchdog duration, will be interpreted as a bad watchdog refresh.

The WD_NOK_CNT[2:0] counter is provided to count WD_NOK events, in order to be able to generate a PMIC reset event if a fault condition is present on the MCU. The WD_NOK_CNT counter uses a 2-by-1 count strategy to ensure the system is not caught in a software loop that is able to service one good WD per each bad WD within the loop.

- An invalid response will increase the WD_NOK_CNT[2:0] by 2
- A valid response will decrease the WD_NOK_CNT[2:0] by 1

If WD_NOK_CNT[2:0] = WD_NOK_MAX[2:0], the device will generate a hard reset event and the RESET_CNT[3:0] bits will be increased by 1. Refer to section 16.4.2 Reset Conditions, for a detailed description of the reset behavior.

The initial value for the WD_NOK_MAX[2:0] is set in the OTP by the OTP_WD_NOK_MAX[2:0] bits.

The WD_NOK_CNT counter uses a 2-by-1 count strategy to ensure the system is not caught in a software loop that is able to service one good WD per each bad WD within the loop.

- An invalid response will increase the WD_NOK_CNT[2:0] by 2
- A valid response will decrease the WD_NOK_CNT[2:0] by 1

Due to the 2-by-1 design of the watchdog counter, when the WD_NOK_MAX[2:0] is set to 0x01 or 0x02, a WD reset event will be initiated as soon as the first bad WD refresh occurs.

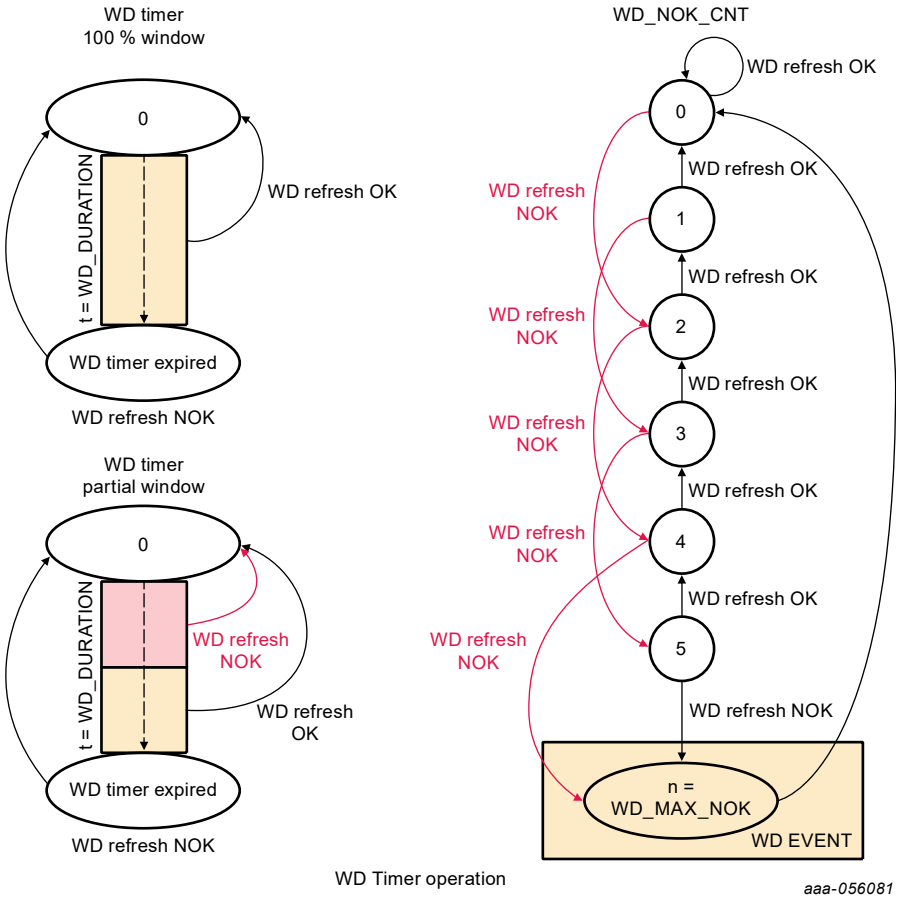


Figure 40. System watchdog operation

The PF09 supports a development mode operation in the watchdog management functionality in order to proof and validate the watchdog functionality without generating a system reset, if system is not able to provide a valid response. The watchdog operates in development mode when the WD_NOK_MAX[2:0] bits are set to 0b000,

When the WD is operating in development mode, the WD_NOK_CNT[2:0] will still count good and bad WD refresh, however, there will be no maximum count, hence no WD reset is possible.

The WD_OK_CNT[2:0] bits are provided to count the number of consecutive WD_OK events. The WD_OK counter increases by 1 every time a good refresh is present, but it will clear to 0 when a bad refresh occurs.

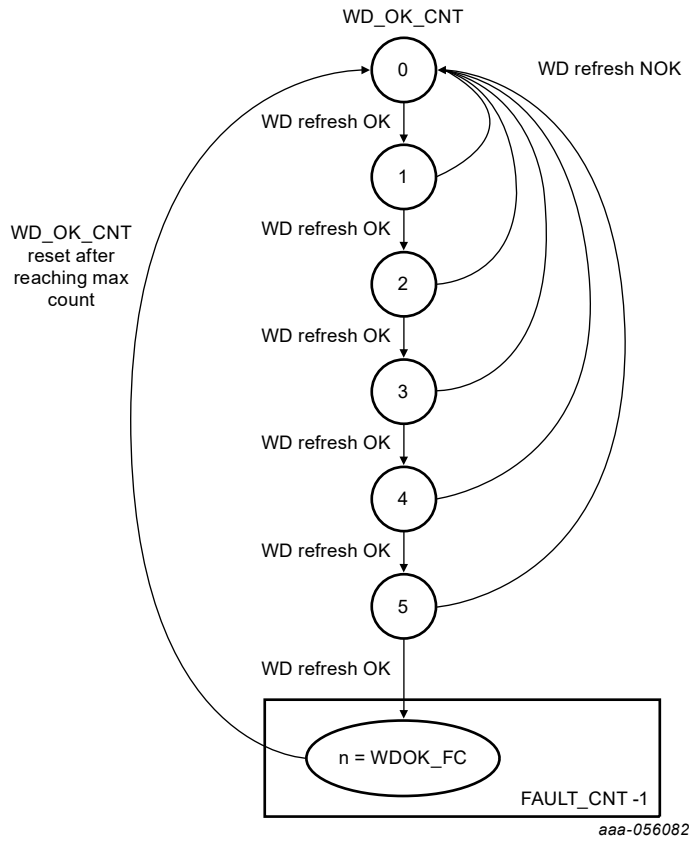


Figure 41. WD_OK counter

The WD_OK counter works together with the WD_OK_FCD[2:0] bits to allow a number of consecutive WD_OK events to reduce the fault and reset counters by 1.

The WD_OK_FCD[2:0] provides an automatic way to keep the system counters clean as long as the system is healthy and able to service the PMIC watchdog. This reduces the need of constant housekeeping which could potentially result in systemic fault conditions where the system can fall into a software loop where it is not able to move forward and the PMIC is not able to reach the maximum fault count limit, because the MCU clears the fault counters within the software loop.

The default value for the WD_OK_FCD[2:0] is loaded from OTP at power up via the OTP_WD_OK_FDC[2:0] bits.

Table 198. WD_OK events required to reduce the Fault counter by 1

WD_OK_FCD[2:0]	Good WD fault clear
000	Good WD cannot clear faults
001	Every one WD refresh OK
010	Every two WD refresh OK
011	Every three WD refresh OK
100	Every four WD refresh OK
101	Every five WD refresh OK
110	Every six WD refresh OK
111	Every seven WD refresh OK

When the WD counter is disabled or the WD_OK_FCD[2:0] bits are set to 0b000, the WD_OK_CTN[2:0] bits will have no effect on the FAULT_CNT[3:0] or RESET_CNT[3:0] counters. In this case, the system must implement a routine to clear the system counters manually, to avoid a turnoff event due to compounded random faults.

14.5 FS0B active safe-state mode

In devices targeting a high safety integrity level, the FS0B is used as a dedicated safety output operating in Active Safe-state mode. In this mode, the PF09 implements several mechanisms to ensure the FS0B is able to assert LOW, to indicate the PMIC is in a safe state.

The PF09 assumes the following safe states:

- PMIC in RUN state with FS0B pin asserted
- PMIC in STANDBY state with FS0B pin asserted
- PMIC in OFF states with RSTB and FS0B asserted
- PMIC in Deep Fail-safe state with RSTB and FS0B asserted
- System reset (WD or XRESET event with RSTB and FS0B asserted)
- Unresponsive main digital control unit with FS0B and RSTB asserted

During the RUN states, the FS0B remains asserted low until the MCU requests an FS0B release command via I^2C. In the STANDBY states, the FS0B is always asserted LOW.

To request an FS0B release command, the MCU must write the code 0xA5 into the FS0B_RELEASE [7:0] bits. Any other value on the FS0B_RELEASE[7:0] bits will be ignored.

The FS0B will be allowed to release only after all conditions flagging a potential safety-related fault are acknowledged and cleared when the FS0B release command is requested:

- Power-up sequence has been finished
- RSTB is released. (device is in the SYSTEM ON states)
- All ABIST flags are 0 (ABIST OK)
- The LBIST_STATUS[1:0] = 11 (LBIST Passed)[1]
- The FAULT_CNT[3:0] = 0x00
- The DCRC_FLG = 0
- The DFS_FLG = 0
- The VIN_OV_FLG = 0
- The XFAIL_FLG = 0
- The WD_FLG = 0
- The XRESET_FLG = 0
- The SFAULT_FLG = 0
- The HFAULT_FLG = 0
- The BGMON_I = 0 (no Bandgap drift detected)
- The CLKMON_I = 0 (no clock drift detected)
- The SHS_I = 0 (no safety handshake fault detected)[1]
- No Short condition is detected on PGOOD and FS0B outputs

Once the FS0B pin is released, the pin will assert LOW if one or more safety-related fault conditions occur:

- The MCU writes a 0x4B code into the FS0B_RELEASE[7:0] bits
- The RSTB pin is asserted LOW (internally or externally)
- An OV condition in the VDIG or VANA supplies
- A hard fault starts a power-down sequence

1 Conditions are evaluated only on devices featuring functions such as LBIST, DMS, or safety handshake.

- The device is powered down into any of the OFF states
- The device moves into the DFS state
- The XFAILB pin is asserted externally
- A dynamic CRC (DCRC) fault is present
- A VIN_OV condition is present
- An XRESET event is present
- An OV/UV/ILIM condition is present and the fault is not bypassed
- An FCCU failure is detected
- An ERRMON failure is detected
- The BGMON detects a bandgap drift condition
- The CLKMN detects a clock drift condition
- A short condition is detected on PGOOD or FS0B outputs

During the RUN states, every time the FS0B pin is asserted the MCU must perform the necessary diagnostic to clear all fault conditions and request an FS0B release command, to release the pin and resume normal operation.

14.5.1 FS0B pin diagnostic bit

The FS0B_S bit provides the real-time state of the FS0B pin.

Table 199. FS0B status bit

FS0B_S	FS0B status
0	Pin sensed LOW
1	Pin sensed HIGH

The FS0B_FLT_I interrupt is provided to notify the system of a short-to-high or short-to-low condition on the FS0B pin. The FS0B fault event will assert the INTB pin if the FS0B_FLT_I interrupt is not masked.

The MCU can inspect the specific condition causing the FS0B_FLT_I interrupt to assert by reading the real-time sense bits FS0B_S2H (short to high) and FS0B_S2L (short to low).

When the FS0B pin is being driven LOW internally, and the FS0B_S bit is sensing a HIGH state, the FS0B_S2H bit is set HIGH until the condition is no longer present.

When the FS0B pin is released HIGH internally, and the FS0B_S is sensing a LOW state, the FS0B_S2L bit is set HIGH until the condition is no longer present.

Note: *Bits with _S in the names are sense bits, which are real time. Their values may disappear after the condition in question goes away. Bits with _I in their names may be called flags or interrupt bits. These are sticky bits, and their values will remain after the event is over.*

14.5.2 Redundant FS0B control

The FS0B pin is provided with redundant control logic to ensure the pin is able to enter the safe state during critical fault conditions (aside from the standard monitoring mechanism), including the loss of the main control input supply (VIN), loss or misbehavior of the internal logic supply (VDIG), and the loss or misbehavior of internal clocks.

In devices targeting high safety integrity levels featuring the digital machine supervisor (DMS) block, secondary control for the FS0B pin is provided by the DMS circuit to support FS0B assertion on fault conditions generated due to a misbehavior or inoperation of the main logic controller.

The third level of redundancy for the FS0B is achieved with an analog path to ensure the pin is asserted LOW if none of the primary control paths are available. The analog path is intended to provide hard control of the

pin when the main digital controller is not operational due to the loss of the main control input supply (VIN), assuming the condition is derived from a pin disconnection.

Note that a loss of the input supply derived from any condition other than a VIN pin disconnection (i.e. the main system supply is lost) is considered as a safe fault condition, because it is assumed all circuits powered by VIN will behave in a safe way as the overall input supply is discharging.

14.6 External error monitoring (ERRMON)

In devices targeting high safety integrity levels, the GPIO3 pin provides a programmable mechanism to monitor a non-critical, safety-related external error signal from the system via the ERRMON mechanism.

The polarity to detect an external error is programmable in OTP via the OTP_ERRMON_POL bit.

Table 200. ERRMON polarity selection bit

OTP_ERRMON_POL	ERRMON polarity
0	Error on rising edge
1	Error on Falling edge

When the ERRMON input detects an external error, the ERRMON block will set the ERRMON_I flag HIGH and start the external fault timer before it can confirm a fault condition. In order for the system to listen to the ERRMON interrupt as soon as it is generated, the ERRMON interrupt must be unmasked to allow it to assert the INTB pin.

If the ERRMON_I flag is cleared before the external fault timer is expired, the device stops and resets the external fault timer, and no protective action is taken. The MCU must write a 1 to the ERRMON_I to clear the interrupt.

If the ERRMON_I flag is not cleared when the external fault timer expires, the device will assert the FS0B pin to indicate an external fault has been confirmed.

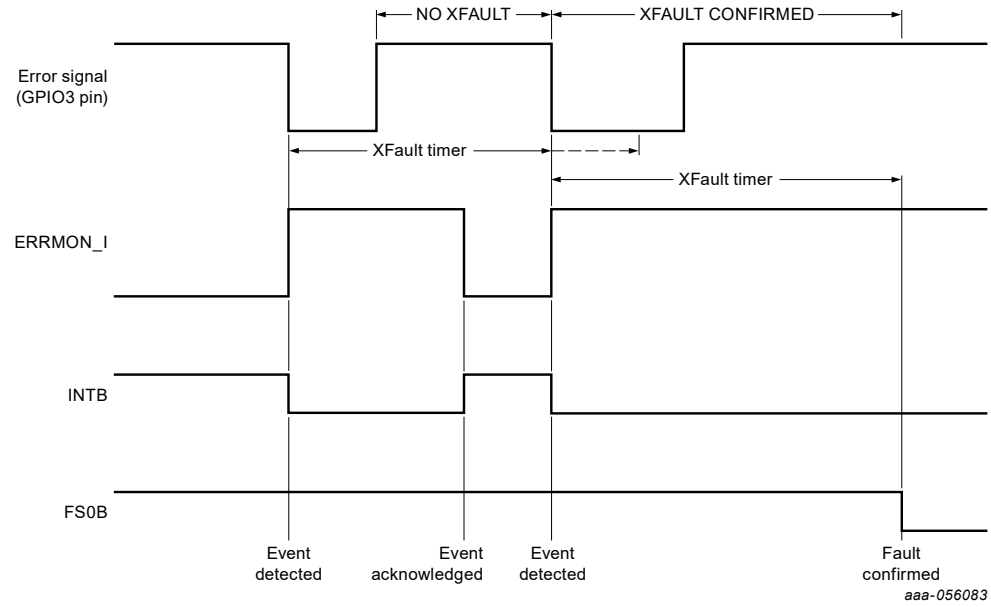


Figure 42. ERRMON operation

By default, the external fault timer is reset to 8 ms at power-up, and it can be changed during the SYSTEM ON states via the ERRMON_TIME bits.

Table 201. ERRMON timer configuration bit

ERRMON_TIME	Error tmer duration
00	1 ms
01	8 ms
10	16 ms
11	32 ms

The ERRMON_RESET bit is provided to define whether the ERRMON fault can also generate a hard reset event upon a fault confirmation. By default, the ERRMON_RESET is set to 0, to ensure the system does not generate a hard reset at power up, until the MCU is able to configure the system and ready to set an OK condition in the ERRMON input.

Table 202. ERRMON reaction configuration bit

ERRMON_RESET	ERRMON reaction
0	No reset (default)
1	Reset on fault confirmed

If the ERRMON reset event is enabled, the reset event will be generated only if the FS0B was previously released. Otherwise, the ERRMON event will be able to notify the system of the event via the INTB pin if the ERRMON_I interrupt is not masked in the interrupt registers.

The device monitors for external errors during the RUN and the Monitored STANDBY States, and it starts monitoring for an external error as soon as the RSTB pin is released after the Power-up sequence.

In the low-power STANDBY state, the ERRMON block is disabled to allow minimum power consumption, and it will start monitoring the ERRMON input as soon as it enters the RUN state.

After the FS0B is asserted by the ERRMON event, the FS0B cannot be released until the ERRMON_I flag is cleared and no fault condition is present in the ERRMON input (assuming there are no other conditions preventing the FS0B from releasing).

If the ERRMON input is stuck in a fault condition (stuck in a NOK level), the system will not be able to clear the ERRMON_I interrupt until the error condition is removed.

The GPIO3_S bit can be used to sense the real-time status of the ERRMON input.

14.6.1 ERRMON dynamic characteristic

Table 203. ERRMON dynamic characteristics

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
t_{FILT_ERRM}	ERRMON deglitch time	9	10	11	µs
t_{ERRM1}	ERRMON_TIME[1:0] = 00	0.9	1	1.1	ms
t_{ERRM2}	ERRMON_TIME[1:0] = 01	7.2	8	8.8	ms
t_{ERRM3}	ERRMON_TIME[1:0] = 10	14.4	16	17.6	ms
t_{ERRM4}	ERRMON_TIME[1:0] = 11	28.8	32	35.2	ms

14.7 FCCU monitoring

The fault conllection and control unit (FCCU) input pins are in charge of monitoring HW failures from an NXP MCU or other protocols compatible with other MCU.

In devices targeting a high safety integrity level where the FCCU block is available, the FCCU configuration is set in the OTP registers via the OTP_FCCUx_MODE[1:0] bits.

In system using a compatible NXP MCU with an FCCU interface, the FCCU0 and FCCU1 are connected to EOUT[0] and EOUT[1] outputs in the MCU. FCCU0 and FCCU1 can be used in bistable mode, or as a single input depending on the targeted safety integrity level of the application.

The OTP_FCCU0_MODE[1:0] bits provide the default mode of operation for the FCCU0 pin.

Table 204. FCCU0 mode selection bits

OTP_FCCU0_MODE[1:0]	Operation
00	No operation
01	Single FCCU0 level monitoring
10	Single FCCU0 PWM monitoring
11	FCCU bistable monitoring

The OTP_FCCU1_MODE[1:0] bits provide the default mode of operation for the FCCU1 pin.

Table 205. FCCU1 mode selection bit

OTP_FCCU1_MODE[1:0]	Operation
00	No operation
01	Single FCCU1 level monitoring
10	Single FCCU1 PWM monitoring
11	XRESET operation

When the OTP_FCCU0_MODE[1:0] = 11, the FCCU0 and FCCU1 will operate in bistable mode, and the OTP_FCCU1_MODE[1:0] bits will be used to decide whether the FCCU1 is operating in full FCCU mode or hybrid mode.

When the FCCU interface is operating in bistable or hybrid mode, the FCCU configuration will be set with the respective FCCU0 bits.

The default debounce time to detect an FCCU error is set in OTP via the OTP_FCCUx_DBNC[1:0] bits, and the system can modify the debounce time during the SYSTEM ON states via the respective functional bits FCCUx_DBNC[1:0].

Table 206. FCCUx debounce time configuration bit

FCCUx_DBNC[1:0]	FCCUx debounce time
00	3 µs
01	6 µs
10	12 µs
11	20 µs

The FCCUx_RESET[1:0] bits are provided to define whether the FCCUx fault should assert the FS0B only, or generate a reset event.

Table 207. FCCUx reaction configuration bit

FCCUx_RESET[1:0]	FCCUx event reaction
00	No reset (only FS0B)
01	Soft reset (FS0B + supply recovery)
10	Hard reset (full power reset)
11	No reset (only FS0B)

FCCU monitoring is always disabled during the Low-power STANDBY and OFF states.

In the Monitored STANDBY state, the system is considered to be in the safe state with the FS0B asserted LOW. In this scenario, the FCCU interface is able to detect a real-time fault condition on the FCCUx pins by reading the FCCUx_S bits, however no fault reaction or FCCU interrupts will be generated while the system is in the Monitored STANDBY state.

Full FCCU monitoring is available during the RUN state as described in this section.

When the FCCU is enabled, the device starts monitoring the FCCU inputs from the MCU as soon as it enters the RUN state.

At power up, the MCU may not have proper control of the FCCU signals, which may result in random fault conditions observed in the FCCU pins during the booting phase. To prevent any false protection, the FCCU interface is defaulted to have effect only over the FS0B pin.

When the MCU is able to provide proper signals in the FCCU pins, it can then configure the system reaction mode and then proceed to release the FS0B to start monitoring the system during normal operation. Refer to section 16.4.2 Reset Conditions for detail description of the soft and hard reset reactions.

The FCCU interface will detect and react to a new fault condition only while the FS0B is released. Fault conditions detected while the FS0B is already asserted LOW will not increase the fault counter nor start any protective reaction.

An FCCU fault detection will always assert the FS0B pin. If the FCCU interface is detecting a fault condition, the FS0B will not be released until all fault conditions are removed.

The FCCU pins have configurable internal pullup or pulldown resistors, to ensure a pin disconnect is properly detected as a fault condition. By default, the internal pull resistors are enabled at power up, and the system can disable the pull resistor during the SYSTEM ON states via the respective FCCUx_RPULL_EN bits.

Table 208. FCCUx internal pull resistor selection bits

FCCUx_RPULL_EN	FCCU Internal pull resistors
0	Internal resistor disabled
1	Internal resistor enabled

The direction of the internal pull resistors is automatically selected based on the mode of operation and the selected pin polarity, as described in the following sections.

14.7.1 FCCU full bistable operation

When OTP_FCCU0_MODE[1:0] = 11 and OTP_FCCU1_MODE[1:0] = 00 or 01, the FCCU interface will be set to full bistable mode by default. In this mode, both the FCCU0 and FCCU1 will be set to detect a bistable fault condition when the state machine is in the RUN or Monitored STANDBY state.

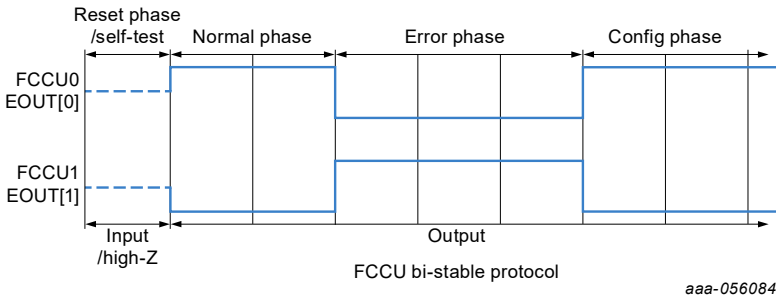


Figure 43. FCCU bistable protocol

During bistable operation, the FCCU0_POL bit will set the polarity to detect a fault condition.

Table 209. Fault detection in bistable mode

FCCU0_POL	FCCU0 pin	FCCU1 pin	Fault status
0	Low	Low	Fault
0	Low	High	Fault
0	High	Low	OK
0	High	High	Fault
1	Low	Low	Fault
1	Low	High	OK
1	High	Low	Fault
1	High	High	Fault

The selection of the pullup /down resistor is done automatically based on the FCCU0 polarity bit, to allow a fault detection upon a pin disconnection.

Table 210. Pull resistor configuration in bistable mode

OTP_FCCU0_MODE	FCCU0_RPULL_EN	FCCU0_POL	Internal pull resistor
11	0	X	FCCUx tri-stated
11	1	0	FCCU0 = pulldown, FCCU1 = pullup
11	1	1	FCCU0 = pullup, FCCU1 = pulldown

14.7.2 Hybrid bistable mode

When OTP_FCCU0_MODE[1:0] = 11 and OTP_FCCU1_MODE[1:0] = 11, the FCCU interface will be set to hybrid bistable mode. The Hybrid bistable mode is provided to address a specific use case with the NXP i.MX9x family of microcontrollers supporting the FCCU interface.

The i.MX9x FCCU interface is always disabled after a reset condition. In this scenario, the FCCU_ERR0 (connected to FCCU0) will be tri-stated and the WDOG_ANY (connected to FCCU1) will be reporting fault conditions with an edge transition to request a PMIC reset if the MCU detects an internal issue during boot-up.

During the booting sequence, the MCU will be in charge of keeping the system in a safe state until it can perform system configuration and enable the FCCU interface to start reporting safety-related failures to the PMIC.

When the MCU is ready to enable the FCCU operation, it must request a transition to the full bistable FCCU mode on the PMIC first, in order to avoid a random transition causing a reset condition on the XRESET input

(FCCU1 pin), followed by enabling its own FCCU operation. Once the FCCU operation is enabled in both the MCU and the PMIC, the MCU can proceed to modify the reaction of the PMIC upon an FCCU failure and request to release the safety output (FS0B) to allow normal operation.

When the PF09 is starting up or coming from a reset condition, the FCCU0 input will be ignored while the FCCU1 pin starts operation as an XRESET input as soon as the device enters the RUN state. Refer to section 16.8.8 FCCU1 (XRESET Mode) for a detailed description of the XRESET behavior.

In order to avoid unsafe operation, the PF09 will not allow the FS0B pin to be released when the FCCU is operating in hybrid bistable mode until the FCCU interface is requested to switch to full FCCU mode.

Switching to full bistable mode is required, but does not constitute sufficient conditions for releasing the FS0B. The MCU must ensure all conditions are met before requesting an FS0B release via the FS0B_RELEASE bits.

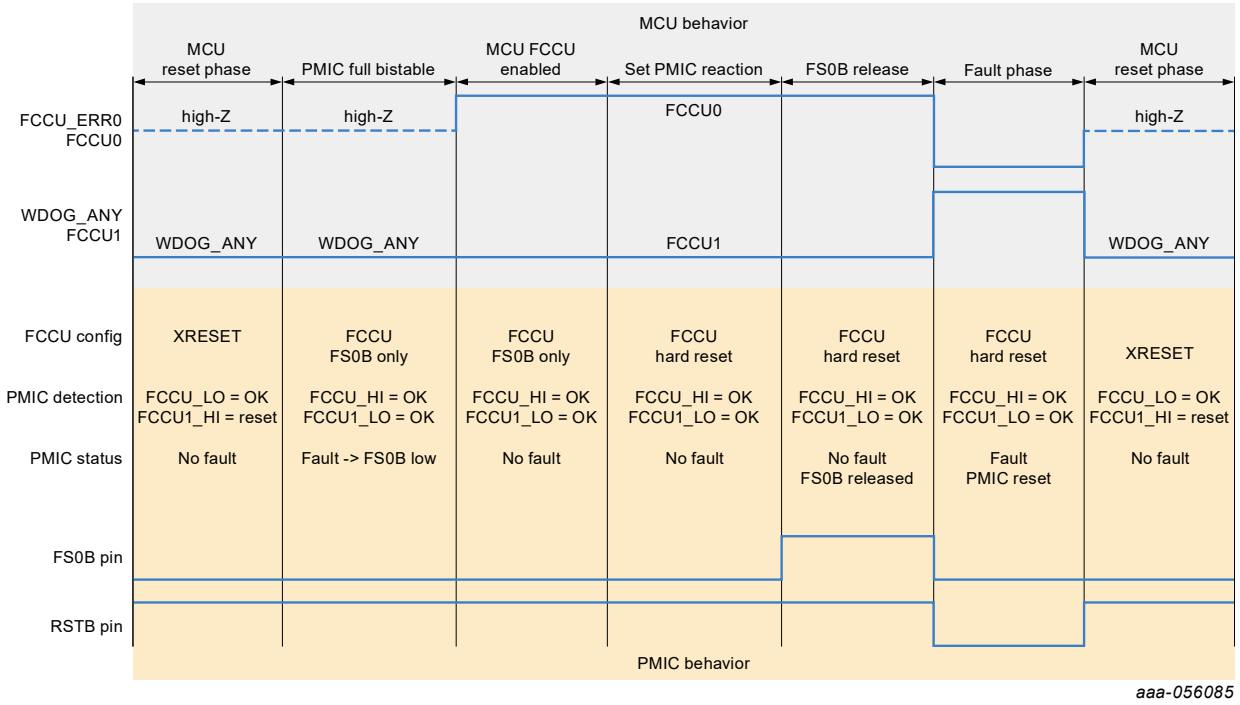


Figure 44. FCCU Hybrid bistable operation

The FCCU pins will change the operation to full bistable mode when the MCU request a transition to FCCU mode via the SYS_CMD[7:0] = 0xB3 (XRESET to FCCU request). Once in the full bistable mode, the device will be able to return to XRESET mode in three ways:

1. The FCCU to XRESET Request command is sent (SYS_CMD[7:0] = 0xBA): to avoid unwanted transition out of safe operation, the FCCU to XRESET request command will take effect only after the FS0B has been asserted LOW, either due to a fault condition or commanded by the MCU via the FS0B_RELEASE[7:0] bits.

When the FCCU to XRESET request command is sent and the FS0B is still released (HIGH), the PF09 will ignore the request and set the BAD_CMD_I to generate an interrupt event to the system.

2. Device moves into the STBY state (Monitored or LP_STBY): When PF09 is going into any of the STBY states, it is assumed the system is going into low-power operation without safety critical operation, therefore the FCCU interface will be reset to the default XRESET operation (FCC0 ignored, FCCU1 = XRESET input).

During the STBY state, the FCCU1 pin will be able to detect an XRESET event as long as the XRESET input is enabled in the STBY state (XRST_STBY_EN = 1)

3. Device goes through a Power-up sequence due to a Turn-off event or a hard reset: When the PF09 goes through a turn-off cycle due to a power off or hard reset, the turn-off FCCU interface will be reset to the default XRESET operation (FCC0 ignored, FCCU1 = XRESET input) and the MCU must request the transition to full bistable mode via the SYS_CMD[7:0] bits once it has performed its corresponding booting sequence.

14.7.3 Single-ended FCCU-level monitoring

When the FCCUx is set in level monitoring mode (OTP_FCCUx_MODE[1:0] = 01), each FCCUx input pin can be used to monitor an independent single-ended error signal.

The FCCUx_POL bit is used to set the polarity to detect a fault condition on each pin independently.

Table 211. FCCUx fault detection in single-ended mode

FCCUx_POL	Fault polarity detection
0	Fault when FCCUx = low
1	Fault when FCCUx = high

In single-ended level monitoring, the selection of the pullup or pulldown resistor is done based on the pin polarity, to allow a fault detection upon a pin disconnection.

Table 212. Pull resistor selection in single-ended level monitoring

FCCUx_RPULL_EN	FCCUx_POL	Internal pull resistor
0	X	FCCUx tri-stated
1	0	FCCUx pulldown
1	1	FCCUx pullup

14.7.4 Single-ended FCCU PWM monitoring

When the FCCUx is set in PWM monitoring mode (OTP_FCCUx_MODE[1:0] = 10), each FCCUx pin can be used to monitor an independent single-ended PWM error signal.

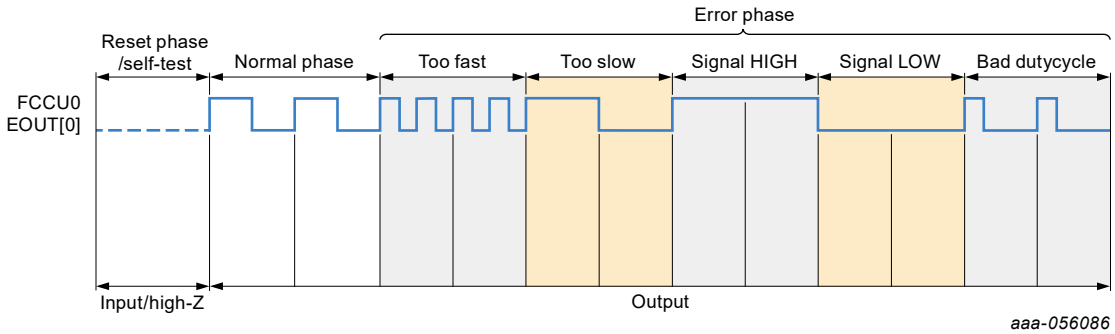


Figure 45. FCCU single-ended PWM operation

In single-ended FCCU PWM error monitoring, the FCCUx input is used to monitor a square waveform error signal. An FCCU fault condition is reported if the signal on the FCCUx pin observes any of the following conditions:

Table 213. FCCUx error conditions

FCCUx Status	Condition	Error type
HIGH	Longer than t_{FCCU_LF}	Too slow
HIGH	Shorter than t_{FCCU_HF}	Too fast
LOW	Longer than t_{FCCU_LF}	Too slow
LOW	Shorter than t_{FCCU_HF}	Too fast

The FCCUx_RPULL_EN bit is used to enable or disable the internal pulldown resistor in the corresponding input.

Table 214. FCCUx internal pull resistor selection in single-ended PWM mode

FCCUx_RPULL_EN	FCCUx internal pull resistor
0	Pull-down disabled
1	Pull-down Enabled

14.7.5 FCCU diagnostics

In single-ended mode (Level or PWM modes) each FCCUx pin is provided with an independent interrupt flag FCCUx_I to report a fault condition on the corresponding FCCU pin. An FCCUx_I interrupt will assert the INTB pin if the interrupt is not masked.

The FCCUx_S bit provides the real time status of the corresponding FCCUx input.

Table 215. FCCUx sense bit

FCCUx_S	FCCUx sense bit
0	No error mode
1	FCCU error detected

In bistable mode, the FCCU will report the fault conditions through the FCCU0_I bit, and the FCCU0_M bit controls the interrupt mask for the FCCU interface. An FCCU0_I interrupt will assert the INTB pin if the interrupt is not masked.

In bistable operation the FCCU0_S bit provides the real time fault status of the FCCU interface.

Table 216. FCCU0 sense bit

FCCU0_S	FCCU0 sense bit
0	No error mode
1	FCCU error detected

14.7.6 Electrical characteristics

Table 217. FCCU electrical characteristics

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and TA = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{IL_FCCUx}	FCCUx low input level threshold • Maximum voltage to ensure a low state	–	–	$0.3*V_{DDIO}$	V
V_{IH_FCCUx}	FCCUx high input level threshold	$0.7*V_{DDIO}$	–	–	V

Table 217. FCCU electrical characteristics...*continued*

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and TA = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• Minimum voltage to ensure a high state				
V_{HYST_FCCUx}	FCCUx input voltage hysteresis	0.1	–	0.4	V
R_{PD_FCCUx}	FCCUx internal pull-down • FCCUx_RPULL_EN = 1	400	800	1300	kΩ
R_{PU_FCCUx}	FCCUx internal pullup to VDDIO • FCCUx_RPULL_EN = 1	100	200	400	kΩ
t_{FCCUx_DBNC0}	FCCUx debounce time in PWM mode	0.8	1	1.2	µs
t_{FCCUx_DBNC1}	FCCUx debounce time • FCCUx_DBNC[1:0] = 00	1	3	4	µs
t_{FCCUx_DBNC2}	FCCUx debounce time • FCCUx_DBNC[1:0] = 01	4	6	8	µs
t_{FCCUx_DBNC3}	FCCUx debounce time • FCCUx_DBNC[1:0] = 10	8	12	16	µs
t_{FCCUx_DBNC4}	FCCUx debounce time • FCCUx_DBNC[1:0] = 11	16	20	24	µs
t_{FCCUx_HF}	FCCUx high-frequency detection time	6	7.75	10	µs
t_{FCCUx_LF}	FCCUx low-frequency detection time	51	64	80	µs

14.8 ABIST

The PF09 implements an analog built-in self test (ABIST) routine to evaluate the integrity of the voltage monitors, safety I/Os and other internal safety-related blocks. ABIST is intended to verify a minimum requirement for ASIL B systems to ensure the internal voltage monitoring circuits are able to notify the logic controller of an OV or UV condition using an internal reference.

The following blocks will be tested during ABIST:

- OV and UV comparators for each individual SWx, LDOx and VAON supply
- OV and UV comparators for each individual VMONx input.
- OV comparator for the internal VDIG supply.
- OV comparator for the internal VANA supply.
- TSD comparator for the thermal monitor
- RSTB pin is tested for short to high conditions
- FS0B pin is tested for short to high conditions

If any of the comparators is not able to toggle during ABIST, the corresponding ABIST flag will be set to 1 to allow the MCU to inspect the fault condition and prevent unsafe operation. The ABIST flags cannot be cleared manually, and they can be cleared only after a new ABIST test is performed and passed.

Table 218. ABIST flags

ABIST flags	Description
AB_SWx_OV	SWx OV monitor ABIST flag
AB_SWx_UV	SWx UV monitor ABIST flag

Table 218. ABIST flags...*continued*

ABIST flags	Description
AB_LDOx_OV	LDOx OV monitor ABIST flag
AB_LDOx_UV	LDOx UV monitor ABIST flag
AB_VAON_OV	VAON OV monitor ABIST flag
AB_VAON_UV	VAON UV monitor ABIST flag
AB_VMONx_OV	VMONx OV monitor ABIST flag
AB_VMONx_UV	VMONx UV monitor ABIST flag
AB_VDIG_OV	VDIG OV monitor ABIST flag
AB_VANA_OV	VANA OV monitor ABIST flag
AB_TSD_NOK	Thermal shutdown comparator ABIST flag
AB_RSTB_NOK	RSTB ABIST flag
AB_FS0B_NOK	FS0B ABIST flag

ABIST is part of the larger self-test routine, but can also be performed separately (see Section 14.9). When ABIST is performed as part of the self-test routine, an ABIST error is not considered to be a self-test routine error. This allows the MCU to debug and take action after reset. When an ABIST error is present, however, the PF09 will not release FS0B until a new ABIST is requested and passed. An exception to this rule occurs when FS0B is used as a safety output.

When FS0B is used as a safety output, an ABIST failure on the FS0B will be considered a critical failure, because the FS0B pin is in charge of maintaining an initial safe state for the system at power up. This kind of failure will cause the self-test to fail and assert the STEST_NOK flag, to prevent the system from powering up with an FS0B short-to-high condition.

14.9 ABIST on demand

A system command is provided to perform an ABIST on demand during the SYSTEM ON states. When the SYS_CMD = 0x55, the control logic will perform an ABIST routine to verify all OV/UV monitoring circuits listed below:

- OV/UV comparators for each individual SWx, LDOx and VAON supply
- OV/UV comparators for each individual VMONx input
- OV monitor for the internal VDIG supply
- OV monitor for the internal VANA supply
- TSD comparator for the thermal monitor

When the ABIST on demand is requested, the ABIST routine will be performed only on voltage regulators and external VMON enabled at the time it is requested.

When the FS0B is operating in Active Safe state, if a failure condition is found during the ABIST on demand command, the FS0B will be asserted immediately to place the system in a safe state. The PF09 will not be able to release the FS0B pin until a new ABIST is requested and passed successfully.

14.10 Logic built-in self-test (LBIST)

14.10.1 Startup LBIST

In devices targeting a high safety integrity level (ASIL D/SIL 2), an LBIST routine is provided to ensure the functional integrity of the logic gates controlling the safety mechanism within the digital control unit.

When LBIST is available in the system, it will be performed during the power-on event when the OTP fuses are loaded. Because the LBIST routine requires a considerable amount of time to be performed, the system designer must take into consideration the extra time needed for the LBIST test for every power-on cycle.

During the LBIST routine, the PF09 will test the logic gates controlling the following safety-related mechanisms:

- OV/UV monitoring logic and deglitchers
- FCCU inputs
- ERRMON input
- Watchdog management
- Dynamic CRC
- FS0B control logic (on main)
- PGOOD control logic
- DMS interface logic (on main)

If the LBIST routine is failed at power-up, the PF09 will not be able to start a power-up sequence to prevent a startup with a potential single-point or latent failure.

For debugging purposes, the LBIST_STATUS[1:0] bits are provided to read the status/result of the LBIST during the DBGOFF state in the event the LBIST has failed.

Table 219. LBIST status bits

LBIST_STATUS[1:0]	LBIST status
00	LBIST not executed
01	Test in progress
10	LBIST Failed
11	LBIST Passed

14.10.2 LBIST on demand

The LBIST on-demand routine can be requested at any time during the RUN state by sending the system command SYS_CMD = 0x4A. It is intended to provide coverage for latent failures in the digital signals controlling the safety mechanism on an automotive system with very long drive cycles, or an industrial system with always-on operating cycles.

To request LBIST on demand:

1. Read all save the Registers content:
   - LDO1_SEQ[7:0]
   - LDO2_SEQ[7:0]
   - LDO3_SEQ[7:0]
   - SW1_SEQ[7:0]
   - SW2_SEQ[7:0]
   - SW3_SEQ[7:0]
   - SW4_SEQ[7:0]
   - SW5_SEQ[7:0]
   - VAON_SEQ[7:0]
   - VAON[1:0]
   - VLDO1_RUN[4:0]
   - VLDO2_RUN[4:0]
   - VLDO3_RUN[4:0]
   - VSW1_RUN[7:0]

- VSW2_RUN[7:0]
- VSW3_RUN[7:0]
- VSW4_RUN[7:0]
- VSW5_RUN[7:0]
- VSELECT_EN
- LDO1_RUN_EN
- LDO2_RUN_EN
- LDO3_RUN_EN
- SW1_RUN_MODE[1:0]
- SW2_RUN_MODE[1:0]
- SW3_RUN_MODE[1:0]
- SW4_RUN_MODE[1:0]
- SW5_RUN_MODE[1:0]

2. Initiate request for LBIST on demand by sending SYS_CMD = 0x4A
3. Wait until the LBIST flag "LBIST_DONE_I" is set to "1"
4. Write back the registers content to the registers
5. Clear the LBIST flag (LBIST_DONE_I)
6. Release FS0B

When an LBIST on-demand routine is started, the device will assert the FS0B pin to set the system into a safe state. It will perform the LBIST routine while maintaining functional operation such as providing proper output voltage regulation.

The PF09 will test the logic gates controlling the following safety related mechanisms:

- OV/UV monitoring logic and deglitchers
- FCCU inputs
- ERRMON input
- Watchdog management
- Dynamic CRC
- FS0B control logic (on main)
- PGOOD control logic
- DMS interface logic (on main)

During LBIST on demand, the RSTB pin remains released to ensure the MCU is still out of reset and in control of the system operation, in order to maintain a safe state during the execution of the LBIST routine.

When the MCU is requesting an LBIST on demand, it knows it will enter a non-monitored condition, therefore it should stop any critical operation and enter a safe state until the LBIST_DONE interrupt is provided. The system can inspect the result for the LBIST routine and proceed to release FS0B via I^2C communication.

The LBIST_STATUS[1:0] bits will be used to read the status/result of the LBIST after the LBIST_DONE interrupt is generated (see Table 219).

If the LBIST routine fails, the PF09 will not be able to release the FS0B pin until a new LBIST on-demand routine is requested and LBIST passes.

To prevent a WD desynchronization during LBIST on demand, if the watchdog monitoring is enabled, the WD counter will be temporarily halted during the LBIST routine and it will regain operation when the LBIST_DONE_I flag is cleared. At this point, the system will be able to re-synchronize the WD when it clears the LBIST_DONE_I flag.

The FS0B will not release if the LBIST_DONE_I flag is asserted.

14.11 Dynamic CRC (DCRC)

The PF09 features a dynamic cyclic redundancy check (DCRC) routine to check the integrity of the functional and OTP configuration registers. The dynamic CRC is able to detect bit-flips in the configuration registers that could lead to a potential single-point or latent failure.

A base CRC code is calculated and stored in memory every time a successful I^2C transaction is made on the functional registers. The base CRC will be used as the reference value to compare with the check CRC code calculated every 5 ms.

If the check CRC code is different from the base CRC code, the dynamic CRC routine is considered a bad dynamic CRC and the PF09 will generate a DCRC_I interrupt to report the fault condition. The dynamic CRC interrupt will assert the INTB pin if the interrupt is not masked.

The dynamic CRC routine is performed within the PF09 logic and does not require any interaction with the system MCU, however, a fault condition in the dynamic CRC will require the MCU to evaluate and try to correct the fault condition, to ensure proper operation of the PMIC.

A control flag DCRC_FLG bit is provided to help manage a dynamic CRC failure. The DCRC_FLG will be set when a bad dynamic CRC condition is present, and the MCU must clear the flag by writing a 1 to it after taking corrective action. When the DCRC_FLG is cleared, the PF09 will perform a new CRC check to ensure the registers' configuration has been corrected and is able to return to safe operation.

A dynamic CRC fault condition can have two levels of severity:

1. The first level of severity includes all fault conditions affecting any of the functional registers. This type of fault can be addressed and fixed by the MCU during the SYSTEM ON states.

The second level of severity includes a fault condition affecting any of the OTP configuration registers. This type of fault cannot be cleared by the MCU directly, and the MCU must take proper action to request a PMIC restart to force a clean OTP reload at power up.

A dynamic CRC fault condition should be managed as follows:

1. When a dynamic CRC fault condition is present, the PF09 will notify the MCU and set the system into a safe state by asserting the FS0B pin.
2. The MCU must verify and/or reload the expected configuration in the functional registers before trying to clear the DCRC_FLG.
3. The MCU must clear the DCRC_FLG to force a new dynamic CRC calculation and read back the flag again.
4. If the DCRC_FLG was successfully cleared, it means the low-severity fault condition has been cleared, and the MCU can proceed to release the FS0B again.
5. If the DCRC_FLG flag is still present after clearing the DCRC_FLG, it means the high-severity fault is on the OTP registers and cannot be fixed. In this scenario, the MCU must place the system into a safe state before it can request a power-down event via the PWRON pin, or by sending a turnoff event via the SYS_CMD registers (0xA5).

Fault conditions in the OTP registers will be mostly latent failures, therefore it is acceptable to allow the system to perform a safe turnoff event to avoid a sudden stop of operation causedby the PMIC.

In devices with lower safety integrity level (ASIL B) where the FS0B pin is used as a programmable fault status output, the dynamic CRC can also drive the FS0B if FS0B_DCRC = 1. This allows the system to prioritize the dynamic CRC fault condition over a regular interrupt.

The strategy to service the dynamic CRC fault is the same, regardless the mode of operation of the FS0B.

14.12 Digital machine supervisor

In devices targeting high safety integrity levels (ASIL D / SIL 2) with the FS0B operating in an active safe state, the PF09 features an NXP proprietary digital machine supervisor (DMS) block to ensure the main digital control

unit in charge of the voltage generation and safety monitoring functions is healthy and operational. The DMS is intended to provide high coverage to detect single-point and latent faults due to random faults in the main digital control unit (DCU).

The DMS is a fully independent, standalone mechanism with a dedicated internal digital supply and clock generation, as well as its own independent logic performing key sanity checks on the main digital control logic.

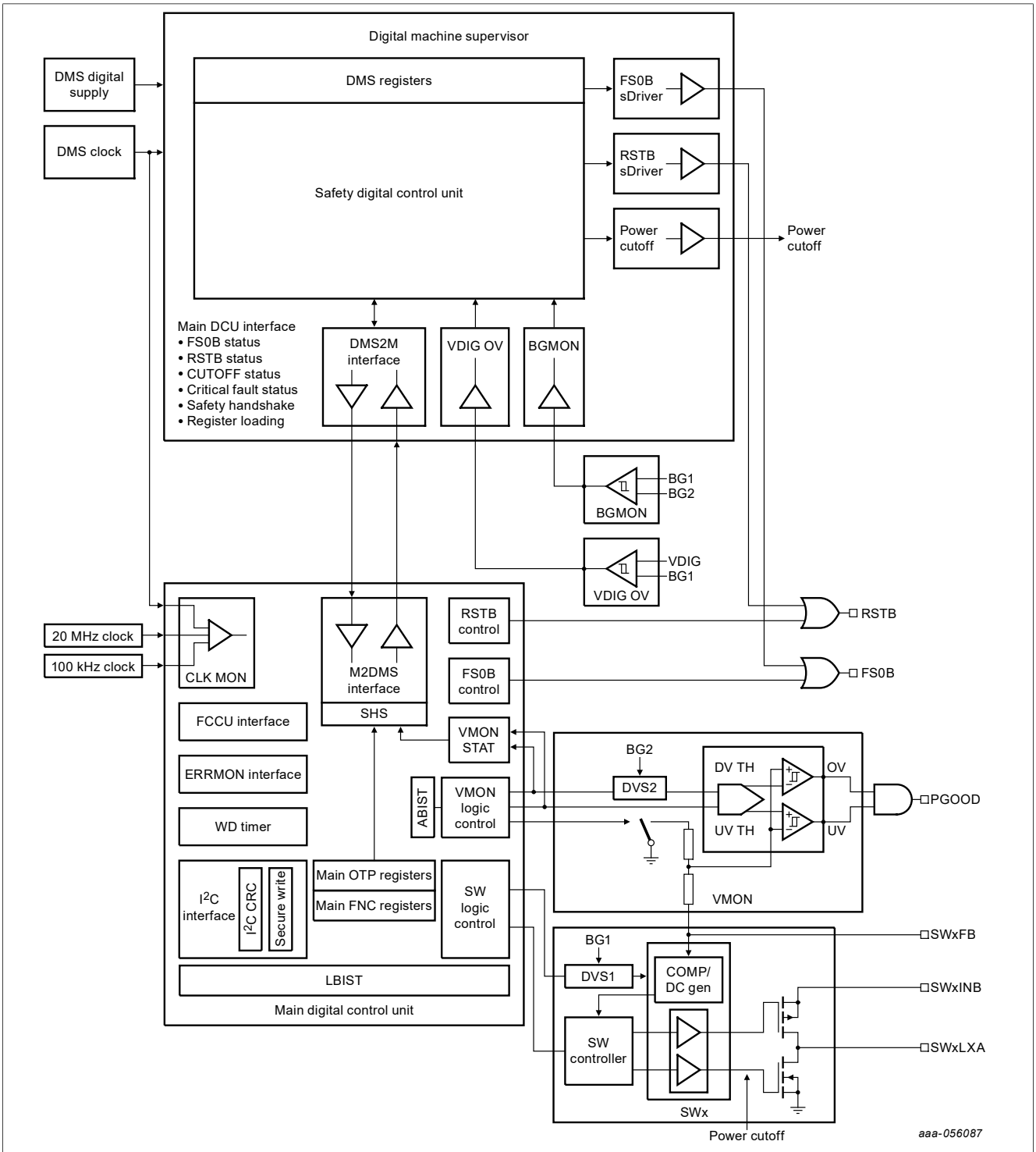


Figure 46. Digital machine supervisor block diagram

Because the DMS is intended to detect and protect against random failures in the main control logic, such failures are considered critical and not fixable at the system level. However random conditions may lead to temporary failures that may return to normal operation before they can be considered to be critical failures.

Each temporary fault condition will cause the DMS to assert the FS0B pin and set the corresponding interrupt. If the fault condition was cleared before it was considered a critical fault, and the system MCU is still responsive, it can go ahead and clear the interrupt and proceed to release the FS0B pin to resume normal operation.

A persistent fault condition will cause the DMS to assert the FS0B and take a strong protective action against a critical fault condition, as defined in the DMS OTP configuration registers.

The DMS provides secondary control of the system safety output (FS0B) and system reset signal (RSTB), to ensure the system is placed in a known safe state when a safety-critical fault condition is found in the digital control unit.

During system operation, the main digital control unit (DCU) has full control of the FS0B and RSTB pins. If the main DCU becomes unresponsive or there is a failure that may affect the ability of the main DCU to detect a failure, the DMS will take control of the safety outputs and assert the pins to place the system in a safe state.

The power cutoff signals in the DMS block provide direct control of the power stage of the voltage regulators, allowing the DMS to disable the output of the power supplies in the event of a critical system failure.

Critical faults leading to a non-functional digital controller will result in the DMS forcing a safe state until the condition is removed and the digital circuit is able to recover logic control.

Critical faults detected by the DMS but still maintaining the main logic operation will result in the DMS forcing a safe state and requesting the main digital control unit to move into the Deep Fail-safe state (DFS). The PF09 can then exit the DFS state based on the OTP configuration for this state.

14.12.1 DMS safety coverage

The independent power supply (VDIG_DMS) is provided to eliminate common-cause failures with respect to the main digital supply, allowing the DMS to detect a fault condition in the main digital controller due to a bad VDIG supply.

The independent DMS clock is provided to eliminate common-cause faults with respect to the main system clocks, allowing the DMS to detect fault conditions in the main digital controller due to clock drift or stuck-at condition.

A bidirectional safety handshake protocol (SHS) is provided to verify that the main digital control unit is responsive. The safety handshake uses key information to verify the integrity of the DMS configuration registers and the real-time status of the logic signal controlling the voltage monitoring circuits.

The safety handshake protocol is designed in such way that It behaves as a self-redundant mechanism that is able to check for single-point or latent failures in the main digital control unit, as well as latent failures in the DMS block itself.

Dedicated input-monitoring signals are also provided to ensure proper operation of key analog blocks that may result in a single-point or latent failure in the main logic controller. These blocks include the main VDIG_OV monitoring and the bandgap comparator, providing a higher level of protection against a random fault that could cause the main digital control unit to become unresponsive, and therefore unable to react.

14.12.2 DMS safety configuration

The severity of the reaction to the various fault conditions is programmable in the main OTP registers. The DMS configuration registers, however, are passed to and stored in the dedicated DMS logic control unit, to ensure the DMS block can perform proper monitoring even if the main logic is lost.

14.12.2.1 Safety handshake configuration registers

A single handshake failure will assert the FS0B pin and set the SHS_I interrupt. The OTP_SHS_RSTB[2:0] bits are provided to set the number of bad safety-handshake transactions needed to cause the RSTB to be asserted and generate a critical fault condition.

Table 220. SHS faults to assert RSTB

OTP_SHS_RSTB[2:0]	SHS faults to assert RSTB	Maximum latency
000	1 HS fault	100 µs
001	2 HS faults	300 µs
010	4 HS faults	700 µs
011	8 HS faults	1,500 µs
100	16 HS faults	3100 µs
101	32 HS faults	6300 µs
110	64 HS faults	12,700 µs
111	No RSTB asserted	Infinite

OTP_SHS_CUTOFF[2:0] bits are provided to set the number of bad safety-handshake transactions needed before the DMS can take full control of the voltage regulators and disable the power stage via the power-cutoff signals.

Table 221. SHS faults to power cutoff

OTP_SHS_CUTOFF[2:0]	HS faults to power cutoff	Maximum latency
000	1 HS fault	100 µs
001	2 HS faults	300 µs
010	4 HS faults	700 µs
011	8 HS faults	1500 µs
100	16 HS faults	3100 µs
101	32 HS faults	6300 µs
110	64 HS faults	12700 µs
111	No Power Cutoff	Infinite

14.12.2.2 Bandgap monitor fault protection

When the DMS detects a drift between the internal bandgaps, the DMS will assert the FS0B output and the BGMON_I interrupt will be set. If the BGMON fault condition is temporary, no critical fault is generated, but the BGMON_I flag and the FS0B output remain asserted until the MCU is able to clear the BGMON flag and release the FS0B.

If the BGMON fault conditions are persistent, the OTP_BGM_RSTB[1:0] bits set the debounce time before the DMS sends a critical fault notification to assert the RSTB pin.

Table 222. BGMON RSTB debounce time to assert RSTB via the DMS

OTP_BGM_RSTB[1:0]	BGMON RSTB debounce
00	No assertion
01	10 µs

Table 222. BGMON RSTB debounce time to assert RSTB via the DMS*...continued*

OTP_BGM_RSTB[1:0]	BGMON RSTB debounce
10	100 µs
11	500 µs

The BGM_CUTOFF[1:0] bits set the debounce time before the DMS sends a critical fault notification and disables the power stages of the voltage regulators.

Table 223. BGMON debounce time to enable the power cutoff via the DMS

OTP_BGM_CUTOFF[1:0]	BGMON power cutoff debounce
00	No Power Cutoff
01	10 µs
10	100 µs
11	500 µs

14.12.2.3 VDIG_OV monitor fault protection

When the DMS detects a fault condition on the VDIG_OV monitor, the DMS will assert the FS0B output and the VDIG_OV_I interrupt will be set. If the VDIG_OV fault condition is temporary, no critical fault will be generated, but the VDIG_OV_I flag and the FS0B output remain asserted until the MCU is able to clear the VDIG_OV flag and release the FS0B.

If the VDIG OV fault condition is persistent, the OTP_VDIGOV_RSTB[1:0] bits set the debounce time before the DMS sends a critical fault to assert the RSTB pin.

Table 224. VDIG_OV debounce time to assert RSTB via the DMS

OTP_VDIGOV_RSTB[1:0]	VDIG OV RSTB debounce
00	No Assertion
01	10 µs
10	100 µs
11	500 µs

If the VDIG OV fault condition is persistent, the OTP_VDIGOV_CUTOFF[1:0] bits set the debounce time before the DMS sends a critical fault to disable the power stages of the voltage regulators.

Table 225. VDIG_OV debounce time to enable the power cutoff via the DMS

OTP_VDIGOV_CUTOFF[1:0]	VDIG OV power cutoff debounce
00	No power cutoff
01	10 µs
10	100 µs
11	500 µs

14.12.3 Electrical characteristics

Table 226. DMS electrical characteristics

All parameters are specified at TA = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and TA = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{DIG_DMS}	DMS digital supply voltage	1.55	1.6	1.65	V
F_{CLK_DMS}	DMS clock frequency	1.9	2	2.1	MHz
T_{SHS_REQ}	Safety handshake request period	190	200	210	µs
t_{SHS_CHK}	Safety handshake response check time	60	–	100	µs
t_{BGM_DGL}	BGMON input fault deglitch time	475	500	525	µs
t_{BGM_RSTB1}	BGMON RSTB debounce • OTP_BGM_RSTB[1:0] = 01	9.5	10	10.5	µs
t_{BGM_RSTB2}	BGMON RSTB debounce • OTP_BGM_RSTB[1:0] = 10	95	100	105	µs
t_{BGM_RSTB3}	BGMON RSTB debounce • OTP_BGM_RSTB[1:0] = 11	475	500	525	µs
$t_{BGM\_CUTOFF1}$	BGMON CUTOFF debounce • OTP_BGM_CUTOFF[1:0] = 01	9.5	10	10.5	µs
$t_{BGM\_CUTOFF2}$	BGMON CUTOFF debounce • OTP_BGM_CUTOFF[1:0] = 10	95	100	105	µs
$t_{BGM\_CUTOFF3}$	BGMON CUTOFF debounce • OTP_BGM_CUTOFF[1:0] = 11	475	500	525	µs
t_{VDIGOV_DGL}	VDIG OV input fault deglitch time	90	100	110	µs
t_{VDIGOV_RSTB1}	VDIG OV RSTB debounce • OTP_VINOV_RSTB[1:0] = 01	9.5	10	10.5	µs
t_{VDIGOV_RSTB2}	VDIG OV RSTB debounce • OTP_VINOV_RSTB[1:0] = 10	95	100	105	µs
t_{VDIGOV_RSTB3}	VDIG OV RSTB debounce • OTP_VINOV_RSTB[1:0] = 11	475	500	525	µs
$t_{VDIGOV\_CUTOFF1}$	VDIG OV CUTOFF debounce • OTP_VINOV_CUTOFF[1:0] = 01	9.5	10	10.5	µs
$t_{VDIGOV\_CUTOFF2}$	VDIG OV CUTOFF debounce • OTP_VINOV_CUTOFF[1:0] = 10	95	100	105	µs
$t_{VDIGOV\_CUTOFF3}$	VDIG OV CUTOFF debounce • OTP_VINOV_CUTOFF[1:0] = 11	475	500	525	µs

15 PF09 register map

15.1 Functional registers

The digital control unit resets the I^{2}C bits differently according to their use and reset type. The following reset types are available in the functional registers:

Table 227. I^{2}C register reset conditions

Reset type	Description
VDIG_POR	Bits are reset when the VDIG_POR is crossed on the rising edge. • Full power cycle (VIN remove) • Returning from ULPOFF state Fault flags are intended to hold fault data through a power-on cycle (LPOFF) and a DFS cycle.
BIST	Bits are reset during LBIST, ABIST or self test. Bits are loaded with the result of the test.
SC	Bits self-clear after a write.
PWRUP_SEQ	Reset with default value before starting a Power-up sequence (power on and hard reset)
OFF_OTP	Bits are loaded directly from the OTP mirror registers. Reset occurs at the following times • Upon entering LPOFF • Right before entering the Power-up sequence • During a hard-reset event.
SOFT_RST	Reset with default value before starting a Power-up sequence (power on and hard reset) and after a soft reset.
SOFT_OTP_RST	Bits are loaded directly from the OTP mirror registers. Reset occurs at the following times • Upon entering LPOFF • Right before entering the Power-up sequence • During a hard reset event. • During a soft reset (if programmed to do so)

Table 228. I^{2}C bit type definitions

Bit type	Description
R	Read-only: writing to this bit will have no effect.
W	Write-only: reading this bit will return a fixed value.
RW	Read and write: Can read and write data to this bit
RW1C	Read current value of the bit, write 1 to clear the bit. Writing 0 will have no effect.
RWRO	Bit is read/write in the test mode (for debug purposes), and read-only in normal operation.

Table 229. Functional register map

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	DEVICE_ID	MSB	FS_ID[2:0]			DEV_ID[4:0]				
		0000_0000	R	R	R	R	R	R	R	R
0x01	DEVICE_FAM	MSB	DEV_FAM[7:0]							
		0000_1001	R	R	R	R	R	R	R	R
0x02	REV_ID	MSB	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			

Table 229. Functional register map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		0011_0000	R	R	R	R	R	R	R	R
0x03	PROG_ID1	MSB	—	—	—	PROG_IDH[4:0]				
		0000_0000	—	—	—	R	R	R	R	R
0x04	PROG_ID2	MSB	—	—	PROG_IDL[5:0]					
		0000_0000	—	—	R	R	R	R	R	R
0x05	SYSTEM_INT	MSB	EWARN_I	GPIO_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
		0000_0000	R	R	R	R	R	R	R	R
0x06	STATUS1_INT	MSB	SDWN_I	FREQ_RDY_I	DCRC_I	I2C_CRC_I	PWRUP_I	PWRDN_I	FSYNC_FLT_I	VIN_OV_I
		0000_0000	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x07	STATUS1_MSK	MSB	SDWN_M	FREQ_RDY_M	DCRC_M	I2C_CRC_M	PWRUP_M	PWRDN_M	FSYNC_FLT_M	VIN_OV_M
		1111_0111	RW	RW	RW	RW	RW	RW	RW	RW
0x08	STATUS1_SNS	MSB	—	—	—	—	—	—	FSYNC_FLT_S	VIN_OV_S
		0000_0000	—	—	—	—	—	—	R	R
0x09	STATUS2_INT	MSB	VANA_OV_I	VDIG_OV_I	BGMON_I	CLKMON_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
		0000_0000	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x0A	STATUS2_MSK	MSB	VANA_OV_M	VDIG_OV_M	BGMON_M	CLKMON_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M
		1111_1111	RW	RW	RW	RW	RW	RW	RW	RW
0x0B	STATUS2_SNS	MSB	VANA_OV_S	VDIG_OV_S	BGMON_S	CLKMON_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
		0000_0000	R	R	R	R	R	R	R	R
0x0C	STATUS3_INT	MSB	—	—	LDO1EN_I	VSELECT_I	WD_ERROR_I	BAD_CMD_I	LBIST_DONE_I	SHS_I
		0000_0000	—	—	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x0D	STATUS3_MSK	MSB	—	—	LDO1EN_M	VSELECT_M	WD_ERROR_M	BAD_CMD_M	LBIST_DONE_M	SHS_M
		0011_1111	—	—	RW	RW	RW	RW	RW	RW
0x0E	SW_MODE_INT	MSB	DVSMAX_I	DVSMIN_I	—	SW5_MODE_I	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
		0000_0000	RW1C	RW1C	—	RW1C	RW1C	RW1C	RW1C	RW1C
0x0F	SW_MODE_MSK	MSB	DVSMAX_M	DVSMIN_M	—	SW5_MODE_M	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
		1101_1111	RW	RW	—	RW	RW	RW	RW	RW
0x10	SW_ILIM_INT	MSB	SW1LS_OCP_I	—	—	SW5_IL_I	SW4_IL_I	SW3_IL_I	SW2_IL_I	SW1_IL_I
		0000_0000	RW1C	—	—	RW1C	RW1C	RW1C	RW1C	RW1C
0x11	SW_ILIM_MSK	MSB	SW1LS_OCP_M	—	—	SW5_IL_M	SW4_IL_M	SW3_IL_M	SW2_IL_M	SW1_IL_M
		1001_1111	RW	—	—	RW	RW	RW	RW	RW
0x12	SW_ILIM_SNS	MSB	—	—	—	SW5_IL_S	SW4_IL_S	SW3_IL_S	SW2_IL_S	SW1_IL_S
		0000_0000	—	—	—	R	R	R	R	R
0x13	LDO_ILIM_INT	MSB	—	—	—	—	—	LDO3_IL_I	LDO2_IL_I	LDO1_IL_I
		0000_0000	—	—	—	—	—	RW1C	RW1C	RW1C
0x14	LDO_ILIM_MSK	MSB	—	—	—	—	—	LDO3_IL_M	LDO2_IL_M	LDO1_IL_M
		0000_0111	—	—	—	—	—	RW	RW	RW
0x15	LDO_ILIM_SNS	MSB	—	—	—	—	—	LDO3_IL_S	LDO2_IL_S	LDO1_IL_S
		0000_0000	—	—	—	—	—	R	R	R
0x16	SW_UV_INT	MSB	MON2_UV_I	MON1_UV_I	—	SW5_UV_I	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
		0000_0000	RW1C	RW1C	—	RW1C	RW1C	RW1C	RW1C	RW1C
0x17	SW_UV_MSK	MSB	MON2_UV_M	MON1_UV_M	—	SW5_UV_M	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
		1101_1111	RW	RW	—	RW	RW	RW	RW	RW
0x18	SW_UV_SNS	MSB	MON2_UV_S	MON1_UV_S	—	SW5_UV_S	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
		0000_0000	R	R	—	R	R	R	R	R
0x19	SW_OV_INT	MSB	MON2_OV_I	MON1_OV_I	—	SW5_OV_I	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
		0000_0000	RW1C	RW1C	—	RW1C	RW1C	RW1C	RW1C	RW1C
0x1A	SW_OV_MSK	MSB	MON2_OV_M	MON1_OV_M	—	SW5_OV_M	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M

Table 229. Functional register map...*continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		1101_1111	RW	RW	—	RW	RW	RW	RW	RW
0x1B	SW_OV_SNS	MSB	MON2_OV_S	MON1_OV_S	—	SW5_OV_S	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
		0000_0000	R	R	—	R	R	R	R	R
0x1C	LDO_UV_INT	MSB	—	—	—	—	VAON_UV_I	LDO3_UV_I	LDO2_UV_I	LDO1_UV_I
		0000_0000	—	—	—	—	RW1C	RW1C	RW1C	RW1C
0x1D	LDO_UV_MSK	MSB	—	—	—	—	VAON_UV_M	LDO3_UV_M	LDO2_UV_M	LDO1_UV_M
		0000_1111	—	—	—	—	RW	RW	RW	RW
0x1E	LDO_UV_SNS	MSB	—	—	—	—	VAON_UV_S	LDO3_UV_S	LDO2_UV_S	LDO1_UV_S
		0000_0000	—	—	—	—	R	R	R	R
0x1F	LDO_OV_INT	MSB	—	—	—	—	VAON_OV_I	LDO3_OV_I	LDO2_OV_I	LDO1_OV_I
		0000_0000	—	—	—	—	RW1C	RW1C	RW1C	RW1C
0x20	LDO_OV_MSK	MSB	—	—	—	—	VAON_OV_M	LDO3_OV_M	LDO2_OV_M	LDO1_OV_M
		0000_1111	—	—	—	—	RW	RW	RW	RW
0x21	LDO_OV_SNS	MSB	—	—	—	—	VAON_OV_S	LDO3_OV_S	LDO2_OV_S	LDO1_OV_S
		0000_0000	—	—	—	—	R	R	R	R
0x22	PWRON_INT	MSB	—	—	—	PWRON_8S_I	PWRON_4S_I	PWRON_3S_I	PWRON_2S_I	PWRON_1S_I
		0000_0000	—	—	—	RW1C	RW1C	RW1C	RW1C	RW1C
0x23	PWRON_MSK	MSB	—	—	—	PWRON_8S_M	PWRON_4S_M	PWRON_3S_M	PWRON_2S_M	PWRON_1S_M
		0001_1111	—	—	—	RW	RW	RW	RW	RW
0x24	IO_INT	MSB	—	—	ERRMON_I	FCCU0_I	FCCU1_I	PGOOD_FLT_I	FS0B_FLT_I	RSTB_FLT_I
		0000_0000	—	—	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x25	IO_MSK	MSB	—	—	ERRMON_M	FCCU0_M	FCCU1_M	PGOOD_FLT_M	FS0B_FLT_M	RSTB_FLT_M
		0011_1111	—	—	RW	RW	RW	RW	RW	RW
0x26	IO_SNS	MSB	—	GPIO4_S	GPIO3_S	FCCU0_S	FCCU1_S	PGOOD_S	FS0B_S	RSTB_S
		0000_0000	—	R	R	R	R	R	R	R
0x27	IOSHORT_SNS	MSB	GPIO2_S	GPIO1_S	FS0B_S2H	FS0B_S2L	PGOOD_S2H	PGOOD_S2L	RSTB_S2H	RSTB_S2L
		0000_0000	R	R	R	R	R	R	R	R
0x28	ABIST_OV1	MSB	AB_VMON2_OV	AB_VMON1_OV	—	AB_SW5_OV	AB_SW4_OV	AB_SW3_OV	AB_SW2_OV	AB_SW1_OV
		0000_0000	R	R	—	R	R	R	R	R
0x29	ABIST_OV2	MSB	AB_VANA_OV	AB_VDIG_OV	AB_DMSVDIG_OV	—	AB_VAON_OV	AB_LDO3_OV	AB_LDO2_OV	AB_LDO1_OV
		0000_0000	R	R	R	—	R	R	R	R
0x2A	ABIST_UV1	MSB	AB_VMON2_UV	AB_VMON1_UV	—	AB_SW5_UV	AB_SW4_UV	AB_SW3_UV	AB_SW2_UV	AB_SW1_UV
		0000_0000	R	R	—	R	R	R	R	R
0x2B	ABIST_UV2	MSB	—	—	—	—	AB_VAON_UV	AB_LDO3_UV	AB_LDO2_UV	AB_LDO1_UV
		0000_0000	—	—	—	—	R	R	R	R
0x2C	ABIST_IO	MSB	—	—	—	—	—	AB_TSD_NOK	AB_FS0B_NOK	AB_RSTB_NOK
		0000_0000	—	—	—	—	—	R	R	R
0x2D	TEST_FLAGS	MSB	—	—	VOTP_NOK	OTP_NOK	TRIM_NOK	STEST_NOK	LBIST_STATUS[1:0]	
		0000_0000	—	—	RWRO	RWRO	RWRO	RWRO	RWRO	RWRO
0x2E	HFAULT_FLAGS	MSB	—	UVDET_FAIL	RSTB_FAIL	PU_FAIL	RESET_FAIL	FLTCNT_FAIL	REG_FAIL	TSD_FAIL
		0000_0000	—	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x2F	FAULT_FLAGS	MSB	DCRC_FLG	DFS_FLG	VIN_OV_FLG	XFAIL_FLG	WD_FLG	XRESET_FLG	SFAULT_FLG	HFAULT_FLG
		0000_0000	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x30	FS0B_CFG	MSB	FS0B_DCRC	FS0B_DFS	FS0B_VIN_OV	FS0B_XFAIL	FS0B_WD	FS0B_XRESET	FS0B_SFAULT	FS0B_HFAULT
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x31	FCCU_CFG	MSB	FCCU1_RPULL_EN	FCCU0_RPULL_EN	FCCU1_DBNC[1:0]		FCCU0_DBNC[1:0]		FCCU1_POL	FCCU0_POL
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW

Table 229. Functional register map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x32	RSTB_CFG1	MSB	RSTB_SOFTRST[1:0]		—	ERRMON_ RESET	FCCU1_RESET[1:0]		FCCU0_RESET[1:0]	
		0000_0000	RW	RW	—	RW	RW	RW	RW	RW
0x33	SYSTEM_CMD	MSB	SYS_CMD[7:0]							
		0000_0000	W	W	W	W	W	W	W	W
0x34	FS0B_CMD	MSB	FS0B_RELEASE[7:0]							
		0000_0000	W	W	W	W	W	W	W	W
0x35	SECURE_WR1	MSB	RANDOM_GEN[7:0]							
		0000_0000	R	R	R	R	R	R	R	R
0x36	SECURE_WR2	MSB	RANDOM_CHK[7:0]							
		0000_0000	W	W	W	W	W	W	W	W
0x37	VMON_CFG1	MSB	VIN_OV_EN	VIN_OV_ SDWN	VIN_OV_DBNC[1:0]		OV_DBNC[1:0]		UV_DBNC[1:0]	
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x38	SYS_CFG1	MSB	ERRMON_TIME[1:0]		XRST_DBNC[1:0]		XRST_MODE	XRST_ STBY_EN	STBY_POL	I2C_ SECURE_EN
		0100_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x39	GPO_CFG	MSB	—	—	—	—	GPO4_ SOFTRST_EN	GPO3_ SOFTRST_EN	GPO2_ SOFTRST_EN	GPO1_ SOFTRST_EN
		0000_0000	—	—	—	—	RW	RW	RW	RW
0x3A	GPO_CTRL	MSB	GPO4_STBY	GPO3_STBY	GPO2_STBY	GPO1_STBY	GPO4_RUN	GPO3_RUN	GPO2_RUN	GPO1_RUN
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x3B	PWRUP_CFG	MSB	—	—	—	PD_SEQ_DLY[2:0]			SEQ_TBASE[1:0]	
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x3C	RSTB_PWRUP	MSB	RSTB_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x3D	GPIO1_PWRUP	MSB	GPIO1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x3E	GPIO2_PWRUP	MSB	GPIO2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x3F	GPIO3_PWRUP	MSB	GPIO3_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x40	GPIO4_PWRUP	MSB	GPIO4_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x41	VMON1_ PWRUP	MSB	VMON1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x42	VMON2_ PWRUP	MSB	VMON2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x43	SW1_PWRUP	MSB	SW1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x44	SW2_PWRUP	MSB	SW2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x45	SW3_PWRUP	MSB	SW3_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x46	SW4_PWRUP	MSB	SW4_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x47	SW5_PWRUP	MSB	SW5_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x48	LDO1_PWRUP	MSB	LDO1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x49	LDO2_PWRUP	MSB	LDO2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x4A	LDO3_PWRUP	MSB	LDO3_SEQ[7:0]							

Table 229. Functional register map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x4B	VAON_PWRUP	MSB	VAON_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x4C	FREQ_CTRL	MSB	FSYNCOUT_EN	FSYNC_RANGE	FSS_MODE	FSS_EN	CLK_FREQ[3:0]			
		0100_0100	RW	RW	RW	RW	RW	RW	RW	RW
0x4D	PWRON_CFG	MSB	—	—	—	PWRON_DBNC[1:0]		PWRON_RST_EN	TRESET[1:0]	
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x4E	WD_CTRL1	MSB	WD_SEED[7:0]							
		1010_0101	RW	RW	RW	RW	RW	RW	RW	RW
0x4F	WD_CTRL2	MSB	WD_CLEAR[7:0]							
		0000_0000	W	W	W	W	W	W	W	W
0x50	WD_CFG1	MSB	WD_EN	WD_OK_FCD[2:0]			WD_DURATION[3:0]			
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x51	WD_CFG2	MSB	WD_SOFTRST_EN	WD_NOK_MAX[2:0]			RESET_MAX[3:0]			
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x52	WD_CNT1	MSB	—	WD_NOK_CNT[2:0]			RESET_CNT[3:0]			
		0000_0000	—	R	R	R	RW	RW	RW	RW
0x53	WD_CNT2	MSB	—	WD_OK_CNT[2:0]			—	—	—	—
		0000_0000	—	R	R	R	—	—	—	—
0x54	FAULT_CFG	MSB	TIMER_FAULT[3:0]				FAULT_MAX_CNT[3:0]			
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x55	FAULT_CNT	MSB	FS_CNT[3:0]				FAULT_CNT[3:0]			
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x56	DFS_CNT	MSB	RETRY_CNT[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x57	AMUX_CFG	MSB	—	—	AMUX_EN	AMUX_SEL[4:0]				
		0000_0000	—	—	RW	RW	RW	RW	RW	RW
0x58	VMON1_RUN_CFG	MSB	VMON1_EN	—	—	VMON1_RUN[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0x59	VMON1_STBY_CFG	MSB	—	—	—	VMON1_STBY[4:0]				
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x5A	VMON1_CTRL	MSB	—	—	VMON1_OVTH_STBY	VMON1_UVTH_STBY	VMON1_TMASK[1:0]		VMON1_SOFTRST_EN	VMON1_PG_EN
		0000_0001	—	—	RW	RW	RW	RW	RW	RW
0x5B	VMON2_RUN_CFG	MSB	VMON2_EN	—	—	VMON2_RUN[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0x5C	VMON2_STBY_CFG	MSB	—	—	—	VMON2_STBY[4:0]				
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x5D	VMON2_CTRL	MSB	—	—	VMON2_OVTH_STBY	VMON2_UVTH_STBY	VMON2_TMASK[1:0]		VMON2_SOFTRST_EN	VMON2_PG_EN
		0000_0001	—	—	RW	RW	RW	RW	RW	RW
0x5E	SW1_VRUN	MSB	VSW1_RUN[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x5F	SW1_VSTBY	MSB	VSW1_STBY[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x60	SW1_MODE	MSB	—	SW1_OVTH_STBY	SW1_UVTH_STBY	SW1_SLOWDVS	SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]	
		0001_0000	—	RW	RW	RW	RW	RW	RW	RW
0x61	SW1_CFG1	MSB	SW1LS_OCP	SW1_ILIM[1:0]		SW1_DVS[1:0]		SW1_PH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW

Table 229. Functional register map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x62	SW1_CFG2	MSB	SW1_UV_BYP	SW1_OV_BYP	SW1_IL_BYP	SW1_UV_STATE	SW1_OV_STATE	SW1_FLT_REN	SW1_SOFTRST_EN	SW1_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x63	SW2_VRUN	MSB	VSW2_RUN[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x64	SW2_VSTBY	MSB	VSW2_STBY[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x65	SW2_MODE	MSB	—	SW2_OVTH_STBY	SW2_UVTH_STBY	SW2_SLOWDVS	SW2_STBY_MODE[1:0]		SW2_RUN_MODE[1:0]	
		0001_0000	—	RW	RW	RW	RW	RW	RW	RW
0x66	SW2_CFG1	MSB	—	SW2_ILIM[1:0]		SW2_DVS[1:0]		SW2_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x67	SW2_CFG2	MSB	SW2_UV_BYP	SW2_OV_BYP	SW2_IL_BYP	SW2_UV_STATE	SW2_OV_STATE	SW2_FLT_REN	SW2_SOFTRST_EN	SW2_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x68	SW3_VRUN	MSB	VSW3_RUN[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x69	SW3_VSTBY	MSB	VSW3_STBY[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x6A	SW3_MODE	MSB	—	SW3_OVTH_STBY	SW3_UVTH_STBY	SW3_SLOWDVS	SW3_STBY_MODE[1:0]		SW3_RUN_MODE[1:0]	
		0001_0000	—	RW	RW	RW	RW	RW	RW	RW
0x6B	SW3_CFG1	MSB	—	SW3_ILIM[1:0]		SW3_DVS[1:0]		SW3_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x6C	SW3_CFG2	MSB	SW3_UV_BYP	SW3_OV_BYP	SW3_IL_BYP	SW3_UV_STATE	SW3_OV_STATE	SW3_FLT_REN	SW3_SOFTRST_EN	SW3_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x6D	SW4_VRUN	MSB	VSW4_RUN[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x6E	SW4_VSTBY	MSB	VSW4_STBY[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x6F	SW4_MODE	MSB	—	SW4_OVTH_STBY	SW4_UVTH_STBY	SW4_SLOWDVS	SW4_STBY_MODE[1:0]		SW4_RUN_MODE[1:0]	
		0001_0000	—	RW	RW	RW	RW	RW	RW	RW
0x70	SW4_CFG1	MSB	—	SW4_ILIM[1:0]		SW4_DVS[1:0]		SW4_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x71	SW4_CFG2	MSB	SW4_UV_BYP	SW4_OV_BYP	SW4_IL_BYP	SW4_UV_STATE	SW4_OV_STATE	SW4_FLT_REN	SW4_SOFTRST_EN	SW4_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x72	SW5_VRUN	MSB	VSW5_RUN[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x73	SW5_VSTBY	MSB	VSW5_STBY[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x74	SW5_MODE	MSB	—	SW5_OVTH_STBY	SW5_UVTH_STBY	SW5_SLOWDVS	SW5_STBY_MODE[1:0]		SW5_RUN_MODE[1:0]	
		0001_0000	—	RW	RW	RW	RW	RW	RW	RW
0x75	SW5_CFG1	MSB	—	SW5_ILIM[1:0]		SW5_DVS[1:0]		SW5_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x76	SW5_CFG2	MSB	SW5_UV_BYP	SW5_OV_BYP	SW5_IL_BYP	SW5_UV_STATE	SW5_OV_STATE	SW5_FLT_REN	SW5_SOFTRST_EN	SW5_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x77	LDO1_RUN	MSB	—	—	LDO1_RUN_EN	VLDO1_RUN[4:0]				
		0000_0000	—	—	RW	RW	RW	RW	RW	RW
0x78	LDO1_STBY	MSB	—	—	LDO1_STBY_EN	VLDO1_STBY[4:0]				

Table 229. Functional register map...*continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		0000_0000	—	—	RW	RW	RW	RW	RW	RW
0x79	LDO1_CFG2	MSB	LDO1_ UV_BYP	LDO1_ OV_BYP	LDO1_IL_BYP	LDO1_ UV_STATE	LDO1_ OV_STATE	LDO1_ FLT_REN	LDO1_ SOFTRST_EN	LDO1_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x7A	LDO2_RUN	MSB	VSELECT_EN	—	LDO2_ RUN_EN	VLDO2_RUN[4:0]				
		1000_0000	RW	—	RW	RW	RW	RW	RW	RW
0x7B	LDO2_STBY	MSB	VLDO2MON_TMASK[1:0]		LDO2_ STBY_EN	VLDO2_STBY[4:0]				
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7C	LDO2_CFG2	MSB	LDO2_ UV_BYP	LDO2_ OV_BYP	LDO2_IL_BYP	LDO2_ UV_STATE	LDO2_ OV_STATE	LDO2_ FLT_REN	LDO2_ SOFTRST_EN	LDO2_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x7D	LDO3_RUN	MSB	—	—	LDO3_ RUN_EN	VLDO3_RUN[4:0]				
		0000_0000	—	—	RW	RW	RW	RW	RW	RW
0x7E	LDO3_STBY	MSB	VLDO3MON_TMASK[1:0]		LDO3_ STBY_EN	VLDO3_STBY[4:0]				
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7F	LDO3_CFG2	MSB	LDO3_ UV_BYP	LDO3_ OV_BYP	LDO3_IL_BYP	LDO3_ UV_STATE	LDO3_ OV_STATE	LDO3_ FLT_REN	LDO3_ SOFTRST_EN	LDO3_PG_EN
		0011_1101	RW	RW	RW	RW	RW	RW	RW	RW
0x80	VAON_CFG1	MSB	—	—	—	VAON_TFLT[2:0]			VAON[1:0]	
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x81	VAON_CFG2	MSB	VAON_ UV_BYP	VAON_ OV_BYP	—	VAON_ UV_STATE	VAON_ OV_STATE	VAON_ FLT_REN	VAON_ RESET_EN	VAON_PG_EN
		0001_1101	RW	RW	—	RW	RW	RW	RW	RW
0x82	SYS_DIAG	MSB	—	CTM_TM	DBG_MODE	STATES[4:0]				
		0000_0000	—	R	RW1C	R	R	R	R	R

15.2 Functional register reset conditions

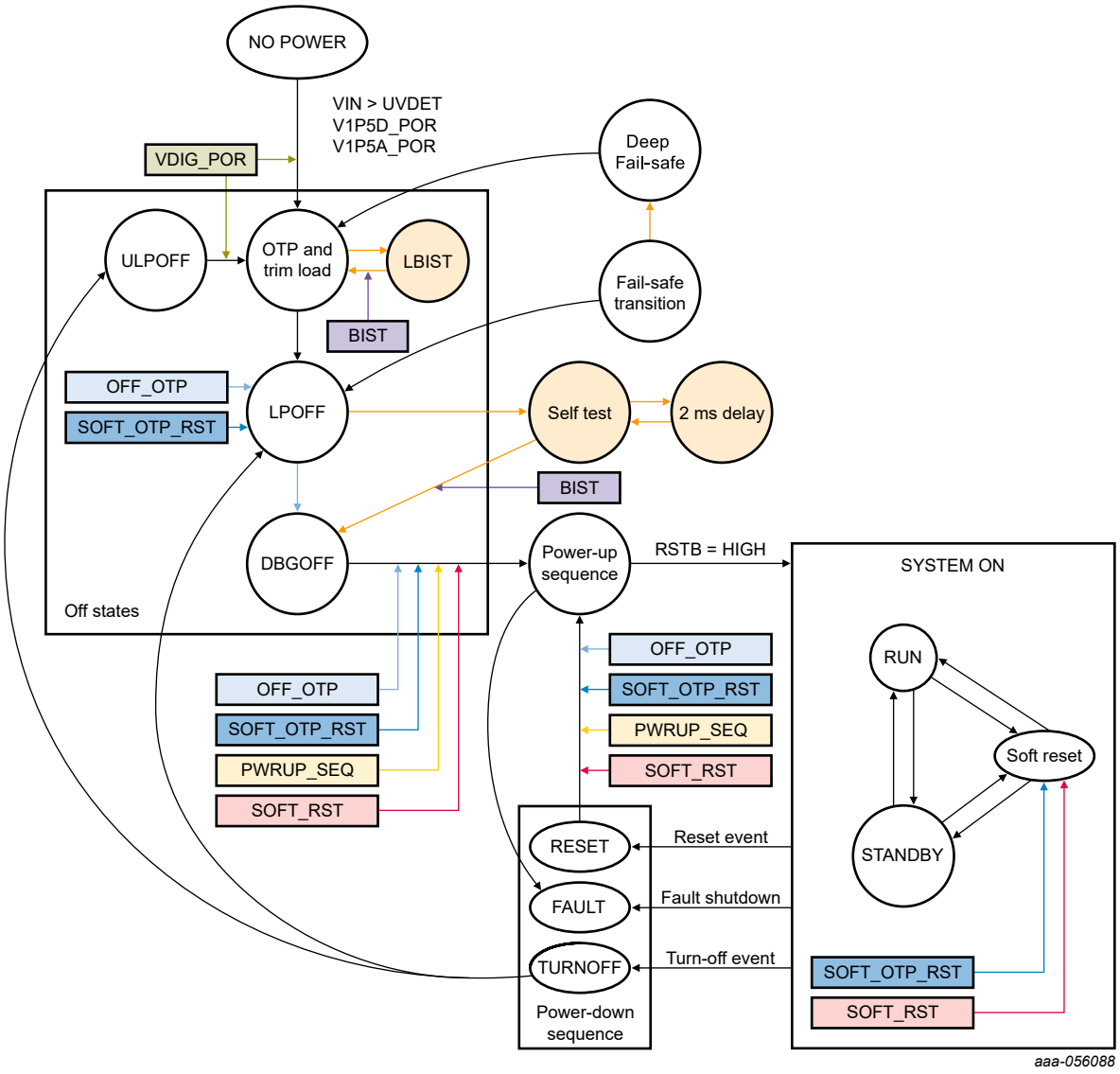


Figure 47. Functional bits reset diagram

All functional registers following either the power up or the soft reset will load the default value from OTP or fixed value when the PF09 is starting a full Power-up sequence, that includes:

1. Transition from the DBGOFF into the Power-up sequence
2. Device performs a hard reset

Only functional registers following the soft reset will be able to reload the default value when a soft reset occurs. provides a list of register characteristics following a soft reset.:

Table 230. Bits reset during soft reset.

Bit Name	Description	Reset Value		Condition
FCCU1_RESET	Reset on FCCU1	0x00	No reset (only FS0B)	Cleared on Soft-Reset, MCU must re-configure the safety reaction.

Table 230. Bits reset during soft reset....*continued*

Bit Name	Description	Reset Value		Condition
FCCU0_RESET	Reset on FCCU0	0x00	No reset (only FS0B)	Cleared on Soft-Reset, MCU must re-configure the safety reaction.
ERRMON_RESET	Reset on ERRMON	0x00	No reset (only FS0B)	Cleared on Soft-Reset, MCU must re-configure the safety reaction.
GPOx_STBY	GPO4 STANDBY control	OTP	Load OTP Value	GPOx_SOFTRST_EN = 0 ➔ Unchanged GPOx_SOFTRST_EN = 1 ➔ Load OTP
GPOx_RUN	GPO4 RUN control	OTP	Load OTP Value	GPOx_SOFTRST_EN = 0 ➔ Unchanged GPOx_SOFTRST_EN = 1 ➔ Load OTP
WD_DURATION	WD Window Duration	OTP	Load OTP Value	WD_SOFTRST_EN = 0 ➔ Unchanged WD_SOFTRST_EN = 1 ➔ Load OTP
VMONx_RUN	VMONx RUN Monitoring Voltage	OTP	Load OTP Value	VMONx_SOFTRST_EN = 0 ➔ Unchanged VMONx_SOFTRST_EN = 1 ➔ Load OTP
VMONx_EN	VMONx Operation	OTP	Load OTP Value	VMONx_SOFTRST_EN = 0 ➔ Unchanged VMONx_SOFTRST_EN = 1 ➔ Load OTP
VMONx_STBY	VMONx STANDBY Monitoring Voltage	OTP	Load OTP Value	VMONx_SOFTRST_EN = 0 ➔ Unchanged VMONx_SOFTRST_EN = 1 ➔ Load OTP
VSWx_RUN	SWx RUN Voltage	OTP	Load OTP Value	SWx_SOFTRST_EN = 0 ➔ Unchanged SWx_SOFTRST_EN = 1 ➔ Load OTP
VSWx_STBY	SWx STANDBY Voltage	OTP	Load OTP Value	SWx_SOFTRST_EN = 0 ➔ Unchanged SWx_SOFTRST_EN = 1 ➔ Load OTP
SWx_STBY_MODE	SWx STANDBY Operation	OTP	Load OTP Value	SWx_SOFTRST_EN = 0 ➔ Unchanged SWx_SOFTRST_EN = 1 ➔ Load OTP
SWx_RUN_MODE	SWx RUN Operation	OTP	Load OTP Value	SWx_SOFTRST_EN = 0 ➔ Unchanged SWx_SOFTRST_EN = 1 ➔ Load OTP
LDOx_RUN_EN	LDOx RUN control	OTP	Load OTP Value	LDOx_SOFTRST_EN = 0 ➔ Unchanged LDOx_SOFTRST_EN = 1 ➔ Load OTP
VLDOx_RUN	LDOx RUN Voltage	OTP	Load OTP Value	LDOx_SOFTRST_EN = 0 ➔ Unchanged LDOx_SOFTRST_EN = 1 ➔ Load OTP
LDOx_STBY_EN	LDOx STANDBY Control	OTP	Load OTP Value	LDOx_SOFTRST_EN = 0 ➔ Unchanged LDOx_SOFTRST_EN = 1 ➔ Load OTP
VLDOx_STBY	LDOx STANDBY Voltage	OTP	Load OTP Value	LDOx_SOFTRST_EN = 0 ➔ Unchanged LDOx_SOFTRST_EN = 1 ➔ Load OTP
VAON	VAON Voltage	OTP	Load OTP Value	VAON_RESET_EN = 0 ➔ Unchanged VAON_RESET_EN = 1 ➔ Load OTP

15.3 OTP registers

Table 231. OTP register color code

Key	Description
OTP only	OTP-only bits are used to set a hardware and software configuration that is not intended to change during the normal system operation.
OTP functional	OTP functional values are used to set the default configuration of the I^2C functional registers at power up. The system can then modify the functional configuration during system operation as required by the application. Not all OTP functional bits have a one-to-one match in the functional registers, however one or more functional bits may set their default value(s) based on the selection of these bits as described in this document.

Table 232. OTP Register Map

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x60	OTP_I2C_CFG	MSB	—	—	—	OTP_I2C_SECURE_EN	OTP_I2C_CRC_EN	OTP_I2C_ADD[2:0]		
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x61	OTP_SYS_CFG1	MSB	OTP_LBIST_BYPASS	OTP_EWARN_TIME[1:0]		OTP_PWRUP_CHK	OTP_STBY_REQ	OTP_LP_STBY	OTP_ERRMON_POL	OTP_STBY_POL
		0000_0100	RW	RW	RW	RW	RW	RW	RW	RW
0x62	OTP_SYS_CFG2	MSB	OTP_VIN_SEL	OTP_SW1LS_EN	OTP_XFAILB_EN	OTP_XFAILB_VAON	OTP_VIN_OV_SDWN	OTP_VIN_OV_EN	OTP_VIN_OV_DBNC[1:0]	
		0000_0000	RW	—	RW	RW	RW	RW	RW	RW
0x63	OTP_SYS_CFG3	MSB	OTP_GPO4_STBY	OTP_GPO3_STBY	OTP_GPO2_STBY	OTP_GPO1_STBY	OTP_SW4CONFIG[1:0]		OTP_SW2CONFIG[1:0]	
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x64	OTP_SYS_CFG4	MSB	OTP_GPIO4_MODE[1:0]		OTP_GPIO3_MODE[1:0]		OTP_GPIO2_MODE[1:0]		OTP_GPIO1_MODE[1:0]	
		0000_0000	RW	RW	RW	RW	—	—	—	RW
0x65	OTP_DFS_CFG	MSB	—	OTP_RETRY_MSK[3:0]				OTP_RETRY_MODE	OTP_RETRY_DFS	OTP_PWRON_DFS
		0000_0001	—	RW	RW	RW	RW	RW	RW	RW
0x66	OTP_DMS_CFG1	MSB	—	OTP_VDIGOV_RSTB[1:0]		OTP_BGM_RSTB[1:0]		OTP_SHS_RSTB[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x67	OTP_DMS_CFG2	MSB	—	OTP_VDIGOV_CUTOFF[1:0]		OTP_BGM_CUTOFF[1:0]		OTP_SHS_CUTOFF[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x68	OTP_FREQ_CFG	MSB	—	OTP_FSYNC_MODE	OTP_FSS_MODE	OTP_FSS_EN	OTP_CLK_FREQ[3:0]			
		0000_0100	—	RW	RW	RW	RW	RW	RW	RW
0x69	OTP_WD_CFG1	MSB	OTP_WD_DURATION[3:0]				—	OTP_WD_WINDOW[1:0]		OTP_WD_EN
		0000_0000	RW	RW	RW	RW	—	RW	RW	RW
0x6A	OTP_WD_CFG2	MSB	—	OTP_WD_NOK_MAX[2:0]			—	OTP_WD_OK_FCD[2:0]		
		0000_0000	—	RW	RW	RW	—	RW	RW	RW
0x6B	OTP_FAULT_CNT	MSB	OTP_TIMER_FAULT[3:0]				OTP_FAULT_MAX_CNT[3:0]			
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x6C	OTP_FAULT_CNT2	MSB	OTP_MAX_FS_CNT[3:0]				OTP_RESET_MAX[3:0]			
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x6D	OTP_RSTB_CFG	MSB	—	—	OTP_RSTB_SOFTRST[1:0]		OTP_RSTB_MODE[1:0]		OTP_RSTB_TSHORT[1:0]	
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0x6E	OTP_FS0B_CFG	MSB	OTP_FS0B_DCRC	OTP_FS0B_DFS	OTP_FS0B_VIN_OV	OTP_FS0B_XFAIL	OTP_FS0B_WD	OTP_FS0B_XRESET	OTP_FS0B_SFAULT	OTP_FS0B_HFAULT
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x6F	OTP_FCCU_CFG	MSB	OTP_FCCU1_MODE[1:0]		OTP_FCCU0_MODE[1:0]		OTP_FCCU1_POL	OTP_FCCU0_POL	OTP_FCCU_DBNC[1:0]	
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW

Table 232. OTP Register Map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x70	OTP_XRESET_CFG	MSB	—	—	—	—	OTP_XRST_STBY_EN	OTP_XRST_MODE	OTP_XRST_DBNC[1:0]	
		0000_0000	—	—	—	—	RW	RW	RW	RW
0x71	OTP_PWRON_CFG	MSB	—	—	OTP_PWRON_MODE	OTP_PWRON_DBNC[1:0]		OTP_PWRON_RST_EN	OTP_TRESET[1:0]	
		0000_0000	—	—	RW	RW	RW	RW	RW	RW
0x72	OTP_SEQ_CFG	MSB	OTP_PD_SEQ_DLY[2:0]			OTP_SEQ_MODE	OTP_SEQ_TSET[1:0]		OTP_SEQ_TBASE[1:0]	
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x73	OTP_RSTB_PWRUP	MSB	OTP_RSTB_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x74	OTP_GPO1_PWRUP	MSB	OTP_GPO1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x75	OTP_GPO2_PWRUP	MSB	OTP_GPO2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x76	OTP_GPO3_PWRUP	MSB	OTP_GPO3_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x77	OTP_GPO4_PWRUP	MSB	OTP_GPO4_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x78	OTP_VMON1_PWRUP	MSB	OTP_VMON1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x79	OTP_VMON2_PWRUP	MSB	OTP_VMON2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7A	OTP_SW1_PWRUP	MSB	OTP_SW1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7B	OTP_SW2_PWRUP	MSB	OTP_SW2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7C	OTP_SW3_PWRUP	MSB	OTP_SW3_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7D	OTP_SW4_PWRUP	MSB	OTP_SW4_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7E	OTP_SW5_PWRUP	MSB	OTP_SW5_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x7F	OTP_LDO1_PWRUP	MSB	OTP_LDO1_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x80	OTP_LDO2_PWRUP	MSB	OTP_LDO2_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x81	OTP_LDO3_PWRUP	MSB	OTP_LDO3_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x82	OTP_VAON_PWRUP	MSB	OTP_VAON_SEQ[7:0]							
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x83	OTP_VMON1_RUN	MSB	OTP_VMON1_UVTH[2:0]			OTP_VMON1_RUN[4:0]				
		0100_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x84	OTP_VMON1_STBY	MSB	OTP_VMON1_OVTH[2:0]			OTP_VMON1_STBY[4:0]				
		0100_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x85	OTP_VMON1_CFG	MSB	—	—	—	—	OTP_VMON1_TSET[1:0]		OTP_VMON1_TMASK[1:0]	
		0000_0000	—	—	—	—	RW	RW	RW	RW
0x86	OTP_VMON2_RUN	MSB	OTP_VMON2_UVTH[2:0]			OTP_VMON2_RUN[4:0]				
		0100_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x87	OTP_VMON2_STBY	MSB	OTP_VMON2_OVTH[2:0]			OTP_VMON2_STBY[4:0]				
		0100_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x88	OTP_VMON2_CFG	MSB	—	—	—	—	OTP_VMON2_TSET[1:0]		OTP_VMON2_TMASK[1:0]	

Table 232. OTP Register Map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		0000_0000	—	—	—	—	RW	RW	RW	RW
0x89	OTP_SW1_VRUN	MSB	OTP_VSW1_RUN[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x8A	OTP_SW1_VSTBY	MSB	OTP_VSW1_STBY[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x8B	OTP_SW1_CFG1	MSB	OTP_SW1_LS_OCP	OTP_SW1_ILIM[1:0]		OTP_SW1_DVS[1:0]		OTP_SW1_PH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x8C	OTP_SW1_CFG2	MSB	OTP_SW1_DVSMAX[3:0]				OTP_SW1_DVSMIN[3:0]			
		1111_1111	RW	RW	RW	RW	RW	RW	RW	RW
0x8D	OTP_SW1_CFG3	MSB	OTP_SW1_2P5TH_HYS	OTP_SW1_LSEL	OTP_SW1_UVTH[2:0]			OTP_SW1_OVTH[2:0]		
		0001_0010	RW	RW	RW	RW	RW	RW	RW	RW
0x8E	OTP_SW1_CFG4	MSB	OTP_SW1_STBY_EN	OTP_SW1_CCOMP[1:0]		OTP_SW1_RCOMP[1:0]		OTP_SW1_GM[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x8F	OTP_SW2_VRUN	MSB	OTP_VSW2_RUN[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x90	OTP_SW2_VSTBY	MSB	OTP_VSW2_STBY[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x91	OTP_SW2_CFG1	MSB	—	OTP_SW2_ILIM[1:0]		OTP_SW2_DVS[1:0]		OTP_SW2_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x92	OTP_SW2_CFG2	MSB	OTP_SW2_DVSMAX[3:0]				OTP_SW2_DVSMIN[3:0]			
		1111_1111	RW	RW	RW	RW	RW	RW	RW	RW
0x93	OTP_SW2_CFG3	MSB	OTP_SW2_2P5TH_HYS	OTP_SW2_LSEL	OTP_SW2_UVTH[2:0]			OTP_SW2_OVTH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x94	OTP_SW2_CFG4	MSB	OTP_SW2_STBY_EN	OTP_SW2_CCOMP[1:0]		OTP_SW2_RCOMP[1:0]		OTP_SW2_GM[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x95	OTP_SW3_VRUN	MSB	OTP_VSW3_RUN[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x96	OTP_SW3_VSTBY	MSB	OTP_VSW3_STBY[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x97	OTP_SW3_CFG1	MSB	—	OTP_SW3_ILIM[1:0]		OTP_SW3_DVS[1:0]		OTP_SW3_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x98	OTP_SW3_CFG2	MSB	OTP_SW3_DVSMAX[3:0]				OTP_SW3_DVSMIN[3:0]			
		1111_1111	RW	RW	RW	RW	RW	RW	RW	RW
0x99	OTP_SW3_CFG3	MSB	OTP_SW3_2P5TH_HYS	OTP_SW3_LSEL	OTP_SW3_UVTH[2:0]			OTP_SW3_OVTH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x9A	OTP_SW3_CFG4	MSB	OTP_SW3_STBY_EN	OTP_SW3_CCOMP[1:0]		OTP_SW3_RCOMP[1:0]		OTP_SW3_GM[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0x9B	OTP_SW4_VRUN	MSB	OTP_VSW4_RUN[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x9C	OTP_SW4_VSTBY	MSB	OTP_VSW4_STBY[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0x9D	OTP_SW4_CFG1	MSB	—	OTP_SW4_ILIM[1:0]		OTP_SW4_DVS[1:0]		OTP_SW4_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0x9E	OTP_SW4_CFG2	MSB	OTP_SW4_DVSMAX[3:0]				OTP_SW4_DVSMIN[3:0]			
		1111_1111	RW	RW	RW	RW	RW	RW	RW	RW

Table 232. OTP Register Map*...continued*

ADDR	REGISTER	DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x9F	OTP_SW4_CFG3	MSB	OTP_SW4_2P5TH_HYS	OTP_SW4_LSEL	OTP_SW4_UVTH[2:0]			OTP_SW4_OVTH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xA0	OTP_SW4_CFG4	MSB	OTP_SW4_STBY_EN	OTP_SW4_CCOMP[1:0]		OTP_SW4_RCOMP[1:0]		OTP_SW4_GM[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xA1	OTP_SW5_VRUN	MSB	OTP_VSW5_RUN[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0xA2	OTP_SW5_VSTBY	MSB	OTP_VSW5_STBY[7:0]							
		0101_1001	RW	RW	RW	RW	RW	RW	RW	RW
0xA3	OTP_SW5_CFG1	MSB	—	OTP_SW5_ILIM[1:0]		OTP_SW5_DVS[1:0]		OTP_SW5_PH[2:0]		
		0000_0000	—	RW	RW	RW	RW	RW	RW	RW
0xA4	OTP_SW5_CFG2	MSB	OTP_SW5_DVSMAX[3:0]				OTP_SW5_DVSMIN[3:0]			
		1111_1111	RW	RW	RW	RW	RW	RW	RW	RW
0xA5	OTP_SW5_CFG3	MSB	OTP_SW5_2P5TH_HYS	OTP_SW5_LSEL	OTP_SW5_UVTH[2:0]			OTP_SW5_OVTH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xA6	OTP_SW5_CFG4	MSB	OTP_SW5_STBY_EN	OTP_SW5_CCOMP[1:0]		OTP_SW5_RCOMP[1:0]		OTP_SW5_GM[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xA7	OTP_LDO1_RUN	MSB	OTP_LDO1_SS	—	—	OTP_VLDO1_RUN[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0xA8	OTP_LDO1_STBY	MSB	OTP_LDO1_STBY_EN	—	—	OTP_VLDO1_STBY[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0xA9	OTP_LDO1_CFG1	MSB	OTP_LDO1LS	—	OTP_LDO1_UVTH[2:0]			OTP_LDO1_OVTH[2:0]		
		0000_0000	RW	—	RW	RW	RW	RW	RW	RW
0xAA	OTP_LDO2_RUN	MSB	OTP_LDO2_SS	—	—	OTP_VLDO2_RUN[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0xAB	OTP_LDO2_STBY	MSB	OTP_LDO2_STBY_EN	—	—	OTP_VLDO2_STBY[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0xAC	OTP_LDO2_CFG1	MSB	OTP_LDO2_MODE[1:0]		OTP_LDO2_UVTH[2:0]			OTP_LDO2_OVTH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xAD	OTP_LDO3_RUN	MSB	OTP_LDO3_SS	—	—	OTP_VLDO3_RUN[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0xAE	OTP_LDO3_STBY	MSB	OTP_LDO3_STBY_EN	—	—	OTP_VLDO3_STBY[4:0]				
		0000_0000	RW	—	—	RW	RW	RW	RW	RW
0xAF	OTP_LDO3_CFG1	MSB	OTP_LDO3_MODE[1:0]		OTP_LDO3_UVTH[2:0]			OTP_LDO3_OVTH[2:0]		
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xB0	OTP_VLDOMON_CFG	MSB	OTP_VLDO3MON_TSET[1:0]		OTP_VLDO3MON_TMASK[1:0]		OTP_VLDO2MON_TSET[1:0]		OTP_VLDO2MON_TMASK[1:0]	
		0000_0000	RW	RW	RW	RW	RW	RW	RW	RW
0xB1	OTP_VAON_CFG1	MSB	—	OTP_VAON_UVTH[1:0]		—	OTP_VAON_OVTH[1:0]		OTP_VAON[1:0]	
		0000_0000	—	RW	RW	—	RW	RW	RW	RW
0xB2	OTP_VAON_CFG2	MSB	—	—	—	—	OTP_VAON_FMODE	OTP_VAON_TFLT[2:0]		
		0000_0000	—	—	—	—	RW	RW	RW	RW
0xB3	OTP_PROG_IDH	MSB	—	—	—	OTP_PROG_IDH[4:0]				
		0000_0000	—	—	—	RW	RW	RW	RW	RW
0xB4	OTP_PROG_IDL	MSB	—	—	OTP_PROG_IDL[5:0]					
		0000_0000	—	—	RW	RW	RW	RW	RW	RW

Note: *Switching regulator compensation bits (OTP_SWx_LSEL, OTP_SWx_CCOMP[1:0], OTP_SWx_RCOMP[1:0], OTP_SWx_GM[2:0]) are intended for part optimization and must be recommended by NXP to ensure proper device operation.*

16 ESD requirements

Table 233. ESD Ratings

Symbol	Description	Min	Typ	Max	Unit
V_{ESDHBM}	Human body model	–	–	2000	V
V_{ESDCDM}	Charge device model • QFN package - all pins	–	–	500	V
$I_{LATCHUP}$	Latch-up current	–	–	100	mA

All ESD specifications will be compliant with the AEC-Q100 specification.

17 Thermal characteristics

Table 234. Thermal characteristics

All parameters are specified up to a junction temperature of 150 °C. All parameters are tested at T_A from −40 °C to 105 °C, to allow headroom for self-heating during operation. If higher T_A operation is required, proper thermal and loading consideration must be made to ensure device operation below the maximum T_J = 150 °C.

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient operating temperature	-40	–	125	°C
T_J	Junction temperature	-40	–	150	°C
T_{ST}	Storage temperature range	-55	–	150	°C
T_{PPRT}	Peak package reflow temperature	–	–	260	°C

Table 235. QFN56 thermal resistance package dissipation ratings

Symbol	Description	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to Ambient Thermal Resistance[1] JESD51-7, 2s2p	–	–	24.4	°C/W
Ψ_{JT}	Junction-to-Top of Package Thermal Characterization Parameter[1] Eight-layer board (4S4P)	–	–	0.2	°C/W
$R_{\theta JC}$	Junction to Case Thermal Resistance[2] JESD51-7, 1s	–	–	1.0	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

18 Operating conditions

Table 236. Operating conditions

All parameters are specified at T_A = -40 to 125 °C, V_{IN} = UVDET to 5.5 V, typical external component values unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V, T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{IN}	Main Input supply voltage	UVDET	–	5.5	V
V_{SWxIN}	SWx regulator input supply[1][2]	UVDET	–	5.5	V
V_{LDO1IN}	LDO1 regulator input supply	1.8	–	5.5	V
V_{LDOxIN}	LDO2 / LDO3 regulator input supply	1.8	–	5.5	V
V_{DDIO}	Typical IO Voltage Supply. (Tolerance: Nominal +/- 7%)	1.8	–	3.3	V
I_{Q_ULPOFF}	Ultra-low power mode quiescent current • VAON regulator disabled • Max IQ Current at T_A = 85 °C • VDDIO = 0 V	–	5	10	µA
I_{Q_LPOFF}	Low-power mode quiescent current • VAON regulator disabled • Max IQ current at T_A = 85 °C • VDDIO = 0 V	–	40	70	µA
I_{Q_SYSON}	SYSTEM ON quiescent current • VAON regulator disabled • All system regulators off • High-frequency clock enabled • VDDIO = 0 V	–	1800	2500	µA
I_{Q_STBY}	STANDBY quiescent current • VAON regulator disabled • All system regulators off • In low-power Standby (OTP_LP_STBY = 1) • High-frequency clock disabled • Max IQ Current at T_A = 85 °C • VDDIO = 0 V	–	100	200	µA
I_{Q_DFS}	Deep Fail-safe (DFS) quiescent current • Max IQ current at T_A = 85 °C • VDDIO = 0 V	–	40	70	µA

[1] VSWxIN must be connected to VIN supply to ensure proper operation of the switching regulators.
[2] Minimum VSWxIN supply must be higher than VSWxOUT + headroom.

19 Package drawing

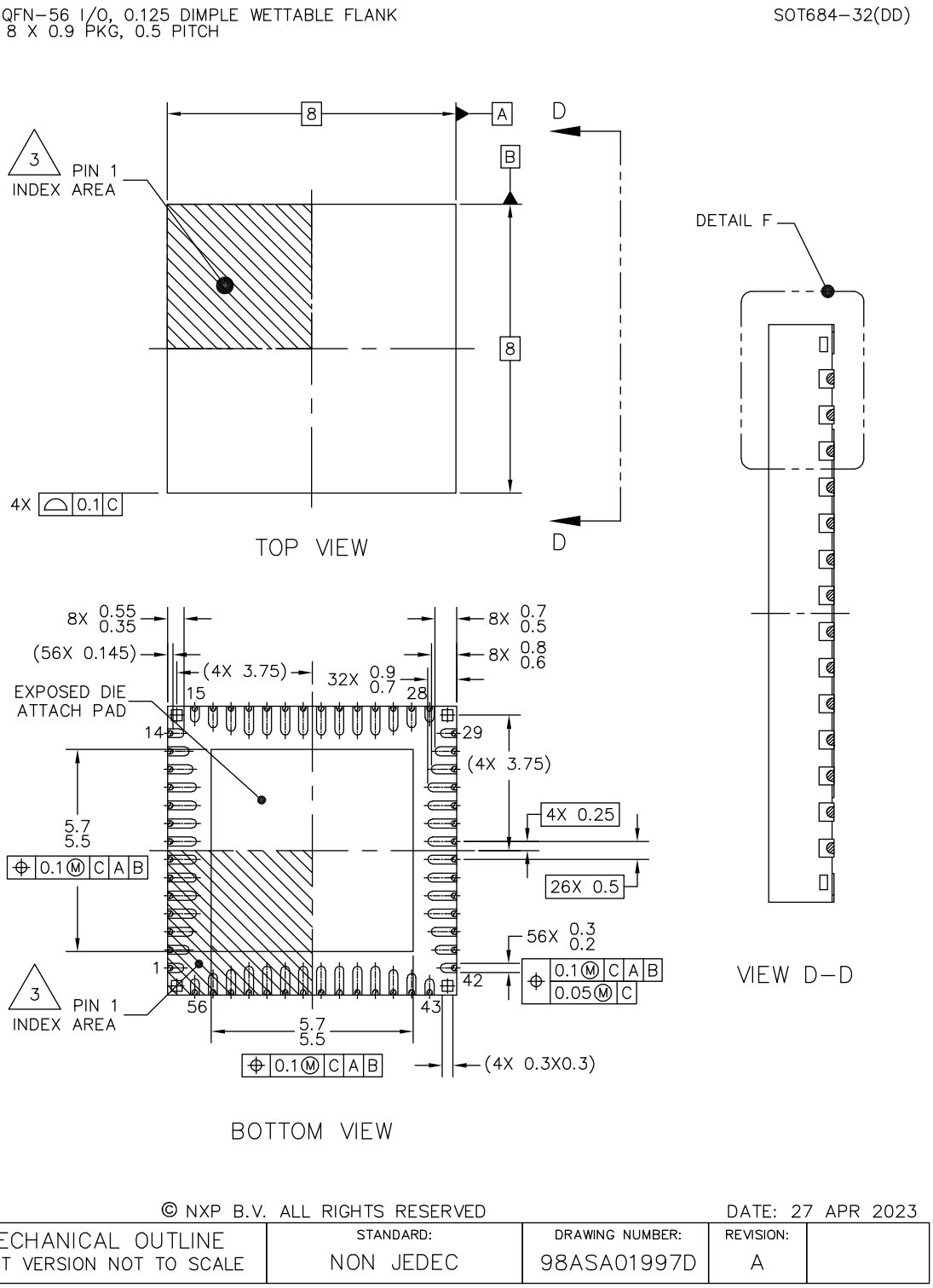
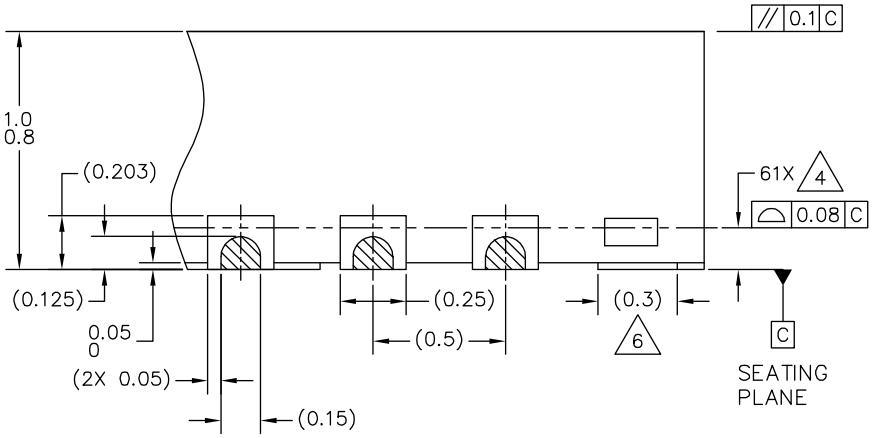


Figure 48. SOT684-32_DD top and bottom views

H–PQFN–56 I/O, 0.125 DIMPLE WETTABLE FLANK
8 X 8 X 0.9 PKG, 0.5 PITCH

SOT684–32(DD)

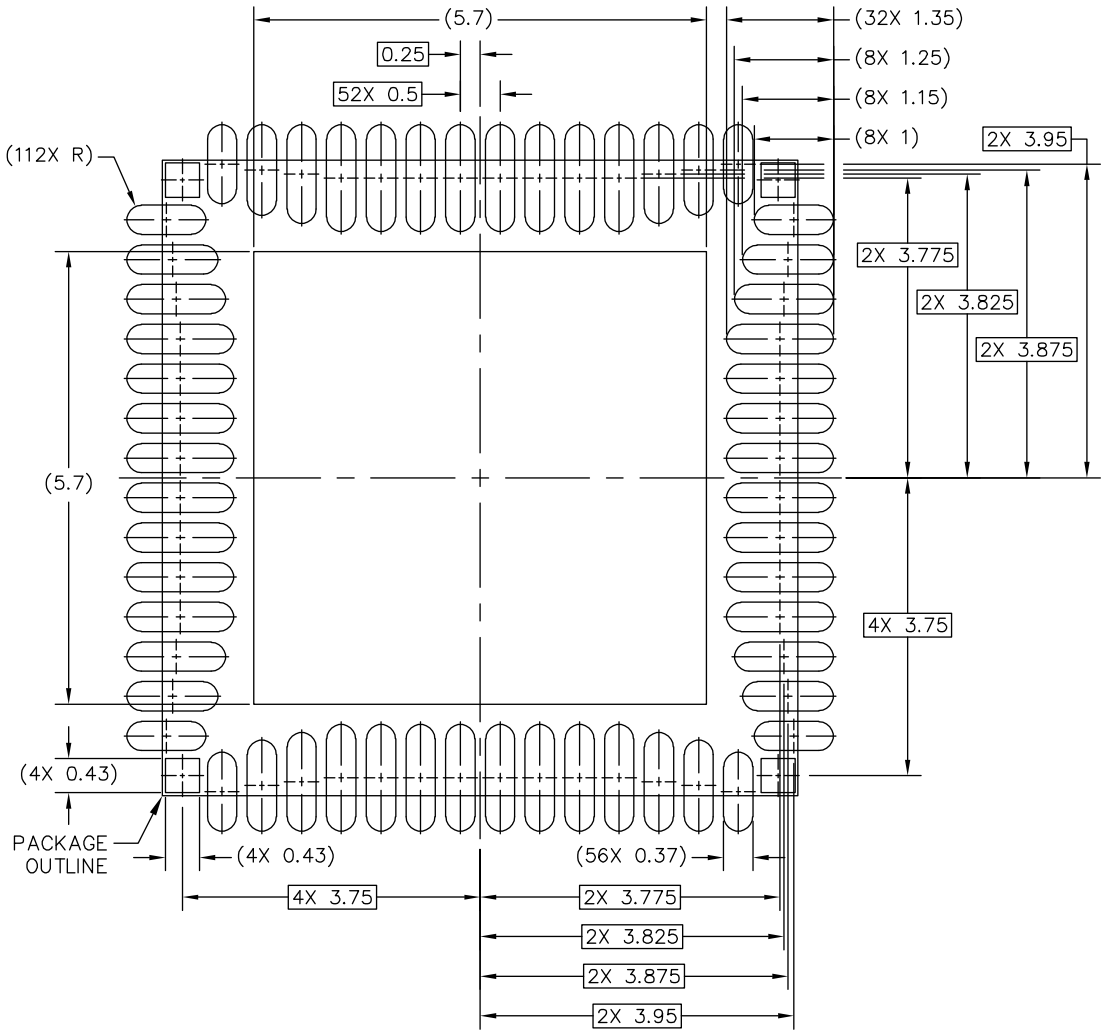


DETAIL F
VIEW ROTATED 90° CW

DATE: 27 APR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01997D	REVISION: A	

Figure 49. Detail F



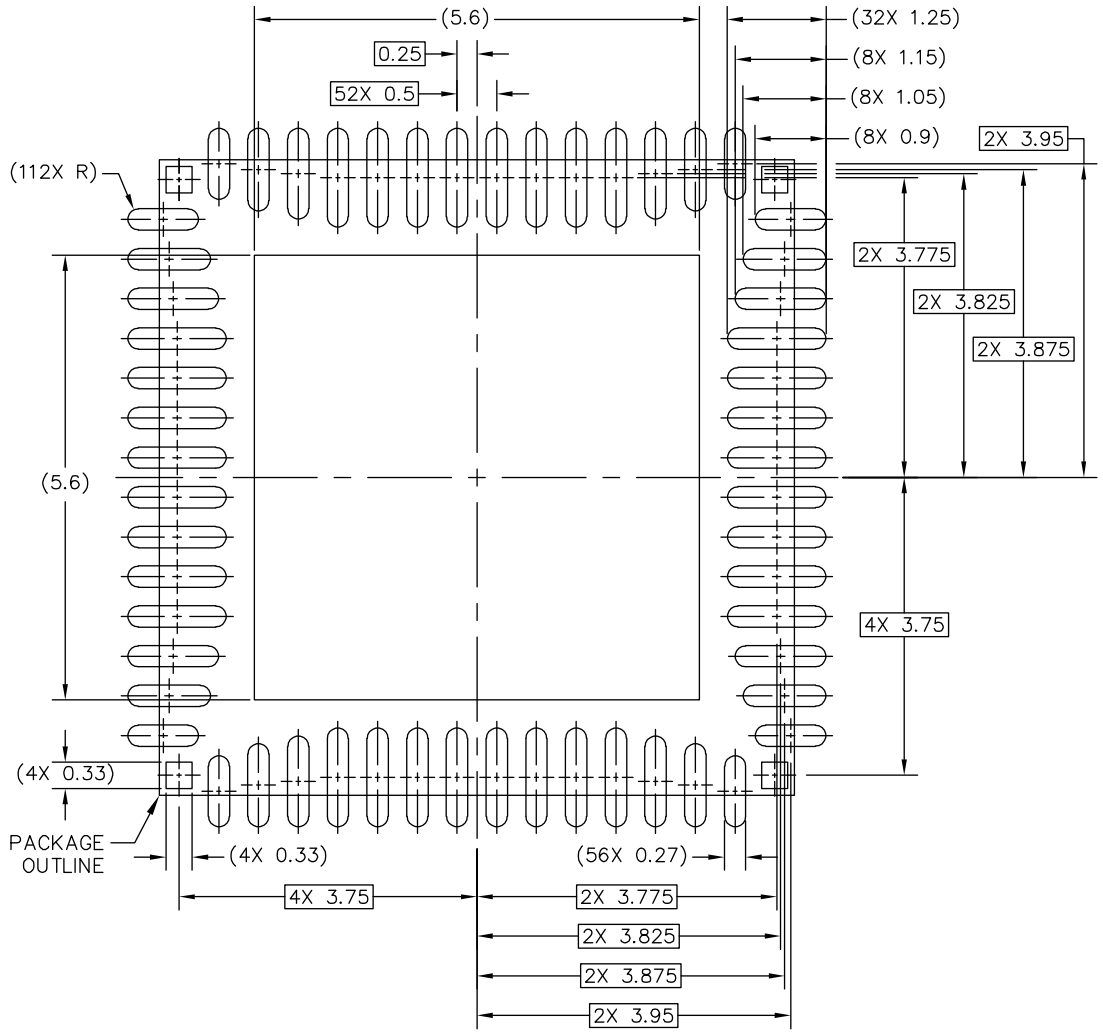
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 27 APR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01997D	REVISION: A	

Figure 50. PCB design guidelines - solder mask opening pattern



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DATE: 27 APR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01997D	REVISION: A	

Figure 51. PCB design guidelines - I/O pads and solderable area

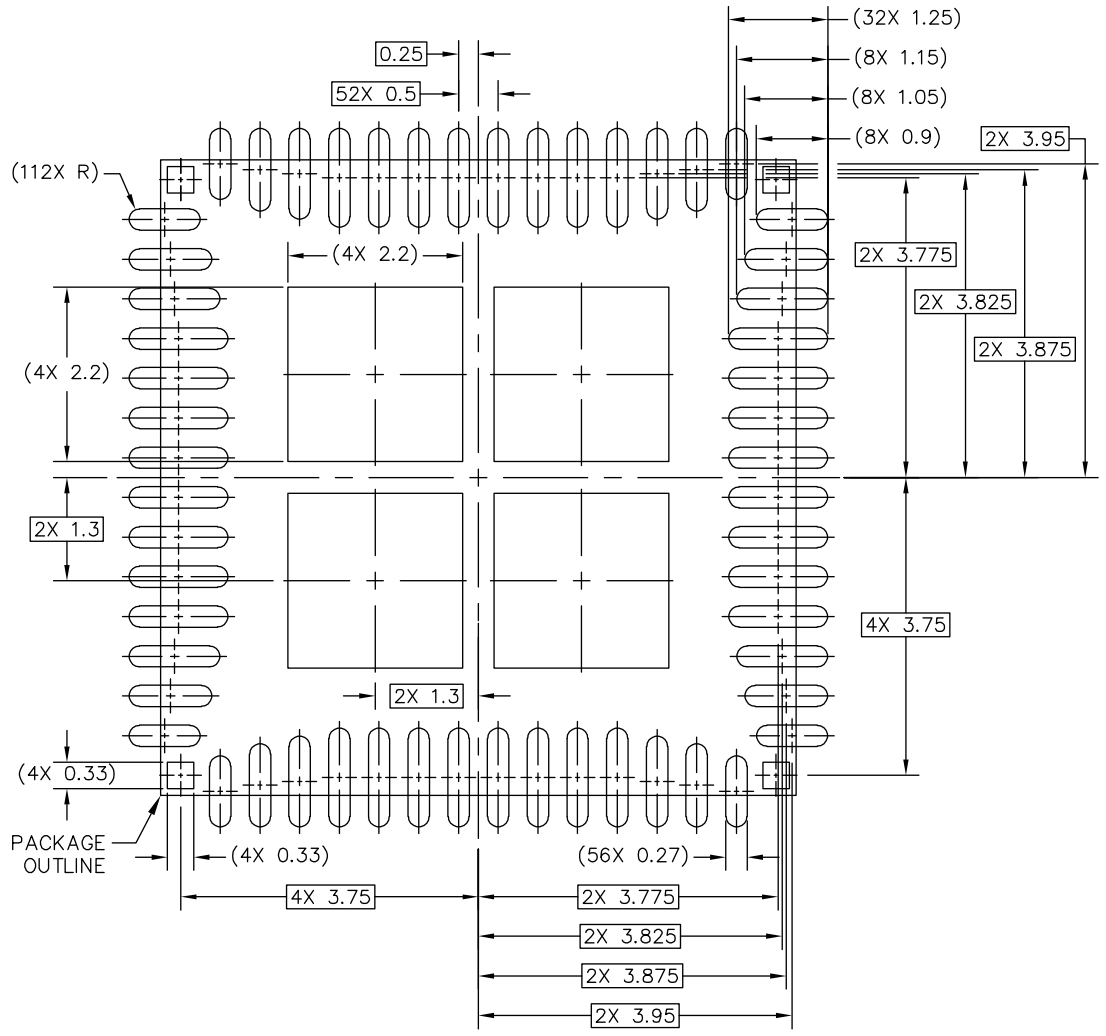

Figure 52. PCB design guidelines - solder paste stencil

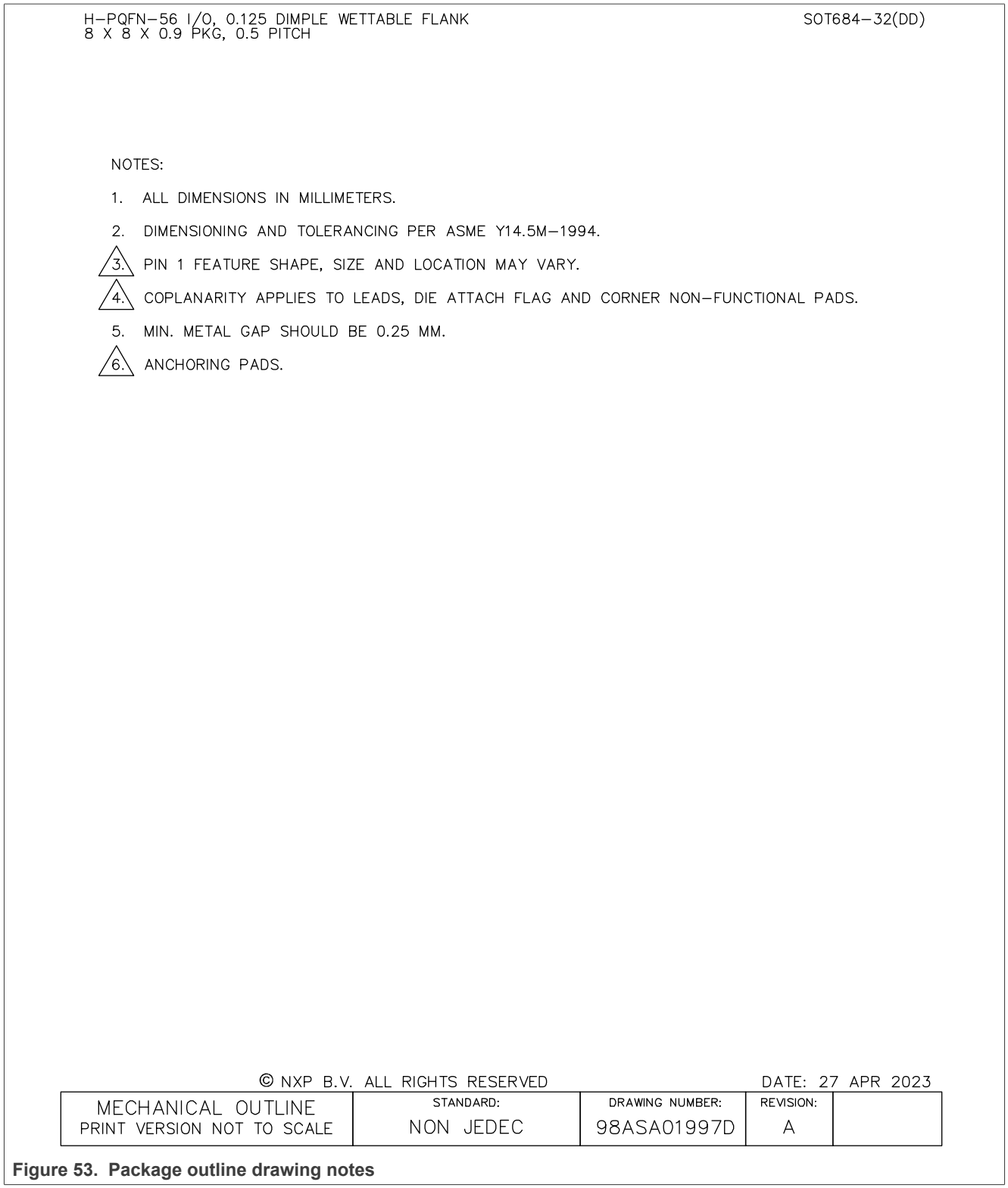

Figure 53. Package outline drawing notes

20 Revision history

Table 237. Revision history

Document ID	Release date	Description
PF09 v.1.3	16 December 2025	• Added new part number "MPF0900AVSA0ES" in Table 2 • Updated V_{AON_TON} Max value from "1" to "1.7" in Table 109
PF09 v.1.2	11 November 2025	• Updated "Automotive qualified by AEC-Q100 rev H up to Grade 1" to "Automotive qualified by AEC-Q100 rev J up to Grade 1" in Section 2 and Section 10.1 • Removed "Max value = 400" from I_{HYS_GPIO1}, I_{HYS_GPIO2}, I_{HYS_GPIO3}, I_{HYS_GPIO4}, I_{HYS_FS0B}, I_{HYS_XFAILB} in Table 63 • Updated 0x0D DEFAULT value from "0001_1111" to "0011_1111" in Table 229
PF09 v.1.1	15 October 2025	• Updated "OTP_MAX_FS[3:0]" parameter to "OTP_MAX_FS_CNT[3:0]" in Section 11.2.11 • Updated description in FLTCNT_FAIL from "The Fault counter reaches the maximum number of failures allowed. (FAULT_CNT[3:0] = MAX_FLT_CNT[3:0]" to "The Fault counter reaches the maximum number of failures allowed. (FAULT_CNT[3:0] = FAULT_MAX_CNT[3:0]" in Table 57 • Removed VAON ILIM INT, VAON ILIM MSK, and VAON ILIM SNS BIT3 register in Table 60 • Updated Figure 20
PF09 v.1.0	30 September 2025	• Changed Figure 23 title from "Dual PMIC interaction with fault on master device" to "Dual PMIC interaction with fault on controller device" • Updated Table 2 • Updated Table 26 – Changed V_{IN_OV} Min value from "5.6" to "5.6.5" and Max value from "6" to "5.9.5" – Changed $V_{IN\_OV\_HYS}$ Min value from "70" to "50" – Added $V_{IN\_OV\_HYS}$ Typ value as "100" • Updated Table 203 – Changed ERRMON deglitch time Min value from "4" to "9" and Max value from "8" to "11" – Added ERRMON deglitch time Typ value as "10" • Updated how to request LBIST on demand steps in Section 14.10.2 • Updated V_{DDIO} description in Table 236
PF09 v.0.7	21 August 2025	• Preliminary data sheet • Global: corrected capitalization, hyphenation, and format (adding and removing subscript format) • Updated Table 2 • Table 3: updated watchdog manager characteristic for SIL2 to static watchdog • Figure 16: adjusted font for legibility • Figure 17: adjusted font for legibility • Added table title to Table 59 • Added table title to Table 90 • Section 12.8.9.2: corrected bit field descriptions for VLDO_RUN and VLDO_STBY • Table 85: corrected bit field descriptions for VLDO_RUN and VLDO_STBY • Section 12.8.10.2: changed LDO2EN to LDO1EN • Section 13.2.2: updated DVS information • Table 126: corrected the heading of the second column • Updated Section 13.2.4 • Table 145: added R_{DSON} information • Updated Section 13.2.5 • Section 13.2.5.3: corrected VLDOx_RUN bit field description

Table 237. Revision history...*continued*

Document ID	Release date	Description
		• Added Figure 25 • Table 154: added R_{DSON} information • Added Figure 29 • Updated Table 180 • Updated Section 13.5.1 • Updated Section 14.7.2 • Updated Section 14.10.2 • Updated Table 229 • Updated Table 232
PF09 v.0.6	24 June 2025	Initial release of preliminary data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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