PF5103; PF5113; PF5123

Power management integrated circuit (PMIC) for high performance applications

Rev. 3.0 — 16 February 2026 **Product data sheet**

1 Overview

The PF51x3 integrates multiple high performance buck regulators and LDO regulators. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I^2C after startup, offering flexibility for different system states.

Functional safety features, developed according to ISO 26262 specifications, enable the device to reach safety levels up to ASIL B.

This data sheet presents details of the PF5103 device. PF5103 is the main device of the PF51x3 family with full functionality. The differences between PF5103 and the PF5113/PF5123 devices are summarized in Section 12.1 and Section 12.4.

2 Features and benefits

The PF5103 is a power management integrated circuit (PMIC) designed to be the primary core power supply for high-end ADAS application processors.

- Buck regulators
  - SW1, SW2, SW3: 0.5 V to 3.3 V; 3500 mA; 1.5 % accuracy
  - Dynamic voltage scaling
  - Configurable as multi-phase regulator
  - Programmable current limit (4 A, 5 A, 6 A)
- LDO regulators with load switch option
  - LDO1: 0.75 V to 3.3 V; 200 mA; 1.5 % accuracy
  - LDO2: 0.75 V to 3.3 V; 500 mA; 1.5 % accuracy
- PGOOD output
  - PGOOD output also used as processor reset signal
  - Independent safety assertion path for certain faults; to ensure safe state
- FCCU input
  - Monitoring MCU fault signal (by PWM detection of level detection)
- Advanced clock management
  - Clock synchronization through configurable input sync pin
  - Manual clock frequency tuning
- System features
  - Advanced state machine for seamless processor interface
  - I^2C communication interface (3.4 MHz)
  - Programmable soft start sequence and power-down sequence
  - Programmable regulator configuration
  - Advanced thermal monitoring and protection
- OTP (One-time programmable) memory for device configuration
- Functional Safety features to fit up to ASIL B safety level
  - Independent voltage monitoring with programmable fault protection; 1 % accuracy
  - Independent clock monitoring
  - Watchdog monitoring – simple
  - OV monitoring of internal regulators
  - I^2C CRC and secure write protection mechanism
  - Analog built-in self-test (ABIST)

3 Applications

- Automotive – Radar, infotainment, domain controllers
- High-end consumer and industrial

4 Simplified application diagram

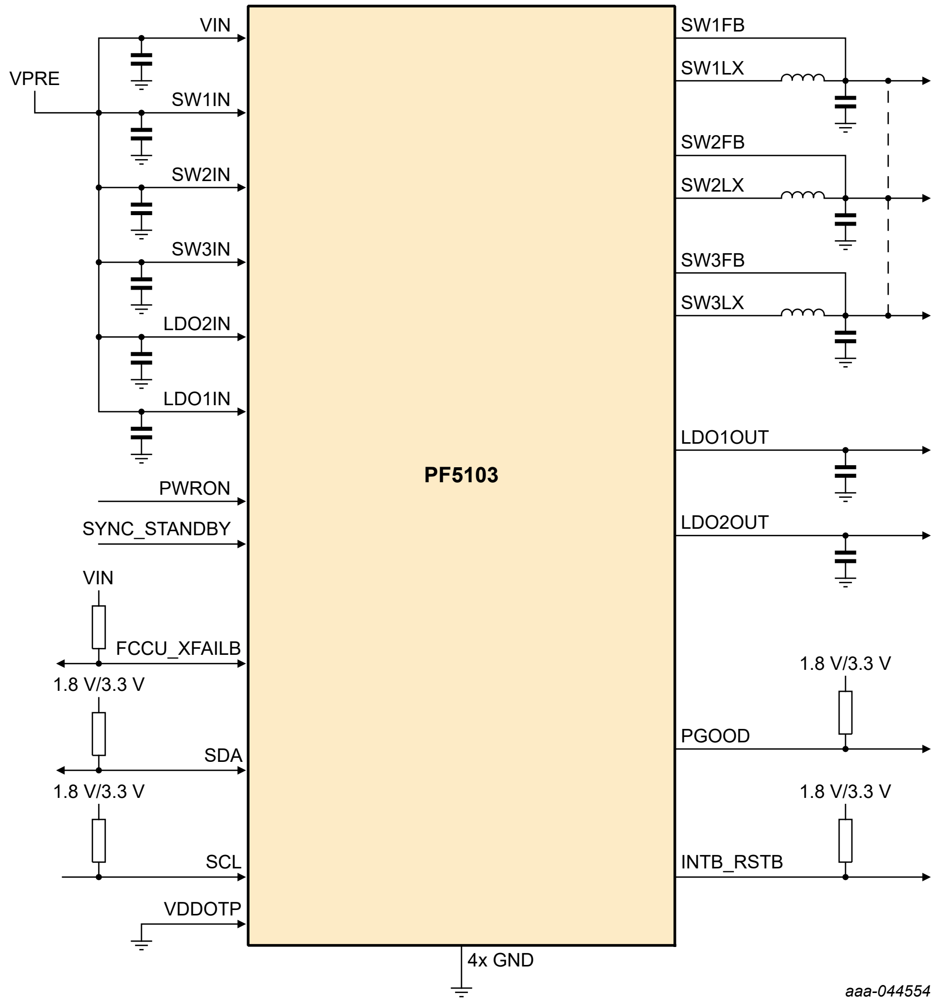


Figure 1. Simplified application diagram

Note:

- *PF5113 and PF5013 have the same hardware implementation.*
- *For PF5123, we can unpopulate the capacitors for LDO1 and LDO2 and keep them floating.*

5 Ordering information

Table 1. Ordering information

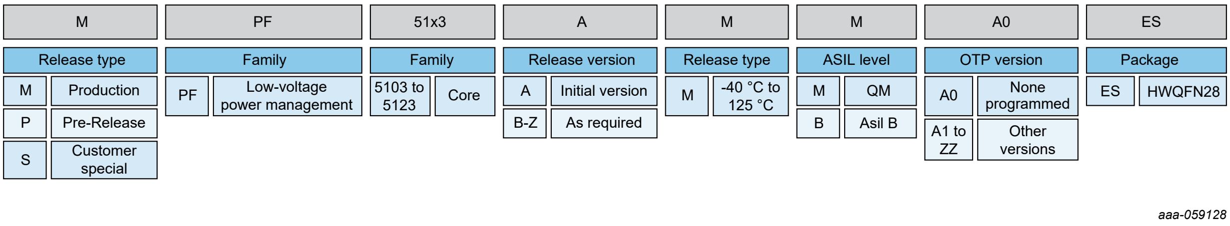
Part number[1]	Description	Main properties						
		SW1 voltage	SW2 voltage	SW3 voltage	LDO1 voltage	LDO2 voltage	Safety grade	Package
MPF5103AMMA0ES[2]	Superset covering PF5103 QM device	Configurable	Configurable	Configurable	Configurable	Configurable	QM	HWQFN28
MPF5103AMBA0ES[3]	Superset covering PF5103 ASIL B device	Configurable	Configurable	Configurable	Configurable	Configurable	ASIL B	
MPF5113AMMA0ES[2]	Superset covering PF5113 QM device	Configurable	Configurable	Configurable	Configurable	Configurable	QM	
MPF5113AMBA0ES[3]	Superset covering PF5113 ASIL B device	Configurable	Configurable	Configurable	Configurable	Configurable	ASIL B	
MPF5123AMMA0ES[2]	Superset covering PF5123 QM device	Configurable	Configurable	Configurable	Configurable	Configurable	QM	
MPF5123AMBA0ES[3]	Superset covering PF5123 ASIL B device	Configurable	Configurable	Configurable	Configurable	Configurable	ASIL B	
MPF5103AMMA6ES	Supplying Ethernet PHY (Marvell AQR113C)	0.7 V	1 V	2 V	OFF	1.8 V	QM	
MPF5103AMMA9ES	Supplying NXP i.MXRT117x	1.125 V	1.8 V	3.3 V	3.3 V	2.8 V	QM	
MPF5103AMMACES	Supplying imaging radar 8T8R (IFX CTRX8191FS)	0.91875 V	0.91875 V	1.3 V	1.8 V	1.1 V	QM	
MPF5103AMBAHES	Supplying radar sensor (NXP SAF85xx)	0.9 V	1.8 V	1.5 V	OFF	OFF	ASIL B	

[1] To order parts in tape and reel, add the R2 suffix to the part number.

[2] Safety grade: QM, non-programmed device. Custom OTP is MPF51x3AMMxxES. xx is a unique letter and number for each OTP configuration.

[3] Safety grade: ASIL B, non-programmed device. Custom OTP is MPF51x3AMBxxES. xx is a unique letter and number for each OTP configuration.

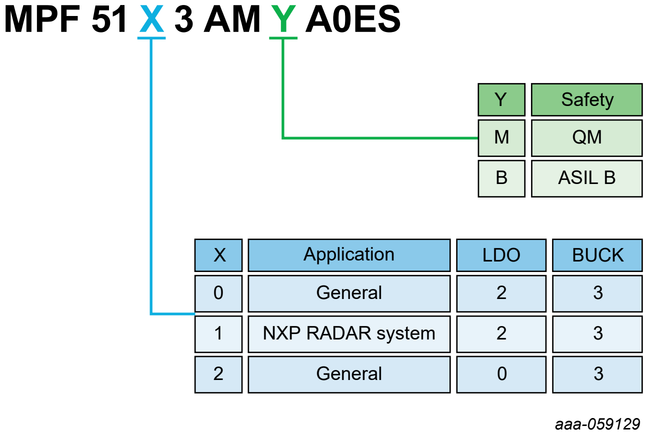
5.1 PF51x3 numbering scheme



M	PF	51x3	A	M	M	A0	ES
Release type	Family	Family	Release version	Release type	ASIL level	OTP version	Package
M Production	PF Low-voltage power management	5103 to 5123 Core	A Initial version	M -40 °C to 125 °C	M QM	A0 None programmed	ES HWQFN28
P Pre-Release			B-Z As required		B Asil B	A1 to ZZ Other versions	
S Customer special							

Figure 2. PF51x3 numbering scheme

5.2 PF51x3 part number definition



MPF 51 X 3 AM Y A0ES

Y	Safety
M	QM
B	ASIL B

X	Application	LDO	BUCK
0	General	2	3
1	NXP RADAR system	2	3
2	General	0	3

Figure 3. PF51x3 product numbering scheme

6 Internal block diagram

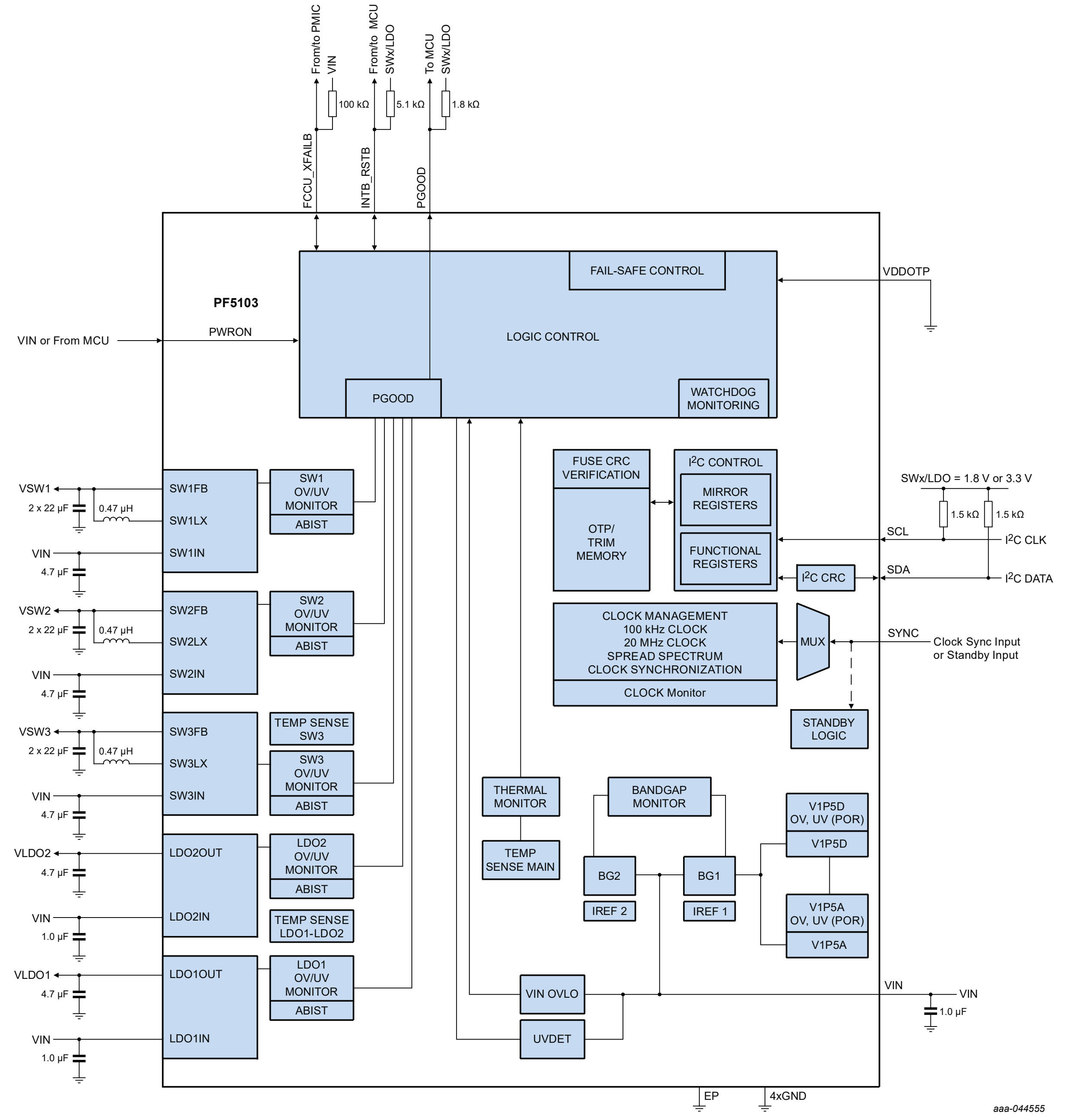


Figure 4. Internal block diagram

7 Pinning information

7.1 Pinout

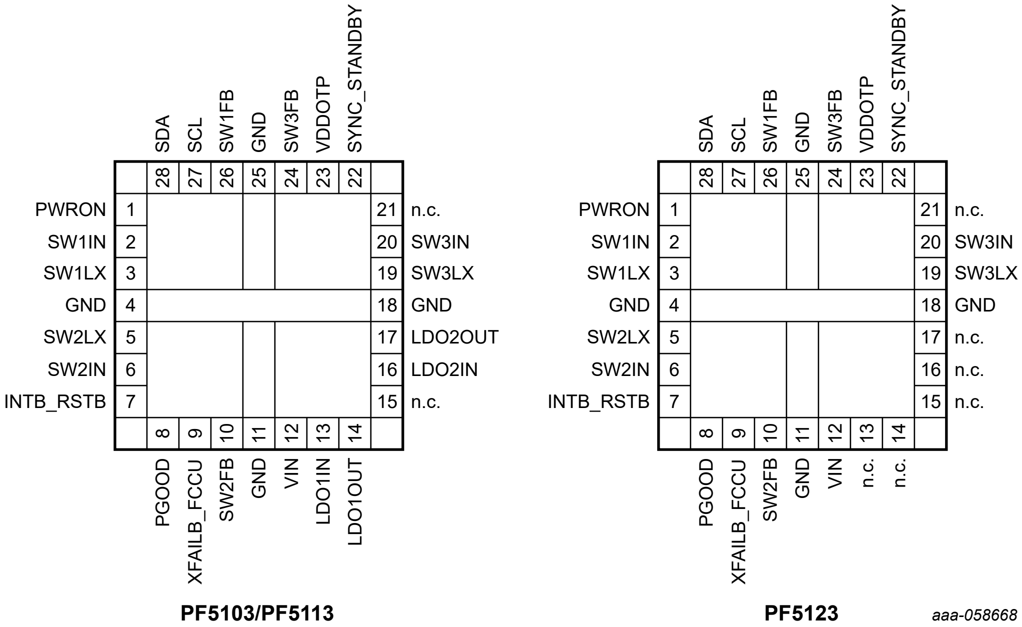


Figure 5. Pin configuration for 28-pin HWQFN (Top view)

7.2 Pin description

Table 2. Pin descriptions

pin number	Pin name	Pin description	Min	Max	Units
1	PWRON	PWRON input	-0.3	5.5	V
2	SW1IN	SW1 input supply	-0.3	5.5	V
3	SW1LX	SW1 switching node	-0.7	5.5	V
4	GND	Ground	-0.3	0.3	V
5	SW2LX	SW2 switching node	-0.7	5.5	V
6	SW2IN	SW2 input supply	-0.3	5.5	V
7	INTB_RSTB	Interrupt output or External reset input	-0.3	5.5	V
8	PGOOD	PGOOD output	-0.3	5.5	V
9	XFAILB_FCCU	FCCU input or XFAILB bidirectional signal	-0.3	5.5	V
10	SW2FB	SW2 feedback input	-0.3	5.5	V
11	GND	Ground	-0.3	0.3	V

Table 2. Pin descriptions*...continued*

pin number	Pin name	Pin description	Min	Max	Units
12	VIN	Input supply	-0.3	5.5	V
13	LDO1IN[1]	LDO1 input	-0.3	5.5	V
14	LDO1OUT [1]	LDO1 output	-0.3	5.5	V
15	NC	Not connected	—	—	—
16	LDO2IN[1]	LDO2 input	-0.3	5.5	V
17	LDO2OUT[1]	LDO2 output	-0.3	5.5	V
18	GND	Ground	-0.3	0.3	V
19	SW3LX	SW3 switching node	-0.7	5.5	V
20	SW3IN	SW3 input supply	-0.3	5.5	V
21	NC	Not connected	—	—	—
22	SYNC_STANDBY	Clock synchronization input or Standby Input	-0.3	5.5	V
23	VDDOTP	Debug mode/ OTP programming input supply	-0.3	10	V
24	SW3FB	SW3 feedback input	-0.3	5.5	V
25	GND	Ground	-0.3	0.3	V
26	SW1FB	SW1 feedback input	-0.3	5.5	V
27	SCL	I^2C SCL signal	-0.3	5.5	V
28	SDA	I^2C SDA signal	-0.3	5.5	V

[1] NC for PF5123.

8 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Main input supply voltage [1]	−0.3	—	6.0	V
SWxIN, LDOxIN	Regulator input supply voltage [1]	−0.3	—	6.0	V
SWxLX	Regulator switching voltage (DC) [1]	−0.7	—	6.0	V
SWxFB, LDOxOUT	Regulator feedback/output voltage [1]	−0.3	—	6.0	V
PGOOD XFAILB_FCCU INTB_RSTB SYNC_STANDBY SCL/SDA PWRON	I/O voltages [1]	−0.3	—	6.0	V
VDDOTP	OTP programming input supply voltage	−0.3	—	10	V

[1] Pin reliability may be affected if system voltages are above the maximum operating range of 6.0 V for extended period of time. To minimize system reliability impact, system must not operate above 6.0 V for more than 1800 sec over the lifetime of the device.

9 ESD ratings

Table 4. ESD ratings

All ESD specifications are compliant with AEC-Q100 specification.

Symbol	Parameter	Min	Typ	Max	Unit
V_{ESD}	Human body model [1]	—	—	2000	V
V_{ESD}	Charge device model [1]	—	—	500	V
$I_{LATCHUP}$	Latch-up current	—	—	100	mA

[1] ESD testing is performed in accordance with the human body model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the charge device model (CDM), robotic (CZAP = 4.0 pF).

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient operating temperature	−40	—	125	°C
T_J	Junction temperature	−40	—	150	°C
T_{ST}	Storage temperature range	−40	—	150	°C
T_{PPRT}	Peak package reflow temperature	—	—	260	°C

Table 6. QFN28 thermal resistance and package dissipation ratings

Symbol	Parameter	Typ	Unit
$R_{\theta JA}$	Junction to Ambient Thermal Resistance JESD51-7, 2s2p [1] [2]	39.4	°C/W
$R_{\theta JA}$	Junction to Ambient Thermal Resistance Customized board, 2s6p [1] [3]	20.8	°C/W
Ψ_{JT}	Junction to Top of Package Thermal JESD51-7, 2s2p [1] [2]	1.3	°C/W
$R_{\theta JC\_TOP}$	Junction to Case (Top) Thermal Resistance [4]	22	°C/W
$R_{\theta JC\_BOT}$	Junction to Case (Bottom) Thermal Resistance [5]	10.2	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

[2] Thermal test board meets JEDEC specification for this package (JESD51-7).

[3] Simulation of PF5103 on an eight-layer (2s6p) application representative PCB. Actual performance on a given application should be simulated by the customer to optimize thermal design of the system. IcePAK, Flotherm and 3D PF5103 simulation models are available on NXP.com

[4] Junction-to-Case (Top) thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.

[5] Junction-to-Case (Bottom) thermal resistance determined using an isothermal cold plate. Case temperature refers to the exposed pad surface temperature at the package bottom side dead center.

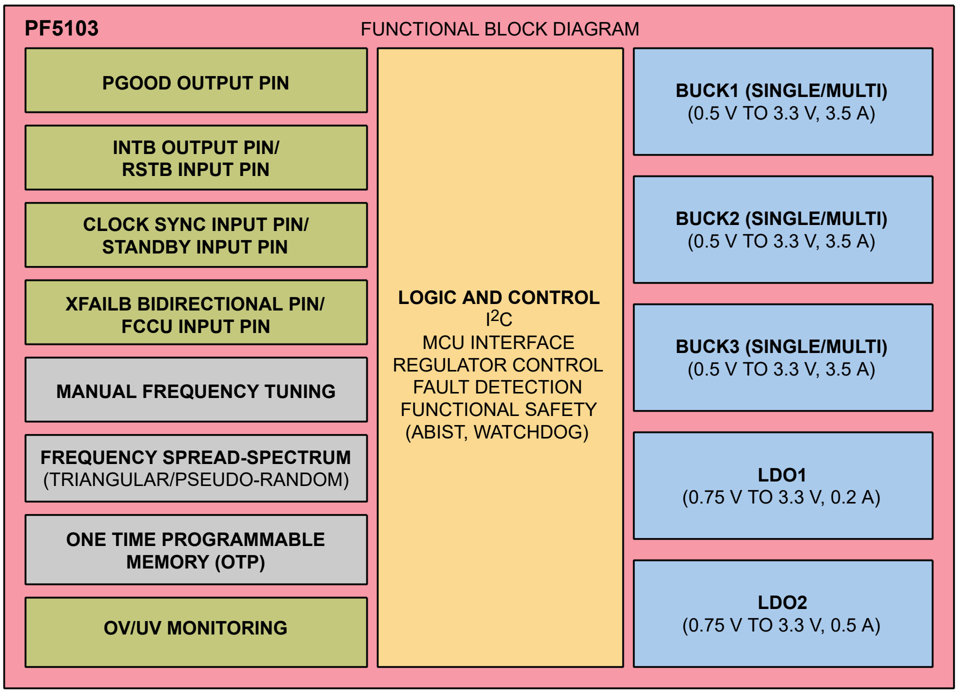
11 Operating conditions

Table 7. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Main input supply voltage VIN, LDOxIN, SWxIN	UVDET	—	5.5	V
VIO	IO input supply voltage PWRON, PGOOD, INTB_RSTB, SYNC_ STANDBY, XFAILB_FCCU	0	—	VIN	V
VI2C	SDA, SCL	0	—	3.65	V
VDDOTP	VDDOTP voltage	0	—	10	V

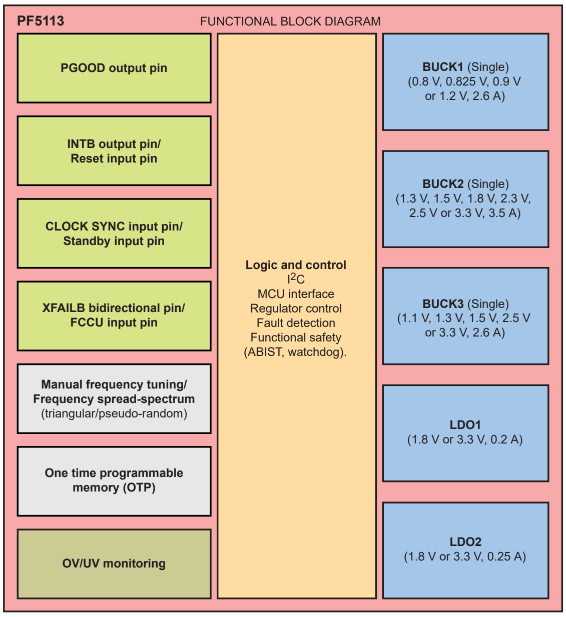
12 General description

12.1 Functional block diagram



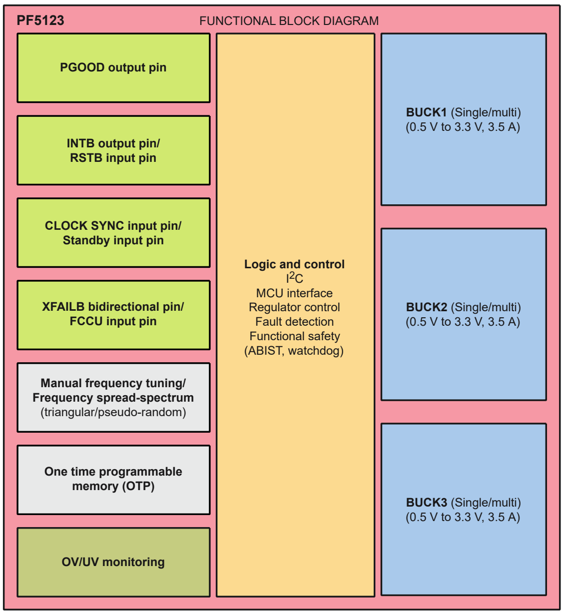
aaa-044557

Figure 6. PF5103 functional block diagram



aaa-049409

Figure 7. PF5113 functional block diagram



aaa-054098

Figure 8. PF5123 functional block diagram

12.2 Power tree summary

The following table provides a summary of the voltage regulators in the PF5103:

Table 8. Voltage supply summary

Regulator	Type	Input supply	Regulated output range (V)	VOUT programmable step (mV)	I_OUT (mA)
SW1	Buck	SW1IN	0.5 V - 3.3 V	6.25 (0.5 V to 1.35 V), 12.5 (1.8 V to 2.5 V), 25 (2.8 V to 3.3 V)	3500
SW2	Buck	SW2IN	0.5 V - 3.3 V	6.25 (0.5 V to 1.35 V), 12.5 (1.8 V to 2.5 V), 25 (2.8 V to 3.3 V)	3500
SW3	Buck	SW3IN	0.5 V - 3.3 V	6.25 (0.5 V to 1.35 V), 12.5 (1.8 V to 2.5 V), 25 (2.8 V to 3.3 V)	3500
LDO1	LDO	LDO1IN	0.75 V to 3.3 V	50 (0.75 V to 1.5 V), 100 (1.8 V to 3.3 V)	200
LDO2	LDO	LDO2IN	0.75 V to 3.3 V	50 (0.75 V to 1.5 V), 100 (1.8 V to 3.3 V)	500

Note: *the programmable voltages for PF5113 and PF5123 are specified in Section 12.4.*

12.3 Safety feature differences

Table 9. Safety feature differences

Description	PF5103 QM	PF5103 ASIL B	Bits not available on PF5103 QM
Self-test routine: • The high speed oscillator circuit is operating within a maximum of 20 % tolerance compared to the low power clock • A CRC is performed on the OTP mirror registers during the self-test routine to ensure the integrity of the registers before powering up • The output of both the voltage generation bandgap and the monitoring bandgap are not more than 45 mV apart from each other • ABIST test on all voltage monitors	Not available	Available	• AB_x_OV • AB_x_UV • AB_RUN • STEST_NOK
Functional register CRC	Available	Available	
Fail-safe state: to lock down the system in case of critical failures cycling the PMIC ON/OFF.	Not available	Available	• FS_BYPASS_CNT[3:0] • OTP_FS_BYPASS • OTP_FS_BYPASS_CNT
Secure I^2C write: I^2C write procedure to modify registers dedicated to safety features (I^2C CRC is still available).	Not available	Available	• I2C_SECURE_EN (default 0) • OTP_I2C_SECURE _EN (default 0) • RANDOM_GEN[7:0] • RANDOM_CHK[7:0]
VDIG, VANA OV	Available	Available	
Clock Stuck Monitor	Available	Available	
FCCU input	Not available	Available	
Bandgap monitor / VIN monitor (always ON)	BG monitor only	BG or VIN monitor (VIN = 3.3 V)	For a QM device, only this configuration is possible: • OTP_BGMON_BYPASS = 1 • OTP_BGMON_SEL = 0
LDOxOUT pin open fault detection	Available	Available	
VIN pin open fault detection	Available	Available	
Watchdog monitoring	Simple	Simple	

12.4 Device family overview

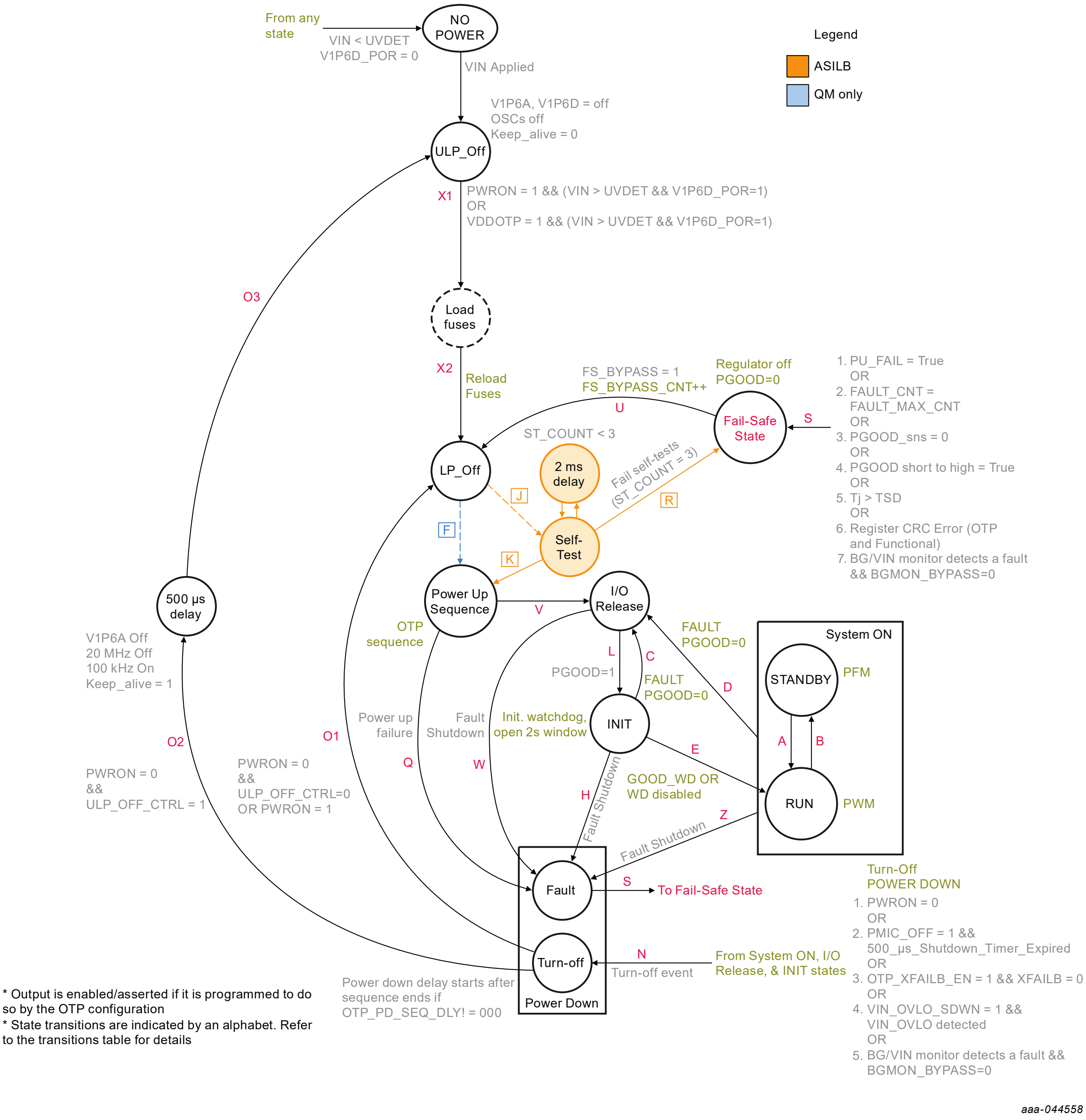
Table 10 summarizes the characteristics of each member of the device family.

Table 10. PF51XX device family

Feature	PF5103	PF5113	PF5123
BUCK1	0.5 V to 3.3 V Current capability: 3.5 A (Single/Multi phase)	0.8 V, 0.825 V, 0.9 V,1.2 V Current capability: 2.6 A (Single phase)	0.5 V to 3.3 V Current capability: 3.5 A (Single/Multi phase)
BUCK2	0.5 V to 3.3 V Current capability: 3.5 A (Single/Multi phase)	1.3 V, 1.5 V, 1.8 V, 2.3 V, 2.5 V, 3.3 V Current capability: 3.5 A (Single phase)	0.5 V to 3.3 V, Current capability: 3.5 A (Single/Multi phase)
BUCK3	0.5 V to 3.3 V Current capability: 3.5 A (Single/Multi phase)	1.1 V, 1.3 V, 1.5 V, 2.5 V, 3.3 V Current capability: 2.6 A (Single phase)	0.5 V to 3.3 V Current capability 3.5 A (Single/Multi phase)
LDO1	0.75 V to 3.3 V, 0.2 A	1.8 V or 3.3 V, 0.2 A	No
LDO2	0.75 V to 3.3 V, 0.5 A	1.8 V or 3.3 V, 0.25 A	No
PWRON	Yes	Yes	Yes
SYNC_STANDBY	Yes	Yes	Yes
XFAILB_FCCU	Yes	Yes	Yes
I2C	Yes	Yes	Yes
PGOOD	Yes	Yes	Yes
INTB_RSTB	Yes	Yes	Yes
Watchdog	Simple	Simple	Simple
SAFETY	QM, ASILB	QM, ASILB	QM, ASILB

13 State machine

The PF51x3 features a state of the art state machine for seamless processor interface. The state machine handles the IC startup, provides fault monitoring and reporting, and protects the IC and the system during fault conditions.



* Output is enabled/asserted if it is programmed to do so by the OTP configuration
* State transitions are indicated by an alphabet. Refer to the transitions table for details

Figure 9. State diagram

Table 11 lists the conditions for the different state machine transitions.

Table 11. State machine transition definition

Symbol	Description	Conditions
Transition A	Standby to Run[1]	1. (STANDBY = 0 && STANDBYINV bit = 0)
		2. (STANDBY = 1 && STANDBYINV bit = 1)
Transition B	Run to Standby	1. (STANDBY = 1 && STANDBYINV bit = 0)
		2. (STANDBY = 0 && STANDBYINV bit = 1)
Transition C	INIT to I/O Release	1. PMIC faults programmed to assert PGOOD
		2. PGOOD_RLS =0; PGOOD asserted low when this bit is set to 0 through I2C (Only in companion mode)
Transition D	System ON to I/O Release	PMIC faults programmed to assert PGOOD low
Transition E	INIT to Run	1. WD enabled && INIT window closed with first good WD refresh (correct WD answer) within INIT time
		2. WD disabled
Transition X (X1 and X2)	ULP_Off to LP_Off	Power-up transition (power-up event present) 1. PWRON = 1 (High)
		Power-up transition (power-up event present) (Debug mode) 2. VDDOTP = 1
Transition F	LP_Off to Power-up sequence (PF5103 QM only	Power-up state (power-up event present) 1. PWRON = 1 && Tj < TSD && VIN > UVDET && ((VIN < VIN_OVLO && VIN_OVLO_EN = 1 && VIN_OVLO_SDWN = 1) OR VIN_OVLO_SDWN = 0 OR VIN_OVLO_EN = 0) && TRIM_NOK = 0 && OTP_NOK = 0 && OTP_XFAILB_EN = 0
		Power-up state (power-up event present) 2. PWRON =1 && Tj < TSD && VIN > UVDET && ((VIN < VIN_OVLO && VIN_OVLO_EN = 1 && VIN_OVLO_SDWN = 1) OR VIN_OVLO_SDWN = 0 OR VIN_OVLO_EN = 0) && TRIM_NOK = 0 && OTP_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = 1
Transition J	LP_Off to self-test (PF5103 ASIL B)	Transitory On state 1. PWRON = 1 && Tj < TSD && VIN > UVDET && ((VIN < VIN_OVLO && VIN_OVLO_EN = 1 && VIN_OVLO_SDWN = 1) OR VIN_OVLO_SDWN = 0 OR VIN_OVLO_EN = 0) && TRIM_NOK = 0 && OTP_NOK = 0
Transition K	Self-test to Power-up sequence (PF5103 ASIL B)	1. Pass all Self-tests except ABIST && OTP_XFAILB_EN = 0
		2. Pass all Self-tests except ABIST && (OTP_XFAILB_EN = 1 && XFAILB = 1)
		3. VDDOTP = 1
Transition V	power up sequence to I/O Release (PGOOD_sns timer becomes active after PGOOD release)	Completion of the Power-up sequence according to OTP
Transition L	I/O Release to INIT	PGOOD_sns = 1 (check the PGOOD feedback for high level after releasing internally)
Transition Z	System On to Power Down (Fault)	1. FAULT_CNT = FAULT_MAX_CNT
		2. Thermal shutdown Tj > TSD
		3. Register map CRC error (OTP and functional bits)
Transition H	INIT to Power Down (Fault)	1. FAULT_CNT = FAULT_MAX_CNT
		2. Thermal shutdown Tj > TSD
		3. Register map CRC error (OTP and functional bits)
Transition W	I/O Release to Power Down (Fault)	1. FAULT_CNT = FAULT_MAX_CNT

Table 11. State machine transition definition*...continued*

Symbol	Description	Conditions
		2. PGOOD_sns = 0 (low) until 100 ms timer expires (after internally releasing PGOOD)
		3. PGOOD short to high is detected (true) (before internally releasing PGOOD)
		4. Thermal shutdown Tj > TSD
		5. Register map CRC error (OTP and functional bits)
Transition Q	Power up sequence to Power down (Fault)	Power-up failure 1. Regx failure (OV/UV) during Power-up sequence
		2. PGOOD_sns = 1 when PGOOD is internally asserted low (PGOOD fails short to high test before PGOOD gets internally released; check the feedback if it's low)
		3. PGOOD_sns = 0 for greater than 100 ms when PGOOD is internally released high (PGOOD fails short to GND test after releasing)
		4. Register map CRC error (OTP and functional bits)
		5. BG/VIN monitor detects a fault && OTP_BGMON_BYPASS = 0
Transition N	System ON, I/O Release, or INIT states to Power down (turn off) (starts power-down sequence)	1. PWRON = 0
		2. PMIC_OFF = 1 && 500us_Shutdown_Timer_Expired
		3. OTP_XFAILB_EN = 1 && XFAILB = 0 (pin pulled low externally)
		4. VIN_OVLO_EN = 1 && VIN_OVLO_SDWN = 1 && VIN_OVLO detected for longer than VIN_OVLO_DBNC time
		5. BG/VIN monitor detects a fault && OTP_BGMON_BYPASS = 0
Transition O1	Power down (turn off) to LP_Off	Requested turn off event moves directly to LP_Off 1. PWRON = 0 && ULP_OFF_CTRL = 0 && Power-down sequences finished
		2. PWRON=1 (ULP_OFF_CTRL= don’t care) && Power down sequences finished
Transition O2/O3	Power down (turn off) to ULP_Off	Requested turn off event moves directly to ULP_Off 1. PWRON = 0 && ULP_OFF_CTRL = 1 && Power Down sequence finished (keep_alive = 1 for 500 µs - delay b/w O2 and O3)
Transition R	Self-test to Fail-safe state	ST_COUNT = 3 (Self-test fails 3 times) && VDDOTP = 0
Transition S	Power down (Fault) to Fail-safe state	Turn off event due to a Fault condition will move to Fail-Safe state; power-down sequencer is finished
Transition U	Fail-safe state to LP_Off	1. OTP_FS_BYPASS = 1 && OTP_FS_BYPASS_CNT = 0 && FS_BYPASS_CNT <1 5
		2. OTP_FS_BYPASS = 1 && OTP_FS_BYPASS_CNT = 1

[1] Power Sequencing has fully completed.

13.1 State descriptions

13.1.1 ULP_Off state

The ULP_Off state is an ultra-low power off mode with very low quiescent current (Iq < 2 µA). When VIN is applied, the state machine moves to this state and waits for a power on event. In this state, the internal bias circuits are kept off to maintain the low Iq requirement and only the PWRON detection circuits are enabled. The VDDOTP pin is also monitored for initiating a startup event. In this case, the device will enter the LP_Off state in debug mode.

During power down, the ULP_OFF_CTRL bit determines the transition to the ULP_Off state. In the power down caused by PWRON going low, if the ULP_OFF_CTRL = 0, the state machine moves to LP_Off directly.

If ULP_OFF_CTRL = 1, the state machine transitions to the ULP_Off state where the internal regulators are turned off to reduce the supply current consumption.

The selection of the ULP_OFF_CTRL bit is based on whether prioritizing low quiescent current (transition to ULP_Off state) or a quick power up without losing the OTP mirror settings (transition to the LP_Off state).

13.1.2 OTP/TRIM load

During a power on event (PWRON=1 or VDDOTP=1) from ULP_Off state, the internal regulators are turned on, then the fuses (for trim and OTP) are loaded into the mirror registers and into the functional I^2C registers.

The fuse circuits have a CRC error check routine which reports and protects against register loading errors on the mirror registers. If a register loading error is detected, the corresponding TRIM_NOK or OTP_NOK flag will be set and stop power sequencing.

13.1.3 LP_Off state

The LP_Off state is a low power off mode with current consumption higher than the ULP_Off mode. In this state, all the internal circuits are ON and device transitions to the Power-up sequence state depending on the PWRON pin status.

During this state, if PWRON goes high, the device moves to start the Power-up sequence as defined in the OTP settings. If instead PWRON is low and VDDOTP goes high, the device stays in the LP_Off state but enters debug mode. In debug mode, the device gives the user access to modify the OTP mirror registers, and also do the OTP programming by burning the fuses.

When ULP_OFF_CTRL=0, the device enters the LP_Off state from I/O Release, INIT, or System ON states.

13.1.4 Self-test routine (PF5103 ASIL B)

When the device transitions from the LP_Off state, it moves into the self-test routine and performs tests to verify the integrity of the internal circuits.

During the self-test routine the following blocks are verified:

- The high speed clock circuit is operating within a maximum of 20 % tolerance
- The output of both the voltage generation bandgap and the monitoring bandgap are not more than 45 mV apart from each other
- A CRC is performed on the OTP mirror registers to ensure the integrity of the registers before powering up
- ABIST test on all voltage monitors
  To allow for varying settling times for the internal bandgap and clocks, the self-test block is executed up to three times (with 2.0 ms between each test). If a failure is encountered, the state machine proceeds to the fail-safe transition.
  A failure in the ABIST test is not interpreted as a self-test failure, and it only sets the corresponding ABIST flag for system information. The processor is responsible for reading the information and deciding whether it can continue with a safe operation. See Section 18.1 for the functional safety strategy for PF5103.

Upon a successful self-test, the state machine proceeds to the Power-up sequence state.

13.1.5 Power-up sequence

During the Power-up sequence, the PF5103 regulators are turned on in a predefined order as programmed by the default OTP sequence.

If any of the regulators fail during the Power-up sequence, the sequencer at the end waits for up to 2 ms to allow all output voltages to settle. If a fault is not cleared within the 2 ms, the device detects a power up failure, aborts the sequence and prevents PGOOD release (if PGOOD is assigned to that particular faulty regulator, x_PG_EN=1). After a power-up failure, the state machine will proceed to the Fail-safe state and increment the fault counter.

If the power up fault is cleared before the 2 ms timer expires, the state machine will proceed with the power up sequence, exit the Power-up sequence state and enter the I/O Release state.

If the power up of all the regulators is successful, then the state machine will release PGOOD towards the end of the sequence (if PGOOD is not assigned a slot). Before releasing PGOOD, the device will check for a PGOOD short to high. If a short fault is detected, then the PGOOD release will be prevented, the PG_SHORT_I interrupt bit will be set, and fault shutdown will be initiated.

The PGOOD can also be programmed as part of the power up sequence. The PGOOD may be released in the middle of the power up sequence by assigning a slot in OTP. In this case, the PGOOD release will be based on the regulation status of the previous regulators turned on in the sequence already. The remaining supplies in the sequence will continue to power up after PGOOD gets released and PGOOD will continue to monitor the remaining regulators for any startup failure. See Section 14.4.2 for details.

When PGOOD is assigned to a slot or released in the end of the sequence, a 100 millisecond (100 ms) timer becomes active as soon as the PGOOD gets internally released. This timer is to check the PGOOD sense feedback for a short to ground externally. If a short to GND is detected, device fault shutdown will be initiated. The 100 ms timer is disabled in debug mode.

13.1.6 I/O Release state

If the Power-up state is successfully completed, the state machine transitions to the I/O Release state.

If the PGOOD feedback sense is still low until the 100 ms timer expires, it’s considered as PGOOD sense fail (PGOOD_sns = 0, Fault Shutdown) and the state machine initiates the fault shutdown.

PGOOD_sns = 1 is a condition to transition to the INIT state.

13.1.7 INIT state

If the Power-up state is successfully completed and PGOOD is released, the state machine transitions to the INIT state. In this state, the processor is expected to boot up and set up specific registers of the PMIC.

The INIT window must be closed within 2 seconds with a good watchdog (WD) refresh. Expiration of this timer (absence of good WD refresh) is considered as a WD event and the state machine will transition to the I/O Release state, assert PGOOD, and increment the fault counter.

Upon state transition, the state machine exits into the System ON states upon successful verification of following conditions: Good watchdog refresh, or the watchdog function is disabled.

13.1.8 System ON state

In the system ON state, the processor is powered and out of reset and the system is fully operational. The system ON is a virtual state composed by two modes of operations: Run state and Standby state. The transition from the Run state to the Standby state or from the Standby state to the Run state is not dependent on completion of the power sequencer.

Run state

In this state, regulator specific registers to control its output voltage, operation mode and/or enable/disable state can be modified.

By default, the VSWx_RUN[7:0] registers are loaded with the data stored in the OTP_VSWx[7:0] registers respectively.

Upon power up, if the switching regulator is part of the Power-up sequence, the mode bits of each regulator will be loaded as needed by the system.

- When OTP_SYNC_EN = 1, default SWx_RUN_MODE at power up will always be PWM (0b01)
- When OTP_FSS_EN = 1, default SWx_RUN_MODE at power up will always be PWM (0b01)
- If none of the Conditions above are met, the default SWx_RUN_MODE bit at power up will be set by the OTP_SW_MODE bits.
  When OTP_SW_MODE = 0, the default value of the SWx_RUN_MODE bits are set to 0b10 (PFM).
  The PFM configuration is applicable for SWx switching frequency set in the range of 2 MHz to 3 MHz.
  When OTP_SW_MODE = 1, the default value of the SWx_RUN_MODE bits are set to 0b01 (PWM).
  If the switching regulator is not part of the Power-up sequence, the SWx_RUN_MODE[1:0] bits are loaded with 0b00 (Off mode).
  In a typical system, each time the processor boots up (PMIC transitions from Off mode to Run state), all output voltage configurations are reset to the default OTP configuration, and the processor should configure the PMIC to its desired usage in the application.

Standby state

The Standby state or the low power ON state is entered when the Standby pin is pulled high or Low as defined by the STANBYINV polarity bit. When in Standby state, the SWx output voltage, operating mode and enable/disable functions are controlled by the corresponding registers VSWx_STBY[7:0], SWx_STBY_MODE, VLDOx_STBY[3:0], and LDOx_STBY_EN bits.

Upon power up the VSWx_STBY[7:0], bits are loaded with the values of the OTP_VSWx[7:0], bits respectively. The VSWx_STBY[7:0] , VLDOx_STBY[3:0] bits can be modified at any time during the System ON States (Run and Standby) and INIT state. The SWx_STBY_MODE, and LDOx_STBY_EN bits can be modified at any time during the System ON States (Run and Standby) and INIT states.

Upon power up, if the regulator is part of the Power-up sequence, the SWx_STBY_MODE[1:0] bits will be loaded as needed by the system:

- When OTP_SYNC_EN = 1, default SWx_STBY_MODE at power up will always be PWM (0b01)
- When OTP_FSS_EN = 1, default SWx_STBY_MODE at power up will always be PWM (0b01)
- If none of the Conditions above are met, the default SWx_STBY_MODE bit at power up will be set by the OTP_SW_MODE bits.
  When OTP_SW_MODE = 0, the default value of the SWx_STBY_MODE[1:0] bits will be 0b10 (PFM).
  The PFM configuration is applicable for SWx switching frequency set in the range of 2 MHz to 3 MHz.
  When OTP_SW_MODE = 1, the default value of the SWx_STBY_MODE[1:0] bits will be 0b01 (PWM).
  Upon power up, the Standby registers are loaded with the same default OTP values as the Run mode. The processor is expected to program the desired Standby values during boot up.
  If any of the regulators are disabled during the transition into the Standby state, the power-down sequencer will be engaged. Upon state transition to the Run state, the disabled regulators will be re-enabled by engaging the power up sequencer again.

13.1.9 Power-down state

During the Power-down state, all regulators are disabled as configured in the power-down sequence. The power-down sequence is programmable as defined in Section 14.5.2.

Two types of events may lead to the power-down sequence:

- Non faulty turn off events: Depending on the ULP_OFF_CTRL bit, move directly into LP_Off state or ULP_OFF state as soon as the power-down sequence is finalized.
- Turn off events due to a PMIC fault: move to the fail-safe transition as soon as the power-down sequence is finalized.

13.1.10 Fail-safe state

The Fail-safe state is a fault state where the PMIC turns off the regulators and remains either in an off mode or restarts the Power-up sequence. The transition to this state is due to any following PMIC faults: power-up fault (PU_FAIL), PGOOD sense fault (PG_FAIL), PGOOD short to high, FAULT_CNT = FAULT_MAX_CNT (REG_FAIL), junction temperature > the thermal shutdown threshold (TSD_FAIL) and register CRC error.

The Fail-safe state will provide the following status bits:

- PU_FAIL will be set to 1 when the state machine powered down due to a power-up failure.
- PG_FAIL will be set to 1 when the state machine powered down due to a PGOOD failure.
- REG_FAIL will be set to 1 when the state machine powered down due to a regulator failure (fault counter maxed out).
- TSD_FAIL will be set to 1 when the state machine powered down due to a thermal shutdown.

The FAIL bits will be reset to 0 when VIN crosses the UVDET threshold. The processor can read the FAIL bits during the System ON states (Run and Standby) and the INIT state, in order to obtain information about the previous failure, provided the state machine is able to power up successfully after such failure. The processor can clear the FAIL bits by writing a 1 to them during the System ON states (Run and Standby) and INIT state, provided the state machine is able to power up successfully after such failure.

The Fail-safe state will work as a safety transition during a fault or as a lock-down upon a critical device/ system failure. Upon entering the Fail-safe state, the OTP_FS_BYPASS bit configures whether the state machine will be able to exit the state back in to the System ON states through LP_Off or stay in the Fail-safe state. When the OTP_FS_BYPASS bit =0, the fail-safe bypass feature is disabled, and the state machine will remain in the Fail-safe state indefinitely. When the OTP_FS_BYPASS bit =1, the Fail-safe bypass feature is enabled, and the state machine will be allowed to transition from the Fail-safe state to LP_Off state depending on OTP_FS_BYPASS_CNT bit. The state machine will provide a Fail-safe bypass counter configured by OTP_FS_BYPASS_CNT bit to count the number of bypass transitions. The Fail-safe bypass counter is incremented every time the transition from Fail-safe state to LP_Off state happens.

When OTP_FS_BYPASS_CNT bit =0, the number of transitions allowed will be configured to 15.
When OTP_FS_BYPASS_CNT bit =1, the number of transitions allowed will be infinite. When OTP_FS_BYPASS_CNT bit =0, and if the Fail-safe bypass counter reaches the maximum count value of 15, the state machine will stay in the Fail-safe state.

In the Fail-safe state, all the regulators will be disabled.

14 General device operation

14.1 UVDET

UVDET works as the main operation threshold for the PF5103. Crossing UVDET on the rising edge is a mandatory condition for OTP fuses to be loaded into the mirror registers and allows the main PF5103 operation.

If VIN is below the UVDET threshold, the device remains in an unpowered state. Hysteresis (150 mV) is implemented on the UVDET comparator to set the falling threshold.

Table 12. UVDET threshold

Symbol	Parameter	Min	Typ	Max	Unit
$UVDET_{\_R}$	Rising UVDET	2.85	2.95	3.05	V
$UVDET_{\_F}$	Falling UVDET	2.7	2.8	2.9	V

14.2 VIN OVLO condition

The VIN_OVLO circuit monitors the main input supply of the PF51x3. When this block is enabled, the PF51x3 monitors its input voltage and can be programmed to react to an overvoltage in two ways:

- When the VIN_OVLO_SDWN = 0, the VIN_OVLO event triggers an OVLO interrupt but does not turn off the device
- When the VIN_OVLO_SDWN = 1, the VIN_OVLO event initiates a power-down sequence

When the VIN_OVLO_EN = 0, the OVLO monitor is disabled and when the VIN_OVLO_EN = 1, the OVLO monitor is enabled. The default configuration of the VIN_OVLO_EN bit is set by the OTP_VIN_OVLO_EN bit in OTP. Likewise, the default value of the VIN_OVLO_SDWN bit is set by the OTP_VIN_OVLO_SDWN upon power up.

During a power up transition, if the OTP_VIN_OVLO_SDWN = 0 the device allows the external regulators to come up and the PF51x3 announces the VIN_OVLO condition through an interrupt. If the OTP_VIN_OVLO_SDWN = 1, the device stops the Power-up sequence and returns to the corresponding Off mode.

Debounce on the VIN_OVLO comparator is programmable to 10 µs, 100 µs or 1.0 ms, by the VIN_OVLO_DBNC[1:0] bits. The default value for the VIN_OVLO debounce is set by the OTP_VIN_OVLO_DBNC[1:0] bits upon power up.

Table 13. VIN_OVLO debounce configuration

VIN_OVLO_DBNC[1:0]	VIN OVLO debounce value (µs)
00	10
01	100
10	1000
11	Reserved

Table 14. VIN_OVLO specifications

Symbol	Parameter	Min	Typ	Max	Unit
VIN_OVLO	VIN overvoltage lockout rising [1]	5.6	5.8	6.0	V
VIN_OVLO_HYS	VIN overvoltage lockout hysteresis [1]	—	—	200	mV

[1] Operating the device above the maximum VIN = 5.5 V for an extended period of time may degrade and cause permanent damage to the device.

14.3 IC startup timing

The PF5103 executes the OTP fuse load and self-test before starting the regulator Power-up sequence. The device detects the PWRON signal when VIN is above UVDET and the internal POR is released.

Timing of the regulator Power-up sequence is programmed by OTP.

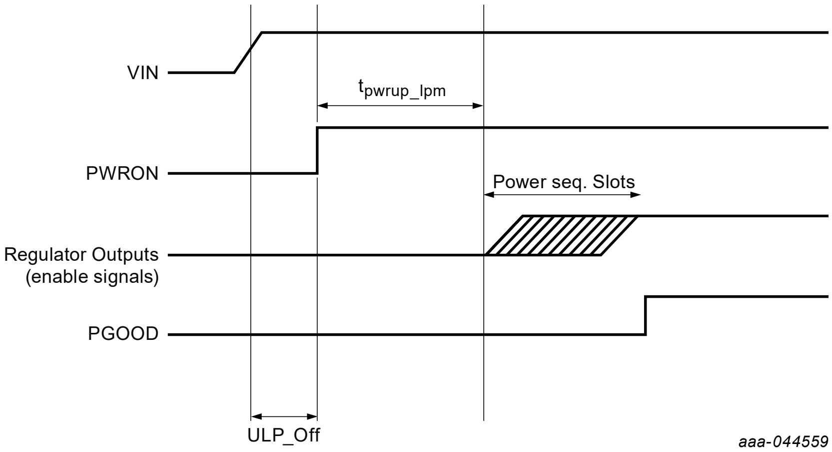


Figure 10. Startup with PWRON pulled high

Table 15. Startup timing requirements (PWRON pulled up)

Symbol	Parameter	Min	Typ	Max	Unit
t_{pwrup_lpm}	Time from PWRON going high to the first slot of the Power-up sequence	—	—	1000	µs

14.4 Power up

14.4.1 Power-up events

Upon a power cycle (VIN > UVDETr), the device moves to the ULP_Off state by default. A power-up event is valid only if:

- VIN > UVDETf
- VIN < VIN_OVLO (unless the OVLO is disabled or OTP_VIN_OVLO_SDWN = 0)
- Tj < thermal shutdown threshold
- TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0
- XFAILB is released (if XFAILB is enabled)
- No OTP CRC error

14.4.2 Power-up sequencing

The power-up sequencer controls the time and order in which the voltage regulators and other controlling I/O are enabled when going from the Off mode into the Run state.

The OTP_SEQ_TBASE[1:0] bits set the default time base for the power-up and power-down sequencer.

The SEQ_TBASE[1:0] bits can be modified during the I/O Release, INIT and System On states (Run and Standby) in order to change the sequencer timing during Run/Standby transitions as well as the power down sequence.

Table 16. Power up time base register

OTP bits OTP_SEQ_TBASE[1:0]	Functional bits SEQ_TBASE[1:0]	Sequencer time base (µs)
00	00	100
01	01	250
10	10	500
11	11	1000

The Power-up sequence may include any of the following:

- Switching regulators
- LDOs
- PGOOD pin if assigned a slot

The x_SEQ[5:0] bits set the regulator/pin sequence from 0 to 62. Sequence code 0x00 indicates that the particular output is not part of the startup sequence and remains in OFF (in case of a regulator) or remains low/ disabled (in case PGOOD pin is used as a GPO).

Table 17. Power-up sequence registers

OTP bits OTP_SWx_SEQ[5:0]/ OTP_LDOx_SEQ[5:0]/ OTP_PGOOD_SEQ[5:0]/	Functional bits SWx_SEQ[5:0]/ LDOx_SEQ[5:0]/ PGOOD_SEQ[5:0]/	Sequence slot	Startup time (µs)
000000	000000	Off	Off
000001	000001	0	SLOT0 (right after PWRON event is valid)
000010	000010	1	SEQ_TBASE x SLOT1
. . .	. . .	. . .	. . .
111111	111111	62	SEQ_TBASE x SLOT62

If PGOOD is not programmed in the OTP sequence, it will be enabled by default after the last regulator programmed in the Powerup sequence successfully powers up.

When the x_SEQ[5:0] bits of all regulators and PGOOD are set to 0x00 (OFF) and a power on event is present, the device moves to the I/O release state in a companion mode. In this mode, the device is enabled without any voltage regulator or PGOOD enabled. Since PGOOD is not programmed in a power up sequence slot, a PGOOD_RLS bit is used to release PGOOD in order for the device to enter the Run state. If OTP_PGOOD_SEQ[5:0] = 0x00, the default value of the PGOOD_RLS=0. The processor can decide to release this bit after turning any one or all of the regulators. When the processor sets PGOOD_RLS=1, then the device will release PGOOD after verifying all the signals assigned to the PGOOD monitor block. The companion mode is a special case of the Power-up sequence to address the scenario where the PF5103 is working as a companion PMIC, and supplies are meant to be enabled by the processor during the system operation. In this scenario, if PGOOD is used, it is connected to the PGOOD pin of the primary PMIC.

Figure 11 provides an example of the power-up/down sequence coming from the Off modes.

The PWRUP_I interrupt bit is asserted at the end of the Power-up sequence when the time slot of the last regulator in the sequence has ended.

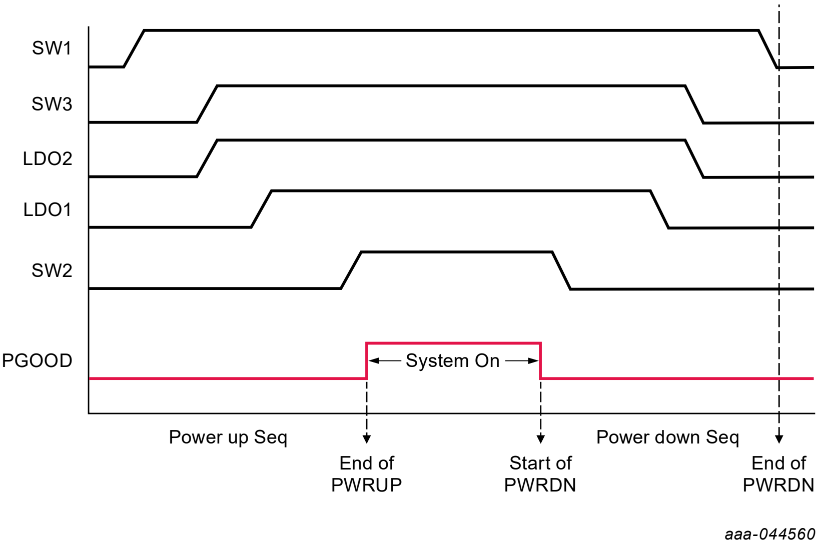


Figure 11. Power-up/down sequence between Off and system On state

When transitioning from Standby mode to Run mode, the power up sequencer is activated only if any of the external regulators is re-enabled during this transition. If none of the regulators toggle from Off to On and only voltage changes are being performed when entering or exiting Standby mode, the changes for the voltage regulators are made simultaneously rather than going through the power up sequencer.

Figure 12 shows an example of the power up/down sequence when transitioning between Run and Standby modes.

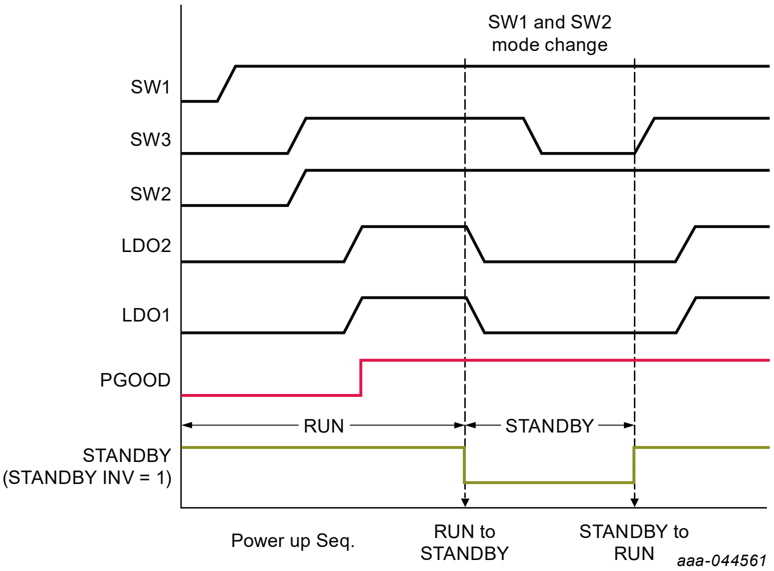


Figure 12. Power up/down sequence between Run and Standby state

The PWRUP_I interrupt is set while transitioning from Standby to Run, even if the sequencer is not used. This is used to indicate that the transition is complete and the device is ready to perform proper operation.

14.5 Power down

14.5.1 Turn-off events

Turn off events may be requested by the processor (non-PMIC fault related) or due to a critical failure of the PMIC (hard fault condition).

The following are considered non-PMIC failure turn-off events:

1. The device starts a power-down sequence when the PWRON pin is pulled low.
2. When bit PMIC_OFF is set to 1, the device starts a 500 µs shutdown timer. When the shutdown timer is started, the PF5103 sets the SDWN_I interrupt and asserts the INTB pin provided it is not masked. At this point, the processor can read the interrupt and decide whether to continue with the turn off event or stop it in case it was sent by mistake. If the SDWN_I bit is cleared before the 500 µs shutdown timer is expired, the shutdown request is canceled and the shutdown timer is reset; otherwise, if the shutdown timer is expired, the PF5103 starts a power down sequence. The PMIC_OFF bit self-clears after SDWN_I flag is cleared.
3. When XFAILB gets pulled low externally in a multi-PMIC scenario.
4. When VIN_OVLO_EN = 1 and VIN_OVLO_SDWN = 1, and a VIN_OVLO event is present.
5. When a BG/VIN monitor failure is detected.

Turn off events due to a hard fault condition:

1. If an OV, UV, ILIM or any other PMIC fault condition is present and the FAULT_CNT[3:0] = FAULT_MAX_CNT[2:0].
2. When a PGOOD sense fault is detected.
3. When a PGOOD short to high fault is detected.
4. When a power-up failure is detected.
5. When Tj crosses the thermal shutdown threshold (TSD) as the temperature rises.
6. When a register CRC error is detected.
   When the PF5103 experiences a turn off event due to a hard fault condition, the device initiates the power-down sequencer, passed through the fail-safe state after the regulators have been powered down.

14.5.2 Power-down sequencing

Sequential power down

When the device is set to the sequential power down, it uses the same x_SEQ[5:0] registers as the power-up sequence to power down in reverse order. All regulators with the x_SEQ[5:0] bits set to 0x00, power down immediately and the remaining regulators power down one OTP_SEQ_TBASE[1:0] delay afterwards, in reverse order as defined in the x_SEQ[5:0] bits. If PGOOD pin is used as a GPO, it is de-asserted as part of the power down sequence as indicated by the PGOODx_SEQ[5:0] bits.

If the processor requires a different power-down sequence, it can change the values of the SEQ_TBASE[1:0] and the x_SEQ[5:0] bits during I/O Release, System On and INIT states state. When the state machine passes through any of the Off modes, the contents of the SEQ_TBASE[1:0] and x_SEQ[5:0] bits are reloaded with the corresponding mirror register (OTP) values before it starts the next power up sequence.

Non-PMIC fault turn off events will transition to ULP_Off or LP_off (based on ULP_OFF_CTRL bit) state after the power-down sequence is finished.

The PWRDN_I interrupt is set at the end of the transition from Run to Standby when the last regulator has reached its final state, even if external regulators are not turned off during this transition.

14.5.2.1 Power-down delay

After a power-down sequence is started, the PWRON pin shall be masked until the sequence is finished and the programmable power-down delay is reached. The device can power up again if a power-up event is present. The power-down delay time can be programmed on an OTP via the OTP_PD_SEQ_DLY[2:0] bits.

Table 18. Power-down delay selection

OTP_PD_SEQ_DLY[2:0]	Delay after power down sequence
000	No delay
001	1.0 ms
010	10 ms
011	50 ms
100	100 ms
101	250 ms
110	500 ms
111	1000 ms

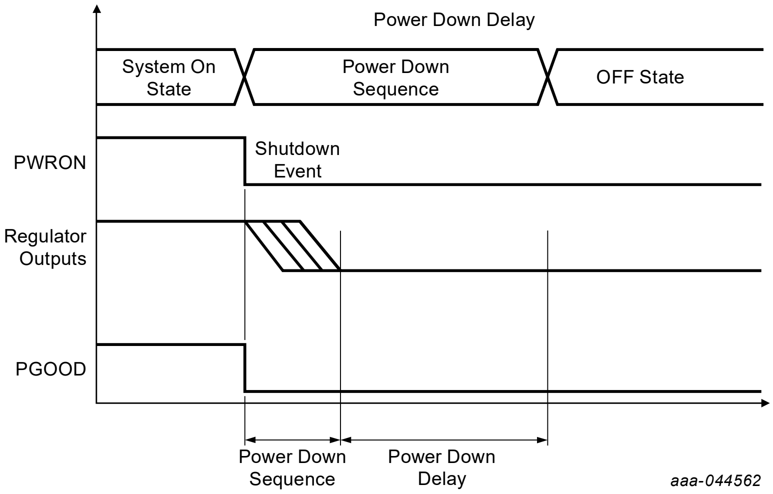


Figure 13. Power down delay

The default value of the OTP_PD_SEQ_DLY[2:0] bits on an unprogrammed OTP device is 00.

14.6 Regulator fault management

Three types of faults are monitored per regulator: UV, OV and ILIM. Faults are monitored during the Power-up sequence, I/O Release, INIT, and System On State (RUN and Standby) states.

A fault event is notified to the processor through the INTB pin if the corresponding fault is not masked. The fault configuration registers are reset to their default value after the power up sequences, and the system must configure them as required during the boot-up process via I^2C commands.

For each type of fault, there is an I^2C bit that is used to select whether the regulator is kept enabled or disabled when the corresponding regulator experiences a fault event.

x_ILIM_STATE

- 0 = regulator disables upon an ILIM fault event
- 1 = regulator remains on upon an ILIM fault event

x_OV_STATE

- 0 = regulator disables upon an OV fault event
- 1 = regulator remains on upon an OV fault event

x_UV_STATE

- 0 = regulator disables upon a UV fault event
- 1 = regulator remains on upon a UV fault event

The following table lists the functional bits associated with enabling/disabling the external regulators when they experience a fault.

Table 19. Regulator control during fault event bits

Regulator	Bit to disable the regulator during current limit	Bit to disable the regulator during undervoltage	Bit to disable the regulator during overvoltage
SWx	SWx_ILIM_STATE	SWx_UV_STATE	SWx_OV_STATE
LDOx	LDOx_ILIM_STATE	LDOx_UV_STATE	LDOx_OV_STATE

ILIM faults are debounced for 1.0 ms before they can be detected as a fault condition. If the regulator is programmed to disable upon an ILIM condition, the regulator turns off as soon as the ILIM condition is detected.

OV/UV faults are debounced for a defined filter time before they are detected as a fault condition. If the regulator is programmed to disable upon an OV or UV, the regulator will turn off if the fault persists for longer than 300 µs after the OV/UV fault has been detected.

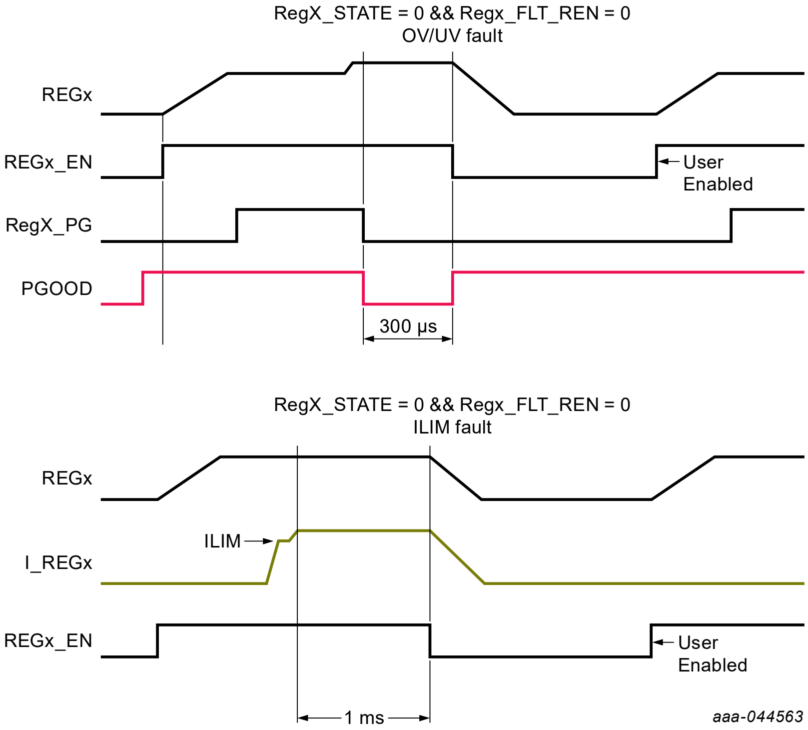


Figure 14. Regulator turned off upon OV, UV or ILIM fault, with RegX_STATE = 0 and FLT_REN = 0

When a regulator is programmed to disable upon an OV, UV, or ILIM fault, a bit is provided to decide whether a regulator can return to its previous configuration or remain disabled when the fault condition is cleared.

x_FLT_REN

- 0 = regulator remains disabled after the fault condition is cleared or no longer present
- 1 = regulator returns to its previous state if fault condition is cleared

If a regulator is programmed to remain disabled after clearing the fault condition, the processor can turn it back ON in I/O Release, INIT and System On states by toggling OFF and ON the corresponding mode/enable bits.

When the bit x_FLT_REN = 1, if a regulator is programmed to turn off upon an OV, UV or ILIM condition, the regulator returns to its previous state 500 µs after the fault condition is cleared. If the regulator is programmed to turn off upon an ILIM condition, the device may take up to 1.0 ms to debounce the ILIM condition removal, in addition to the 500 µs wait period to re-enable the regulator.

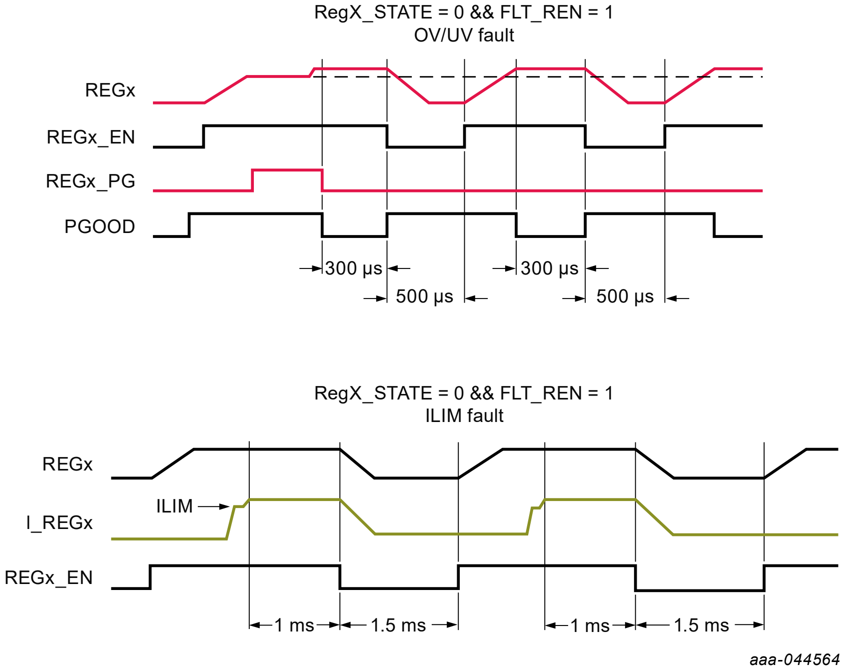


Figure 15. Regulator turned off upon OV, UV or ILIM fault, with RegX_STATE = 0 and FLT_REN = 1

To avoid fault cycling, a global fault counter is provided. Each time any of the external regulators encounter a fault event, the PF5103 compares the value of the FAULT_CNT[3:0] against the OTP_FAULT_MAX_CNT[2:0].

Table 20. Fault timer register configuration

OTP bits OTP_FAULT_MAX_CNT [2:0]	Functional bits FAULT_MAX_CNT [2:0]	Value
000	000	1
001	001	2
010	010	4
011	011	6
100	100	8
101	101	10
110	110	12
111	111	15

Every time any of the regulators encounter a fault event and the corresponding x_BYPASS bit is 0, the logic will compare the FAULT_CNT[3:0] to the FAULT_MAX_CNT[2:0] register.

Table 21. Fault count register

Functional Bits FAULT_CNT [3:0]	Value
0000	0
0001	1
0010	2
0011	3
0100	4

Table 21. Fault count register*...continued*

Functional Bits FAULT_CNT [3:0]	Value
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

If the FAULT_CNT[3:0] = FAULT_MAX_CNT[2:0], it initiates the fault protection mechanism as programed in the Functional Register bits.

The fault protection mechanisms are the following:

- Disable the faulty regulator or not as programmed with the x_fault_STATE bit
- Re-enable the faulty regulator if programmed with the x_FLT_REN bit

For ASIL B devices, the FAULT_CNT[3:0] bits can be decremented by doing a good watchdog refresh via an I2C command. A good WD refresh is done by writing the correct value to the WD_ANSWER register within the appropriate WD window period. If the processor does not decrement the fault counter and it equals the FAULT_MAX_CNT[2:0] value, the state machine initiates a power-down sequence. The FAULT_CNT[3:0] is reset to 0 when the state machine enters the LP_off state. Once regulators are turned off after a FAULT_CNT[3:0] maxed out, the device moves to the LP_off transition if FS_BYPASS=1. For each type of fault, there is an I^2C bit that is used to bypass the fault detection mechanism for that specific fault.

SWx_ILIM_BYPASS / LDOx_ILIM_BYPASS

0 = ILIM Protection enabled

1 = ILIM Fault bypassed

SWx_OV_BYPASS / LDOx_OV_BYPASS

0 = OV Protection enabled

1 = OV Fault bypassed

SWx_UV_BYPASS / LDOx_UV_BYPASS

0 = UV Protection Enabled

1 = UV Fault bypassed

Table 22. Fault bypass bits

Regulator	Bit to bypass a current limit	Bit to bypass an undervoltage	Bit to bypass an overvoltage
SWx	SWx_ILIM_BYPASS	SWx_UV_BYPASS	SWx_OV_BYPASS
LDOx	LDOx_ILIM_BYPASS	LDOx_UV_BYPASS	LDOx_OV_BYPASS

- The OTP_SWx_OV_BYPASS bits are used to bypass the OV Faults by default upon power up.
- The OTP_SWx_UV_BYPASS bits are used to bypass the UV Faults by default upon power up.
- The OTP_SWx_ILIM_BYPASS bits are used to bypass the ILIM Faults by default upon power up.
- The OTP_LDOx_OV_BYPASS bits are used to bypass the OV Faults by default upon power up.
- The OTP_LDOx_UV_BYPASS bits are used to bypass the UV Faults by default upon power up.
- The OTP_LDOx_ILIM_BYPASS bits are used to bypass the ILIM Faults by default upon power up.

Bypassing the fault detection prevents the specific fault to increment the counter and disable the regulator, if programmed to turn off upon the specific fault.

The OV condition will not assert the PGOOD pin if OTP_SWx_PG_EN/OTP_LDOx_PG_EN bits are set to 0.

The UV condition will not assert the PGOOD pin if OTP_SWx_PG_EN/OTP_LDOx_PG_EN bits are set to 0.

The ILIM condition will not by itself assert the PGOOD pin LOW or increment the fault counter.

Even if a specific fault is bypassed, the corresponding interrupt bit is still set and the INTB pin is asserted, provided the interrupt is not masked.

Table 23. Fault types and the corresponding PGOOD pins response

Safety mechanism	Monitored State	Error Flag	Fault Counter [1] [2] [3]	WD_ ERROR_CNT	PGOOD Low Assertion	FSM State Transition from INIT & System ON	Comments
SW1 UV	Power Up Sequence, I/O Release, INIT, and System ON states	SW1_UV_I	+1 if SW1_UV_ BYPASS bit = 0	—	Yes, if SW1_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
SW1 OV		SW1_OV_I	+1 if SW1_OV_ BYPASS bit = 0	—	Yes, if SW1_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
SW2 UV		SW2_UV_I	+1 if SW2_UV_ BYPASS bit = 0	—-	Yes, if SW2_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
SW2 OV		SW2_OV_I	+1 if SW2_OV_ BYPASS bit = 0	—	Yes, if SW2_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
SW3 UV		SW3_UV_I	+1 if SW3_UV_ BYPASS bit = 0	—	Yes, if SW3_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
SW3 OV		SW3_OV_I	+1 if SW3_OV_ BYPASS bit = 0	—	Yes, if SW3_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
LDO1 UV		LDO1_UV_I	+1 if LDO1_UV_ BYPASS bit = 0	—	Yes, if LDO1_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
LDO1 OV		LDO1_OV_I	+1 if LDO1_OV_ BYPASS bit = 0	—	Yes, if LDO1_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-upsequence
LDO2 UV	Power Up Sequence, I/O Release, INIT, and System ON states	LDO2_UV_I	+1 if LDO2_UV_ BYPASS bit = 0	—	Yes, if LDO2_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
LDO2 OV		LDO2_OV_I	+1 if LDO2_OV_ BYPASS bit = 0	—	Yes, if LDO2_PG_ EN bit = 1	I/O Release	Fault Shutdown from Power-up sequence
PGOOD short to high	Power Up Sequence, I/O Release, INIT, and System ON states	PG_SHORT_I	—	—	—	—	Fault Shutdown from Power-up sequence & I/O Release; No transition from INIT & System ON
BG1 & BG2 Drift apart or VIN OV/ UV (BGMON monitor)		BGMON_I VIN_OV_I VIN_UV_I	—	—	Yes, if OTP_ BGMON_ BYPASS=0 [4]	—	Power down
Reg map CRC error (OTP and functional bits)		REGMAP_ CRC_I	—	—	Yes[4]	—	Fault shutdown
CLOCK stuck monitoring		—	Cleared	—	Yes	—-	FSM reset/shutdown
Bad WD refresh	INIT, System ON states	WD_BAD_I	—	+2 if WD_EN = 1	—	—	—
WD Event	INIT, System ON states	WD_ EVENT_I	+1 if WD_EN = 1	—	Yes, if WD_EN = 1	I/O Release	—
FCCU fault with WDW recovery	System ON states	FCCU_I	+1 if OTP_ FCCU_EN= 1	—	No, if OTP_ WD_FAULT_ REC=1[5]	—	FSM stays in System ON [5]
FCCU fault w/o WDW recovery	System ON states	FCCU_I	+1 if OTP_ FCCU_EN= 1	—	Yes, if OTP_ WD_FAULT_ REC=0	I/O Release	—

Table 23. Fault types and the corresponding PGOOD pins response*...continued*

Safety mechanism	Monitored State	Error Flag	Fault Counter [1] [2] [3]	WD_ ERROR_CNT	PGOOD Low Assertion	FSM State Transition from INIT & System ON	Comments
FCCU short	Self-Test state	AB_FCCU_H	—	—	—	—	—
VIN_OV (OVLO monitor)	I/O Release, INIT, and System ON states	VIN_OVLO_I	1	—	Yes, if VIN_ OVLO_ SDWN=1 [4]	—	Power down
External reset from MCU (RSTB mode)	System ON state	RSTB_I	+1	—	—	—	FSM stays in System ON
ABIST OV/UV error (Startup and AB_RUN)	Self-Test state, I/O Release, INIT, and System ON states	AB_x_OV, AB_x_UV	—	—	—	—	—
VIN pin disconnection fault	INIT, I/O Release, System ON states	—	Cleared	—	Yes (analog safety path)	—	FSM reset/shutdown
OTP / TRIM corrupted	Self-Test state	OTP_NOK TRIM_NOK	—	—	Yes [6]	—	—
BG1 & BG2 Drift apart	Self-Test state	BGMON_I	—	—	Yes[6]	—	-—
CLK Drift Error 20 MHz and 100 KHz	Self-Test state	CLK_MON_I	—	—	Yes [6]	—	—
CLOCK sync error	INIT, System ON states	FSYNC_ FLT_I	—	—	—	—	Switch to internal CLK

[1] FAULT_ CNT reset to 0 in LP_Off mode.
[2] Even if a specific fault is bypassed, the corresponding interrupt bit is still set and the INTB pin is asserted, provided the interrupt is not masked.
[3] Fault count could be incremented more than once for the same type of fault (regx OV, UV) if the fault persists after the voltage setpoint changes. This could be either a voltage change in the same state or voltage change during state change b/w Run and Standby.
[4] Power-down/shutdown event. PGOOD doesn't get asserted low immediately upon fault. PGOOD assertion will be handled by the state machine and the sequencer.
[5] PGOOD gets asserted low if WDW recovery fails. FSM transitions to IO_Release.
[6] Startup fault. PGOOD is asserted by default as device doesn't progress to power up state. Valid only for normal mode.

14.6.1 Fault monitoring during Power-up state

The output voltage of each regulator is verified and the internal PGOOD signal must be released during the Power-up sequence to release the PGOOD. The OV and UV faults during the Power-up sequence are reported based on the internal PG (Power Good) signals of the corresponding regulator (provided the regulator output is assigned to the PGOOD signal). See Section 14.8.4 for details on PGOOD pin operation and configuration.

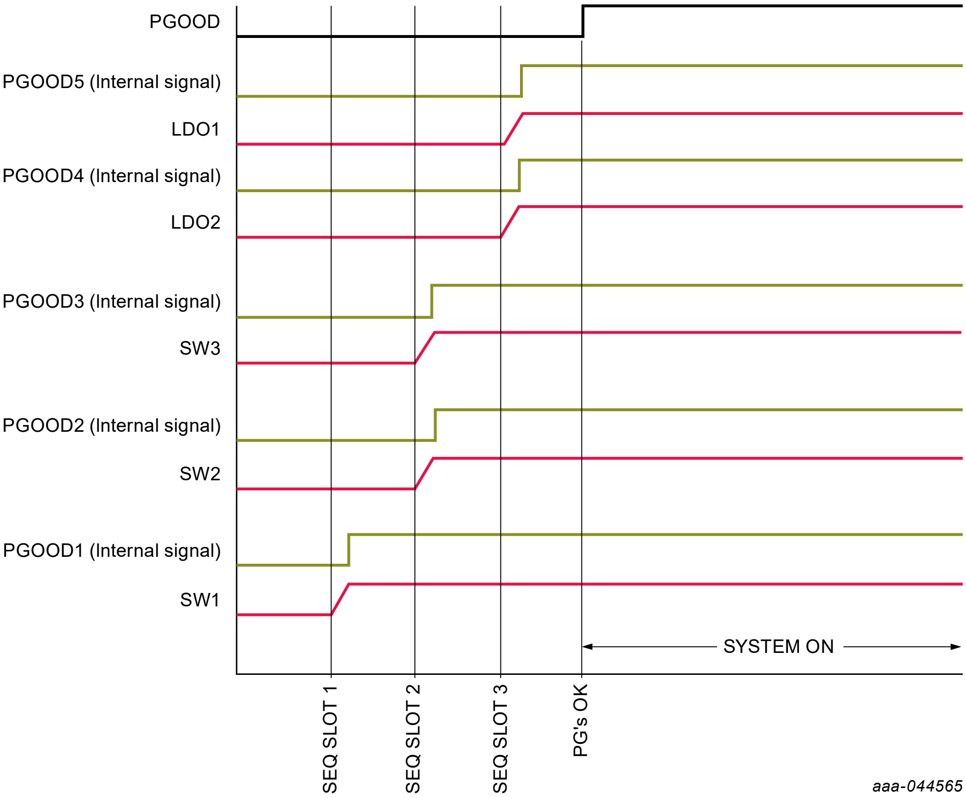


Figure 16. Regular startup with PGOOD released in the end (no slot assignment)

If any of the regulators powered up before PGOOD are out of regulation, PGOOD is not de-asserted and the power up sequencer waits for up to 2.0 ms. If the fault is cleared and all internal PG signals are de-asserted within the 2.0 ms timer, PGOOD is de-asserted and the Power-up sequence is completed as shown in Figure 17.

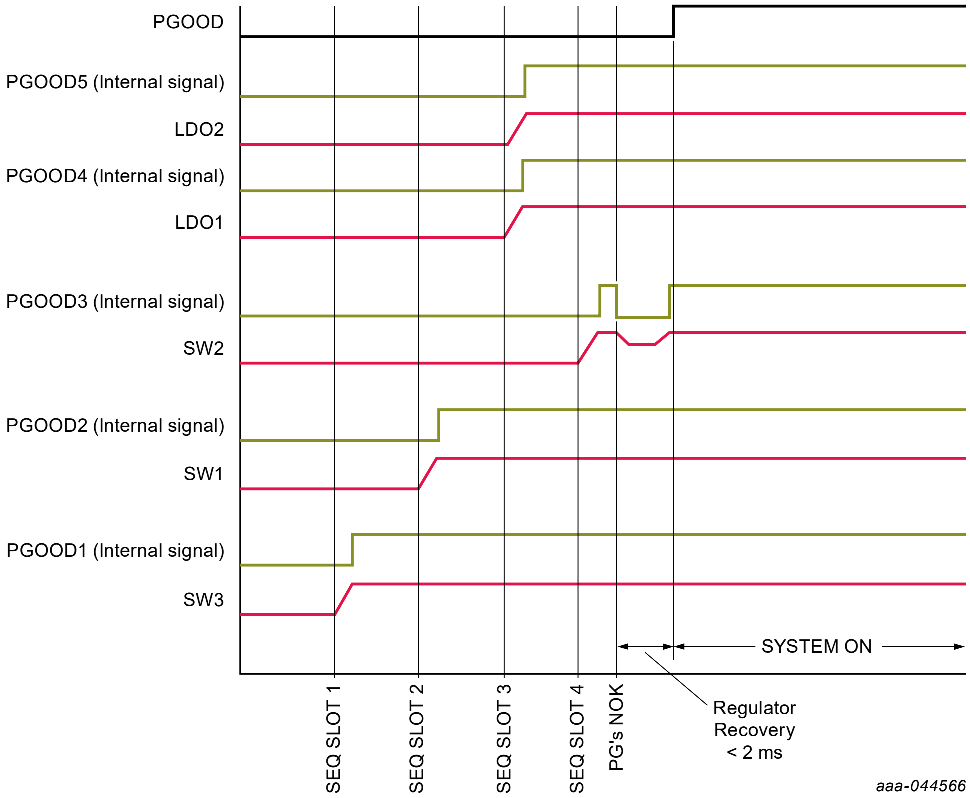


Figure 17. Regular startup with regulator recovery and PGOOD released in the end (no slot assignment)

If the faulty condition is not cleared within the 2.0 ms timer, the Power-up sequence is aborted and the PF5103 initiates a fault shutdown.

When PGOOD is assigned a slot during power up, the device checks for any OV/UV condition for the regulators turned on so far. If all regulators powered up before or in the same sequence slot as PGOOD are in regulation, PGOOD is de-asserted and the power up sequence continues.

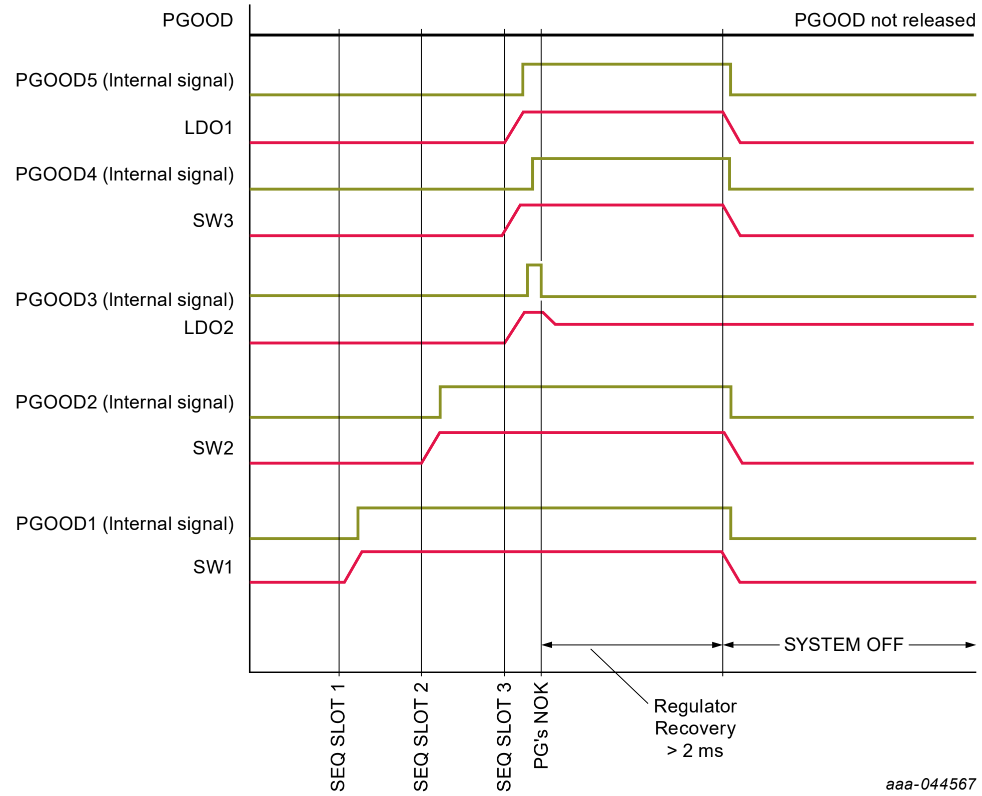


Figure 18. Power up sequencer aborted as fault persists for longer than 2.0 ms

Supplies enabled after PGOOD are checked for OV and UV faults after each of them are enabled. If an OV or UV condition is present, the PF5103 starts a fault detection and protection mechanism as described in Section 14.6. At this point, the processor should be able to read the interrupt and react upon a fault event as defined by the system.

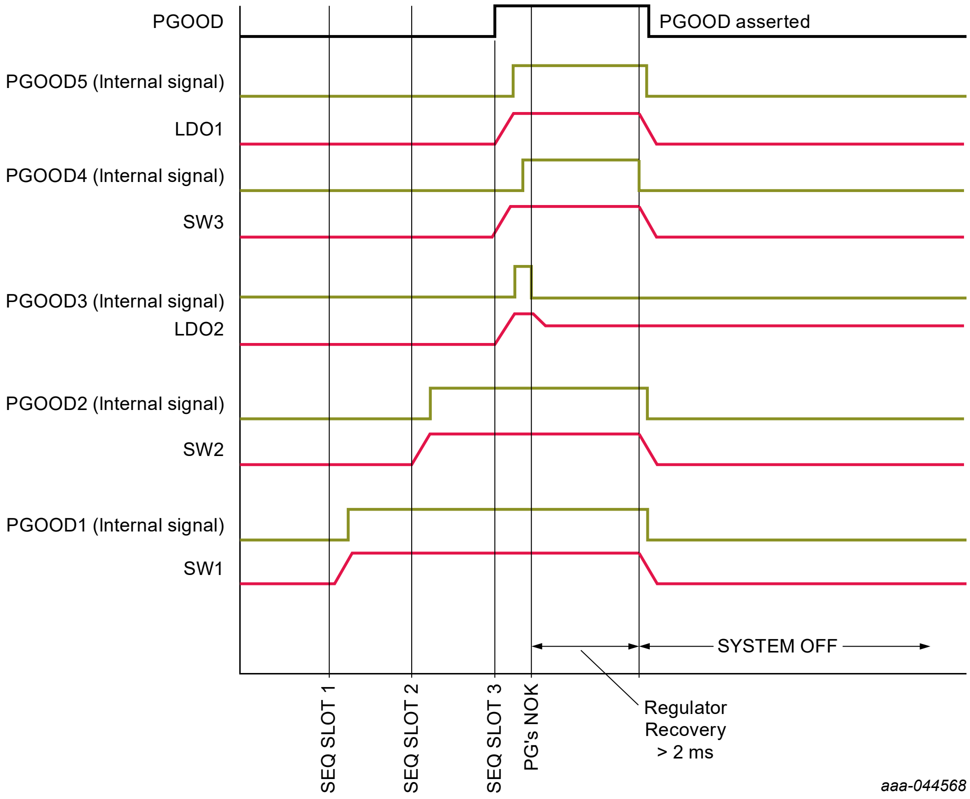


Figure 19. Regular startup with PGOOD released in the end (PGOOD assigned a slot)

14.7 Interrupt management

The processor is notified of any interrupt through various interrupt registers.

The interrupt registers are composed of three types of bits to help manage all the interrupt requests in the PF5103:

- The interrupt latch XXXX_I: This bit is set when the corresponding interrupt event occurs. It can be read at any time, and is cleared by writing a 1 to the bit.
- The sense bit XXXX_S: If available, the sense bit provides the actual status of the signal triggering the interrupt.
  Interrupts are stored in two levels on the interrupts registers. At the first level, the SYS_INT register provides information about the Interrupt register that originated the interrupt event.
  The corresponding SYS_INT bits are set with any of the interrupt bits of the respective interrupt registers.
- STATUS1_I: This bit is set when the interrupt is generated within the INT STATUS1 register.
- STATUS2_I: This bit is set when the interrupt is generated within the INT STATUS2 register.
- STATUS3_I: This bit is set when the interrupt is generated within the INT STATUS3 register.
- MODE_I: This bit is set when the interrupt is generated within the SW MODE INT register.
- ILIM_I: This bit is set when the interrupt is generated within any of the SWx/LDOx ILIM INT registers.
- UV_I: This bit is set when the interrupt is generated within any of the SWx/LDOx UV INT registers.
- OV_I: This bit is set when the interrupt is generated within any of the SWx/LDOx OV INT registers.
- PWRON_I: This bit is set when the interrupt is generated within the PWRON INT register.
  The SYS_INT bits are set by any of the second level interrupt bits that have not been masked in their corresponding mask registers. When the second level interrupt bit is cleared, the corresponding first level interrupt bit on the SYS_INT register will be cleared automatically.

After the first level interrupts bit is set, it will be de-asserted only when all the unmasked second level interrupts are cleared and thus all the first level interrupts are cleared as well. At the second level, the remaining registers provide the exact source for the interrupt event.

Table 24. Interrupt registers

Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INT STATUS1	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	—	PGOOD_I	VIN_OVLO_I
INT_MASK1	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	—	PGOOD_M	VIN_OVLO_M
INT_SENSE1	—	—	—	PWRON_S	—	—	PGOOD_S	VIN_OVLO_S
INT_STATUS2	WD_EVENT_I	WD_ERROR_I	WD_INIT_I	REGMAP_ CRC_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
INT_MASK2	WD_EVENT_M	WD_ ERROR_M	WD_INIT_M	REGMAP_ CRC_M	THERM_ 155_M	THERM_ 140_M	THERM_ 125_M	THERM_ 110_M
INT_SENSE2	—	—	—	—	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
INT_STATUS3	BGMON_I	FSYNC_I	FSYNC_FLT_I	CLK_MON_I	RSTB_I	FCCU_I	—	PG_SHORT_I
INT_MASK3	BGMON_M	FSYNC_M	FSYNC_FLT_M	CLK_MON_M	—	FCCU_M	—	PG_SHORT_M
INT_SENSE3	BGMON_S	FSYNC_S	FSYNC_FLT_S	—	RSTB_S	FCCU_S	—	—
SW_MODE_ INT	—	—	—	—	—	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
SW_MODE_ MASK	—	—	—	—	—	SW3_ MODE_M	SW2_ MODE_M	SW1_ MODE_M
REGx_ILIM_ INT	—	LDO2_ILIM_I	LDO1_ILIM_I	—	—	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I
REGx_ILIM_ MASK	—	LDO2_ILIM_M	LDO1_ILIM_M	—	—	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
REGx_ILIM_ SENSE	—	LDO2_ ILIM_S	LDO1_ILIM_S	—	—	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
REGx_UV_INT	VIN_UV_I	LDO2_UV_I		—	—	SW3_UV_I	SW2_UV_I	SW1_UV_I
REGx_UV_ MASK	VIN_UV_M	LDO2_UV_M	LDO1_UV_M	—	—	SW3_UV_M	SW2_UV_M	SW1_UV_M
REGx_UV_ SENSE	VIN_UV_S	LDO2_UV_S	LDO1_UV_S	—	—	SW3_UV_S	SW2_UV_S	SW1_UV_S
REGx_OV_INT	VIN_OV_I		LDO1_OV_I	—	—	SW3_OV_I	SW2_OV_I	SW1_OV_I
REGx_OV_ MASK	VIN_OV_M	LDO2_OV_M	LDO1_OV_M	—	—	SW3_OV_M	SW2_OV_M	SW1_OV_M
REGx_OV_ SENSE	VIN_OV_S	LDO2_OV_S	LDO1_OV_S	—	—	SW3_OV_S	SW2_OV_S	SW1_OV_S
SYS INT	—	STATUS3_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I

14.8 I/O interface pins

The PF5103 PMIC is fully programmable via the I^2C interface. Additional communication between the processor, PF5103 and other companion PMICs is provided by direct logic interfacing, including PGOOD, among other pins.

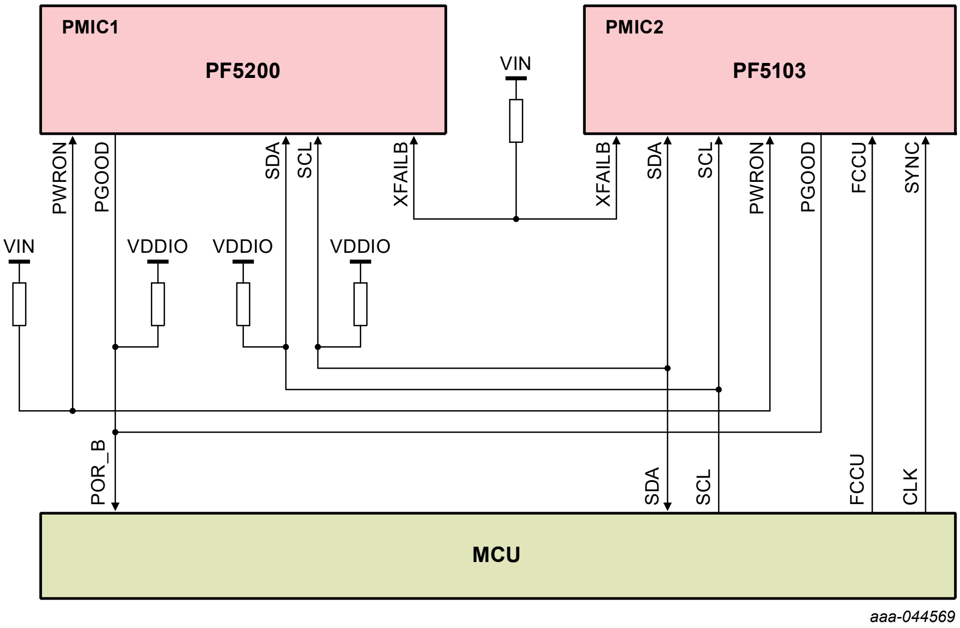


Figure 20. Multi-PMIC interface diagram

Table 25. I/O electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
PWRON_V_{IL}	PWRON low input voltage	—	—	0.4	V
PWRON_V_{IH}	PWRON high input voltage	1.4	—	5.5	V
FCCU_V_{IL}	FCCU low input voltage	—	—	0.4	V
FCCU_V_{IH}	FCCU high input voltage	1.4	—	5.5	V
SYNC_STANDBY_V_{IL}	Standby low input voltage	—	—	0.4	V
SYNC_STANDBY_V_{IH}	Standby high input voltage	1.4	—	5.5	V
PGOOD_V_{OL}	PGOOD low output voltage −2.0 mA load current	0	—	0.4	V
PGOOD_V_{IH}	PGOOD monitor high input voltage −2.0 mA load current	1.4	—	5.5	V
INTB_RSTB_V_{OL}	INTB low output voltage −2.0 mA load current	0	—	0.4	V
INTB_RSTB _V_{IL}	RSTB low input voltage	0	—	0.4	V
INTB_RSTB _V_{IH}	RSTB high input voltage	1.4	—	5.5	V
XFAILB_V_{IL}	XFAILB low input voltage	0	—	0.4	V
XFAILB_V_{IH}	XFAILB high input voltage	1.4	—	5.5	V
XFAILB_V_{OH}	XFAILB high output voltage Pulled-up to V1P6	V1P6 − 0.5	—	—	V
XFAILB_V_{OL}	XFAILB low output voltage −2.0 mA load current	0	—	0.4	V
SCL_V_{IL}	SCL low input voltage	0	—	0.4	V
SCL_V_{IH}	SCL high input voltage	1.4	—	5.5	V

Table 25. I/O electrical specifications*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
SDA_V_{IL}	SDA low input voltage	0	—	0.4	V
SDA_V_{IH}	SDA high input voltage	1.4	—	5.5	V
SDA_V_{OL}	SDA low output voltage −20 mA load current	0	—	0.4	V

14.8.1 PWRON

PWRON is an input signal to the IC that acts as a power-up event signal in the PF5103.

The PWRON pin operates in level sensitive mode. In this mode, the device is in the corresponding off mode when the PWRON pin is pulled low. Pulling the PWRON pin high is a necessary condition to generate a power on event.

PWRON may be pulled up to VIN with an external 10 kΩ resistor if device is intended to come up automatically with VIN application. See Section Section 14.4 for details on power-up requirements.

14.8.2 INTB/RSTB

The INTB_RSTB pin is a dual-function pin used either as an open-drain, active-low output or as an input.

The INTB_RSTB can also be used as an RSTB input, as a secondary function based on the OTP_INTB_RSTB bit selection.

Table 26. OTP_INTB_RSTB bit

OTP_INTB_RSTB	Description
0	INTB function enabled
1	RSTB function enabled

INTB is asserted (i.e., pulled low) when any interrupt occurs, provided that the interrupt is unmasked.

The INTB is asserted on the rising edge of the interrupt bits.

INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the interrupt bit.

An INTB_TEST bit is provided to allow a manual test of the INTB pin.

When INTB_TEST is set to 1, the interrupt pin will assert for 100 µs and then de-assert to its normal state.

The INTB_TEST bit is reset to 0 automatically after the test pulse is generated.

See Section 14.7 for interrupt management details.

In the application, the INTB (RSTB) pin can be pulled up to the 1.8 V or 3.3 V source with an external pull-up resistor.

14.8.3 SYNC/STANDBY

The SYNC_STANDBY pin has dual functions. It is used either as the clock synchronization input (SYNC) or Standby mode selection (Standby). The Standby function can be enabled when the SYNC function is disabled (SYNC_EN=0). If not used as SYNC, this pin can be selected in OTP to be used as the Standby input, using the OTP_SYNC_STBY bit.

Table 27. OTP_SYNC_STANDBY bit

OTP_SYNC_STBY	Description
0	Standby mode disabled
1	Standby mode enabled

STANDBY can be configured as active high or active low using the STANDBYINV bit.

Table 28. Standby pin polarity control

STANDBY (pin)	STANDBYINV (I^2C bit)	STANDBY control
0	0	Not in Standby mode
0	1	In Standby mode
1	0	In Standby mode
1	1	Not in Standby mode

14.8.4 PGOOD

PGOOD is an open drain output used as a PGOOD indicator pin. PGOOD can be assigned a slot in the Power-up sequence (to behave like a GPO), or it can be released after all the regulators in the slot have turned on.

If PGOOD is not assigned to any slot in OTP_PGOOD_SEQ[5:0], the PGOOD pin is released or de-asserted at the end of the Power-up sequence and before entering the I/O Release state. The PGOOD pin is driven low or asserted when it is out of the RUN state and enters the Fail-Safe state .

When VIN is applied, the PGOOD pin is driven low as soon as the logic is able to control, to ensure no floating condition is present on the load being controlled by this pin.

The pin acts as a PGOOD indicator that provides the status of all the selected regulator outputs in the PF5103. There is an individual Power Good monitor for every regulator that reports its status via I^2C registers.

The PG_S bit for a particular regulator goes low if the regulator sees an output in an undervoltage or overvoltage condition. There is a global PGOOD_S sense signal to report the real time value of the PGOOD signal.

The status of the PGOOD pin is a logic AND function of the internal SWx_PG_S bits of selected individual monitors.

The PGOOD pin is pulled low when any of the selected regulator outputs falls above or below the programmed OV/UV thresholds.

If the faulty condition is removed, the corresponding PG_S bit goes high to indicate the output is back in regulation, however, the interrupt remains latched until it is cleared.

When bit x_PG_EN = 1(OTP_x_PG_EN), the PG bit of that specific regulator (SWx/LDOx) becomes part of the AND function that controls the PGOOD pin.

When a particular regulator is disabled (via OTP, I^2C, or by a change in state of the PMIC such as going to STANDBY state), it no longer controls the PGOOD pin and its respective PG_S bit goes to 0.

If all regulators are disabled, the PGOOD pin is asserted low to indicate there are no supplies enabled.

The PGOOD pin is low in the OFF modes.

The PGOOD pin is asserted low during the Power-up sequence.

If all internal PG_S bits configured as part of the logic AND controlling the PGOOD pin are high by the time power up sequencing is completed, the PGOOD pin is de-asserted.

If at least one of the internal PG_S bits configured as part of the logic AND controlling the PGOOD pin is low during the power up sequencing, the PGOOD pin is kept low as long as the fault condition is not cleared.

In the application, PGOOD can be pulled up to 1.8 V or 3.3 V source with a pull-up resistor.

A PG interrupt is generated when a regulator experiences an OV, UV condition.

The actual condition causing the interrupt (OV, UV) can be read in the Fault Interrupt Registers.

For more details on interrupt management, refer to section Section 14.7.

The PGOOD_S bit is available to report the real time status of the PGOOD pin.

Table 29. PGOOD_S bit

PGOOD_S	Description
0	low
1	high

The PG_SHORT_I bit is available to notify the processor about the PGOOD short to high status.

Table 30. PG_SHORT_I bit

PG_SHORT_I	Description
0	No short detected
1	Short to high

A PGOOD short to high check is performed before releasing the PGOOD signal during the Power-up sequence and I/O Release states. A PGOOD short to high check is performed before the assertion of the PGOOD signal during the Power-up sequence, I/O Release, INIT, and System On states.

PGOOD is asserted for 2 ms after every event that is programmed to assert PGOOD. If a fault condition is not removed, PGOOD is kept in low. Refer to section Section 14.6.1 for details on the Power up fault timer operation. Refer to section Section 14.6 for details on the sources of faults causing PGOOD assertion.

The actual condition causing the interrupt (OV, UV) can be read in the fault interrupt registers. For more details on handling interrupts, see Section 14.7. When a particular regulator is disabled (via OTP, I^{2}C, or by a change in state of the PMIC such as going to Standby mode) it no longer controls the PGOOD pin.

14.8.5 FCCU (ASIL B)

The FCCU input pin monitors hardware failures from an NXP processor, or any other error output from a non-NXP processor. The initial PF5103AMBA0 prototypes do not contain the FCCU feature. Future builds with the same part numbers will implement this FCCU feature. Please refer to the date code and factory for further details.

The OTP_FCCU_EN bit will be used to enable the FCCU monitoring feature.

Table 31. OTP_FCCU_EN bit

OTP_FCCU_EN	Description
0	FCCU monitoring disabled
1	FCCU monitoring enabled

When the FCCU function is enabled in OTP, FCCU_CFG[1:0] bits will be used to configure the detection type as either input level detection (10) or as PWM detection (01).

Table 32. FCCU_CFG[1:0]

FCCU_CFG[1:0]	Description
00 (Default)	FCCU monitoring disabled
01	FCCU monitored with PWM detection
10	FCCU monitored with input level detection
11	Reserved

Monitoring of the FCCU pin becomes active after the INIT state.

The FCCU pin has an internal glitch filter, typically 10 μs for level detection and 1 μs for PWM detection. For processor diagnostics, the FCCU_S bit is available to report the real state of the FCCU pin to be used when X_CFG=10.

Table 33. FCCU_S bit

FCCU_S	Description
0	FCCU low
1	FCCU high

An FCCU_I interrupt bit is available to report to the processor of an error in the FCCU input.

Table 34. FCCU_I bit

FCCU_I	Description
0	No Error
1	Error detected

14.8.5.1 FCCU_CFG[1:0] = 01 (FCCU input monitoring with PWM detection)

In this configuration, the FCCU pin detects an error by monitoring a time switching or PWM waveform.

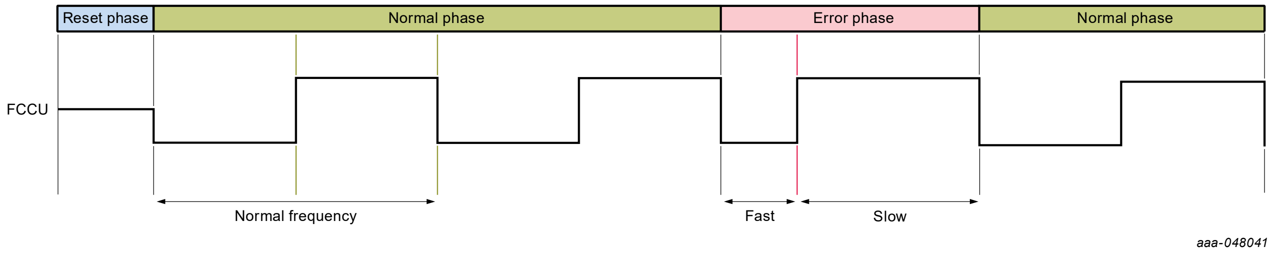


Figure 21. FCCU input monitoring with PWM detection

The normal frequency of the FCCU PWM signal is 11.7 kHz.

An error is reported in the following cases.

- FCCU pin at high level stays longer than the T_FCCU_slow time.
- FCCU pin at low level stays longer than the T_FCCU_slow time.
- FCCU pin at high level stays shorter than the T_FCCU_fast time.
- FCCU pin at low level stays shorter than the T_FCCU_fast time.

The assertion of the PGOOD low to an FCCU error is done based on fault types and the corresponding PGOOD response.

Table 35. FCCU signal detection time in PWM mode

Symbol	Parameter	Min	Typ	Max	Unit
T_FCCU_slow	FCCU signal slow detection time in PWM mode	54.4	64	73.6	µs
T_FCCU_fast	FCCU signal fast detection time in PWM mode	18.7	22	25.3	µs

14.8.5.2 FCCU_CFG[1:0] = 10 (FCCU single input monitoring activated)

In this configuration, the FCCU input is monitored for errors with single input level detection according to the configured polarity. The polarity of the FCCU fault signal is configurable using the FCCU_POL register.

Table 36. FCCU_POL

FCCU_POL	Description
0 (reset)	FCCU = 0 is a fault (Default)
1	FCCU = 1 is a fault

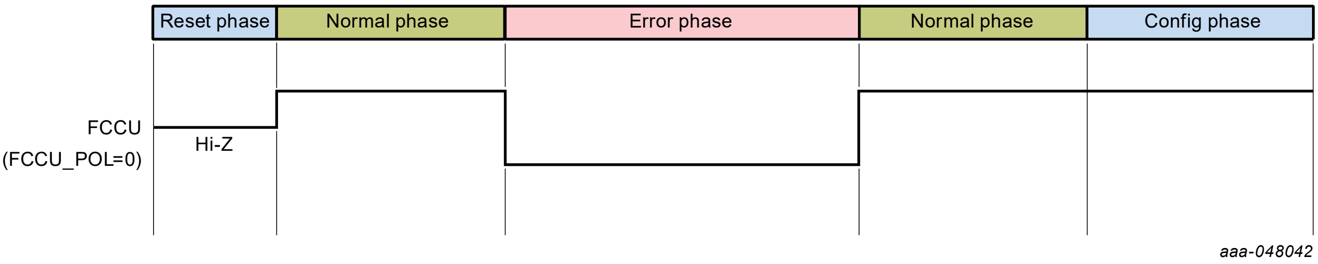


Figure 22. FCCU single input monitoring activated

An error is reported in the following cases.

- FCCU pin = Low and if FCCU_POL is set to "0".
- FCCU pin = High and if FCCU_POL is set to "1".

The assertion of the PGOOD low to an FCCU error are done based on fault types and the corresponding PGOOD response.

14.8.6 XFAILB

XFAILB is a bidirectional pin with an open drain output used to synchronize the power up and power-down sequences of two or more PMICs.

The OTP_XFAILB_EN bit is used to enable or disable the XFAILB mode of operation.

- When OTP_XFAILB_EN = 0, the XFAILB mode is disabled and any events on this pin are ignored.
- When OTP_XFAILB_EN = 1, the XFAILB mode is enabled

When the XFAILB mode is enabled, and the PF5103 has a turn off event generated by an internal fault, the XFAILB pin is asserted low 20 µs before starting the power-down sequence.

A power-down event caused by the following conditions will assert the XFAILB pin:

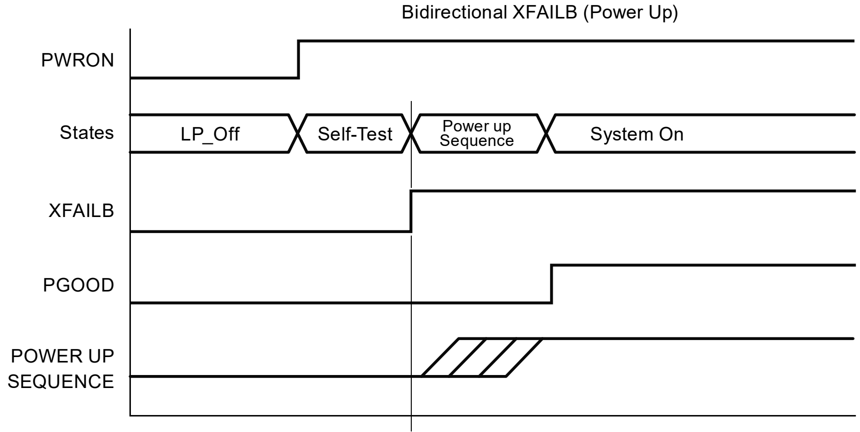
- FAULT_CNT = FAULT_MAX_CNT (Regulator fault counter max out)
- Power up failure
- Thermal shutdown
- PGOOD sense fail

The XFAILB pin is forced low during the Off mode.

During the system On state, if the XFAILB pin is externally pulled low, it will detect an XFAIL event after a 20 µs debounce. When an XFAIL event is detected, the XFAILB pin is asserted low internally and the device starts a power-down sequence.

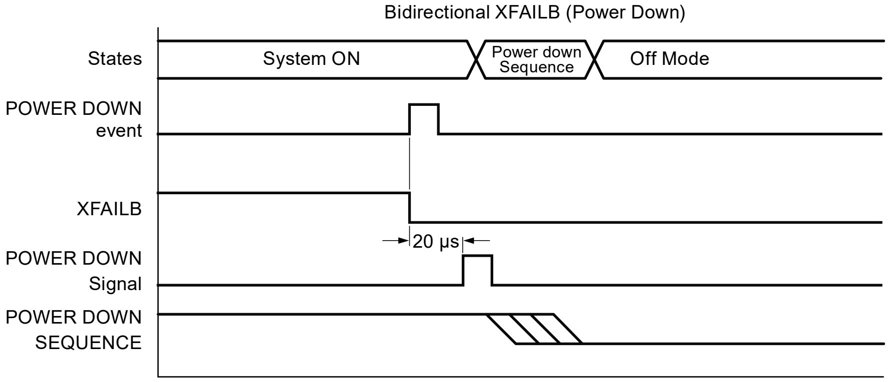
If a PWRON event is present, the device will start a turn-on event and proceed to release the XFAILB pin when it is ready to start the Power-up sequence state. If the XFAILB pin is pulled down externally during the power up event, the PF5103 will stop the Power-up sequence until the pin is no longer pulled down externally. This will help both PMICs to synchronize the Power-up sequence, allowing it to continue only when both PMICs are ready to initiate the Power-up sequence.

If the XFAILB is asserted low externally during the Power-up sequence (before PGOOD is released), the device detects a Power-up sequence failure after a 20 µs debounce, asserts its own XFAILB pin, and turns off all supplies immediately.



aaa-044570

Figure 23. XFAILB operation – power up



aaa-044571

Figure 24. XFAILB operation – power down

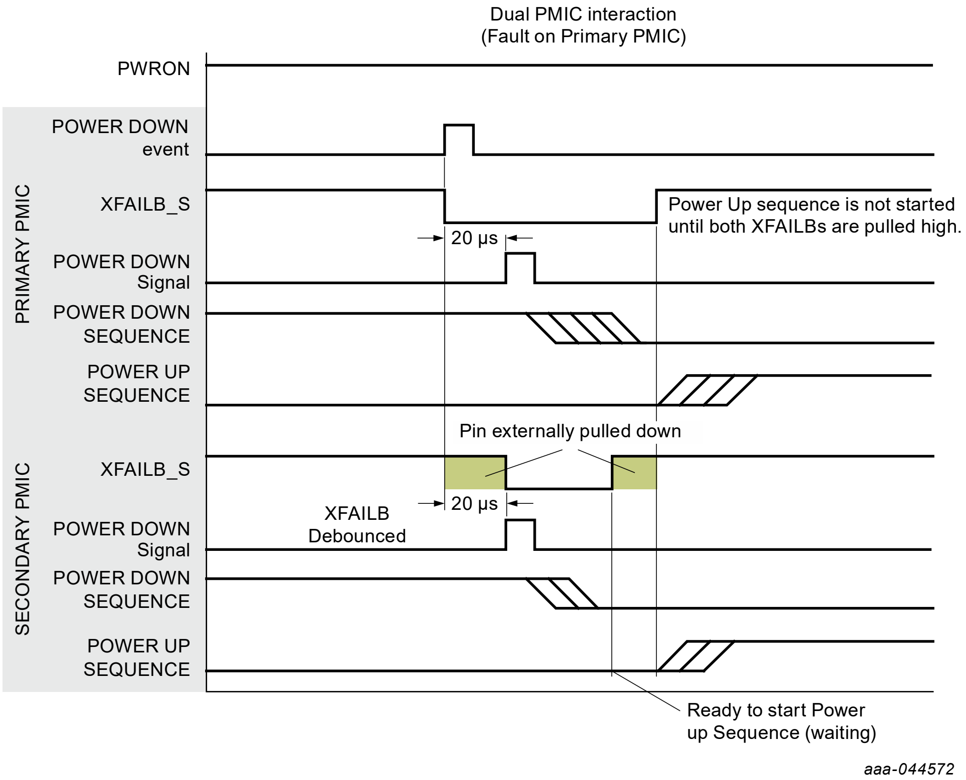


Figure 25. XFAILB operation – Multi-PMIC synchronization, Fault on primary PMIC

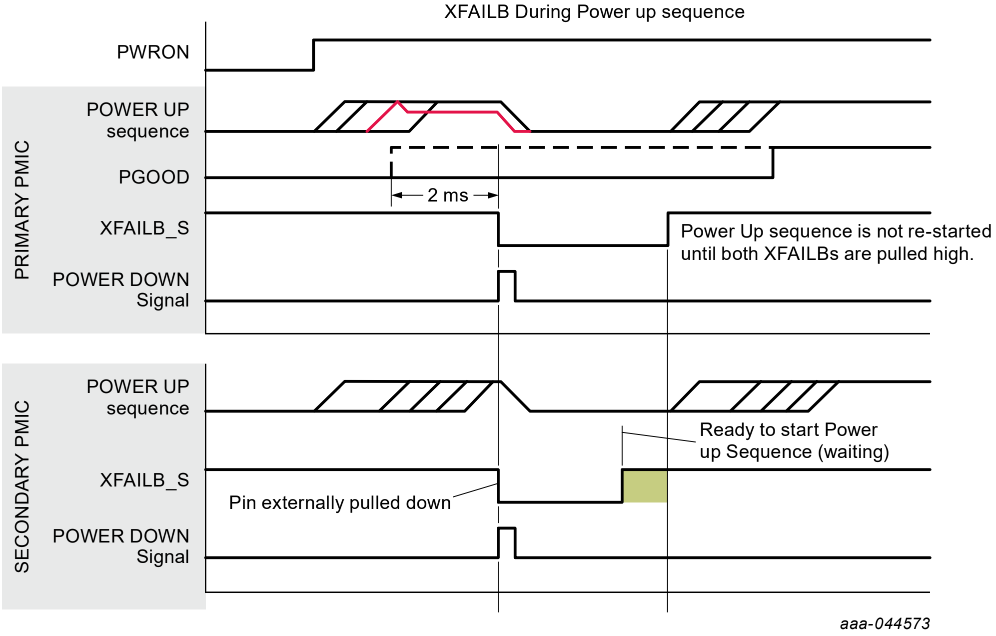


Figure 26. XFAILB operation – Multi-PMIC synchronization, Fault on primary PMIC

14.8.7 SDA and SCL (I^2C bus)

Communication with the PF5103 is done through I^2C and it supports high-speed operation mode with up to 3.4 MHz operation. SDA and SCL are pulled up externally to 1.8 V/3.3 V with 1.5 k Ω resistors to support operation up to the fast mode.

To use the high speed operation mode, a suitable pull up resistor must be used in the range of 500 Ω to 1 KΩ.

The PF5103 is designed to operate as a companion device during I^2C communication. The default I^2C device address is set by the OTP_I2C_ADD[2:0].

Table 37. I^2C address configuration

OTP_I2C_ADD[2:0]	Device address
000	0x08
001	0x09
010	0x0A
011	0x0B
100	0x0C
101	0x0D
110	0x0E
111	0x0F

During an I^2C transaction, the communication will latch after the eighth bit sent. If the data sent is not a multiple of 8 bits, any word with less than 8 bits will be ignored. If only 7 bits are sent, no data is written and the logic will not provide an ACK bit to the MCU.

From an IC level, an incorrect I^2C command can create a system level safety issue. For example, though the processor may have intended to set a given regulator's output to 1.0 V, it may be erroneously registered as 1.1 V due to noise in the bus.

To prevent an incorrect I^2C configuration, various protective mechanisms are implemented.

14.8.7.1 I^2C CRC verification

When this feature is enabled, a selectable CRC verification is performed on each I^2C transaction.

- When OTP_I2C_CRC_EN = 0, the CRC verification mechanism is disabled.
- When OTP_I2C_CRC_EN = 1, the CRC verification mechanism is enabled.

After each I^2C transaction, the device calculates the corresponding CRC byte to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the PF5103 ignores the erroneous configuration command and triggers a CRC_I interrupt, asserting the INTB pin, provided the interrupt is not masked.

The PF5103 implements a CRC-8-SAE, per the SAE J1850 specification.

- Polynomial = 0x11D
- Initial value = 0xFF

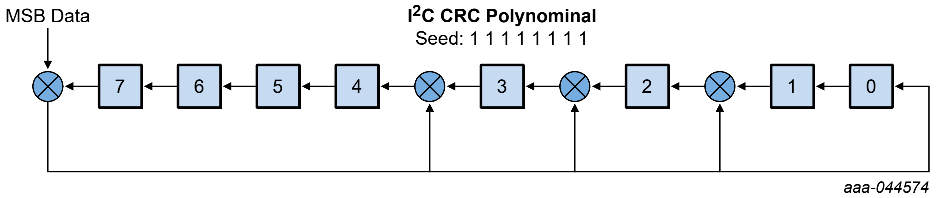


Figure 27. 8 bit SAE J1850 CRC polynomial

14.8.7.2 I^2C secure write

A secure write mechanism is implemented for specific registers critical to the functional safety of the device.

- When OTP_I2C_ SECURE_EN = 0, the secure write is disabled.
- When OTP_I2C_ SECURE_EN = 1, the secure write is enabled.

When the secure write is enabled, a specific sequence must be followed in order to grant writing access on the corresponding secure register.

The secure write sequence is as follows:

- Processor sends command to modify the secure registers
- PMIC generates a random code in the RANDOM_GEN register
- Processor reads the random code from the RANDOM_GEN register and writes it back on the RANDOM_CHK register

The PMIC compares the RANDOM_CHK against the RANDOM_GEN register:

- If RANDOM_CHK [7:0] = RANDOM_GEN[7:0], the device applies the configuration on the corresponding secure register, and self-clears both the RANDOM_GEN and RANDOM_CHK registers.
- If RANDOM_CHK[7:0] different from RANDOM_GEN[7:0], the device ignores the configuration command and self-clears both the RANDOM_GEN and RANDOM_CHK registers.

In the event the processor sends any other command instead of providing a value for the RANDOM_CHK register, the state machine cancels the ongoing secure write transaction and performs the new I^2C command.

In the event the processor does not provide a value for the RANDOM_CHK register, the I^2C transaction will time out 10 ms after the RANDOM_GEN code is generated, and the device is then ready for a new transaction.

Table 38. I^2C secure write bits

Register	Bit	Description
ABIST_OV1	AB_SWx_OV	Writing a 1 to this flag clears the ABIST fault
ABIST_UV1	AB_SWx_UV	Writing a 1 to this flag clears the ABIST fault
ABIST_CTRL	AB_RUN	Writing a 1 starts an ABIST routine on demand
CTRL1	TMP_MON_EN	Writing a 0 disables the thermal monitor, preventing the thermal interrupts and thermal shutdown event from being detected.
CTRL1	VIN_OVLO_EN	Writing a 0 disables the VIN overvoltage lockout monitor completely.

Table 38. I^{2}C secure write bits*...continued*

Register	Bit	Description
CTRL1	VIN_OVLO_SDWN	Writing a 0 disables a shutdown event upon a VIN overvoltage condition (only interrupts are provided)
CTRL1	WD_STBY_EN	Writing a 0 disables the watchdog timer during the Standby mode
CTRL1	I2C_SECURE_EN	Writing a 0 disables the I^{2}C secure write mode
VMONEN1	SWxVMON_EN	Writing a 0 disables the OV/UV monitor for SWx
VMONEN1	LDOxVMON_EN	Writing a 0 disables the OV/UV monitor for LDOx

14.8.7.3 Continuous CRC

The key bits in the I^{2}C functional registers will be continuously monitored for bit flips via the CRC (cyclic redundancy check) checker. The bits/registers in Section 16.3 and Section 16.1 are the bits/registers covered by the CRC checker. If a bit flip is detected, REGMAP_CRC_I is set and the device proceeds to the Fail-safe state (transition Q/W/H/Z of the state machine). The CRC is implemented per SAE J1850 (CRC-8-SAE) with polynimal = 0x11D and initial value=0xFF. The CRC checker runs during the Power-up sequence, IO release, INIT, RUN and Standby states.

.

15 Functional blocks

15.1 DC-DC buck regulators (SW1-SW3)

The PF5103 features four low voltage buck regulators with input supply range from UVDET to 5.5 V and output voltage range from 0.5 V to 3.3 V.

Each voltage regulator is capable of supplying 3.5 A and features a programmable soft-start and DVS ramp for system power optimization.

The OTP_SWxDVS_RAMP bit sets the default step/time ratio for the power up ramp during the power up/down sequence, as well as the DVS slope during the system On.

The power-down ramp and DVS rate during the system On of SW1 to SW3 can be modified during the system On state by changing the SWxDVS_RAMP bit on the I^2C register map.

The DVS ramp rate is based on the internal clock configuration as shown in Table 39.

Table 39. SWx ramp rates

All ramp rates are typical values at 2.5 MHz switching frequency. Clock frequency tolerance = ± 5 %.

CLK_ FREQ[3:0]	OSC frequency (MHz)	DVS_RAMP = 00		DVS_RAMP = 01		DVS_RAMP = 10		DVS_RAMP = 11	
		Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)
0000	20	7.8	7.8	15.6	15.6	3.9	3.9	1.95	1.95

Buck regulators SWx use 8 bits to set the output voltage. The VSWx_RUN[7:0] bits set the output voltage during Run mode. The default output voltage configuration for Run and Standby modes is loaded from the OTP_VSWx[7:0] registers upon power up.

Table 40. SWx output voltage configuration

Set point	VSWx_RUN[7:0] VSWx_STBY[7:0]	VSWxFB (V)
0	00000000	0.5000
1	00000001	0.6000
2	00000010	0.60625
3	00000011	0.61250
. .	. .	. .
119	01110111	1.33750
120	01111000	1.34375
121	01111001	1.3500
125	01111101	1.4500
127	01111111	1.5000
128	10000000	1.8000

Table 40. SWx output voltage configuration*...continued*

Set point	VSWx_RUN[7:0] VSWx_STBY[7:0]	VSWxFB (V)
129	10000001	1.8125
. .	. .	. .
184	10111000	2.5000
187	10111011	2.6000
192	11000000	2.8000
193	11000001	2.8250
. .	. .	. .
212	11010100	3.3000

DVS operation is available for all voltage settings between 0.6 V to 1.35 V.

Each regulator is provided with two bits to set its mode of operation.

To avoid potential detection of an OV/UV fault during SWx ramp up, it is recommended to power up the regulator in PWM or autoskip mode.

- The SWx_RUN_MODE[1:0] bits allow the user to change the mode of operation of the SWx regulators during the run state. If the regulator was programmed as part of the power up sequence, the SWx_RUN_MODE[1:0] bits are loaded with 0b10 (autoskip) by default. Otherwise it is loaded with 0b00 (disabled).
  The SWx_MODE_I interrupt asserts the INTB pin when any of the regulators have changed the mode of operation, provided the corresponding interrupt is not masked.
  To avoid potential detection of an OV/UV fault during SWx ramp up, it is recommended to power up the regulator in PWM or autoskip mode.

SWx regulators use two bits, SWxILIM[1:0], to program the current limit detection.

Table 41. SWx current limit selection

SWxILIM[1:0]	Typical current limit
00	Reserved
01	4.0 A
10	5.0 A
11	6.0 A

During single-phase operation, all buck regulators use three bits (SWxPHASE[2:0]) to control the phase shift of the switching frequency. Upon power up, the switching phase of all regulators is defaulted to 0 degrees and can be modified during the system On state.

Table 42. SWx phase configuration

SWx_PHASE[2:0]	Phase shift [defined by # of CLK cycles] (reference to the main high-frequency clock)
000	No phase shift
001	Shifted by 1 CLK
010	Shifted by 2 CLK

Table 42. SWx phase configuration...*continued*

SWx_PHASE[2:0]	Phase shift [defined by # of CLK cycles] (reference to the main high-frequency clock)
011	Shifted by 3 CLK
100	Shifted by 4 CLK
101	Reserved
110	Reserved
111	Reserved

Each one of the buck regulators provides two OTP bits to configure the value of the inductor used in the corresponding block. The OTP_SWx_LSELECT[1:0] allows a choice of inductors as shown in Table 43.

Table 43. SWx inductor selection bits

OTP_SWx_LSELECT[1:0]	Inductor value
00	0.22 µH
01	0.47 µH
10	Reserved
11	Reserved

The switching regulators integrate an internal pullup to VIN in the feedback pad, in order to properly detect an overvoltage condition upon a disconnection of the FB pin.

15.1.1 Multiphase operation

Regulators SW1, SW2, SW3 can be configured in multi-phase mode. In this mode, SW1 registers control the output voltage and other configurations. Likewise, the SW1FB pin becomes the main feedback node for the resulting voltage rail, however the two FB pins should be connected together.

The OTP_SW1CONFIG[1:0] bits are used to select the multiphase configuration for SW1/SW2/SW3.

Table 44. OTP_SW1CONFIG register description

OTP_SW4CONFIG[1:0]	Description
00	SW1, SW2 and SW3 operate in single phase mode
01	SW1/SW2 operate in dual phase mode
10	SW1/SW2/SW3 operate in triple phase mode
11	Reserved

15.1.2 Electrical characteristics

Table 45. Type 1 buck regulator electrical characteristics

All parameters are specified at T_A = −40 °C to 125 °C, V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
V_{SWxIN}	Operating functional input voltage	UVDET	—	5.5	V
V_{SWxIN_HDR}	Minimum headroom (V_{SWxIN}-V_{SWx}) For worst case at: I_{SWx} = 3.5 A V_{FBx} = 3.3 V T_a = 125 ℃	300	—	—	mV
V_{SWxACC}	Output voltage accuracy PWM mode 0.5 V < VSWxFB ≤ 3.3 V 0 ≤ ISWx ≤ 3.5 A	−1.5	—	1.5	%
$V_{SWxACCPFM}$	Output voltage accuracy PFM mode 0.5 V ≤ VSWxFB < 0.8 V 0 ≤ ISWx ≤ 100mA 2 MHz < Fsw < 3 MHz	-24	—	24	mV
$V_{SWxACCPFM}$	Output voltage accuracy PFM mode 0.8 V ≤ VSWxFB ≤ 3.3 V 0 ≤ ISWx ≤ 100 mA 2 MHz < Fsw < 3 MHz	−3.0	—	3.0	%
$V_{SWxACCPFMPWM}$	Output voltage accuracy PFM to PWM transition 0.5 V ≤ VSWxFB ≤ 3.3 V 0 ≤ ISWx ≤ 3.5A 2 Mhz < Fsw < 3 Mhz	-5	—	5	%
IQ_SWx	SWx regulator quiescent current, PFM Mode No switching operation	—	20	30	µA
I_{SWxLIM}	Current limit in single phase operation SWxILIM = 01	2.8	4.0	5	A
I_{SWxLIM}	Current limit in single phase operation SWxILIM = 10	3.8	5.0	6	A
I_{SWxLIM}	Current limit in single phase operation SWxILIM = 11	4.75	6.0	7	A
$I_{SWxNLIM}$	Negative current limit in single phase mode	1.8	2.5	3.52	A

Table 45. Type 1 buck regulator electrical characteristics*...continued*

All parameters are specified at T_A = −40 °C to 125 °C, V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
$I_{SWxxLIM\_DP}$	Current limit in dual phase operation SWxILIM = 01	5.6	8.0	10	A
$I_{SWxxLIM\_DP}$	Current limit in dual phase operation SWxILIM = 10	7.6	10	12	A
$I_{SWxxLIM\_DP}$	Current limit in dual phase operation SWxILIM = 11	9.5	12	14	A
$I_{SWxxLIM\_DP}$	Current limit in triple phase operation SWxILIM = 01	8.4	12	15	A
$I_{SWxxLIM\_DP}$	Current limit in triple phase operation SWxILIM = 10	11.4	15	18	A
$I_{SWxxLIM\_DP}$	Current limit in triple phase operation SWxILIM = 11	14.25	18	21	A
$V_{SWxLOTR\_s}$	Transient load regulation (overshoot/undershoot) in single phase 0.6 V ≤ VFBx ≤ 1.35 V Fsw = 2.5 MHz I_{STEP} = 200 mA to 1 A di/dt = 2 A/µs Cout ≥ 40 µF effective L = 0.47 µH Vin = 3.3 V	-25	—	25	mV
$V_{SWxLOTR\_D}$	Transient load regulation (overshoot/undershoot) in dual phase 0.6 V ≤ VFBx ≤ 1.35 V Fsw = 2.5 MHz I_{STEP} = 400 mA to 2 A di/dt = 4 A/µs Cout ≥ 40 µF effective L = 0.47 µH Vin = 3.3 V	-25	—	25	mV
$V_{SWxLOTR\_T}$	Transient load regulation (overshoot/undershoot) in triple phase 0.6 V ≤ VFBx ≤ 1.35 V Fsw = 2.5 MHz I_{STEP} = 600 mA to 3 A di/dt = 6 A/µs Cout ≥ 40 µF effective L = 0.47 µH Vin = 3.3 V	-25	—	25	mV

Table 45. Type 1 buck regulator electrical characteristics*...continued*

All parameters are specified at T_A = −40 °C to 125 °C, V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
$V_{SWxLOTR\_S4M}$	Transient load regulation (overshoot/undershoot) at 4 MHz 0.6 V ≤ VFBx ≤ 1.35 V Fsw = 4 MHz I_{STEP} = 200 mA to 1.0 A di/dt = 2 A/µs Cout ≥ 20 µF effective L = 0.22 µH, Vin = 3.3 V	-25	—	25	mV
$V_{SWxLOTR\_s}$	Transient load regulation (overshoot/undershoot) 1.8 V ≤ VFBx < 2.5 V Fsw = 2.5 MHz I_{STEP} = 200 mA to 1.0 A di/dt = 2 A/µs Cout ≥ 20 µF effective L = 0.47 µH Vin = 3.3 V	-3	—	3	%
$V_{SWxLOTR\_s}$	Transient load regulation (overshoot/undershoot) 2.8 V ≤ VFBx ≤ 3.3 V Fsw = 2.5 MHz I_{STEP} = 200 mA to 1.0 A di/dt = 2 A/µs Cout ≥ 20 µF effective L = 0.47 µH Vin > V_{SWxIN} min.	-50	—	50	mV
FSWx	PWM switching frequency range L = 0.47 µH L = 0.22 µH	 2 3.6	—	 3 4.4	MHz
DVSWx	Output ripple in PWM mode at V_{SWxIN} = 3.3 V, 2.5 MHz, VSWxFB = 0.8 V	—	—	5	mV
R_{SWxDIS}	Discharge resistance Regulator disabled and ramp down completed	—	50	—	Ω

[1] **For VSWx configurations greater than 1.35 V, full parametric operation is guaranteed for 2.7 V < SWxVIN < 5.5 V. Below 2.7 V, the SWx regulators are fully functional with degraded operation due to headroom limitation.**

[2] For VSWx = 1.8 V, output capacitance should be kept at or below the maximum recommended value. Likewise, it is recommended to use the slow turn on/off ramp rate to ensure the output is discharged completely when it is disabled.

Table 46. Recommended external components

Symbol	Parameter	Min	Typ	Max	Unit
L	Output inductor[1] Maximum inductor DC resistance: 20 mΩ Minimum saturation current at full load: 4.5 A • 2.2 MHz • 4 MHz[2]	— —	0.47 0.22	— —	μH
C_{out}	Output capacitor Use 2 × 22 μF, 6.3 V X7T ceramic capacitor to reduce output capacitance ESR	35	44	53	μF
C_{in}	Input capacitor 4.7 μF, 10 V X7R ceramic capacitor	4.23	4.7	—	μF

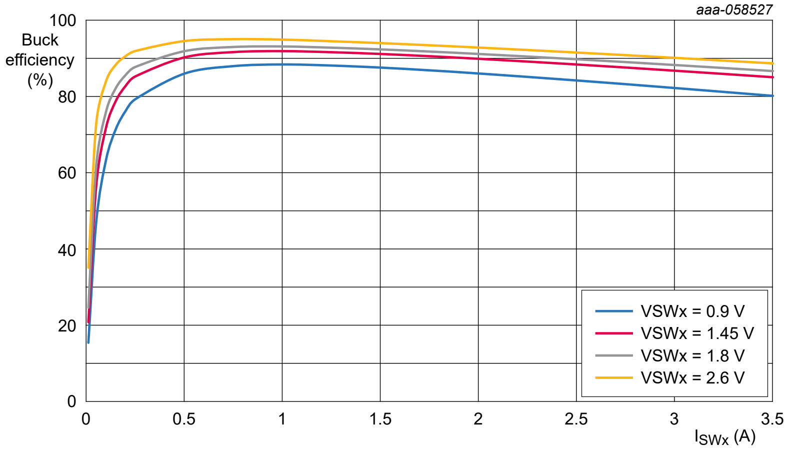
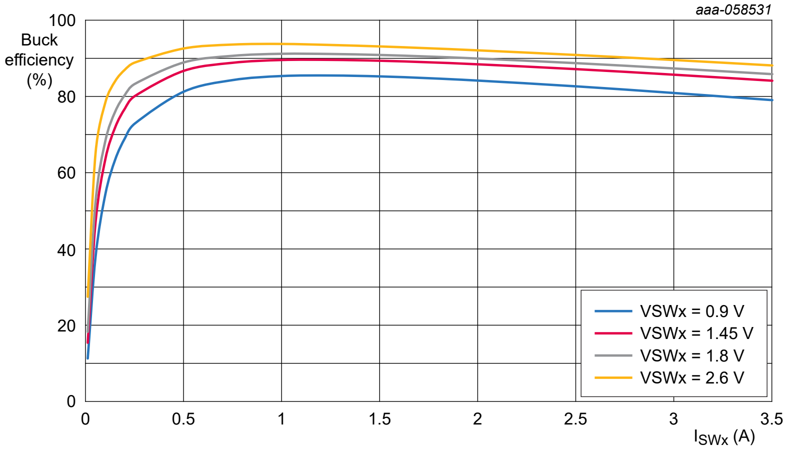
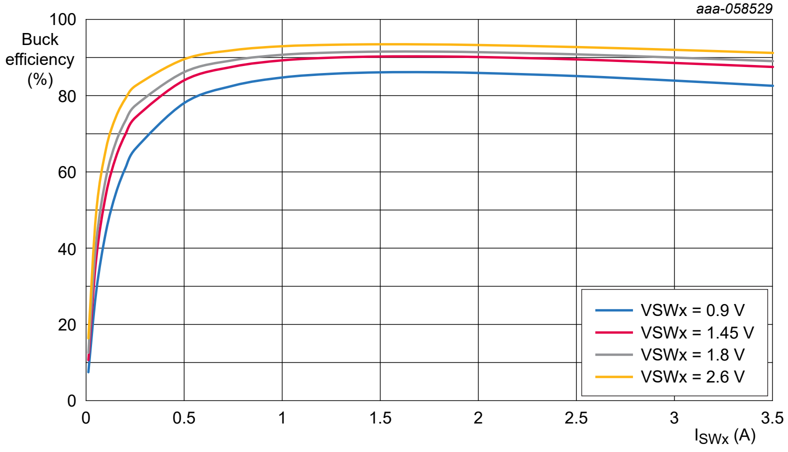
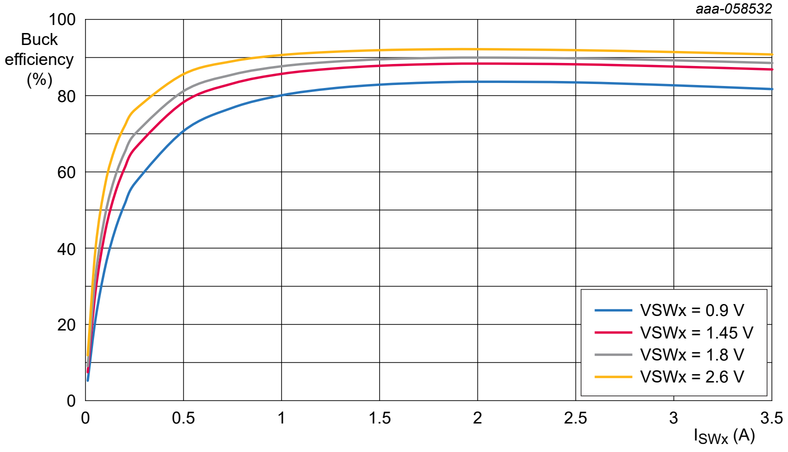
[1] Keep inductor DCR as low as possible to improve regulator efficiency. The inductor values in this table are sized for 3.5 A, which is the full current capability of each buck regulator.

[2] We can use 0.22 μH or 0.47 μH at 4 MHz, and only 0.47 μH at 2.2 Mhz. The value indicated in the table is the minimum recommended value for the full-load use case.

15.1.3 Efficiency performance

Low-voltage buck regulator performance is given based on the use of external components listed in Table 46.

Table 47. Buck efficiency vs. I_{SWx} at ambient temperature Ta = 25 ℃

	2.22 MHz	4 MHz
Vin = 3.3 V		
Vin = 5 V		

15.2 LDOx regulator

LDOx will support LDO mode or load switch, depending on the OTP_LDOxLS bit.

In all states where the LDOx is intended to remain disabled or when the output voltage is changed to a lower value which requires a discharge, the output of the regulator is pulled down internally with a 75 Ω pull down resistor.

LDOx uses 5 bits of OTP_VLDOx[4:0] to set the output voltage during the System On and INIT states. The default output voltage configuration for the System ON (VLDOx_RUN[4:0], VLDOx_STBY[4:0]) and INIT states (VLDOx_RUN[4:0]) is loaded from the OTP_VLDOx[4:0] registers upon power up.

Table 48. LDOx output voltage configuration

Set Point	OTP_VLDOx[4:0] VLDOx_RUN[4:0] VLDOx_STBY[4:0]	VLDOx (V)
0	00000	0.75
1	00001	0.8
2	00010	0.85
3	00011	0.9
4	00100	0.95
5	00101	1
6	00110	1.05
7	00111	1.1
8	01000	1.15
9	01001	1.2
10	01010	1.25
11	01011	1.3
12	01100	1.35
13	01101	1.4
14	01110	1.45
15	01111	1.5
16	10000	1.8
17	10001	1.9
18	10010	2
19	10011	2.1
20	10100	2.2
21	10101	2.3
22	10110	2.4
23	10111	2.5
24	11000	2.6
25	11001	2.7
26	11010	2.8

Table 48. LDOx output voltage configuration *...continued*

Set Point	OTP_VLDOx[4:0] VLDOx_RUN[4:0] VLDOx_STBY[4:0]	VLDOx (V)
27	11011	2.9
28	11100	3
29	11101	3.1
30	11110	3.2
31	11111	3.3

When the device toggles between Run and Standby states, the LDO output voltage will follow the setting in VLDOx_RUN or VLDOx_STBY registers.

LDO1 and LDO2 will be able to select the turn-on ramp speed using the OTP_LDOx_RAMP, LDOx_RAMP bits.

Table 49. LDO ramp speed selection

OTP_LDOx_RAMP	Description LDO ramp speed
0	Fast ramp - 180 µs
1	Slow ramp - 390 µs

15.2.1 LDO regulator electrical characteristics

Table 50. LDO regulator electrical characteristics

All parameters are specified at Ta = -40 °C to 125 °C, VLDOxIN = 2.7 to 5.5 V, VLDOx = 1.8 V, ILDO1 = 100 mA, typical external component values, unless otherwise noted. Typical values are characterized at VLDOxIN = 3.3 V, VLDOx = 1.8 V, ILDO1 = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
VLDOxIN	LDO1 operating input voltage range 0.75 V ≤ VLDOx < 2.25 V	2.5	—	5.5	V
VLDOxIN	LDO1 operating input voltage range 2.25 V < VLDOx < 3.3 V	VLDOx + 0.25	—	5.5	V

Table 50. LDO regulator electrical characteristics*...continued*

All parameters are specified at Ta = -40 °C to 125 °C, VLDOxIN = 2.7 to 5.5 V, VLDOx = 1.8 V, ILDO1 = 100 mA, typical external component values, unless otherwise noted. Typical values are characterized at VLDOxIN = 3.3 V, VLDOx = 1.8 V, ILDO1 = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
LDO1					
ILDO1	DC operating load current	0	—	200	mA
VLDOxTOL	Output voltage tolerance	-1.5	—	1.5	%
VLDO1LOR	Load regulation (0 mA-200 mA)	—	—	20	mV
ILDO1ILIM	Current limit ILDO1 when VLDO1 is forced to VLDO1 NOM/2	230	650	910	mA
ILDO1Q	Quiescent current (measured at TA = 25 °C)	—	14	20	uA
RDS(ON)	Load switch on resistance at VLDOINx = 3.3 V ILDOx=1 mA	—	340	500	mΩ
PSRRVLDO1	DC PSRR ILDO1 = 100 mA Cout = 4.7 uF	60	—	—	dB
tSS1_LDOx	LDOx Soft Start time • LDOx_RAMP = 1 • From 10 % to 90 % of final VOUT • VLDOxIN = 5.5 V • VLDOx = 3.3 V • RLoad = 20 Ω • COUT = 4.7 µF	190	390	650	µs
tSS0_LDOx	LDOx Soft Start time • LDOx_RAMP = 0 • From 10 % to 90 % of final VOUT • VLDOxIN = 3.3 V • VLDOx = 1.8 V • RLoad = 20 Ω • COUT = 4.7 µF	80	180	325	µs

Table 50. LDO regulator electrical characteristics*...continued*

All parameters are specified at Ta = -40 °C to 125 °C, VLDOxIN = 2.7 to 5.5 V, VLDOx = 1.8 V, ILDO1 = 100 mA, typical external component values, unless otherwise noted. Typical values are characterized at VLDOxIN = 3.3 V, VLDOx = 1.8 V, ILDO1 = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
tON1_LDOx	LDOx Turn-on time • LDOx_RAMP=1 • From Enable - to 90 % of final VOUT • VLDOxIN = 5.5 V • VLDOx = 3.3 V • RLoad = 20 Ω • COUT = 4.7 µF	—	—	1000	µs
tON0_LDOx	LDOx Turn on time • LDOx_RAMP=0 • From enable - to 90 % of final VOUT • VLDOxIN = 3.3 V • VLDOx = 1.8 V • RLoad = 20 Ω • COUT = 4.7 µF	—	—	500	µs
tOFFLDO1	Turn off time Disable to 10 % of initial value VLDO1 = 5.0 V ILDO1 = 0.0 mA	—	—	3500	µs
VLDO1IN_HDR	Minimum headroom (VLDO1IN-VLDO1) For worst case at: ILDO1 = 200 mA VLDO1=3.3 V Ta = 125 ℃ (In Load Switch mode)	150	—	—	mV
VLDO1OSHT	Startup overshoot VLDOINx = VLDOINxMIN VLDO1 = 5.0 V ILDO1 = 0.0 mA	—	1	2	%
VLDO1LOTR	Transient load response 1.8 V ≤ VLDO1 ≤ 3.3 V ILDO1 = 10 mA to 100 mA in 2.0 µs Peak of overshoot or undershoot of LDO1 with respect to final value	-5	—	5	%
TonLDO1LS	Load switch mode turn on rise time	—	150	300	µs
RdischLDO1	Output discharge resistance when LDO is disabled in load switch mode	—	100	300	Ω
Cout	Output capacitor X7R 6.3 V ceramic capacitor	—	4.7	—	µF
Cin	Input capacitor X7R 10 V ceramic capacitor	—	1	—	µF
LDO2					
ILDO2	DC operating load current	0	—	500	mA

Table 50. LDO regulator electrical characteristics*...continued*

All parameters are specified at Ta = -40 °C to 125 °C, VLDOxIN = 2.7 to 5.5 V, VLDOx = 1.8 V, ILDO1 = 100 mA, typical external component values, unless otherwise noted. Typical values are characterized at VLDOxIN = 3.3 V, VLDOx = 1.8 V, ILDO1 = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
VLDO2TOL	Output voltage tolerance	-1.5	—	1.5	%
VLDO2LOR	Load regulation (0 mA-500 mA)	—	—	20	mV
ILDO2ILIM	Current limit ILDO2 when VLDO2 is forced to VLDO2 NOM/2	540	1400	2100	mA
ILDO2Q	Quiescent current (measured at TA = 25 °C)	—	18	30	μA
RDS(ON)	Load Switch On resistance at VLDOINx = 3.3 V ILDOx=1 mA	—	170	250	mΩ
PSRRVLDO2	DC PSRR ILDO2 = 100 mA Cout = 4.7 uF	60	—	—	dB
tOFFLDO2	Turn off time Disable to 10% of initial value VLDO2 = 5.0 V ILDO1 = 0.0 mA	—	—	3500	μs
VLDO2IN_HDR	Minimum headroom (VLDO2IN - VLDO2) For worst case at: ILDO2 = 500 mA VLDO2=3.3 V Ta = 125 ℃	200	—	—	mV
VLDO2OSHT	Startup overshoot VLDOINx = VLDOINxMIN VLDO2 = 5.0 V ILDO2 = 0.0 mA	—	1	2	%
VLDO2LOTR	Transient load response 1.8 V ≤ VLDO1 ≤ 3.3 V ILDO2 = 10 mA to 200 mA in 2.0 μs Peak of overshoot or undershoot of LDO2 with respect to final value	-6	—	6	%
TonLDO2LS	Load switch mode turn on rise time	—	150	300	μs
RdischLDO2	Output discharge resistance when LDO is disabled in load switch mode	—	75	300	Ω

Table 51. Recommended external components

Symbol	Parameter	Min	Typ	Max	Unit
C_{out}	Output capacitor	—	4.7	—	μF
C_{in}	Input capacitor	—	1		μF

In all states where the LDOx is intended to remain disabled or when the output voltage is changed to a lower value which requires a discharge, the output of the regulator is pulled down internally with a 75 Ω pulldown resistor for 1000 µs. After the 1000 µs timer expires, the discharge/pulldown resistor is disabled and the LDO resumes normal operation with the new output voltage setting.

15.2.2 LDO pin open fault detection

An internal pullup resistor can be enabled or disabled by OTP in order to detect an open pin situation at the output of the LDOxOUT. The following table provides instructions for activating this feature:

Table 52. Detecting open pin at LDOxOUT output

OTP_LDOxOUT_OPEN	Description
0	Disabled
1	Enabled

When an overvoltage fault is detected due to an open at the LDOxOUT pin, the device has the same fault reaction as with a VMONx OV fault.

15.3 Voltage monitoring

The PF5103 provides OV and UV monitoring capability for the following voltage regulators:

- SW1
- SW2
- SW3
- LDO1
- LDO2
- VIN

A programmable UV threshold is selected via the OTP_SWxUV_TH[1:0], OTP_LDOxUV_TH[1:0] bits, and OTP_VINUV_TH[1:0] bits.

UV threshold selection represents a percentage of the nominal voltage programmed on each regulator.

Table 53. UV threshold configuration level specific to VIN

OTP_VINUV_TH	UV threshold level
00	96.75 %
01	96.25 %
10	95.75 %
11	95.25 %

Table 54. OV threshold configuration level specific to VIN

OTP_VINOV_TH	OV threshold level
00	103.25 %
01	103.75 %
10	104.25 %
11	104.75 %

Table 55. UV voltage threshold configuration register

OTP_SWxUV_TH[1:0] OTP_LDOxUV_TH[1:0]	UV threshold level
00	96.5 %
01	96 %
10	95.5 %
11	95 %

A programmable OV threshold will be selected via the OTP_SWxOV_TH[1:0], OTP_LDOxOV_TH[1:0] bits.

Table 56. OV threshold configuration register

OTP_SWxOV_TH[1:0] OTP_LDOxOV_TH[1:0]	OV threshold level
00	103.5 %
01	104 %
10	104.5%
11	105 %

Two functional bits are provided to program the UV debounce time for the voltage regulators.

Table 57. UV debounce timer configuration

UV_DB[1:0]	UV debounce time
00	5 μs
01	15 μs
10	30 μs
11	40 μs

The default value of the UV_DB[1:0] upon a full register reset is 0b10.

Two functional bits are used to program the OV debounce time for all the voltage regulators.

Table 58. OV debounce timer configuration

OV_DB[1:0]	OV debounce time
00	5 μs
01	15 μs
10	30 μs
11	40 μs

The default value of the OV_DB[1:0] upon a full register reset is 0b10.

The VMON_EN bits enable or disable the OV/UV monitor for each one of the regulators. (SWxVMON_EN, LDOxVMON_EN). When the VMON_EN bit of a specific regulator is 1, the voltage monitor for that specific block is enabled. When the VMON_EN bit of a specific regulator is 0, the voltage monitor for that specific block is disabled.

By default, the VMON_EN bits are set to 1 upon power up. The x_PG_EN bits enable or disable the PGOOD control for each one of the regulators. (SWx_PG_EN, LDOx_PG_EN). The x_PG_EN bits enable or disable the PGOOD control for each one of the regulators.(SWx_PG_EN, LDOx_PG_EN).

When the I2C_SECURE_EN = 1, a secure write is needed to clear the VMON_EN bits and disable the voltage monitoring for a specific block.

If a voltage monitor is disabled, the UV_S and OV_S indicators from that monitor will be reset to zero. When a regulator is enabled, it will monitor for an OV/UV condition. If the output of the regulator voltage meets the condition UV < VOUT < OV at the point of regulation, the output is considered to be within regulation.

When a regulator is enabled, its corresponding PG_S signal will be kept low until the output reaches the point of regulation. At this point, the device will monitor for an OV/UV condition before the PG_S signal can be released and be part of the AND function controlling the PGOOD pin, and the OV/UV monitor is ready to detect regulator faults.

For SWx, the point of regulation will be taken 40 µs after the last DVS code is sent by the logic. When a regulator is disabled, the OV/UV monitor is disabled at the same time as the corresponding regulator output.

The VIN voltage monitor is enabled when OTP_BGMON_SEL = 1. The VIN voltage monitor can only be used when the input voltage is 3.3 V. For input voltages higher than 3.3 V, VIN monitoring is not allowed while bandgap monitoring is still permitted (OTP_BGMON_SEL = 0).

15.3.1 VMON electrical characteristics

Table 59. VMON electrical characteristics

All parameters are specified at Tj = -40 °C to 150 °C, unless otherwise noted. Typical values are characterized at VIN = 3.3 V, VSWxFB = 1.0 V (Buck regulator), 3.3 V (LDOx), and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
I_{QON}	Block quiescent current, when block is enabled one block per regulator	—	17	30	µA
I_{OFF}	Block leakage current when disabled	—	—	450	nA
t_{ON_MON}	Voltage monitor settling time after enabled	—	—	30	µs

Table 59. VMON electrical characteristics...*continued*

All parameters are specified at Tj = -40 °C to 150 °C, unless otherwise noted. Typical values are characterized at VIN = 3.3 V, VSWxFB = 1.0 V (Buck regulator), 3.3 V (LDOx), and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{FBxUVHysteresis}$	Power good (UV) hysteresis Voltage difference between UV rising and falling thresholds	—	0.5	—	%
V_{UV_Tol}	Undervoltage falling threshold accuracy With respect to target feedback voltage tolerance For type 1 switching regulator when VSWxFB > 0.75 V	−1	—	1	%
V_{UV_Tol}	Undervoltage falling threshold accuracy With respect to target feedback voltage For type 1 switching regulator when VSWxFB ≤ 0.75 V	−1.5	—	1.5	%
t_{UV_DB}	Power good (UV) debounce time UV_DV = 00	2.5	5.0	7.5	µs
	Power good (UV) debounce time UV_DV = 01	10	15	20	
	Power good (UV) debounce time UV_DV = 10	20	30	40	
	Power good (UV) debounce time UV_DV = 11	25	40	55	
V_{OV_Tol}	Overvoltage rising threshold accuracy With respect to target feedback voltage tolerance For type 1 switching regulator when VSWxFB > 0.75 V	−1	—	1	%

Table 59. VMON electrical characteristics*...continued*

All parameters are specified at Tj = -40 °C to 150 °C, unless otherwise noted. Typical values are characterized at VIN = 3.3 V, VSWxFB = 1.0 V (Buck regulator), 3.3 V (LDOx), and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{OV_Tol}	Overvoltage rising threshold With respect to target feedback voltage tolerance For type 1 switching regulator when VSWxFB ≤ 0.75 V	−1.5	—	1.5	%
$V_{FBxOVHysteresis}$	Overvoltage (OV) hysteresis Voltage difference between OV rising and falling thresholds	—	0.5	—	%
t_{OV_DB}	Power good (OV) debounce time OV_DV = 00	2.5	5.0	7.5	µs
	Power good (OV) debounce time OV_DV = 01	10	15	20	
	Power good (OV) debounce time OV_DV = 10	20	30	40	
	Power good (OV) debounce time OV_DV = 11	25	40	55	

Note: *V_{UV_Tol} min expresses the difference between UV_TH typ and UV_TH min in percentage. V_{UV_Tol} max expresses the difference between UV_TH max and UV_TH typ in percentage. Regarding V_{OV_Tol}, the principle is respectively the same.*

15.4 Clock management

Clock management provides a top-level management control scheme of internal clock and external synchronization, intended to be primarily used for the switching regulators. Clock management incorporates various subblocks:

- Low power 100 kHz clock
- Internal high frequency clock with programmable frequency
- Phase-locked loop (PLL)

A digital clock management interface is in charge of supporting interaction among these blocks.

Clock management provides clocking signals for the internal state machine, the switching frequencies for the buck converters, as well as the multiples of those switching frequencies in order to enable phase shifting for multiple phase operation.

15.4.1 Low-frequency clock

A low-power 100 kHz clock is provided for overall logic and digital control. Internal logic and debounce timers are based on this 100 kHz clock.

15.4.2 High-frequency clock

The PF5103 features a high-frequency clock with a nominal frequency of 20 MHz. The clock frequency is programmable over a range of ±20 % via the CLK_FREQ[3:0] control bits.

15.4.3 Manual frequency tuning

PF5103 provides manual frequency tuning of the high speed oscillator to modulate the switching frequency. The CLK_FREQ [3:0] bits select manual frequency tuning of the high speed oscillator from 18 MHz to 22 MHz. If a frequency change of two or more steps is requested by a single I^2C command, the device performs a gradual frequency change, passing through all steps in between.

A FREQ_RDY_I interrupt is provided to indicate the frequency has reached the selected frequency. The OTP_CLK_DIVx[1:0] bits are used to select the default Switching frequency upon power up. The two clock outputs are used to provide the switching frequency for the Buck regulators.

Each switching regulator SWx uses either of the OTP_CLK_DIVx register outputs as the default switching frequency, based on the OTP_SWx_CLK bit.

Table 60. Output switching frequency

OTP_SWx_CLK	Description
0	CLK_DIV1
1	CLK_DIV2

Manual tuning is not available when frequency spread spectrum or external clock synchronization are used.

Table 61. Manual frequency tuning configuration

CLK_FREQ[3:0]	High speed clock frequency (MHz)
0000	20
0001	21
0010	22
0011	Not used
0100	Not used
0101	Not used
0110	Not used
0111	Not used
1000	Not used
1001	Not used
1010	Not used
1011	18
1100	19
1101	Not used

Table 61. Manual frequency tuning configuration*...continued*

CLK_FREQ[3:0]	High speed clock frequency (MHz)
1110	Not used
1111	Not used

Table 62. Clock divider configuration

OTP_CLK_ DIVx [1:0]	High speed oscillator frequency (MHz)	CLK DIV1 Ratio	Clock divider 1 output frequency (MHz)	CLK DIV2 Ratio	Clock divider 2 output frequency (MHz)
00	18	Divide by 5	3.6	Divide by 7	2.57
01	18	Reserved	Reserved	Divide by 8	2.25
10	18	Divide by 8	2.25	Divide by 9	2
11	18	Divide by 9	2	Reserved	Reserved
00	19	Divide by 5	3.8	Divide by 7	2.71
01	19	Reserved	Reserved	Divide by 8	2.38
10	19	Divide by 8	2.38	Divide by 9	2.11
11	19	Divide by 9	2.11	Reserved	Reserved
00	20	Divide by 5	4.00	Divide by 7	2.86
01	20	Reserved	Reserved	Divide by 8	2.50
10	20	Divide by 8	2.50	Divide by 9	2.22
11	20	Divide by 9	2.22	Reserved	Reserved
00	21	Divide by 5	4.2	Divide by 7	3
01	21	Reserved	Reserved	Divide by 8	2.63
10	21	Divide by 8	2.63	Divide by 9	2.33
11	21	Divide by 9	2.33	Reserved	Reserved
00	22	Divide by 5	4.4	Divide by 7	3.14
01	22	Reserved	Reserved	Divide by 8	2.75
10	22	Divide by 8	2.75	Divide by 9	2.44
11	22	Divide by 9	2.44	Reserved	Reserved

15.4.4 Phase-locked loop

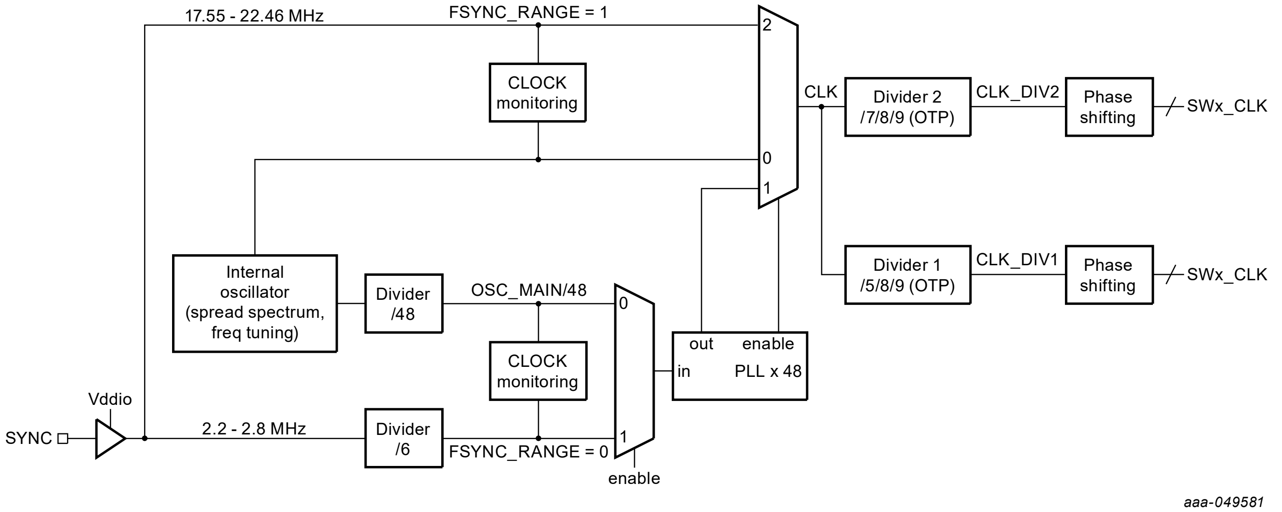


Figure 28. Phase-locked loop

15.4.5 Spread spectrum

The internal clock provides a programmable frequency spread spectrum with two ranges for narrow spread and wide spread to help manage EMC in the automotive applications.

- When the FSS_EN = 1, the frequency spread-spectrum is enabled.
- When the FSS_EN = 0, the frequency spread-spectrum is disabled.

The default state of the FSS_EN bit upon a power up can be configured via the OTP_FSS_EN bit.

The OTP_FSS_SEL bit is used to select the spread spectrum type.

Table 63. OTP_FSS_SEL bit

OTP_FSS_SEL	Description
0	Triangular modulation
1	Pseudo-random modulation

When FSS_SEL= 0, an OTP_FSS_FMOD bit is available to select the spread spectrum range and set the default setting of FSS_FMOD in the I^2C register map.

Table 64. OTP_FSS_FMOD bit

OTP_FSS_FMOD	Description
0	23.5 KHz
1	Reserved

When the triangular modulation type is selected, with FSS_SEL=0, there will be an absolute frequency deviation of +/-10 % with a step of 0.5 % around the CLK_FREQ frequency setting.

When the external clock synchronization is enabled, spread-spectrum is disabled.

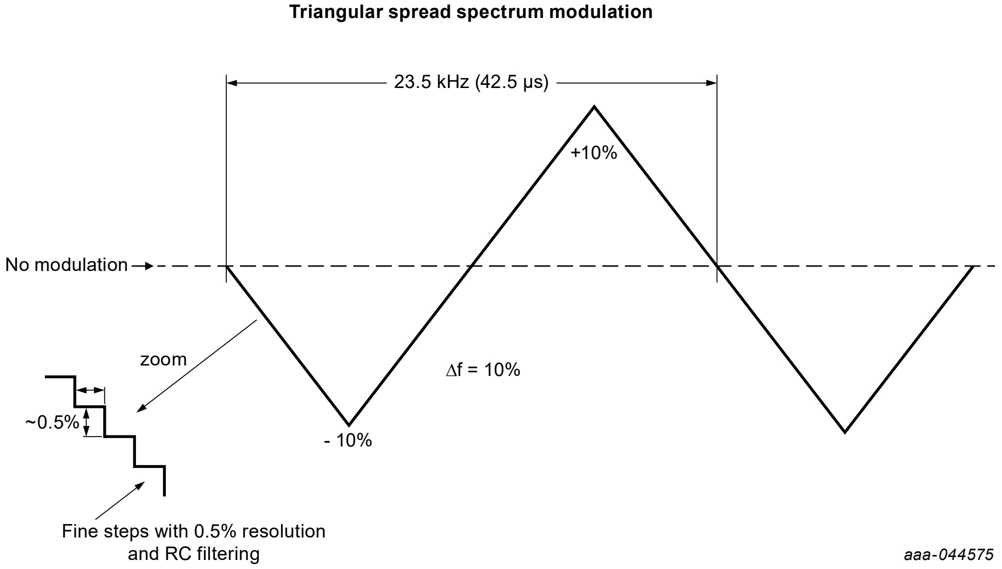


Figure 29. Triangular spread-spectrum modulation

When the pseudo-random modulation type is selected, with FSS_SEL= 1, the frequency will transition from 0 % to -10 %, through three random steps in between, and 0 % to +10 % through three random steps in between.

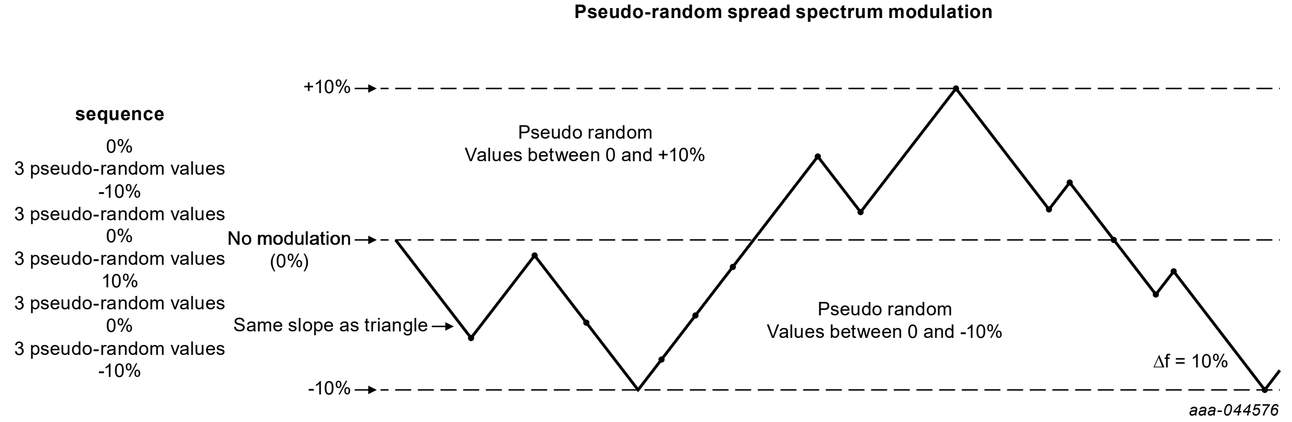


Figure 30. Pseudo-random spread-spectrum modulation

If the frequency spread-spectrum is enabled, the switching regulators should be set in PWM mode to ensure clock synchronization at all times.

If the external clock synchronization is enabled, the spread-spectrum is disabled regardless of the value of the FSS_EN bit.

15.4.6 Clock synchronization

An external clock can be fed via the SYNC pin to synchronize the switching regulators to this external clock. When OTP_SYNC_STBY = 0 and OTP_SYNC_EN = 1, the SYNC function is enabled. In this mode, the internal PLL is always on and can use either the internal high frequency oscillator or the SYNC pin as its source to generate the main frequency used for the switching regulators.

When the OTP_SYNC_EN = 0, the SYNC function is not enabled and the pin should be grounded.

The SYNC pin is compatible with 1.8 V or 3.3 V input signals. If the SYNCIN function is not used, the pin should be grounded. If the external clock is meant to start up after the PMIC has started, the SYNC pin must be maintained low until the external clock is applied.

The SYNC pin is prepared to detect clock signals with a 1.8 V or 3.3 V amplitude and within the frequency range set by the FSYNC_RANGE bit.

- When the FSYNC_RANGE = 0, the input frequency range at the SYNC pin is between 2200 kHz and 2800 kHz.
- When the FSYNC_RANGE = 1 the input frequency range at the SYNC pin is between 17.55 MHz and 22.46 MHz.
  The OTP_FSYNC_RANGE bit is used to select the default frequency range accepted in the SYNC pin.
  The external clock duty cycle at the SYNC pin should be between 40 % and 60 %. An input frequency in the SYNC pin outside the range defined by the FSYNC_RANGE bit is detected as invalid.
  If the external clock is not present or invalid, the device will automatically switch to the internal clock and set the FSYNC_FLT_I interrupt. The FSYNC_FLT_I is able to assert the INTB pin provided it is not masked. The FSYNC_FLT_S bit is set to 1 as long as the Frequency watchdog detects an invalid input frequency on the SYNC pin.
  The FSYNC_FLT_S bit is cleared to 0 as long as the Frequency watchdog detects a valid input frequency on the SYNC pin. The device switches back to the external switching frequency only when the FSYNC_FLT_I interrupt has been cleared and the Frequency watchdog is detecting a valid input frequency (FSYNC_FLT_S = 0).
  If the OTP_SYNC_EN = 0, both the FSYNC_FLT_I and the FSYNC_FLT_S bit are always set to 0. In SYNC mode, the switching regulators are set in PWM mode to ensure clock synchronization at all times.

Table 65. Clock management specifications

Symbol	Parameter	Min	Typ	Max	Unit
Low-frequency clock					
$I_{Q100KHz}$	100 kHz clock quiescent current	—	—	3.0	µA
$f_{100KHzACC}$	100 kHz clock accuracy	−5.0	—	5.0	%
High-frequency clock					
f_{20MHz}	High-frequency clock nominal frequency via CLK_FREQ[3:0] = 0000	—	20	—	MHz
$f_{20MzACC}$	High-frequency clock accuracy	-6.0	—	6.0	%
fosc1	High Frequency Oscillator Frequency CLK_FREQ[3:0]=0000	18.8	20	21.2	MHz
fosc2	High Frequency Oscillator Frequency CLK_FREQ[3:0]=0001	19.74	21	22.26	MHz
fosc3	High Frequency Oscillator Frequency CLK_FREQ[3:0]=0010	20.68	22	23.32	MHz
fosc4	High Frequency Oscillator Frequency CLK_FREQ[3:0]=1011	16.92	18	19.08	MHz
fosc5	High Frequency Oscillator Frequency CLK_FREQ[3:0]=1100	17.86	19	20.14	MHz
$t_{20MHzStep}$	Clock step transition time Minimum time to transition from one frequency step to the next in manual tuning mode	—	5.2	—	µs
FSS_{RANGE}	Spread-spectrum range Spread-spectrum is done around center frequency of CLK_FREQ[3:0]	—	±10.0	—	%
FSS_{mod}	Spread-spectrum frequency modulation	—	23.5	—	kHz
Clock synchronization					
FIN_RNG_LO1	FSYNC_RANGE=0 CLK_FREQ[3:0]=0000 Internal Clock : 20Mhz	2.45		2.54	Mhz
FIN_RNG_LO2	FSYNC_RANGE=0 CLK_FREQ[3:0]=0001 Internal Clock : 21Mhz	2.57		2.67	Mhz
FIN_RNG_LO3	FSYNC_RANGE=0 CLK_FREQ[3:0]=0010 Internal Clock : 22Mhz	2.7		2.8	Mhz
FIN_RNG_LO4	FSYNC_RANGE=0 CLK_FREQ[3:0]=1011 Internal Clock : 18Mhz	2.2		2.3	Mhz

Table 65. Clock management specifications*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
FIN_RNG_LO5	FSYNC_RANGE=0 CLK_FREQ[3:0]=1100 Internal Clock : 19Mhz	2.32		2.42	Mhz
FIN_RNG_HI1	FSYNC_RANGE=1 CLK_FREQ[3:0]=0000 Internal Clock : 20Mhz	19.51		20.41	Mhz
FIN_RNG_HI2	FSYNC_RANGE=1 CLK_FREQ[3:0]=0001 Internal Clock : 21Mhz	20.49		21.43	Mhz
FIN_RNG_HI3	FSYNC_RANGE=1 CLK_FREQ[3:0]=0010 Internal Clock : 22Mhz	21.46		22.46	Mhz
FIN_RNG_HI4	FSYNC_RANGE=1 CLK_FREQ[3:0]=1011 Internal Clock : 18Mhz	17.55		18.37	Mhz
FIN_RNG_HI5	FSYNC_RANGE=1 CLK_FREQ[3:0]=1100 Internal Clock : 19Mhz	18.54		19.39	Mhz

15.5 Thermal monitoring

The PF5103 features a temperature sensor at the center of the die which is used to generate the thermal interrupts and thermal shutdown.

The figure below shows a high-level block diagram of the thermal monitoring architecture in PF5103.

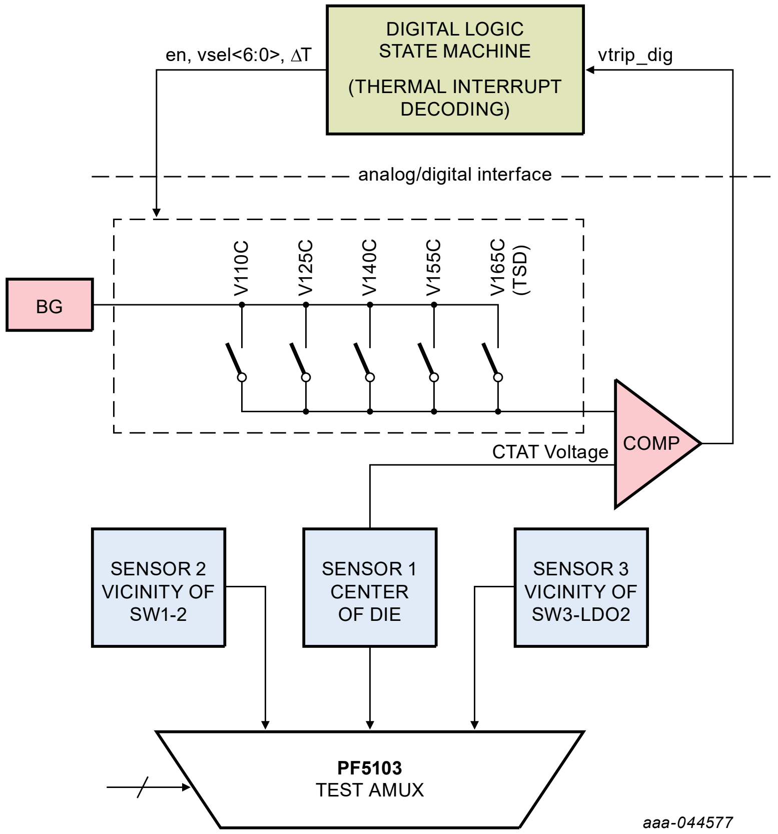


Figure 31. Thermal monitoring architecture

Table 66. Thermal monitor specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Operating voltage range of thermal circuit	UVDET	—	5.5	V
TCOF	Thermal sensor coefficient	—	-3.72	—	mV/ºC
V_{TSROMM}	Thermal sensor voltage 24 ºC	—	1.375	—	V
T_{SEN_RANGE}	Thermal sensor temperature range	–40	—	175	ºC
T_{110C}	110 ºC temperature threshold	100	110	120	ºC
T_{125C}	125 ºC temperature threshold	115	125	135	ºC
T_{140C}	140 ºC temperature threshold	130	140	150	ºC

Table 66. Thermal monitor specifications*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
T_{155C}	155 ºC temperature threshold	145	155	165	ºC
T_{SD}	Thermal shutdown threshold	155	165	175	ºC
T_{WARN_HYS}	Thermal threshold hysteresis	—	5.0	—	ºC
T_{SD_HYS}	Thermal shutdown hysteresis	—	10	—	ºC
$t_{Sinterval}$	Sampling interval time When TMP_MON_AON = 1	—	3	—	ms
$t_{Swindow}$	Sampling window When TMP_MON_AON = 1	—	380	—	µs

As the temperature crosses the thermal thresholds, the corresponding interrupts are set to notify the system. The processor may take appropriate action to bring down the temperature (either by turning off external regulators, reducing load, or turning on a fan).

A 5 ºC hysteresis is implemented on a falling temperature in order to release the corresponding THERM_x_S signal. When the shutdown threshold is crossed, the PF5103 initiates a thermal shutdown and it prolongs shutdown until the 15 ºC thermal shutdown hysteresis is crossed as the device cools down.

The temperature monitor can be enabled or disabled via I^2C with the TMP_MON_EN bit.

- When TMP_MON_EN = 0, the temperature monitor circuit is disabled.
- When TMP_MON_EN = 1, the temperature monitor circuit is enabled.

In the Run state, the temperature sensor can operate in always On or Sampling modes.

- When the TMP_MON_AON = 1, the device is always on during the Run mode.
- When the TMP_MON_AON = 0, the device operates in sampling mode to reduce current consumption in the system. In Sampling mode, the thermal monitor is turned on for 450 µs at a 3.0 ms sampling interval.

In the Standby mode, the thermal monitor operates only in sampling mode as long as the TMP_MON_EN = 1.

Table 67. Thermal monitor bit description

Bit(s)	Description
THERM_110_I, THERM_110_S, THERM_110_M	Interrupt, sense and mask bits for 110 ºC threshold
THERM_125_I, THERM_125_S, THERM_125_M	Interrupt, sense and mask bits for 125 ºC threshold
THERM_140_I, THERM_140_S, THERM_140_M	Interrupt, sense and mask bits for 140 ºC threshold
THERM_155_I, THERM_155_S, THERM_155_M	Interrupt, sense and mask bits for 155 ºC threshold
TMP_MON_EN	Disables temperature monitoring circuits when cleared
TMP_MON_AON	When set, the temperature monitoring circuit is always ON. When cleared, the temperature monitor operates in Sampling mode.

15.6 Analog multiplexer

An analog multiplexer (AMUX) is provided to allow access to the internal temperature monitor. The selected voltage is buffered and made available on the PGOOD1 output pin.

When the AMUX_EN bit is 0, the AMUX block is disabled and the PGOOD block is enabled.

When the AMUX_EN bit is 1, the AMUX block is enabled and the PGOOD block is disabled. The system can select the channel to be read using the AMUX_SEL bits. The AMUX output is selected by the AMUX_SEL[4:0] bits.

Table 68. AMUX channel selection

AMUX_EN	AMUX_SEL[4:0]	AMUX selection
0	XXXXX	PGOOD mode
1	00000	Disabled - high impedance
1	00001 to 10110	Reserved
1	10111	TEMP_IC
1	11000 to 11111	Reserved

When the AMUX_EN = 1, and the AMUX_SEL = 00000, the AMUX output is set to a high impedance mode to allow an external signal to drive the AMUX node. The AMUX is enabled and accessible during the system ON states.

15.7 Watchdog event management

A watchdog event is triggered by one of the following events:

- The watchdog refresh doesn’t happen for more than 2 seconds after entering the INIT state, due to a watchdog failure on the processor
- The internal watchdog error counter reaches the maximum value

A watchdog event initiated by one of the two events above will assert PGOOD low for 2 ms and the state machine will transition to the I/O Release state.

15.7.1 Internal watchdog timer

The OTP_WD_EN bit selects whether the watchdog timer is active by default or not. The internal WD timer counts up, and it expires when it reaches the value in the WD_DURATION[3:0] register. Upon power up, after PGOOD is de-asserted and the state machine reaches the INIT state, a 2 second window becomes active during which a good WD refresh is expected from the processor. A good WD refresh from the processor during the INIT state is required to close the 2 second window and to continue to the system ON states.

When the WD timer starts counting, the WD_ANSWER register must be written with the correct value within the correct window. The WD timer is reset when device goes into any of the Off modes. The correct WD_ANSWER value will be based on the value in the WD_SEED register and the watchdog type selected with the OTP_WD_SEL bit. The WD_SEED register, by default, contains the seed value of 0x5B always when OTP_WD_SEL=0 (Simple WD).

The OTP_WD_DURATION[3:0] selects the initial configuration for the watchdog window duration between 1 ms and 32768 ms (typical values). The Watchdog window duration can be changed during the INIT and System On states by modifying the WD_DURATION[3:0] bits on the functional register map. If the WD_DURATION[3:0] bits get changed during the INIT and System On states, the WD Timer is reset.

Table 69. Watchdog duration selection

WD_DURATION[3:0]	Watchdog timer duration (ms)
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

The WD_ERROR_CNT[3:0] counter is used to ensure no cyclic watchdog condition occurs.

Table 70. Watchdog error counter

WD_ERROR_CNT[3:0]	Watchdog error count
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8

The OTP_WDWINDOW bit selects whether the watchdog is singled-ended or Window mode. When OTP_WDWINDOW = 0, the WD_ANSWER can be written within 100% of the watchdog timer. When OTP_WDWINDOW = 1, the WD_ANSWER can only be written within the second half of the programmed watchdog timer. If the OTP_WDWINDOW =1, writing to the WD_ANSWER register within the first half of the watchdog window is interpreted as a bad watchdog refresh.

When the WD_ANSWER is written successfully before the WD Timer expires, the WD_ERROR_CNT[3:0] is decreased by 1. When the processor fails to write to the WD_ANSWER register, the WD_ERROR_CNT[3:0] is increased by 2.

When the processor fails to write to the WD_ANSWER register within the correct window or if it writes a wrong answer within the window, or writes a correct answer in the wrong window, the WD_ERROR_CNT[3:0] is increased by 2.

If WD_ERROR_CNT[3:0] ≥ WD_MAX_ERROR[1:0], a WD event is initiated. Upon Power up, The WD_MAX_ERROR[1:0] is loaded with the value on the OTP_WD_MAX_ERROR[1:0] bits. The minimum value allowed in the OTP_WD_MAX_ERROR[1:0] bits is 0x02.

Table 71. WD_MAX_ERROR

WD_MAX_ERROR[1:0]	Watchdog error maximum value
00	8
01	6
10	4
11 (Reset)	**2 (Default)**

When the user writes the WD_MAX_ERROR with a value less or equal to 0x02, a watchdog event is initiated immediately after the first WD error. The WD_ERROR_CNT[3:0] is reset to 0 when the device enters the LP_Off state.

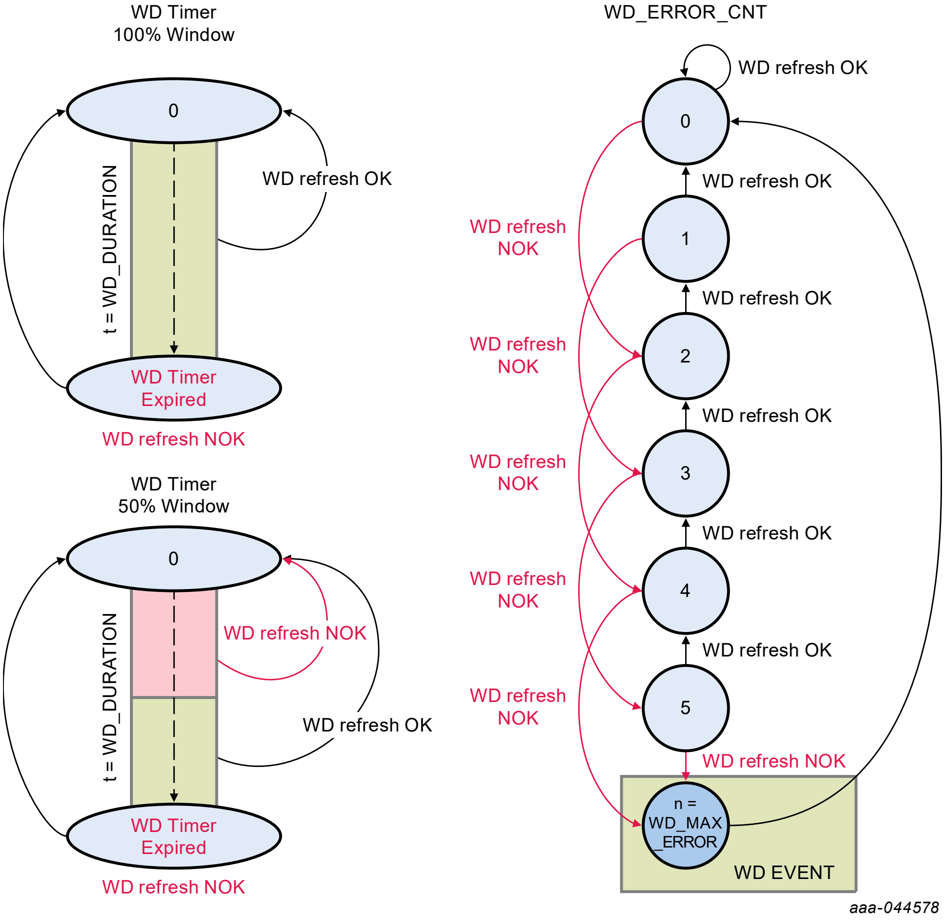


Figure 32. Watchdog timer and error counter

The watchdog timer can also be enabled or disabled by writing the WD_EN bit on the I^{2}C register map. OTP_WD_EN defines the state of the watchdog after boot up. It is possible to activate the watchdog through I^{2}C by writing WD_EN = 1 even if OTP_WD_EN = 0.

When WD_EN=0, the internal watchdog timer operation is disabled.

When WD_EN=1, the internal watchdog timer operation is enabled.

When the I2C_SECURE_EN = 1, a Secure Write is needed to change the WD_EN bit. The OTP_WD_STBY_EN bit selects whether the watchdog is active in Standby mode by default or not. The watchdog function can be programmed to be enabled or disabled during the Standby state by writing the WD_STBY_EN bit on the I^2C register map when OTP_WD_STBY_EN=1.

When WD_STBY_EN = 0 the Internal watchdog timer operation during Standby is disabled. When WD_STBY_EN = 1 the Internal watchdog timer operation during Standby is enabled. When the I2C_SECURE_EN = 1, a Secure Write is needed to modify the WD_STBY_EN bit.

Refer to section Section 14.8.7.2 for a detailed description of the secure write feature.

When a watchdog (WD) event happens, the fault counter FAULT_CNT[3:0] is incremented by 1, and PGOOD will be asserted if it is programmed to do so.

A WD event keeps the PGOOD asserted all the time until it is safe to release the PGOOD again.

15.7.2 Fault recovery

An extended watchdog function is included in the PMIC in case a processor recovery is needed during an FCCU fault. The watchdog recovery feature is enabled using the OTP_WD_FAULT_REC bit. This functionality extends the watchdog window to allow the MCU to perform a fault recovery strategy. The goal is to prevent the MCU from being reset while it is trying to recover the application after a failure event.

The FCCU fault recovery bit using the watchdog is described in Table 72:

Table 72. Fault recovery bit for watchdog

OTP_WD_FAULT_REC	Watchdog fault recovery
0	Disabled
1	Enabled

With the fault recovery mode enabled, when a fault is trigged by the processor via its FCCUx pins, the fault counter is incremented and the WD window duration automatically becomes an open window (no more duty cycle).

This open window duration is configurable by the processor during the INIT and System On states using the WDW_RECOVERY[3:0] bits.

It is not be possible to modify the WDW_RECOVERY[3:0] bits when the FCCU fault recovery is active.

Table 73. Watchdog window duration (configurable using the WDW_RECOVERY[3:0] bits)

WDW_RECOVERY[3:0]	Watchdog open window duration during fault recovery duration (ms)
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110 (Reset)	**64 (default)**
0111	128
1000	256
1001	512

Table 73. Watchdog window duration (configurable using the WDW_RECOVERY[3:0] bits)*...continued*

WDW_RECOVERY[3:0]	Watchdog open window duration during fault recovery duration (ms)
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

The transition from WD_DURATION to WDW_RECOVERY happens when the FCCUx pins indicate an error and the fault counter is incremented.

If the processor sends a good watchdog refresh before the end of the WDW_RECOVERY duration, the device switches back to the WD_DURATION timer and associated duty cycle if the FCCUx pins no longer indicate an error. Otherwise, a new WDW_RECOVERY period is started.

If the processor does not send a good watchdog refresh before the end of the WDW_RECOVERY duration, then a PGOOD pulse is generated, the state machine moves to the I/O release state, and eventually to the INIT state, where the WD duration resumes again.

Figure 33 illustrates the recovery mechanism:

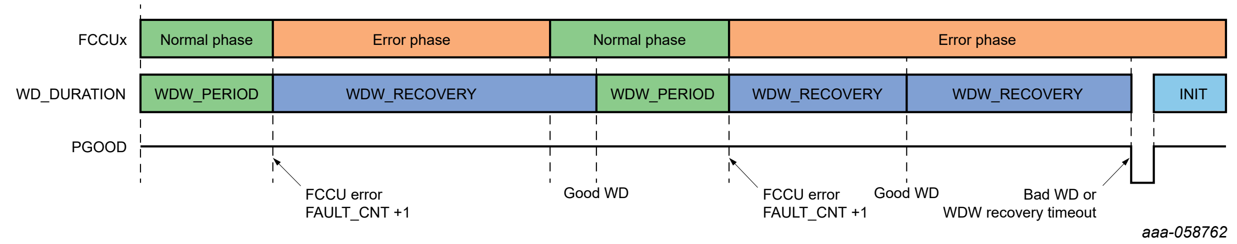


Figure 33. Fault recovery mechanism

16 I²C register map

The PF5103 provides a complete set of registers for control and diagnostics of the PMIC operation. The configuration of the device is done at two different levels.

At the first level, the OTP mirror registers provide the default hardware and software configuration for the PMIC upon power up.

At the second level, the PF5103 provides a set of functional registers intended for system configuration and diagnostics during the system operation. These registers are accessible during the system On state and can be modified at any time by the system control unit.

The device ID register (Address 0x00) provides general information about the PMIC:

- DEVICE_FAM[3:0]: indicates the PF510x family of devices = 0b0111 (fixed)
- DEVICE_ID[3:0]: provides the device type identifier for each device in the family = 0b0011 (PF5103)

The following customizable program ID registers can be use to identify the OTP configuration to be programmed in the part.

- PROG_ID (Address 0x02): contains the PROG_ID_H and the two MSBs of PROG_ID_L
- PROG_ID_REV (Address 0x03): contain the 4 LSBs of PROG_ID_L and PROG_ID_REV

16.1 PF5103 OTP mirror register map

Table 74. OTP mirror register map

ADDR	Register Name	R/W	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
3F	OTP_I2C	RW	0000_0000	—	—	—	**OTP_I2C_SECURE_EN**	**OTP_I2C_CRC_EN**	OTP_I2C_ADD[2:0]		
40	OTP_CTRL1	RW	0000_0000	—	—	—	—	OTP_LP_STBY	OTP_STANDBYINV	OTP_INTB_RSTB	OTP_XFAILB_EN
41	OTP_CTRL2	RW	0000_0000	**OTP_VINUV_TH[1:0]**		**OTP_VINOV_TH[1:0]**		OTP_VIN_OVLO_SDWN	OTP_VIN_OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
42	OTP_CTRL3	RW	0000_0000	—	OTP_PD_SEQ_DLY[2:0]			—		OTP_SW1CONFIG[1:0]	
43	OTP_FREQ_CTRL1	RW	0000_0000	OTP_SW_MODE	OTP_SYNC_EN	—	OTP_FSYNC_RANGE	OTP_CLK_FREQ[3:0]			
44	OTP_FREQ_CTRL2	RW	0000_0000	OTP_FSS_EN	OTP_FSS_FMOD	OTP_FSS_SEL	—	OTP_CLK_DIV2[1:0]		OTP_CLK_DIV1[1:0]	
45	OTP_WD_CONFIG	RW	0000_0000	OTP_WD_DURATION[3:0]				OTP_WD_EN	OTP_WD_STBY_EN	OTP_WD_SEL	OTP_WDWINDOW
46	OTP_WD_FLT_EXPIRE	RW	0000_0000	—	**OTP_FAULT_MAX_CNT[2:0]**			—	—	OTP_WD_MAX_ERROR[1:0]	
47	OTP_PWRUP_CTRL	RW	0000_0000	OTP_PGOOD_SEQ[5:0]						OTP_SEQ_TBASE[1:0]	
48	OTP_FSO_GPO_CTRL	RW	0000_0000	OTP_GPO_SEQ[5:0]						—	—
49	OTP_SW1_VOLT	RW	0000_0000	OTP_VSW1[7:0]							
4A	OTP_SW1_PWRUP	RW	0000_0000	—	—	OTP_SW1_SEQ[5:0]					
4B	OTP_SW1_CONFIG1	RW	0000_0000	**OTP_SW1_UV_TH[1:0]**		**OTP_SW1_OV_TH[1:0]**		—	—	OTP_SW1ILIM[1:0]	
4C	OTP_SW1_CONFIG2	RW	0000_0000	OTP_SW1_LSELECT[1:0]		OTP_SW1PHASE[2:0]			OTP_SW1_STBY_EN	**OTP_SW1_PG_EN**	OTP_SW1_CLK
4D	OTP_SW2_VOLT	RW	0000_0000	OTP_VSW2[7:0]							
4E	OTP_SW2_PWRUP	RW	0000_0000	—	—	OTP_SW2_SEQ[5:0]					
4F	OTP_SW2_CONFIG1	RW	0000_0000	**OTP_SW2_UV_TH[1:0]**		**OTP_SW2_OV_TH[1:0]**		—	—	OTP_SW2ILIM[1:0]	
50	OTP_SW2_CONFIG2	RW	0000_0000	OTP_SW2_LSELECT[1:0]		OTP_SW2PHASE[2:0]			OTP_SW2_STBY_EN	**OTP_SW2_PG_EN**	OTP_SW2_CLK
51	OTP_SW3_VOLT	RW	0000_0000	OTP_VSW3[7:0]							
52	OTP_SW3_PWRUP	RW	0000_0000	—	—	OTP_SW3_SEQ[5:0]					

Table 74. OTP mirror register map*...continued*

ADDR	Register Name	R/W	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
53	OTP_SW3_CONFIG1	RW	0000_0000	**OTP_SW3_UV_TH[1:0]**		**OTP_SW3_OV_TH[1:0]**		—	—	OTP_SW3ILIM[1:0]	
54	OTP_SW3_CONFIG2	RW	0000_0000	OTP_SW3_LSELECT[1:0]		OTP_SW3PHASE[2:0]			OTP_SW3_STBY_EN	**OTP_SW3_PG_EN**	OTP_SW3_CLK
5D	OTP_LDO1_VOLT	RW	0000_0000		—	—	RESERVEDOTP_VLDO1[4:0]				
5E	OTP_LDO1_PWRUP	RW	0000_0000	—	—	RESERVEDOTP_LDO1_SEQ[5:0]					
5F	OTP_LDO1_CONFIG	RW	0000_0000	**OTP_LDO1UV_TH[1:0]**		**OTP_LDO1OV_TH[1:0]**		OTP_LDO1_STBY_EN	**OTP_LDO1_PG_EN**	OTP_LDO1_RAMP	OTP_LDO1LS
60	OTP_LDO2_VOLT	RW	0000_0000	—	—	—	OTP_VLDO2[4:0]				
61	OTP_LDO2_PWRUP	RW	0000_0000	—	—	OTP_LDO2_SEQ[5:0]					
62	OTP_LDO2_CONFIG	RW	0000_0000	**OTP_LDO2UV_TH[1:0]**		**OTP_LDO2OV_TH[1:0]**		OTP_LDO2_STBY_EN	**OTP_LDO2_PG_EN**	OTP_LDO2_RAMP	OTP_LDO2LS
63	OTP_OV_BYPASS	RW	0000_0000	—	OTP_LDO2_OV_BYPASS	OTP_LDO1_OV_BYPASS	—	—	OTP_SW3_OV_BYPASS	OTP_SW2_OV_BYPASS	OTP_SW1_OV_BYPASS
64	OTP_UV_BYPASS	RW	0000_0000	—	OTP_LDO2_UV_BYPASS	OTP_LDO1_UV_BYPASS	—	—	OTP_SW3_UV_BYPASS	OTP_SW2_UV_BYPASS	OTP_SW1_UV_BYPASS
65	OTP_ILIM_BYPASS	RW	0000_0000	—	OTP_LDO2_ILIM_BYPASS	OTP_LDO1_ILIM_BYPASS	—	—	OTP_SW3_ILIM_BYPASS	OTP_SW2_ILIM_BYPASS	OTP_SW1_ILIM_BYPASS
66	OTP_ID_2	RW	0000_0000	OTP_ID_REV[3:0]				OTP_ID_H[3:0]			
67	OTP_ID_1	RW	0000_0000	—	—	OTP_ID_L[5:0]					
68	OTP_SW_COMP1	RW	0000_0000	—		OTP_SW2_GM_COMP[2:0]			OTP_SW1_GM_COMP[2:0]		
69	OTP_SW_COMP2	RW	0000_0000	—	—	—			OTP_SW3_GM_COMP[2:0]		
6A	OTP_SW_COMP3	RW	0000_0000	OTP_SW2_C_COMP[1:0]		OTP_SW2_R_COMP[1:0]		OTP_SW1_C_COMP[1:0]		OTP_SW1_R_COMP[1:0]	
6B	OTP_SW_COMP4	RW	0000_0000	—		—		OTP_SW3_C_COMP[1:0]		OTP_SW3_R_COMP[1:0]	
6C	OTP_SW_RAMP	RW	0000_0000	—		OTP_SW3DVS_RAMP[1:0]		OTP_SW2DVS_RAMP[1:0]		OTP_SW1DVS_RAMP[1:0]	
6D	OTP_ASIL_CONFIG	RW	0000_0000	OTP_BGMON_SEL	**OTP_LDOxOUT_OPEN**	**OTP_BGMON_BYPASS**	OTP_FS_BYPASS_CNT	**OTP_FS_BYPASS**	OTP_SYNC_STBY	OTP_WD_FAULT_REC	**OTP_FCCU_EN**
6E	OTP_S2_CRC_LSB	RW	0000_0000	OTP_S2_CRC_LSB[7:0]							
6F	OTP_S2_CRC_MSB	RW	0000_0000	OTP_S2_CRC_MSB[7:0]							

Note: *OTP bits in bold with continuous CRC check.*

16.2 OTP registers

16.2.1 OTP_I2C

Table 75. OTP_I2C – OTP I2C register (address 3Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	OTP_I2C_ SECURE_EN	OTP_I2C_ CRC_EN	OTP_I2C_ADD[2:0]		
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RW	RW	RW	RW	R

Table 76. OTP_I2C – OTP I2C register (address 3Fh) bit description

Bit	Symbol	Description	
4	OTP_I2C_ SECURE_EN	I^{2}C Secure Write config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
3	OTP_I2C_CRC_EN	I^{2}C CRC verification config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
2 to 0	OTP_I2C_ADD[2:0]	I^{2}C address	
		3b'000	Address 0h8
		3b'001	Address 0h9
		3b'010	Address 0hA
		3b'011	Address 0hB
		3b'100	Address 0hC
		3b'101	Address 0hD
		3b'110	Address 0hE
		3b'111	Address 0hF
		Default condition	000

16.2.2 OTP_CTRL1

Table 77. OTP_CTRL1 – OTP control 1 register (address 40h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	OTP_LP_STBY	OTP_ STANDBYINV	OTP_INTB_ RSTB	OTP_ XFAILB_EN
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RW	RW	RW	RW

Table 78. OTP_CTRL1 – OTP control 1 register (address 40h) bit description

Bit	Symbol	Description	
2	OTP_STANDBYINV	**STANDBY pin polarity configs**	
		1b'0	Active high
		1b'1	Active low
		Default condition	0
1	OTP_INTB_RSTB	**INTB/RSTB pin config**	
		1b'0	Enable INTB function
		1b'1	Enable RSTB function
		Default condition	0
0	OTP_XFAILB_EN	**XFAILB function config**	
		1b'0	Disable
		1b'1	Enable
		Default condition	0

16.2.3 OTP_CTRL2

Table 79. OTP_CTRL2 – OTP control 2 register (address 41h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_VINUV_TH[1:0]		OTP_VINOV_TH[1:0]		OTP_VIN_ OVLO_SDWN	OTP_VIN_ OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 80. OTP_CTRL2 – OTP control 2 register (address 41h) bit description

Bit	Symbol	Description	
7 to 6	OTP_VINUV_TH[1:0]	VIN UV threshold config	
		2b'00	96.75 %
		2b'01	96.25 %
		2b'10	95.75 %
		2b'11	95.25 %
		Default Condition	00
5 to 4	OTP_VINOV_TH[1:0]	VIN OV threshold config	
		2b'00	103.25 %
		2b'01	103.75 %
		2b'10	104.25 %
		2b'11	104.75 %
		Default Condition	00
3	OTP_VIN_ OVLO_SDWN	OVLO shutdown config	
		1b'0	Disable
		1b'1	Enable
		Default Condition	0
2	OTP_VIN_OVLO_EN	VIN OVLO config	
		1b'0	Disable
		1b'1	Enable
		Default Condition	0

Table 80. OTP_CTRL2 – OTP control 2 register (address 41h) bit description*...continued*

Bit	Symbol	Description	
1 to 0	OTP_VIN_ OVLO_DBNC[1:0]	VIN OVLO debounce time config	
		2b'00	10 µs
		2b'01	100 µs
		2b'10	1000 µs
		2b'11	Reserved
		Default Condition	00

16.2.4 OTP_CTRL3

Table 81. OTP_CTRL3 – OTP control 3 register (address 42h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	OTP_PD_SEQ_DLY[2:0]			NOT USED	NOT USED	OTP_SW1CONFIG[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RW	RO	R0	RW	RW

Table 82. OTP_CTRL3 – OTP control 3 register (address 42h) bit description

Bit	Symbol	Description	
6 to 4	OTP_PD_ SEQ_DLY[2:0]	Delay after Power Down Sequence config	
		3b'000	No delay
		3b'001	1 ms
		3b'010	10 ms
		3b'011	50 ms
		3b'100	100 ms
		3b'101	250 ms
		3b'110	500 ms
		3b'111	1000 ms
		Default condition	000
1 to 0	OTP_SW1CONFIG[1:0]	SW multiphase config	
		2b'00	SW1, SW2, SW3 operate in single phase mode
		2b'01	SW1/SW2 operate in dual phase mode; SW1 is the primary controller
		2b'10	SW1/SW2/SW3 operate in Triple phase mode; SW1 is the primary controller
		2b'11	Reserved
		Default condition	00

16.2.5 OTP_FREQ_CTRL1

Table 83. OTP_FREQ_CTRL1 – OTP frequency control 1 register (address 43h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW_ MODE	OTP_ SYNC_EN	NOT USED	OTP_FSYNC_ RANGE	OTP_CLK_FREQ[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RO	RW	RW	RW	RW	RW

Table 84. OTP_FREQ_CTRL1 – OTP frequency control 1 register (address 43h) bit description

Bit	Symbol	Description	
7	OTP_SW_MODE	SW default mode config	
		1b'0	PFM mode
		1b'1	PWM mode
		Default condition	0
6	OTP_SYNC_EN	SYNC config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
4	OTP_FSYNC_RANGE	SYNC frequency range config	
		1b'0	Between 2200 KHz and 2800 KHz
		1b'1	Between 17.55 MHz and 22.46 MHz
		Default condition	0
3 to 0	OTP_CLK_FREQ[3:0]	Manual Frequency Turning Config	
		4b'0000	20 MHz
		4b'0001	21 MHz
		4b'0010	22 MHz
		4b'0011	Not used
		4b'0100	Not used
		4b'0101	Not used
		4b'0110	Not used
		4b'0111	Not used
		4b'1000	Not used
		4b'1001	Not used
		4b'1010	Not used
		4b'1011	18 MHz
		4b'1100	19 MHz
		4b'1101	Not used
		4b'1110	Not used
		4b'1111	Not used
		Default condition	0000

16.2.6 OTP_FREQ_CTRL2

Table 85. OTP_FREQ_CTRL2 – OTP frequency control 2 register (address 44h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_FSS_EN	OTP_FSS_ FMOD	OTP_FSS_SEL	NOT USED	OTP_CLK_DIV2[1:0]		OTP_CLK_DIV1[1:0]	
Reset	0	0	1	0	0	0	0	0
Access	RW	RW	RW	RO	RW	RW	RW	RW

Table 86. OTP_FREQ_CTRL2 – OTP frequency control 2 register (address 44h) bit description

Bit	Symbol	Description	
7	OTP_FSS_EN	Spread spectrum config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
6	OTP_FSS_FMOD	Spread spectrum modulation config	
		1b'0	23.5 KHz
		1b'1	Reserved
		Default condition	0
5	OTP_FSS_SEL	Spread Spectrum mode config	
		1b'0	Triangular modulation
		1b'1	Pseudo-random modulation
		Default condition	1
3 to 2	OTP_CLK_DIV2[1:0]	CLK DIV2 config	
		2b'00	2.86
		2b'01	2.52
		2b'10	2.22
		2b'11	Reserved
		Default condition	00
1 to 0	OTP_CLK_DIV1[1:0]	CLK DIV1 config	
		2b'00	4.00
		2b'01	Reserved
		2b'10	2.50
		2b'11	2.20
		Default condition	00

16.2.7 OTP_WD_CONFIG

Table 87. OTP_WD_CONFIG – OTP watchdog configuration register (address 45h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_WD_DURATION[3:0]				OTP_WD_EN	OTP_WD_ STBY_EN	OTP_WD_SEL	OTP_ WDWINDOW
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 88. OTP_WD_CONFIG – OTP watchdog configuration register (address 45h) bit description

Bit	Symbol	Description	
7 to 4	OTP_WD_ DURATION[3:0]	Watchdog duration config	
		4b'0000	1 ms
		4b'0001	2 ms
		4b'0010	4 ms
		4b'0011	8 ms
		4b'0100	16 ms
		4b'0101	32 ms
		4b'0110	64 ms
		4b'0111	128 ms
		4b'1000	256 ms
		4b'1001	512 ms
		4b'1010	1024 ms
		4b'1011	2048 ms
		4b'1100	4096 ms
		4b'1101	8192 ms
		4b'1110	16384 ms
		4b'1111	32768 ms
		Default condition	0000
3	OTP_WD_EN	Watchdog config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
2	OTP_WD_STBY_EN	Watchdog in Standby mode config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
1	OTP_WD_SEL	Watchdog type selection	
		1b'0	Simple
		1b'1	Reserved
		Default condition	0
0	OTP_WDWINDOW	Watchdog window duty config	
		1b'0	100 % open
		1b'1	The second half of the programmed watchdog timer
		Default condition	0

16.2.8 OTP_WD_FLT_EXPIRE

Table 89. OTP_WD_FLT_EXPIRE – OTP watchdog fault expire register (address 46h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	OTP_FAULT_MAX_CNT[2:0]			NOT USED	NOT USED	OTP_WD_MAX_ERROR[1:0]	
Reset	0	0	1	0	0	0	0	0
Access	RO	RW	RW	RW	RO	RO	RW	RW

Table 90. OTP_WD_FLT_EXPIRE – OTP watchdog fault expire register (address 46h) bit description

Bit	Symbol	Description	
6 to 4	OTP_FAULT_ MAX_CNT[2:0]	Fault maximum counter config	
		3b'000	1
		3b'001	2
		3b'010	4
		3b'011	6
		3b'100	8
		3b'101	10
		3b'110	12
		3b'111	15
		Default condition	010
1 to 0	OTP_WD_MAX_ ERROR[1:0]	Watchdog maximum error counter config	
		2b'00	8
		2b'01	6
		2b'10	4
		2b'11	2
		Default condition	00

16.2.9 OTP_PWRUP_CTRL

Table 91. OTP_PWRUP_CTRL – OTP power-up control register (address 47h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_PGOOD_SEQ[5:0]						OTP_CLK_DIV1[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 92. OTP_PWRUP_CTRL – OTP power-up control register (address 47h) bit description

Bit	Symbol	Description	
7 to 2	OTP_PGOOD_ SEQ[5:0]	PGOOD power up sequence slot config	
		slot = (the value) - 1	
		Default condition	000000
1 to 0	OTP_SEQ_TBASE[1:0]	Power up time base config	
		2b'00	100 μs
		2b'01	250 μs
		2b'10	500 μs
		2b'11	1000 μs
		Default condition	00

16.2.10 OTP_SWx_VOLT

Table 93. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_VSWx[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 93. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 94. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit description

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
7 to 0	OTP_VSWx[7:0]	8b'00000000	0.5
		8b'00000001	0.6
		8b'00000010	0.60625
		8b'00000011	0.6125
		8b'00000100	0.61875
		8b'00000101	0.625
		8b'00000110	0.63125
		8b'00000111	0.6375
		8b'00001000	0.64375
		8b'00001001	0.65
		8b'00001010	0.65625
		8b'00001011	0.6625
		8b'00001100	0.66875
		8b'00001101	0.675
		8b'00001110	0.68125
		8b'00001111	0.6875
		8b'00010000	0.69375
		8b'00010001	0.7
		8b'00010010	0.70625
		8b'00010011	0.7125
		8b'00010100	0.71875
		8b'00010101	0.725
		8b'00010110	0.73125
		8b'00010111	0.7375
		8b'00011000	0.74375
		8b'00011001	0.75
		8b'00011010	0.75625
		8b'00011011	0.7625
		8b'00011100	0.76875
		8b'00011101	0.775
		8b'00011110	0.78125
		8b'00011111	0.7875
		8b'00100000	0.79375
		8b'00100001	0.8
		8b'00100010	0.80625
		8b'00100011	0.8125
		8b'00100100	0.81875
		8b'00100101	0.825
		8b'00100110	0.83125

Table 94. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'00100111	0.8375
		8b'00101000	0.84375
		8b'00101001	0.85
		8b'00101010	0.85625
		8b'00101011	0.8625
		8b'00101100	0.86875
		8b'00101101	0.875
		8b'00101110	0.88125
		8b'00101111	0.8875
		8b'00110000	0.89375
		8b'00110001	0.9
		8b'00110010	0.90625
		8b'00110011	0.9125
		8b'00110100	0.91875
		8b'00110101	0.925
		8b'00110110	0.93125
		8b'00110111	0.9375
		8b'00111000	0.94375
		8b'00111001	0.95
		8b'00111010	0.95625
		8b'00111011	0.9625
		8b'00111100	0.96875
		8b'00111101	0.975
		8b'00111110	0.98125
		8b'00111111	0.9875
		8b'01000000	0.99375
		8b'01000001	1
		8b'01000010	1.00625
		8b'01000011	1.0125
		8b'01000100	1.01875
		8b'01000101	1.025
		8b'01000110	1.03125
		8b'01000111	1.0375
		8b'01001000	1.04375
		8b'01001001	1.05
		8b'01001010	1.05625
		8b'01001011	1.0625
		8b'01001100	1.06875
		8b'01001101	1.075
		8b'01001110	1.08125
		8b'01001111	1.0875
		8b'01010000	1.09375
		8b'01010001	1.1
		8b'01010010	1.10625

Table 94. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'01010011	1.1125
		8b'01010100	1.11875
		8b'01010101	1.125
		8b'01010110	1.13125
		8b'01010111	1.1375
		8b'01011000	1.14375
		8b'01011001	1.15
		8b'01011010	1.15625
		8b'01011011	1.1625
		8b'01011100	1.16875
		8b'01011101	1.175
		8b'01011110	1.18125
		8b'01011111	1.1875
		8b'01100000	1.19375
		8b'01100001	1.2
		8b'01100010	1.20625
		8b'01100011	1.2125
		8b'01100100	1.21875
		8b'01100101	1.225
		8b'01100110	1.23125
		8b'01100111	1.2375
		8b'01101000	1.24375
		8b'01101001	1.25
		8b'01101010	1.25625
		8b'01101011	1.2625
		8b'01101100	1.26875
		8b'01101101	1.275
		8b'01101110	1.28125
		8b'01101111	1.2875
		8b'01110000	1.29375
		8b'01110001	1.3
		8b'01110010	1.30625
		8b'01110011	1.3125
		8b'01110100	1.31875
		8b'01110101	1.325
		8b'01110110	1.33125
		8b'01110111	1.3375
		8b'01111000	1.34375
		8b'01111001	1.35
		8b'01111010	Reserved
		8b'01111011	Reserved
		8b'01111100	Reserved
		8b'01111101	1.45
		8b'01111110	Reserved

Table 94. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'01111111	1.5
		8b'10000000	1.8
		8b'10000001	1.8125
		8b'10000010	1.825
		8b'10000011	1.8375
		8b'10000100	1.85
		8b'10000101	1.8625
		8b'10000110	1.875
		8b'10000111	1.8875
		8b'10001000	1.9
		8b'10001001	1.9125
		8b'10001010	1.925
		8b'10001011	1.9375
		8b'10001100	1.95
		8b'10001101	1.9625
		8b'10001110	1.975
		8b'10001111	1.9875
		8b'10010000	2
		8b'10010001	2.0125
		8b'10010010	2.025
		8b'10010011	2.0375
		8b'10010100	2.05
		8b'10010101	2.0625
		8b'10010110	2.075
		8b'10010111	2.0875
		8b'10011000	2.1
		8b'10011001	2.1125
		8b'10011010	2.125
		8b'10011011	2.1375
		8b'10011100	2.15
		8b'10011101	2.1625
		8b'10011110	2.175
		8b'10011111	2.1875
		8b'10100000	2.2
		8b'10100001	2.2125
		8b'10100010	2.225
		8b'10100011	2.2375
		8b'10100100	2.25
		8b'10100101	2.2625
		8b'10100110	2.275
		8b'10100111	2.2875
		8b'10101000	2.3
		8b'10101001	2.3125
		8b'10101010	2.325

Table 94. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'10101011	2.3375
		8b'10101100	2.35
		8b'10101101	2.3625
		8b'10101110	2.375
		8b'10101111	2.3875
		8b'10110000	2.4
		8b'10110001	2.4125
		8b'10110010	2.425
		8b'10110011	2.4375
		8b'10110100	2.45
		8b'10110101	2.4625
		8b'10110110	2.475
		8b'10110111	2.4875
		8b'10111000	2.5
		8b'10111001	Reserved
		8b'10111010	Reserved
		8b'10111011	2.6
		8b'10111100	Reserved
		8b'10111101	Reserved
		8b'10111110	Reserved
		8b'10111111	Reserved
		8b'11000000	2.8
		8b'11000001	2.825
		8b'11000010	2.85
		8b'11000011	2.875
		8b'11000100	2.9
		8b'11000101	2.925
		8b'11000110	2.95
		8b'11000111	2.975
		8b'11001000	3
		8b'11001001	3.025
		8b'11001010	3.05
		8b'11001011	3.075
		8b'11001100	3.1
		8b'11001101	3.125
		8b'11001110	3.15
		8b'11001111	3.175
		8b'11010000	3.2
		8b'11010001	3.225
		8b'11010010	3.25
		8b'11010011	3.275
		8b'11010100	3.3
		8b'11010101	Reserved
		8b'11010110	Reserved

Table 94. OTP_SWx_VOLT OTP - Switcher voltage register (address 49h, 4Dh, 51h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'11010111	Reserved
		8b'11011000	Reserved
		8b'11011001	Reserved
		8b'11011010	Reserved
		8b'11011011	Reserved
		8b'11011100	Reserved
		8b'11011101	Reserved
		8b'11011110	Reserved
		8b'11011111	Reserved
		8b'11100000	Reserved
		8b'11100001	Reserved
		8b'11100010	Reserved
		8b'11100011	Reserved
		8b'11100100	Reserved
		8b'11100101	Reserved
		8b'11100110	Reserved
		8b'11100111	Reserved
		8b'11101000	Reserved
		8b'11101001	Reserved
		8b'11101010	Reserved
		8b'11101011	Reserved
		8b'11101100	Reserved
		8b'11101101	Reserved
		8b'11101110	Reserved
		8b'11101111	Reserved
		8b'11110000	Reserved
		8b'11110001	Reserved
		8b'11110010	Reserved
		8b'11110011	Reserved
		8b'11110100	Reserved
		8b'11110101	Reserved
		8b'11110110	Reserved
		8b'11110111	Reserved
		8b'11111000	Reserved
		8b'11111001	Reserved
		8b'11111010	Reserved
		8b'11111011	Reserved
		8b'11111100	Reserved
		8b'11111101	Reserved
		8b'11111110	Reserved
		8b'11111111	Reserved
		Reset condition	OFF_OTP

16.2.11 OTP_SWx_PWRUP

Table 95. OTP_SWx_PWRUP – OTP switcher power-up register (address 4Ah, 4Eh, 52h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	OTP_SWx_SEQ[5:0]					
Reset	0	0	1	0	0	0	0	0
Access	RW	RW	RW	RW	RO	RO	RW	RW

Table 96. OTP_SWx_PWRUP – OTP switcher power-up register (address 4Ah, 4Eh, 52h) bit description

Bit	Symbol	Description	
5 to 0	OTP_SWx_SEQ[5:0]	OTP_SWx_SEQ	
		Default condtion	000000

16.2.12 OTP_SWx_CONFIG1

Table 97. OTP_SWx_CONFIG1 – OTP switcher configuration 1 register (address 4Bh, 4Fh, 53h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SWx_UV_TH[1:0]		OTP_SWx_OV_TH[1:0]		NOT USED	NOT USED	OTP_SWx_ILIM[1:0]	
Reset	0	0	1	0	0	0	0	0
Access	RW	RW	RW	RW	RO	RO	RW	RW

Table 98. OTP_SWx_CONFIG1 – OTP switcher configuration 1 register (address 4Bh, 4Fh, 53h) bit description

Bit	Symbol	Description	
7 to 6	OTP_SWx_UV_TH[1:0]	SWx UV threshold config	
		2b'00	96.5 %
		2b'01	96 %
		2b'10	95.5 %
		2b'11	95 %
		Default condition	00
5 to 4	OTP_SWx_OV_TH[1:0]	SWx OV threshold config	
		2b'00	103.5 %
		2b'01	104 %
		2b'10	104.5 %
		2b'11	105 %
		Default condition	10
1 to 0	OTP_SWxILIM[1:0]	SWx Current Limit Config	
		2b'00	Reserved
		2b'01	4.0 A
		2b'10	5.0 A
		2b'11	6.0 A
		Default condition	01

16.2.13 OTP_SWx_CONFIG2

Table 99. OTP_SWx_CONFIG2 – OTP switcher configuration 2 register (address 4Ch, 50h, 54h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	OTP_SWx_LSELECT[1:0]		OTP_SWxPHASE[2:0]			NOT USED	OTP_SWx_PG_EN	OTP_SWx_CLK
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RO	RW	RW

Table 100. OTP_SWx_CONFIG2 – OTP switcher configuration 2 register (address 4Ch, 50h, 54h) bit description

Bit	Symbol	Description	
7 to 6	OTP_SWx_LSELECT[1:0]	SWx inductor selection	
		2b'00	0.22 µH
		2b'01	0.44 µH
		2b'10	Reserved
		2b'11	Reserved
		Default condition	00
5 to 3	OTP_SWxPHASE[2:0]	SWx phase config	
		3b'000	No phase shift
		3b'001	Shifted by 1 CLK
		3b'010	Shifted by 2 CLK
		3b'011	Shifted by 3 CLK
		3b'100	Shifted by 4 CLK
		3b'101	Reserved
		3b'110	Reserved
		3b'111	Reserved
		Default condition	000
1	OTP_SWx_PG_EN	SWx PGOOD impact config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
0	OTP_SWx_CLK	SWx CLK config	
		1b'0	CLK DIV1
		1b'1	CLK DIV2
		Default condition	0

16.2.14 OTP_LDOx_VOLT

Table 101. OTP_LDOx_VOLT – OTP LDO Voltage register (address 60h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	—	—	—	OTP_VLDOx[4:0]				
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RW	RW	RW	RW	RW

Table 102. OTP_LDOx_VOLT – OTP LDO Voltage register (address 60h) bit description

Bit	Symbol	Description	
4 to 0	OTP_VLDOx[4:0]	LDOx output voltage configuration (V)	
		5b'00000	0.75
		5b'00001	0.8
		5b'00010	0.85
		5b'00011	0.9
		5b'00100	0.95
		5b'00101	1
		5b'00110	1.05
		5b'00111	1.1
		5b'01000	1.15
		5b'01001	1.2
		5b'01010	1.25
		5b'01011	1.3
		5b'01100	1.35
		5b'01101	1.4
		5b'01110	1.45
		5b'01111	1.5
		5b'10000	1.8
		5b'10001	1.9
		5b'10010	2
		5b'10011	2.1
		5b'10100	2.2
		5b'10101	2.3
		5b'10110	2.4
		5b'10111	2.5
		5b'11000	2.6
		5b'11001	2.7
		5b'11010	2.8
		5b'11011	2.9
		5b'11100	3
		5b'11101	3.1
		5b'11110	3.2
		5b'11111	3.3
		Default condition	00000

16.2.15 OTP_LDOx_PWRUP

Table 103. OTP_LDOx_PWRUP – OTP LDO power-up register (address 61h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LDOx_RAMP	—	OTP_LDOx_SEQ[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RW	RW	RW	RW	RW	RW

Table 104. OTP_LDOx_PWRUP – OTP LDO power-up register (address 61h) bit description

Bit	Symbol	Description	
7	LDOx_RAMP	LDO ramp speed	
		Fast ramp	0
		Slow ramp	1
		Default condition	0
5 to 0	OTP_LDOx_SEQ[5:0]	LDO1 Power up sequence slot config	
		slot = (the value) - 1	
		Default condition	000000

16.2.16 OTP_LDOx_CONFIG

Table 105. OTP_LDOx_CONFIG – OTP LDO configuration register (address 62h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_LDOxUV_TH[1:0]		OTP_LDOxOV_TH[1:0]		NOT USED	OTP_LDOx_ PG_EN	OTP_LDOx_ RAMP	OTP_LDOxLS
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RO	RW	RW	RW

Table 106. OTP_LDOx_CONFIG – OTP LDO configuration register (address 62h) bit description

Bit	Symbol	Description	
7 to 6	OTP_LDOxUV_TH[1:0]	LDOx UV threshold config	
		2b'00	96.5 %
		2b'01	96 %
		2b'10	95.5 %
		2b'11	95 %
		Default condition	00
5 to 4	OTP_LDOxOV_TH[1:0]	LDOx OV threshold config	
		2b'00	103.5 %
		2b'01	104 %
		2b'10	104.5 %
		2b'11	105 %
		Default condition	00
2	OTP_LDOx_PG_EN	LDOx PGOOD Impact Config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
1	OTP_LDOx_RAMP	LDOx Ramp Rate Config	
		1b'0	Fast ramp
		1b'1	Slow ramp
		Default condition	0
0	OTP_LDOxLS	LDOx Load Switch Mode Config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0

16.2.17 OTP_OV_BYPASS

Table 107. OTP_OV_BYPASS – OTP overvoltage bypass register (address 63h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	OTP_LDO2_ OV_BYPASS	OTP_LDO1_ OV_BYPASS	NOT USED	NOT USED	OTP_SW3_ OV_BYPASS	OTP_SW2_ OV_BYPASS	OTP_SW1_ OV_BYPASS
Reset	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RO	RO	RW	RW	RW

Table 108. OTP_OV_BYPASS – OTP overvoltage bypass register (address 63h) bit description

Bit	Symbol	Description	
6	OTP_LDO2_ OV_BYPASS	LDO2 OV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
5	OTP_LDO1_ OV_BYPASS	LDO1 OV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
2	OTP_SW3_ OV_BYPASS	SW3 OV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
1	OTP_SW2_ OV_BYPASS	SW2 OV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
0	OTP_SW1_ OV_BYPASS	SW1 OV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0

16.2.18 OTP_UV_BYPASS

Table 109. OTP_UV_BYPASS – OTP undervoltage bypass register (address 64h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	OTP_LDO2_ UV_BYPASS	OTP_LDO1_ UV_BYPASS	NOT USED	NOT USED	OTP_SW3_ UV_BYPASS	OTP_SW2_ UV_BYPASS	OTP_SW1_ UV_BYPASS
Reset	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RO	RO	RW	RW	RW

Table 110. OTP_UV_BYPASS – OTP undervoltage bypass register (address 64h) bit description

Bit	Symbol	Description	
6	OTP_LDO2_ UV_BYPASS	LDO2 UV BYPASS Configf	
		1b'0	Disable bypass

Table 110. OTP_UV_BYPASS – OTP undervoltage bypass register (address 64h) bit description*...continued*

Bit	Symbol	Description	
		1b'1	Enable bypass
		Default condition	0
5	OTP_LDO1_ UV_BYPASS	LDO1 UV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
2	OTP_SW3_ UV_BYPASS	SW3 UV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
1	OTP_SW2_ UV_BYPASS	SW2 UV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
0	OTP_SW1_ UV_BYPASS	SW1 UV BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0

16.2.19 OTP_ILIM_BYPASS

Table 111. OTP_ILIM_BYPASS – OTP current limit bypass register (address 65h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	OTP_LDO2_ ILIM_BYPASS	OTP_LDO1_ ILIM_BYPASS	NOT USED	NOT USED	OTP_SW3_ ILIM_BYPASS	OTP_SW2_ ILIM_BYPASS	OTP_SW1_ ILIM_BYPASS
Reset	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RO	RO	RW	RW	RW

Table 112. OTP_ILIM_BYPASS – OTP current limit bypass register (address 65h) bit description

Bit	Symbol	Description	
6	OTP_LDO2_ ILIM_BYPASS	LDO2 ILIM BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
5	OTP_LDO1_ ILIM_BYPASS	LDO1 ILIM BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
2	OTP_SW3_ ILIM_BYPASS	SW3 ILIM BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
1	OTP_SW2_ ILIM_BYPASS	SW2 ILIM BYPASS Config	

Table 112. OTP_ILIM_BYPASS – OTP current limit bypass register (address 65h) bit description*...continued*

Bit	Symbol	Description	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
0	OTP_SW1_ ILIM_BYPASS	SW1 ILIM BYPASS Config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0

16.2.20 OTP_ID_2

Table 113. OTP_ID_2 – OTP identification 2 register (address 66h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_ID_REV[3:0]				OTP_ID_H[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 114. OTP_ID_2 – OTP identification 2 register (address 66h) bit description

Bit	Symbol	Description	
7 to 4	OTP_ID_REV[3:0]	OTP_ID_REV[3:0]	
		Default condition	0000
3 to 0	OTP_ID_H[3:0]	OTP_ID_H[3:0]	
		Default condition	0000

16.2.21 OTP_ID_1

Table 115. OTP_ID_1 – OTP identification 1 register (address 67h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol			OTP_ID_L[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RW	RW	RW	RW	RW	RW

Table 116. OTP_ID_1 – OTP identification 1 register (address 67h) bit description

Bit	Symbol	Description	
5 to 0	OTP_ID_L[5:0]	OTP_ID_L[3:0]	
		Reset condition	000000

16.2.22 OTP_SW_COMP1

Table 117. OTP_SW_COMP1 – OTP switcher compensation 1 register (address 68h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	OTP_SW2_GM_COMP[2:0]			OTP_SW1_GM_COMP[2:0]		
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RW	RW	RW	RW	RW	RW

Table 118. OTP_SW_COMP1 – OTP switcher compensation 1 register (address 68h) bit description

Bit	Symbol	Description	
5 to 3	OTP_SW2_ GM_COMP[2:0]	SW2 GM COMP Config	
		3b'000	18 µS
		3b'001	35 µS
		3b'010	53 µS
		3b'011	70 µS
		3b'100	88 µS
		3b'101	105 µS
		3b'110	123 µS
		3b'111	140 µS
		Default condition	100
2 to 0	OTP_SW1_ GM_COMP[2:0]	SW1 GM COMP Config	
		3b'000	18 µS
		3b'001	35 µS
		3b'010	53 µS
		3b'011	70 µS
		3b'100	88 µS
		3b'101	105 µS
		3b'110	123 µS
		3b'111	140 µS
		Default condition	100

16.2.23 OTP_SW_COMP2

Table 119. OTP_SW_COMP2 - OTP switcher compensation 2 register (address 69h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OTP_SW3_GM_COMP[2:0]		
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	Ro	RO	RO	RW	RW	RW

Table 120. OTP_SW_COMP2 - OTP switcher compensation 2 register (address 69h) bit description

Bit	**Symbol**	**Description**	
2 to 0	OTP_SW3_ GM_COMP[2:0]	SW3 GM COMP Config	
		3b'000	18 µS
		3b'001	35 µS
		3b'010	53 µS
		3b'011	70 µS
		3b'100	88 µS
		3b'101	105 µS
		3b'110	123 µS
		3b'111	140 µS
		Default condition	100

16.2.24 OTP_SW_COMP3

Table 121. OTP_SW_COMP3 – OTP switcher compensation 3 register (address 6Ah) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	OTP_SW2_C_COMP[1:0]		OTP_SW2_R_COMP[1:0]		OTP_SW1_C_COMP[1:0]		OTP_SW1_R_COMP[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 122. OTP_SW_COMP3 – OTP switcher compensation 3 register (address 6Ah) bit description

Bit	**Symbol**	**Description**	
7 to 6	OTP_SW2_ C_COMP[1:0]	SW2 C COMP Config	
		2b'00	40 pF
		2b'01	60 pF
		2b'10	80 pF
		2b'11	100 pF
		Default condition	11
5 to 4	OTP_SW2_ R_COMP[1:0]	SW2 R COMP Config	
		2b'00	40 kΩ
		2b'01	80 kΩ
		2b'10	40 kΩ
		2b'11	160 kΩ
		Default condition	01

Table 122. OTP_SW_COMP3 – OTP switcher compensation 3 register (address 6Ah) bit description*...continued*

Bit	Symbol	Description	
3 to 2	OTP_SW1_C_COMP[1:0]	SW1 C COMP Config	
		2b'00	40 pF
		2b'01	60 pF
		2b'10	80 pF
		2b'11	100 pF
		Default condition	11
1 to 0	OTP_SW1_R_COMP[1:0]	SW1 R COMP Config	
		2b'00	40 kΩ
		2b'01	80 kΩ
		2b'10	40 kΩ
		2b'11	160 kΩ
		Default condition	01

16.2.25 OTP_SW_COMP4

Table 123. OTP_SW_COMP4 – OTP switcher compensation 4 register (address 68h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	OTP_SW3_C_COMP[1:0]		OTP_SW3_R_COMP[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RW	RW	RW	RW

Table 124. OTP_SW_COMP4 – OTP switcher compensation 4 register (address 68h) bit description

Bit	Symbol	Description	
3 to 2	OTP_SW3_C_COMP[1:0]	SW3 C COMP Config	
		2b'00	40 pF
		2b'01	60 pF
		2b'10	80 pF
		2b'11	100 pF
		Default condition	11
1 to 0	OTP_SW3_R_COMP[1:0]	SW3 R COMP Config	
		2b'00	40 kΩ
		2b'01	80 kΩ
		2b'10	40 kΩ
		2b'11	160 kΩ
		Default condition	01

16.2.26 OTP_SW_RAMP

Table 125. OTP_SW_RAMP – OTP switcher ramp register (address 6Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	OTP_SW3DVS_RAMP[1:0]		OTP_SW2DVS_RAMP[1:0]		OTP_SW1DVS_RAMP[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R0	R0	RW	RW	RW	RW	RW	RW

Table 126. OTP_SW_RAMP – OTP switcher ramp register (address 6Ch) bit description

Bit	Symbol	Description	
5 to 4	OTP_SW3DVS_RAMP[1:0]	SW3 DVS ramp configuration	
		2b'00	7.8 mV/µs at fsw = 2.5 MHz
		2b'01	15.6 mV/µs at fsw = 2.5MHz
		2b'10	3.9 mV/us at fsw = 2.5 MHz
		2b'11	1.95 mV/µs at fsw = 2.5 MHz
		Default condition	00
3 to 2	OTP_SW2DVS_RAMP[1:0]	SW2 DVS ramp configuration	
		2b'00	7.8 mV/µs at fsw = 2.5 MHz
		2b'01	15.6 mV/µs at fsw = 2.5 MHz
		2b'10	3.9 mV/us at fsw = 2.5 MHz
		2b'11	1.95 mV/µs at fsw = 2.5 MHz
		Default condition	00
1 to 0	OTP_SW1DVS_RAMP[1:0]	SW1 DVS ramp configuration	
		2b'00	7.8 mV/µs at fsw = 2.5 MHz
		2b'01	15.6 mV/µs at fsw = 2.5 MHz
		2b'10	3.9 mV/us at fsw = 2.5 MHz
		2b'11	1.95 mV/µs at fsw = 2.5 MHz
		Default condition	00

16.2.27 OTP_ASIL_CONFIG

Table 127. OTP_ASIL_CONFIG - Configuration register (address 6Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_ BGMON_SEL	OTP_LDOx OUT_OPEN	OTP_BGMON_ BYPASS	OTP_FS_ BYPASS_CNT	OTP_FS_ BYPASS	OTP_ SYNC_STBY	OTP_WD_ FAULT_REC	OTP_ FCCU_EN
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RO	RO

Table 128. OTP_ASIL_CONFIG - Configuration register (address 6Dh) bit description

Bit	Symbol	Description	
7	OTP_BGMON_SEL	Bandgap/VIN voltage monitor config	
		1b'0	Enable only Bandgap voltage monitor
		1b'1	Enable Bandgap and VIN voltage monitor
		Default condition	0
6	OTP_LDOx OUT_OPEN	LDOx output open fault detection config	
		1b'0	Disable
		1b'1	Enable
		Default condition	0
5	OTP_BGMON_ BYPASS	Bandgap voltage monitor bypass config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
4	OTP_FS_ BYPASS_CNT	Fail-safe bypass counter config	
		1b'0	The maximum number of transitions is 15
		1b'1	The number of transition is infinite
		Default condition	0
3	OTP_FS_BYPASS	Fail-safe bypass config	
		1b'0	Disable bypass
		1b'1	Enable bypass
		Default condition	0
2	OTP_SYNC_STBY	SYNC/STANDBY pin config	
		1b'0	Enable SYNC mode
		1b'1	Enable Standby mode
		Default condition	0
1	OTP_WD_FAULT_REC	Watchdog fault recovery	
		1b'0	FCCU fault without watchdog window recovery
		1b'1	FCCU fault with watchdog window recovery
		Default condition	0
0	OTP_FCCU_EN	**OTP FCCU Enable**	
		1b'0	FCCU monitoring disabled
		1b'1	FCCU monitoring enabled
		Default condition	0

16.2.28 OTP_S2_CRC_LSB

Table 129. OTP_S2_CRC_LSB – OTP S2 CRC least significant bits register (address 6Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_S2_CRC_LSB[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 130. OTP_S2_CRC_LSB – OTP S2 CRC least significant bits register (address 6Eh) bit description

Bit	Symbol	Description	
7 to 0	OTP_S2_CRC_LSB[7:0]	CRC LSB code	
		Default condition	00000000

16.2.29 OTP_S2_CRC_MSB

Table 131. OTP_S2_CRC_MSB – OTP S2 CRC most significant bits register (address 6Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_S2_CRC_MSB[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Table 132. OTP_S2_CRC_MSB – OTP S2 CRC most significant bits register (address 6Fh) bit description

Bit	Symbol	Description	
7 to 0	OTP_S2_CRC_MSB[7:0]	CRC MSB code	
		Default condition	00000000

16.3 PF5103 functional register map

Table 133. Functional register map

ADDRESS	Register Name	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	DEVICE_ID	0111_0011	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
0x01	REV_ID	0010_0001	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
0x02	PROG_ID	0000_0000	PROG_ID_ASIL[1:0]							
0x03	PROG_ID_REV	0000_0000	PROG_ID_REV[3:0]							
0x04	INT_STATUS1	0000_0000	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	—	PGOOD_I	VIN_OVLO_I
0x05	INT_MASK1	1111_1011	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	—	PGOOD_M	VIN_OVLO_M
0x06	INT_SENSE1	0000_0000	—	—	—	PWRON_S	—	—	PGOOD_S	VIN_OVLO_S
0x07	INT_STATUS2	0000_0000	WD_EVENT_I	WD_ERROR_I	WD_INIT_I	REGMAP_CRC_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
0x08	INT_MASK2	1111_1111	WD_EVENT_M	WD_ERROR_M	WD_INIT_M	REGMAP_CRC_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M
0x09	INT_SENSE2	0000_0000	—	—	—	—	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
0x0A	INT_STATUS3	0000_0000	BGMON_I	FSYNC_I	FSYNC_FLT_I	CLK_MON_I	RSTB_I	FCCU_I	—	PG_SHORT_I
0x0B	INT_MASK3	1111_0111	BGMON_M	FSYNC_M	FSYNC_FLT_M	CLK_MON_M	—	FCCU_M	—	PG_SHORT_M
0x0C	INT_SENSE3	0000_0000	BGMON_S	FSYNC_S	FSYNC_FLT_S	—	RSTB_S	FCCU_S	—	—
0x0D	SW_MODE_INT	0000_0000	—	—	—	—	—	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
0x0E	SW_MODE_MASK	0000_1111	—	—	—	—	—	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
0x0F	REG_ILIM_INT	0000_0000	—	LDO2_ILIM_I	LDO1_ILIM_I	—	—	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I
0x10	REG_ILIM_MASK	0111_1111	—	LDO2_ILIM_M	LDO1_ILIM_M	—	—	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
0x11	REG_ILIM_SENSE	0000_0000	—	LDO2_ILIM_S	LDO1_ILIM_SRESERVED	—	—	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
0x12	REG_UV_INT	0000_0000	VIN_UV_I	LDO2_UV_I	LDO1_UV_I	—	—	SW3_UV_I	SW2_UV_I	SW1_UV_I
0x13	REG_UV_MASK	1111_1111	VIN_UV_M	LDO2_UV_M	LDO1_UV_M	—	—	SW3_UV_M	SW2_UV_M	SW1_UV_M
0x14	REG_UV_SENSE	0000_0000	VIN_UV_S	LDO2_UV_S	LDO1_UV_S	—	—	SW3_UV_S	SW2_UV_S	SW1_UV_S
0x15	REG_OV_INT	0000_0000	VIN_OV_I	LDO2_OV_I	LDO1_OV_I	—	—	SW3_OV_I	SW2_OV_I	SW1_OV_I
0x16	REG_OV_MASK	1111_1111	VIN_OV_M	LDO2_OV_M	LDO1_OV_M	—	—	SW3_OV_M	SW2_OV_M	SW1_OV_M
0x17	REG_OV_SENSE	0000_0000	VIN_OV_S	LDO2_OV_S	LDO1_OV_S	—	—	SW3_OV_S	SW2_OV_S	SW1_OV_S
0x18	SYS_INT	0000_0000	—	STATUS3_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
0x19	HARDFAULT_FLAGS	0000_0000	—	—	—	—	PU_FAIL	PG_FAIL	REG_FAIL	TSD_FAIL
0x1B	ABIST_CTRL	0000_0000	—	—	—	—	—	AB_FCCU_H	AB_DONE	AB_RUN
0x1C	ABIST_OV1	0000_0000	AB_VIN_OV	AB_LDO2_OV	AB_LDO1_OV	—	—	AB_SW3_OV	AB_SW2_OV	AB_SW1_OV
0x1D	ABIST_UV1	0000_0000	AB_VIN_UV	AB_LDO2_UV	AB_LDO1_UV	—	—	AB_SW3_UV	AB_SW2_UV	AB_SW1_UV
0x1E	TEST_FLAGS	0000_0000	—	—	—	RESERVED	RESERVED	STEST_NOK	TRIM_NOK	OTP_NOK
0x20	RANDOM_GEN	0000_0000	RANDOM_GEN[7:0]							
0x21	RANDOM_CHK	0000_0000	RANDOM_CHK[7:0]							
0x22	**VMONEN1**	0111_1111	—	LDO2VMON_EN	LDO1VMON_EN	—	—	SW3VMON_EN	SW2VMON_EN	SW1VMON_EN
0x23	**CTRL1**	0001_0000	VIN_OVLO_EN	VIN_OVLO_SDWN	SYNC_EN	TMP_MON_EN	WD_SEL	WD_STBY_EN	WD_EN	I2C_SECURE_EN
0x24	**CTRL2**	0001_0000	VIN_OVLO_DBNC[1:0]		—	TMP_MON_AON	—	STANDBYINV	—	—
0x25	**CTRL3**	1010_0000	OV_DB[1:0]		UV_DB[1:0]		PGOOD_RLS	ULP_OFF_CTRL	PMIC_OFF	INTB_TEST
0x26	PWRUP_CTRL	0000_0000	PGOOD_SEQ[5:0]						SEQ_TBASE[1:0]	
0x27	**FREQ_CTRL**	0000_0000	FSS_SEL	FSYNC_RANGE	FSS_EN	FSS_FMOD	CLK_FREQ[3:0]			
0x28	GPO_CTRL	0000_0000	—	—	GPO_SEQ[5:0]					
0x29	**WD_CONFIG**	0110_0000	WDW_RECOVERY[3:0]				WD_DURATION[3:0]			

Table 133. Functional register map*...continued*

ADDRESS	Register Name	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x2A	WD_ANSWER	0000_0000	WD_ANSWER[7:0]							
0x2B	WD_SEED	0101_1011	WD_SEED[7:0]							
0x2C	WD_ERROR	0011_0000	—	—	WD_MAX_ERROR[1:0]		WD_ERROR_CNT[3:0]			
0x2D	**ASIL_CFG**	0000_0000	—	—	—	—	—	FCCU_POL	FCCU_CFG[1:0]	
0x2E	**FAULT_COUNTER**	0000_0000	—	FAULT_MAX_CNT[2:0]			FAULT_CNT[3:0]			
0x2F	FSAFE_COUNTER	0000_0000	—	—	—	—	FS_BYPASS_CNT[3:0]			
0x30	AMUX	0000_0000	—	—	AMUX_EN	AMUX_SEL[4:0]				
0x31	SW_RAMP	0000_0000	—		SW3DVS_RAMP[1:0]		SW2DVS_RAMP[1:0]		SW1DVS_RAMP[1:0]	
0x32	**SW1_CONFIG1**	0001_1100	SW1_UV_BYPASS	SW1_OV_BYPASS	SW1_ILIM_BYPASS	SW1_UV_STATE	SW1_OV_STATE	SW1_ILIM_STATE	—	SW1_PG_EN
0x33	**SW1_CONFIG2**	1000_0000	SW1_FLT_REN	—	—	SW1ILIM[1:0]		SW1PHASE[2:0]		
0x34	**SW1_PWRUP**	0000_0000	—	—	SW1_SEQ[5:0]					
0x35	**SW1_MODE**	0000_0000	SW1_OV_TH[1:0]		SW1_UV_TH[1:0]		SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]	
0x36	**SW1_RUN_VOLT**	0000_0000	VSW1_RUN[7:0]							
0x37	**SW1_STBY_VOLT**	0000_0000	VSW1_STBY[7:0]							
0x39	**SW2_CONFIG1**	0001_1100	SW2_UV_BYPASS	SW2_OV_BYPASS	SW2_ILIM_BYPASS	SW2_UV_STATE	SW2_OV_STATE	SW2_ILIM_STATE	—	SW2_PG_EN
0x3A	**SW2_CONFIG2**	1000_0000	SW2_FLT_REN	—	—	SW2ILIM[1:0]		SW2PHASE[2:0]		
0x3B	**SW2_PWRUP**	0000_0000	—	—	SW2_SEQ[5:0]					
0x3C	**SW2_MODE**	0000_0000	SW2_OV_TH[1:0]		SW2_UV_TH[1:0]		SW2_STBY_MODE[1:0]		SW2_RUN_MODE[1:0]	
0x3D	**SW2_RUN_VOLT**	0000_0000	VSW2_RUN[7:0]							
0x3E	**SW2_STBY_VOLT**	0000_0000	VSW2_STBY[7:0]							
0x40	**SW3_CONFIG1**	0001_1100	SW3_UV_BYPASS	SW3_OV_BYPASS	SW3_ILIM_BYPASS	SW3_UV_STATE	SW3_OV_STATE	SW3_ILIM_STATE	—	SW3_PG_EN
0x41	**SW3_CONFIG2**	1000_0000	SW3_FLT_REN	—	—	SW3ILIM[1:0]		SW3PHASE[2:0]		
0x42	**SW3_PWRUP**	0000_0000	—	—	SW3_SEQ[5:0]					
0x43	**SW3_MODE**	0000_0000	SW3_OV_TH[1:0]		SW3_UV_TH[1:0]		SW3_STBY_MODE[1:0]		SW3_RUN_MODE[1:0]	
0x44	**SW3_RUN_VOLT**	0000_0000	VSW3_RUN[7:0]							
0x45	**SW3_STBY_VOLT**	0000_0000	VSW3_STBY[7:0]							
0x55	**LDO1_CONFIG1**	0001_1100	LDO1_UV_BYPASS	LDO1_OV_BYPASS	LDO1_ILIM_BYPASS	LDO1_UV_STATE	LDO1_OV_STATE	LDO1_ILIM_STATE	—	LDO1_PG_EN
0x56	**LDO1_CONFIG2**	1000_0000	LDO1_FLT_REN	—	—	—	—	—	LDO1_RUN_EN	LDO1_STBY_EN
0x57	**LDO1_PWRUP**	0000_0000	LDO1_RAMP	—	LDO1_SEQ[5:0]					
0x58	**LDO1_RUN_VOLT**	0000_0000	—	—	—	VLDO1_RUN[4:0]				
0x59	**LDO1_STBY_VOLT**	0000_0000	—	—	—	VLDO1_STBY[4:0]				
0x5B	**LDO2_CONFIG1**	0001_1100	LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2_ILIM_BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2_ILIM_STATE	—	LDO2_PG_EN
0x5C	**LDO2_CONFIG2**	1000_0000	LDO2_FLT_REN	—	—	—	—	—	LDO2_RUN_EN	LDO2_STBY_EN
0x5D	**LDO2_PWRUP**	0000_0000	LDO2_RAMP	—	LDO2_SEQ[5:0]					
0x5E	**LDO2_RUN_VOLT**	0000_0000	—	—	—	VLDO2_RUN[4:0]				
0x5F	**LDO2_STBY_VOLT**	0000_0000	—	—	—	VLDO2_STBY[4:0]				
0x60	STATE	0000_0000	NXP_TM	CUST_TM	DBG_MODE	STATE[4:0]				

Note: *Functional bits are in bold with continuous CRC check.*

16.4 Functional registers

16.4.1 DEVICE_ID

Table 134. DEVICE_ID – Device identification register (address 00h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
Reset	0	0	0	1	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 135. DEVICE_ID – Device identification register (address 00h) bit description

Bit	Symbol	Description	
7 to 4	DEVICE_FAM[3:0]	Device family is hardcoded for every device	
		4b'0111	PF51 family
		Other combinations	RESERVED
		Reset condition	OFF_OTP
3 to 0	DEVICE_ID[3:0]	Device ID is loaded from Trim OTP	
		4b'0011	PF5103
		4b'1000	RESERVED
		4b'1001	PF5113
		4b'1010	PF5123
		Other combinations	RESERVED
		Reset condition	OFF_OTP

16.4.2 REV_ID

Table 136. REV_ID – Revision identification register (address 01h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
Reset	0	0	1	0	0	0	0	1
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 137. REV_ID – Revision identification register (address 01h) bit bit description

Bit	Symbol	Description	
7 to 4	**FULL_LAYER_REV[3:0]**	Full layer revision per silicon pass	
		4b'0000	0
		4b'0001	A
		4b'0010	B
		4b'0011	C
		4b'0100	D
		4b'0101	E
		4b'0110	F
		4b'0111	G
		4b'1000	H
		4b'1001	J
		4b'1010	K
		4b'1011	L
		4b'1100	M
		4b'1101	N
		4b'1110	P
		4b'1111	Q
		Reset condition	—
3 to 0	**METAL_LAYER_REV[3:0]**	Metal layer revision per silicon pass	
		4b'0000	0
		4b'0001	1
		4b'0010	2
		4b'0011	3
		4b'0100	4
		4b'0101	5
		4b'0110	6
		4b'0111	7
		4b'1000	8
		4b'1001	9
		4b'1010	10
		4b'1011	11
		4b'1100	12
		4b'1101	13
		4b'1110	14
		4b'1111	15
		Reset condition	—

16.4.3 PROG_ID

Table 138. PROG_ID – Programmable identification register (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PROG_ID_ASIL		PROG_ID_H				PROG_ID_L_MSB	
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 139. PROG_ID – Programmable identification register (address 02h) bit description

Bit	Symbol	Description	
7 to 6	PROG_ID_ASIL[1:0]	ASIL selection from VOTP_MARK_ASIL[3:0]	
		2b'00	QM
		2b'01	x
		2b'10	ASIL B
		2b'11	x
		Reset condition	OFF_OTP
5 to 2	PROG_ID_H[3:0]	4b'0000	OTP_ID_H[3:0]
		4b'0001	
		4b'0010	
		4b'0011	
		4b'0100	
		4b'0101	
		4b'0110	
		4b'0111	
		4b'1000	
		4b'1001	
		4b'1010	
		4b'1011	
		4b'1100	
		4b'1101	
		4b'1110	
		4b'1111	
		Reset condition	OFF_OTP
1 to 0	PROG_ID_L_MSB[1:0]	2 MSBs of OTP_ID_L register	
		2b'00	OTP_ID_L[5:4]
		2b'01	
		2b'10	
		2b'11	
		Reset condition	OFF_OTP

16.4.4 PROG_ID_REV

Table 140. PROG_ID_REV – Programmable identification revision register (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PROG_ID_L_LSB				PROG_ID_REV			
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 141. PROG_ID_REV – Programmable identification revision register (address 03h) bit description

Bit	Symbol	Description	
7 to 4	PROG_ID_L_LSB[3:0]	4 LSBs of OTP_ID_L register	
		4b'0000	OTP_ID_L[3:0]
		4b'0001	
		4b'0010	
		4b'0011	
		4b'0100	
		4b'0101	
		4b'0110	
		4b'0111	
		4b'1000	
		4b'1001	
		4b'1010	
		4b'1011	
		4b'1100	
		4b'1101	
		4b'1110	
		4b'1111	
		Reset condition	OFF_OTP
3 to 0	PROG_ID_REV	4b'0000	OTP_ID_REV[3:0]
		4b'0001	
		4b'0010	
		4b'0011	
		4b'0100	
		4b'0101	
		4b'0110	
		4b'0111	
		4b'1000	
		4b'1001	
		4b'1010	
		4b'1011	
		4b'1100	
		4b'1101	
		4b'1110	
		4b'1111	
		Reset condition	OFF_OTP

16.4.5 INT_STATUS1

Table 142. INT_STATUS1 – Interrupt status 1 register (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	NOT USED	PGOOD_I	VIN_OVLO_I
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 143. INT_STATUS1 – Interrupt status 1 register (address 04h) bit description

Bit	Symbol	Description	
7	SDWN_I	Interrupt bit to indicate start of shutdown timer when PMIC_OFF bit is set	
		1b'0	No shutdown or bit cleared by writing
		1b'1	500 µs shutdown timer starts
		Reset condition	OFF_TOG
6	FREQ_RDY_I	Interrupt bit to indicate the settling of clock frequency change due to manual tuning	
		1b'0	No change or frequency not settled or bit cleared by writing
		1b'1	New clock frequency settled
		Reset condition	OFF_TOG
5	CRC_I	Interrupt bit to indicate I^{2}C CRC error	
		1b'0	No CRC error or bit cleared by writing
		1b'1	CRC error detected
		Reset condition	OFF_TOG
4	PWRUP_I	Interrupt bit to indicate a power up event completion	
		1b'0	No power up event or bit cleared by writing
		1b'1	Power up event completed (startup or Standby to Run transition)
		Reset condition	OFF_TOG
3	PWRDN_I	Interrupt bit to indicate completion of Run to Standby transition	
		1b'0	No transition event or bit cleared by writing
		1b'1	Run to Standby transition is completed
		Reset condition	OFF_TOG
1	PGOOD_I	PGOOD Interrupt bit to indicate PGOOD low assertion due to fault	
		1b'0	PGOOD not asserted low or bit cleared by writing
		1b'1	PGOOD asserted low
		Reset condition	OFF_TOG
0	VIN_OVLO_I	VIN Overvoltage Lockout Interrupt bit	
		1b'0	No VIN OVLO event or bit cleared by writing
		1b'1	VIN OVLO event
		Reset condition	OFF_TOG

16.4.6 INT_MASK1

Table 144. INT_MASK1 – Interrupt mask 1 register (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	NOT USED	PGOOD_M	VIN_OVLO_M
Reset	1	1	1	1	1	1	1	1
Access	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR

Table 145. INT_MASK1 – Interrupt mask 1 register (address 05h) bit description

Bit	Symbol	Description	
7	SDWN_M	Mask the SDWN_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
6	FREQ_RDY_M	Mask the FREQ_RDY_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
5	CRC_M	Mask the CRC_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
4	PWRUP_M	Mask the PWRUP_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
3	PWRDN_M	Mask the PWRDN_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
1	PGOOD_M	Mask the PGOOD_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	VIN_OVLO_M	Mask the VIN_OVLO_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.7 INT_SENSE1

Table 146. INT_SENSE1 – Interrupt sense 1 register (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	PWRON_S	NOT USED	NOT USED	PGOOD_S	VIN_OVLO_S
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 147. INT_SENSE1 – Interrupt sense 1 register (address 06h) bit description

Bit	Symbol	Description	
4	**PWRON_S**	Reports the real time status of PWRON pin	
		1b'0	PWRON low
		1b'1	PWRON high
		Reset condition	OFF_TOG

Table 147. INT_SENSE1 – Interrupt sense 1 register (address 06h) bit description*...continued*

Bit	Symbol	Description	
1	**PGOOD_S**	Reports the real time status of PGOOD pin	
		1b'0	PGOOD low
		1b'1	PGOOD high
		Reset condition	OFF_TOG
0	**VIN_OVLO_S**	Reports the real time status of VIN_OVLO event	
		1b'0	VIN_OVLO event not active
		1b'1	VIN_OVLO event active
		Reset condition	OFF_TOG

16.4.8 INT_STATUS2

Table 148. INT_STATUS2 – Interrupt status 2 register (address 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_EVENT_I	WD_ERROR_I	WD_INIT_I	REGMAP_CRC_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 149. INT_STATUS2 – Interrupt status 2 register (address 07h) bit description

Bit	Symbol	Description	
7	WD_EVENT_I	Interrupt bit to indicate a WD event	
		1b'0	No WD event or bit cleared by writing
		1b'1	WD event detected
		Reset condition	OFF_TOG
6	WD_ERROR_I	Interrupt bit to indicate WD error due to bad WD refresh	
		1b'0	No WD error or bit cleared by writing
		1b'1	WD error detected
		Reset condition	OFF_TOG
5	WD_INIT_I	Interrupt bit to indicate WD INIT timeout error	
		1b'0	Interrupt bit to indicate WD INIT timeout error
		1b'1	No WD INIT timeout or bit cleared by writing
		Reset condition	OFF_TOG
4	REGMAP_CRC_I	Interrupt bit to indicate regmap CRC error	
		1b'0	No CRC error or bit cleared by writing
		1b'1	CRC error detected
		Reset condition	OFF_TOG
3	THERM_155_I	Interrupt bit to indicate the temperature crossing the 155C threshold	
		1b'0	Temperature below threshold or bit cleared by writing
		1b'1	Temperature above threshold
		Reset condition	OFF_TOG

Table 149. INT_STATUS2 – Interrupt status 2 register (address 07h) bit description*...continued*

Bit	Symbol	Description	
2	THERM_140_I	Interrupt bit to indicate the temperature crossing the 140C threshold	
		1b'0	Temperature below threshold or bit cleared by writing
		1b'1	Temperature above threshold
		Reset condition	OFF_TOG
1	THERM_125_I	Interrupt bit to indicate the temperature crossing the 125C threshold	
		1b'0	Temperature below threshold or bit cleared by writing
		1b'1	Temperature above threshold
		Reset condition	OFF_TOG
0	THERM_110_I	Interrupt bit to indicate the temperature crossing the 110C threshold	
		1b'0	Temperature below threshold or bit cleared by writing
		1b'1	Temperature above threshold
		Reset condition	OFF_TOG

16.4.9 INT_MASK2

Table 150. INT_MASK2 – Interrupt mask 2 register (address 08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_EVENT_M	WD_ ERROR_M	WD_INIT_M	REGMAP_ CRC_M	THERM_ 155_M	THERM_ 140_M	THERM_ 125_M	THERM_ 110_M
Reset	1	1	1	1	1	1	1	1
Access	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR

Table 151. INT_MASK2 – Interrupt mask 2 register (address 08h) bit description

Bit	Symbol	Description	
7	WD_EVENT_M	Mask the WD_EVENT_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
6	WD_ERROR_M	Mask the WD_ERROR_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
5	WD_INIT_M	Mask the WD_INIT_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
4	REGMAP_CRC_M	Mask the REGMAP_CRC_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

Table 151. INT_MASK2 – Interrupt mask 2 register (address 08h) bit description*...continued*

Bit	Symbol	Description	
3	THERM_155_M	Mask the THERM_155_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
2	THERM_140_M	Mask the THERM_140_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
1	THERM_125_M	Mask the THERM_125_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	THERM_110_M	Mask the THERM_110_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.10 INT_SENSE2

Table 152. INT_SENSE2 – Interrupt sense 2 register (address 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 153. INT_SENSE2 – Interrupt sense 2 register (address 09h) bit descriptions

Bit	Symbol	Description	
3	THERM_155_S	Reports the status of real temperature relative to 155C threshold	
		1b'0	Temperature is below the threshold by hysteresis level (5C)
		1b'1	Temperature is above the threshold
		Reset condition	OFF_TOG
2	THERM_140_S	Reports the status of real temperature relative to 140C threshold	
		1b'0	Temperature is below the threshold by hysteresis level (5C)
		1b'1	Temperature is above the threshold
		Reset condition	OFF_TOG
1	THERM_125_S	Reports the status of real temperature relative to 125C threshold	
		1b'0	Temperature is below the threshold by hysteresis level (5C)
		1b'1	Temperature is above the threshold
		Reset condition	OFF_TOG

Table 153. INT_SENSE2 – Interrupt sense 2 register (address 09h) bit descriptions*...continued*

Bit	Symbol	Description	
0	THERM_110_S	Reports the status of real temperature relative to 110C threshold	
		1b'0	Temperature is below the threshold by hysteresis level (5C)
		1b'1	Temperature is above the threshold
		Reset condition	OFF_TOG

16.4.11 INT_STATUS3

Table 154. INT_STATUS3 – Interrupt status 3 register (address 0Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BGMON_I	FSYNC_I	FSYNC_FLT_I	CLK_MON_I	RSTB_I	FCCU_I	NOT USED	PG_SHORT_I
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 155. INT_STATUS3 – Interrupt status 3 register (address 0Ah) bit descriptions

Bit	Symbol	Description	
7	BGMON_I	Interrupt bit to indicate the BGMON error (drift b/w BG1 and BG2)	
		1b'0	No BG drift detected or bit cleared by writing
		1b'1	BG drift detected
		Reset condition	OFF_TOG
6	FSYNC_I	Interrupt bit to indicate the clock switchover between internal and external sources	
		1b'0	No clock switchover or bit cleared by writing
		1b'1	Clock switchover happens
		Reset condition	OFF_TOG
5	FSYNC_FLT_I	Interrupt bit to indicate the FSYNC fault (external clock invalid)	
		1b'0	No FSYNC fault or bit cleared by writing
		1b'1	FSYNC fault detected
		Reset condition	OFF_TOG
4	CLK_MON_I	Interrupt bit to indicate the 20 MHz OSC drift error during self-test	
		1b'0	No OSC error or bit cleared by writing
		1b'1	OSC drift error detected
		Reset condition	OFF_TOG
3	RSTB_I	Flag bit to indicate external RSTB event	
		1b'0	No external RSTB toggle detected
		1b'1	External RESET detected
		Reset condition	OFF_TOG
2	FCCU_I	Interrupt bit to indicate the FCCU error	
		1b'0	No FCCU error or bit cleared by writing
		1b'1	FCCU short detected
		Reset condition	OFF_TOG

Table 155. INT_STATUS3 – Interrupt status 3 register (address 0Ah) bit descriptions*...continued*

Bit	Symbol	Description	
0	PG_SHORT_I	Interrupt bit to indicate the PGOOD short to high fault	
		1b'0	No PGOOD short detected or bit cleared by writing
		1b'1	PGOOD short detected
		Reset condition	OFF_TOG

16.4.12 INT_MASK3

Table 156. INT_MASK3 – Interrupt mask 3 register (address 0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BGMON_M	FSYNC_M	FSYNC_FLT_M	CLK_MON_M	NOT USED	FCCU_M	NOT USED	PG_SHORT_M
Reset	1	1	1	1	0	1	1	1
Access	RWCLR	RWCLR	RWCLR	RWCLR	RO	RWCLR	RWCLR	RWCLR

Table 157. INT_MASK3 – Interrupt mask 3 register (address 0Bh) bit description

Bit	Symbol	Description	
7	BGMON_M	Mask the BGMON_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
6	FSYNC_M	Mask the FSYNC_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
5	FSYNC_FLT_M	Mask the FSYNC_FLT_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
4	CLK_MON_M	Mask the CLK_MON_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
2	FCCU_M	Mask the FCCU_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	PG_SHORT_M	Mask the PG_SHORT_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.13 INT_SENSE3

Table 158. INT_SENSE3 – Interrupt sense 3 register (address 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BGMON_S	FSYNC_S	FSYNC_FLT_S	NOT USED	RSTB_S	FCCU_S	NOT USED	NOT USED
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 159. INT_SENSE3 – Interrupt sense 3 register (address 0Ch) bit description

Bit	Symbol	Description	
7	BGMON_S	Reports real time status of BGMON fault (drift b/w BG1 and BG2)	
		1b'0	No BGMON fault
		1b'1	BGMON fault is active
		Reset condition	OFF_TOG
6	FSYNC_S	Reports real time status for the clock source	
		1b'0	Internal 20 MHz OSC used
		1b'1	External clock at SYNC pin used
		Reset condition	OFF_TOG
5	FSYNC_FLT_S	Reports the status of valid external clock at SYNC pin	
		1b'0	Clock watchdog detects a valid external clock (in range)
		1b'1	Clock watchdog detects an invalid external clock (out of range)
		Reset condition	OFF_TOG
3	RSTB_S	Reports real time status of RSTB pin	
		1b'0	RSTB low
		1b'1	RSTB high
		Reset condition	OFF_TOG
2	FCCU_S	Reports real time status of FCCU pin (when FCCU_CFG = 10)	
		1b'0	FCCU low
		1b'1	FCCU high
		Reset condition	OFF_TOG

16.4.14 SW_MODE_INT

Table 160. SW_MODE_INT – Switcher mode interrupt register (address 0Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 161. SW_MODE_INT – Switcher mode interrupt register (address 0Dh) bit descriptions

Bit	Symbol	Description	
2	SW3_MODE_I	Interrupt bit to indicate the change of switching mode for SW3 (OFF, PWM, PFM)	
		1b'0	No mode change detected or bit cleared by writing
		1b'1	Mode change detected
		Reset condition	OFF_TOG
1	SW2_MODE_I	Interrupt bit to indicate the change of switching mode for SW2 (OFF, PWM, PFM)	
		1b'0	No mode change detected or bit cleared by writing
		1b'1	Mode change detected
		Reset condition	OFF_TOG
0	SW1_MODE_I	Interrupt bit to indicate the change of switching mode for SW1 (OFF, PWM, PFM)	
		1b'0	No mode change detected or bit cleared by writing
		1b'1	Mode change detected
		Reset condition	OFF_TOG

16.4.15 SW_MODE_MASK

Table 162. SW_MODE_MASK – Switcher mode mask register (address 0Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	SW3_ MODE_M	SW2_ MODE_M	SW1_ MODE_M
Reset	0	0	0	0	0	1	1	1
Access	RO	RO	RO	RO	RO	RWCLR	RWCLR	RWCLR

Table 163. SW_MODE_MASK – Switcher mode mask register (address 0Eh) bit description

Bit	Symbol	Description	
2	SW3_MODE_M	Mask the SW3_MODE_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
1	SW2_MODE_M	Mask the SW2_MODE_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	SW1_MODE_M	Mask the SW1_MODE_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.16 REG_ILIM_INT

Table 164. REG_ILIM_INT – Regulator current limit interrupt register (address 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	LDO2_ILIM_I	LDO1_ILIM_I	NOT USED	NOT USED	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I

Table 164. REG_ILIM_INT – Regulator current limit interrupt register (address 0Fh) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Access	RO	FLGWC_CLR	FLGWC_CLR	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 165. REG_ILIM_INT – Regulator current limit interrupt register (address 0Fh) bit description

Bit	Symbol	Description	
6	LDO2_ILIM_I	Interrupt bit to indicate the status of ILIM fault of LDO2	
		1b'0	No ILIM fault detected or bit cleared by writing
		1b'1	ILIM fault detected
		Reset condition	OFF_TOG
5	LDO1_ILIM_I	Interrupt bit to indicate the status of ILIM fault of LDO1	
		1b'0	No ILIM fault detected or bit cleared by writing
		1b'1	ILIM fault detected
		Reset condition	OFF_TOG
2	SW3_ILIM_I	Interrupt bit to indicate the status of ILIM fault of SW3	
		1b'0	No ILIM fault detected or bit cleared by writing
		1b'1	ILIM fault detected
		Reset condition	OFF_TOG
1	SW2_ILIM_I	Interrupt bit to indicate the status of ILIM fault of SW2	
		1b'0	No ILIM fault detected or bit cleared by writing
		1b'1	ILIM fault detected
		Reset condition	OFF_TOG
0	SW1_ILIM_I	Interrupt bit to indicate the status of ILIM fault of SW1	
		1b'0	No ILIM fault detected or bit cleared by writing
		1b'1	ILIM fault detected
		Reset condition	OFF_TOG

16.4.17 REG_ILIM_MASK

Table 166. REG_ILIM_MASK – Regulator current limit mask register (address 10h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	LDO2_ILIM_M	LDO1_ILIM_M	NOT USED	NOT USED	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
Reset	0	1	1	0	0	1	1	1
Access	RO	RWCLR	RWCLR	RO	RO	RWCLR	RWCLR	RWCLR

Table 167. REG_ILIM_MASK – Regulator current limit mask register (address 10h) bit description

Bit	Symbol	Description	
5	LDO2_ILIM_M	Mask the LDO2_ILIM_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked

Table 167. REG_ILIM_MASK – Regulator current limit mask register (address 10h) bit description*...continued*

Bit	Symbol	Description	
		Reset condition	OFF_TOG
6	LDO1_ILIM_M	Mask the LDO1_ILIM_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
2	SW3_ILIM_M	Mask the SW3_ILIM_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
1	SW2_ILIM_M	Mask the SW2_ILIM_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	SW1_ILIM_M	Mask the SW1_ILIM_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.18 REG_ILIM_SENSE

Table 168. REG_ILIM_SENSE – Regulator current limit sense register (address 11h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	LDO2_ILIM_S	LDO1_ILIM_S	NOT USED	NOT USED	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 169. REG_ILIM_SENSE – Regulator current limit sense register (address 11h) bit description

Bit	Symbol	Description	
6	LDO2_ILIM_S	Reports real time status of LDO2 ILIM fault	
		1b'0	No LDO2 ILIM fault
		1b'1	LDO2 ILIM fault is active
		Reset condition	OFF_TOG
5	LDO1_ILIM_S	Reports real time status of LDO1 ILIM fault	
		1b'0	No LDO1 ILIM fault
		1b'1	LDO1 ILIM fault is active
		Reset condition	OFF_TOG
2	SW3_ILIM_S	Reports real time status of SW3 ILIM fault	
		1b'0	No SW3 ILIM fault
		1b'1	SW3 ILIM fault is active
		Reset condition	OFF_TOG

Table 169. REG_ILIM_SENSE – Regulator current limit sense register (address 11h) bit description*...continued*

Bit	Symbol	Description	
1	SW2_ILIM_S	Reports real time status of SW2 ILIM fault	
		1b'0	No SW2 ILIM fault
		1b'1	SW2 ILIM fault is active
		Reset condition	OFF_TOG
0	SW1_ILIM_S	Reports real time status of SW1 ILIM fault	
		1b'0	No SW1 ILIM fault
		1b'1	SW1 ILIM fault is active
		Reset condition	OFF_TOG

16.4.19 REG_UV_INT

Table 170. REG_UV_INT – Regulator undervoltage interrupt register (address 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_UV_I	LDO2_UV_I	LDO1_UV_I	NOT USED	NOT USED	SW3_UV_I	SW2_UV_I	SW1_UV_I
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 171. REG_UV_INT – Regulator undervoltage interrupt register (address 12h) bit description

Bit	Symbol	Description	
7	VIN_UV_I	Interrupt bit to indicate the status of UV fault of VIN	
		1b'0	No UV fault detected or bit cleared by writing
		1b'1	UV fault detected
		Reset condition	OFF_TOG
6	LDO2_UV_I	Interrupt bit to indicate the status of UV fault of LDO2	
		1b'0	No UV fault detected or bit cleared by writing
		1b'1	UV fault detected
		Reset condition	OFF_TOG
5	LDO1_UV_I	Interrupt bit to indicate the status of UV fault of LDO1	
		1b'0	No UV fault detected or bit cleared by writing
		1b'1	UV fault detected
		Reset condition	OFF_TOG
2	SW3_UV_I	Interrupt bit to indicate the status of UV fault of SW3	
		1b'0	No UV fault detected or bit cleared by writing
		1b'1	UV fault detected
		Reset condition	OFF_TOG
1	SW2_UV_I	Interrupt bit to indicate the status of UV fault of SW2	
		1b'0	No UV fault detected or bit cleared by writing
		1b'1	UV fault detected
		Reset condition	OFF_TOG
0	SW1_UV_I	Interrupt bit to indicate the status of UV fault of SW3	

Table 171. REG_UV_INT – Regulator undervoltage interrupt register (address 12h) bit description*...continued*

Bit	Symbol	Description	
		1b'0	No UV fault detected or bit cleared by writing
		1b'1	UV fault detected
		Reset condition	OFF_TOG

16.4.20 REG_UV_MASK

Table 172. REG_UV_MASK – Regulator undervoltage mask register (address 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_UV_M	LDO2_UV_M	LDO1_UV_M	NOT USED	NOT USED	SW3_UV_M	SW2_UV_M	SW1_UV_M
Reset	1	1	1	0	0	1	1	1
Access	RWCLR	RWCLR	RWCLR	RO	RO	RWCLR	RWCLR	RWCLR

Table 173. REG_UV_MASK – Regulator undervoltage mask register (address 13h) bit description

Bit	Symbol	Description	
7	VIN_UV_M	Mask the VIN_UV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
6	LDO2_UV_M	Mask the LDO2_UV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
5	LDO1_UV_M	Mask the LDO1_UV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
2	SW3_UV_M	Mask the SW3_UV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
1	SW2_UV_M	Mask the SW2_UV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	SW1_UV_M	Mask the SW1_UV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.21 REG_UV_SENSE

Table 174. REG_UV_SENSE – Regulator undervoltage sense register (address 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_UV_S	LDO2_UV_S	LDO1_UV_S	NOT USED	NOT USED	SW3_UV_S	SW2_UV_S	SW1_UV_S
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 175. REG_UV_SENSE – Regulator undervoltage sense register (address 14h) bit description

Bit	Symbol	Description	
7	VIN_UV_S	Reports real time status of VIN UV fault	
		1b'0	No VIN UV fault
		1b'1	VIN UV fault is active
		Reset condition	OFF_TOG
6	LDO2_UV_S	Reports real time status of LDO2UV fault	
		1b'0	No LDO2UV fault
		1b'1	LDO2 UV fault is active
		Reset condition	OFF_TOG
5	LDO1_UV_S	Reports real time status of LDO1 UV fault	
		1b'0	No LDO1 UV fault
		1b'1	LDO1 UV fault is active
		Reset condition	OFF_TOG
2	SW3_UV_S	Reports real time status of SW3 UV fault	
		1b'0	No SW3 UV fault
		1b'1	SW3 UV fault is active
		Reset condition	OFF_TOG
1	SW2_UV_S	Reports real time status of SW2 UV fault	
		1b'0	No SW2 UV fault
		1b'1	SW2 UV fault is active
		Reset condition	OFF_TOG
0	SW1_UV_S	Reports real time status of SW1 UV fault	
		1b'0	No SW1 UV fault
		1b'1	SW1 UV fault is active
		Reset condition	OFF_TOG

16.4.22 REG_OV_INT

Table 176. REG_OV_INT – Regulator overvoltage interrupt register (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_OV_I	LDO2_OV_I	LDO1_OV_I	NOT USED	NOT USED	SW3_OV_I	SW2_OV_I	SW1_OV_I
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 177. REG_OV_INT – Regulator overvoltage interrupt register (address 15h) bit description

Bit	Symbol	Description	
7	VIN_OV_I	**Interrupt bit to indicate the status of OV fault of VIN**	
		1b'0	No OV fault detected or bit cleared by writing
		1b'1	OV fault detected
		Reset condition	OFF_TOG
6	LDO2_OV_I	Interrupt bit to indicate the status of OV fault of LDO2	
		1b'0	No OV fault detected or bit cleared by writing
		1b'1	OV fault detected
		Reset condition	OFF_TOG
5	LDO1_OV_I	Interrupt bit to indicate the status of OV fault of LDO1	
		1b'0	No OV fault detected or bit cleared by writing
		1b'1	OV fault detected
		Reset condition	OFF_TOG
2	SW3_OV_I	Interrupt bit to indicate the status of OV fault of SW3	
		1b'0	No OV fault detected or bit cleared by writing
		1b'1	OV fault detected
		Reset condition	OFF_TOG
1	SW2_OV_I	Interrupt bit to indicate the status of OV fault of SW2	
		1b'0	No OV fault detected or bit cleared by writing
		1b'1	OV fault detected
		Reset condition	OFF_TOG
0	SW1_OV_I	Interrupt bit to indicate the status of OV fault of SW1	
		1b'0	No OV fault detected or bit cleared by writing
		1b'1	OV fault detected
		Reset condition	OFF_TOG

16.4.23 REG_OV_MASK

Table 178. REG_OV_MASK – Regulator overvoltage mask register (address 16h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_OV_M	LDO2_OV_M	LDO1_OV_M	NOT USED	NOT USED	SW3_OV_M	SW2_OV_M	SW1_OV_M
Reset	1	1	1	0	1	1	1	1
Access	RWCLR	RWCLR	RWCLR	RO	RO	RWCLR	RWCLR	RWCLR

Table 179. REG_OV_MASK – Regulator overvoltage mask register (address 16h) bit description

Bit	Symbol	Description	
7	VIN_OV_M	Mask the VIN_OV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

Table 179. REG_OV_MASK – Regulator overvoltage mask register (address 16h) bit description...*continued*

Bit	Symbol	Description	
6	LDO2_OV_M	Mask the LDO2_OV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
5	LDO1_OV_M	Mask the LDO1_OV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
2	SW3_OV_M	Mask the SW3_OV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
1	SW2_OV_M	Mask the SW2_OV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG
0	SW1_OV_M	Mask the SW1_OV_I interrupt	
		1b'0	Interrupt unmasked
		1b'1	Interrupt masked
		Reset condition	OFF_TOG

16.4.24 REG_OV_SENSE

Table 180. REG_OV_SENSE – Regulator overvoltage sense register (address 17h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_OV_S	LDO2_OV_S	LDO1_OV_S	NOT USED	NOT USED	SW3_OV_S	SW2_OV_S	SW1_OV_S
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 181. REG_OV_SENSE – Regulator overvoltage sense register (address 17h) bit description

Bit	Symbol	Description	
7	VIN_OV_S	Reports real time status of VIN OV fault	
		1b'0	No VIN OV fault
		1b'1	VIN OV fault is active
		Reset condition	OFF_TOG
6	LDO2_OV_S	Reports real time status of LDO2 OV fault	
		1b'0	No LDO2 OV fault
		1b'1	LDO2 OV fault is active
		Reset condition	OFF_TOG
5	LDO1_OV_S	Reports real time status of LDO1 OV fault	
		1b'0	No LDO1 OV fault
		1b'1	LDO1 OV fault is active
		Reset condition	OFF_TOG

Table 181. REG_OV_SENSE – Regulator overvoltage sense register (address 17h) bit description*...continued*

Bit	Symbol	Description	
2	SW3_OV_S	Reports real time status of SW3 OV fault	
		1b'0	No SW3 OV fault
		1b'1	SW3 OV fault is active
		Reset condition	OFF_TOG
1	SW2_OV_S	Reports real time status of SW2 OV fault	
		1b'0	No SW2 OV fault
		1b'1	SW2 OV fault is active
		Reset condition	OFF_TOG
0	SW1_OV_S	Reports real time status of SW1 OV fault	
		1b'0	No SW1 OV fault
		1b'1	SW1 OV fault is active
		Reset condition	OFF_TOG

16.4.25 SYS_INT

Table 182. SYS_INT – System interrupt register (address 18h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	STATUS3_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 183. SYS_INT – System interrupt register (address 18h) bit description

Bit	Symbol	Description	
6	STATUS3_I	Interrupt bit to indicate the status of STATUS3_I interrupts	
		1b'0	No STATUS3 interrupt is set or bit cleared by writing
		1b'1	STATUS3 interrupt is set
		Reset condition	OFF_TOG
5	OV_I	Interrupt bit to indicate the status of OV_I interrupts	
		1b'0	No OV interrupt is set or bit cleared by writing
		1b'1	One of the OV interrupts is set
		Reset condition	OFF_TOG
4	UV_I	Interrupt bit to indicate the status of UV_I interrupts	
		1b'0	No UV interrupt is set or bit cleared by writing
		1b'1	One of the UV interrupts is set
		Reset condition	OFF_TOG
3	ILIM_I	Interrupt bit to indicate the status of ILIM_I interrupts	
		1b'0	No ILIM interrupt is set or bit cleared by writing
		1b'1	One of the ILIM interrupts is set
		Reset condition	OFF_TOG
2	MODE_I	Interrupt bit to indicate the status of MODE_I interrupts	
		1b'0	No MODE interrupt is set or bit cleared by writing

Table 183. SYS_INT – System interrupt register (address 18h) bit description*...continued*

Bit	Symbol	Description	
		1b'1	One of the MODE interrupts is set
		Reset condition	OFF_TOG
1	STATUS2_I	Interrupt bit to indicate the status of STATUS2_I interrupts	
		1b'0	No STATUS2 interrupt is set or bit cleared by writing
		1b'1	STATUS2 interrupt is set
		Reset condition	OFF_TOG
0	STATUS1_I	Interrupt bit to indicate the status of STATUS1_I interrupts	
		1b'0	No STATUS1 interrupt is set or bit cleared by writing
		1b'1	STATUS1 interrupt is set
		Reset condition	OFF_TOG

16.4.26 HARDFAULT_FLAGS

Table 184. HARDFAULT_FLAGS – Hard fault flags register (address 19h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	PU_FAIL	PG_FAIL	REG_FAIL	TSD_FAIL
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 185. HARDFAULT_FLAGS – Hard fault flags register (address 19h) bit description

Bit	Symbol	Description	
3	PU_FAIL	Flag bit to indicate device shutdown due to power up fault	
		1b'0	No PU_FAIL event or bit cleared by writing
		1b'1	Shutdown caused by PU_FAIL event (power up failure)
		Reset condition	UVDET
2	PG_FAIL	Flag bit to indicate device shutdown due to PGOOD fault	
		1b'0	No PG_FAIL event or bit cleared by writing
		1b'1	Shutdown caused by PG_FAIL event
		Reset condition	UVDET
1	REG_FAIL	Flag bit to indicate device shutdown due to regulator fault	
		1b'0	No REG_FAIL event or bit cleared by writing
		1b'1	Shutdown caused by REG_FAIL event (fault count maximum)
		Reset condition	UVDET
0	TSD_FAIL	Flag bit to indicate device shutdown due to TSD fault	
		1b'0	No TSD event or bit cleared by writing
		1b'1	Shutdown caused by TSD event
		Reset condition	UVDET

16.4.27 ABIST_CTRL

Table 186. ABIST_CTRL – Analog built-in self-test control register (address 1Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	AB_FCCU_H	AB_DONE	AB_RUN
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	FLGWC_CLR	RO	RWCLR

Table 187. ABIST_CTRL – Analog built-in self-test control register (address 1Bh) bit description

Bit	Symbol	Description	
2	AB_FCCU_H	Flag bit to indicate the status of FCCU short to high test at startup	
		1b'0	No FCCU short fault or bit cleared by writing
		1b'1	FCCU short to high fault
		Reset condition	OFF_TOG
1	AB_DONE	Status bit to report the status of completion of ABIST	
		1b'0	ABIST not started or not completed
		1b'1	ABIST completed
		Reset condition	OFF_TOG
0	AB_RUN	Control bit enable the ABIST on demand or AB_RUN feature	
		1b'0	On-demand ABIST not requested or bit self cleared
		1b'1	Run on-demand ABIST
		Reset condition	Self Clear

16.4.28 ABIST_OV

Table 188. ABIST_OV – Analog built-in self-test overvoltage register (address 1Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AB_VIN_OV	AB_LDO2_OV	AB_LDO1_OV	NOT USED	NOT USED	AB_SW3_OV	AB_SW2_OV	AB_SW1_OV
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 189. ABIST_OV – Analog built-in self-test overvoltage register (address 1Ch) bit description

Bit	Symbol	Description	
7	AB_VIN_OV	Flag bit to indicate the status of VIN ABIST OV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in VIN OV comparator
		Reset condition	UVDET
6	AB_LDO2_OV	Flag bit to indicate the status of LDO2 ABIST OV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in LDO2 OV comparator
		Reset condition	UVDET
5	AB_LDO1_OV	Flag bit to indicate the status of LDO1 ABIST OV failure	

Table 189. ABIST_OV – Analog built-in self-test overvoltage register (address 1Ch) bit description*...continued*

Bit	Symbol	Description	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in LDO1 OV comparator
		Reset condition	UVDET
2	AB_SW3_OV	Flag bit to indicate the status of SW3 ABIST OV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in SW3 OV comparator
		Reset condition	UVDET
1	AB_SW2_OV	Flag bit to indicate the status of SW2 ABIST OV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in SW2 OV comparator
		Reset condition	UVDET
0	AB_SW1_OV	Flag bit to indicate the status of SW1 ABIST OV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in SW1 OV comparator
		Reset condition	UVDET

16.4.29 ABIST_UV

Table 190. ABIST_UV – Analog built-in self-test undervoltage register (address 1Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AB_VIN_UV	AB_LDO2_UV	AB_LDO1_UV	NOT USED	NOT USED	AB_SW3_UV	AB_SW2_UV	AB_SW1_UV
Reset	0	0	0	0	0	0	0	0
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	RO	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 191. ABIST_UV – Analog built-in self-test undervoltage register (address 1Dh) bit description

Bit	Symbol	Description	
7	AB_VIN_UV	Flag bit to indicate the status of VIN ABIST UV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in VIN UV comparator
		Reset condition	UVDET
6	AB_LDO2_UV	Flag bit to indicate the status of LDO2 ABIST UV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in UV comparator
		Reset condition	UVDET
5	AB_LDO1_UV	Flag bit to indicate the status of LDO1 ABIST UV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in LDO1 UV comparator
		Reset condition	UVDET

Table 191. ABIST_UV – Analog built-in self-test undervoltage register (address 1Dh) bit description*...continued*

Bit	Symbol	Description	
2	AB_SW3_UV	Flag bit to indicate the status of SW3 ABIST UV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in SW3 UV comparator
		Reset condition	UVDET
1	AB_SW2_UV	Flag bit to indicate the status of SW2 ABIST UV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in SW2 UV comparator
		Reset condition	UVDET
0	AB_SW1_UV	Flag bit to indicate the status of SW1 ABIST UV failure	
		1b'0	No ABIST fault or bit cleared by writing
		1b'1	ABIST fault detected in SW1 UV comparator
		Reset condition	UVDET

16.4.30 TEST_FLAGS

Table 192. TEST_FLAGS – Test flags register (address 1Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	RESERVED	RESERVED	STEST_NOK	TRIM_NOK	OTP_NOK
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 193. TEST_FLAGS – Test flags register (address 1Eh) bit description

Bit	Symbol	Description	
2	STEST_NOK	Flag bit to indicate the status of Self Test failure	
		1b'0	No STEST failure
		1b'1	STEST failure detected
		Reset condition	OFF_TOG
1	TRIM_NOK	Flag bit to indicate the status of TRIM fuse loading failure	
		1b'0	No TRIM_NOK fault
		1b'1	TRIM_NOK fault detected (TRIM fuse loading error)
		Reset condition	OFF_TOG
0	OTP_NOK	Flag bit to indicate the status of OTP fuse loading error	
		1b'0	No OTP_NOK fault
		1b'1	OTP_NOK fault detected (OTP fuse loading error)
		Reset condition	OFF_TOG

16.4.31 RANDOM_GEN

Table 194. RANDOM_GEN – Random code generation register (address 21h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RANDOM_GEN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 195. RANDOM_GEN – Random code generation register (address 21h) bit description

Bit	Symbol	Description	
7 to 0	RANDOM_GEN[7:0	Random code generation register for secure write feature	
		Reset condition	Self clear

16.4.32 RANDOM_CHK

Table 196. RANDOM_CHK – Random code generation register (address 21h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RANDOM_CHK[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW

Table 197. RANDOM_CHK – Random code generation register (address 21h) bit description

Bit	Symbol	Description	
7 to 0	RANDOM_CHK[7:0	Random code verification register for secure write feature	
		Reset condition	Self clear

16.4.33 VMONEN1

Table 198. VMONEN1 – Voltage monitor enable 1 register (address 22h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	LDO2 VMON_EN	LDO1 VMON_EN	NOT USED	NOT USED	SW3 VMON_EN	SW2 VMON_EN	SW1 VMON_EN
Reset	0	1	1	0	0	1	1	1
Access	RO	RWCLR	RWCLR	RO	RO	RWCLR	RWCLR	RWCLR

Table 199. VMONEN1 – Voltage monitor enable 1 register (address 22h) bit description

Bit	Symbol	Description	
6	LDO2VMON_EN	Control bit to enable the LDO2 VMON	
		1b'0	LDO2 VMON is disabled
		1b'1	LDO2 VMON is enabled
		Reset condition	UVDET
5	LDO1VMON_EN	Control bit to enable the LDO1 VMON	
		1b'0	LDO1 VMON is disabled

Table 199. VMONEN1 – Voltage monitor enable 1 register (address 22h) bit description*...continued*

Bit	Symbol	Description	
		1b'1	LDO1 VMON is enabled
		Reset condition	UVDET
2	SW3VMON_EN	Control bit to enable the SW3 VMON	
		1b'0	SW3 VMON is disabled
		1b'1	SW3 VMON is enabled
		Reset condition	UVDET
1	SW2VMON_EN	Control bit to enable the SW2 VMON	
		1b'0	SW2 VMON is disabled
		1b'1	SW2 VMON is enabled
		Reset condition	UVDET
0	SW1VMON_EN	Control bit to enable the SW1 VMON	
		1b'0	SW1 VMON is disabled
		1b'1	SW1 VMON is enabled
		Reset condition	UVDET

16.4.34 CTRL1

Table 200. CTRL1 – Control 1 register (address 23h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_OVLO_EN	VIN_OVLO_SDWN	SYNC_EN	TMP_MON_EN	WD_SEL	WD_STBY_EN	WD_EN	I2C_SECURE_EN
Reset	0	0	0	1	0	0	0	0
Access	RWOTP	RWOTP	RWOTP	RW	RWOTP	RWOTP	RWOTP	RWOTP

Table 201. CTRL1 – Control 1 register (address 23h) bit description

Bit	Symbol	Description	
7	VIN_OVLO_EN	Control bit to enable/disable the VIN OVLO monitor	
		1b'0	VIN OVLO monitor disabled
		1b'1	VIN OVLO monitor enabled
		Reset condition	OFF_OTP
6	VIN_OVLO_SDWN	Control bit to configure the response up on VIN OVLO event	
		1b'0	VIN OVLO doesn't initiate power down but sets an interrupt
		1b'1	VIN OVLO initiates power down
		Reset condition	OFF_OTP
5	SYNC_EN	Control bit to enable/disable the external clock synchronization feature	
		1b'0	CLK sync disabled
		1b'1	CLK sync enabled
		Reset condition	OFF_OTP
4	TMP_MON_EN	Control bit to enable/disable the temperature monitor	
		1b'0	Temperature monitor disabled
		1b'1	Temperature monitor enabled
		Reset condition	UVDET
3	WD_SEL	Control bit to select the watchdog type	

Table 201. CTRL1 – Control 1 register (address 23h) bit description*...continued*

Bit	Symbol	Description	
		1b'0	Simple watchdog
		1b'1	Reserved
		Reset condition	OFF_OTP
2	WD_STBY_EN	Control bit to enable/disable the watchdog feature in Standby state	
		1b'0	Watchdog disabled
		1b'1	Watchdog enabled
		Reset condition	OFF_OTP
1	WD_EN	Control bit to enable/disable the watchdog feature	
		1b'0	Watchdog disabled
		1b'1	Watchdog enabled
		Reset condition	OFF_OTP
0	I2C_SECURE_EN	Control bit to enable/disable the I^2C secure write feature	
		1b'0	Secure write disabled
		1b'1	Secure write enabled
		Reset condition	OFF_OTP

16.4.35 CTRL2

Table 202. CTRL2 – Control 2 register (address 24h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VIN_OVLO_DBNC[1:0]		NOT USED	TMP_ MON_AON	NOT USED	STANDBYINV	NOT USED	NOT USED
Reset	0	0	0	1	0	0	0	0
Access	RWOTP	RWOTP	RO	RW	RO	RWOTP	RO	RO

Table 203. CTRL2 – Control 2 register (address 24h) bit description

Bit	Symbol	Description	
7 to 6	VIN_OVLO_DBNC[1:0	Control bit to configure the VIN OVLO fault debounce value	
		2b'00	10 µs
		2b'01	100 µs
		2b'10	1000 µs
		2b'11	Reserved
		Reset condition	OFF_OTP
4	TMP_MON_AON	Control bit to enable/disable the temperature monitor always on feature	
		1b'0	Temperature monitor sampling mode is enabled
		1b'1	Temperature monitor is always enabled
		Reset condition	UVDET
2	STANDBYINV	Control bit to configure the Standby mode entry/exit (Inversion of Standby pin)	
		1b'0	Not in Standby (if STBY pin = low) / In Standby (if STBY pin = high)
		1b'1	Not in Standby (if STBY pin = high) / In Standby (if STBY pin = low)
		Reset condition	OFF_OTP

16.4.36 CTRL3

Table 204. CTRL3 – Control 3 register (address 25h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	OV_DB[1:0]		UV_DB[1:0]		PGOOD_RLS	ULP_OFF_CTRL	PMIC_OFF	INTB_TEST
Reset	1	0	1	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RWCLR	RWCLR

Table 205. CTRL3 – Control 3 register (address 25h) bit description

Bit	Symbol	Description	
7 to 6	OV_DB[1:0]	Bits to configure overvoltage detection debounce time	
		2b'00	5 µs
		2b'01	15 µs
		2b'10	30 µs
		2b'11	40 µs
		Reset condition	OFF_TOG
5 to 4	UV_DB[1:0]	Bits to configure undervoltage detection debounce time	
		2b'00	5 µs
		2b'01	15 µs
		2b'10	30 µs
		2b'11	40 µs
		Reset condition	OFF_TOG
3	PGOOD_RLS	Control bit to release/control the PGOOD pin (only in companion mode)	
		1b'0	PGOOD remains low or asserts low
		1b'1	PGOOD is de-asserted or released
		Reset condition	OFF_TOG
2	ULP_OFF_CTRL	Control bit to select the transition to the ULP_Off state when PWRON pin goes low	
		1b'0	Device transitions to LP_Off state (when PWRON=0)
		1b'1	Device transitions to ULP_Off state (when PWRON=0)
		Reset condition	OFF_TOG
1	PMIC_OFF	Control bit to request a turn off the device after a 500 µs delay	
		1b'0	No PMIC turn off requested or bit self cleared
		1b'1	Device starts a 500 µs timer and shuts down after the timer expires
		Reset condition	Self clear
0	INTB_TEST	Control bit to perform real time test of the INTB pin	
		1b'0	No INTB test or bit self cleared
		1b'1	INTB toggles low for 100 µs and returns to normal state
		Reset condition	Self clear

16.4.37 PWRUP_CTRL

Table 206. PWRUP_CTRL – Power-up control register (address 26h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PGOOD_SEQ[5:0]						SEQ_TBASE[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 207. PWRUP_CTRL – Power-up control register (address 26h) bit description

Bit	Symbol	Description	
7 to 2	PGOOD_SEQ[5:0]	Bits to configure the power up/down slot sequence of PGOOD	
		6b'000000	OFF
		6b'000001	Slot 0
		6b'000010	Slot 1
		6b'000011	Slot 2
		6b'000100	Slot 3
		6b'000101	Slot 4
		6b'000110	Slot 5
		6b'000111	Slot 6
		6b'001000	Slot 7
		6b'001001	Slot 8
		6b'001010	Slot 9
		6b'001011	Slot 10
		6b'001100	Slot 11
		6b'001101	Slot 12
		6b'001110	Slot 13
		6b'001111	Slot 14
		6b'010000	Slot 15
		6b'010001	Slot 16
		6b'010010	Slot 17
		6b'010011	Slot 18
		6b'010100	Slot 19
		6b'010101	Slot 20
		6b'010110	Slot 21
		6b'010111	Slot 22
		6b'011000	Slot 23
		6b'011001	Slot 24
		6b'011010	Slot 25
		6b'011011	Slot 26
		6b'011100	Slot 27
		6b'011101	Slot 28
		6b'011110	Slot 29
		6b'011111	Slot 30
		6b'100000	Slot 31
		6b'100001	Slot 32
		6b'100010	Slot 33

Table 207. PWRUP_CTRL – Power-up control register (address 26h) bit description*...continued*

Bit	Symbol	Description	
		6b'100011	Slot 34
		6b'100100	Slot 35
		6b'100101	Slot 36
		6b'100110	Slot 37
		6b'100111	Slot 38
		6b'101000	Slot 39
		6b'101001	Slot 40
		6b'101010	Slot 41
		6b'101011	Slot 42
		6b'101100	Slot 43
		6b'101101	Slot 44
		6b'101110	Slot 45
		6b'101111	Slot 46
		6b'110000	Slot 47
		6b'110001	Slot 48
		6b'110010	Slot 49
		6b'110011	Slot 50
		6b'110100	Slot 51
		6b'110101	Slot 52
		6b'110110	Slot 53
		6b'110111	Slot 54
		6b'111000	Slot 55
		6b'111001	Slot 56
		6b'111010	Slot 57
		6b'111011	Slot 58
		6b'111100	Slot 59
		6b'111101	Slot 60
		6b'111110	Slot 61
		6b'111111	Slot 62
		Reset condition	OFF_OTP
1 to 0	SEQ_TBASE[1:0]	Bits to configure the time base of each slot of the sequencer	
		2b'00	100 µs
		2b'01	250 µs
		2b'10	500 µs
		2b'11	1000 µs
		Reset condition	OFF_OTP

16.4.38 FREQ_CTRL

Table 208. FREQ_CTRL – Power-up control register (address 26h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FSS_SEL	FSYNC_ RANGE	FSS_EN	FSS_FMOD	CLK_FREQ[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RWOTP	RWOTP	RWOTP	RW	RWOTP	RWOTP	RWOTP	RWOTP

Table 209. FREQ_CTRL – Power-up control register (address 26h) bit description

Bit	Symbol	Description	
7	FSS_SEL	Control bits to select the type of frequency spread spectrum modulation	
		1b'0	Triangular modulation
		1b'1	Pseudo-random modulation
		Reset condition	OFF_OTP
6	FSYNC_RANGE	Control bits to configure the external clock sync frequency range	
		1b'0	Between 2.2 MHz and 2.8 MHz
		1b'1	Between 17.55 MHz and 22.46 MHz
		Reset condition	OFF_OTP
5	FSS_EN	Control bits to enable/disable the frequency spread spectrum feature (FSS)	
		1b'0	FSS disabled
		1b'1	FSS enabled
		Reset condition	OFF_OTP
4	FSS_FMOD	Control bits to configure the frequency spread spectrum period for triangular modulation	
		1b'0	23.5 KHz
		1b'1	Reserved
		Reset condition	OFF_OTP
3 to 0	CLK_FREQ[3:0]	Control bits to configure the frequency of the main oscillator (manual tuning)	
		4b'0000	20 MHz
		4b'0001	21 MHz
		4b'0010	22 MHz
		4b'0011	Reserved
		4b'0100	Reserved
		4b'0101	Reserved
		4b'0110	Reserved
		4b'0111	Reserved
		4b'1000	Reserved
		4b'1001	Reserved
		4b'1010	Reserved
		4b'1011	18 MHz
		4b'1100	19 MHz
		4b'1101	Reserved
		4b'1110	Reserved
		4b'1111	Reserved
		Reset condition	OFF_OTP

16.4.39 GPO_CTRL

Table 210. GPO_CTRL – General purpose output control register (address 28h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	GPO_SEQ[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 211. GPO_CTRL – General purpose output control register (address 28h) bit description

Bit	Symbol	Description	
5 to 0	GPO_SEQ[5:0]	Bits to configure the power up/down slot sequence of GPO	
		6b'000000	OFF
		6b'000001	Slot 0
		6b'000010	Slot 1
		6b'000011	Slot 2
		6b'000100	Slot 3
		6b'000101	Slot 4
		6b'000110	Slot 5
		6b'000111	Slot 6
		6b'001000	Slot 7
		6b'001001	Slot 8
		6b'001010	Slot 9
		6b'001011	Slot 10
		6b'001100	Slot 11
		6b'001101	Slot 12
		6b'001110	Slot 13
		6b'001111	Slot 14
		6b'010000	Slot 15
		6b'010001	Slot 16
		6b'010010	Slot 17
		6b'010011	Slot 18
		6b'010100	Slot 19
		6b'010101	Slot 20
		6b'010110	Slot 21
		6b'010111	Slot 22
		6b'011000	Slot 23
		6b'011001	Slot 24
		6b'011010	Slot 25
		6b'011011	Slot 26
		6b'011100	Slot 27
		6b'011101	Slot 28
		6b'011110	Slot 29
		6b'011111	Slot 30
		6b'100000	Slot 31
		6b'100001	Slot 32
		6b'100010	Slot 33
		6b'100011	Slot 34
		6b'100100	Slot 35
		6b'100101	Slot 36
		6b'100110	Slot 37
		6b'100111	Slot 38
		6b'101000	Slot 39
		6b'101001	Slot 40
		6b'101010	Slot 41

Table 211. GPO_CTRL – General purpose output control register (address 28h) bit description*...continued*

Bit	Symbol	Description	
		6b'101011	Slot 42
		6b'101100	Slot 43
		6b'101101	Slot 44
		6b'101110	Slot 45
		6b'101111	Slot 46
		6b'110000	Slot 47
		6b'110001	Slot 48
		6b'110010	Slot 49
		6b'110011	Slot 50
		6b'110100	Slot 51
		6b'110101	Slot 52
		6b'110110	Slot 53
		6b'110111	Slot 54
		6b'111000	Slot 55
		6b'111001	Slot 56
		6b'111010	Slot 57
		6b'111011	Slot 58
		6b'111100	Slot 59
		6b'111101	Slot 60
		6b'111110	Slot 61
		6b'111111	Slot 62
		Reset condition	OFF_OTP

16.4.40 WD_CONFIG

Table 212. WD_CONFIG – Watchdog configuration register (address 29h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WDW_RECOVERY[3:0]				WD_DURATION[3:0]			
Reset	0	1	1	0	0	0	0	0
Access	RWCLR	RWCLR	RWCLR	RWCLR	RWOTP	RWOTP	RWOTP	RWOTP

Table 213. WD_CONFIG – Watchdog configuration register (address 29h) bit description

Bit	Symbol	Description	
7 to 4	WDW_ RECOVERY[3:0]	Bits to configure the watchdog recovery timer duration	
		4b'0000	1 ms
		4b'0001	2 ms
		4b'0010	4 ms
		4b'0011	8 ms
		4b'0100	16 ms
		4b'0101	32 ms
		4b'0110	64 ms
		4b'0111	128 ms
		4b'1000	256 ms
		4b'1001	512 ms
		4b'1010	1024 ms
		4b'1011	2048 ms
		4b'1100	4096 ms
		4b'1101	8192 ms
		4b'1110	16384 ms
		4b'1111	32768 ms
		Reset condition	OFF_TOG
3 to 0	WD_DURATION[3:0]]	Bits to configure the watchdog timer duration	
		4b'0000	1 ms
		4b'0001	2 ms
		4b'0010	4 ms
		4b'0011	8 ms
		4b'0100	16 ms
		4b'0101	32 ms
		4b'0110	64 ms
		4b'0111	128 ms
		4b'1000	256 ms
		4b'1001	512 ms
		4b'1010	1024 ms
		4b'1011	2048 ms
		4b'1100	4096 ms
		4b'1101	8192 ms
		4b'1110	16384 ms
		4b'1111	32768 ms
		Reset condition	OFF_TOG

16.4.41 WD_ANSWER

Table 214. WD_ANSWER – Watchdog answer register (address 2Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_ANSWER[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW

Table 215. WD_ANSWER – Watchdog answer register (address 2Ah) bit description

Bit	Symbol	Description	
7 to 0	WD_ANSWER[7:0]	Register to write the correct WD answer within the valid WD time	
		0x5B (Simple WD) or bitwise inversion of WD_SEED (Challenger WD)	
		Reset condition	OFF_TOG

16.4.42 WD_SEED

Table 216. WD_SEED – Watchdog seed register (address 2Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_SEED[7:0]							
Reset	0	1	0	1	1	0	1	1
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 217. WD_SEED – Watchdog seed register (address 2Bh) bit description

Bit	Symbol	Description	
7 to 0	WD_SEED[7:0	Register to access the WD seed	
		0x5B (Simple WD)	
		Reset condition	OFF_TOG

16.4.43 WD_ERROR

Table 218. WD_ERROR – Watchdog error register (address 2Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	WD_MAX_ERROR[1:0]		WD_ERROR_CNT[3:0]			
Reset	0	0	1	1	0	0	0	0
Access	RO	RO	RWOTP	RWOTP	RO	RO	RO	RO

Table 219. WD_ERROR – Watchdog error register (address 2Ch) bit description

Bit	Symbol	Description	
5 to 4	WD_MAX_ERROR[1:0]	Bits to configure the watchdog max error value	
		2b'00	8
		2b'01	6
		2b'10	4
		2b'11	2
		Reset condition	OFF_OTP

Table 219. WD_ERROR – Watchdog error register (address 2Ch) bit description *...continued*

Bit	Symbol	Description	
3 to 0	WD_ERROR_CNT[3:0]	Bits to access the WD error count	
		4b'0000	0
		4b'0001	1
		4b'0010	2
		4b'0011	3
		4b'0100	4
		4b'0101	5
		4b'0110	6
		4b'0111	7
		4b'1000	8
		4b'1001	Reserved
		4b'1010	Reserved
		4b'1011	Reserved
		4b'1100	Reserved
		4b'1101	Reserved
		4b'1110	Reserved
		4b'1111	Reserved
		Reset condition	OFF_TOG

16.4.44 ASIL_CFG

Table 220. ASIL_CFG – ASIL configuration register (address 2Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	FCCU_POL	FCCU_CFG[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RWCLR	RWCLR	RWCLR	RWCLR

Table 221. ASIL_CFG – ASIL configuration register (address 2Dh) bit description

Bit	Symbol	Description	
2	FCCU_POL	Bits to configure the polarity of FCCU detection when FCCU_CFG=10	
		1b'0	FCCU = 0 is a fault
		1b'1	FCCU = 1 is a fault
		Reset condition	OFF_TOG
1 to 0	FCCU_CFG[1:0]]	Bits to configure the FCCU monitoring feature	
		2b'00	FCCU monitoring disabled
		2b'01	FCCU monitoring enabled with PWM detection
		2b'10	FCCU monitoring enabled with single input level detection
		2b'11	Reserved
		Reset condition	OFF_TOG

16.4.45 FAULT_COUNTER

Table 222. FAULT_COUNTER – Fault counter register (address 2Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	FAULT_MAX_CNT[2:0]			FAULT_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RO	RWOTP	RWOTP	RWOTP	EXTRW	EXTRW	EXTRW	EXTRW

Table 223. FAULT_COUNTER – Fault counter register (address 2Eh) bit description

Bit	Symbol	Description	
6 to 4	FAULT_MAX_CNT[2:0]	Bits to configure the fault counter max value	
		3b'000	1
		3b'001	2
		3b'010	4
		3b'011	6
		3b'100	8
		3b'101	10
		3b'110	12
		3b'111	15
		Reset condition	OFF_OTP
3 to 0	FAULT_CNT[3:0]	Register to access the fault error count	
		4b'0000	0
		4b'0001	1
		4b'0010	2
		4b'0011	3
		4b'0100	4
		4b'0101	5
		4b'0110	6
		4b'0111	7
		4b'1000	8
		4b'1001	9
		4b'1010	10
		4b'1011	11
		4b'1100	12
		4b'1101	13
		4b'1110	14
		4b'1111	15
		Reset condition	OFF_TOG

16.4.46 FSAFE_COUNTER

Table 224. FSAFE_COUNTER – Fail-safe counter register (address 2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	NOT USED	FS_BYPASS_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 225. FSAFE_COUNTER – Fail-safe counter register (address 2Fh) bit description

Bit	Symbol	Description	
3 to 0	FS_BYPASS_CNT[3:0]	Bits to access the fail-safe bypass count	
		4b'0000	0
		4b'0001	1
		4b'0010	2
		4b'0011	3
		4b'0100	4
		4b'0101	5
		4b'0110	6
		4b'0111	7
		4b'1000	8
		4b'1001	9
		4b'1010	10
		4b'1011	11
		4b'1100	12
		4b'1101	13
		4b'1110	14
		4b'1111	15
		Reset condition	UVDET

16.4.47 AMUX

Table 226. AMUX – Analog multiplexer register (address 30h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol			AMUX_EN	AMUX_SEL[4:0]				
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR	RWCLR

Table 227. AMUX – Analog multiplexer register (address 30h) bit description

Bit	Symbol	Description	
5	AMUX_EN	Bits to enable/disable the AMUX function	
		1b'0	AMUX disabled / PGOOD mode
		1b'1	AMUX enabled
		Reset condition	OFF_TOG

Table 227. AMUX – Analog multiplexer register (address 30h) bit description*...continued*

Bit	Symbol	Description	
4 to 0	AMUX_SEL[4:0]	Bits to configure the AMUX selection	
		5b'00000	Disabled - Hi-Z
		5b'00001	Reserved
		5b'00010	Reserved
		5b'00011	Reserved
		5b'00100	Reserved
		5b'00101	Reserved
		5b'00110	Reserved
		5b'00111	Reserved
		5b'01000	Reserved
		5b'01001	Reserved
		5b'01010	Reserved
		5b'01011	Reserved
		5b'01100	Reserved
		5b'01101	Reserved
		5b'01110	Reserved
		5b'01111	Reserved
		5b'10000	Reserved
		5b'10001	Reserved
		5b'10010	Reserved
		5b'10011	Reserved
		5b'10100	Reserved
		5b'10101	Reserved
		5b'10110	Reserved
		5b'10111	TEMP_IC (reports temperature of die)
		5b'11000	Reserved
		5b'11001	Reserved
		5b'11010	Reserved
		5b'11011	Reserved
		5b'11100	Reserved
		5b'11101	Reserved
		5b'11110	Reserved
		5b'11111	Reserved
		Reset condition	OFF_TOG

16.4.48 SW_RAMP

Table 228. SW_RAMP – Switcher ramp register (address 31h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	SW3DVS_RAMP[1:0]		SW2DVS_RAMP[1:0]		SW1DVS_RAMP[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 229. SW_RAMP – Switcher ramp register (address 31h) bit description

Bit	Symbol	Description	
5 to 4	SW3DVS_RAMP[1:0]	Bits to configure the DVS ramp settings for SW3 (2.5 MHz)	
		2b'00	7.8 mV/µs
		2b'01	15.6 mV/µs
		2b'10	3.9 mV/µs
		2b'11	1.95 mV/µs
		Reset condition	OFF_OTP
3 to 2	SW2DVS_RAMP[1:0]	Bits to configure the DVS ramp settings for SW2 (2.5 MHz)	
		2b'00	7.8 mV/µs
		2b'01	15.6 mV/µs
		2b'10	3.9 mV/µs
		2b'11	1.95 mV/µs
		Reset condition	OFF_OTP
1 to 0	SW1DVS_RAMP[1:0]	Bits to configure the DVS ramp settings for SW1 (2.5 MHz)	
		2b'00	7.8 mV/µs
		2b'01	15.6 mV/µs
		2b'10	3.9 mV/µs
		2b'11	1.95 mV/µs
		Reset condition	OFF_OTP

16.4.49 SWx_CONFIG1

Table 230. SWx_CONFIG1 – Switcher configuration 1 register (address 32h, 39h, 40h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SWx_UV_ BYPASS	SWx_OV_ BYPASS	SWx_ILIM_ BYPASS	SWx_UV_ STATE	SWx_OV_ STATE	SWx_ILIM_ STATE	NOT USED	SWx_PG_EN
Reset	0	0	0	1	1	1	0	0
Access	RWOTP	RWOTP	RWOTP	RWCLR	RWCLR	RWCLR	RO	RWOTP

Table 231. SWx_CONFIG1 – Switcher configuration 1 register (address 32h, 39h, 40h) bit description

Bit	Symbol	Description	
7	SWx_UV_BYPASS	Bits to configure the UV fault protection bypass	
		1b'0	No fault bypass
		1b'1	Fault bypassed
		Reset condition	OFF_OTP
6	SWx_OV_BYPASS	Bits to configure the OV fault protection bypass	
		1b'0	No fault bypass
		1b'1	Fault bypassed
		Reset condition	OFF_OTP
5	SWx_ILIM_BYPASS	Bits to configure the ILIM fault protection bypass	
		1b'0	No fault bypass
		1b'1	Fault bypassed
		Reset condition	OFF_OTP

Table 231. SWx_CONFIG1 – Switcher configuration 1 register (address 32h, 39h, 40h) bit description*...continued*

Bit	Symbol	Description	
4	SWx_UV_STATE	Bits to configure the UV fault reaction	
		1b'0	SWx disables upon an UV fault
		1b'1	SWx remains on upon an UV fault
		Reset condition	OFF_TOG
3	SWx_OV_STATE	Bits to configure the OV fault reaction	
		1b'0	SWx disables upon an OV fault
		1b'1	SWx remains on upon an OV fault
		Reset condition	OFF_TOG
2	SWx_ILIM_STATE	Bits to configure the ILIM fault reaction	
		1b'0	SWx disables upon an ILIM fault
		1b'1	SWx remains on upon an ILIM fault
		Reset condition	OFF_TOG
0	SWx_PG_EN	Bits to configure the PGOOD assignment for SWx	
		1b'0	PGOOD is not assigned to SWx output
		1b'1	PGOOD is assigned to SWx output
		Reset condition	OFF_OTP

16.4.50 SWx_CONFIG2

Table 232. SWx_CONFIG2 – Switcher configuration 2 register (address 33h, 3Ah, 41h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SWx_FLT_REN	NOT USED	NOT USED	SWxILIM[1:0]		SWxPHASE[2:0]		
Reset	1	0	0	1	0	0	0	0
Access	RWCLR	RO	RO	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 233. SWx_CONFIG2 – Switcher configuration 2 register (address 33h, 3Ah, 41h) bit description

Bit	Symbol	Description	
7	SWx_FLT_REN	Bits to configure the fault re-enable mode for SWx	
		1b'0	SWx remains disabled even after clearing the fault
		1b'1	SWx returns to previous state after the fault is cleared
		Reset condition	OFF_TOG
4 to 3	SWxILIM[1:0]	Bits to configure the current limit values for SWx	
		2b'00	Reserved
		2b'01	4.0 A
		2b'10	5.0 A
		2b'11	6.0 A
		Reset condition	OFF_OTP

Table 233. SWx_CONFIG2 – Switcher configuration 2 register (address 33h, 3Ah, 41h) bit description*...continued*

Bit	Symbol	Description	
2 to 0	SWxPHASE[2:0]	Bits to configure the clock phase configuration for SWx (CLK ref to the main high-frequency clock)	
		3b'000	No clock phase shift
		3b'001	Shifted by 1 CLK
		3b'010	Shifted by 2 CLK
		3b'011	Shifted by 3 CLK
		3b'100	Shifted by 4 CLK
		3b'101	Reserved
		3b'110	Reserved
		3b'111	Reserved
		Reset condition	OFF_OTP

16.4.51 SWx_PWRUP

Table 234. SWx_PWRUP – Switcher power-up register (address 34h, 3Bh, 42h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	SWx_SEQ[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 235. SWx_PWRUP – Switcher power-up register (address 34h, 3Bh, 42h) bit description

Bit	Symbol	Description	
5 to 0	SWx_SEQ[5:0]]	Bits to configure the power up/down slot sequence of SWx	
		6b'000000	OFF
		6b'000001	Slot 0
		6b'000010	Slot 1
		6b'000011	Slot 2
		6b'000100	Slot 3
		6b'000101	Slot 4
		6b'000110	Slot 5
		6b'000111	Slot 6
		6b'001000	Slot 7
		6b'001001	Slot 8
		6b'001010	Slot 9
		6b'001011	Slot 10
		6b'001100	Slot 11
		6b'001101	Slot 12
		6b'001110	Slot 13
		6b'001111	Slot 14
		6b'010000	Slot 15
		6b'010001	Slot 16
		6b'010010	Slot 17
		6b'010011	Slot 18

Table 235. SWx_PWRUP – Switcher power-up register (address 34h, 3Bh, 42h) bit description_...continued_

Bit	Symbol	Description	
		6b'010100	Slot 19
		6b'010101	Slot 20
		6b'010110	Slot 21
		6b'010111	Slot 22
		6b'011000	Slot 23
		6b'011001	Slot 24
		6b'011010	Slot 25
		6b'011011	Slot 26
		6b'011100	Slot 27
		6b'011101	Slot 28
		6b'011110	Slot 29
		6b'011111	Slot 30
		6b'100000	Slot 31
		6b'100001	Slot 32
		6b'100010	Slot 33
		6b'100011	Slot 34
		6b'100100	Slot 35
		6b'100101	Slot 36
		6b'100110	Slot 37
		6b'100111	Slot 38
		6b'101000	Slot 39
		6b'101001	Slot 40
		6b'101010	Slot 41
		6b'101011	Slot 42
		6b'101100	Slot 43
		6b'101101	Slot 44
		6b'101110	Slot 45
		6b'101111	Slot 46
		6b'110000	Slot 47
		6b'110001	Slot 48
		6b'110010	Slot 49
		6b'110011	Slot 50
		6b'110100	Slot 51
		6b'110101	Slot 52
		6b'110110	Slot 53
		6b'110111	Slot 54
		6b'111000	Slot 55
		6b'111001	Slot 56
		6b'111010	Slot 57
		6b'111011	Slot 58
		6b'111100	Slot 59
		6b'111101	Slot 60
		6b'111110	Slot 61
		6b'111111	Slot 62

Table 235. SWx_PWRUP – Switcher power-up register (address 34h, 3Bh, 42h) bit description*...continued*

Bit	Symbol	Description	
		Reset condition	OFF_OTP

16.4.52 SWx_MODE

Table 236. SWx_MODE – Switcher mode register (address 35h, 3Ch, 43h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SWx_OV_TH[1:0]		SWx_UV_TH[1:0]		SWx_STBY_MODE[1:0]		SWx_RUN_MODE[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 237. SWx_MODE – Switcher mode register (address 35h, 3Ch, 43h) bit description

Bit	Symbol	Description	
7 to 6	SWx_OV_TH[1:0]	Bits to configure the overvoltage detection threshold of SWx	
		2b'00	103.50 %
		2b'01	104 %
		2b'10	104.50 %
		2b'11	105 %
		Reset condition	OFF_OTP
5 to 4	SWx_UV_TH[1:0]	Bits to configure the undervoltage detection threshold of SWx	
		2b'00	96.50 %
		2b'01	96 %
		2b'10	95.50 %
		2b'11	95 %
		Reset condition	OFF_OTP
3 to 2	SWx_STBY_MODE[1:0]	Bits to configure the switching mode of SWx in Standby state	
		2b'00	OFF
		2b'01	PWM
		2b'10	PFM
		2b'11	OFF
		Reset condition	OFF_OTP
1 to 0	SWx_RUN_MODE[1:0]	Bits to configure the switching mode of SWx in ON states (except Standby)	
		2b'00	OFF
		2b'01	PWM
		2b'10	PFM
		2b'11	OFF
		Reset condition	OFF_OTP

16.4.53 SWx_RUN_VOLT

Table 238. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VSWx_RUN[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 238. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Access	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 239. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit description

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
7 to 0	VSWx_RUN[7:0]	8b'00000000	0.5
		8b'00000001	0.6
		8b'00000010	0.60625
		8b'00000011	0.6125
		8b'00000100	0.61875
		8b'00000101	0.625
		8b'00000110	0.63125
		8b'00000111	0.6375
		8b'00001000	0.64375
		8b'00001001	0.65
		8b'00001010	0.65625
		8b'00001011	0.6625
		8b'00001100	0.66875
		8b'00001101	0.675
		8b'00001110	0.68125
		8b'00001111	0.6875
		8b'00010000	0.69375
		8b'00010001	0.7
		8b'00010010	0.70625
		8b'00010011	0.7125
		8b'00010100	0.71875
		8b'00010101	0.725
		8b'00010110	0.73125
		8b'00010111	0.7375
		8b'00011000	0.74375
		8b'00011001	0.75
		8b'00011010	0.75625
		8b'00011011	0.7625
		8b'00011100	0.76875
		8b'00011101	0.775
		8b'00011110	0.78125
		8b'00011111	0.7875
		8b'00100000	0.79375
		8b'00100001	0.8
		8b'00100010	0.80625
		8b'00100011	0.8125
		8b'00100100	0.81875
		8b'00100101	0.825
		8b'00100110	0.83125

Table 239. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'00100111	0.8375
		8b'00101000	0.84375
		8b'00101001	0.85
		8b'00101010	0.85625
		8b'00101011	0.8625
		8b'00101100	0.86875
		8b'00101101	0.875
		8b'00101110	0.88125
		8b'00101111	0.8875
		8b'00110000	0.89375
		8b'00110001	0.9
		8b'00110010	0.90625
		8b'00110011	0.9125
		8b'00110100	0.91875
		8b'00110101	0.925
		8b'00110110	0.93125
		8b'00110111	0.9375
		8b'00111000	0.94375
		8b'00111001	0.95
		8b'00111010	0.95625
		8b'00111011	0.9625
		8b'00111100	0.96875
		8b'00111101	0.975
		8b'00111110	0.98125
		8b'00111111	0.9875
		8b'01000000	0.99375
		8b'01000001	1
		8b'01000010	1.00625
		8b'01000011	1.0125
		8b'01000100	1.01875
		8b'01000101	1.025
		8b'01000110	1.03125
		8b'01000111	1.0375
		8b'01001000	1.04375
		8b'01001001	1.05
		8b'01001010	1.05625
		8b'01001011	1.0625
		8b'01001100	1.06875
		8b'01001101	1.075
		8b'01001110	1.08125
		8b'01001111	1.0875
		8b'01010000	1.09375
		8b'01010001	1.1
		8b'01010010	1.10625

Table 239. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'01010011	1.1125
		8b'01010100	1.11875
		8b'01010101	1.125
		8b'01010110	1.13125
		8b'01010111	1.1375
		8b'01011000	1.14375
		8b'01011001	1.15
		8b'01011010	1.15625
		8b'01011011	1.1625
		8b'01011100	1.16875
		8b'01011101	1.175
		8b'01011110	1.18125
		8b'01011111	1.1875
		8b'01100000	1.19375
		8b'01100001	1.2
		8b'01100010	1.20625
		8b'01100011	1.2125
		8b'01100100	1.21875
		8b'01100101	1.225
		8b'01100110	1.23125
		8b'01100111	1.2375
		8b'01101000	1.24375
		8b'01101001	1.25
		8b'01101010	1.25625
		8b'01101011	1.2625
		8b'01101100	1.26875
		8b'01101101	1.275
		8b'01101110	1.28125
		8b'01101111	1.2875
		8b'01110000	1.29375
		8b'01110001	1.3
		8b'01110010	1.30625
		8b'01110011	1.3125
		8b'01110100	1.31875
		8b'01110101	1.325
		8b'01110110	1.33125
		8b'01110111	1.3375
		8b'01111000	1.34375
		8b'01111001	1.35
		8b'01111010	Reserved
		8b'01111011	Reserved
		8b'01111100	Reserved
		8b'01111101	1.45
		8b'01111110	Reserved

Table 239. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'01111111	1.5
		8b'10000000	1.8
		8b'10000001	1.8125
		8b'10000010	1.825
		8b'10000011	1.8375
		8b'10000100	1.85
		8b'10000101	1.8625
		8b'10000110	1.875
		8b'10000111	1.8875
		8b'10001000	1.9
		8b'10001001	1.9125
		8b'10001010	1.925
		8b'10001011	1.9375
		8b'10001100	1.95
		8b'10001101	1.9625
		8b'10001110	1.975
		8b'10001111	1.9875
		8b'10010000	2
		8b'10010001	2.0125
		8b'10010010	2.025
		8b'10010011	2.0375
		8b'10010100	2.05
		8b'10010101	2.0625
		8b'10010110	2.075
		8b'10010111	2.0875
		8b'10011000	2.1
		8b'10011001	2.1125
		8b'10011010	2.125
		8b'10011011	2.1375
		8b'10011100	2.15
		8b'10011101	2.1625
		8b'10011110	2.175
		8b'10011111	2.1875
		8b'10100000	2.2
		8b'10100001	2.2125
		8b'10100010	2.225
		8b'10100011	2.2375
		8b'10100100	2.25
		8b'10100101	2.2625
		8b'10100110	2.275
		8b'10100111	2.2875
		8b'10101000	2.3
		8b'10101001	2.3125
		8b'10101010	2.325

Table 239. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'10101011	2.3375
		8b'10101100	2.35
		8b'10101101	2.3625
		8b'10101110	2.375
		8b'10101111	2.3875
		8b'10110000	2.4
		8b'10110001	2.4125
		8b'10110010	2.425
		8b'10110011	2.4375
		8b'10110100	2.45
		8b'10110101	2.4625
		8b'10110110	2.475
		8b'10110111	2.4875
		8b'10111000	2.5
		8b'10111001	Reserved
		8b'10111010	Reserved
		8b'10111011	2.6
		8b'10111100	Reserved
		8b'10111101	Reserved
		8b'10111110	Reserved
		8b'10111111	Reserved
		8b'11000000	2.8
		8b'11000001	2.825
		8b'11000010	2.85
		8b'11000011	2.875
		8b'11000100	2.9
		8b'11000101	2.925
		8b'11000110	2.95
		8b'11000111	2.975
		8b'11001000	3
		8b'11001001	3.025
		8b'11001010	3.05
		8b'11001011	3.075
		8b'11001100	3.1
		8b'11001101	3.125
		8b'11001110	3.15
		8b'11001111	3.175
		8b'11010000	3.2
		8b'11010001	3.225
		8b'11010010	3.25
		8b'11010011	3.275
		8b'11010100	3.3
		8b'11010101	Reserved
		8b'11010110	Reserved

Table 239. SWx_RUN_VOLT – Switcher running voltage register (address 36h, 3Dh, 44h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in ON states (except Standby) (V)
		8b'11010111	Reserved
		8b'11011000	Reserved
		8b'11011001	Reserved
		8b'11011010	Reserved
		8b'11011011	Reserved
		8b'11011100	Reserved
		8b'11011101	Reserved
		8b'11011110	Reserved
		8b'11011111	Reserved
		8b'11100000	Reserved
		8b'11100001	Reserved
		8b'11100010	Reserved
		8b'11100011	Reserved
		8b'11100100	Reserved
		8b'11100101	Reserved
		8b'11100110	Reserved
		8b'11100111	Reserved
		8b'11101000	Reserved
		8b'11101001	Reserved
		8b'11101010	Reserved
		8b'11101011	Reserved
		8b'11101100	Reserved
		8b'11101101	Reserved
		8b'11101110	Reserved
		8b'11101111	Reserved
		8b'11110000	Reserved
		8b'11110001	Reserved
		8b'11110010	Reserved
		8b'11110011	Reserved
		8b'11110100	Reserved
		8b'11110101	Reserved
		8b'11110110	Reserved
		8b'11110111	Reserved
		8b'11111000	Reserved
		8b'11111001	Reserved
		8b'11111010	Reserved
		8b'11111011	Reserved
		8b'11111100	Reserved
		8b'11111101	Reserved
		8b'11111110	Reserved
		8b'11111111	Reserved
		Reset condition	OFF_OTP

16.4.54 SWx_STBY_VOLT

Table 240. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VSWx_STBY[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
7 to 0	VSWx_STBY[7:0]	8b'00000000	0.5
		8b'00000001	0.6
		8b'00000010	0.60625
		8b'00000011	0.6125
		8b'00000100	0.61875
		8b'00000101	0.625
		8b'00000110	0.63125
		8b'00000111	0.6375
		8b'00001000	0.64375
		8b'00001001	0.65
		8b'00001010	0.65625
		8b'00001011	0.6625
		8b'00001100	0.66875
		8b'00001101	0.675
		8b'00001110	0.68125
		8b'00001111	0.6875
		8b'00010000	0.69375
		8b'00010001	0.7
		8b'00010010	0.70625
		8b'00010011	0.7125
		8b'00010100	0.71875
		8b'00010101	0.725
		8b'00010110	0.73125
		8b'00010111	0.7375
		8b'00011000	0.74375
		8b'00011001	0.75
		8b'00011010	0.75625
		8b'00011011	0.7625
		8b'00011100	0.76875
		8b'00011101	0.775
		8b'00011110	0.78125
		8b'00011111	0.7875
		8b'00100000	0.79375
		8b'00100001	0.8
		8b'00100010	0.80625

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
		8b'00100011	0.8125
		8b'00100100	0.81875
		8b'00100101	0.825
		8b'00100110	0.83125
		8b'00100111	0.8375
		8b'00101000	0.84375
		8b'00101001	0.85
		8b'00101010	0.85625
		8b'00101011	0.8625
		8b'00101100	0.86875
		8b'00101101	0.875
		8b'00101110	0.88125
		8b'00101111	0.8875
		8b'00110000	0.89375
		8b'00110001	0.9
		8b'00110010	0.90625
		8b'00110011	0.9125
		8b'00110100	0.91875
		8b'00110101	0.925
		8b'00110110	0.93125
		8b'00110111	0.9375
		8b'00111000	0.94375
		8b'00111001	0.95
		8b'00111010	0.95625
		8b'00111011	0.9625
		8b'00111100	0.96875
		8b'00111101	0.975
		8b'00111110	0.98125
		8b'00111111	0.9875
		8b'01000000	0.99375
		8b'01000001	1
		8b'01000010	1.00625
		8b'01000011	1.0125
		8b'01000100	1.01875
		8b'01000101	1.025
		8b'01000110	1.03125
		8b'01000111	1.0375
		8b'01001000	1.04375
		8b'01001001	1.05
		8b'01001010	1.05625
		8b'01001011	1.0625
		8b'01001100	1.06875
		8b'01001101	1.075
		8b'01001110	1.08125

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
		8b'01001111	1.0875
		8b'01010000	1.09375
		8b'01010001	1.1
		8b'01010010	1.10625
		8b'01010011	1.1125
		8b'01010100	1.11875
		8b'01010101	1.125
		8b'01010110	1.13125
		8b'01010111	1.1375
		8b'01011000	1.14375
		8b'01011001	1.15
		8b'01011010	1.15625
		8b'01011011	1.1625
		8b'01011100	1.16875
		8b'01011101	1.175
		8b'01011110	1.18125
		8b'01011111	1.1875
		8b'01100000	1.19375
		8b'01100001	1.2
		8b'01100010	1.20625
		8b'01100011	1.2125
		8b'01100100	1.21875
		8b'01100101	1.225
		8b'01100110	1.23125
		8b'01100111	1.2375
		8b'01101000	1.24375
		8b'01101001	1.25
		8b'01101010	1.25625
		8b'01101011	1.2625
		8b'01101100	1.26875
		8b'01101101	1.275
		8b'01101110	1.28125
		8b'01101111	1.2875
		8b'01110000	1.29375
		8b'01110001	1.3
		8b'01110010	1.30625
		8b'01110011	1.3125
		8b'01110100	1.31875
		8b'01110101	1.325
		8b'01110110	1.33125
		8b'01110111	1.3375
		8b'01111000	1.34375
		8b'01111001	1.35
		8b'01111010	Reserved

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
		8b'01111011	Reserved
		8b'01111100	Reserved
		8b'01111101	1.45
		8b'01111110	Reserved
		8b'01111111	1.5
		8b'10000000	1.8
		8b'10000001	1.8125
		8b'10000010	1.825
		8b'10000011	1.8375
		8b'10000100	1.85
		8b'10000101	1.8625
		8b'10000110	1.875
		8b'10000111	1.8875
		8b'10001000	1.9
		8b'10001001	1.9125
		8b'10001010	1.925
		8b'10001011	1.9375
		8b'10001100	1.95
		8b'10001101	1.9625
		8b'10001110	1.975
		8b'10001111	1.9875
		8b'10010000	2
		8b'10010001	2.0125
		8b'10010010	2.025
		8b'10010011	2.0375
		8b'10010100	2.05
		8b'10010101	2.0625
		8b'10010110	2.075
		8b'10010111	2.0875
		8b'10011000	2.1
		8b'10011001	2.1125
		8b'10011010	2.125
		8b'10011011	2.1375
		8b'10011100	2.15
		8b'10011101	2.1625
		8b'10011110	2.175
		8b'10011111	2.1875
		8b'10100000	2.2
		8b'10100001	2.2125
		8b'10100010	2.225
		8b'10100011	2.2375
		8b'10100100	2.25
		8b'10100101	2.2625
		8b'10100110	2.275

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
		8b'10100111	2.2875
		8b'10101000	2.3
		8b'10101001	2.3125
		8b'10101010	2.325
		8b'10101011	2.3375
		8b'10101100	2.35
		8b'10101101	2.3625
		8b'10101110	2.375
		8b'10101111	2.3875
		8b'10110000	2.4
		8b'10110001	2.4125
		8b'10110010	2.425
		8b'10110011	2.4375
		8b'10110100	2.45
		8b'10110101	2.4625
		8b'10110110	2.475
		8b'10110111	2.4875
		8b'10111000	2.5
		8b'10111001	Reserved
		8b'10111010	Reserved
		8b'10111011	2.6
		8b'10111100	Reserved
		8b'10111101	Reserved
		8b'10111110	Reserved
		8b'10111111	Reserved
		8b'11000000	2.8
		8b'11000001	2.825
		8b'11000010	2.85
		8b'11000011	2.875
		8b'11000100	2.9
		8b'11000101	2.925
		8b'11000110	2.95
		8b'11000111	2.975
		8b'11001000	3
		8b'11001001	3.025
		8b'11001010	3.05
		8b'11001011	3.075
		8b'11001100	3.1
		8b'11001101	3.125
		8b'11001110	3.15
		8b'11001111	3.175
		8b'11010000	3.2
		8b'11010001	3.225
		8b'11010010	3.25

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
		8b'11010011	3.275
		8b'11010100	3.3
		8b'11010101	Reserved
		8b'11010110	Reserved
		8b'11010111	Reserved
		8b'11011000	Reserved
		8b'11011001	Reserved
		8b'11011010	Reserved
		8b'11011011	Reserved
		8b'11011100	Reserved
		8b'11011101	Reserved
		8b'11011110	Reserved
		8b'11011111	Reserved
		8b'11100000	Reserved
		8b'11100001	Reserved
		8b'11100010	Reserved
		8b'11100011	Reserved
		8b'11100100	Reserved
		8b'11100101	Reserved
		8b'11100110	Reserved
		8b'11100111	Reserved
		8b'11101000	Reserved
		8b'11101001	Reserved
		8b'11101010	Reserved
		8b'11101011	Reserved
		8b'11101100	Reserved
		8b'11101101	Reserved
		8b'11101110	Reserved
		8b'11101111	Reserved
		8b'11110000	Reserved
		8b'11110001	Reserved
		8b'11110010	Reserved
		8b'11110011	Reserved
		8b'11110100	Reserved
		8b'11110101	Reserved
		8b'11110110	Reserved
		8b'11110111	Reserved
		8b'11111000	Reserved
		8b'11111001	Reserved
		8b'11111010	Reserved
		8b'11111011	Reserved
		8b'11111100	Reserved
		8b'11111101	Reserved
		8b'11111110	Reserved

Table 241. SWx_STBY_VOLT – Switcher Standby voltage register (address 37h, 3Eh, 45h) bit description*...continued*

Bit	Symbol	Description	Bits to configure the output voltage of SWx in Standby state (V)
		8b'11111111	Reserved
		Reset condition	OFF_OTP

16.4.55 LDOx_CONFIG1

Table 242. LDOx_CONFIG1 – LDO configuration 1 register (address 55h, 5Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LDOx_UV_ BYPASS	LDOx_OV_ BYPASS	LDOx_ILIM_ BYPASS	LDOx_ UV_STATE	LDOx_ OV_STATE	LDOx_ ILIM_STATE	NOT USED	LDOx_PG_EN
Reset	0	0	0	1	1	1	0	0
Access	RWOTP	RWOTP	RWOTP	RWCLR	RWCLR	RWCLR	RO	RWOTP

Table 243. LDOx_CONFIG1 – LDO configuration 1 register (address 55h, 5Bh) bit description

Bit	Symbol	Description	
7	LDOx_UV_BYPASS	Bits to configure the UV fault protection bypass	
		1b'0	No fault bypass
		1b'1	Fault bypassed
		Reset condition	OFF_OTP
6	LDOx_OV_BYPASS	Bits to configure the OV fault protection bypass	
		1b'0	No fault bypass
		1b'1	Fault bypassed
		Reset condition	OFF_OTP
5	LDOx_ILIM_BYPASS	Bits to configure the ILIM fault protection bypass	
		1b'0	No fault bypass
		1b'1	Fault bypassed
		Reset condition	OFF_OTP
4	LDOx_UV_STATE	Bits to configure the UV fault reaction	
		1b'0	LDOx disables upon an UV fault
		1b'1	LDOx remains on upon an UV fault
		Reset condition	OFF_TOG
3	LDOx_OV_STATE	Bits to configure the OV fault reaction	
		1b'0	LDOx disables upon an OV fault
		1b'1	LDOx remains on upon an OV fault
		Reset condition	OFF_TOG
2	LDOx_ILIM_STATE	Bits to configure the ILIM fault reaction	
		1b'0	LDOx disables upon an ILIM fault
		1b'1	LDOx remains on upon an ILIM fault
		Reset condition	OFF_TOG
0	LDOx_PG_EN	Bits to configure the PGOOD assignment for LDOx	
		1b'0	PGOOD is not assigned to LDOx output
		1b'1	PGOOD is assigned to LDOx output
		Reset condition	OFF_OTP

16.4.56 LDOx_STBY_VOLT

Table 244. LDOx_STBY_VOLT – LDO Standby voltage register (address 59h, 5Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NOT USED	NOT USED	NOT USED	VLDOX_STBY[4:0]				
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 245. LDOx_STBY_VOLT – LDO Standby voltage register (address 59h, 5Fh) bit description

Bits	Symbol	Description	
5 to 0	VLDOx_STBY[4:0]	Bits to configure the output voltage of LDOx in ON states (except Standby) (V)	
		5b'00000	0.75
		5b'00001	0.8
		5b'00010	0.85
		5b'00011	0.9
		5b'00100	0.95
		5b'00101	1
		5b'00110	1.05
		5b'00111	1.1
		5b'01000	1.15
		5b'01001	1.2
		5b'01010	1.25
		5b'01011	1.3
		5b'01100	1.35
		5b'01101	1.4
		5b'01110	1.45
		5b'01111	1.5
		5b'10000	1.8
		5b'10001	1.9
		5b'10010	2
		5b'10011	2.1
		5b'10100	2.2
		5b'10101	2.3
		5b'10110	2.4
		5b'10111	2.5
		5b'11000	2.6
		5b'11001	2.7
		5b'11010	2.8
		5b'11011	2.9
		5b'11100	3
		5b'11101	3.1
		5b'11110	3.2
		5b'11111	3.3
		Reset condition	OFF_OTP

16.4.57 STATE

Table 246. STATE – State register (address 60h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NXP_TM	CUST_TM	DBG_MODE	STATE[4:0]				
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Table 247. STATE – State register (address 60h) bit description

Bit	Symbol	Description	
7	NXP_TM	Bit to indicate the status of NXP only test mode	
		1b'0	Not in NXP only test mode
		1b'1	NXP only test mode
		Reset condition	OFF_TOG
6	CUST_TM	Bit to indicate the status of customer test mode	
		1b'0	Not in customer test mode
		1b'1	Customer test mode
		Reset condition	OFF_TOG
5	DBG_MODE	Bit to indicate the status of debug mode	
		1b'0	Not in debug mode
		1b'1	Debug mode
		Reset condition	OFF_TOG

Table 247. STATE – State register (address 60h) bit description*...continued*

Bit	Symbol	Description	
4 to 0	STATE[4:0]	Bits to access the state machine status	
		5b'00000	Reserved
		5b'00001	LP_Off
		5b'00010	Self-Test
		5b'00011	Power-up Sequence
		5b'00100	I/O Release
		5b'00101	INIT
		5b'00110	Run
		5b'00111	Standby
		5b'01000	Fault Power Down
		5b'01001	Turn-off Power down
		5b'01010	Reserved
		5b'01011	Reserved
		5b'01100	Reserved
		5b'01101	Reserved
		5b'01110	Reserved
		5b'01111	Reserved
		5b'10000	Fail-safe (only in Debug Mode)
		5b'10001	Reserved
		5b'10010	Reserved
		5b'10011	Reserved
		5b'10100	Reserved
		5b'10101	Reserved
		5b'10110	Reserved
		5b'10111	Reserved
		5b'11000	Reserved
		5b'11001	Reserved
		5b'11010	Reserved
		5b'11011	Reserved
		5b'11100	Reserved
		5b'11101	Reserved
		5b'11110	Reserved
		5b'11111	Reserved
		Reset condition	OFF_TOG

17 OTP programming debug mode

The PF5103 supports OTP fuse bank configuration and debug mode through the VDDOTP pin.

- If VDDOTP = GND, the device loads the configuration from the OTP fuses and operates in normal mode.
- If VDDOTP >= 1.4 V, the device enters the debug mode, the OTP configuration is accessible through mirror registers and the device operates in a limited functionality mode.

OTP emulation and programming performed by the customer is allowed during engineering development using NXP’s latest graphical user interface and socketed evaluation board. Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

17.1 Debug operation

The PF5103 allows temporary configuration to debug or test a customized power up configuration in the system. In order to access the debug mode, the VDDOTP pin should be pulled up to high above 1.4 V.

In the debug mode, the following conditions are valid:

- I^2C communication uses standard communication, with no CRC and secure write disabled.
- The default I^2C address is 0x08, regardless of the address configured by OTP.
- Watchdog monitoring is disabled.

The PF5103 can operate normally using the Debug mode configuration, as long as VIN does not go below the UVDET threshold. If VIN is lost (VIN < UVDET) the mirror register will be reset, and Debug mode configuration must be performed again.

17.2 OTP fuse programming

A permanent OTP configuration is possible by burning the OTP fuses. OTP fuse burning is performed in the LP_Off state. Contact your NXP representative for detailed information on OTP fuse programming.

18 Functional safety

18.1 System safety strategy

The PF5103 is defined in a context of safety, and will provide a set of features to achieve the safety goals in this context.

It provides a flexible yet complete safety architecture to comply with up to ASIL B systems, providing full programmability to enable or disable features to address the safety goal. This architecture includes protective mechanisms to avoid unwanted modification on the respective safety features, as required by the system.

The following are features considered to be critical for the functional safety strategy:

- Internal watchdog timer and watchdog monitor (simple type)
- Output voltage monitoring with dedicated bandgap reference
- CRC protection for I^2C protocol and select I^2C, OTP registers
- Input voltage monitoring with dedicated bandgap reference
- Clock monitoring at startup and during normal operation
- Analog built-in self-test (ABIST) on voltage monitors

18.2 Output voltage monitoring with dedicated bandgap reference

The OV/UV monitors for the regulators operate from an independent reference other than the regulator. To ensure the integrity of the regulators, a comparison between the regulator bandgap (BG1) and the monitoring bandgap (BG2) is performed. A 45 mV difference between the two bandgaps is an indicator of a potential regulation or monitoring fault, and is considered as a critical issue. Therefore, the device prevents the switching regulators from powering up. The input to the bandgap monitoring is selectable through the OTP_BGMON_SEL bit described in Table 248.

Table 248. Bandgap monitoring input

OTP_BGMON_SEL	Description
0	Monitor BG1 and BG2
1	Monitor VIN

On the PF51x3 ASIL B device, if a bandgap error is detected during a power-up event, the self-test will fail and prevent the device from powering up regardless of the value of the OTP_BGMON_BYPASS bit.

During the System On state, if a drift between two bandgaps is detected:

- When OTP_BGMON_BYPASS = 0, the power stage of the voltage regulators will be shut down.
- When OTP_BGMON_BYPASS = 1, The bandgap monitor only sends an interrupt to the system to announce the bandgap failure.

The BGMON_I is asserted when a bandgap failure occurs, provided it is not masked.

The BGMON_S bit is set to 0 when the bandgaps are within range, and set to 1 when the bandgaps are out of range.

18.3 ABIST verification

PF5103 provides an ABIST verification of all output voltage monitors of all the regulators at startup and through on-demand ABIST (AB_RUN).

- The device tests the OV comparators for each individual SWx, LDOx supply during the Self-Test routine and on-demand ABIST (AB_RUN) sequence

- The device tests the UV comparators for each individual SWx, LDOx supply during the Self-Test routine and on-demand ABIST (AB_RUN) sequence
- During the ABIST verification, it is required to ensure the corresponding OV/UV comparators are able to toggle, which in turn is a sign of the integrity of these functions
- If any of the comparators is not able to toggle, a warning bit is set on the I^2C register map
  - The ABIST_OV1 register contains the AB_SWx_OV, AB_LDOx_O bits for all regulators
  - The ABIST_UV1 register contain the AB_SWx_UV, AB_LDOx_UV bits for all regulators
- The ABIST registers are cleared or overwritten each time the ABIST check is performed
- The ABIST registers are part of the secure registers and will require an I2C secure write to be cleared if this feature is enabled
  Once an ABIST check is performed, the PF5103 can proceed with the Power-up sequence and the processor should be able to request the value of these registers and learn if ABIST failed for any of the voltage monitors.
  The AB_RUN bit is provided to perform an ABIST verification on demand.
  When the AB_RUN bit is set to 1, the control logic performs an ABIST verification on all OV/UV monitoring circuits. When the ABIST verification is finished, the AB_RUN bit self-clears to 0 and a new ABIST verification can be commanded as needed.
  When the secure write feature is enabled, the system must perform a secure write sequence in order to start an ABIST verification on demand.
  When the PF5103 performs an ABIST verification on demand, the OV/UV fault monitoring is blanked for a maximum period of 200 μs. During this time, the system must ensure it is in a safe state, or it is safe to perform this action without violating the safety goals of the system.
  If a failure on the OV/UV monitor is detected during the ABIST on demand request, the PMIC will assert the corresponding ABIST flags. It is the responsibility of the system to perform a diagnostic check after each ABIST verification to ensure it places the system in a safe state if an ABIST fault is detected.

19 IC level quiescent current requirements

Table 249. Quiescent current requirements
All parameters are specified at T_A = −40 to 125 °C, unless otherwise noted. Typical values are characterized at VIN = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
I_{ULPOFF}	ULP_Off state (PWRON = 0) ULP_OFF_CTRL = 1 LDOxIN = SWxIN = OPEN V_{IN} > UVDET -40 ℃ to 85 ℃	—	0.52	2	µA
$I_{ULPOFF\ SYS}$	ULP_OFF state (PWRON = 0); ULP_OFF_CTRL = 1 LDOxIN = SWxIN = VIN = 5 V LDOx = SWx = Disabled VIN > UVDET -40 ℃ to 85 ℃	—	1.5	6	µA
I_{LPOFF}	LP_Off state (PWRON = 1 or VDDOTP = 1) ULP_OFF_CTRL = 0 V_{IN} > UVDET	—	1.7	2	mA
I_{SYSON_STBY}	VIN > UVDET 20 MHz_OSC = ON 100KHz_OSC = ON SW1 = 0.9 V SW2 = 1.8 V SW3 = 3.3 V LDO1 = 3.0 V LDO2 = 3.3 V -40 °C to 85 °C	—	2.5	3	mA
I_LP_STBY	VIN > UVDET 20MHz_OSC = OFF 100KHz_OSC = ON SW1 = 0.9 V SW2 = 1.8 V SW3 = 3.3 V LDO1 = 3.0 V LDO2 = 3.3 V -40 °C to 85 °C	—	350	415	µA
I_{FSAFE}	Fail-safe mode (VDDOTP = 0) V_{IN} > UVDET	—	220	750	µA

20 Package drawing

20.1 Package outline

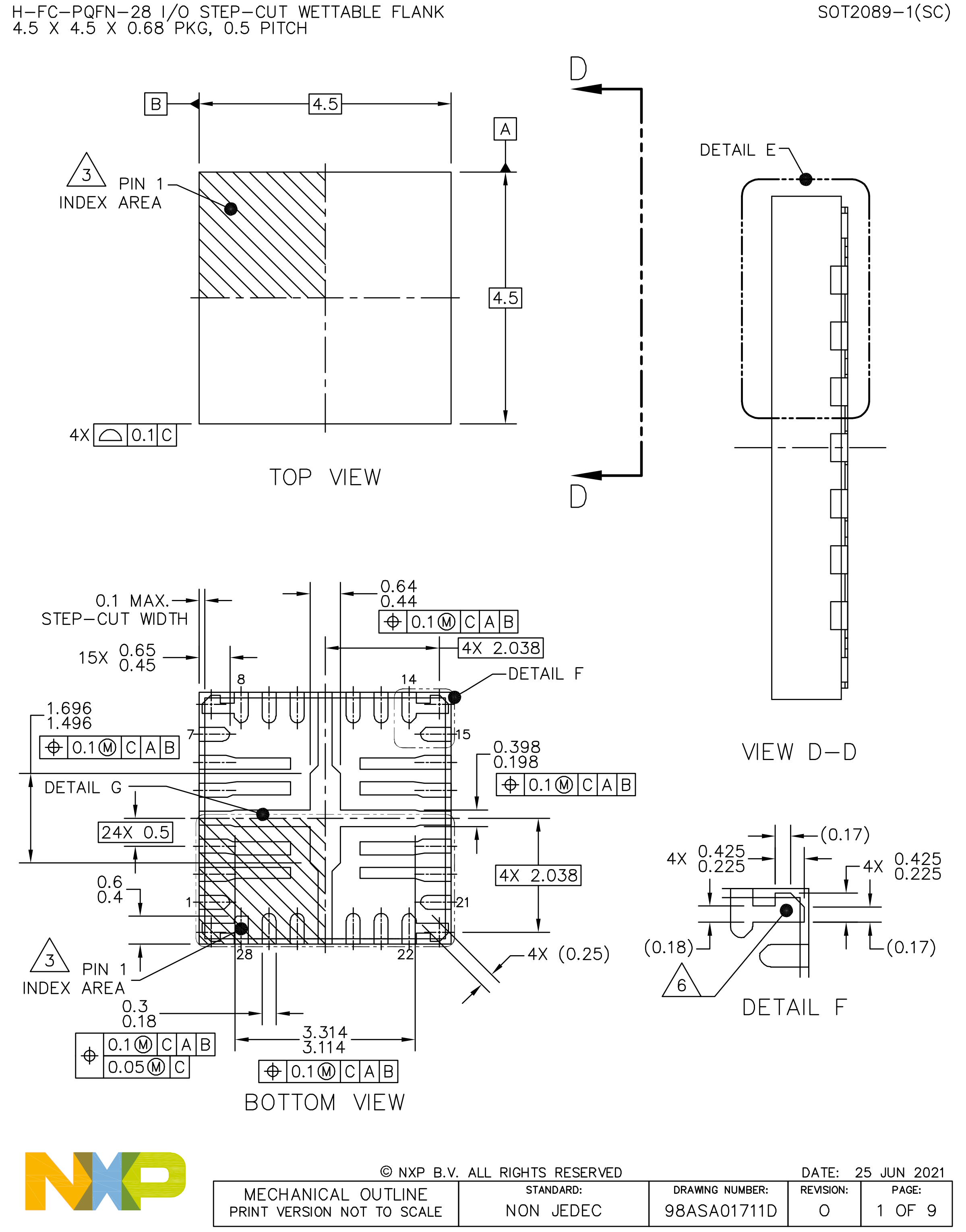
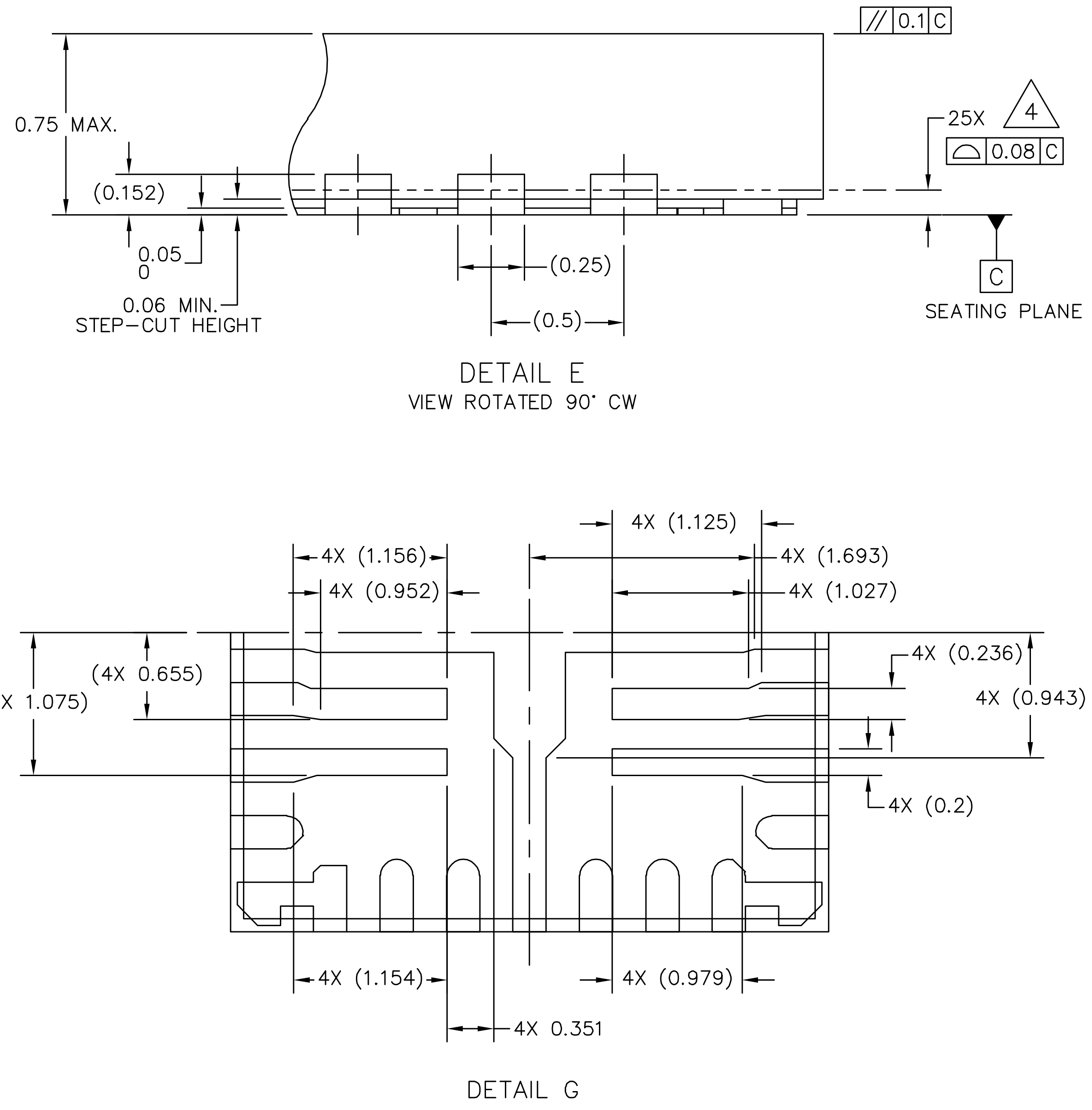


Figure 34. Package outline for PQFN28

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)



© NXP B.V. ALL RIGHTS RESERVED

DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01711D	REVISION: 0	PAGE: 2

Figure 35. Package outline detail for PQFN28

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE, SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.

DATE: 25 JUN 2021

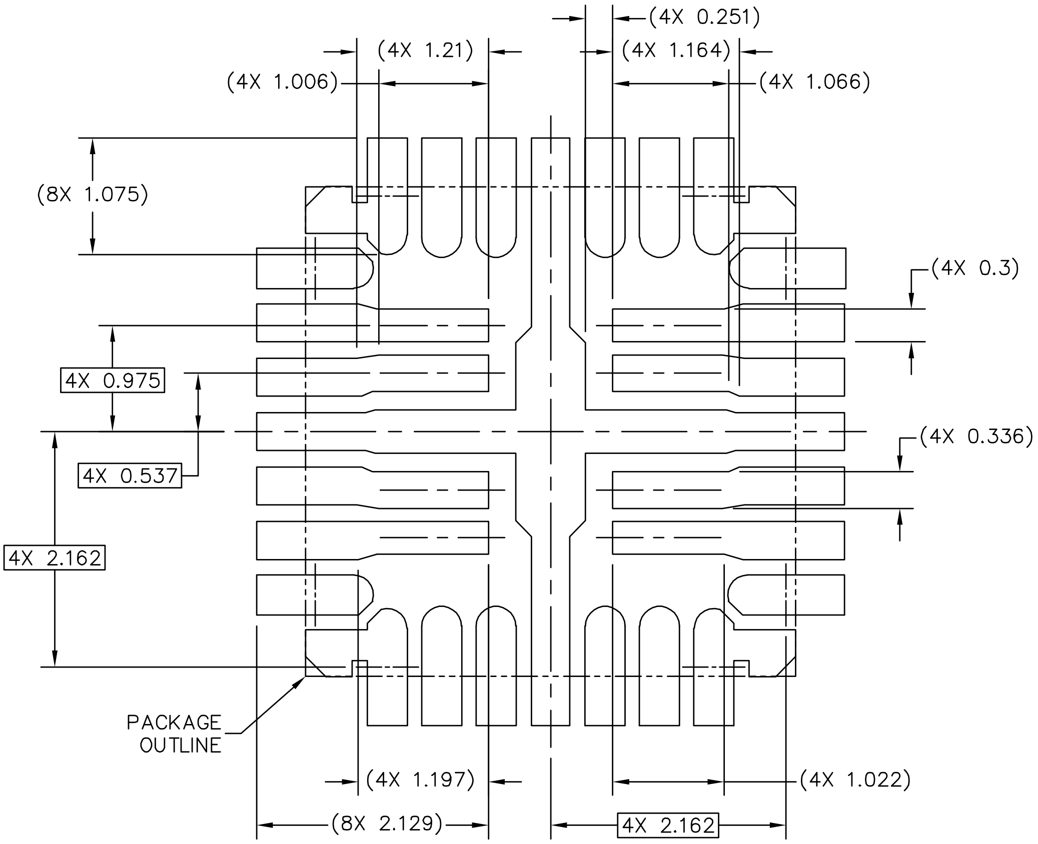
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
	NON JEDEC	98ASA01711D	O	9

Figure 36. Package outline notes for PQFN28

20.2 Package design guidelines

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

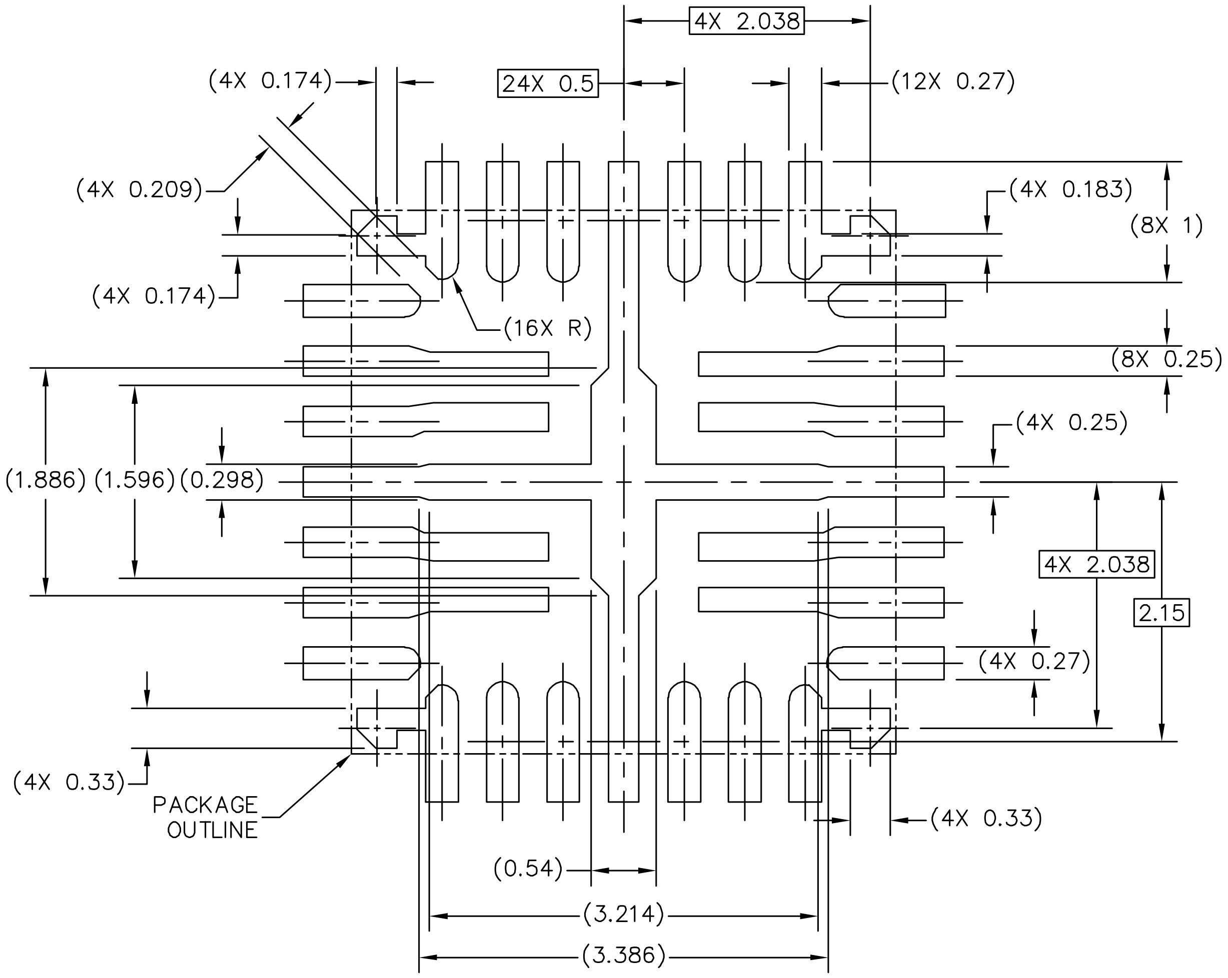
DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
	NON JEDEC	98ASA01711D	0	4

Figure 37. PCB design guidelines for PQFN28 – solder mask opening pattern

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

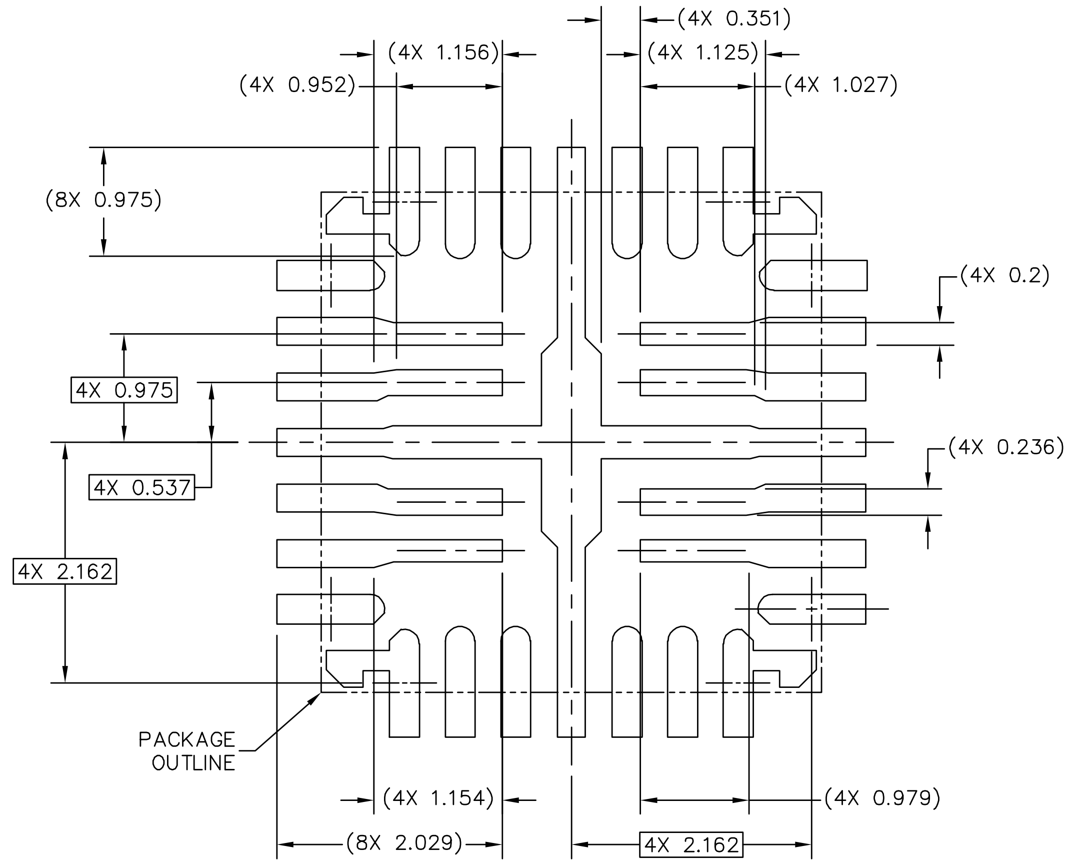
DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01711D	REVISION: 0	PAGE: 5

Figure 38. PCB design guidelines for PQFN28, I/O pads and solderable area

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

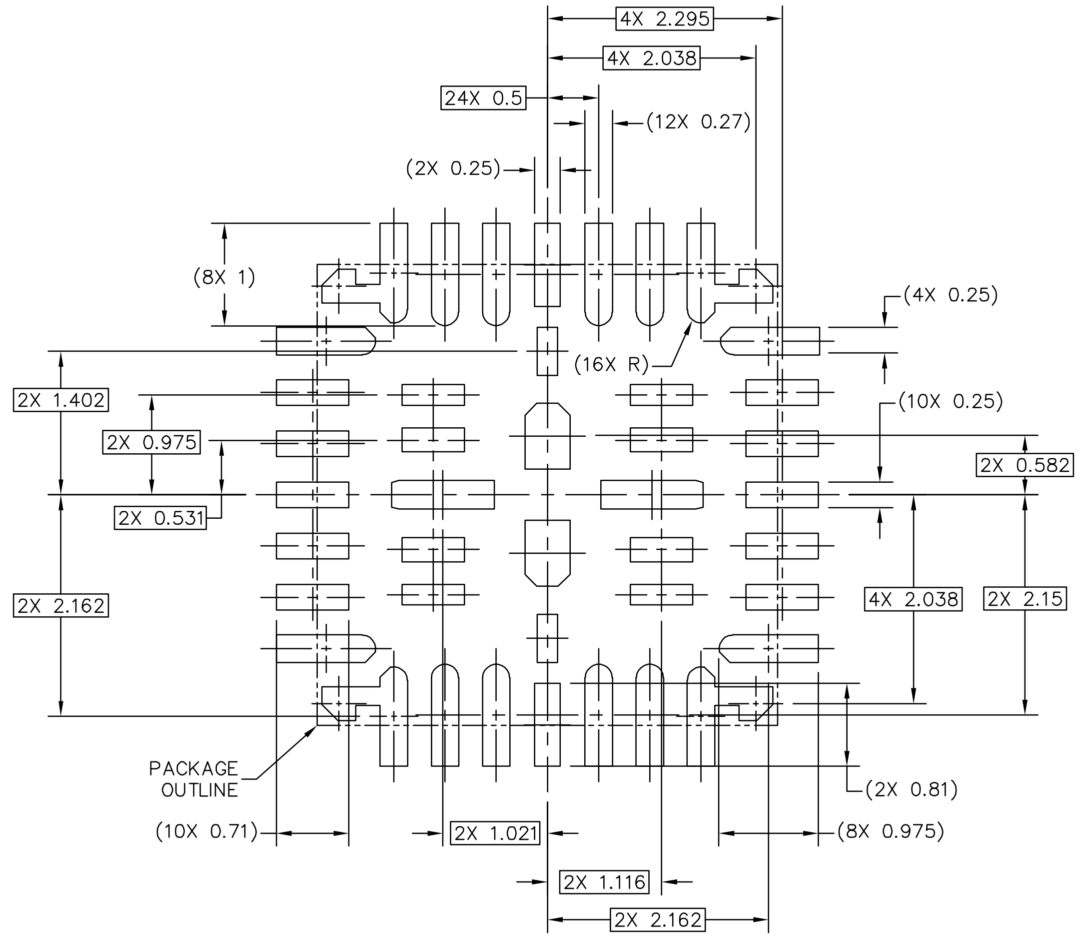
DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01711D	REVISION: O	PAGE: 6

Figure 39. PCB design guidelines for PQFN28, I/O pads and solderable area, continued

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

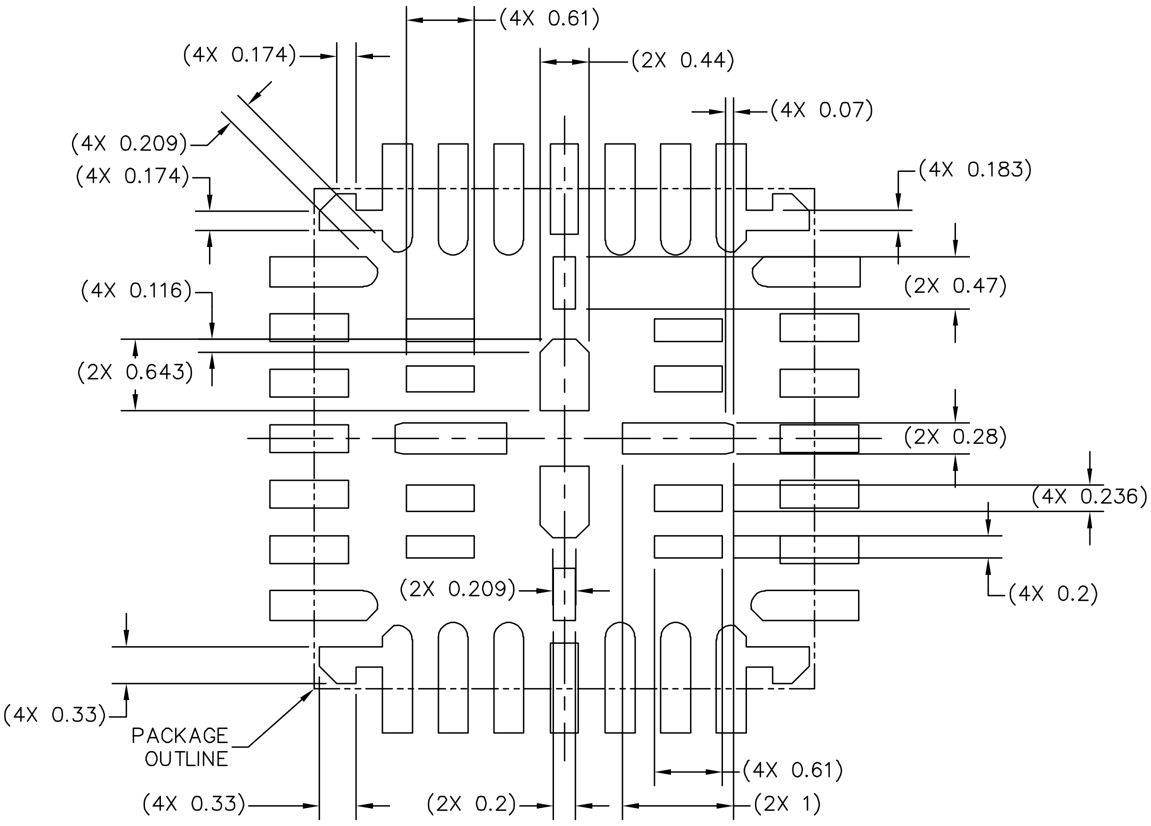
DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01711D	REVISION: O	PAGE: 7

Figure 40. PCB design guidelines for PQFN28, solder paste stencil

H-FC-PQFN-28 I/O STEP-CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089-1(SC)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
	NON JEDEC	98ASA01711D	0	8

Figure 41. PCB design guidelines for PQFN28, solder paste stencil, continued

21 Revision history

Table 250. Revision history

Document ID	Release date	Description
PF5103_PF5113_PF5123 v. 3.0	16 Feb 2026	• Changed classification from confidential to public • Product data sheet • This data sheet version takes the place of PB_PF5103, PB_PF5113, and PB_PF5123 • Updated Section 16.3, changing default value of the REV_ID register • Updated Table 136, changing default value of the REV_ID register • Global: updated all bit description table titles to current standard
PF51x3 v. 2.0	28 Oct 2025	• Product data sheet • Updated Table *Ordering information* • Updated title of table *Buck efficiency vs. ISWx at ambient temperature Ta = 25 #* • Updated table *IC Level Quiescent Current Requirements*

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents