PN5190B1

NFC Frontend

Rev. 4.7 — 22 October 2026 Product short data sheet

1 General description

This document describes the functionality and electrical specification of the high-power NFC-IC PN5190B1, silicon version B1, using firmware V2.0 or higher.

Additional documents supporting a design-in of the PN5190B1 are available from NXP, this additional design-in information is not part of this document.

The PN5190B1 supports highly innovative and unique features, which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

The independence of real-time host controller interactions makes this product a good fit for systems, which operate a preemptive multitasking OS like Linux or Android.

In this document, the term "MIFARE card“ refers to a contactless card using an IC out of the MIFARE Classic, MIFARE Plus, MIFARE Ultralight, or MIFARE DESFire product family.

For more information, refer to the PN5190 product page ref.[1] and full data sheet ref.[2] on nxp.com.

2 Features and benefits

2.1 RF functionality

- As a highly integrated high performance full NFC Forum-compliant frontend IC for contactless communication at 13.56 MHz, this NFC frontend IC utilizes a modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.
  PN5190B1 supports communication with all products of the MIFARE product-based card family including MIFARE Ultralight, MIFARE Classic 1K/4K, MIFARE DESFire EV1/EV2, and MIFARE Plus cards CRYPTO implemented in hardware for R/W of all NXP MIFARE product-based cards (includes intellectual-property licensing rights for NXP ISO/IEC 14443-A, Innovatron ISO/IEC 14443-B, and NXP MIFARE products).
  The PN5190B1 frontend IC supports the following RF operating modes:

2.1.1 ISO/IEC 14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC 14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 1, type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
- Proprietary data rates based on ISO/IEC 15693 with 106 kbit and 212 kbit/s (for NXP NTAG 5 communication)

2.1.7 ISO/IEC 18000-3 Mode 3

- Reader/writer mode supporting ISO/IEC 18000-3 Mode 3

2.1.8 ISO/IEC 18092

- ISO/IEC 18092 (NFC-IP1)

2.1.9 ISO/IEC 21481

- ISO/IEC 21481 (NFC-IP-2)

2.1.10 Peer to peer

- P2P Passive 106 kbit/s to 424 kbit/s, initiator and target

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- P2P Active 106 kbit/s to 424 kbit/s, initiator and target
- Proprietary passive communication for type A up to 848 kbit/s
- Functionality according to ISO/IEC 21481 (NFC-IP-2)

2.1.11 Card emulation

- ISO/IEC 14443-A card mode from 106 kbit/s up to 848 kbit/s (PICC) with active load modulation for increased communication range.

2.2 Host interface

- One host interface based on SPI is implemented:
  - SPI interface with data rates up to 15 Mbit/s with MOSI, MISO, NSS, and SCK signals
  - Interrupt request line to inform host controller on events
  - Independent TX and RX buffer for RF data with size of 1024 bytes each

2.3 Integrated DC-DC

- The PN5190B1 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 V, this simplifies the design of the power supply.
  A single supply concept for the RF system, e.g. with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.
  The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.
  The usage of the DC-DC is optional.
  For applications making use of the low-power card detection, the DC-DC is available. For applications using the ultra low-power card detection (ULPCD), the DC-DC cannot be used.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

3 Applications

- Payment
- Physical access
- eGov

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VDD_{(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$VDD_{(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, T_{amb} = 25 °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
I_{ULPCD}	average ultra-low-power card detection current	T_{amb} = 25 °C, VDD(VDDPA) = VDD(VDDIO) =VDD(VDD) 3.0 V, 330 ms Polling interval, 50 Ω antenna matching	-	22	-	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	Transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 350 mA @ $VDDPA_{max}$ = 5.7 V	-40	-	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 120 mA @ $VDDPA_{max}$ = 3.6 V	-40	-	+105	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5190B1HN/C121Y	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one reel, MSL=3. Minimum order quantity = 4000 pcs, the ending Y in the product name is indicating the packing "reel" Initialized with FW 2.1, supports encrypted firmware download	SOT2062-1
PN5190B1HN/C121E	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one tray, bakeable, MSL=3. Minimum order quantity = 490 pcs, the ending E in the product name is indicating the packing "single tray" Initialized with FW 2.1, supports encrypted firmware download	SOT2062-1
PN5190B1HN/C127Y	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one reel, MSL=3. Minimum order quantity = 4000 pcs, the ending Y in the product name is indicating the packing "reel" Initialized with FW 2.7, supports encrypted firmware download	SOT2062-1
PN5190B1HN/C127K	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in multiple trays, MSL=3. Minimum order quantity = 2450 pcs, the ending K in the product name is indicating the packing "multiple trays" Initialized with FW 2.7, supports encrypted firmware download	SOT2062-1
PN5190B1EV/C121Y	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel" Initialized with FW 2.1, supports encrypted firmware download	SOT1307-2
PN5190B1EV/C121E	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered in one tray, MSL = 3. Minimum order quantity = 490 pcs The ending E in the product name is indicating the packing "single tray" Initialized with FW 2.1, supports encrypted firmware download	SOT1307-2
PN5190B1EV/C127Y	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel" Initialized with FW 2.7, supports encrypted firmware download	SOT1307-2
PN5190B1EV/C127K	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered in one tray, MSL = 3. Minimum order quantity = 2450 pcs, the ending K in the product name is indicating the packing "multiple trays" Initialized with FW 2.7, supports encrypted firmware download	SOT1307-2

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6 Block diagram with VFBGA64 connections

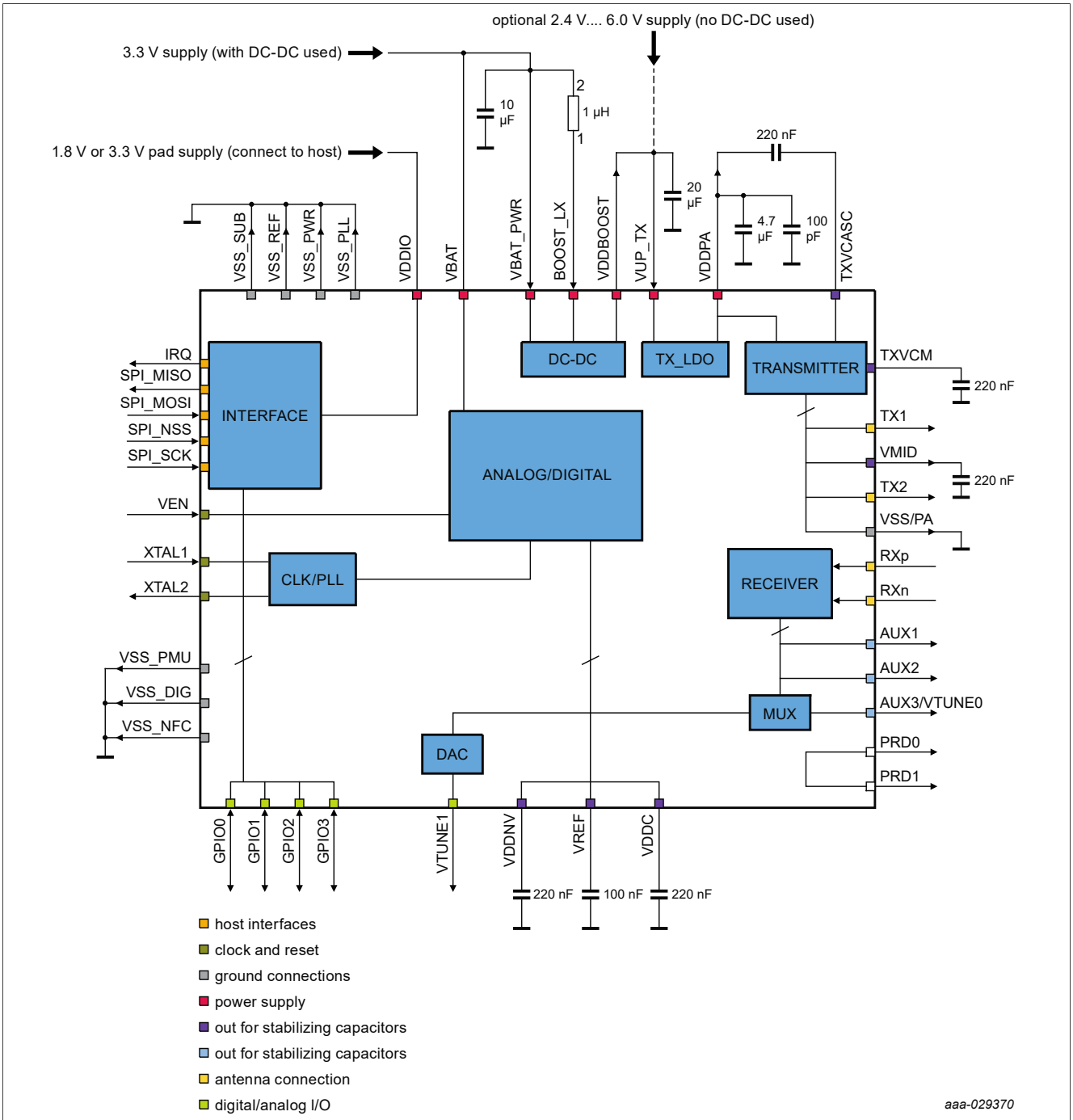

Figure 1. Block diagram (external connections: DC-DC mode)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	+ 2.0	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	+ 2.0	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	+500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	+150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

8 References

[1] Webpage – PN5190: NFC Frontend Supporting Challenging RF Environment for Payment, Physical Access Control (link)

[2] Data sheet – PN5190B1 (link)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

9 Revision history

Table 4. Revision history

Document ID	Release date	Description
PN5190B1_SDS v.4.7	22 October 2026	Released alongside data sheet update.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between and its customer, unless and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Licenses

Purchase of NXP ICs with NFC technology — Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

FeliCa — is a trademark of Sony Corporation.

ICODE — is a trademark of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

MIFARE — is a trademark of NXP B.V.

MIFARE Classic — is a trademark of NXP B.V.

MIFARE Plus — is a trademark of NXP B.V.

MIFARE Ultralight — is a trademark of NXP B.V.

NTAG — is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tables

Tab. 1. Quick reference data 5
Tab. 2. Ordering information 6
Tab. 3. Limiting values 8
Tab. 4. Revision history 10

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Figures

Fig. 1. Block diagram (external connections: DC-DC mode) 7

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Contents

1 General description 1
2 Features and benefits 2
2.1 RF functionality 2
2.1.1 ISO/IEC 14443-A 2
2.1.2 ISO/IEC 14443-B 2
2.1.3 FeliCa 2
2.1.4 Tag type reading 2
2.1.5 MIFARE card reading 2
2.1.6 ISO/IEC 15693 2
2.1.7 ISO/IEC 18000-3 Mode 3 2
2.1.8 ISO/IEC 18092 2
2.1.9 ISO/IEC 21481 2
2.1.10 Peer to peer 2
2.1.11 Card emulation 3
2.2 Host interface 3
2.3 Integrated DC-DC 3
3 Applications 4
4 Quick reference data 5
5 Ordering information 6
6 Block diagram with VFBGA64 connections 7
7 Limiting values 8
8 References 9
9 Revision history 10
Legal information 11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. **All rights reserved.**