PN7220

NFC controller with NCI interface supporting EMV and NFC Forum applications

Rev. 3.9 — 14 September 2026 Product short data sheet

1 General description

This document describes the functionality and electrical specification of the PN7220 high-power NFC controller family with NCI interface.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, the NXP PN7220 is a robust solution for payment terminals and all readers that must generate a strong RF field in a difficult environment. Offering full compliance with EMVCo 3.1 L1 analog and digital, the PN7220 simplifies designs while ensuring interoperability with a broad range of smartcards and mobile phones.

In addition to the reader/writer functionality, the device supports the host card emulation of ISO14443-A cards up to 848 kbit/s and allows to connect up to 3 TDA8035 which offer the possibility for an ISO7816 contact interface connection.

The PN7221 is based on the PN7220 and supports all features of PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple - this description is not part of this document. Note, that the ECP feature is available after formal authorization only.

Two host connection options are available for this product:

1. Connection to one single host - this is typically one host running an Android operating system
2. Connection to two hosts - in this case one host is typically a security CPU connected by the SPI interface to meet PCI compliance requirements for an EMVCo payment subsystem, and the second host connected by an I2C interface which is typically used to run an Android operating system for all non-EMVCo payment related applications.

The PN7220 communicates with a connected host through a physical interface using the NCI 2.2 protocol.

The PN7220 supports two types of configurable polling loops: one NFC Forum polling loop, and one EMVCo compliant polling loop. Switching between the polling loops is done based on a hardware input (GPIO) triggered by a connected host - in case of a switching of the polling loop all data from an ongoing transaction is cleared from the internal buffers, the NCI software stack is being reset and an RF reset is being executed. This helps to ensure data integrity for the performed transaction and allows to connect the right logical software endpoints to each of the polling loops.

To speed-up the switching between NFC Forum polling and EMVCo polling and ease the RF configuration of each polling loop, two independent sets of RF configuration data can be stored in EEPROM. This allows to optimize each polling loop to meet individual RF requirements.

The PN7220 product family supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the are available from NXP, this additional design-in information is not part of this document.

In this document, the term "MIFARE card" refers to a contactless card with an embedded MIFARE IC.

For more information, refer to the PN7220 product page ref.[1] and full data sheet ref.[2] on nxp.com.

2 Features and benefits

2.1 RF functionality

2.1.1 ISO/IEC 14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC 14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic Crypto supporting MIFARE Classic en-/decryption is integrated in hardware

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
  - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 6.6 kBd
  - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 26 kBd

2.1.7 NFC Forum compliancy

- NFC Forum version 13 compliance for R/W – analog and digital

2.1.8 EMVCo contactless compliancy

- Contactless EMVCo 3.1 compliance for R/W – digital
- Contactless EMVCo 3.1 compliance for R/W analog can be achieved, but depends on connected antenna geometry and size, matching network and RF settings.

2.1.9 Host interface

The devices PN7220 and PN7221 support one host interface using a single interface connection based on an I^2C interface host interface (host interface 1) with data rates up to 3.4 Mbit/s.

In addition, the device support two host interfaces using one interface connection based on an I^2C interface (host interface 2) up to 3.4Mbit/s and one SPI interface (host interface 1) up to 15Mbit/s.

The logical interface layer of the host interfaces is based on the NCI 2.2 interface specification, enhanced by NXP proprietary commands.

2.2 Transmitter

- Transmitter with high RF output power of 2.0 W
- Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
- Adaptive waveshape control (AWC)

2.3 Receiver

- Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

2.4 Integrated polling loop

- RF polling loop according to NFC Forum
- RF Polling loop according to EMVCo 3.1, integrated EMVCo L1 software stack

2.5 Integrated DC-DC

The PN7220 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply.

A single supply concept for the RF system, for example, with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.

The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.

The usage of the DC-DC is optional.

For applications making use of the low-power card detection, the DC-DC is available.

2.6 RF debugging support

- RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on pre-define trigger conditions – ideal debugging solution for PCI-compliant POS terminals
- One digital and one analog debug signal is provided by the chip for connection of an oscilloscope.

2.7 ISO7816 contact interface

The product supports the connection of up to three TDA8035 ICs which is the default EEPROM configuration of the device.

The device features an integrated EMVCo L1 contact card activation, and is compliant with contactless EMVCO specification 3.x.

The contact interface can be used for a single or dual host configuration.

3 Applications

- Payment terminals following the COTS security requirements with full EMVCo3.1 analog and digital compliancy
- Multi-application terminals
- Ticket validators for the controlling staff in public transport
- E-vehicle charging stations
- Vending machines

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VDD_{(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$VDD_{(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$VDD_{(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	PN7220 - supply with VDDPA from internal VDDPALDO with DC-DC	1.5	-	5.7	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, T_{amb} = 25 °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 350 mA @ $VDDPA_{max}$ = 5.7V	-40	-	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 120 mA @ $VDDPA_{max}$ = 3.6 V	-40	-	+105	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7220EV/C100K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller Initialized with firmware version 1.00	SOT1307-2
PN7220EV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller Initialized with firmware version 1.00	SOT1307-2
PN7221EV/C100K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00	SOT1307-2
PN7221EV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00	SOT1307-2
PN7220EV/C101K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 or 2 host microcontroller Initialized with firmware version 2.02	SOT1307-2
PN7220EV/C101Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 or 2 host microcontroller Initialized with firmware version 2.02	SOT1307-2

Table 2. Ordering information...*continued*

Type number	Package		
	Name	Description	Version
PN7221EV/C101K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.02	SOT1307-2
PN7221EV/C101Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.02	SOT1307-2

6 Block diagram

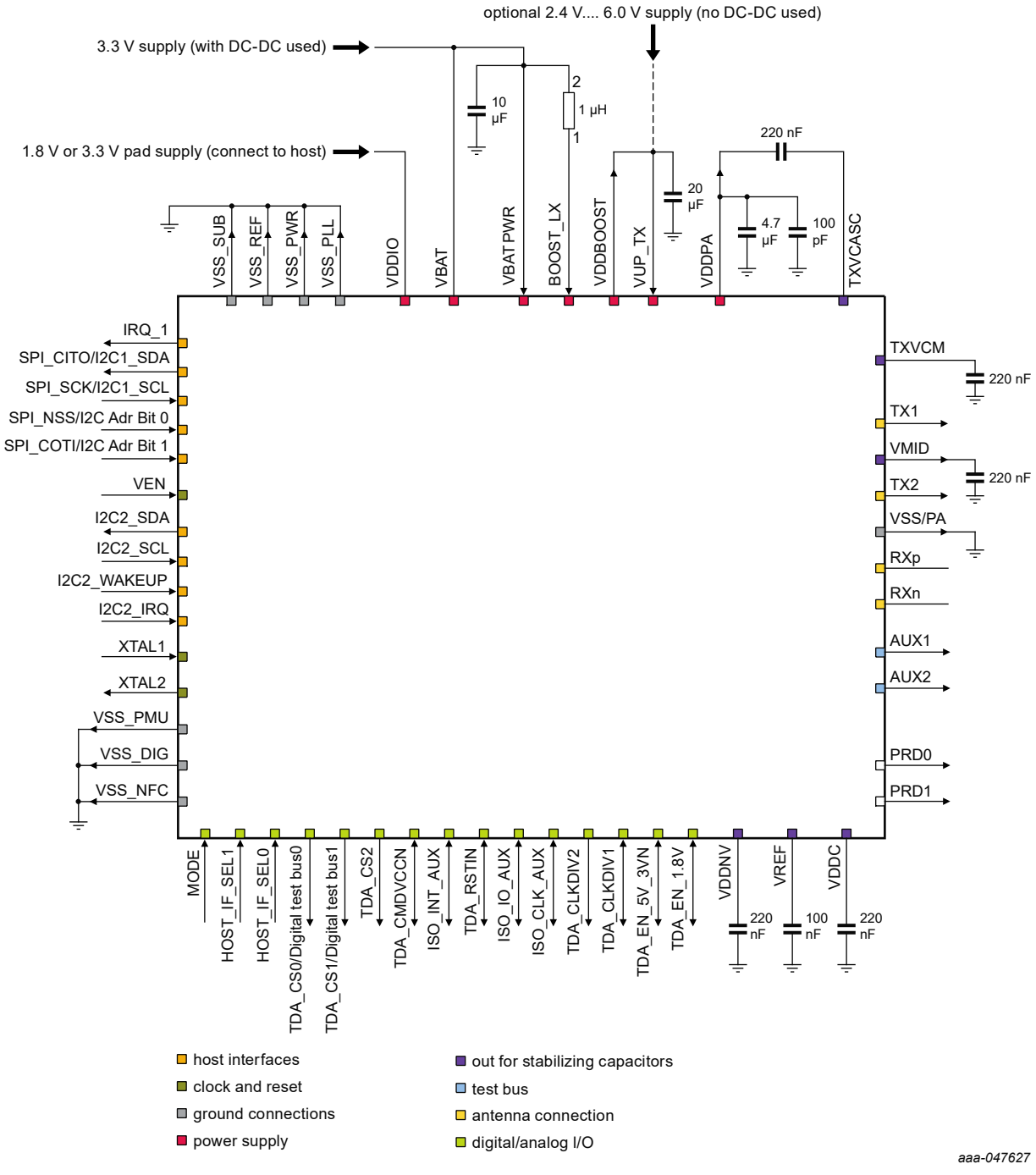

Figure 1. System connections [1]

[1] The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I^2C standards organization.

The PN7220 is connected to an application processor / host CPU based on an NCI interface.

The device offers high compatibility to existing solutions which offer an NCI interface (Host IF_1). The physical interface used for the connection is a I2C interface.

Host IF_1 allows I^2C data rates up to 3.4 Mbit/s.

I^2C address:

The PN7220 host interface 1 supports the 7-bit addressing mode, first 5-bits are fixed and is decimal 40, last two bits are configurable using ADDR0 and ADDR1 pins . This provides maximum flexibility even in cases where the I^2C bus is shared with other devices on top of the PN7220.

Default mode after boot:

The system is always booting in mode (EMVCo polling or NFC Forum polling) defined by the level on the pin MODE/GPIO2.

Switching between NFC Forum and EMVCo polling:

Switching to a EMVCo polling loop is done based on a physical signal "MODE/GPIO2" controlled by the application processor / host CPU. All previous data from earlier communications are erased, and the NCI software stack is being reset. The system enters then the new EMVCo polling mode. Switching back to NFC Forum mode again clears all previous data from earlier communication and resets the NCI software stack.

7 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP\_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(GPIO\_x)}$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	2	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	2	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

8 References

[1] Webpage – PN7220: High-Performance, One-Chip NFC Controller for EMVCo 3.2 and NFC Forum Operation (link)

[2] Data sheet – PN7220 (link)

9 Revision history

Table 4. Revision history

Document ID	Release date	Description
PN7220_SDS v.3.9	14 September 2026	Released alongside data sheet update.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Licenses

Purchase of NXP ICs with NFC technology — Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Apple — is a registered trademark of Apple Inc.

FeliCa — is a trademark of Sony Corporation.

ICODE — is a trademark of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

MIFARE Classic — is a trademark of NXP B.V.

MIFARE Plus — is a trademark of NXP B.V.

Tables

Figures

Contents