# PN76AC

## NFC controller with ultra-low-power card detection and NCI interface

Rev. 1.5 — 24 August 2026 Objective short data sheet

## 1 General description

This document describes the functionality and electrical specification of the PN76AC high power NFC controller with NCI interface.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, PN76AC is a robust solution for access solution that is generating strong RF field in a difficult environment.

PN76AC communicates with a connected host through a physical interface using the NCI 2.2 protocol.

PN76AC supports highly innovative and unique features, which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the PN76AC are mentioned in Section 15.

# 2 Features and benefits

## 2.1 RF functionality

As a highly integrated high performance full NFC Forum-compliant NFC controller for contactless communication at 13.56 MHz, this NFC controller IC utilizes an outstanding modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.

PN76AC supports the following RF operating modes:

### 2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

### 2.1.2 ISO/IEC14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kBit/s

### 2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

### 2.1.4 Card emulation

- ISO/IEC4443-A card mode from 106 kbit/s up to 848 kbit/s (PICC) with active load modulation for increased communication range.

## 2.2 Transmitter

- Transmitter with high RF output power of 2.0 W
- Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
- Adaptive waveshaping control (AWC)

## 2.3 Receiver

- Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

## 2.4 Integrated polling loop

- RF polling loop according to NFC Forum

## 2.5 RF debugging support

- RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on predefined trigger conditions.
- One digital and one analog debug signal is provided by the chip for connection of an oscilloscope

## 2.6 Host interface

PN76AC supports host connection based on SPI target interface with data rates up to 15 Mbit/s.


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PN76AC supports host connection based on $I^2C$ target interface with data rates up to 3.4 Mbit/s.


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# 3 Applications

- Aliro-based Physical Access Control


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# 4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $VDD_{(VBAT)}$ | battery supply voltage on pin VBAT | VBAT ≥ VDDIO | 2.4 | - | 5.5 | V |
| $VDD_{(VDDIO)}$ | supply voltage on pin VDDIO | 1.8 V supply | 1.62 | - | 1.98 | V |
| | | 3.3 V supply | 2.4 | - | 3.6 | V |
| $VDD_{(VDDPA)}$ | supply voltage on pin VDDPA (input of the transmitter power amplifier) | supply with VDDPA from internal VDDPA LDO | 1.5 | - | 5.7 | V |
| $I_{pd}$ | power down current | $VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, $T_{amb}$ = 25 °C, External supply by VDDIO | - | 40 | 105 | µA |
| $I_{stb}$ | standby current | $T_{amb}$ = 25 °C | - | 45 | 110 | µA |
| $I_{ULPCD}$ | average ultra low-power card detection current | $T_{amb}$ = 25 °C, VDD(VDDPA) = VDD(VDDIO) =VDD(VDD) 3.0 V, 330 ms Polling interval, 50 R antenna matching | - | 22 | - | µA |
| $IDD_{(VDDPA)}$ | supply current on pin VDDPA | supplied via VUP_TX (TX_LDO active) | - | - | 350 | mA |
| $P_{(PA)}$ | Transmitter output power | supplied via VUP_TX (TX_LDO active) | - | - | 2.0 | W |
| $T_{amb}$ | ambient operating temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB, | -40 | - | +85 | °C |
| $T_{stg}$ | storage temperature | no supply voltage applied | -55 | - | +150 | °C |
| $T_{j_max}$ | maximum junction temperature | - | - | - | +125 | °C |


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# 5 Ordering information

**Table 2. Ordering information**

| Type number | Package | | | Packing | 12NC |
|---|---|---|---|---|---|
| | Name | Description | Version | | |
| PN76ACEV/C100Y | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3. This version has the firmware v03.01.01 installed. | SOT1307-2 | Tape and Reel packing. Minimum order quantity = 4000 pcs | 9354 659 05518 |


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## 6 Block diagram

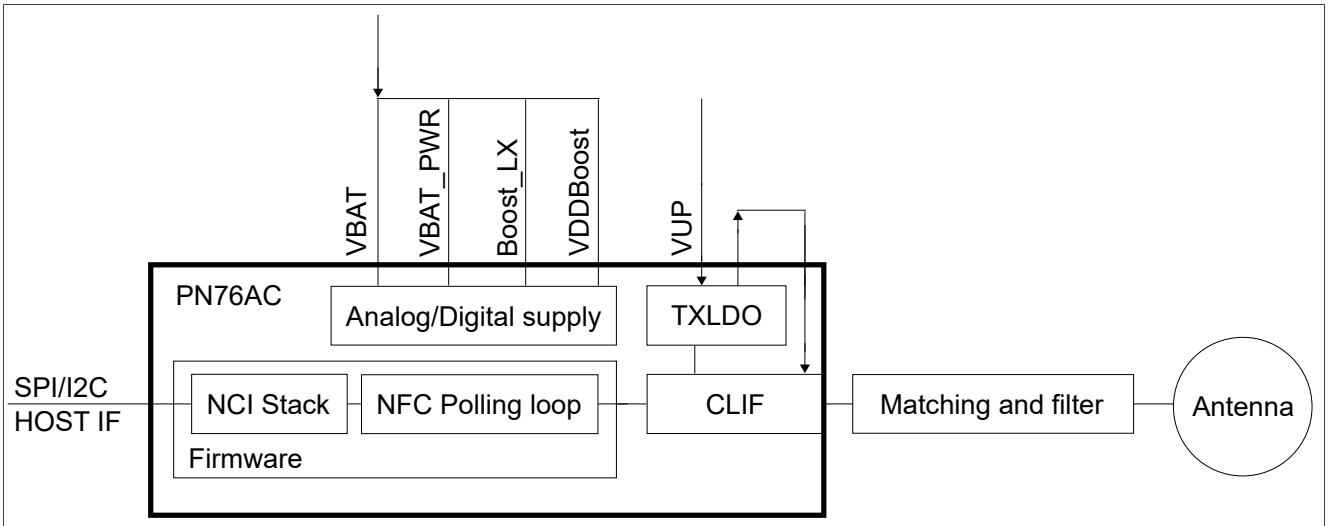


**Figure 1. Block diagram PN76AC**


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# 7 Pinning information

## 7.1 Pin description VFBGA64

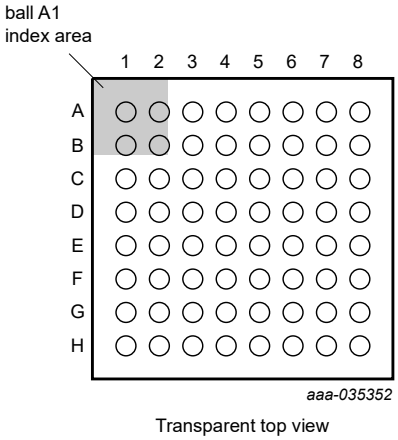


**Figure 2. Pin configuration for VFBGA64**

**Table 3. Pin description VFBGA64**

| Pin number | Symbol | Type | Description PN76AC |
|---|---|---|---|
| **Host interface** | | | |
| E6 | ATX_A | I/O | HSUART RX, $I^3C$ SDA, SPI MISO, $I^2C$ SDA |
| E5 | ATX_B | I/O | HSUART CTS, $I^3C$ SCL, SPI SCK, $I^2C$ SCL |
| D6 | ATX_C | I/O | HSUART RTS, $I^3C$ address bit 0, SPI NSS, $I^2C$ address bit 0 |
| D5 | ATX_D | I/O | HSUART TX, $I^3C$ address bit 1, SPI MOSI, $I^2C$ address bit 1 |
| B7 | IRQ | Output | Host communication / event interrupt signal |
| **XTAL connection** | | | |
| F8 | XTAL1 | Input | Crystal / system clock input |
| G8 | XTAL2 | Output | Clock output (amplifier-inverted signal output) for crystal |
| **Hardware reset** | | | |
| B3 | VEN | Input | Hardware reset, low active (independent from $V_{VDDIO}$)<br>Avoid a floating or unexpected toggling of the pin. |
| **Supply pins** | | | |
| H2 | VSS_PA | Supply GND | Transmitter ground |
| G3 | VSS_PLL | Supply GND | PLL ground (low noise) |
| A2 | VSS_PWR | Supply GND | DC-DC disabled but boost ground must be connected |
| D3 | VSS_REF | Supply GND | PMU ground |
| B2, E3 | VSS_SUB | Supply GND | Substrate ground |
| C3 | VSS_PMU | Supply GND | PMU ground |
| F4 | VSS_DIG | Supply GND | Digital ground |


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**Table 3. Pin description VFBGA64***...continued*

| Pin number | Symbol | Type | Description PN76AC |
|---|---|---|---|
| F3 | VSS_NFC | Supply GND | NFC ground |
| E1 | VBAT | Supply | System supply, used to supply the analog and digital blocks, memory and internal voltage references |
| A8 | VDDIO | Supply | I/O pads power supply |
| G1 | VDDPA | Supply | Transmitter supply |
| F1 | VUP_TX | Supply | Input supply voltage for transmitter LDO |
| B1 | VDDBOOST | Supply | DC-DC boost supply - DC-DC disabled but supply must be connected |
| A1 | BOOST_LX | Output | DC-DC disabled but output must be connected |
| A3 | VBATPWR | Supply | To be connected to BOOST_LX and transmitter power supply |
| **Outputs for stabilizing cap** | | | |
| A4 | VDDNV | Output | Nonvolatile memory power supply, to be connected to ground via a 220 nF blocking cap |
| D2 | VREF | Output | High quiescent reference voltage, to be connected to ground via a 100 nF blocking cap |
| C1 | VDDC | Output | Power supply for Digital Core, to be connected to ground via a 220 nF blocking cap |
| G2 | TXVCM | Output | Transmitter voltage common mode, to be connected to ground via a 220 nF blocking cap |
| F2 | TXVCASC | Output | TX decoupling cap, to be connected to VDDPA |
| H6 | VMID | Output | Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap |
| **RF debug signals** | | | |
| G7 | AUX1 | I/O | Test bus 1 / Digital I/O |
| F7 | AUX2 | I/O | Test bus 2 / Digital I/O |
| H8 | AUX3 | Output | Test bus 3 / GPIO 8 |
| **Antenna connections** | | | |
| H5 | RXP | Input | Receiver input "Positive" |
| H4 | RXN | Input | Receiver input "Negative" |
| H1 | TX1 | Output | Antenna driver output 1 |
| H3 | TX2 | Output | Antenna driver output 2 |
| **Wake-up / Digital debug signals** | | | |
| E8 | GPIO0/ Digital TestBus0 | Input/Output | GPIO0 / Digital test bus 0 |
| D8 | GPIO1/Digital TestBus1 | Input/Output | GPIO1 / Digital test bus 1 |
| E7 | GPIO2/ Digital TestBus2 | Input/Output | GPIO2 / Digital test bus 2 |


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**Table 3. Pin description VFBGA64***...continued*

| Pin number | Symbol | Type | Description PN76AC |
|---|---|---|---|
| D7 | WKUP_REQ / GPIO3 / Digital TestBus3 | Input | Wake-up request when in Standby and ULPCD; GPIO3 / Digital test bus 3 |
| C5 | GPIO4 | Input/Output | GPIO4 |
| B5 | GPIO5 | Input/Output | GPIO5 |
| **Host interface selection** | | | |
| C6 | HOST_IF_SEL1 | Input | Shall always be on GND on PN76AC |
| C7 | HOST_IF_ SEL0 | Input | Host interface select 0 - selection of SPI or $I^2C$<br>Level L: $I^2C$ host interface<br>Level H: SPI host interface |
| **Pins not to be connected** | | | |
| B4 | RFU | N/A | Do not connect or connect to GND |
| G4 | RFU | N/A | Do not connect or connect to GND |
| H7 | RFU | N/A | Do not connect |
| A6 | RFU | N/A | Do not connect |
| B6 | RFU | N/A | Do not connect |
| C2 | RFU | N/A | Internal test pin. To be connected to GND. |
| A7 | RFU | N/A | Do not connect |
| B8 | RFU | N/A | Do not connect |
| C4 | RFU | N/A | Do not connect |
| C8 | RFU | N/A | Do not connect |
| D1 | RFU | N/A | Do not connect |
| D4 | RFU | N/A | Do not connect |
| E2 | RFU | Output | Do not connect |
| E4 | RFU | N/A | Do not connect |
| F5 | RFU | N/A | Do not connect |
| F6 | RFU | N/A | Do not connect |
| G5 | RFU | N/A | Do not connect |
| G6 | RFU | N/A | Do not connect |
| A5 | RFU | Output | Do not connect |

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.


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# 8 Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD(VUP_TX)}$ | supply voltage on pin VUP_TX | - | -0.3 | 6.3 | V |
| $V_{DD(VBAT)}$ | supply voltage on pin VBAT | - | -0.3 | 5.8 | V |
| $V_{DD(VDDIO)}$ | supply voltage on pin VDDIO | on pin VDDIO, power supply for host interface and GPIOs | -0.3 | 3.8 | V |
| $V_{DD(GPIO_x)}$ | input voltage on pin used as GPIO | - | -0.3 | 3.8 | V |
| $V_{DD(VDDPA)}$ | supply voltage on pin VDDPA | maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated | - | 6.0 | V |
| $V_{i(RXP)}$ | input voltage on pin RXP | - | -0.3 | + 2.0 | V |
| $V_{i(RXN)}$ | input voltage on pin RXN | - | -0.3 | + 2.0 | V |
| $V_{ESD}$ | electrostatic discharge voltage | human body model (HBM)[1] | -2000 | 2000 | V |
| | | charge device model (CDM)[2] | -500 | +500 | V |
| $T_{j(max)}$ | junction temperature | - | - | 125 | °C |
| $T_{stg}$ | storage temperature | no supply voltage applied | -55 | +150 | °C |

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime. The product might not behave according to specification.


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# 9 Package outline

## 9.1 VFBGA64 package

**Table 5. Package outline VFBGA64 (SOT1307-2)**

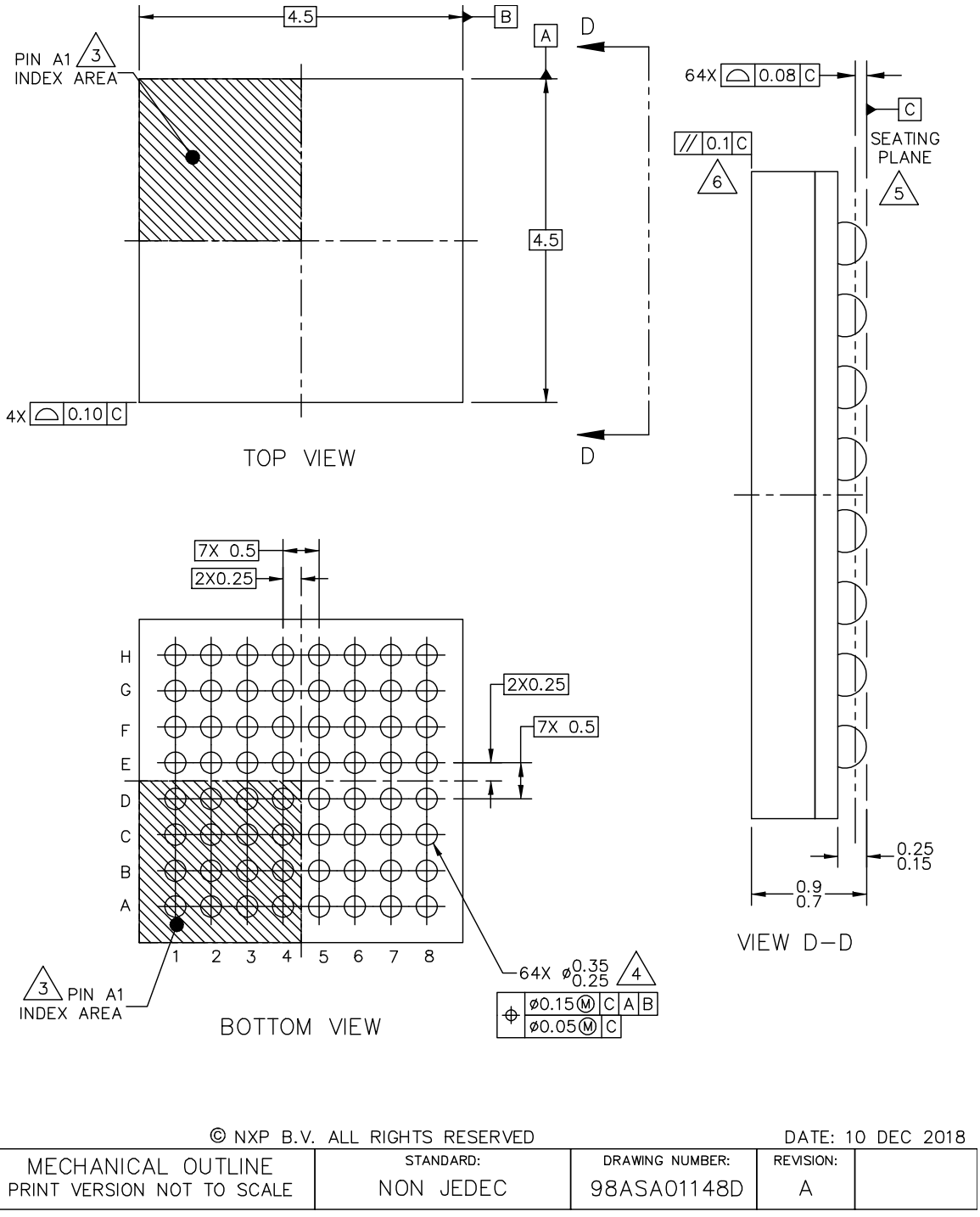


**Figure 3. Package outline VFBGA64 (SOT1307-2)**


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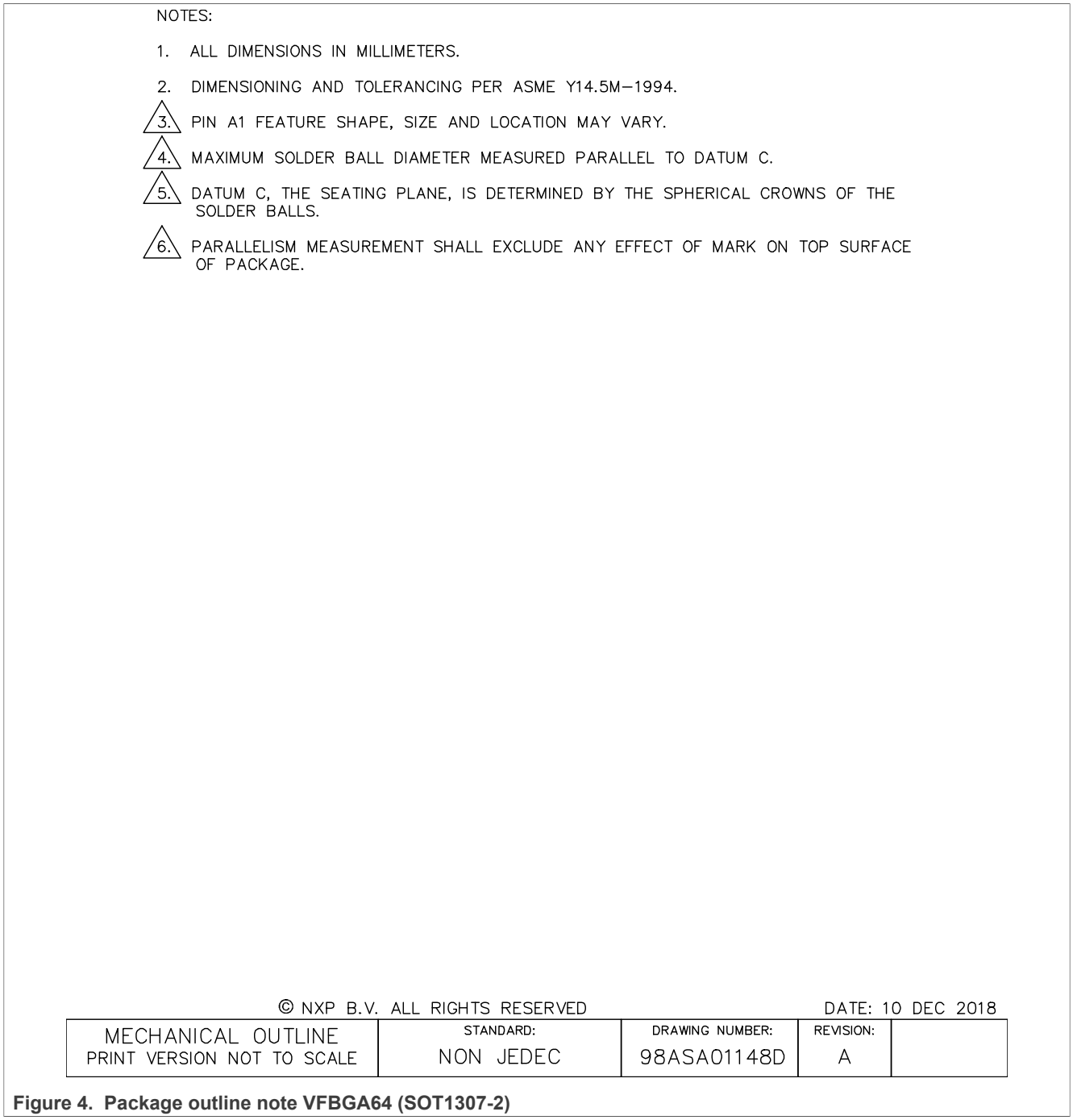


**Figure 4. Package outline note VFBGA64 (SOT1307-2)**


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# 10 Package marking

## 10.1 Package marking drawing VFBGA64

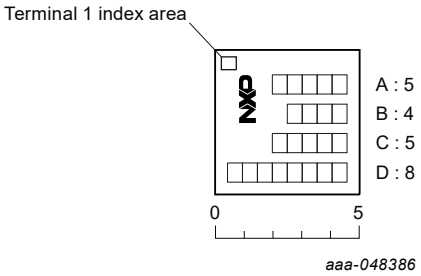


**Figure 5. VFBGA64 Package 4 line marking**

Line A: 5 characters; 76AC followed by a blank " "

Line B: Firmware version programmed during production

Line C: 5 characters; contains the diffusion batch identifier (DB ID), a blank " " and the assembly sequence identifier (AS ID)

Line D: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level (“X” = engineering samples, “ “ = released product)


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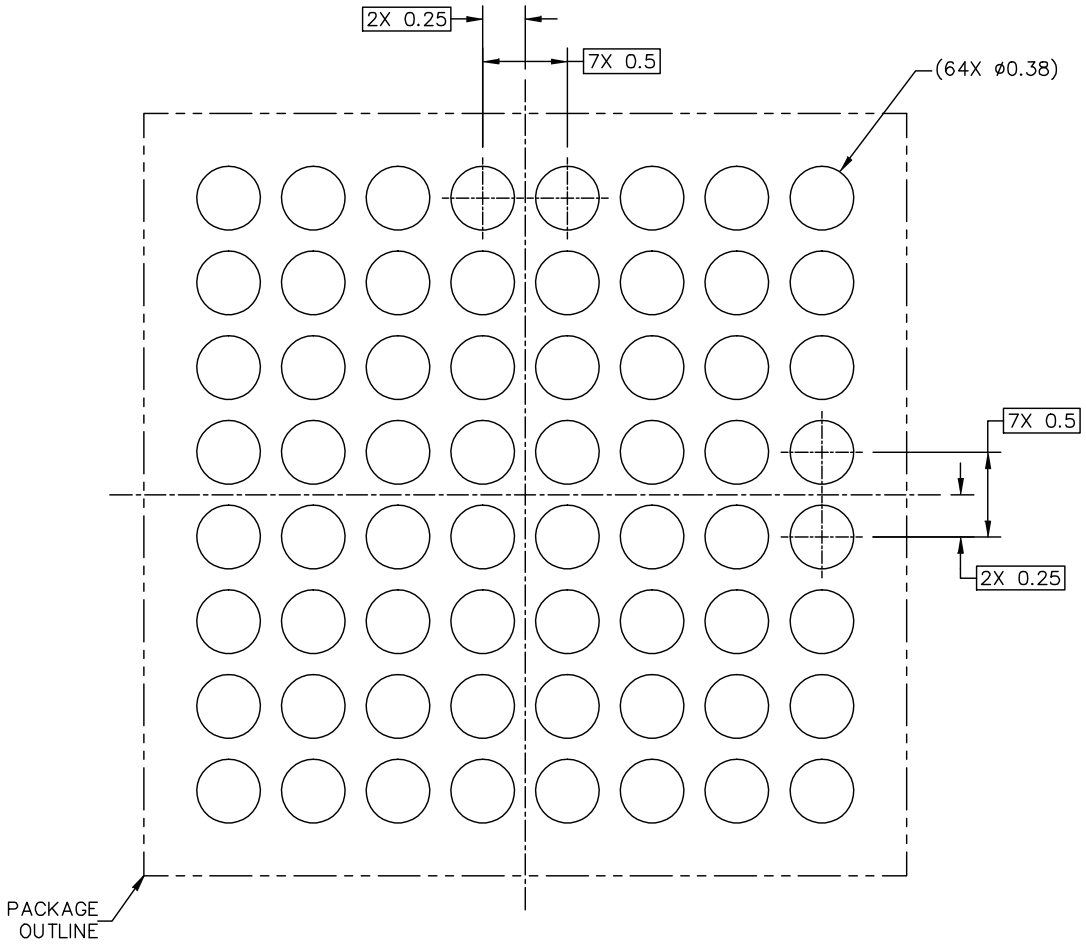
## 11 Reflow soldering footprint VFBGA64




PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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DATE: 10 DEC 2018

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01148D | REVISION:<br>A | |
|---|---|---|---|---|

**Figure 6. Reflow soldering footprint part1 for VFBGA64 (SOT1307-2)**


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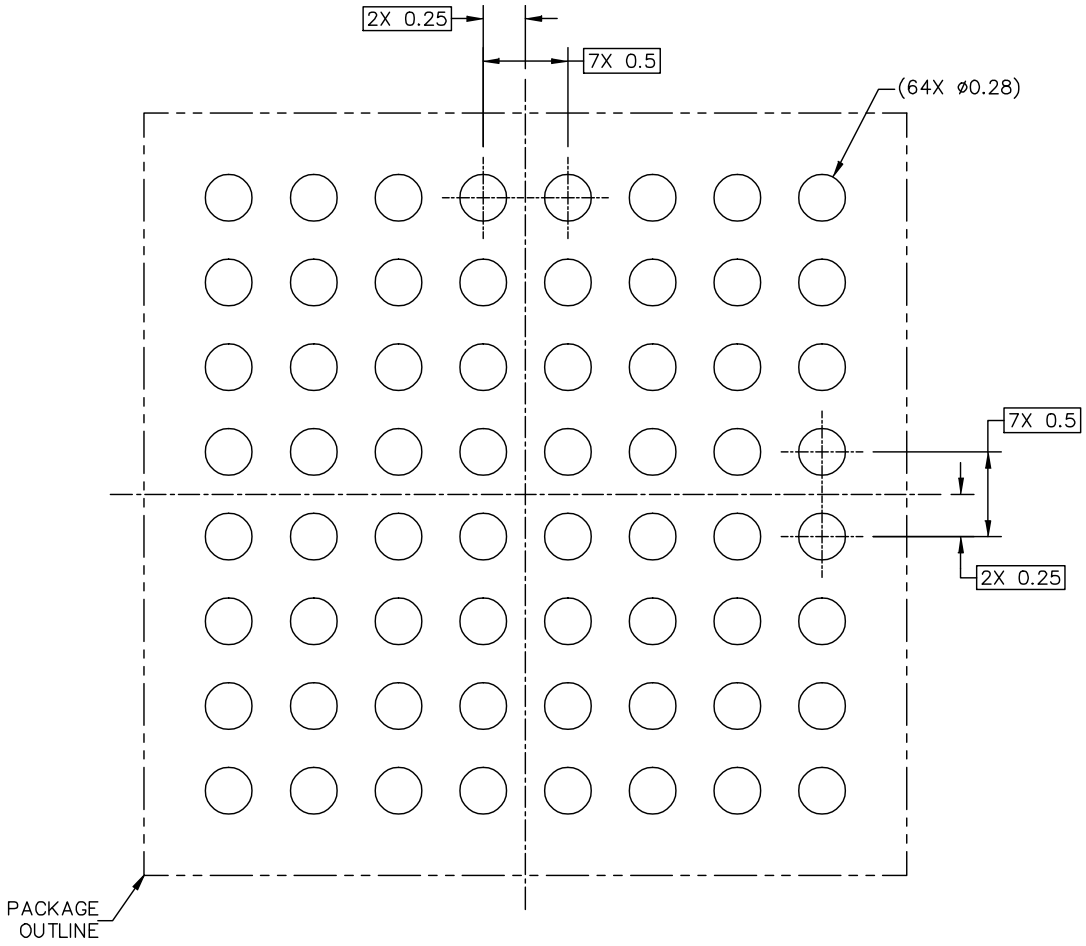


**Figure 7. Reflow soldering footprint part2 for VFBGA64 (SOT1307-2)**


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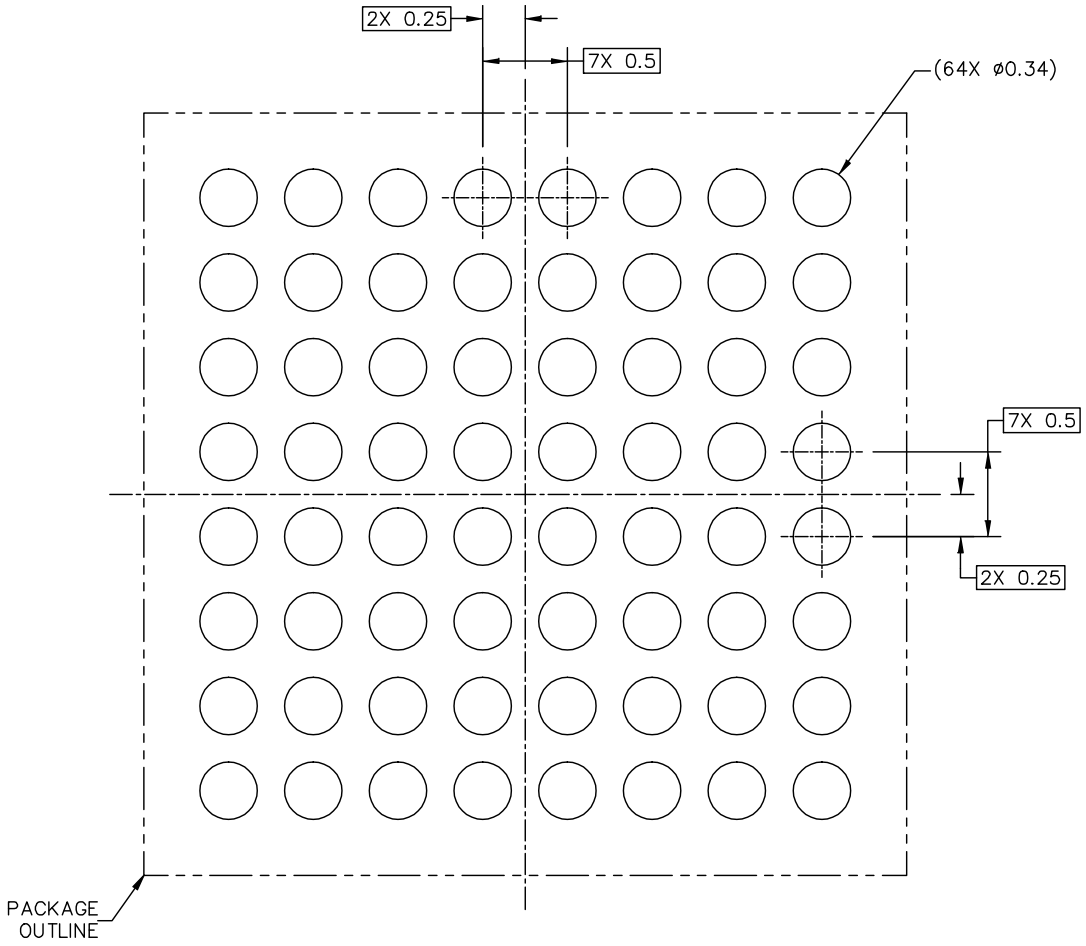


RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 10 DEC 2018

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01148D | REVISION:<br>A | |
|---|---|---|---|---|

**Figure 8. Reflow soldering footprint part3 for VFBGA64 (SOT1307-2)**


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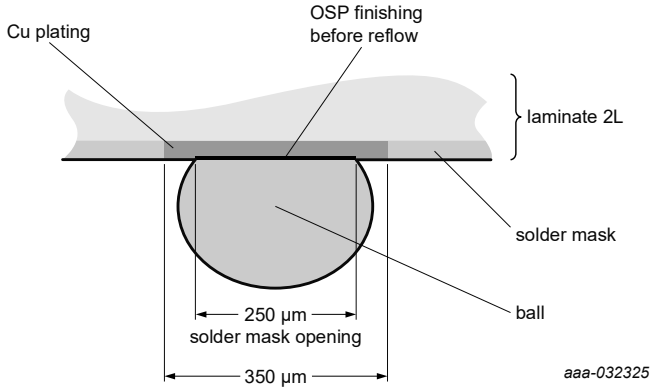


**Figure 9. Soldering and footprint representative illustration for VFBGA64 (SOT1307-2)**


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## 12 Surface mount reflow soldering

For information on surface mount, reflow soldering and component handling, refer to the Application note – AN10365 Surface mount reflow soldering. This application note provides guidelines for the board mounting and handling of NXP Semiconductor packages


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## 13 Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow soldering, to remove any moisture that might have soaked into the package.

**For MSL3:**

168h out-of-pack floor life at maximum ambient temperature. Conditions: < 30 °C / 60 % RH.

**For MSL2:**

- 1 year out-of-pack floor life at maximum ambient temperature. Conditions: < 30 °C / 60 % RH.

**For MSL1:**

- No out-of-pack floor live specification required. Conditions: < 30 °C / 85 % RH.

**CAUTION**

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.


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# 14 Abbreviations

**Table 6. Abbreviations**

| Acronym | Description |
|---|---|
| AA | audio accelerator |
| ADC | analog-to-digital converter |
| AGC | automatic gain control |
| AHB | advanced high-performance bus |
| AHB-Lite | advanced high-performance bus (single-controller implementation) |
| AHB bus | advanced high-performance bus |
| APB | advanced peripheral bus |
| API | application programming interface |
| ARC | adaptive receiver control |
| Arm | Advanced RISC Machine |
| AWC | adaptive waveshape control |
| BBA | baseband amplifier |
| BOD | brownout detection |
| CITO | controller input target output |
| CLIF | contactless interface |
| COTI | controller output target input |
| CPU | central processing unit |
| CRC | cyclic redundancy check |
| CTR | current transfer ratio |
| CTS | clear to send |
| DAC | digital-to-analog converter |
| DC-DC | switch-mode voltage regulator, which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN76AC integrates a step-up/boost converter |
| DDR | double data rate |
| DMA | direct memory access |
| DPC | dynamic power control |
| ECC | elliptic curve cryptography |
| EEPROM | electrically erasable programmable read-only memory |
| EMC | electromagnetic compatibility |
| EMD | electromagnetic disturbance |
| ETB | Embedded Trace Buffer |
| ETM | Embedded Trace Macro |
| EOF | end-of-frame |
| Fm+ | Fast-mode Plus |
| FSM | finite state machine |


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**Table 6. Abbreviations**...*continued*

| Acronym | Description |
|---|---|
| GND | Ground |
| GPIO | general-purpose input output |
| HID | human interface device |
| HPD | hard power down |
| HW | hardware |
| IC | Integrated Circuit |
| IIR | infinite impulse response |
| IrDA | Infrared Data Association |
| IAP | In-Application Programming |
| ISP | In-System Programming |
| I/O | input/output |
| I/Q | in-phase/quadrature-phase |
| JEDEC | Joint Electron Device Engineering Council |
| LDO | low dropout regulator |
| LPUART | Low-Power Universal Asynchronous Receiver / Transmitter |
| LSB | least significant bit |
| LSByte | least significant byte |
| MISO | SPI interface controller in target out |
| MSL | moisture sensitivity level |
| MOSI | SPI interface controller out target In |
| NFC | near-field communication |
| NRZ | non-return-to-zero |
| NSS | SPI interface active-low target-select signal |
| NTS | not target select |
| NVIC | nested vectored interrupt controller |
| OS | operating system |
| OTP | one time programmable |
| PCB | printed-circuit board |
| PC | personal computer |
| PCD | power card detection |
| PICC | proximity inductive coupling card |
| PLL | phase-locked loop |
| PMU | power management unit |
| PWM | pulse width modulation |
| RAM | random-access memory |
| RF | radio frequency |


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**Table 6. Abbreviations**...*continued*

| Acronym | Description |
|---|---|
| RNG | random number generator |
| ROM | read-only memory |
| RSA | Rivest, Shamir, and Adleman public key cryptosystem |
| RSSI | receiver signal strength indicator |
| RTOS | real-time operating system |
| RTS | request to send |
| SCK | SPI interface serial clock |
| SCL | $I^2C$ interface serial clock |
| SDA | serial data |
| SMPS | switch mode power supply |
| SPI | serial peripheral interface |
| SRAM | static random-access memory |
| SWD | serial wire debug |
| TFT | display technology: thin-film transistor-display |
| TX | transmit |
| UART | universal asynchronous receiver transmitter |
| UID | Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards. |
| ULPCD | ultra low-power card detection |
| USB | universal serial bus |
| VREF | voltage reference |


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## 15 References

1. Specification – Apple Enhanced Contactless Polling Specification: Version 1.1.
2. User manual – UM12399 – PN76AC user manual
3. Application note – AN13996 How to use the low-power features of the PN76 family NFC controller (link)
4. Application note – AN14518 Crystal Oscillator Design Guide (link)
5. Application note – AN10365 Surface mount reflow soldering (link)


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# 16 Revision history

**Table 7. Revision history**

| Document ID | Release date | Description |
|---|---|---|
| PN76AC_SDS v.1.5 | 24 August 2026 | Objective short data sheet.<br>Document title updated.<br>• Section 5 "Ordering information": updated. |
| PN76AC_SDS v.1.4 | 8 June 2026 | Objective short data sheet.<br>Document security status updated to "public". |
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