PTN37011

Multiprotocol USB3.2 and DisplayPort Linear Redriver

Rev. 1.0 — 14 January 2026 **Product data sheet**

Document information

Information	Content
Keywords	PTN37011, data sheet, multiprotocol linear redriver, USB3.2, DisplayPort 2.0
Abstract	PTN37011 is a high-performance USB3.2/DP2.0 multiprotocol linear redriver that is optimized for USB3.2 and DisplayPort 2.0 applications on either the downstream facing port (DFP) or upstream facing port (UFP) applications.

1 General description

PTN37011 is a high performance USB3.2/DP2.0 multiprotocol linear redriver that is optimized for USB3.2 and DisplayPort 2.0 applications on either the downstream facing port (DFP) or upstream facing port (UFP) applications. It addresses high-speed signal quality enhancement requirements for USB-Type C interface in a platform that supports the USB-Type C and VESA DisplayPort Alternate Mode standards.

PTN37011 provides programmable linear equalization and output swing linearity control by I2C interface to improve signal integrity and enable channel extension by reducing intersymbol interference (ISI). To reduce number of I2C transactions to place PTN37011 in a valid operating mode, load default channel setting values from OTP to registers upon device power-on reset.

PTN37011 is tailored to support USB3.2 electrical idle, receiver detection, and power-saving modes. It maintains two separate input signal detectors – loss of high-speed signal (LoS) and USB low frequency periodic signaling (LFPS) detectors with built-in hysteresis.

For USB3.2 operation, PTN37011 has built-in advanced power management capability that enables significant power saving under USB3.2 low power modes (U2/U3). It detects LFPS to configure the operation (USB3.2 Gen 1/Gen 2 x1) and link electrical conditions and it activates/deactivates internal circuitry and logic dynamically. The device performs these actions without host software intervention and conserves power. The host processor keeps PTN37011 in deep power saving or USB3.2 mode until alternate mode has been entered.

While operating in DisplayPort mode, AUX snooping is performed to follow relevant DisplayPort source-sink AUX transactions and configure the redriver to meet link requirements. Entering and exiting DisplayPort low power mode (D3) is based on either AUX snooping result, or LoS detector status.

An enable control pin can place the chip in a disabled state to achieve low power consumption. PTN37011 is powered from 1.8 V and 1.2 V supplies, and is available in a small high performance WLCSP package.

2 Features and benefits

- Flexible multiprotocol linear redriver supports three signaling combinations specified in the USB-Type C and VESA specifications
  - Mode 0: Deep Power saving
  - Mode 1: USB3.2 Gen1 x 1 / Gen2 x 1
  - Mode 2: USB3.2 + DP 2-Lane + AUX snooping
  - Mode 3: DP 4-Lane + AUX snooping
- Supports USB 3.2 Gen1 x 1, Gen2 x 1 (5 Gbit/s and 10 Gbit/s)
  - Implement controlled power on/off aligned with the latest USB3.2 specification and computing platform capabilities
  - Automatic receiver termination detection
  - I2C register based flat gain, peaking gain, and output linearity controls
  - Flat gain of +1 dB, 0 dB, and -1 dB
  - Peaking gain of 12 dB at 5 GHz
  - Output linearity control: 600 mVppd, 700 mVppd, and 800 mVppd
- Supports DisplayPort link rates at 1.62 Gbit/s (RBR), 2.7 Gbit/s (HBR), 5.4 Gbit/s (HBR2), 8.1 Gbit/s (HBR3), 10 Gbit/s (UHBR10)
  - DisplayPort AUX monitoring during DP link training to enable DP channels
  - Flat gain of +1 dB, 0 dB, and -1 dB
  - Peaking gain of 12 dB at 5 GHz
  - Output linearity control: 600 mVppd, 700 mVppd, and 800 mVppd
- Supports DP2.0, USB3.2 standard and USB-Type C Alternate Mode interoperability testing
  - Implements USB-Type C safe state conditions on all connector facing pins
- Signal integrity
  - Integrated termination resistors provide impedance matching on both transmit and receive sides
  - Receiver equalizers on all high-speed inputs to compensate for signal attenuation
  - Good linearity over the frequency band (50 MHz to 5 GHz) and voltage dynamic range
  - Excellent differential return loss performance: < -13 dB up to 5 GHz
  - Low crosstalk: DDNEXT < -45 dB up to 5 GHz
- Low active current consumption for output swing linearity control of 800 mVppd
  - USB3.2 Gen1/2 x 1 (Mode 1) U0 state: 170 mW (Typ)
  - 1 lane DP UHBR10 (Mode 2 or 3): 89 mW (Typ)
  - 2 lane DP UHBR10 (Mode 2 or 3): 170 mW (Typ)
  - 4 lane DP only UHBR10 (Mode 3): 334 mW (Typ)
- Power-saving states
  - Disabled state (EN = LOW): 30 µW (Typ)
  - Deep power-saving state (Mode 0): 73 µW (Typ)
  - USB3.2 (Mode 1)
    - USB3 x1 U1 state is not supported
    - USB3 x1 U2/U3 state: 1.23 mW (Typ)
    - RX detection (enabled when no connection is detected): 1.01 mW (Typ)
  - DisplayPort (Mode 3)
    - D3 mode: 0.54 mW (Typ)
- GPIO pins (SCL/SDA/DTB/AUXP/AUXN) are fail-safe when device power supplies are not present, or ramping up/down
  - Present as high-impedance

  - Low leakage current
- Power supplies
  - VCC0/1/2, VDDD: 1.62 V to 1.98 V (1.8 V ± 10 %)
  - VDD_{IO}: 1.08 V to 1.32 V (1.2 V ± 10 %)
- Small high performance 32 pin WLCSP package
- Tolerant to VBus short fault events up to 15 V, across AC capacitors on high-speed, and AUX snooping pins with external TVS diodes
- IEC61000-4-2 contact discharge at ±8 kV, with appropriate TVS diodes and AC capacitors on high-speed and AUX snooping pins
- ESD HBM 1.25 kV, CDM 500 V
- Operating temperature range -20 °C to +85 °C

3 Applications

- For USB-Type C host/source application:
  - Smartphones and tablets
  - Notebooks, AIO, and desktop computers
  - Hub or dock devices
- For USB-Type C device/sink application:
  - Docking stations
  - Display units

4 Ordering information

Table 1 describes the ordering information for PTN37011.

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PTN37011UK	WLCSP32	Wafer Level Chip Scale Package, 32 terminals, 0.35 mm pitch, 2.79 mm x 1.39 mm x 0.46 mm body (backside coating included)	SOT2166-1

4.1 Ordering options

Table 2 describes the ordering options for PTN37011.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
PTN37011UK	PTN37011UKZ	WLCSP32	REEL 13" Q1 DP CHIPS	15000	T_{amb} = -20 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

5 Block diagram

Figure 1 shows the labeled block diagram of PTN37011.

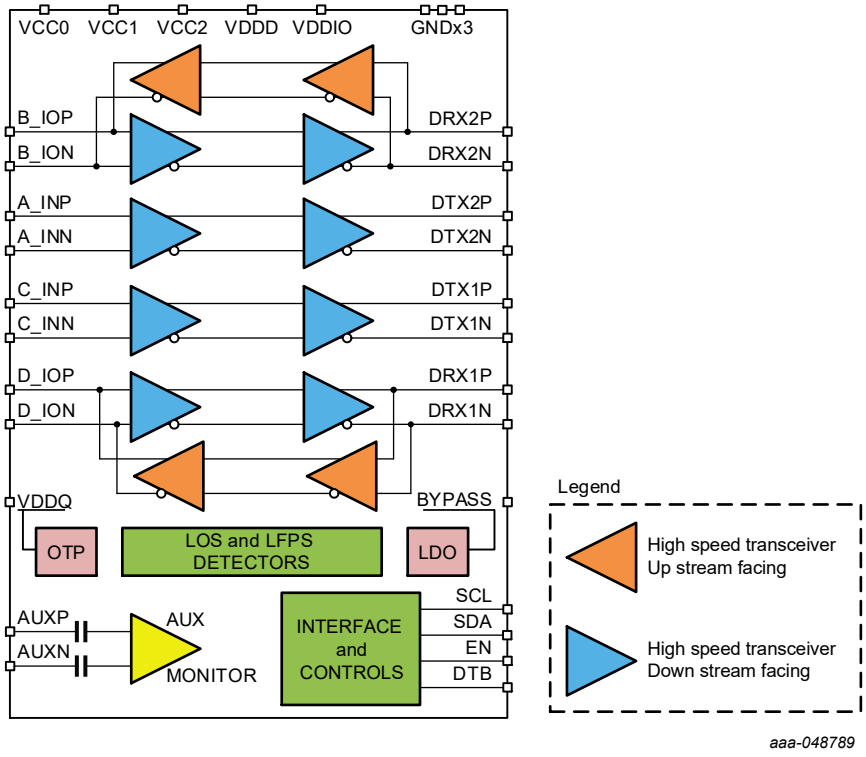


Figure 1. PTN37011 block diagram

6 Pinning

This section provides the pin configuration and description of PTN37011.

6.1 Pinning

Figure 2 show the pinning for PTN37011.

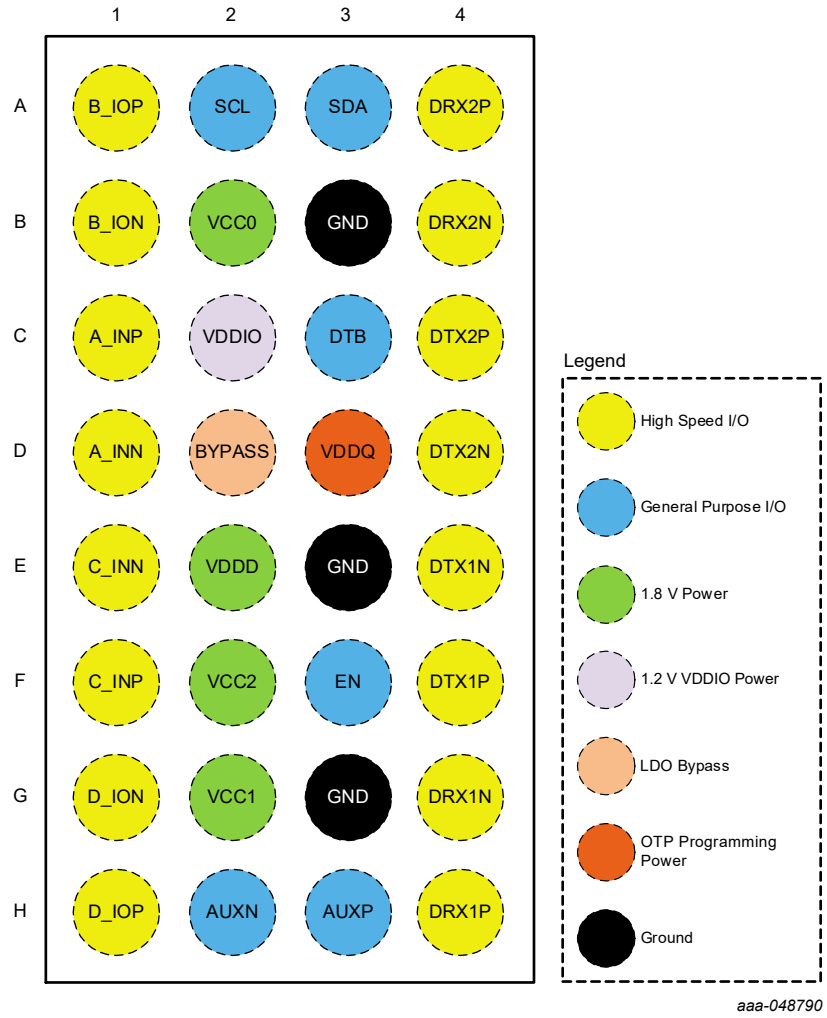


Figure 2. Pinning (transparent top view)

6.2 Pin description

Table 3 provides detailed description of various pins on PTN37011.

Table 3. Pin description

Symbol	Pin Name	Type	Description
A1	B_IOP	Self-biasing differential input/output	Differential signal high-speed input/output. B_IOP makes a differential pair with B_ION. The associated output/input pair is DRX2P and DRX2N. The mode setting controls the I/O configuration.
B1	B_ION		

Table 3. Pin description...*continued*

Symbol	Pin Name	Type	Description
C1	A_INP	Self-biasing differential input	Differential signal from high-speed RX path. A_INP makes a differential pair with A_INN. The associated TX output pair is DTX2P and DTX2N. The mode setting controls the I/O configuration.
D1	A_INN		
E1	C_INN	Self-biasing differential input	Differential signal from high-speed RX path. C_INP makes a differential pair with C_INN. The associated TX output pair is DTX1P and DTX1N. The mode setting controls the I/O configuration.
F1	C_INP		
G1	D_ION	Self-biasing differential input/output	Differential signal high-speed input/output. D_IOP makes a differential pair with D_ION. The associated output/input pair is DRX1P and DRX1N. The mode setting controls the I/O configuration.
H1	D_IOP		
A4	DRX2P	Self-biasing differential input/output	Differential signal high-speed input/output. DRX2P makes a differential pair with DRX2N. The associated output/input pair is B_IOP and B_ION. The mode setting controls the I/O configuration.
B4	DRX2N		
C4	DTX2P	Self-biasing differential output	Differential signal of high-speed TX path. DTX2P makes a differential pair with DTX2N. The associated RX input pair is A_INP and A_INN. The mode setting controls the I/O configuration.
D4	DTX2N		
E4	DTX1N	Self-biasing differential output	Differential signal of high-speed TX path. DTX1P makes a differential pair with DTX1N. The associated RX input pair is C_INP and C_INN. The mode setting controls the I/O configuration.
F4	DTX1P		
G4	DRX1N	Self-biasing differential input/output	Differential signal high-speed input/output. DRX1P makes a differential pair with DRX1N. The associated output/input pair is D_IOP and D_ION. The mode setting controls the I/O configuration.
H4	DRX1P		
A2	SCL	Open-drain input	This pin is a peripheral I2C clock pin, and an external pullup resistor to VDD_{IO} supply (1.2 V) is required.
A3	SDA	Open-drain input/output	This pin is a peripheral I2C data pin, and an external pullup resistor to VDD_{IO} supply (1.2 V) is required.
H3	AUXP	Input	DisplayPort AUX channel snooping input
H2	AUXN		
F3	EN	Input	1.2 V compatible asynchronous chip enable input during normal operation
C3	DTB		Reserved. Leave this pin as open during normal operation.
B2	VCC_0	Power	1.8 V power supplies for high-speed differential channels. $VCC_{0/1/2}$ and VDD_D pins must be tied together on the PCB.
G2	VCC_1		
F2	VCC_2		
E2	VDD_D	Power	1.8 V digital supply for AUX snooping and digital blocks. $VCC_{0/1/2}$ and VDD_D pins must be tied together on the PCB.
C2	VDD_{IO}	Power	1.2 V supply for I2C/AUX/EN interface pins
D2	BYPASS	Power	Internal LDO bypass pin. A decoupling capacitor value of 2.2 µF must be placed on this pin to GND.
D3	VDDQ	Power	OTP programming voltage supply. This pin must tie to the GND during normal operation.
B3	GND	Ground	These pins must be connected to system ground plane for electrical grounding.
E3	GND		
G3	GND		

7 Functional description

7.1 Power-on reset

PTN37011 powers up to disabled state after VDD_D, $VCC_{0/1/2}$, and VDD_{IO} reach their respective valid voltages, regardless of the power supply sequence applied. After all power rails reach valid operating voltage levels, the lowest power consumption is achieved by driving the EN pin LOW. If the EN pin is held HIGH before supplies ramp up and after all power rails reach their respective valid voltages, the lowest power state (EN = 0) is omitted. PTN37011 continues to complete its power on sequence to safe state (mode = 0).

When EN pin transitions from LOW to HIGH state:

- The internal LDO is powered up to supply digital and analog power
- The FRO clock, analog, and digital blocks are initialized
- Internal register values are reset to default values
- OTP contents are read out and populated in the channel setting registers

PTN37011 is ready to accept any I2C command after t_{READY} time.

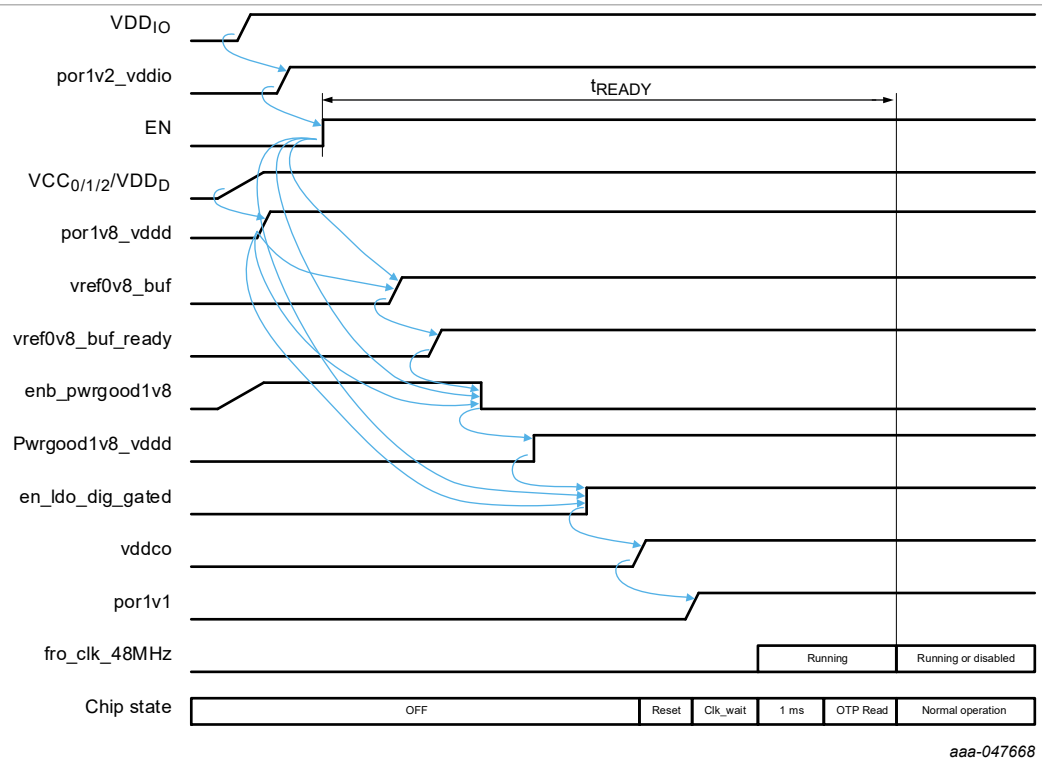


Figure 3. PTN37011 power up sequence

If 1.8 V (VDD_D, $VCC_{0/1/2}$) dips below 1.55 V, or if 1.2 V (VDD_{IO}) dips below 1.08 V, PTN37011 behavior is not predictable. Once the power rails stabilize to their valid operating voltage, the system must toggle EN pin LOW for at least 500 µs (t_{EN_RESET}) to ensure that all blocks are reinitialized properly and to restore functionality.

There is a built-in glitch filter on the EN pin input. After EN input is driven HIGH, any LOW pulse that is less than 50 ns is ignored. If system wants to disable and re-enable PTN37011, EN must stay LOW for minimum of 500 µs (t_{EN_RESET}) to ensure all digital and analog blocks are shut down properly before EN pin goes HIGH again. Similarly, when EN pin input is driven LOW, any HIGH pulse that is less than 50 ns is also ignored.

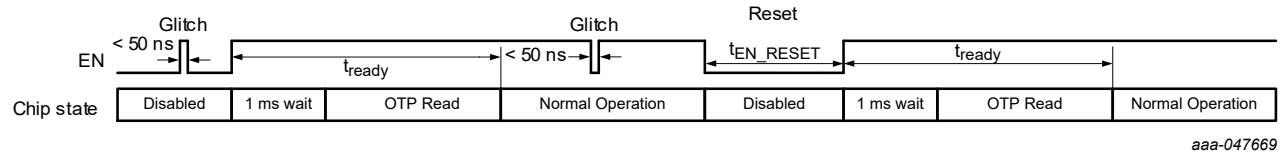


Figure 4. EN pin glitch filter and reset

7.2 Soft reset

An I2C controller can issue a soft reset by writing a '1' to register [0x05] bit [0]. A soft reset resets digital logic, including restoring I2C register contents to default values and loading channel register values from OTP shadow registers (instead of reading from OTP directly). Analog circuits (band gap, internal LDO, POR, power good, and FRO clock) are not powered down. High-speed analog transceivers are reinitialized to the same condition as in deep power-saving state.

If the programming register [0x05] is part of a series of transactions separated by repeated-START conditions, the soft reset process cannot start until the STOP condition is reached. After soft reset starts, PTN37011 is ready to receive any I2C transaction again after 60 µs.

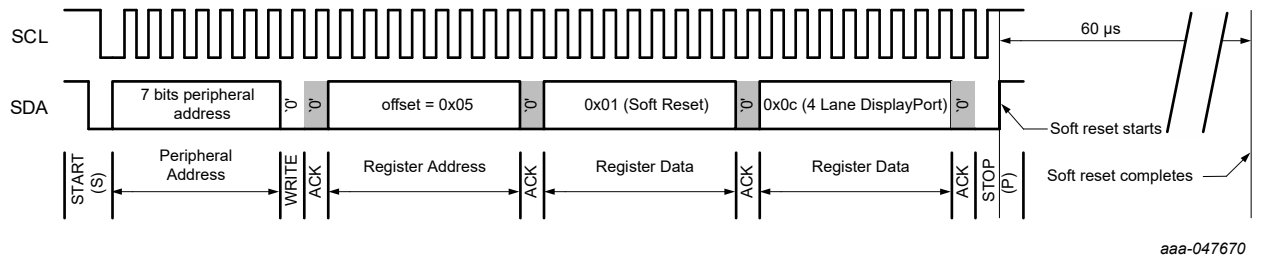


Figure 5. Soft reset I2C transaction and timing

7.3 Mode transitions

After PTN37011 is powered up and enabled, the device enters deep power-saving state (DPSS). In DPSS, all high-speed pins are put in USB safe state and the AUX snooping function is disabled. When a valid Type-C host/device is connected, the PD controller places the PTN37011 in USB3 mode (mode 1) as the default operating mode. Once DP Alternate Mode is negotiated, PTN37011 adheres the USB safe state requirements before making the mode transition.

The mode transitions follow the USB safe state transition requirements of the USB-Type C cable and connection specification, USB Power Delivery specification, and Alternate Mode specification. Figure 6 illustrates the various functional modes and deep power-saving state transitions.

DFP/UFP and orientation selections must be determined before entering modes 1, 2, or 3. Once a valid operating mode is entered, the user can configure PTN37011 to transition between different modes at any time, with fixed DFP/UFP and orientation selections. The user must transition to mode 0 (DPSS) first with new DFP/UFP and/or orientation settings before transitioning to a different mode if DFP/UFP and/or orientation selections must be modified during mode transition.

While in mode 1, the non-config lane is held in the USB-C safe state of USB3. It is possible to transition from DP 4-Lane to USB only without entering a deep power-saving state, or vice versa. PTN37011 takes care of transition to USB Safe state internally.

The I2C controller must not perform burst read/write at 1 MHz bit rate to PTN37011 while the device is in USB3 only state (mode = 1). Only the first byte of data read/written from/to PTN37011 executes correctly, while the other following bytes of data could be invalid. In this case, burst read/write transactions must be done at a lower bit rate such as 100 kHz (standard mode) or 400 kHz (fast mode).

When transitioning from mode 1 to mode 2, the USB3 connectivity is left undisturbed and DP 2-Lane + AUX functionality is included. When transitioning from mode 2 to mode 1, USB3 connectivity is left undisturbed while the DisplayPort redriver function is disabled.

When transitioning from mode 2 to mode 3, the current ongoing DisplayPort operation is not disturbed. When transitioning from mode 3 to mode 2, the operations for DP, ML2, and ML3 are interrupted, and cause display issues if all four lanes remain active from the perspective of the system. It is the responsibility of the system (chipset or PD controller) to toggle HPD signaling and initiate a new AUX training session, so that the correct number of lanes are set up accordingly.

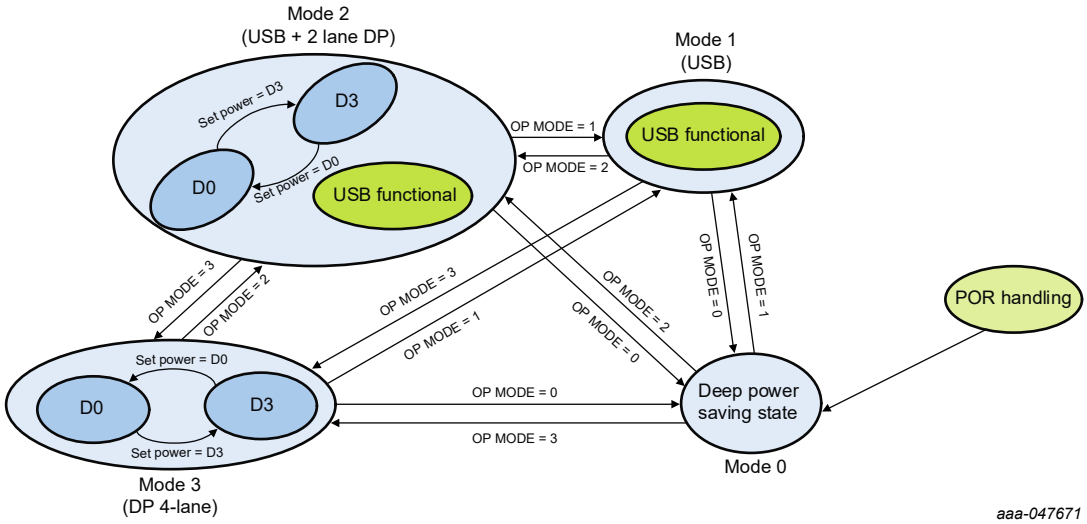


Figure 6. Mode transition state diagram

7.4 USB3.2 operation

PTN37011 supports USB3.2 redriver operation at Gen1 (5 Gbit/s) and Gen2 (10 Gbit/s) data rates. The receiver equalization (flat gain, peaking gain, and output linearity control) is configured through I2C register settings. Default values of these registers load from OTP after the device powers up and EN pin transitions from LOW to HIGH, or load from OTP shadow registers when a software reset issues through the I2C register [0x05] bit [0].

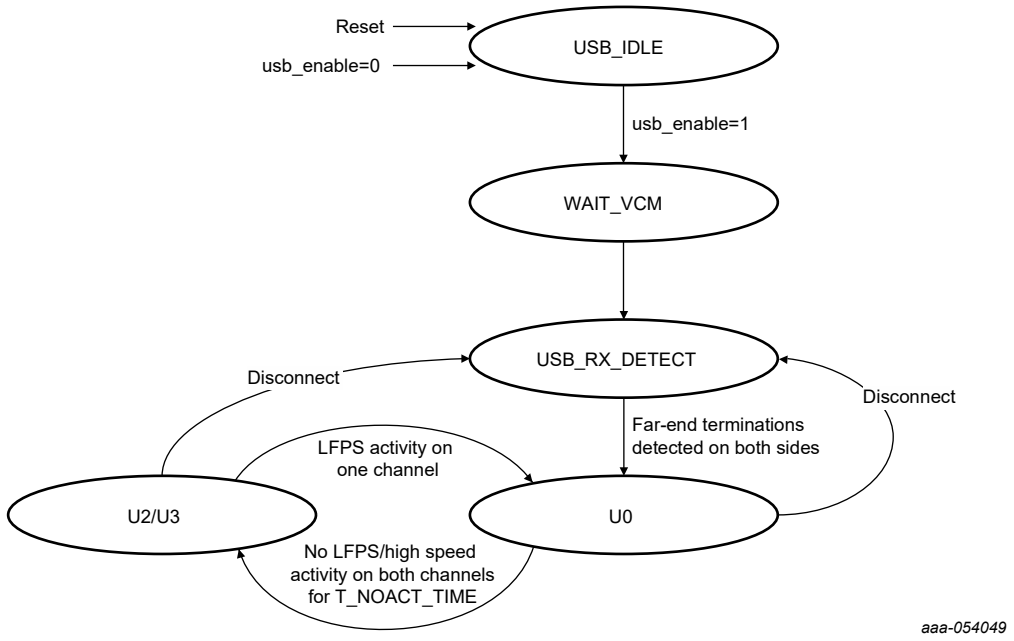


Figure 7. PTN37011 USB3 state machine

PTN37011 implements an advanced power management scheme that operates in tune with USB3 bus electrical condition. Though the device does not decode USB3 power management commands (related to USB3 U1/U2/U3 transitions) exchanged between USB3 host and device, it relies on bus electrical conditions and register settings to decide to be in one of the following states:

- Active state, wherein the device is fully operational. In this state, the USB connection exists and the received termination remains active.
- Power-saving state, wherein some portions of the TX and RX channels are kept enabled. In this state, LoS detector, LFPS detection, and/or receive termination detection circuitry are active. Based on the USB connection, there are two possibilities:
  - No USB connection (also called RX-detect state)
    - Receive termination detection circuitry keeps polling periodically
    - RX and TX signal paths (including LoS detector) are not enabled
    - Receive termination is not active
  - When a USB connection exists and when the link is in USB U2/U3 mode
    - Receive termination detection circuitry keeps polling periodically
    - RX and TX signal paths are not enabled; LFPS detector is enabled, LoS detector is disabled
    - Receive termination is active

7.4.1 USB3 state machine manual control

PTN37011 provides optional manual control of the USB state machine in U0/Active state or U2/U3 low-power state, or transitions from low-power state back to U0/Active state. The system can choose to disable the LoS detector in U0/Active state and/or the LFPS detector in U2/U3 state. When the LoS detector is disabled in U0/Active state, absence of high-speed signals does not cause PTN37011 to transition to low-power states. When the LFPS detector is disabled in U2/U3 state, receiving U2 exit or U3 wake-up LFPS signals does not cause PTN37011 to transition to U0/Active states.

To enable USB3 state machine manual control, system must set register [0x0F] bit [6] to 1 (LoS detector disable in U0/Active state) and set register [0x0F] bit [3:2] to b'00 (U0/Active state) when PTN37011 is in deep power-

saving state. Optionally, system can set the register [0x0F] bit [7] (LFPS detector disable in U2/U3 state) to either 0 or 1 when PTN37011 is in deep power-saving state, or any other USB functional modes (mode 1 or 2).

The system can then transition to USB functional modes (mode 1 or 2). USB state machine first establishes a common mode voltage (WAIT_VCM) and starts performing far end RX detection (RX.DETECT state). After both TX and RX channels' far-end terminations are detected, the USB state machine is directed to U0/Active state by register [0x0F] bit [3:2]. Since LoS detector is disabled in this U0/Active state, absent of high-speed signals do not cause PTN37011 to transition to low-power states. There are two ways to exit U0/Active state:

- To transition to RX.DETECT state, a warm reset LFPS signal must be received on one of the channel inputs.
- To force transition to U2/U3 state, the system can set register [0x0F] bit [3:2] to b'01 (U2/U3 state). At the same time, the system must set up register [0x0F] bit [7] with a proper value, such that it affects the exit condition of U2/U3 state to U0/Active state.

When PTN37011 transitions into U2/U3 state, high-speed signal paths are disabled, and only LFPS signals pass through the channels. Any ongoing high-speed signal coming into PTN37011 is suppressed at the output. Depending on register [0x0F] bit [7] value, PTN37011 can exit U2/U3 state when:

- If register [0x0F] bit [7] = 0 (LFPS detector is enabled during U2/U3 state), upon receiving U2 exit, U3 wake-up, or warm reset LFPS signals on at least one channel, transitions USB state machine to U0/Active state. After transitioning in U0/Active state, register [0x0F] bit [3:2] self-clears to b'00.
- If register [0x0F] bit [7] = 1 (LFPS detector is disabled during U2/U3 state), the system must set register [0x0F] bit [3:2] = b'11 (transition from U2/U3 state to U0/Active state) to force USB state machine to return to U0/Active state. After transitioning in U0/Active state, register [0x0F] bit [3:2] self-clears to b'00.
- If removal of any far end termination is detected during U2/U3 state, the USB state machine transitions to RX.DETECT state. If far-end terminations on both sides of PTN37011 are detected again, USB state machines continue to transition into U0/Active state, and register [0x0F] bit [3:2] self-clears to b'00 depending on the state of register [0x0F] bit [7].

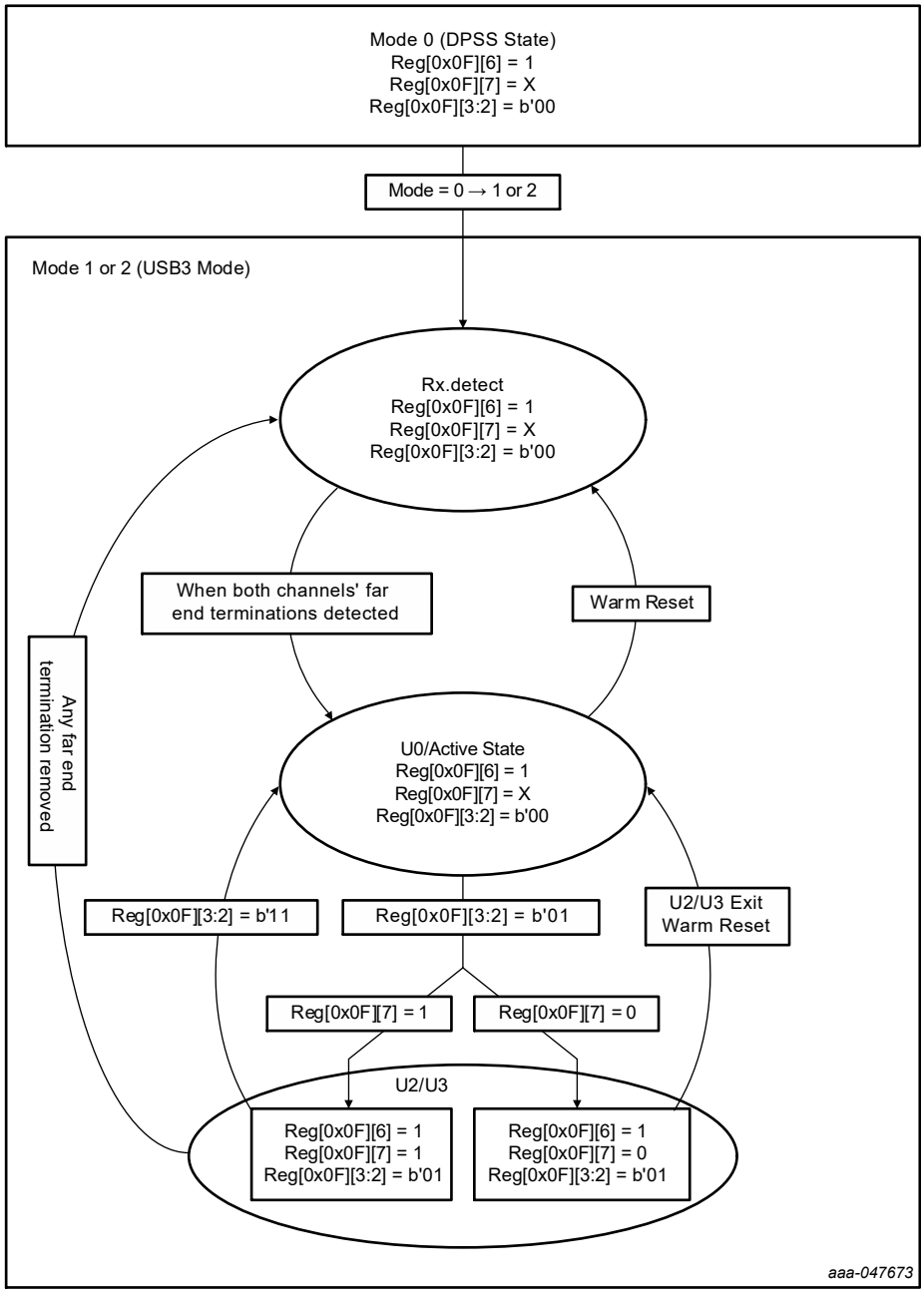


Figure 8. USB3 state machine manual control flowchart

7.5 DisplayPort operation

PTN37011 supports DisplayPort v2.0 operation at RBR (1.62 Gbit/s), HBR (2.7 Gbit/s), HBR2 (5.4 Gbit/s), HBR3 (8.1 Gbit/s), and UHBR10 (10 Gbit/s), with receiver equalization and linearity controls configured through I2C register settings. Default values of these registers load from OTP after the device powers up and EN pin transitions from LOW to HIGH, or load from OTP shadow registers when a software reset issues through I2C register [0x05] bit [0].

The DisplayPort mode is selected only when DP alternate mode enters by the host PD controller. The DisplayPort source can activate power down via an AUX command. The DisplayPort specification supports

two modes – D0/active, or D3/Low power mode. In D0 mode, the linear redriver data path is active depending on the state of the DP link. In D3 mode, the AUX snooping logic is active while high-speed paths are disabled, which results in lower current consumption.

The DisplayPort lane count is configured during the DisplayPort link training phase based on AUX communication exchanges between source and sink. PTN37011 uses lane count information to enable the transmitters and receivers. It is possible that only a subset of lanes get selected during DP Link training and the remaining lanes are not active. Depending on the number of lanes selected, PTN37011 is configured to operate with the selected lane count and therefore, saving power consumption on unused lanes.

PTN37011 does not support AUX-less ALPM.

7.5.1 AUX monitoring and configuration

PTN37011 monitors DP AUX communication exchanges that occur between DP source and DP sink. It detects AUX communication involving DPCD register controls (lane count, sleep, and wake) and configures its operation suitably. The AUX monitor function is enabled when operating mode is set to mode 2 (USB+DP 2-Lane) or 3 (DP 4-Lane), and is disabled in other mode settings.

The list of DPCD registers (with only the relevant bit fields) supported are as follows:

- LANE_COUNT_SET (DPCD Address 0002h)
- SET_POWER_STATE (DPCD Address 00600h, bit [2:0])
- Other DPCD registers, LTTPR DPCD registers, and I2C over AUX transactions are not decoded

I2C registers determine the input receiver equalization. All lanes of DP Redriver can be configured separately on a per lane basis. When the Lane count is set via AUX, the legal values are 1, 2, and 4. If AUX tries to set it to 0, PTN37011 ignores it and continues with the last known legal value. When the Lane count is set via I2C, then the legal values are 0, 1, 2, and 4. If I2C sets it to 0, PTN37011 disables all the lanes.

- Operational Mode = 0/1, possible DP Lane count = 0
- Operational Mode = 2, possible DP Lane count = 1 or 2
- Operational Mode = 3, possible DP Lane count = 1, 2, or 4

7.6 Signal detectors

PTN37011 implements two types of signal detectors:

- The LFPS detector is used to detect LFPS signaling on high-speed data path, and is implemented only on lanes wherein USB3 data flows. The LFPS detector has a nominal bandwidth of 433 MHz.
- Loss of (high-speed) signal detector (LoS detector) is meant for detecting both presence and absence of high-speed signal at the input pins over all protocols – USB3 and DisplayPort. The LoS detection is used to enter and exit from low-power states.

Based on LoS detector output, PTN37011 turns off certain portions of the internal circuitry and optimizes current consumption under various modes: USB3 (U2/U3), DisplayPort (D3 mode), and especially under electrical idle conditions. For DisplayPort operation, the following power management methods are used:

- DisplayPort entry:
  - (00b) Wait for AUX snoop transaction and then start up.
  - (01b) Wait for high-speed data input and then start up.
  - (10b - default) Wait for AUX snoop transaction, then wait for LoS detector to detect HS signal to start up.
  - (11b) Wait for AUX snoop transaction or high-speed data input and then start up.
- D3 entry:
  - (00b - default) Wait for POWER_STATE register set to D3.

- (01b) LoS detector detects absence of high-speed signals - This option must not be used if the DP source and DP sink support AUXless ALPM.
- (10b) Wait for POWER_STATE register set to D3, and when LoS detector detects absence of high-speed signals.

- D3 exit:
  - (00b - default) Wait for AUX snooping transaction to transition back to D0, and then wake up.
  - (01b) Wait for high-speed data input and then wake up - This option must not be used if the DP source and DP sink support AUXless ALPM.
  - (10b) Wait for AUX snoop transaction to transition back to D0, then wait for high-speed data input, and then wake up.
  - (11b) Wait for AUX snoop transaction to transition back to D0, or wait for high-speed data input, and then wake up.

7.7 USB-Type C DFP receptacle application (USB3 host, DisplayPort source)

Refer to Figure 9 for using PTN37011 in USB-Type C DFP receptacle application. In this configuration, upstream (left) side of PTN37011 is connected to host processor and downstream (right) side is connected to Type-C receptacle.

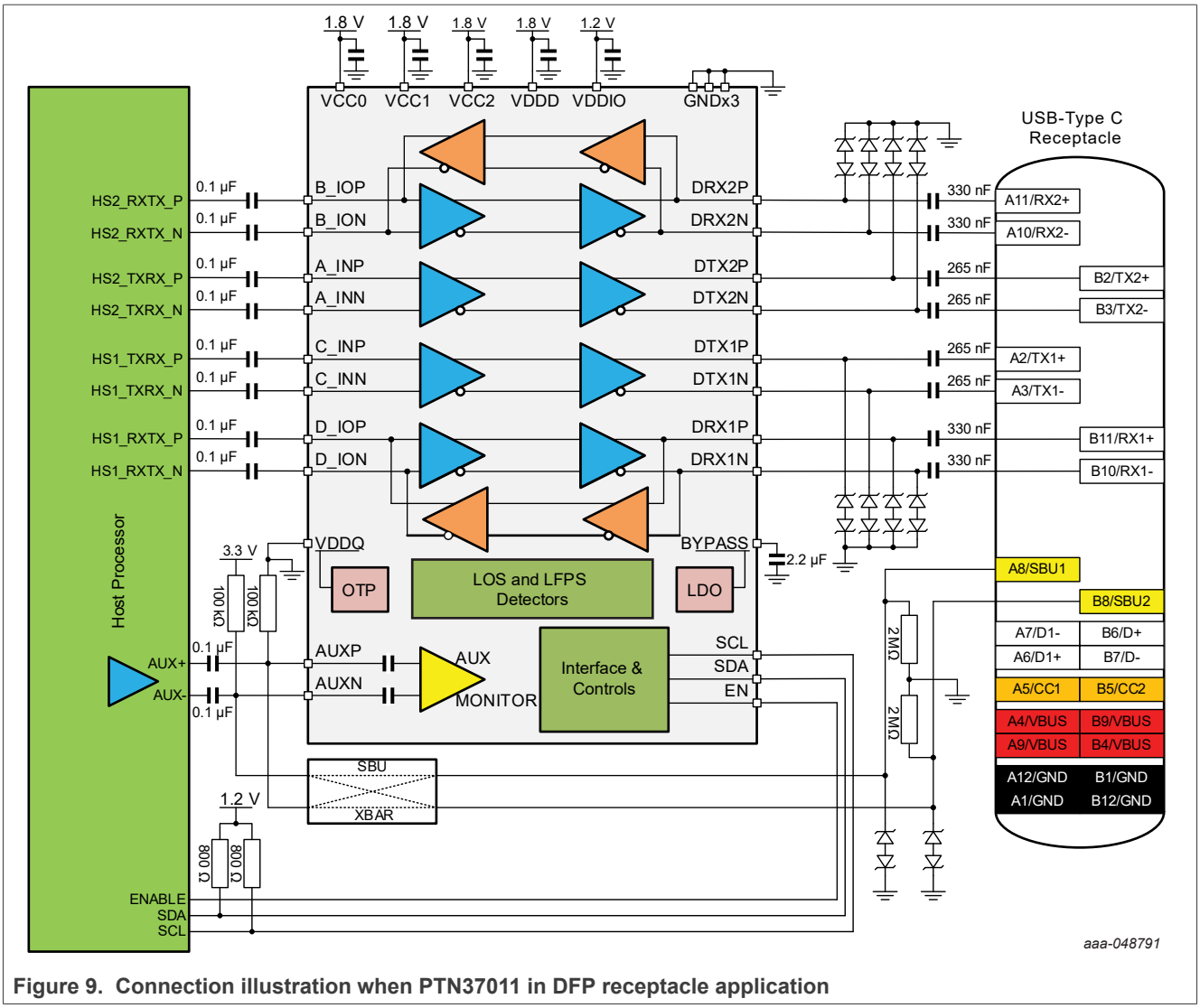


Figure 9. Connection illustration when PTN37011 in DFP receptacle application

Each pin on the downstream (right) side of PTN37011 connecting to the Type-C connector has a specific input/output configuration, and must match the signal assignments on the upstream (left) side accordingly. Table 4 shows the downstream (right) side pin connection facing the Type-C receptacle.

Table 4. Downstream (right) side pin connection to Type-C receptacle in DFP application

PTN37011 pins		USB-Type C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
A4	DRX2P	A11	RX2+
B4	DRX2N	A10	RX2-
C4	DTX2P	B2	TX2+
D4	DTX2N	B3	TX2-
E4	DTX1N	A3	TX1-
F4	DTX1P	A2	TX1+
G4	DRX1N	B10	RX1-

Table 4. Downstream (right) side pin connection to Type-C receptacle in DFP application*...continued*

PTN37011 pins		USB-Type C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
H4	DRX1P	B11	RX1+
H3	AUXP		Input or output of SBU XBAR
H2	AUXN		Input or output of SBU XBAR

The upstream (left) side pins of PTN37011 are connected to the host processor, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN37011 controls which transmitters or receivers to turn on or turn off, and operating in USB3.2 or DisplayPort mode according to the mode setting.

Table 5. Upstream (left) side pin connection to host processor in DFP receptacle application

PTN37011 pins		Host processor signal names					
Symbol	**Pin name**	**USB3.2 Gen1/2 x 1**		**USB3 + 2-Lane DP**		**4-Lane DP**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
A1	B_IOP		SSRX+	ML0+	SSRX+	ML0+	ML3+
B1	B_ION		SSRX-	ML0-	SSRX-	ML0-	ML3-
C1	A_INP		SSTX+	ML1+	SSTX+	ML1+	ML2+
D1	A_INN		SSTX-	ML1-	SSTX-	ML1-	ML2-
E1	C_INN	SSTX-		SSTX-	ML1-	ML2-	ML1-
F1	C_INP	SSTX+		SSTX+	ML1+	ML2+	ML1+
G1	D_ION	SSRX-		SSRX-	ML0-	ML3-	ML0-
H1	D_IOP	SSRX+		SSRX+	ML0+	ML3+	ML0+

The "DFP" and "UFP" use cases in Section 7.7 and Section 7.8 refer primarily to the DisplayPort source and sink locations. This fact is because PTN37011's channel A and channel C only operate in unidirectional mode. PTN37011's left side channels must connect to the DisplayPort source, and right side channels must connect to the DisplayPort sink. In a system that the Type-C port operates in DRP mode, the port can be configured as a USB3.2 host or a device role depending on the PD power contract or data role negotiation. The physical connection (SSTX and SSRX definitions in Table 5 and Table 7) from chipset and to Type-C remain the same within the system, but the corresponding port on the chipset defines the logical role (host or device). The transceivers of PTN37011 are agnostic to the logical role of USB3.2, and register settings only refer to the physical connections within the system.

Data role swap for DisplayPort within a defined system (that is, DFP or UFP as mentioned above) is not possible and not supported.

7.8 USB-Type C UFP receptacle application (USB3 device, DisplayPort sink)

Refer to Figure 10 for using PTN37011 in USB-Type C UFP receptacle application. In this configuration, downstream (right) side of PTN37011 is connected to device processor while the upstream (left) side is connected to Type-C receptacle.

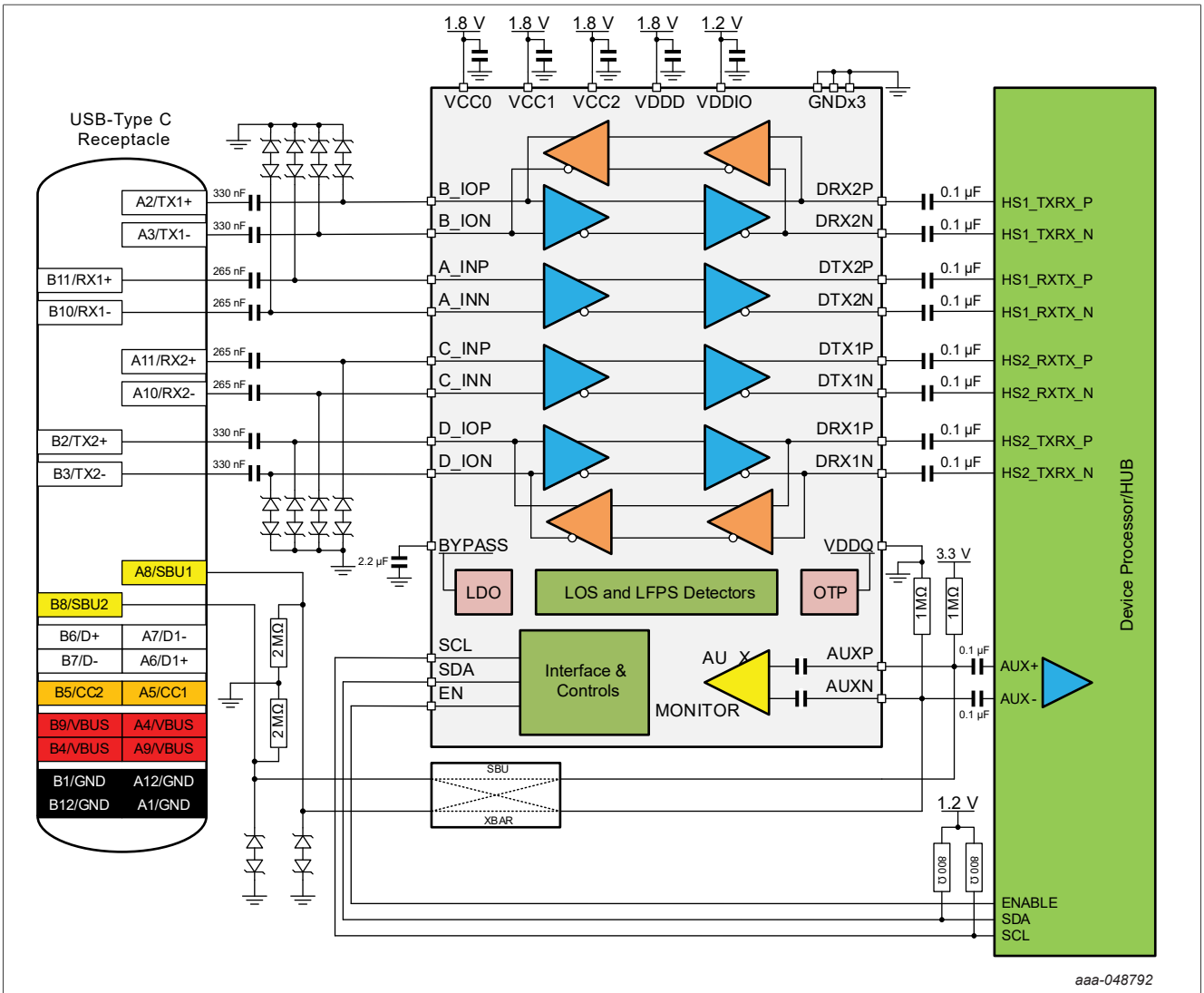


Figure 10. Connection illustration when in UFP receptacle application

Each pin on the upstream (left) side of PTN37011 connecting to the Type-C connector has specific input/output configuration, and must match the signal assignments on the downstream (right) side accordingly. Table 6 shows the upstream (left) side pin connection facing the Type-C receptacle.

Table 6. Upstream (left) side pin connection to Type-C receptacle in UFP application

PTN37011 pins		USB-Type C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
A1	B_IOP	A2	TX1+
B1	B_ION	A3	TX1-
C1	A_INP	B11	RX1+
D1	A_INN	B10	RX1-
E1	C_INN	A10	RX2-
F1	C_INP	A11	RX2+

Table 6. Upstream (left) side pin connection to Type-C receptacle in UFP application*...continued*

PTN37011 pins		USB-Type C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
G1	D_ION	B3	TX2-
H1	D_IOP	B2	TX2+
H3	AUXP		Input or output of SBU XBAR
H2	AUXN		Input or output of SBU XBAR

The downstream (right) side pins of PTN37011 are connected to the device processor, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN37011 controls which transmitters/receivers to turn on/off, and operate in USB3.2 or DisplayPort mode, according to the mode setting.

Table 7. Downstream (right) side pin connection to device processor in UFP receptacle application

PTN37011 pins		Device processor signal names					
Symbol	**Pin name**	**USB3.2 Gen1/2 x1**		**USB3 + 2-Lane DP**		**4-Lane DP**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
A4	DRX2P	SSTX+		SSTX+	ML0+	ML3+	ML0+
B4	DRX2N	SSTX-		SSTX-	ML0-	ML3-	ML0-
C4	DTX2P	SSRX+		SSRX+	ML1+	ML2+	ML1+
D4	DTX2N	SSRX-		SSRX-	ML1-	ML2-	ML1-
E4	DTX1N		SSRX-	ML1-	SSRX-	ML1-	ML2-
F4	DTX1P		SSRX+	ML1+	SSRX+	ML1+	ML2+
G4	DRX1N		SSTX-	ML0-	SSTX-	ML0-	ML3-
H4	DRX1P		SSTX+	ML0+	SSTX+	ML0+	ML3+

7.9 Control and programmability

7.9.1 Linear redriver controls

PTN37011 allows for programming of linear redriver functions (flat gain, equalizer, and output swing linearity) on a per channel basis. The USB3.2 and DP1.4 input channels support different data rates and the corresponding input equalization on those paths must be tuned accordingly.

Each linear redriver channel path has individual control of:

- Flat gain that can be controlled via I2C register for all the high-speed data paths
- Peaking gain referenced to the maximum data rate (or Nyquist channel) in that channel
- Output swing linear that is set up based on selected input source signal amplitude, preemphasis, and considering channel attenuation

7.9.2 Channel settings for USB3.2 and DisplayPort modes

During power-on reset, I2C register values are reset to default power-on reset values, and the default values of channel setting registers are loaded from OTP. The user can change channel condition register values through I2C interfaces while PTN37011 is in deep power-saving state.

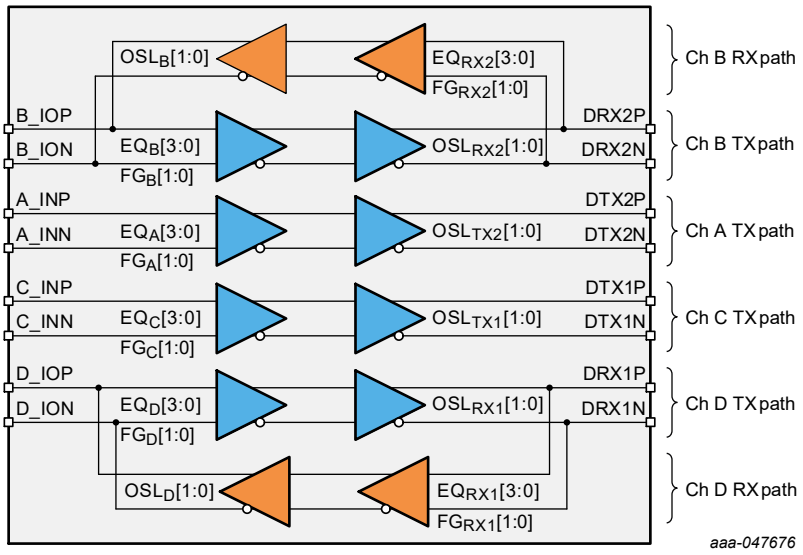


Figure 11. Equalizer, flat gain, and output swing linearity of corresponding transceiver path

Figure 11 illustrates six different transceiver paths in PTN37011, and each path has its own flat gain, equalizer gain, and output swing linearity settings. These settings are accessible through I2C registers.

In PTN37011, there are three flat gain settings that can be configured on each channel path, and they are listed in Table 8. Flat gain settings are mapped to I2C registers [0x02] and [0x03] as illustrated in Table 9.

Table 8. Flat gain control

I2C register value [1:0]	Flat gain control
b'00	+1 dB
b'01	0 dB
b'10	-1 dB
b'11	Reserved

Table 9. Flat gain register mapping

Transceiver path	Corresponding I2C register
Ch B RX	Reg[0x02][3:2] – FG_{RX2}
Ch B TX	Reg[0x03][7:6] – FG_B
Ch A TX	Reg[0x03][5:4] – FG_A
Ch C TX	Reg[0x03][3:2] – FG_C
Ch D TX	Reg[0x03][1:0] – FG_D
Ch D RX	Reg[0x02][1:0] – FG_{RX1}

Table 10 through Table 15 record the measurement results of the peaking gains from three nominal parts under typical PVT condition. Unidirectional channel results are the average of these three parts' AIN and CIN channels. The bidirectional channels results are the average of these three parts' BIO/DIO/DRX2/DRX1 channels.

Table 10, Table 11, and Table 12 are expanded to cover peaking gain values for the bidirectional channels (BIO, DIO, DRX1, DRX2) at different link rates of USB3 and DisplayPort protocols at flat gain of +1 dB, 0 dB, and -1 dB.

Table 10. Bidirectional channel equalizer peaking gain configurations when flat gain = +1 dB

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0000	dB	1.1	-0.1	-0.3	-0.6	-0.7	-0.9	-2.0
b'0001	dB	1.1	0.4	0.3	0.2	0.2	0.1	-1.0
b'0010	dB	1.1	0.8	0.9	1.0	1.0	1.1	0.0
b'0011	dB	1.1	1.1	1.5	1.8	1.8	1.9	0.9
b'0100	dB	1.1	1.5	1.9	2.4	2.5	2.7	1.8
b'0101	dB	1.1	1.8	2.5	3.2	3.3	3.6	2.7
b'0110	dB	1.1	2.2	3.0	3.9	4.0	4.6	3.8
b'0111	dB	1.1	2.6	3.5	4.7	4.9	5.6	4.9
b'1000	dB	1.2	2.9	4.0	5.5	5.6	6.5	5.9
b'1001	dB	1.2	3.3	4.6	6.3	6.5	7.5	7.0
b'1010	dB	1.3	3.7	5.2	7.1	7.3	8.5	8.1
b'1011	dB	1.5	4.2	5.7	7.8	8.0	9.3	8.9
b'1100	dB	Reserved						
b'1101	dB	Reserved						
b'1110	dB	Reserved						
b'1111	dB	Reserved						

Table 11. Bidirectional channel equalizer peaking gain configurations when flat gain = 0 dB

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0000	dB	0.2	0.1	0.1	0.1	0.1	0.3	-0.6
b'0001	dB	0.2	0.5	0.7	0.8	0.9	1.2	0.4
b'0010	dB	0.2	0.9	1.2	1.6	1.7	2.1	1.3
b'0011	dB	0.2	1.3	1.7	2.3	2.4	2.9	2.2
b'0100	dB	0.3	1.6	2.2	2.9	3.0	3.7	3.0
b'0101	dB	0.3	1.9	2.7	3.6	3.8	4.5	3.9
b'0110	dB	0.3	2.3	3.2	4.3	4.5	5.4	4.9
b'0111	dB	0.3	2.6	3.7	5.1	5.3	6.4	6.0
b'1000	dB	0.4	3.0	4.2	5.8	6.0	7.3	7.1
b'1001	dB	0.4	3.3	4.7	6.6	6.8	8.3	8.2
b'1010	dB	0.5	3.8	5.3	7.4	7.7	9.4	9.4

Table 11. Bidirectional channel equalizer peaking gain configurations when flat gain = 0 dB*...continued*

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'1011	dB	0.6	4.2	5.8	8.1	8.4	10.2	10.3
b'1100	dB	Reserved						
b'1101	dB	Reserved						
b'1110	dB	Reserved						
b'1111	dB	Reserved						

Table 12. Bidirectional channel equalizer peaking gain configurations when flat gain = -1 dB

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0000	dB	-0.8	0.3	0.4	0.7	0.8	1.4	0.8
b'0001	dB	-0.7	0.7	0.9	1.4	1.5	2.2	1.7
b'0010	dB	-0.7	1.0	1.5	2.1	2.2	3.1	2.6
b'0011	dB	-0.6	1.4	1.9	2.8	2.9	3.9	3.5
b'0100	dB	-0.6	1.7	2.4	3.4	3.5	4.6	4.2
b'0101	dB	-0.6	2.0	2.9	4.0	4.2	5.4	5.1
b'0110	dB	-0.5	2.3	3.3	4.7	4.9	6.2	6.0
b'0111	dB	-0.5	2.7	3.8	5.4	5.7	7.2	7.1
b'1000	dB	-0.5	3.0	4.3	6.1	6.4	8.1	8.2
b'1001	dB	-0.5	3.4	4.8	6.9	7.2	9.1	9.4
b'1010	dB	-0.4	3.8	5.4	7.7	8.0	10.2	10.6
b'1011	dB	-0.4	4.2	5.9	8.4	8.8	11.1	11.7
b'1100	dB	Reserved						
b'1101	dB	Reserved						
b'1110	dB	Reserved						
b'1111	dB	Reserved						

Table 13, Table 14, and Table 15 are expanded to cover peaking gain values for the unidirectional channels (AIN and CIN) at different link rates of USB3 and DisplayPort protocols at flat gain of +1 dB, 0 dB, and -1 dB.

Table 13. Unidirectional channel equalizer peaking gain configurations when flat gain = +1 dB

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0000	dB	1.1	-0.5	-0.9	-0.9	-0.9	-0.1	0.0
b'0001	dB	1.1	0.0	-0.2	0.0	0.0	1.0	1.1
b'0010	dB	1.0	0.4	0.5	0.9	1.0	2.0	2.2

Table 13. Unidirectional channel equalizer peaking gain configurations when flat gain = +1 dB*...continued*

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0011	dB	1.0	0.9	1.1	1.7	1.9	3.0	3.3
b'0100	dB	1.0	1.3	1.7	2.5	2.7	3.9	4.2
b'0101	dB	1.0	1.7	2.3	3.3	3.5	4.9	5.3
b'0110	dB	1.1	2.1	2.9	4.2	4.4	6.0	6.4
b'0111	dB	1.1	2.5	3.5	5.1	5.3	7.0	7.5
b'1000	dB	1.1	2.9	4.1	5.9	6.2	8.1	8.7
b'1001	dB	1.2	3.3	4.7	6.8	7.1	9.1	9.8
b'1010	dB	1.3	3.8	5.4	7.7	8.0	10.2	10.9
b'1011	dB	1.4	4.3	6.0	8.5	8.8	11.1	11.7
b'1100	dB	Reserved						
b'1101	dB	Reserved						
b'1110	dB	Reserved						
b'1111	dB	Reserved						

Table 14. Unidirectional channel equalizer peaking gain configurations when flat gain = 0 dB

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0000	dB	0.2	-0.2	-0.4	-0.2	0.0	1.2	1.6
b'0001	dB	0.2	0.2	0.2	0.7	0.8	2.2	2.6
b'0010	dB	0.2	0.6	0.8	1.5	1.7	3.2	3.7
b'0011	dB	0.2	1.0	1.4	2.3	2.5	4.1	4.6
b'0100	dB	0.2	1.4	2.0	3.0	3.3	4.9	5.5
b'0101	dB	0.2	1.8	2.5	3.8	4.1	5.8	6.5
b'0110	dB	0.3	2.2	3.1	4.7	4.9	6.8	7.6
b'0111	dB	0.3	2.6	3.7	5.5	5.8	7.9	8.7
b'1000	dB	0.3	3.0	4.3	6.3	6.6	8.9	9.9
b'1001	dB	0.4	3.4	4.9	7.2	7.5	10.0	11.1
b'1010	dB	0.4	3.9	5.5	8.0	8.4	11.1	12.2
b'1011	dB	0.5	4.3	6.1	8.8	9.2	12.0	13.2
b'1100	dB	Reserved						
b'1101	dB	Reserved						
b'1110	dB	Reserved						
b'1111	dB	Reserved						

Table 15. Unidirectional channel equalizer peaking gain configurations when flat gain = -1 dB

I2C register value [3:0]	Unit	100 MHz (reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5 GHz
b'0000	dB	-0.8	0.0	0.0	0.5	0.7	2.4	3.1
b'0001	dB	-0.7	0.4	0.6	1.3	1.5	3.3	4.1
b'0010	dB	-0.7	0.8	1.2	2.1	2.4	4.2	5.1
b'0011	dB	-0.7	1.2	1.7	2.9	3.1	5.1	5.9
b'0100	dB	-0.6	1.5	2.2	3.5	3.8	5.9	6.8
b'0101	dB	-0.6	1.9	2.7	4.3	4.6	6.7	7.7
b'0110	dB	-0.6	2.3	3.3	5.1	5.4	7.7	8.8
b'0111	dB	-0.6	2.7	3.9	5.9	6.2	8.7	9.9
b'1000	dB	-0.5	3.1	4.4	6.7	7.0	9.8	11.1
b'1001	dB	-0.5	3.5	5.0	7.5	7.9	10.8	12.3
b'1010	dB	-0.4	3.9	5.6	8.3	8.8	11.9	13.5
b'1011	dB	-0.4	4.3	6.2	9.1	9.6	12.9	14.6
b'1100	dB	Reserved						
b'1101	dB	Reserved						
b'1110	dB	Reserved						
b'1111	dB	Reserved						

Peaking gain is defined as the AC gain with respect to the flat gain values. For the same boost code (BST) across different flat gain settings, design keeps the same AC gain at 5 GHz and only varies the flat gain (FG) values. Therefore, lower flat gain settings result in a higher peaking gain.

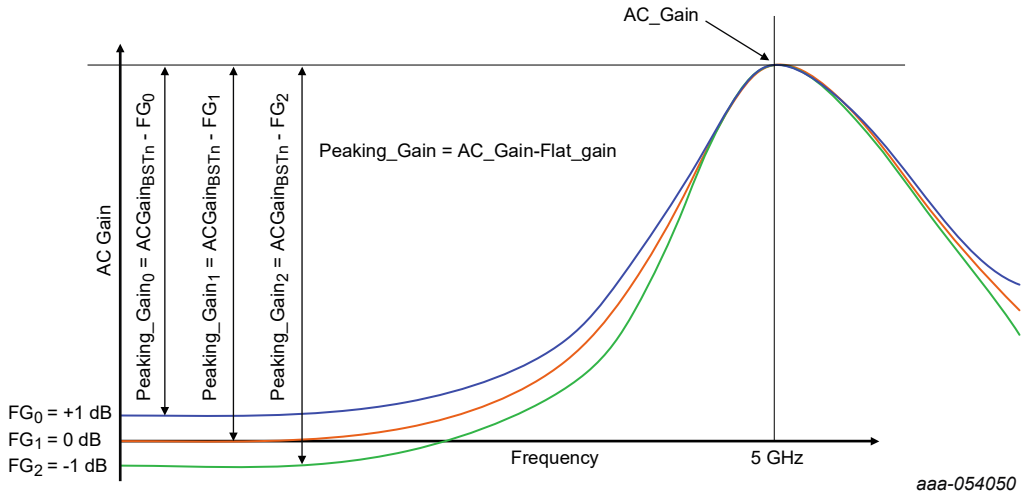


Figure 12. AC gain, peaking gain, and flat gain illustration

Table 16. Output swing linearity

I2C register value [1:0]	Output swing linearity
b'00	600 mVppd

Table 16. Output swing linearity*...continued*

I2C register value [1:0]	Output swing linearity
b'01	700 mVppd
b'10	800 mVppd
b'11	Reserved

Equalizer gain and output swing linearity settings are mapped to I2C registers based on various functions in the mode control register. Table 17 summarizes equalizer gain and output swing linearity register mappings in USB3 and DisplayPort modes.

Table 17. Equalizer gain and output swing linearity register mapping according to a different function

	USB3.2 Gen1/2 x1 (Mode = 1, 2)		2/4-Lane DP (Mode = 2, 3)	
Transceiver path	**DFP/Normal or UFP/Reversed**	**DFP/Reversed or UFP/Normal**	**DFP/Normal or UFP/Reversed**	**DFP/Reversed or UFP/Normal**
Ch B RX		SSRX (Reg[0x10][3:0] – EQ_{RX2}) (Reg[0x11][1:0] – OSL_B)		
Ch B TX			ML0 (Reg[0x07][3:0] – EQ_B) (Reg[0x08][1:0] – OSL_{RX2})	ML3 (Reg[0x0d][3:0] – EQ_B) (Reg[0x0e][1:0] – OSL_{RX2})
Ch A TX		SSTX (Reg[0x12][3:0] – EQ_A) (Reg[0x13][1:0] – OSL_{Tx2})	ML1 (Reg[0x09][3:0] – EQ_A) (Reg[0x0a][1:0] – OSL_{TX2})	ML2 (Reg[0x0b][3:0] – EQ_A) (Reg[0x0c][1:0] – OSL_{TX2})
Ch C TX	SSTX (Reg[0x12][3:0] – EQ_C) (Reg[0x13][1:0] – OSL_{TX1})		ML2 (Reg[0x0b][3:0] – EQ_C) (Reg[0x0c][1:0] – OSL_{TX1})	ML1 (Reg[0x09][3:0] – EQ_C) (Reg[0x0a][1:0] – OSL_{TX1})
Ch D TX			ML3 (Reg[0x0d][3:0] – EQ_D) (Reg[0x0e][1:0] – OSL_{RX1})	ML0 (Reg[0x07][3:0] – EQ_D) (Reg[0x08][1:0] – OSL_{RX1})
Ch D RX	SSRX (Reg[0x10][3:0] – EQ_{RX1}) (Reg[0x11][1:0] – OSL_D)			

7.10 System interface

Figure 9 and Figure 10 illustrate possible PTN37011 connections in a USB-Type C subsystem.

One side of PTN37011's high speed pins are connected to a chipset or a hub, through 100 nF AC-coupling capacitors on BIO/AIN/CIN/DIO pins. The other side of PTN37011's high speed pins are connected to USB-Type C connectors, with 330 nF AC-coupling capacitors on the RX pins and 220 nF AC-coupling capacitors on the TX pins. TVS diodes (NXP recommends using PESD2V5Y1BSF) must be placed between these TX and RX AC-coupling capacitors and PTN37011s high-speed pins to protect PTN37011 from VBus short fault events (up to 15 V @ 3 A) on the Type-C connector.

It is necessary to have 1.5 Ω trace resistance between PTN37011's high-speed pins and TVS diodes to achieve the IEC61000-4-2 ±8 kV contact discharge performance. Without 1.5 Ω trace resistance and ESDL1531 TVS diode, IEC performance remains lower to ~2 kV to 3 kV for the negative stress, and ~5 kV for the positive stress.

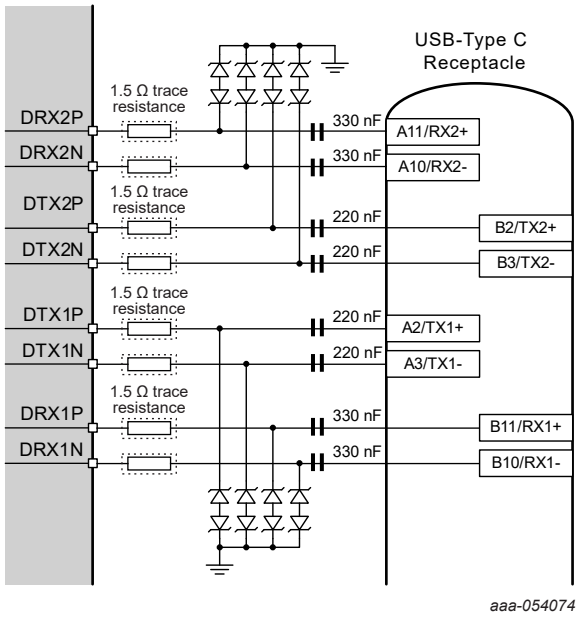


Figure 13. PTN37011 connector facing side connections in a system

PTN37011's AUXP and AUXN snooping pins are typically connected between SBU crossbar switch and the chipset or the hub, before or after the AC-coupling capacitors on a USB-Type C application (Figure 14).

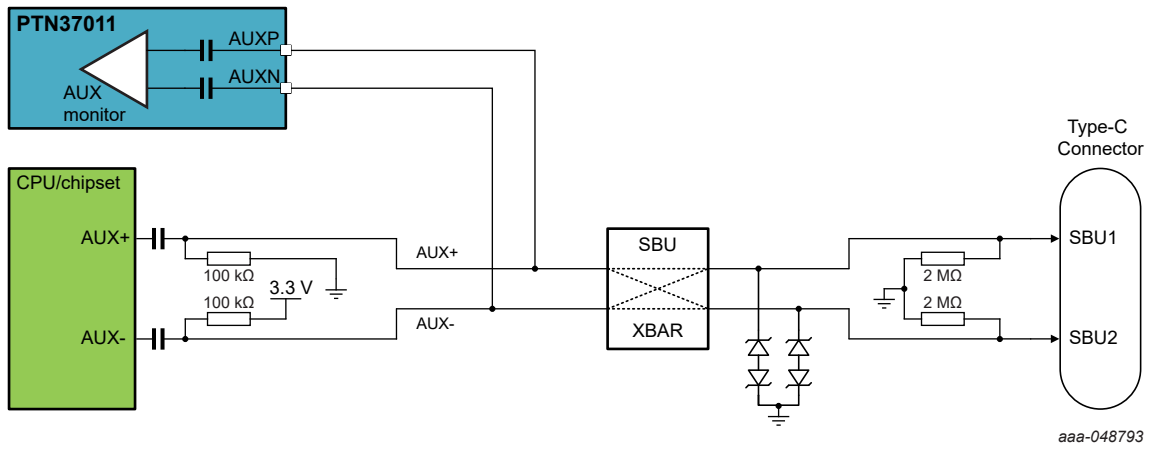


Figure 14. AUX snooping pins connection in a USB-Type C connector application

When PTN37011 is used in a DisplayPort or other connector application, where there is no SBU crossbar switch to isolate PTN37011 from ESD events, PTN37011's AUXP and AUXN snooping pins must be connected between AC-coupling capacitors and the chipset, with TVS diodes (NXP recommends using PESD2V5Y1BSF) and 2 Ω series resistors (Figure 15) to protect PTN37011 from ESD and power short fault events (up to 15 V @ 3 A) on the connector side.

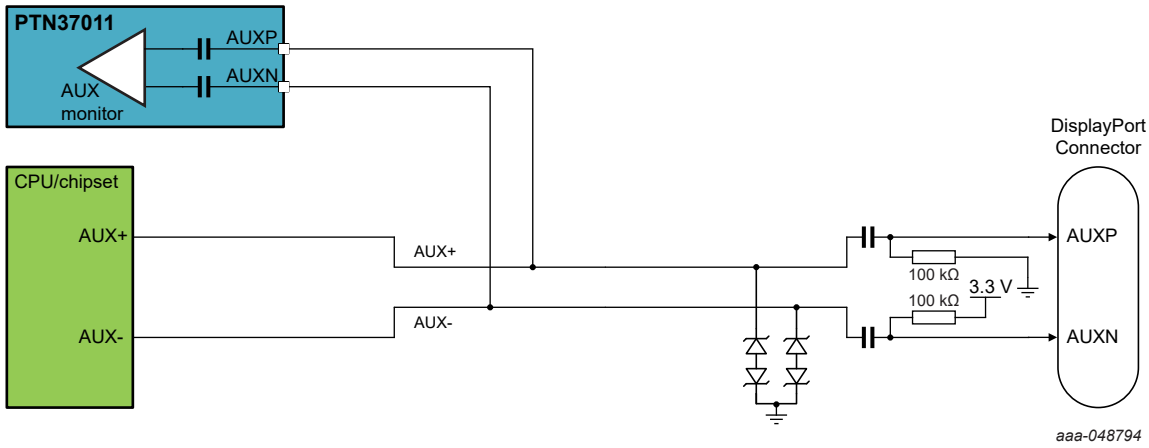


Figure 15. AUX snooping pins connection in a DisplayPort connector application

PTN37011 has two power rails, where 1.8 V must be connected on VDD_D and $VCC_{0/1/2}$ pins together on the PCB, and 1.2 V must be connected on VDD_{IO} pin. Each power pin must have its own 100 nF decoupling capacitor placed close to the pin. During normal operation, the VDDQ pin must tie to the ground directly.

BYPASS pin must have a 2.2 µF decoupling capacitor (0201 size, for example, https://www.digikey.com) placed close to the pin, such that the PCB trace resistance and capacitor ESR values total is less than 1 Ω. BYPASS pin capacitor must be below characteristics:

- Capacitance range: 0.9 µF minimum to 2.64 µF maximum, overtemperature, voltage, and aging derations range
- ESR value between 50 mΩ to 1 Ω maximum

7.11 I2C configurability

PTN37011 is an I2C peripheral-only device. It responds to I2C protocols up to 1 Mbit/s (Fm+) when all power rails are supplied with a valid voltage level. The I2C interface operates at VDD_{IO} level. When $VCC_{0/1/2}$, VDD_D, or VDD_{IO} power supplies are absent or when EN input pin is LOW, SCL and SDA pins are placed in high-impedance state, and must not affect any existing I2C transaction between I2C controller and other I2C peripheral devices on the bus.

The I2C interface of PTN37011 does not support general call addressing. It does not perform clock stretching during operation. But, it tolerates other peripheral devices performing clock stretching under the legal conditions defined in *I2C - bus specification and user manual* (document UM10204).

The controller uses the I2C bus to write to and read from registers using the register access protocol specified in the following sections. Each operation of writing to or reading from one or more consecutive registers is referred to as a transaction. Consecutive registers are defined as a series of incrementing register addresses, regardless of whether the given address has a definition in the register map of peripherals.

A transaction can be a part of a series of transactions addressed to multiple different peripherals or to the same peripheral repeatedly with different register address offsets, with each transaction separated by repeated-START conditions.

There is no register address aliasing in PTN37011. During read or write transactions with multiple consecutive registers, the register address rolls back to [0x00] when max register address (0xFF) is reached. When an undefined or invalid register address is addressed for read or write operation, PTN37011 acknowledges the I2C transaction, but returns 0x00 for a read operation or takes no action for a write operation.

7.11.1 I2C peripheral addresses

PTN37011 has an I2C register interface that enables the system integrator to program register settings suitable as per the application requirement. The I2C peripheral addresses are shown in Table 18. By default, only the peripheral address of 0x30 is assigned to PTN37011. Changing the peripheral address to one other value can only be done through OTP programming in the factory.

Table 18. I2C peripheral address options

7-bit I2C peripheral address	8-bit I2C address							
011-0000 (0x30) (default)	0	1	1	0	0	0	0	R/W
011-0001 (0x31) (OTP option)	0	1	1	0	0	0	1	R/W
011-0010 (0x32) (OTP option)	0	1	1	0	0	1	0	R/W
011-0011 (0x33) (OTP option)	0	1	1	0	0	1	1	R/W
011-0000 (0x34) (OTP option)	0	1	1	0	1	0	0	R/W
011-0001 (0x35) (OTP option)	0	1	1	0	1	0	1	R/W
011-0010 (0x36) (OTP option)	0	1	1	0	1	1	0	R/W
011-0011 (0x37) (OTP option)	0	1	1	0	1	1	1	R/W

7.11.2 I2C read/write operations

Reading/writing the registers must be done according to protocols defined in UM10204, following the sequences shown below.

7.11.2.1 Register reads

The read sequence contains two phases: command phase and data phase. The command phase is an I2C write to PTN37011 containing a single data byte. The LS bit indicates if the command that is being executed reads or writes data from/to the device. The other seven bits are the device peripheral address. The single data byte that follows is the register offset used to indicate which register address is being accessed (read or written). The data phase is a second I2C transaction that starts with a 7-bit peripheral address, with the LS bit set to 1 indicating a read operation, followed by an 8-bit data read back from the device register address.

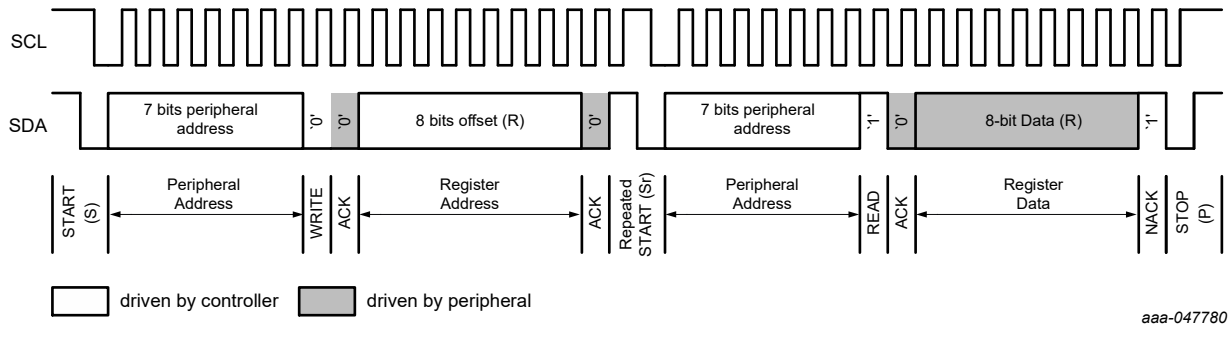


Figure 16. Single byte I2C read sequence

To read multiple bytes, follow the similar command phase and data phase sequence above. In the data phase, after PTN37011 clocks out the first byte of data, if controller wishes to read the next consecutive register, it issues an ACK and then provides another set of clock pulses, whereby PTN37011 supplies the value of the next register. As long as the controller continues to issue an ACK and supplies additional clock pulses, PTN37011 continues to supply the value of consecutive registers.

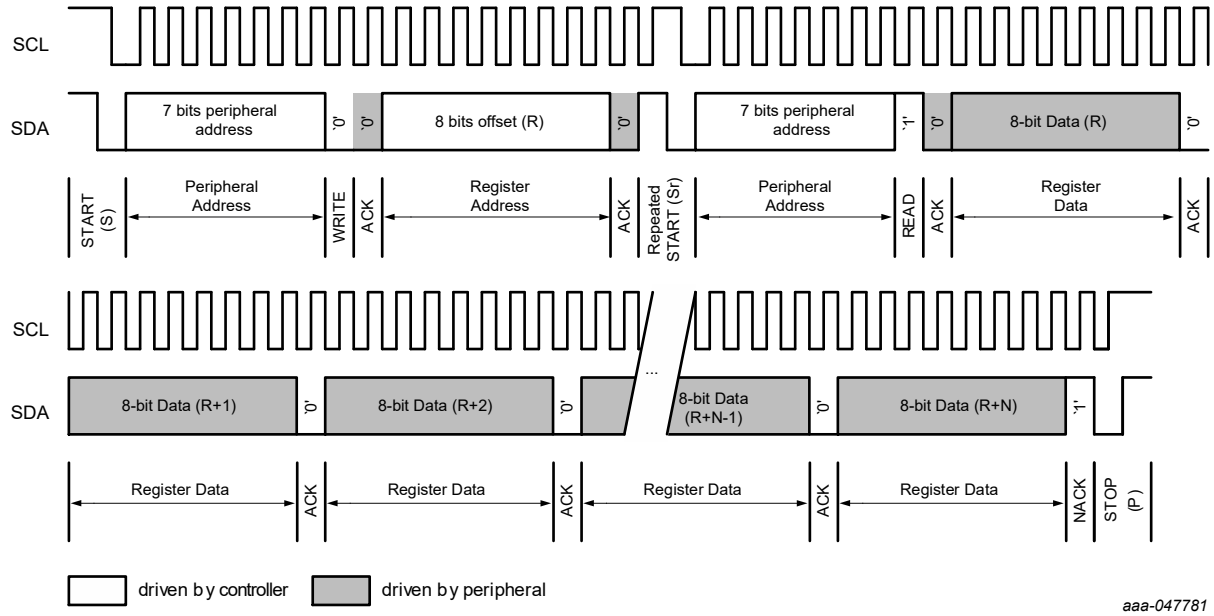


Figure 17. Multiple byte I2C read sequence

7.11.2.2 Register writes

The write sequence starts with a 7-bit peripheral address, with the LS bit set to 0 indicating a write access. The next byte is the register offset that is used to indicate which device register address is being written to. The last byte is the 8-bit register data that writes to the device register address.

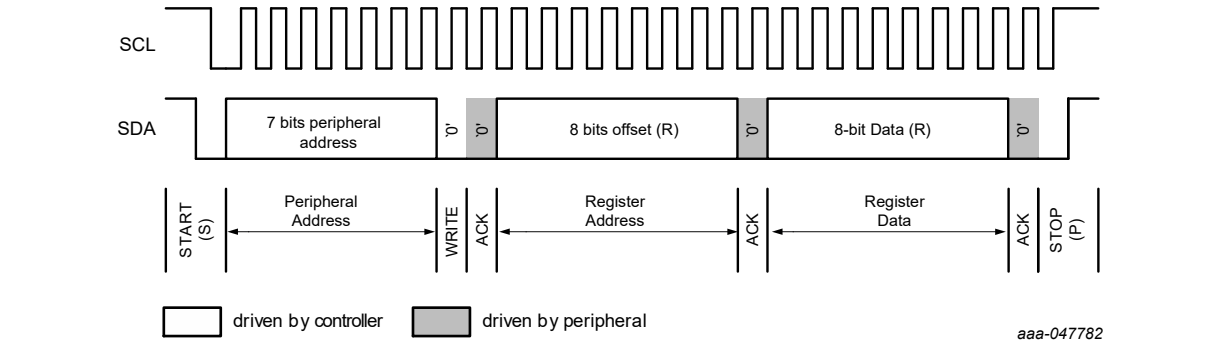


Figure 18. Single byte I2C write sequence

To write multiple bytes, follow a similar sequence shown in Figure 18. After I2C controller writes the first data byte, PTN37011 acknowledges the data with an ACK. If the controller wishes to write to the next consecutive register address, it supplies another data byte, which PTN37011 ACKs. The controller continues writing data bytes for consecutive registers. When the controller finishes writing one or more desired registers, it issues either a STOP condition or a repeated-START condition.

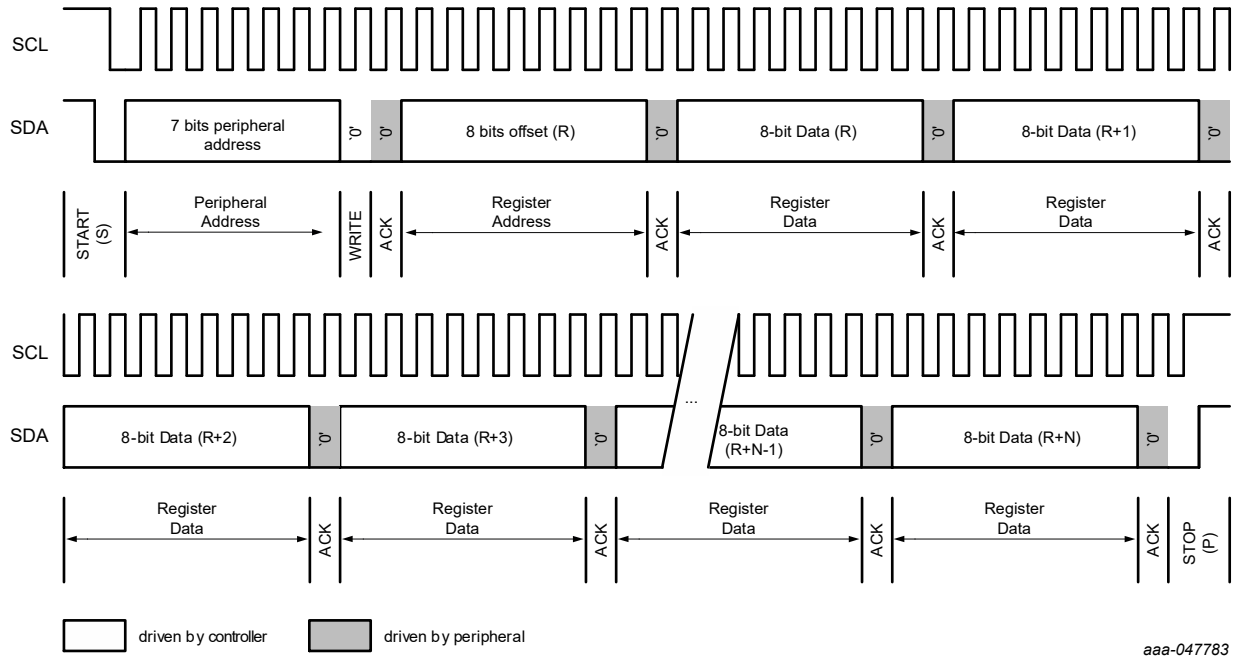


Figure 19. Multiple byte I2C write sequence

7.11.3 I2C registers

The system integrator must program the registers of the device for proper operation. Further, it is expected that the system integrator performs I2C configuration after power up and before data transport is initiated over the link.

Table 19. I2C registers and description

Register offset	Register name	Bits	POR default value	Description
0x00 Read only	Chip ID	7:4	b'0111	Chip ID Number
		3:0	b'0001	Part type. The field tracks sets of default values, and I2C peripheral addresses to be programmed in the factory. This field must be a non-zero value.
0x01 Read only	Chip Revision	7:4	b'1010	Chip base layer version
		3:0	b'0001	Chip metal layer version
0x02 Read/write	Flat gain control 1	7:4	b'0000	Reserved
		3:2	b'01	FG_{RX2} Channel B RX path (Figure 11) flat gain control • 00: Flat gain of +1 dB • 01: Flat gain of 0 dB • 10: Flat gain of -1 dB • 11: Reserved
		1:0	b'01	FG_{RX1} Channel D RX path (Figure 11) flat gain control • 00: Flat gain of +1 dB • 01: Flat gain of 0 dB • 10: Flat gain of -1 dB • 11: Reserved
0x03 Read/write	Flat gain control 2	7:6	b'01	FG_B Channel B TX path (Figure 11) flat gain control • 00: Flat gain of +1 dB • 01: Flat gain of 0 dB

Table 19. I2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
				• 10: Flat gain of -1 dB • 11: Reserved
		5:4	b'01	FG_A Channel A TX path (Figure 11) flat gain control • 00: Flat gain of +1 dB • 01: Flat gain of 0 dB • 10: Flat gain of -1 dB • 11: Reserved
		3:2	b'01	FG_C Channel C TX path (Figure 11) flat gain control • 00: Flat gain of +1 dB • 01: Flat gain of 0 dB • 10: Flat gain of -1 dB • 11: Reserved
		1:0	b'01	FG_D Channel D TX path (Figure 11) flat gain control • 00: Flat gain of +1 dB • 01: Flat gain of 0 dB • 10: Flat gain of -1 dB • 11: Reserved
0x04 Read/write	Mode control	7:6	b'00	Reserved
		5	b'0	DFP or UFP configuration • 0: DFP configuration • 1: UFP configuration
		4	b'0	Plug orientation control. This orientation condition applies to high-speed TX/RX configuration. • 0: Normal plug orientation of Type-C connection • 1: Reverse plug orientation of Type-C connection
		3	b'0	AUX snooping polarity control bit • When 0, AUXP/AUXN signal polarities follow pin naming: – Pin H3: AUXP – Pin H2: AUXN • When 1, AUXP/AUXN signal polarities are reversed of the pin naming: – Pin H2: AUXP – Pin H3: AUXN
		2:0	b'000	Operational mode of the device. Refer to section 7.3 for mode transition requirement • 0: Deep power-saving state • 1: USB3.2 x1 • 2: USB3.2 + DP 2-Lane + AUX snooping • 3: DP 4-Lane + AUX snooping • 4-7: Reserved
0x05 Read/write	Device control	7:1	b'0000 000	Reserved
		0	b'0	Device reset bit. This bit is a self-clearing bit. Software reset is processed at the I2C STOP condition after writing an '1' to this field. After software reset is processed, this field self-clears to a '0'. Reading from this register field returns the last value written to it if the software reset is not yet processed, or returns '0' if the software reset is processed. • Writing a '1' to this register resets digital logic, including restoring I2C register contents to default values, and loading channel register values from OTP shadow registers (instead of reading from OTP directly). Analog circuitries (band gap, internal LDO, POR, power good, and

Table 19. I2C registers and description...*continued*

Register offset	Register name	Bits	POR default value	Description
				FRO clock) are not powered down, and high-speed analog transceivers are reinitialized to the same condition as in deep power-saving state. • Writing a '0' does not have any effect.
0x06 Read/write	DP link control and status	7:5	b'000	Reserved
		4	b'0	DisplayPort power-saving mode selection on all DP lanes. • 0: D0 normal/active mode • 1: D3 power-saving mode, all lanes are in low-power mode. This field can be modified through an I2C write or AUX monitor function. When corresponding DPCD register changes are detected via the AUX monitor, this field is updated.
		3:2	b'00	DisplayPort operating lane count • 0: 0 DP lane • 1: 1 DP lane • 2: 2 DP lanes • 3: 4 DP lanes This field can be modified through an I2C write or the AUX monitor function. When corresponding DPCD register changes are detected via the AUX monitor, this field is updated. Two consecutive read-outs with the same value confirm the DisplayPort operating lane count.
		1:0	b'00	Reserved
0x07 Read/write	DP Lane 0 Control_1	7:4	b'0000	Reserved
		3:0	b'1000	DP lane 0 link equalization gain. Refer to peaking gain tables (Table 10, Table 11, and Table 12) for more details.
0x08 Read/write	DP Lane 0 Control_2	7:2	b'0000 00	Reserved
		1:0	b'10	DP lane 0 output signal swing linearity • 0: 600 mVppd • 1: 700 mVppd • 2: 800 mVppd • 3: Reserved
0x09 Read/write	DP Lane 1 Control_1	7:4	b'0000	Reserved
		3:0	b'1000	DP lane 1 link equalization gain. Refer to peaking gain tables (Table 10, Table 11, and Table 12) for more details.
0x0A Read/write	DP Lane 1 Control_2	7:2	b'0000 00	Reserved
		1:0	b'10	DP lane 1 output signal swing linearity • 0: 600 mVppd • 1: 700 mVppd • 2: 800 mVppd • 3: Reserved
0x0B Read/write	DP Lane 2 Control_1	7:4	b'0000	Reserved
		3:0	b'1000	DP lane 2 link equalization gain. Refer to peaking gain tables (Table 10, Table 11, and Table 12) for more details.
0X0C Read/write	DP Lane 2 Control_2	7:2	b'0000 00	Reserved
		1:0	b'10	DP lane 2 output signal swing linearity • 0: 600 mVppd • 1: 700 mVppd

Table 19. I2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
				• 2: 800 mVppd • 3: Reserved
0x0D Read/write	DP Lane 3 Control_1	7:4	b'0000	Reserved
		3:0	b'1000	DP lane 3 link equalization gain. Refer to peaking gain tables (Table 10, Table 11, and Table 12) for more details.
0x0E Read/write	DP Lane 3 Control_2	7:2	b'0000 00	Reserved
		1:0	b'10	DP lane 3 output signal swing linearity • 0: 600 mVppd • 1: 700 mVppd • 2: 800 mVppd • 3: Reserved
0X0F Read/write	LoS detector threshold	7	0	LFPS detection is disabled in U2/U3 state in USB3 operation. This bit can be set/changed during any functional state. • 0: LFPS detector is used in U2/U3 state to transition back to U0 state. • 1: LFPS detector is not used to transition from U2/U3 state to U0 state.
		6	0	LoS detector disable in USB3 operation. This bit can be set/changed only during deep power-saving mode. • 0: LoS detector is enabled. • 1: LoS detector is disabled.
		5:4	b'10	Ports B_IO, A_IN, C_IN, and D_IO sides LoS detector threshold setting. • 0: unsquelched to squelched level @ 45 mV, squelched to unsquelched level @ 65 mV • 1: unsquelched to squelched level @ 60 mV, squelched to unsquelched level @ 80 mV • 2: unsquelched to squelched level @ 70 mV, squelched to unsquelched level @ 90 mV • 3: unsquelched to squelched level @ 80 mV, squelched to unsquelched level @ 100 mV The setting is applicable to USB3.2 and DisplayPort operational modes. It is used as a signal threshold reference for low-power state management.
		3:2	b'00	USB3 active mode and power-saving mode (U2/U3) select. This function is only valid when bit [6] is set to 1. For details, see Section 7.4.1. Two consecutive read-outs with the same value confirms USB3 state transition. • 00: Active state (U0) • 01: Power-saving state (U2/U3) • 10: Reserved. It has the same function effect as setting 11. • 11: Transition from power-saving state (U2/U3) to active state (U0)
		1:0	b'10	Ports DRX2 and DRX1 sides LoS detector threshold setting. • 0: unsquelched to squelched level @ 45 mV, squelched to unsquelched level @ 65 mV • 1: unsquelched to squelched level @ 60 mV, squelched to unsquelched level @ 80 mV • 2: unsquelched to squelched level @ 70 mV, squelched to unsquelched level @ 90 mV • 3: unsquelched to squelched level @ 80 mV, squelched to unsquelched level @ 100 mV

Table 19. I2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
				The setting is applicable for USB3.2 operational mode. It is used as a signal threshold reference for low-power state management.
0x10 Read/write	USB_Right_Side_RX_ Control	7:4	b'0000	Reserved
		3:0	b'1000	USB3.2 Mode right side (DRX2 and DRX1) link equalization gain. Refer to peaking gain tables (Table 10, Table 11, and Table 12) for more details.
0x11 Read/write	USB_Left_Side_TX_ Control	7:2	b'0000 00	Reserved
		1:0	b'10	USB3.2 Mode left side (B_IO and D_IO) link output signal swing linearity • 0: 600 mVppd • 1: 700 mVppd • 2: 800 mVppd • 3: Reserved
0x12 Read/write	USB_Left_Side_RX_ Control	7:4	b'0000	Reserved
		3:0	b'1000	USB3.2 Mode left side (A_IN and C_IN) link equalization gain. Refer to peaking gain tables (Table 10, Table 11, and Table 12) for more details.
0x13 Read/write	USB_Right_Side_TX_ Control	7:2	b'0000 00	Reserved
		1:0	b'10	USB3.2 Mode right side (DTX2 and DTX1) link output signal swing linearity • 0: 600 mVppd • 1: 700 mVppd • 2: 800 mVppd • 3: Reserved
0x14 to 0xFF	Reserved			Reserved for NXP internal use only; do not write to these registers.

8 Limiting values

Table 20 describes the limiting values of PTN37011.

Table 20. Limiting values

Stresses beyond those listed under absolute maximum ratings can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique identifier
VDD_D	Digital supply voltage	VDD_D	-0.5		2.376	V	LTC-VOL-PRIO1-001
VCC_X	Supply voltage for high-speed lanes	VCC_0, VCC_1, VCC_2	-0.5		2.376	V	LTC-VOL-PRIO1-002
VDD_{IO}	Supply voltage for I2C interface	VDD_{IO}	-0.5		2.0	V	LTC-VOL-PRIO1-003
V_I	Input voltage	AUXP, AUXN	-0.5		3.6	V	LTC-VOL-PRIO1-004
		SCL, SDA	-0.5		2.0	V	LTC-VOL-PRIO1-005
		EN, DTB	-0.5		2.0	V	LTC-VOL-PRIO1-006
		High-speed pins	-0.5		VCC_x + 0.3	V	LTC-VOL-PRIO1-007
T_{stg}	Storage temperature		-65		150	°C	LTC-TMP-PRIO1-008
V_{esd}	Electrostatic discharge	HBM[1] for High-speed and AUX pins	1250			V	LTC-VOL-PRIO1-009
		HBM[1] for other control pins	1250			V	LTC-VOL-PRIO1-010
		CDM[2] for High-speed and AUX pins	500			V	LTC-VOL-PRIO1-011
		CDM[2] for other control pins	500			V	LTC-VOL-PRIO1-012
	IEC61000-4-2 contact discharge (TVS diode: PESD2V5Y1BSF)	ESD strike on the connector side, with 1.5 Ω trace resistance and TVS diodes between AC caps and high-speed pins	±8			kV	LTC-VOL-PRIO1-013
	IEC61000-4-2 air discharge (TVS diode: PESD2V5Y1 BSF)	ESD strike on the connector side, with TVS diodes between AC caps and high-speed pins	±15			kV	LTC-VOL-PRIO1-014
	VBus short fault tolerance (TVS diode: PESD2V5Y1 BSF)	On high-speed pins, across AC capacitors and TVS diodes, up to 1000 times.			15	V	LTC-VOL-PRIO1-015
		On AUXP/AUXN pins, across AC capacitors and TVS diodes, up to 1000 times.			15	V	LTC-VOL-PRIO1-016
$R_{th(j-a)}$	Thermal resistance from junction to ambient environment	JESD51-9, 2s2p		63.3		°C/W	LTC-RES-PRIO2-018
$R_{th(j-c)}$	Thermal resistance from junction to case	JESD51-9, 2s2p		3.3		°C/W	LTC-RES-PRIO2-019

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA

9 Recommended operating conditions

Table 21 describes the recommended operating conditions for PTN37011.

Table 21. Operating conditions

Over operating free-air temperature range (unless otherwise noted). Typical values are specified for VCC_X/VDD_D = 1.8 V, VDD_{IO} = 1.2 V and 25 °C operating temperature.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique identifier
VDD_D	Digital supply voltage	VDD_D	1.62	1.8	1.98	V	ROC-VOL-PRIO1-001
VCC_X	Supply voltage for high-speed lanes	VCC_0, VCC_1, VCC_2	1.62	1.8	1.98	V	ROC-VOL-PRIO1-002
VDD_{IO}	Supply voltage for I2C interface	VDD_{IO}	1.08	1.2	1.32	V	ROC-VOL-PRIO1-003
V_I	Input voltage	AUXP, AUXN	-0.3		3.6	V	ROC-VOL-PRIO1-004
		SCL, SDA	-0.3		1.32	V	ROC-VOL-PRIO1-005
		EN	-0.3		1.32	V	ROC-VOL-PRIO1-006
		High-speed pins	-0.3		VCC_x + 0.3	V	ROC-VOL-PRIO1-007
T_{amb}	Ambient temperature	Operating in free air	-20		85	°C	ROC-TMP-PRIO1-008

10 Characteristics

This section describes the device key characteristics including input, output, and I2C-specific characteristics.

10.1 Device characteristics

Table 22. Device characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
V_{GND_VCC} noise	Noise voltage from DUT (50 Hz to 1 MHz) GND noise/bounce with VCC as the reference point	DUT only and No bypass cap during testing	Bench		18		mVpp	DEV-VOL-PRIO2-001
DJ	Intrinsic jitter, an added jitter by linear redriver	Measurement setup according to USB3.2 LRD_CTS appendix B	Bench			4	ps	DEV-DB-PRIO2-002
CMRR	Common mode rejection ratio (diff_ gain /cm_gain)	10 MHz to 1 GHz	Bench		30		dB	DEV-DB-PRIO2-003
PSRR	Power supply rejection ratio Δ(VCC)/Δ(Vout_ diff)	10 MHz to 200 MHz	Bench		41		dB	DEV-DB-PRIO2-004
t_{Ready}	Startup time	Between EN goes HIGH to I2C ready for transaction	Bench			5	ms	DEV-TIM-PRIO1-005
t_{EN_RESET}	Device disable time to ensure that internal LDO is powered off and discharged	EN = 0, when all power rails (VDD_D, $VCC_{0/1/2}$, and VDD_{IO}) are supplied with valid supply voltages	ATE	500			µs	DEV-TIM-PRIO1-052
$t_{Startup\_USB}$	USB startup time	Time between configuration in USB operating mode until automatic receive detection is active	Bench			5	ms	DEV-TIM-PRIO1-006
t_{RX_DET}	RX.Detect repetition rate	Initial idle period	Bench			8	ms	DEV-TIM-PRIO1-007
		In U2/U3 states	Bench			8	ms	DEV-TIM-PRIO1-008
$t_{S(EN-DIS)}$	Device transition from functional mode (mode = 1/2/3) to DPSS state (mode = 0)	The device is supplied with a valid supply voltage, and EN = 1	ATE			1	ms	DEV-TIM-PRIO1-009
t_{mode_rcfg}	Mode control reconfiguration time	Mode control configuration change	ATE			0.5	ms	DEV-TIM-PRIO1-010
t_{PD}	Differential propagation delay	Differential propagation delay between 50 % level at input and output of Super-Speed pins	Bench			700	ps	DEV-TIM-PRIO1-011
t_{idle}	Idle time	Time to wait before getting into power saving U2/U3 state (in USB Mode), D3 state (in DP)	Bench		300	400	ms	DEV-TIM-PRIO1-012
$t_{power\_saving\_exit}$	Power saving exit time, time to exit from power saving U2/U3 state and get into U0 active state in USB3.2 mode, or D0 in DisplayPort mode	USB3.2 mode (LFPS polling disabled, usb_ sqd_poll_u2_u3 = '0'; usb_u2u3_lfps_poll_ tmr = 'xx')	ATE-Char			60	µs	DEV-TIM-PRIO1-013a
		USB3.2 mode (LFPS polling 77 % on, usb_ sqd_poll_u2_u3 = '1';	ATE-Char			75	µs	DEV-TIM-PRIO1-013b

Table 22. Device characteristics*...continued*

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
		usb_u2u3_lfps_poll_tmr = '00')						
		USB3.2 mode (LFPS polling 44 % on, usb_sqd_poll_u2_u3 = '1'; usb_u2u3_lfps_poll_tmr = '01')	ATE-Char			87	µs	DEV-TIM-PRIO1-013c
		USB3.2 mode (LFPS polling 19 % on, usb_sqd_poll_u2_u3 = '1'; usb_u2u3_lfps_poll_tmr = '10')	ATE-Char			120	µs	DEV-TIM-PRIO1-013d
		USB3.2 mode (LFPS polling 13 % on, usb_sqd_poll_u2_u3 = '1'; usb_u2u3_lfps_poll_tmr = '11')	ATE			150	µs	DEV-TIM-PRIO1-013e
		DisplayPort mode (D3 wake-up through AUX transaction)	ATE		10		µs	DEV-TIM-PRIO1-013f
Gp_Bi	Peaking gain (EQ gain compensation relative to gain at 100 MHz) of the bidirectional channels (BIO, DIO, DRX1, DRX2) at 5 GHz, 4.05 GHz, and 2.5 GHz, 0 °C to 65 °C	Setting b'1011 in Table 10, Table 11, and Table 12 at 5.0 GHz	ATE		12		dB	DEV-DB-PRIO2-014
		Setting b'1011 in Table 10, Table 11, and Table 12 at 4.05 GHz	ATE		10.5		dB	DEV-DB-PRIO2-015
		Setting b'1011 in Table 10, Table 11, and Table 12 at 2.5 GHz	ATE		8.2		dB	DEV-DB-PRIO2-016
Gp_Uni	Peaking gain (EQ gain compensation relative to gain at 100 MHz) of the unidirectional channels (AIN and CIN) at 5 GHz, 4. 05 GHz, and 2.5 GHz, 0 °C to 65 °C	Setting b'1011 in Table 13, Table 14, Table 15 at 5.0 GHz	ATE		13.2		dB	DEV-DB-PRIO2-052
		Setting b'1011 in Table 13, Table 14, Table 15 at 4.05 GHz	ATE		12.5		dB	DEV-DB-PRIO2-053
		Setting b'1011 in Table 13, Table 14, Table 15 at 2.5 GHz	ATE		9.2		dB	DEV-DB-PRIO2-054
Gp, var	Peaking gain variation at BST6(unidir)/ BST8(bidir) at 5.0 GHz, 0 °C to 65 °C		ATE-Char	-3		1	dB	DEV-DB-PRIO1-017
Gf	Flat gain at 100 MHz	Setting b'00 in Table 8	ATE		1		dB	DEV-DB-PRIO2-018
		Setting b'01 in Table 8	ATE		0		dB	DEV-DB-PRIO2-019
		Setting b'10 in Table 8	ATE		-1		dB	DEV-DB-PRIO2-020
Gf, var	Flat gain variations over Gf at 100 MHz		ATE-Char	-2		2	dB	DEV-DB-PRIO1-021
OSL_{5GHz}	Output swing linearity (-1 dB compression point) at 5.0 GHz, maximum peaking gain setting. 0 °C to 65 °C	Setting b'00 in Table 16	Bench	430	600		mVppd	DEV-VOL-PRIO2-022
		Setting b'01 in Table 16	Bench	540	700		mVppd	DEV-VOL-PRIO2-023
		Setting b'10 in Table 16	Bench	630	800		mVppd	DEV-VOL-PRIO2-024
V_{noise_in}	Input referred noise	100 MHz to 5 GHz; Peaking gain of 12 dB (at 5 GHz) and OSL 800 mVppd	Bench		0.7	1.5	mV_{rms}	DEV-VOL-PRIO2-025
V_{LOS}	LoS threshold level, tested at DC level, 0 °C to 65 °C	Setting b'11 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	ATE-Char	70	100	130	mVppd	DEV-VOL-PRIO1-026

Table 22. Device characteristics...*continued*

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
		Setting b'11 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	ATE-Char	50	80	110	mVppd	DEV-VOL-PRIO1-027
		Setting b'10 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	ATE-Char	60	90	120	mVppd	DEV-VOL-PRIO1-028
		Setting b'10 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	ATE-Char	40	70	100	mVppd	DEV-VOL-PRIO1-029
		Setting b'01 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	ATE-Char	50	80	110	mVppd	DEV-VOL-PRIO1-030
		Setting b'01 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	ATE-Char	30	60	90	mVppd	DEV-VOL-PRIO1-031
		Setting b'00 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	ATE-Char	35	65	95	mVppd	DEV-VOL-PRIO1-032
		Setting b'00 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	ATE-Char	15	45	75	mVppd	DEV-VOL-PRIO1-033
	LoS threshold level, tested at DC - 5GHz level, 0 °C to 65 °C	Setting b'11 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	Bench	60	100	200	mVppd	DEV-VOL-PRIO1-054
		Setting b'11 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	Bench	38	80	155	mVppd	DEV-VOL-PRIO1-055
		Setting b'10 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	Bench	53	90	182	mVppd	DEV-VOL-PRIO1-056
		Setting b'10 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	Bench	30	70	135	mVppd	DEV-VOL-PRIO1-057
		Setting b'01 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	Bench	43	80	167	mVppd	DEV-VOL-PRIO1-058
		Setting b'01 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	Bench	20	60	120	mVppd	DEV-VOL-PRIO1-059
		Setting b'00 in I2C Reg[0x0F] bit [5:4] or [1:0], squelched to unsquelch transition	Bench	30	65	145	mVppd	DEV-VOL-PRIO1-060
		Setting b'00 in I2C Reg[0x0F] bit [5:4] or [1:0], unsquelched to squelch transition	Bench	10	45	90	mVppd	DEV-VOL-PRIO1-061
$I_{DD(Active)}$	Total supply power on VDD_D and VCC_X. All 4	Output swing linearity of 800 mVppd	ATE		334	504	mW	DEV-CUR-PRIO1-034

Table 22. Device characteristics...*continued*

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
	channels active, mode 2/3	Output swing linearity of 700 mVppd	ATE-Char		312	482	mW	DEV-CUR-PRIO1-035
		Output swing linearity of 600 mVppd	ATE-Char		292	465	mW	DEV-CUR-PRIO1-036
	Total supply power on VDD_D and VCC_X. 2 channels USB 3.2 active, mode 1, or mode 3 DP 2 lane.	Output swing linearity of 800 mVppd	ATE		170	257	mW	DEV-CUR-PRIO1-037
		Output swing linearity of 700 mVppd	ATE-Char		159	246	mW	DEV-CUR-PRIO1-038
		Output swing linearity of 600 mVppd	ATE-Char		149	237	mW	DEV-CUR-PRIO1-039
	Total supply power on VDD_D and VCC_X. 1 lane/channel DP active, mode 3 DP 1 lane	Output swing linearity of 800 mVppd	ATE		89	135	mW	DEV-CUR-PRIO1-040
		Output swing linearity of 700 mVppd	ATE-Char		83	129	mW	DEV-CUR-PRIO1-041
		Output swing linearity of 600 mVppd	ATE-Char		78	125	mW	DEV-CUR-PRIO1-042
$I_{DD(PowerSave)}$	Total supply power on VDD_D and $VCC_{0/1/2}$, EN = HIGH	Mode 1, USB3 x1, U2/U3 state (LFPS polling 13 % on, usb_sqd_poll_u2_u3 = '1'; usb_u2u3_lfps_poll_tmr = '11')	ATE		1.23	2.05	mW	DEV-CUR-PRIO2-043
		Mode 1, USB3 x1, no cable connection, only RX detect circuitries are enabled	ATE		1.01	1.75	mW	DEV-CUR-PRIO1-044
		Mode 3, DP D3 mode, when LoS detector is disabled on ML0, and AUX snooping is enabled	ATE		0.54	0.87	mW	DEV-CUR-PRIO2-045
		Mode 0, deep power-saving state	ATE		73	450	µW	DEV-CUR-PRIO2-046
$I_{DD(Disable)}$	Supply current in disabled state. EN = LOW	VDD_{IO}	ATE		1	10	µA	DEV-CUR-PRIO2-047
		VDD_D + VCC_x	ATE		16	117	µA	DEV-CUR-PRIO2-048
$I_{DDIO(Enable)}$	VDD_{IO} supply current in enable state, EN = HIGH. Excluding external pullup current.[1]	When the I2C interface is inactive	ATE		1	10	µA	DEV-CUR-PRIO2-052
$I_{backpower}$	Back power current when VDD_D, VDD_{IO}, VCC_X are at ground	Current into SCL pin when SCL is tied to 1.2 V	ATE			1	µA	DEV-CUR-PRIO2-049
		Current into SDA pin when SDA is tied to 1.2 V	ATE			1	µA	DEV-CUR-PRIO2-050
$t_{Supply\_startup}$	Power supplies ramp up time		System	0.02		5	ms	DEV-TIM-PRIO2-051

[1] When I2C interface is operating at Fast-mode Plus bit rate, instantaneous current on VDD_{IO} supply is approximately 10 µA (typical), 25 µA (max).

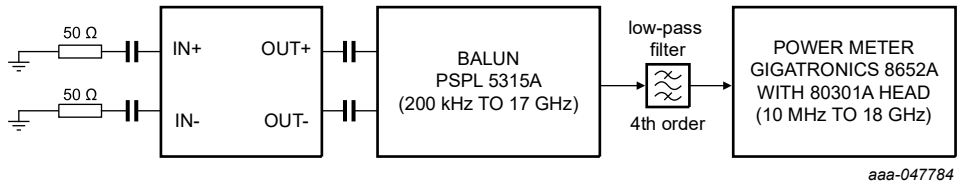


Figure 20. Noise test configuration

10.2 Input AC/DC characteristics

Table 23. Input AC/DC characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
$C_{RX\_AC\_COUPLING}$	RX AC coupling capacitance		System	297	330	363	nF	INC-CAP-PRIO1-001
$R_{RX-DC-CM}$	Receiver DC common mode impedance, 0 °C to 65 °C		ATE	18	25	30	Ω	INC-RES-PRIO1-002
$R_{RX-DIFF-DC}$	Receiver DC differential mode impedance, 0 °C to 65 °C		ATE	90	100	110	Ω	INC-RES-PRIO1-003
$Z_{RX-HIGH-IMP-DC-POS}$	DC input common mode impedance during reset or power down.		ATE	10			kΩ	INC-RES-PRIO1-004
$V_{RX-LFPS-DET-DIFFp-p}$	LFPS detect threshold		ATE-Char	100	180	300	mVpp	INC-VOL-PRIO1-005
$V_{RX-CM-AC-PP}$	RX AC common mode voltage tolerance for USB3.2	A single tone test at 120 MHz is deemed to be an adequate stress test	Bench			300	mVpp	INC-VOL-PRIO1-006
$V_{DP-RX-CM-PP1}$	RX AC common mode voltage tolerance for DP2.0 application	A single tone test at 400 MHz is deemed to be an adequate stress test	Bench			100	mVpp	INC-VOL-PRIO1-007
$V_{RX-CM-DC-ACTIVE-IDLE-DELTA\_pp}$	RX AC common mode voltage during U1 to U0 transition		Bench			400	mVpp	INC-VOL-PRIO1-008
$V_{IP-DC-CM}$	DC biasing/common mode voltage	Biasing on all Super-Speed pins	ATE		1.8		V	INC-VOL-PRIO2-009
$V_{RX-CM-DC\_CONN}$	Instantaneous DC common mode voltage coupled from far-end TX	With 50 Ω receiver load	Bench	-0.3		1	V	INC-VOL-PRIO1-010
		With 50 kΩ receiver load[1]	Bench	-0.5		1	V	INC-VOL-PRIO1-011
$V_{RX-DIFF-PP}$	USB and DP Input voltage (peak-to-peak differential signal)	Minimum value to be aligned with LoS detector threshold level	System			1200	mVppd	INC-VOL-PRIO1-012
$RL_{DD, IN}$	Input differential mode return loss	Sdd11, Sdd22; 10 MHz to 5 GHz; 90 Ω reference, 0 °C to 65 °C	Bench		13		dB	INC-DB-PRIO2-013
$RL_{CC, IN}$	Input common mode return loss	Scc11, Scc22; 10 MHz to 5 GHz; 90 Ω reference, 0 °C to 65 °C	Bench		12		dB	INC-DB-PRIO2-014
$RL_{CD, IN}$	Differential-to-common mode conversion	Scd11, Scd21, Scd22, Scd12; 10 MHz to 5 GHz; 90 Ω reference, BST = 0, FG = 0 dB, 0 °C to 65 °C	Bench			-23	dB	INC-DB-PRIO2-015

Table 23. Input AC/DC characteristics*...continued*

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
DDNEXT1	Crosstalk between adjacent high-speed pairs operating in opposite directions	10 MHz to 5 GHz; between DTX1 and DRX1, or between DTX2 and DRX2, or between B_IO and A_IN, or between C_IN and D_IO	Bench		-45		dB	INC-DB-PRIO2-016
DDNEXT2	Crosstalk between adjacent high-speed pairs operating in the same directions	10 MHz to 5 GHz; between DTX1 and DRX1, or between DTX1 and DTX2, or between DTX2 and DRX2, or between B_IO and A_IN, or between A_IN and C_IN, or between C_IN and D_IO	Bench		-35		dB	INC-DB-PRIO2-017

[1] If the SoC design cannot meet the 50 kΩ impedance requirement during off state, external pulldown resistors must be installed on the PCB.

10.3 Output AC/DC characteristics

Table 24. Output AC/DC characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
$C_{TX\_AC\_COUPLING}$	TX AC coupling capacitance		System	75		265	nF	OUC-CAP-PRIO1-001
R_{TX-DC}	Transmitter output DC common mode impedance, 0 °C to 65 °C		ATE	18	25	30	Ω	OUC-RES-PRIO1-002
$R_{TX-DIFF-DC}$	Transmitter output differential impedance, 0 °C to 65 °C		ATE	72	80	88	Ω	OUC-RES-PRIO1-003
$V_{TX-RCV-DET}$	Voltage change allowed during USB receiver detection	Positive voltage swing to sense the receiver termination detection	ATE			600	mV	OUC-VOL-PRIO1-004
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change	When the link is in Electrical Idle	ATE	-300		600	mVppd	OUC-VOL-PRIO1-005
$I_{TX-SHORT}$	The total current TX can source if short to ground		Bench			60	mA	OUC-CUR-PRIO1-006
$V_{TX-DC-CM}$	Transmitter DC biasing/ common mode voltage	Output swing linearity of 800 mVppd	ATE		1.1		V	OUC-VOL-PRIO2-007
		Output swing linearity of 700 mVppd	ATE		1.2		V	OUC-VOL-PRIO2-008
		Output swing linearity of 600 mVppd	ATE		1.3		V	OUC-VOL-PRIO2-009
$V_{TX-CM-AC-PP\_ACTIVE}$	TX AC common mode voltage due to TXp TXn mismatch	Device input fed with differential signal	Bench			100	mVpp	OUC-VOL-PRIO1-010
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common mode voltage between the USB U1 and U0 states		ATE			200	mV	OUC-VOL-PRIO1-011
$V_{TX-IDLE-DIFF-AC-pp}$	Differential peak-to-peak output voltage during idle		ATE	0		10	mV	OUC-VOL-PRIO1-012

Table 24. Output AC/DC characteristics...*continued*

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	DC electrical idle differential output voltage		ATE	0		10	mV	OUC-VOL-PRIO1-013
$V_{TX\text{-}DC+AC\text{-}CONN}$	Instantaneous DC common mode voltage coupled from far-end RX	With 50 Ω receiver load	Bench	-0.3		1	V	OUC-VOL-PRIO1-014
		With 50 kΩ receiver load[1]	Bench	-0.5		1	V	OUC-VOL-PRIO1-015
$RL_{DD,\ OP}$	Output differential mode return loss	Sdd33, Sdd44; 100 MHz to 5 GHz; 90 Ω reference, 0 °C to 65 °C	Bench	11	13		dB	OUC-DB-PRIO2-016
$RL_{CC,\ OP}$	Output common mode return loss	Scc33, Scc44; 100 MHz to 5 GHz; 90 Ω reference, 0 °C to 65 °C	Bench	9	12		dB	OUC-DB-PRIO2-017

[1] If the SoC design cannot meet the 50 kΩ impedance requirement during off state, external pulldown resistors must be installed on the PCB.

10.4 AUX monitor characteristics

Table 25. AUX monitor characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
$V_{I\text{-}AUX}$	Bias voltage at the pin	AUXP/AUXN pins	System	-0.3		3.6	V	AUX-VOL-PRIO1-001
f_{AUX}	AUX bit rate		System	0.87	1	1.17	Mbit/s	AUX-FRQ-PRIO2-002
$V_{AUX\text{-}AC\text{-}DIFF\text{-}pp}$	AUX AC differential peak-to-peak	AUXP/AUXN pins	System	0.087		1.5	Vppd	AUX-VOL-PRIO1-003
I_{IL}	Leakage current at the pin	Pin voltage 3.6 V	ATE			2.5	µA	AUX-CUR-PRIO1-004
$I_{backpower}$	Back power current when VDD_D, VDD_{IO}, VCC_X are at ground	Current into AUXP/AUXN pins when pins are tied to 3.3 V	ATE			2.5	µA	AUX-CUR-PRIO2-005
Z_{in}	AUX monitor differential input impedance	Over frequency range of interest DC to 5 MHz	Bench		4		kΩ	AUX-RES-PRIO2-006

10.5 EN characteristics

Table 26. EN characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
V_{IH}	High-level voltage		ATE-Char	$0.7VDD_{IO}$			V	ENC-VOL-PRIO1-001
V_{IL}	Low-level voltage		ATE-Char			$0.3VDD_{IO}$	V	ENC-VOL-PRIO1-002
V_{HYS}	Input hysteresis voltage		ATE-Char	$0.1VDD_{IO}$				ENC-VOL-PRIO1-003
I_{IL}	Leakage current at the pin	VDD_{IO} = 1.2 V, pin voltage = 1.2 V	ATE			12	µA	ENC-CUR-PRIO1-004
$I_{backpower}$	Back power current when VDD_D, VDD_{IO}, VCC_X are at ground	Current into EN pin when EN is tied to 1.2 V	ATE			12	µA	ENC-CUR-PRIO1-005
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		ATE	0		50	ns	ENC-TIM-PRIO1-006
$R_{PullDown}$	Internal pulldown		ATE	100			kΩ	ENC-RES-PRIO1-007

10.6 I2C AC/DC characteristics

10.6.1 Standard mode

Table 27. Standard mode dynamic characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
f_{I2C}	I2C clock frequency	Standard mode	ATE	0		100	kHz	STD-FRQ-PRIO1-001
V_{PULLUP}	I2C interface operation voltage	Standard mode, system requirement	System	1.08	1.2	1.32	V	STD-VOL-PRIO1-002
R_{PULLUP}	I2C interface pullup resistor	Standard mode, system requirement	System		2.2		kΩ	STD-RES-PRIO1-003
V_{IH}	High-level input voltage	Standard mode	ATE-Char	$0.7VDD_{IO}$			V	STD-VOL-PRIO1-004
V_{IL}	Low-level input voltage	Standard mode	ATE-Char			$0.3VDD_{IO}$	V	STD-VOL-PRIO1-005
V_{hys}	Hysteresis of Schmitt trigger inputs	Standard mode	ATE-Char	$0.1VDD_{IO}$			V	STD-VOL-PRIO1-006
V_{OL}	Low-level output voltage	Standard mode, 2 mA sink current	ATE	0		0.3	V	STD-VOL-PRIO1-007
I_{OL}	Low-level output current	V_{OL} = 0.3 V	ATE	6		45[1]	mA	STD-CUR-PRIO1-009
I_{IL}	Low-level input current	Standard mode, Pin voltage = 0.1 V_{PULLUP} to 0.9 $V_{PULLUP, max}$	ATE	-10		10	µA	STD-CUR-PRIO1-010
C_I	Capacitance of I/O pins	Standard mode	Bench			10	pF	STD-CAP-PRIO1-011
$t_{HD,STA}$	Hold time (repeated-START) condition	Standard mode	ATE	4			µs	STD-TIM-PRIO1-012
t_{LOW}	Low period of I2C clock	Standard mode	ATE	4.7			µs	STD-TIM-PRIO1-013
t_{HIGH}	High period of I2C clock	Standard mode	ATE	4			µs	STD-TIM-PRIO1-014
$t_{SU,STA}$	Setup time (REPEAT) START condition	Standard mode	ATE	4.7			µs	STD-TIM-PRIO1-015
$t_{HD, DAT}$	Data hold time	Standard mode	ATE	0			µs	STD-TIM-PRIO1-016
$t_{SU, DAT}$	Data setup time	Standard mode	ATE	250			ns	STD-TIM-PRIO1-017
$t_{SU, STO}$	Setup time for STOP condition	Standard mode	ATE	4			µs	STD-TIM-PRIO1-018
t_{BUF}	Bus free time between STOP and START condition	Standard mode	ATE	4.7			µs	STD-TIM-PRIO1-019
t_r	Rise time of SCL/SDA signals	Standard mode, pullup resistor of 2.2 kΩ to VDD_{IO}, with C_b = 120 pF	System			1000	ns	STD-TIM-PRIO1-020
t_f	Fall time of SCL/SDA signals	Standard mode, pullup resistor of 2.2 kΩ to VDD_{IO}, with C_b = 120 pF	Bench			300	ns	STD-TIM-PRIO1-021
$t_{VD,DAT}$	Data valid time	Standard mode	ATE			3.45	µs	STD-TIM-PRIO1-022
$t_{VD,ACK}$	Data valid acknowledge time	Standard mode	ATE			3.45	µs	STD-TIM-PRIO1-023
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Standard mode	ATE	0		50	ns	STD-TIM-PRIO1-024
C_b	Capacitive load for each bus line	Standard mode, system requirement	System		120		pF	STD-CAP-PRIO1-027

[1] I/O implements Miller cap based slew rate control.

10.6.2 Fast mode

Table 28. Fast mode dynamic characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
f_{I2C}	I2C clock frequency	Fast mode	ATE	0		400	kHz	FST-FRQ-PRIO1-001
V_{PULLUP}	I2C interface operation voltage	Fast mode, system requirement	System	1.08	1.2	1.32	V	FST-VOL-PRIO1-002
R_{PULLUP}	I2C interface pullup resistor	Fast mode, system requirement	System		800		Ω	FST-RES-PRIO1-003
V_{IH}	High-level input voltage	Fast mode	ATE-Char	$0.7VDD_{IO}$			V	FST-VOL-PRIO1-004
V_{IL}	Low-level input voltage	Fast mode	ATE-Char			$0.3VDD_{IO}$	V	FST-VOL-PRIO1-005
V_{hys}	Hysteresis of Schmitt trigger inputs	Fast mode	ATE-Char	$0.1VDD_{IO}$			V	FST-VOL-PRIO1-006
V_{OL}	Low-level output voltage	Fast mode, 2 mA sink current	ATE	0		0.4	V	FST-VOL-PRIO1-007
I_{OL}	Low-level output current	V_{OL} = 0.3 V	ATE	6		45[1]	mA	FST-CUR-PRIO1-009
I_{IL}	Low-level input current	Fast mode, Pin voltage = 0.1 V_{PULLUP} to 0.9 $V_{PULLUP, max}$	ATE	-10		10	µA	FST-CUR-PRIO1-010
C_I	Capacitance of I/O pins	Fast mode	Bench			10	pF	FST-CAP-PRIO1-011
$t_{HD,STA}$	Hold time (repeated-START) condition	Fast mode	ATE	0.6			µs	FST-TIM-PRIO1-012
t_{LOW}	Low period of I2C clock	Fast mode	ATE	1.3			µs	FST-TIM-PRIO1-013
t_{HIGH}	High period of I2C clock	Fast mode	ATE	0.6			µs	FST-TIM-PRIO1-014
$t_{SU,STA}$	Setup time (REPEAT) START condition	Fast mode	ATE	0.6			µs	FST-TIM-PRIO1-015
$t_{HD, DAT}$	Data hold time	Fast mode	ATE	0			µs	FST-TIM-PRIO1-016
$t_{SU, DAT}$	Data setup time	Fast mode	ATE	100			ns	FST-TIM-PRIO1-017
$t_{SU, STO}$	Setup time for STOP condition	Fast mode	ATE	0.6			µs	FST-TIM-PRIO1-018
t_{BUF}	Bus free time between STOP and START condition	Fast mode	ATE	1.3			µs	FST-TIM-PRIO1-019
t_r	Rise time of SCL/SDA signals	Fast mode, pullup resistor of 800 Ω to VDD_{IO}, with C_b = 120 pF	System	5		300	ns	FST-TIM-PRIO1-020
t_f	Fall time of SCL/SDA signals	Fast mode, pullup resistor of 800 Ω to VDD_{IO}, with C_b = 120 pF	Bench	5		300	ns	FST-TIM-PRIO1-021
$t_{VD,DAT}$	Data valid time	Fast mode	ATE			0.9	µs	FST-TIM-PRIO1-022
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode	ATE			0.9	µs	FST-TIM-PRIO1-023
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast mode	ATE	0		50	ns	FST-TIM-PRIO1-024
C_b	Capacitive load for each bus line	Fast mode, system requirement	System		120		pF	FST-CAP-PRIO1-027

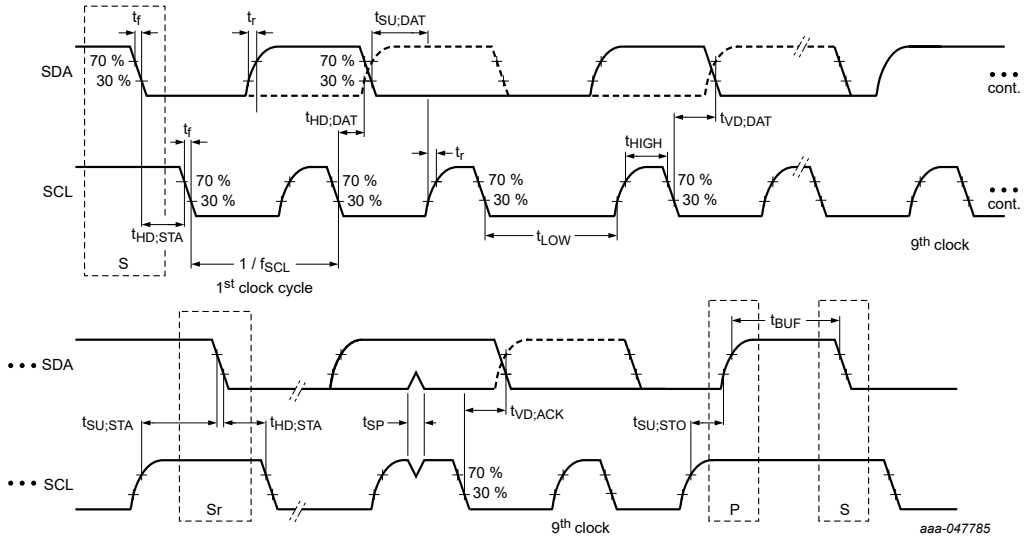
[1] I/O implements Miller cap based slew rate control.

10.6.3 Fast-mode Plus

Table 29. Fast-mode Plus (Fm+) dynamic characteristics

Symbol	Parameter	Conditions	Specification guaranteed by	Min	Typ	Max	Unit	Unique identifier
f_{I2C}	I2C clock frequency	Fast-mode Plus	ATE	0		1000	kHz	FMP-FRQ-PRIO1-001
V_{PULLUP}	I2C interface operation voltage	Fast-mode Plus, system requirement	System	1.08	1.2	1.32	V	FMP-VOL-PRIO1-002
R_{PULLUP}	I2C interface pullup resistor	Fast-mode Plus, system requirement	System		800		Ω	FMP-RES-PRIO1-003
V_{IH}	High-level input voltage	Fast-mode Plus	ATE-Char	$0.7VDD_{IO}$			V	FMP-VOL-PRIO1-004
V_{IL}	Low-level input voltage	Fast-mode Plus	ATE-Char			$0.3VDD_{IO}$	V	FMP-VOL-PRIO1-005
V_{hys}	Hysteresis of Schmitt trigger inputs	Fast-mode Plus	ATE-Char	$0.1VDD_{IO}$			V	FMP-VOL-PRIO1-006
V_{OL}	Low-level output voltage	Fast-mode Plus, 2 mA sink current	ATE	0		0.4	V	FMP-VOL-PRIO1-007
I_{OL}	Low-level output current	V_{OL} = 0.3 V	ATE	6		45[1]	mA	FMP-CUR-PRIO1-009
I_{IL}	Low-level input current	Fast-mode Plus, Pin voltage = 0.1 V_{PULLUP} to 0.9 $V_{PULLUP, max}$	ATE	-10		10	µA	FMP-CUR-PRIO1-010
C_I	Capacitance of I/O pins	Fast-mode Plus	Bench			10	pF	FMP-CAP-PRIO1-011
$t_{HD,STA}$	Hold time (repeated-START) condition	Fast-mode Plus	ATE	0.26			µs	FMP-TIM-PRIO1-012
t_{LOW}	Low period of I2C clock	Fast-mode Plus	ATE	0.5			µs	FMP-TIM-PRIO1-013
t_{HIGH}	High period of I2C clock	Fast-mode Plus	ATE	0.26			µs	FMP-TIM-PRIO1-014
$t_{SU,STA}$	Setup time (REPEAT) START condition	Fast-mode Plus	ATE	0.26			µs	FMP-TIM-PRIO1-015
$t_{HD, DAT}$	Data hold time	Fast-mode Plus	ATE	0			µs	FMP-TIM-PRIO1-016
$t_{SU, DAT}$	Data setup time	Fast-mode Plus	ATE	50			ns	FMP-TIM-PRIO1-017
$t_{SU, STO}$	Setup time for STOP condition	Fast-mode Plus	ATE	0.26			µs	FMP-TIM-PRIO1-018
t_{BUF}	Bus free time between STOP and START condition	Fast-mode Plus	ATE	0.5			µs	FMP-TIM-PRIO1-019
t_r	Rise time of SCL/SDA signals	Fast-mode Plus, pullup resistor of 800 Ω to VDD_{IO}, with C_b = 120 pF	System	5		120	ns	FMP-TIM-PRIO1-020
t_f	Fall time of SCL/SDA signals	Fast-mode Plus, pullup resistor of 800 Ω to VDD_{IO}, with C_b = 120 pF	Bench	5		120	ns	FMP-TIM-PRIO1-021
$t_{VD,DAT}$	Data valid time	Fast-mode Plus	ATE			0.45	µs	FMP-TIM-PRIO1-022
$t_{VD,ACK}$	Data valid acknowledge time	Fast-mode Plus	ATE			0.45	µs	FMP-TIM-PRIO1-023
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast-mode Plus	ATE	0		50	ns	FMP-TIM-PRIO1-024
C_b	Capacitive load for each bus line	Fast-mode Plus, system requirement	System			120	pF	FMP-CAP-PRIO1-027

[1] I/O implements Miller cap based slew rate control.



$V_{IL} = 0.3V_{DD}$; $V_{IH} = 0.7V_{DD}$

Figure 21. Definition of timing for standard/fast mode devices on the I2C bus

11 Package outline

This section includes Figure 22, which illustrates the package outline for PTN37011.

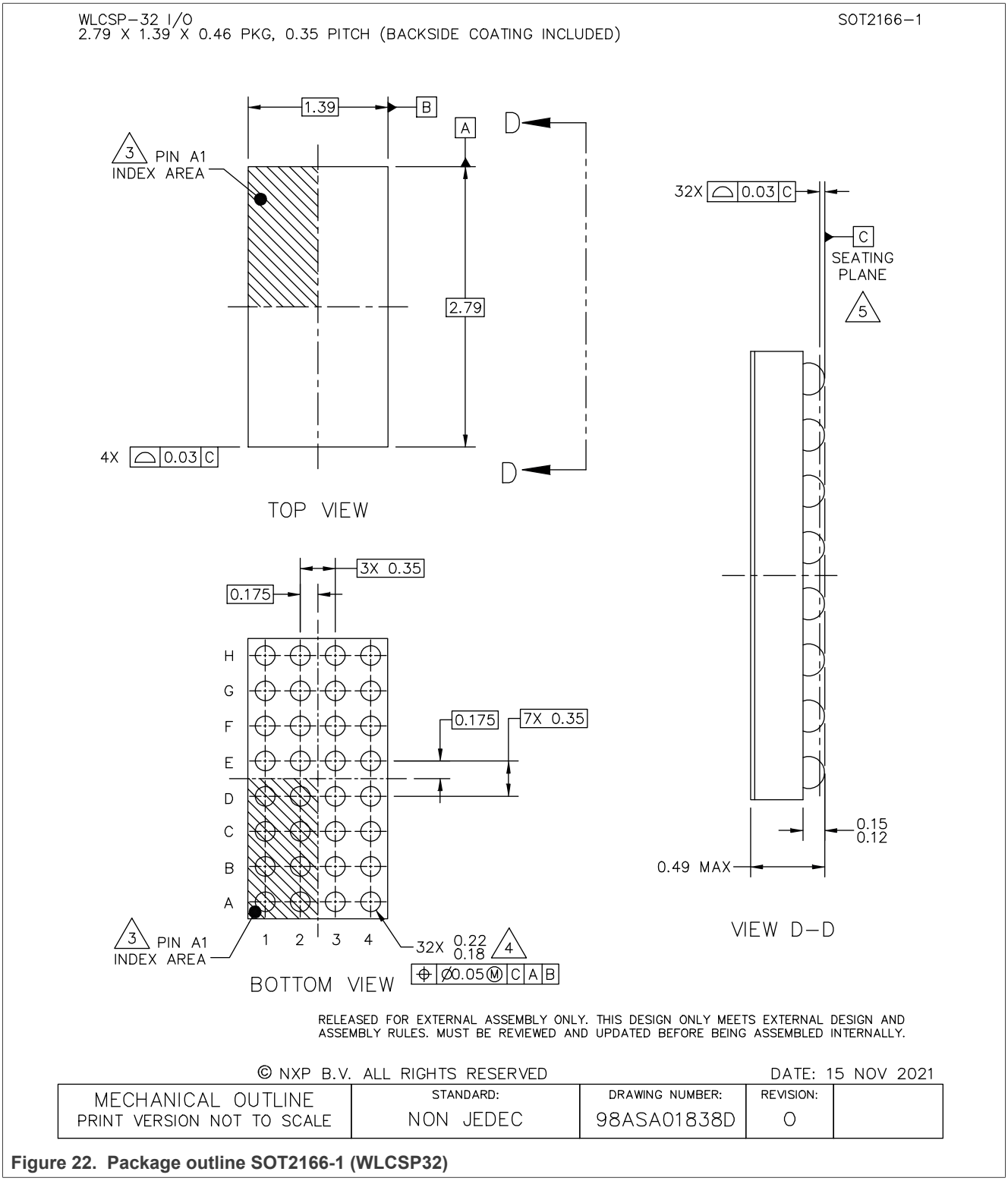


Figure 22. Package outline SOT2166-1 (WLCSP32)

11.1 UBM stack-up information

This section describes the UBM stack-up information for PTN37011.

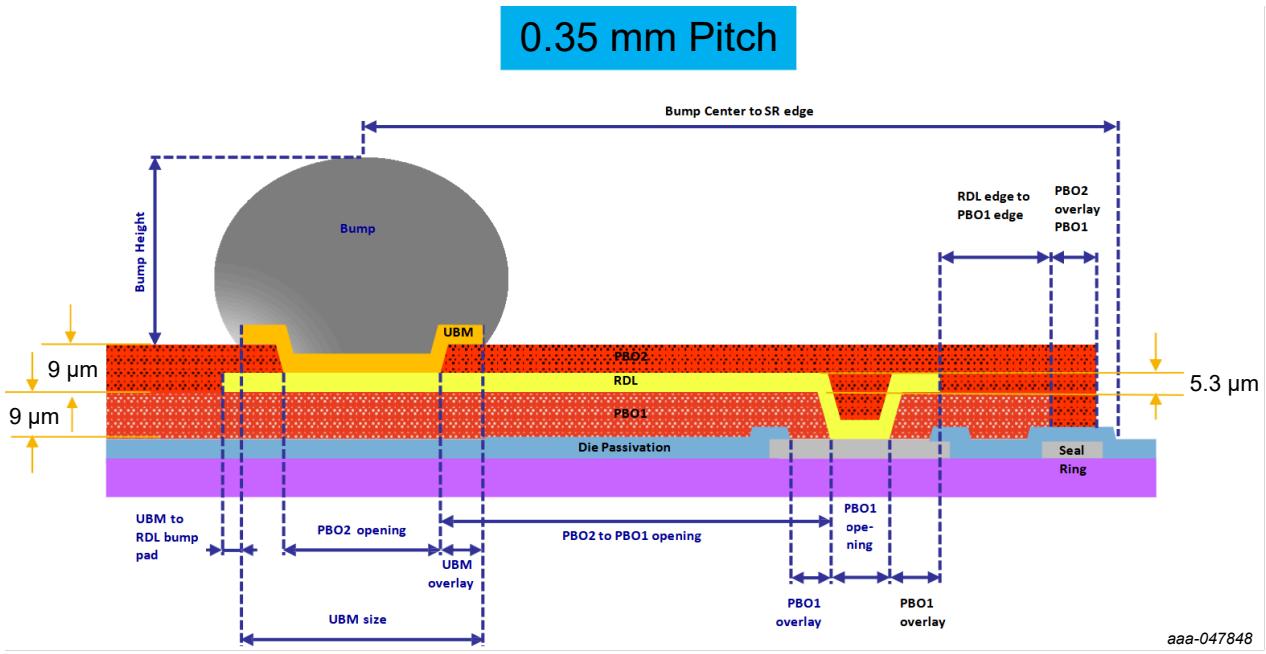


Figure 23. UBM stack-up

Table 30. UBM stack-up parameters

Parameter (Typical)	Description
UBM size	190 µm
UBM thickness	8.6 µm
Ball size	180 µm (prior reflow) 200 µm (after reflow)
Bump height	135 µm
Bump diameter	200 µm
PBO1	9 µm
PBO1 opening	≥ 25 µm
RDL thickness	5.3 µm
PBO2	9 µm
PBO2 opening	150 µm
RDL capture pad	220 µm
PBO termination on top of seal ring	

12 Packing information

This section describes the PTN37011 packing information.

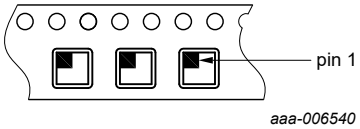
12.1 Dimensions and quantities

Table 31. Dimensions and quantities

Reel dimensions (d × w (mm))[1]	SPQ/PQ (pcs)[2]	Reels per box
330 × 12	6000	1

[1] D = reel diameter; w = tape width
[2] Packing quantity dependent on the specific product type. For ordering and availability details, contact your local NXP representative.

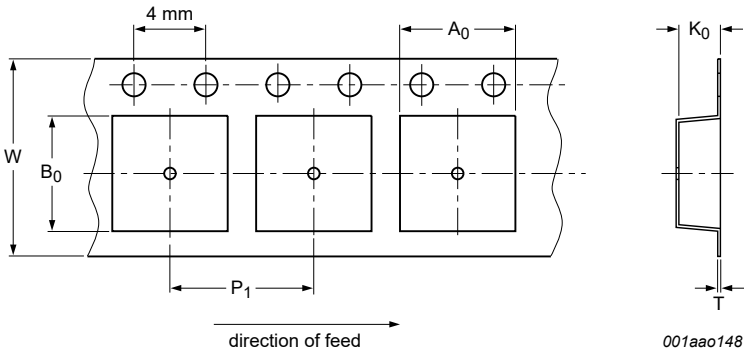
12.2 Product orientation



Pin 1 is in quadrant 1.

Figure 24. Product orientation in carrier tape

12.3 Carrier tape dimensions



Not drawn to scale.

Figure 25. Carrier tape dimensions

Table 32. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	P1 (mm)	W (mm)
1.59 ± 0.05	2.99 ± 0.05	0.62 ± 0.05	0.25 ± 0.02	4 ± 0.1	12 +0.3/-0.1

12.4 Barcode label

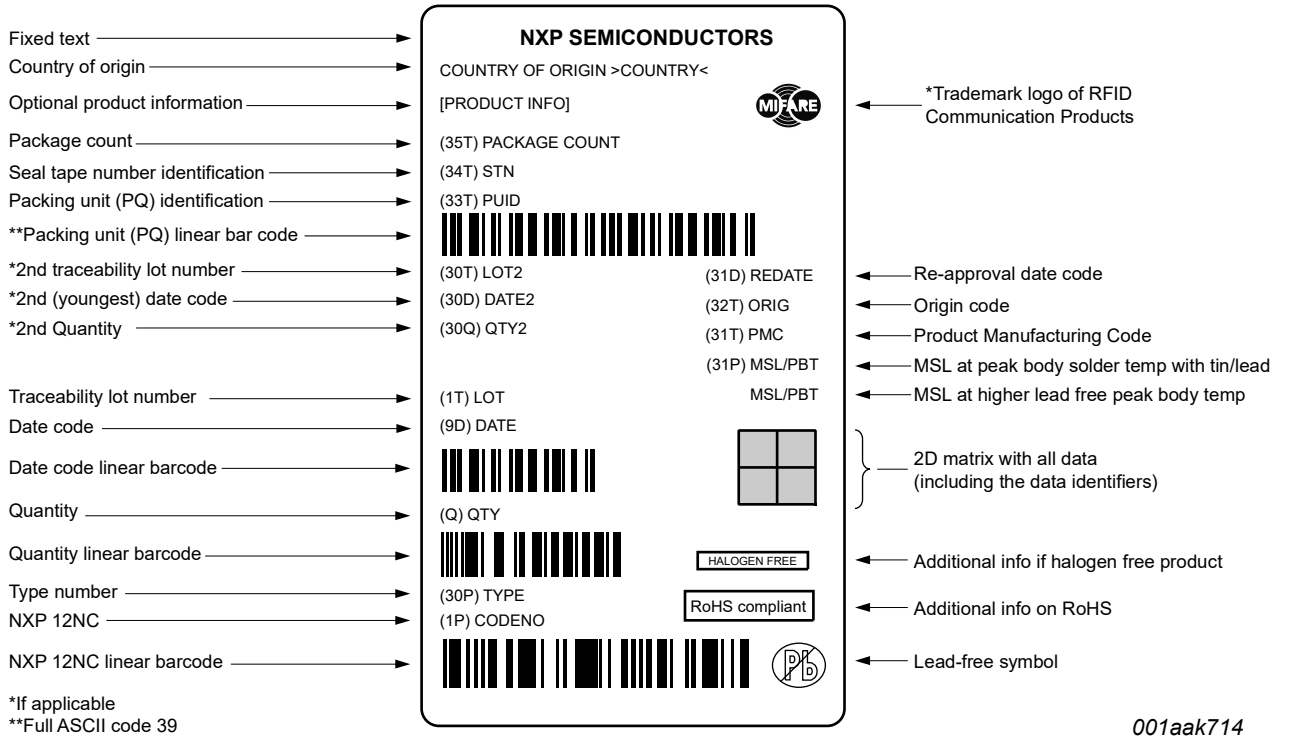


Figure 26. Example of a typical box and reel information barcode label

Table 33. Barcode label dimensions

Box barcode label (l × w (mm))	Reel barcode label (l × w (mm))
100 × 75	100 x 75

13 Soldering

This section provides the PCB footprint figures for soldering the PTN37011.

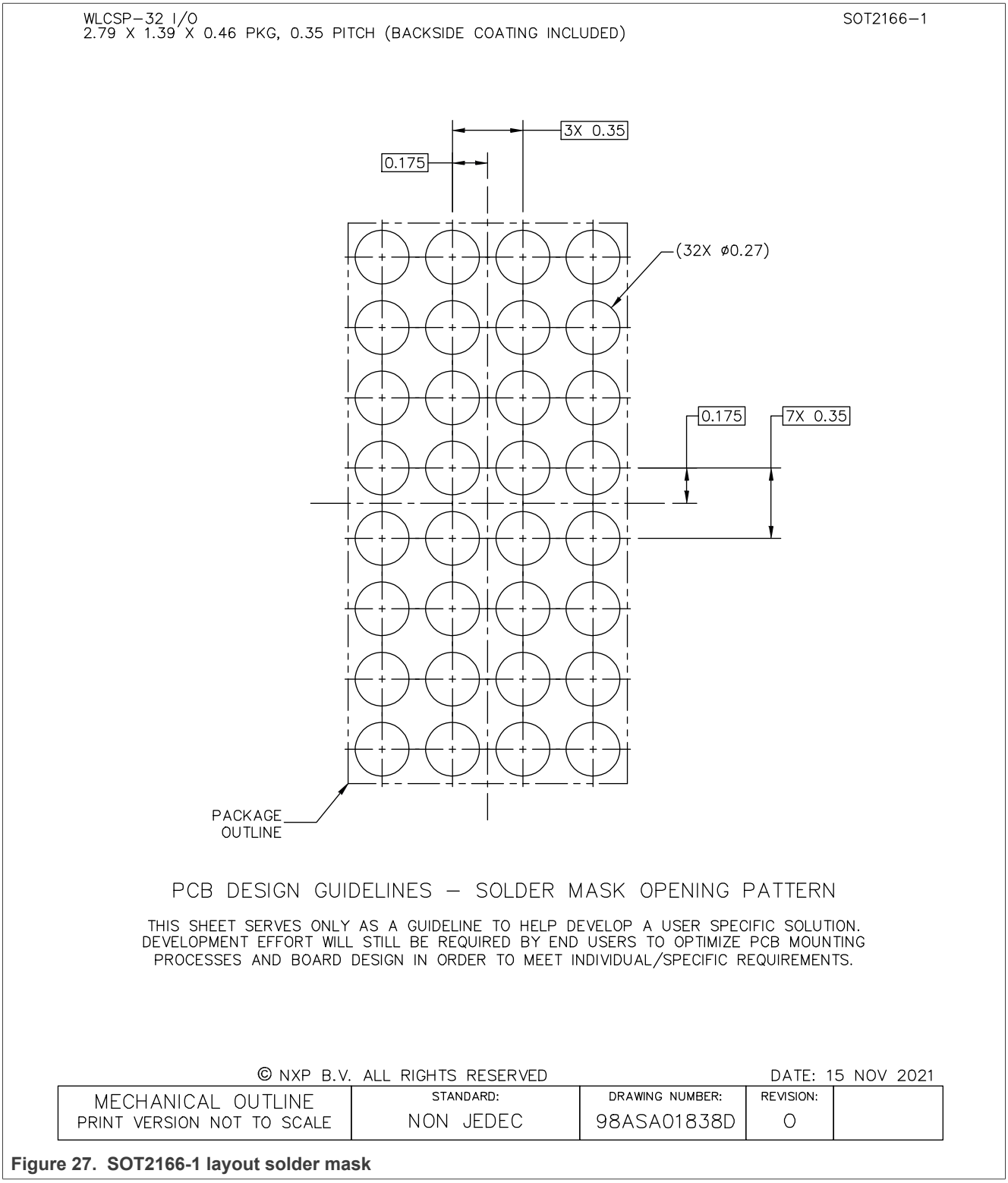


Figure 27. SOT2166-1 layout solder mask

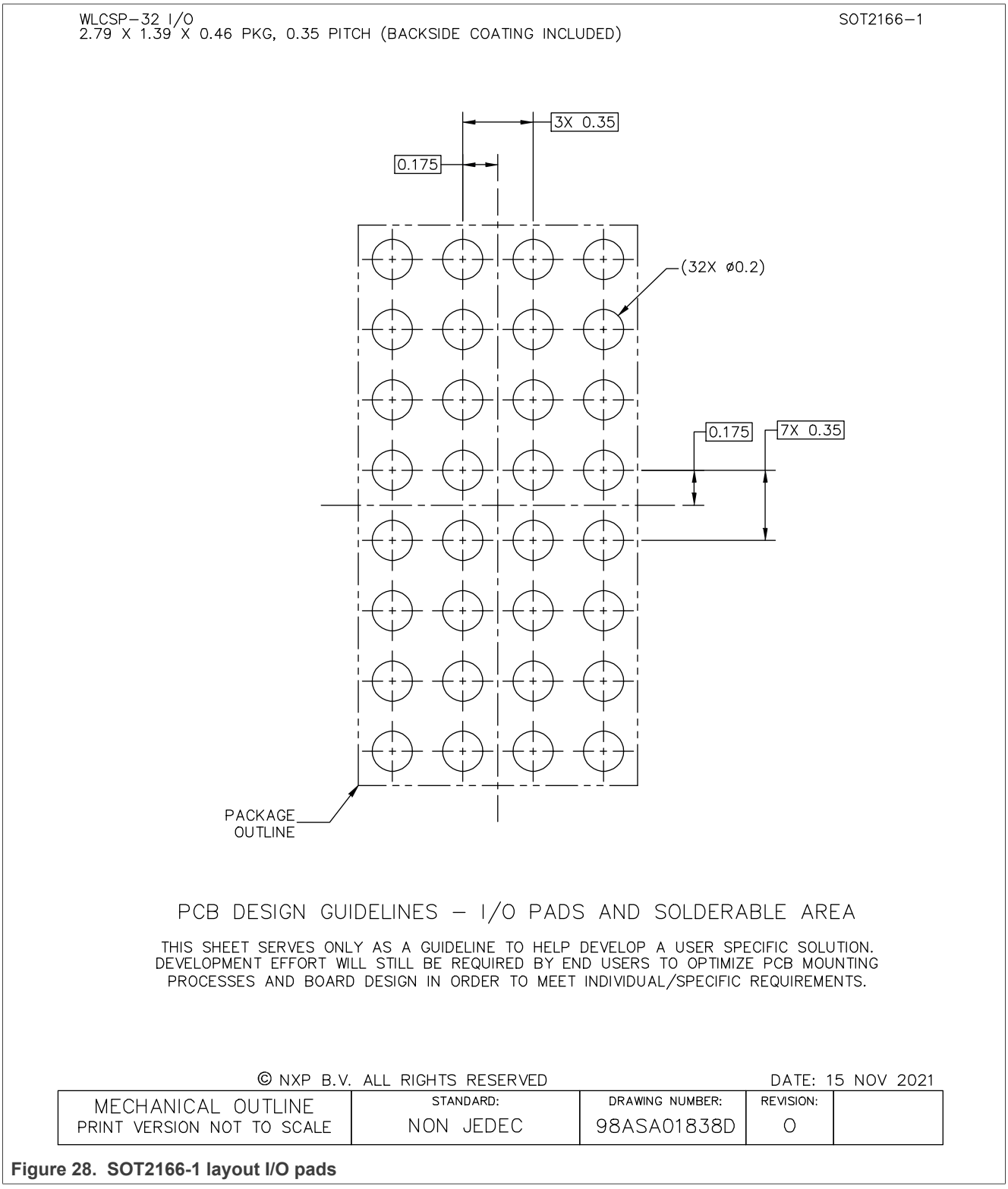


Figure 28. SOT2166-1 layout I/O pads

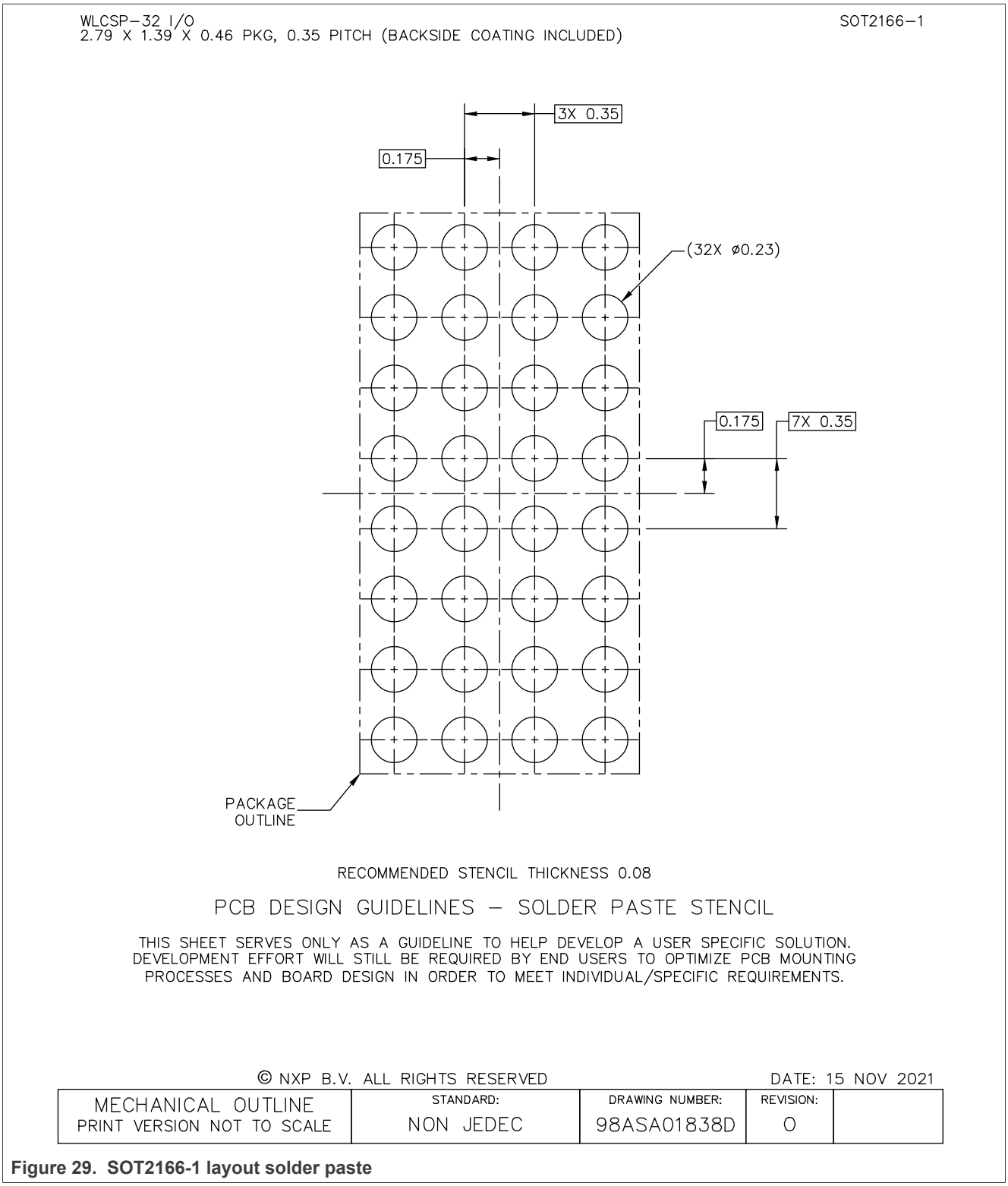


Figure 29. SOT2166-1 layout solder paste

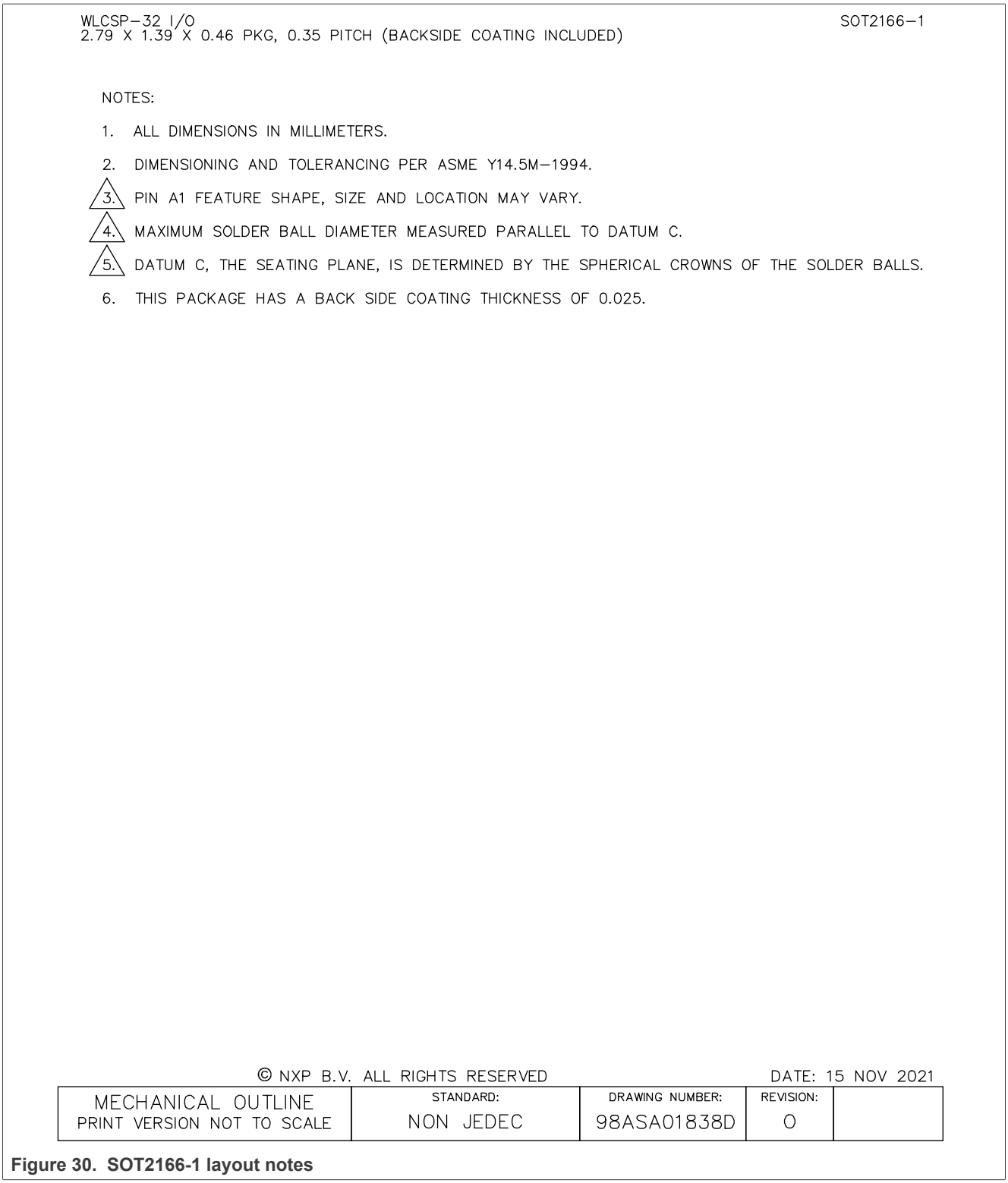


Figure 30. SOT2166-1 layout notes

14 Acronyms

Table 34 describes the acronyms used in this data sheet.

Table 34. Acronyms

Acronym	Description
DFP	Downstream Facing Port
DP	DisplayPort
Gbit/s	Gigabits per second
LBPM	LFPS-Based PWM Message
LFPS	Low Frequency Periodic Signaling
LPM	Link Power Management
NC	No Connect
POR	Power-On Reset
RX	Receiver
TX	Transmitter
UFP	Upstream Facing Port
USB	Universal Serial Bus

15 References

Table 35 lists and explains the additional documents and resources that you can refer to for more information. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 35. Related documentation

Document/Reference	Description
UM10204	I2C-bus specification and user manual, NXP Semiconductors
USB3.2 Specification	USB3.2 Specification, Revision 1.0, September 22, 2017
VESA DisplayPort	VESA DisplayPort v1.4a, Apr 19, 2018 (with the addition of additional data rates - 10/13.5/20 Gbits/s from DisplayPort v2.0 specification)
	VESA DisplayPort Standard Version 2.0, June 26, 2019

16 Revision history

Table 36 summarizes revisions to this document.

Table 36. Revision history

Document ID	Release date	Description
PTN37011 v.1.0	14 January 2026	• Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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