	Compensation Capacitor	125 pF (default)
	Compensation Resistor	500 kΩ (default)

Table 4. BUCK Regulators

Functional block	Feature	OTP selection
BUCK1/2 - Dual Phase	Output Voltage	0.80 V
	Current Limit	3.6 A
	Output Inductor	1 uH(default)
	DVS Ramp of BUCK12	15.6 mV/us (power up) / 10.4 mV/us (powerdown)
	7 U D Q V F R Q G X F W D Q F H	65 umho
BUCK3	Output Voltage	1.10V
	Current Limit	3.6 A
	Output Inductor	1uH(default)
	Ramp	3.47mV/us (power up/down)
	Trans F R Q G X F W D Q F H	65 umho
	R Comp	56 KΩ

Table 5. LDO Regulators

Functional block	Feature	OTP selection
LDO1 Regulator	Output Voltage	1.8 V
	Current Limit	400 mA (default)
LDO2 Regulator	Output Voltage	1.8 V
	LDO Mode	LDO Mode (default)
LDO3 Regulator	Output Voltage	LS_Mode
	LDO Mode	Load Switch (default)

Configuration report for QM OTP program ID: AH rev B

Table 6. HVLDO Regulator

Functional block	Feature	OTP selection
HVLDO Regulator	HVLDO Voltage	0.8 V (default)
	Transition Mode	Switch in Normal / LDO in Standby (default)
	Sequence Control	Follows HVLDOS_OTP slot

Table 7. Voltage Sequence and Timing Configuration

Regulator	Sequence	Enabled	Phase Delay	Clock	TSD Event
VPRE	Auto-enabled	Enabled	No delay	CLK2	
VBOOST	Slot 0	Enabled	No delay	CLK1	Shutdown + DFS
BUCK1	Slot 3	Enabled	1 clock delay	CLK1	Shutdown + DFS
BUCK2	Slot 3	Enabled	2 clock delay	CLK1	Shutdown + DFS
BUCK3	Slot 1	Enabled	3 clock delay	CLK1	Shutdown + DFS
LDO1	Slot 1	Enabled			Shutdown + DFS
LDO2	Slot 0	Enabled			Shutdown + DFS
LDO3	Slot 0	Enabled			Shutdown + DFS
HVLDO	Slot 2	Enabled			Shutdown + DFS
SLOT Width	250 us				

Table 8. Safety State Machine Configuration

Functional block	Feature	OTP selection
Safety Configuration	FailSafe I2C Address	0x21
	8sec Timer to DFS	Timer Disabled
	ABIST1 to RSTB delay	5 ms Delay
	VCOREMON SVS Clamp Limit	16 steps available (default)
	VCOREMON SVS Offset Type	Negative offset (default)

Configuration report for QM OTP program ID: AH rev B

	PGOOD assert with RSTB	PGOOD Asserts with RSTB Fault (default)
	HVLDO Mode Select	Switch Mode (default)
	WDI Polarity	Falling Edge
	WDI on FCCU1	WDI Disabled (default)
	STANDBY Mode	STANDBY Enabled (default)
	STANDBY Polarity	Active Low in standby mode (default)
	STANDBY Request Path	I2C + STBY Pin Transition (default)
	STANDBY Window	STBY Window Enabled (default)
	WD Init Timeout	1024 ms
	Fault Recovery Mode	Disabled
	WD Selection	Simple WD
	WD Monitoring	WD Disabled
	FCCU Monitoring	FCCU Disabled
	LBIST Enable	LBIST Disabled

Table 9. Voltage Monitoring

	VMONEN	Voltage	UV_TH	OV_TH	UV Dbnc	OV Dbnc	PGOOD Ctrl	ABIST Ctrl
VCOREMON	Enabled	0.80000V	95.5%	106%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
VDDIOMON	Enabled	3.3 V	95%	105%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
HVLDOMON	Enabled	0.8 V	93%	107%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
VMON1	Enabled	0.8 V	95%	105%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
VMON2	Enabled	0.8 V	97.5%	104.5%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP

VMON3	Enabled	0.8 V	95.5%	106%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
VMON4	Enabled	0.8 V	95%	105%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP

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Contents

Revision History

Date	OTP Rev / PDF Rev	OTP Changes from the first revision
Oct 21 2020	Rev A / Rev 1.0	Initial prototype release of the OTP settings
Mar 3 2021	Rev B / Rev 1.0	Production release of the OTP 1. ABIST1 to RSTB Delay: Changed to 5ms Delay from No Delay (default) 2. BUCK3 Non DVS Ramp: Changed to 3.47mV/us (power up/down) from 10.42mV/us (power up/down) 3. Standby PGOOD Release Delay: Changed to 400us from 300us 4. LDO1 Sequence: Changed to Slot 1 from Slot 0
Sept 8 2021	Rev B / Rev 1.1	1. Fixed typographical errors in the previously released rev B production OTP