EB00875

Considerations for Avoiding Stuck-In-Reset Scenarios Caused by Non-Correctable ECC Errors in Flash

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by: NXP Semiconductors

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1 Introduction

The MPC574xB/C/G functionality is to keep the device in stuck-in-reset (SIR) mode if a non-correctable ECC error is detected within the flash regions listed:

Table 1. Flash addresses

Start Address	End Address	Size (bytes)	Description
0x00F8_C000	0x00F8_C018	28	HSM Code Flash (Sub-Region)
0x0061_0000	0x0061_0018	28	HSM Code Block 2 (Sub-Region)
0x0061_4000	0x0061_4018	28	HSM Code Block 2 (Sub-Region)
0x0062_0000	0x0062_0018	28	HSM Code Block 3 (Sub-Region)
0x0040_0200	0x0040_024F	80	Lifecycle region in UTEST
0x0040_0300	0x0040_0FFF	3328	DCF record region in UTEST

Care must be taken by the customer when erasing or programming these flash addresses so as to not cause any non-correctable ECC errors.

2 RESET behaviour

To check if the device is successfully leaving reset or if it is permanently SIR, the RESET line of the device must be monitored.

Table 2. MPC574xB/C/G

Package	Package Pin
100 BGA	F1
176 LQFP	29
256 BGA	K1
324 BGA	L1

An oscilloscope must be used to probe the RESET line and begin capturing the state of the pin as the device is powered on:

- On power up, if the RESET line is brought high at any point or is seen to toggle, then the device is **leaving reset**. In this case, the device can be recovered by attaching a debugger and further analysis can be performed to determine the source of the reset.
- On power up, if the RESET line is always low then the device is never leaving reset and is said to be **SIR**. In this scenario, the device can never be recovered and a debugger cannot be attached. Alternative methods of analysis must be explored.

Although there are few methods for debugging a device which is SIR, the reasons for the device demonstrating this behaviour are also few.

3 Common causes of ECC errors

Below is a list of the most common causes of non-correctable ECC errors, in order of most likely:

1. Unstable power supply during programming/erasing causing flash commands to be interrupted mid-execution.
2. EEPROM emulation is always prone to ECC errors. Performing EEPROM emulation in inappropriate regions of flash can cause the device to be caught in a reset escalation. Customer must keep EEPROM emulation contained within the flash regions marked for EEPROM in the reference manual. NXP also provide an EEPROM emulation library.
3. Poorly written flash code by either the customer or the tool vendor which is either not using the NXP Flash driver library, or is not following the same correct implementation.
4. Depending on the device & mask set, BIST can run by default on power-up. The programmer tool must wait a sufficient length of time until this BIST is complete before it begins sending flash commands.

Table 3. Reset duration

Device	Mask set	Reset duration
MPC5748G	1N81M (Cut 2.0)	0.4ms
	0N78S (Cut 3.0)	7.6ms
MPC5746C	1N06M (Cut 1.1)	6.2ms
	1N84S (Cut 2.1)	6.2ms

4 Questions for customers experiencing SIR

If device is not exiting reset, below are a set of questions which should be answered and forwarded to NXP to help find the root cause which is triggering this behaviour:

1. Which device and which mask set is being used, provide full device markings?
2. What is the behaviour of the RESET line at the moment of device power up? Low/high/toggling? (Provide scope plots)
3. Which percentage of devices are experiencing this reset issue?
4. Can the issue be recreated? If so, how?
5. Has anything changed in the customer's process that coincides with these issues occurring?
6. Is the issue being generated at run-time, or during programming of the device?
7. If during programming, which tool is being used to program the device (Lauterbach, PEmicro, Cyclone, ..)?
8. If during runtime, which piece of SW is modifying flash (Bootloader, EEPROM, and which provider?)
9. Which areas of flash are being erased ? Which flash blocks are being written ?
10. Have any of the four HSM code blocks listed in Table 1 been programmed, erased, or used for EEPROM emulation?
11. What is the Life Cycle (LC) of the device?

12. Is there an external watchdog in the system which requires servicing from the device?

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