EB00913

LPDDR2/LPDDR3 Parameter Optimizations for i.MX 7ULP

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by: NXP Semiconductors

Contents

1 Introduction

The intent of this document is to describe the configuration for specific LPDDR2/3 parameters that can help you to achieve the best performance as well as debug target application hardware.

The software and hardware modifications recommended in this document are based on i.MX 7ULP evaluation using NXP software and validation development boards. It is important to highlight that i.MX 7ULP LPDDR2/3 achieved 380 MHz performance, confirmed by the product test data and bench long duration stress testing.

2 LPDDR2/3 parameters covered by this document

The following LPDDR2/3 parameters are covered by this document:

- DDR clock configuration
- Duty cycle
- VIX (differential clock crosspoint voltage)
- IO driver strength adjustment
- IO per-bit de-skew

2.1 DDR clock configuration

It is recommended to use SCG1 APLL:PFD0 as the clock source for the DDR interface. PFD0 is specifically tuned to provide more precise duty cycle accuracy over process variation.

The LPDDR2/3 maximum frequency for i.MX 7ULP is 380.16 MHz, which corresponds to the following configuration (combination of APLLCFG and available in the 7ULP reference manual)

APLLvco Frequency = Fref * (MULT + NUM/DENOM)

PFD Clock Frequency = APLLvco output frequency * 18/frac value

The APLL frequency is tuned for operation at 528 MHz, so it is recommended for the DDR clock to use a combination of MULT and NUM/DENOM that matches 528 MHz.

For example, if a 24-MHz crystal is used for Fref (reference clock), then you should configure 22 for MULT and keep NUM/DENOM at the default values (or DENOM>>NUM). The i.MX 7ULP validation is performed with NUM = 0.

The final frequency is achieved by the fractional value adjustment. 380.16 MHz is achieved with PFD = 25.

2.2 Duty cycle

There are two configurations available in i.MX 7ULP for adjusting the DDR clock duty cycle.

2.2.1 DDR IO duty cycle configuration

The DDR IO configuration reference is in the *i.MX7ULP Reference Manual* (document IMX7ULPRM) section “IOMUXC1 memory map”.

DDR IO duty cycle adjustment is available for both DDR differential clocks and DDR single IO pins and corresponds to the DCYCLE_TRIM parameter. The description extracted from the documentation is as follows:

- DCYCLE_TRIM: Duty Cycle Control Field
  - 00 **DCYCLE_TRIM_0_no_duty_cycle_change** — no duty cycle change
  - 01 **DCYCLE_TRIM_1_duty_cycle_increased** — duty cycle increased ~3.7 %
- EXAMPLE: from 46.3 % HIGH / 53.7 % LOW -> 50 % HIGH / 50 % LOW
  - 10 **DCYCLE_TRIM_2_duty_cycle_decreased** — duty cycle decreased ~3.7 %
- EXAMPLE: from 53.7 % HIGH / 46.3 % LOW -> 50 % HIGH / 50 % LOW
  - 11 **DCYCLE_TRIM_3_no_duty_cycle_change** — no duty cycle change

2.2.2 MMDC MPDCCR register

Additional duty cycle adjustment is available at DDR controller register MMDC MPDCCR. See the detailed description in the *i.MX 7ULP Reference Manual* (document IMX7ULPRM).

The differential DQS3-0 duty cycle can be adjusted by ~1.5 %, independently for read and write paths.

Differential CK0 has two steps of ~1.5 % duty cycle adjustment that can be programmed independently.

NOTE

Any duty cycle adjustments must be applied before running the calibration. NXP i.MX 7ULP development boards achieve the best performance results with the default configuration values.

2.3 VIX (differential clock crosspoint voltage)

DDR IO VIX adjustment is available only for DDR differential clocks (DDR_CLK0 and DDR_CLK0_B) and strobes (DDR_DQS[0-3] and DDR_DQS[0-3]_B). The crosspoint adjustment is controlled by the CRPOINT_TRIM field in the pad control registers **IOMUXC1_DDR_SW_PAD_CTL_PAD_DDR_CLK0** and **IOMUXC1_DDR_SW_PAD_CTL_PAD_DDR_DQSn**.

The description extracted from the reference manual is as follows:

- Crosspoint Adjustment Field:
  - 00 **CRPOINT_TRIM_0_no_output_crosspoint_Vix_change** — no output crosspoint (Vix) change
  - 01 **CRPOINT_TRIM_1_100mV_Vix_shift_down** — 100 mV Vix shift down
  - 10 **CRPOINT_TRIM_2_100mV_Vix_shift_up** — 100 mV Vix shift up
  - 11 **CRPOINT_TRIM_3_200mV_Vix_shift_up** — 200 mV Vix shift up

NOTE

Any VIX adjustments must be applied before running the calibration. NXP i.MX 7ULP development boards achieve the best performance results with the default configuration of CRPOINT_TRIM.

2.4 IO driver strength adjustment

DDR provides different driver strength configuration to allow the best power vs. performance solution for a given application. On lower performance applications, weaker driver strength can be chosen to reduce power consumption.

The following MMDC registers are available for IO driver configuration:

IOMUXC1_DDR_SW_PAD_CTL_PAD_DDR_DQS0-3

IOMUXC1_DDR_SW_PAD_CTL_PAD_DDR_DQM0-3

IOMUXC1_DDR_SW_PAD_CTL_PAD_DDR_CLK0

IOMUXC1_DDR_SW_PAD_CTL_GRP_DS_ADDR (CA0-9 pad groups)

IOMUXC1_DDR_SW_PAD_CTL_GRP_DS_CTRL (CKE0-1, CS0-1_B)

IOMUXC1_DDR_SW_PAD_CTL_GRP_DS_DAT0 (DQ0-7 pad groups)

IOMUXC1_DDR_SW_PAD_CTL_GRP_DS_DAT1 (DQ8-15 pad groups)

IOMUXC1_DDR_SW_PAD_CTL_GRP_DS_DAT2 (DQ16-23 pad groups)

IOMUXC1_DDR_SW_PAD_CTL_GRP_DS_DAT3 (DQ24-31 pad groups)

NOTE

Drive strength should be adjusted with a sufficient margin for operation. The i.MX 7ULP DDR Stress Test tool can be used to evaluate configuration settings and assess the design margin for a target board.

2.5 IO per-bit de-skew

DDR IO de-skew adjustment is available only for single IO (non-differential) signals and corresponds to the DDR_TRIM parameter.

- Output Driver Delay Trim Field:
  - 00 **DDR_TRIM_0_0pS** — 0 pS
  - 01 **DDR_TRIM_1_50pS** — 50 pS
  - 10 **DDR_TRIM_2_100pS** — 100 pS
  - 11 **DDR_TRIM_3_150pS** — 150 pS

Figure 1 illustrates the signal delay achieved by DDR_TRIM settings.

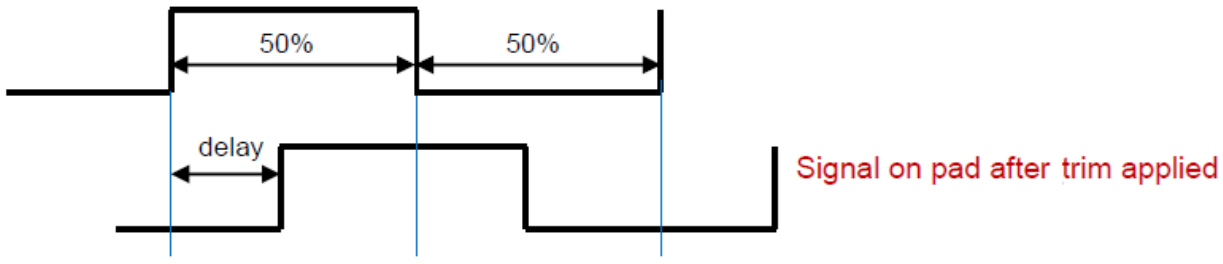

Figure 1. Signal delay achieved by DDR_TRIM settings

NOTE

Any PAD delay adjustments must be applied before running the calibration. NXP i.MX 7ULP development boards achieve the best performance results with the default configuration of PAD delay settings.

3 General recommendations to optimize the DDR interface

The following section provides brief recommendations on how to further optimize the DDR interface. The following recommendations are not absolutely necessary to optimize various parameters and may also have limited applicability on certain customer designs.

3.1 Drive strength configuration

NXP testing shows that lowering the drive strengths can degrade the SDCLK Duty Cycle performance. NXP does not recommend using 60 Ohms (or lower) for any customer design. For the IOPAD Drive Strength, you should set the DSE = 110b (40 Ohms (default value) bits 5, 4, 3) in the IOMUXC1_DDR* registers listed in IO driver strength adjustment .

NXP testing also shows that using DSE = 110b (40 Ohms (default value) bits 5, 4, 3) provides optimal VIX and tDSQH performance. Note that drive strength configuration and optimization is dependent on the customer board layout and design.

3.2 Supply configurations

NXP testing showns that increasing the A7 VDD_PMC11_DIG1_CAP/VDD_DIG1 core voltage level from the default specification can improve the SDCLK jitter and VIX marginally. This is valid for both LDO-enabled (achieved by internal PMC configuration) and LDO-bypass (achieved by configuring external PMIC) modes. See the recommended operating conditions in the *i.MX 7ULP Data Sheet* (document IMX7ULPCEC).

3.3 Supply ripple

Regulation instabilities and ripples on the LDO output can also increase the system clock jitter, which can impact the SDCLK duty cycle and other DDR signal parameters. Ensure correct capacitors sizing and placement on VDD_PMC11_DIG1_CAP, VDD_DDR, VDD18_DDR, and VDD_PLL18.

To minimize jitter, follow the layout and decoupling recommendations in the *i.MX7ULP Hardware Development Guide* (document IMX7ULPHDG).

4 References

- *JEDEC LPDDR2/LPDDR3 SDRAM Standard* (document JEDEC- JESD209-2F / JESD209-3C)
- *i.MX7 Hardware Development Guide* (document IMX7ULPHDG)
- *i.MX 7ULP Data Sheet* (document IMX7ULPCEC)
- *i.MX 7ULP Reference Manual* (document IMX7ULPRM)
- *i.MX 7ULP LPDDR2/LPDDR3* Register Programming Aid
- *i.MX 7ULP* DDR Stress Test Tool

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