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Turn Off Your E Clock to Reduce Noise Emission on the MC68HC11

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Introduction

Since the introduction of the MC68HC11A8 in 1984, many new functions and peripherals have been developed, adding functionality and variety to this versatile family of microcontrollers.

Because of the expanding ROM, EPROM, and RAM available on newer members of the MC68HC11 family, many applications are now feasible in single-chip mode, thereby reducing the number of integrated circuits necessary to complete a control application. Many of the products which now contain MC68HC11's are also noise sensitive applications like digital pagers and cellular phones. This paper describes a feature on MC68HC11's which will reduce noise radiating from the application in addition to reducing the current drawn by the part.

IRVNE Control Bit

Derivatives of the MC68HC11A8 have expanded this family of microcontrollers to more than 45 unique members with more on the way. The original A8 had a unique feature which allowed internal memory resource read cycles to be driven out the data bus. This feature is known as internal read visibility (IRV).

IRV is useful in expanded or special test modes; however, it is not valid in single-chip or special bootstrap modes since the address and data buses are configured as parallel I/O ports.

When IRV is enabled, read cycles of internal memory resources are driven out the data bus, which aids in debugging with a bus state analyzer or logic analyzer. Remember that this feature may cause bus contention unless external memory resources are properly decoded so that no two resources, internal or external, respond to the same address. This complex decoding may be worthwhile in the debug phase of product development but certainly has no place in production systems.

In early MC68HC11s, IRV was enabled in special test mode, and it was disabled in normal expanded multiplexed mode. On newer parts, this bit is writable once in any mode, but only comes out of reset enabled in special test mode. Refer to the following tables for a complete functional description of the IRVNE bit and/or the IRV bit.

After some time and customer feedback, it became apparent that single-chip applications should be able to reduce noise radiation by removing the E clock. Resistors to ground and resistive/capacitive loads were all applied to the E clock to try to smooth the edges of E clock to reduce the high-frequency emissions associated with near vertical edges. The MC68HC11 drivers are strong, and these methods were hardly successful in reducing noise inherent to the fast-switching E clock.

So as a result, the ability to turn off the E clock was implemented. Since this function is only necessary in single-chip and bootstrap modes, its functionality was merged with the IRV bit.

To date, there are three distinct classes of functionality for the IRV function and/or the NE function:

- The first group does not have any control over the E clock. These parts only implement IRV, and this bit can only be written once in any mode.
- The second group includes implementation of the NE function. In single-chip and bootstrap modes, the user can disconnect the E clock from its pin, which is then driven low. These parts allow writes to the IRV/NE bit once in any mode.
- The third group of parts also includes the NE function. However, the IRV/NE bit can be written multiple times in special operating modes (special test and special bootstrap).

Table 1 and Table 2 show the function of the bit and which parts belong to which class.

Table 1. Devices with IRV Described in Table 2

Masked ROM EEPROM	Masked ROM, no EEPROM	No ROM, EEPROM	No ROM, N0 EEPROM	EPROM
MC68HC11A8	MC68HC11A7	MC68HC11A1	MC68HC11A0	—
—	—	MC68HC11E2	—	—
—	—	MC68HC11F1	—	—
MC68HC11G5	—	—	MC68HC11G0	MC68HC711G5
MC68HC11G7	—	—	—	—

Table 2. IRV/NE Bit Functionality for Parts in Table 1

Mode	IRVNE out of reset	E clock out of reset	IRV out of reset	IRVNE affects only	IRVNE an be written
Single-chip	0	On	Off	N/A	Once
Expanded	0	On	Off	IRV	Once
Bootstrap	1	On	Off	N/A	Once
Special Test	1	On	On	IRV	Once

Table 3 and Table 4 describe devices which do not contain the not E clock (NE) function. The E clock is driven out its pin in single-chip modes which may radiate high-frequency noise throughout the application. To reduce noise in these applications, the user may include power and ground planes in multi-layer PC boards or load the E clock pin in an attempt to round the edges of this square wave. Rounding of the corners will reduce high-frequency emissions; however, at least the fundamental frequency remains.

In an effort to reduce radiated noise, the following chips contain the not E clock function in addition to internal read visibility.

Table 3. Devices with IRV Described in Table 4

Masked ROM EEPROM	Masked ROM, no EEPROM	No ROM, EEPROM	No ROM, N0 EEPROM	EPROM
—	MC68HC11D3	—	MC68HC11D0	MC68HC711D3
MC68HC11E9	MC68HC11E8	MC68HC11E1	MC68HC11E0	MC68HC711E9
—	—	—	MC68HC711E9	—
MC68HC11E20	—	—	—	MC68HC711E20
MC68HC11J6	—	—		MC68HC711J6
MC68HC11L6	MC68HC11L5	MC68HC11L1	MC68HC11L0	MC68HC711L6

Table 4. IRV/NE Bit Functionality for Parts in Table 3

Mode	IRVNE out of reset	E clock out of reset	IRV out of reset	IRVNE affects only	IRVNE an be written
Single-chip	**0**	**On**	**Off**	**E clock**	**Once**
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	E clock	Once
Special Test	1	On	On	IRV	Once

When the not E clock function is enabled (IRV/NE = 1 while operating in either single-chip or bootstrap mode), the E clock output driver is disabled and the pin drives a logic 0. In expanded multiplexed mode, the E clock is always driven because IRV/NE only affects the internal read visibility function. Applications which are noise-sensitive should make every attempt to operate in single-chip or bootstrap mode and turn off the E clock. This will be especially helpful, since the address and data bus drivers will also substantially reduce high-frequency emissions since they are not switching as rapidly as they do in expanded or special test mode.

Noise-Sensitive Applications

Applications which are noise sensitive and require large external memories should take advantage of the ability to switch modes.

NOTE: *Some devices only allow the MDA bit to be written while operating in one of the special modes (special test or special bootstrap), so be sure to research the ability to change modes before using this example.*

For example, an application with external memory may operate normally in special test mode. However, when analog samples are acquired, the code jumps to an internal memory resource and changes to bootstrap mode, so that the address and data bus drivers will not switch. If the not E clock function is also enabled, then noise emission will be greatly reduced. Remember that only one write is allowed to the IRV/NE bit, so when returning to an expanded mode be careful that no bus conflicts will occur.

Table 5 and **Table 6** show devices where the IRV/NE bit is writable multiple times in special operating modes.

Table 5. Devices with IRV/NE Described in Table 6

Masked ROM EEPROM	Masked ROM, no EEPROM	No ROM, EEPROM	No ROM, N0 EEPROM	EPROM
MC68HC11K4	MC68HC11K3	MC68HC11K1	MC68HC11K0	MC68HC711K4
MC68HC11KA4	MC68HC11KA3	MC68HC11KA1	MC68HC11KA0	MC68HC711KA4
MC68HC11KA2	—	—	—	MC68HC711KA2
—	MC68HC711M2	—	—	MC68HC711M2
MC68HC11N4	—	—	—	MC68HC711N4
—	MC68HC11P2	—	—	MC68HC711P2

Table 6. IRV/NE Bit Functionality for Parts in Table 6

Mode	IRVNE out of reset	E clock out of reset	IRV out of reset	IRVNE affects only	IRVNE an be written
Single-chip	**0**	**On**	**Off**	**E clock**	**Once**
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	N/A	Anytime
Special Test	1	On	On	E clock	Anytime

The ability to write to the IRV/NE multiple times will help reduce the amount of logic necessary in expanded operating modes. Some users may want to turn off the E clock to reduce noise emission. However, they do not want the extra burden of complete decoding of the address space to prevent bus conflicts. These users will be able to turn the E clock back on when the critical operation is complete, so that returning to an expanded mode will disable the internal read visibility mechanism (IRV/NE = 0).

The information in these tables conflict with some technical data books and other distributed technical documentation. The tables in this engineering bulletin were built after empirically testing a member of each device series.

Conclusion

Careful planning and use of the IRV/NE bit can be helpful in noise-sensitive applications. Software designers should take care to make every effort to reduce the inherent noise in the system at the critical time. This certainly helps hardware designers who must still remember to decouple and filter at all times.

The net effect of your teamwork against noise may be increased accuracy of your analog subsystem at no extra system cost.

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