

# PLL Lock Detection on the HC12 D-Family

By **Darci Ernst**  
Applications Engineering  
Austin, Texas

---

## Introduction / Background

All HC12 D-Family of microcontrollers have PLL (phase-locked loop) clock generation circuitry. This allows the external resonator (crystal, ceramic, etc.) or other external clock source to be multiplied up to a higher internal frequency.

This has many advantages such as:

- Software controllable bus frequency
- Ability to scale the bus frequency for lower power consumption when needed
- Ability to run in LHM (limp home mode) when external clock source is lost
- Improved EMC due to jitter spreading the spectrum

This product incorporates SuperFlash<sup>®</sup> technology licensed from SST.

© Freescale Semiconductor, Inc., 2004. All rights reserved.

## Detailed Description

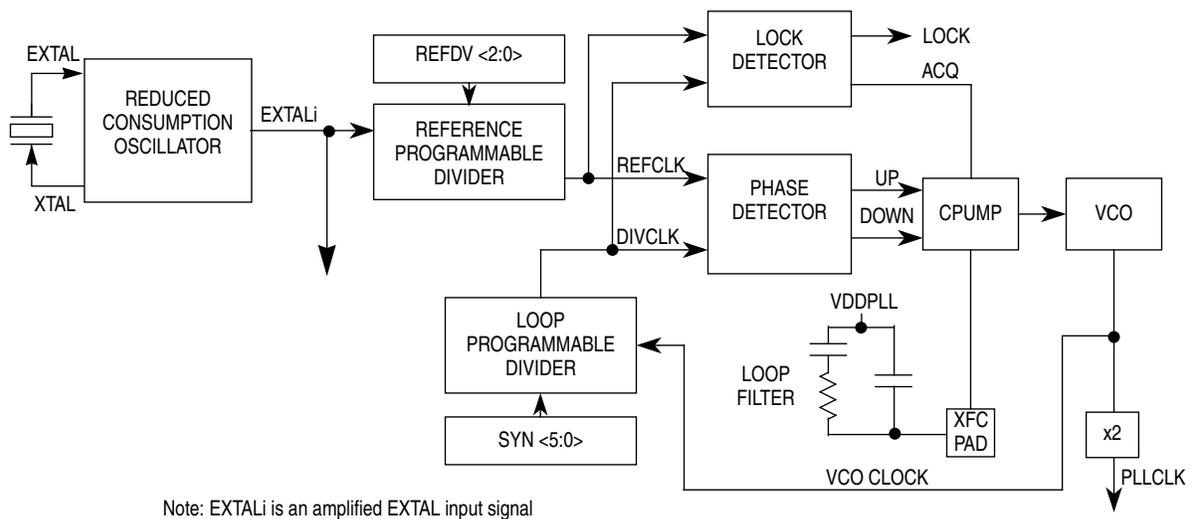
The PLL contains control registers to specify the “divide by” and “multiply by” values, and to select auto or manual mode. It also has status registers that indicate how near the PLL is to the desired frequency, bandwidth control, and limp home mode status.

In automatic bandwidth control (default from reset), the ACQ status bits indicates whether the PLL is in acquisition or tracking mode.

- Acquisition mode is where the PLL is trying to acquire the reference frequency. The PLL starts up in acquisition mode and will stay in this mode until the detected PLL error is within 3 to 4% of its targeted frequency, at which time the device will enter tracking mode. The detected PLL error must be off by more than 6 to 8% for it to return to acquisition mode.
- When in tracking mode, the detected PLL error is within 8% of the desired frequency and the PLL is attempting to track the reference frequency.

One of the other status bits is the LOCK bit, which indicates that the PLL is locked. The LOCK bit will be set when the detected PLL error is within 0 to 1.5% of its target frequency. After the part is in lock, the detected PLL error must be more than 0.5 to 2.5% for it to clear the LOCK bit.

The status bit LOCKIF indicates a change in the state of the LOCK bit. If that interrupt is enabled, the application software can respond to the LOCKIF bit and read the state of the LOCK bit to determine which way it changed.



## Description of Lock/Unlock Detect Circuitry

On the HC12, the lock detection circuitry consists of two counters and some comparators.

- One counter counts REFCLK, which is the reference clock (EXTALi) divided by (REFDV + 1)
- The other counter counts DIVCLK, which is the output of the VCO (voltage controlled oscillator) divided by the multiplier value (SYNR + 1)

Ideally, the counters would always be equal, indicating perfect tracking, which would result in a constant XFC voltage. In general however, tracking will not be perfect because the PLL control loop contains analog components, which allow some variation in the clock pulses. The voltage on the XFC pin (output from phase error amp) directly controls the VCO frequency. Therefore, any noise on XFC will directly modulate the VCO frequency, resulting in some clock jitter. Also, any leakage into or out of the XFC pin will pull the phase relationship between the two clocks. Due to the nature of the PLL design, if a proper XFC filter is used, the VCO frequency error will average very close to 0 over the long term because of positive and negative variations.

On the HC12 Family, the lock detector operation is as follows. The REFCLK (EXTALi divided by (REFDV + 1)) is used to open “a window,” or in other words enable the counter for the DIVCLK (VCO divided by (SYNR + 1)). In this way, the two clocks can be compared within that window. When the MCU is in acquisition mode, it uses a 5-bit counter (0 to 31). When the MCU is in tracking mode, it uses a 7-bit counter (0 to 127). [Table 1](#) provides the conditions necessary to change the states of the ACQ or LOCK bits and conditions.

**Table 1. Conditions Necessary to Change States of ACQ or LOCK**

Operation	Action	ACQ	LOCK
Initial state	None	1	0
27 or 28 VCO clocks per 28 reference clocks	Enter tracking, switch to divide by 128	0	0
111 or 112 VCO clocks per 112 reference clocks	Enter lock	0	1
<110 or >113 VCO clocks per 112 reference clocks	Exit lock	0	0
<104 or >119 VCO clocks per 112 reference clocks	Exit tracking, re-enter acquisition	1	0

For example, in tracking mode, there is a window of 112 REFCLK (reference clocks). The lock-detection circuit uses the last few counts of the 7-bit counter to update the acquisition and lock bits and prepare for the next count cycle. The lock detector counts the DIVCLK (VCO clock divided by (SYNR + 1)) that occur within the window. If the VCO count is less than 110, or greater than 113, the LOCK bit is cleared. If the feedback counter is 111 or 112, the LOCK bit is set. If the feedback counter is exactly 110, or exactly 113, the LOCK bit status remains the same.

---

## Scenarios

Freescale Semiconductor is aware of three scenarios used in various customer applications:

- **Scenario 1: Noisy Environment** — Applications that use the “interrupt on change of LOCK state” but the “unlock” indication occurs unexpectedly.
- **Scenario 2: Wait for LOCK Bit** — Applications that wait on the LOCK bit when first setting up the PLL and the LOCK indication does not occur when it was expected.
- **Scenario 3: Write to PLL Registers** — Applications that get the LOCK bit before it was expected.

The first two scenarios are influenced by quantization, or phase error, which can cause error in the count between the REFCLK and the DIVCLK. If those two clocks are almost in sync (approximately 0 degrees of phase separation), then the counter may not count either the first or the last edge of the DIVCLK, causing it to be off by up to two counts. Normally, there is sufficient phase error to prevent this situation from occurring, but note that leakage on the XFC pin can greatly influence this phase relationship.

Therefore, if this phase relationship is at the worst location—in regard to the lock detection circuit—such that the two clocks (first and last) are exactly on top of each other, the DIVCLK counter can miss those two counts, causing it to be off by as many as two counts.

### Scenario 1: Noisy Environment

In a noisy environment, the count can be affected whenever the MCU sees the noise events. If the counter is off by three or more, there will be a loss-of-lock detection. As described above, the LOCK bit can indicate loss-of-lock when the PLL frequency is off by as little as one count. However, because the PLL adjusts on every clock cycle of the reference clock during this loss-of-lock indication, the PLL stays frequency-locked on the reference clock. The unexpected lock indication is a more sensitive unlock status detection than when there is no quantization error.

Most users do not interrupt on change of LOCK bit status. However, if it is desired, a subroutine can be written to determine what action should be taken. For example, the ACQ bit can be used to indicate whether the PLL is significantly off from the desired frequency (more than 3%). The ACQ bit can be read in the LOCKIF interrupt service routine in order to determine the appropriate course of action for the application.

### Scenario 2: Wait for LOCK Bit

**Scenario 2: Wait for LOCK Bit** is very closely related to **Scenario 1: Noisy Environment**, except that it occurs when the customer software is waiting for the LOCK bit to be set. If the PLL is already very stable, the lock detection circuit may not set the LOCK bit (due the quantization error). If the XFC filter values are such that the VCO is over dampened (resulting in no overshoot of target voltage) and the leakage on the XFC pin causes the quantization error, the lock detection circuit could theoretically never set the LOCK bit. Under these conditions, when starting up from power-on or writing to the REFDV or SYNRR, the VCO is usually ramping up and overshoots the desired frequency as it locks onto the reference frequency.

Users who use a time delay and do not use the LOCK bit are not affected. Users may implement software that deals with this scenario by other means, for example by doing a COP RESET. The reset forces the VCO to minimum speed, and the subsequent re-ramp of the VCO helps set the LOCK bit. The reset also can inject some noise, which can help reduce the quantization error. The only consequence is a longer than expected time before the LOCK bit is set.

### Scenario 3: Write to PLL Registers

When the PLL is already locked and the application writes to the REFDV or SYNR registers, it is necessary to wait before checking the LOCK bit. Because the lock detection circuit has a period of 127 reference clocks and it occurs asynchronously to the application software write to REFDV or SYNR, there can be a delay before the LOCK bit reflects the current status.

Users should wait for a minimum of 128 reference clocks before checking the LOCK bit after writing to either the REFDV or the SYNR register. This wait time ensures that the lock detection circuit updates the lock bit to the current status.

If the XFC filter is properly sized, the MCU should still operate correctly, even if the wait for the 128 reference clocks is not implemented. This is because the bus frequency will ramp to the target frequency. Note that during this time, any timing-critical code could be off until the VCO is locked.

---

## Conclusion

If your system is already up and running, you should not need this document. This document is intended for the users who would like to make better use of the PLL lock/unlock feature in their system. Though the scenarios described in this document can seem problematic at first, the implementation of the PLL with the lock/unlock circuit is not difficult at the system level when the circuit is understood.

This page is intentionally blank

This page is intentionally blank

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **E-mail:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2004. All rights reserved.