HC912D60A / HC912Dx128A 0.5µ Microcontrollers

Mask sets 2K38K, 1L02H/2L02H/3L02H & K91D, 0L05H/1L05H/2L05H

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This document explains certain characteristics of the following devices:

- HC912D60A mask sets 2K38K from TSMC and 1L02H, 2L02H, and 3L02H from TSC6 (SND-FAB)
- HC912Dx128A mask sets K91D from TSMC and 0L05H, 1L05H, and 2L05H from TSC6 (SND-FAB)

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1 Introduction

As a result of an investigation into issues reported by customers and analysis of related application modules, Freescale has found that some units behave in a manner that may lead to these issues when the microcontroller is operated outside of its specification.

This document describes this behavior and tells customers how to avoid the conditions that give rise to the issue.

2 Issue Description

Some applications have encountered a situation where the microcontroller occasionally fails to restart when the power is cycled off and on, but V_{DD} fails to decay to zero volts within the cycle period, and toggling the reset pin does not recover the microcontroller.

3 Issue Cause

Freescale's analysis has determined that the cause of the issue is a disturbance of reset or residual voltage applied to the device, which may be caused by a combination of factors present on the application.

Such factors include bounce on the reset line and the improper decay of V_{DD} to zero volts. The impact of bounce on the reset line is heightened by the lower operating voltage during the power off cycle.

The diagram below illustrates one such situation whereby reset toggling features an unusual pulse that coincides with non-POR (power on reset) V_{DD} level, and the oscillator does not restart even after reset and V_{DD} are returned to 5V (device is locked-up).

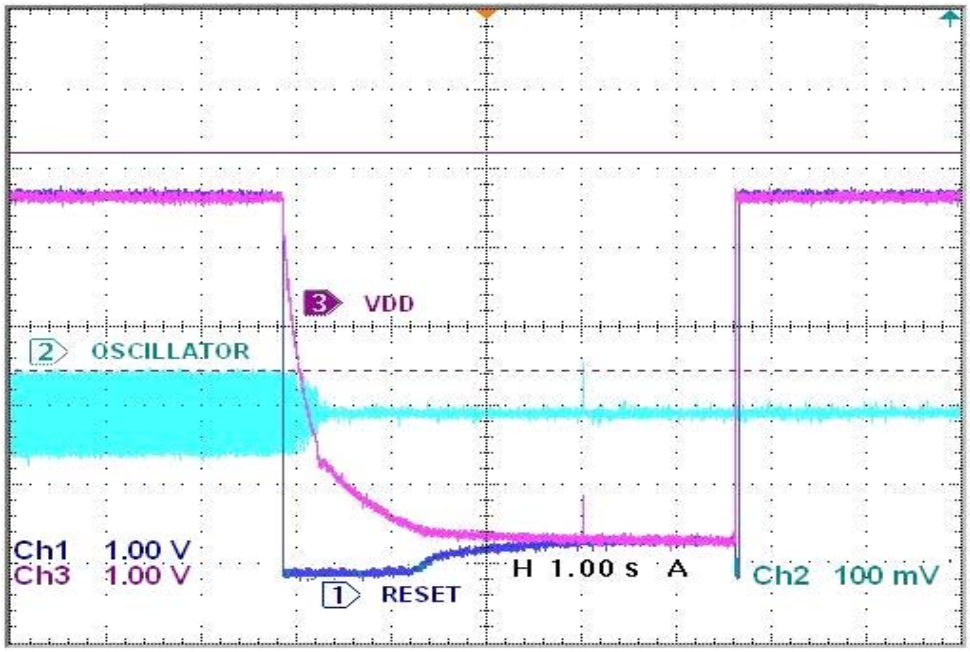

Figure 1. Reset Toggling Featuring an Unusual Pulse

As a result of these factors, the oscillator is disabled and prevented from being re-started, a situation similar to a stop mode.

After the device has entered into this locked-up state, toggling the external reset pin does not restart the oscillator, as it would following a software stop instruction.

This situation requires a power on reset to recover the device.

Freescale notes no fault with the external reset, which is designed to reset the device while V_{DD} is within the operational range.

If the voltage drops low enough to induce POR, then this issue does not arise.

4 Freescale Recommendation

Applications should be reviewed to determine whether the power down cycle shows any indication of fluctuating low voltages or unstable behavior on the reset.

It is recommended that whenever V_{DD} is powered off, the application should be arranged to allow V_{DD} to decay to 0.1V or less, to guarantee POR operation, before a clean rise back to the recommended operating voltage.

5 POR Clarification

Device specification 9.6.1 Power-On Reset states “The POR circuit only initializes internal circuitry during cold starts and cannot be used to force a reset as system voltage drops.” Cold start is conventionally understood to be 0V, but for practical application purposes, Freescale recommends a voltage level lower than 100mV.

NOTE

HC12 0.5υ family of parts is considered to be of older technology and Freescale does not plan on any design revisions of these devices. Newer versions of the HC12 parts exist in the HCS12 family of products. The issue addressed in this document does not apply to the HCS12 family of products because the reset circuitry is a different design.

6 Additional Notes: HC12 POR Description

These notes are provided to help with the understanding of the POR circuit.

- Architecture was designed in 1990.
- Circuit uses SR latch with cap to V_{DD} on S input and cap to V_{SS} on R input, as described in the figure below:

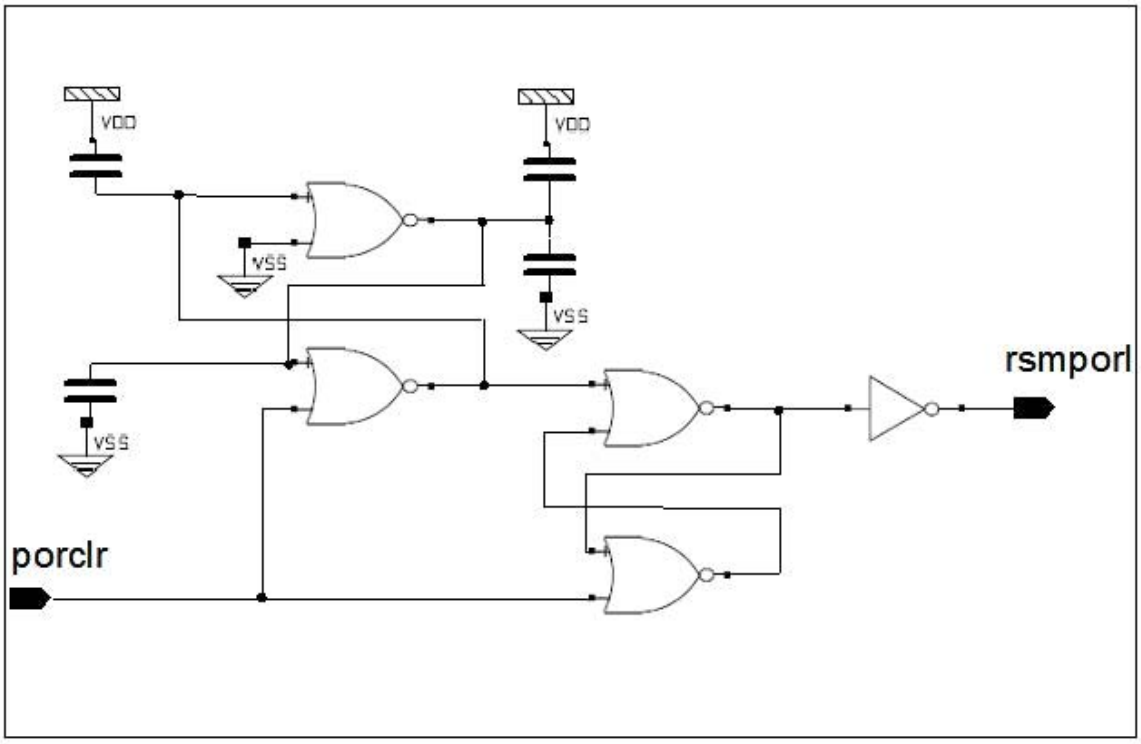

Figure 2. SR Latch with Cap to VDD on S Input and Cap to V_{SS} on R Input

- When V_{DD} ramps, a positive voltage difference in favor of the S input is required to initialize the POR circuit.
- When V_{DD} powers down, the capacitor will start to discharge. The voltage on the S input must discharge to a sufficiently low value with respect to the R input to ensure that the latch resets before the next V_{DD} ramp. This action re-arms the POR circuit.
- The POR circuit is not a forced circuit. It uses charging and discharging capacitors. Therefore the re-arm voltage of the circuit is not an absolute, and it is impossible to specify an exact re-arm voltage.
- To guarantee a proper recovery, V_{DD} must go to 0.1V or below to margin against process variations affecting switch-points and discharge currents.

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