Freescale Semiconductor
Engineering Bulletin

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56F8300 ADC Clock Considerations

Introduction

This bulletin explains how to ensure proper operation in 56F834x, 56F835x, or 56F836x devices with multiple dual analog-to-digital converters (ADCs) that share a voltage reference.

Details

Dual ADCs in many 56F8300 devices (56F834x, 56F835x, or 56F836x) share a voltage reference and each sample the reference voltage at every half-ADC clock, even when the digital wrapper prevents the ADC from running. The ADCs' independent accesses to the shared reference voltage produces inconsistent results. In this situation, an ADC can capture data which appears to have bi-modal distribution of values due to disturbance of the common reference voltage by other channels. When ADC channels operate off a common ADC clock, this bi-modal distribution is not seen, as all samples occur concurrently.

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ADC Clocks

At start-up, or when clocks have been re-enabled by PCE bits:

- The ADC clocks are in sync
- The analog core is capturing data
- The digital wrapper is ignoring data because the ADCs are stopped

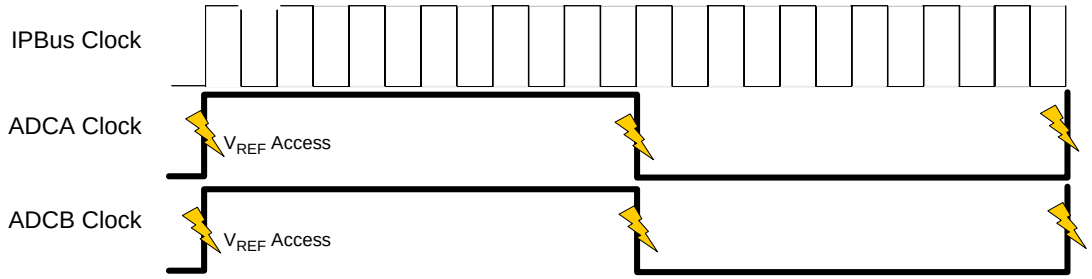


Figure 1 ADC Clock at Start-up or After Re-enabling

When the ADCA clock is started by writing to the START bit:

- The ADCA clock is resynchronized to the next IPBus clock
- The ADCB clock doesn't change
- The clocks are now out of sync

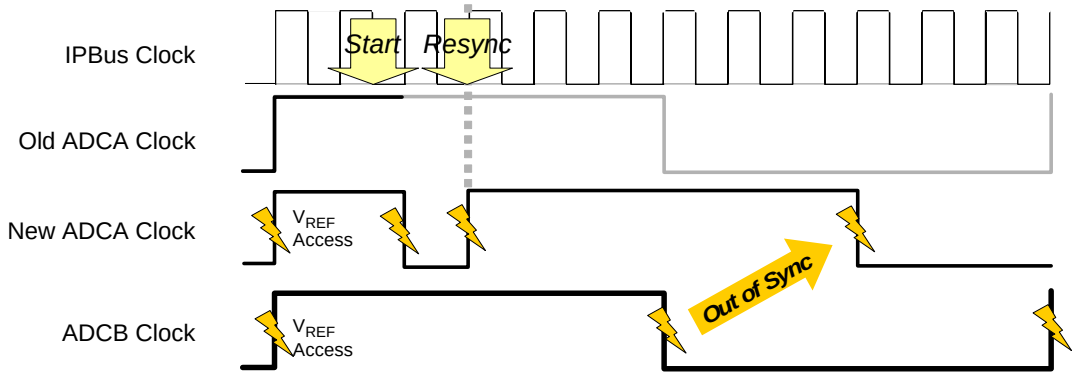


Figure 2 When ADCA Clock Is Started by Writing to the START Bit

Solutions

When using software to start ADC scans:

- Use only one ADC

  or

- If both ADCs are needed, use the auto power down (APD) mode and run only one ADC at a time

Ensure simultaneous voltage references

- Align ADC clocks
  - Use a common ADC clock divider
  - Trigger ADCs using a quad timer
  - Ensure the trigger occurs when the ADC clocks are either in phase or 180 degrees out of phase
  - The trigger rate should be a sub-multiple of the ADC clock rate so the trigger period is an even number of ADC clock periods

Common Questions

Q: Does this mean a system can't operate the ADCs at different sample rates?

A: No. ADCs must have a common clock rate, but may trigger at any sampling rate, as long as clock edges remain aligned.

Points to remember:

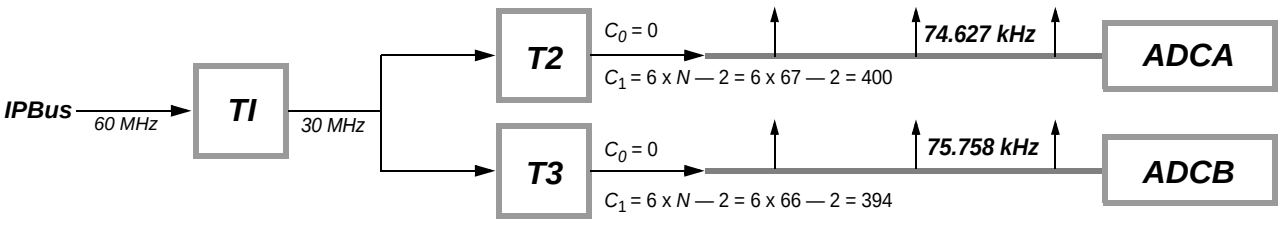
- Trigger ADCs from a common timer
- Use only samples rates that are submultiples of the ADC clock

Example:

$$\text{Common ADC clock}: f_{ADC} = IPBus/12 = 5\ \text{MHz}$$

$$\text{ADC A}: f_{ADC}/67 = 74.627\ \text{KHz} \Rightarrow \Pi_{ADCA} = 12 \cdot 67 = 804\ \text{sys clocks}$$

$$\text{ADC B}: f_{ADC}/66 = 75.758\ \text{KHz} \Rightarrow \Pi_{ADCB} = 12 \cdot 66 = 792\ \text{sys clocks}$$



Q: Does this work around affect PWM-ADC synchronization?

A: Yes, but the effect is small.

- Phase adjustments must maintain clock edge alignment
  - PWM reload rates should be identical
  - Phase adjustments must be in multiples of one-half the ADC clock (6 sys clock), implying a 6x coarser adjustment of PWM-ADC phasing
- The phase difference between PWM clocks and PWM reload pulse should be measured by the timer after set-up
  - Include phase delta in timer 2 and timer 3 values

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